National Semiconductor

400034

National Application Specific Analog Products Databook

Audio
Automotive
Video
Special Functions

APPLICATION SPECIFIC ANALOG PRODUCTS

DATABOOK

1995 Edition

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ADC0816 8-Bit μP Compatible A/D Converter with 16-Channel Multiplexer ..... Section 2 Data Acquisition
ADC0817 8-Bit μP Compatible A/D Converter with 16-Channel Multiplexer ..... Section 2 Data Acquisition
ADC0819 8-Bit Serial I/O A/D Converter with 19-Channel Multiplexer ..... Section 2 Data Acquisition
ADC0820 8-Bit High Speed μP Compatible A/D Converter with Track/Hold Function ..... Section 2 Data Acquisition
ADC0831 8-Bit Serial I/O A/D Converter with Multiplexer Options ..... Section 2 Data Acquisition
ADC0832 8-Bit Serial I/O A/D Converter with Multiplexer Options ..... Section 2 Data Acquisition
ADC0833 8-Bit Serial I/O A/D Converter with 4-Channel Multiplexer ..... Section 2 Data Acquisition
ADC0834 8-Bit Serial I/O A/D Converter with Multiplexer Options ..... Section 2 Data Acquisition
ADC0838 8-Bit Serial I/O A/D Converter with Multiplexer Options ..... Section 2 Data Acquisition
ADC0841 8-Bit μP Compatible A/D Converter ..... Section 2 Data Acquisition
ADC0844 8-Bit μP Compatible A/D Converter with Multiplexer Options ..... Section 2 Data Acquisition
ADC0848 8-Bit μP Compatible A/D Converter with Multiplexer Options ..... Section 2 Data Acquisition
ADC0851 8-Bit Analog Data Acquisition and Monitoring System ..... Section 1 Data Acquisition
ADC0852 Multiplexed Comparator with 8-Bit Reference Divider ..... Section 2 Data Acquisition
ADC0854 Multiplexed Comparator with 8-Bit Reference Divider ..... Section 2 Data Acquisition
ADC0858 8-Bit Analog Data Acquisition and Monitoring System ..... Section 1 Data Acquisition
ADC08031 8-Bit High-Speed Serial I/O A/D Converter with Multiplexer Options, Voltage Reference, and Track/Hold Function ..... Section 2 Data Acquisition
ADC08032 8-Bit High-Speed Serial I/O A/D Converter with Multiplexer Options, Voltage Reference, and Track/Hold Function ..... Section 2 Data Acquisition
ADC08034 8-Bit High-Speed Serial I/O A/D Converter with Multiplexer Options, Voltage Reference, and Track/Hold Function ..... Section 2 Data Acquisition
ADC08038 8-Bit High-Speed Serial I/O A/D Converter with Multiplexer Options, Voltage Reference, and Track/Hold Function ..... Section 2 Data Acquisition
ADC08061 500 ns A/D Converter with S/H Function and Input Multiplexer ..... Section 2 Data Acquisition
ADC08062 500 ns A/D Converter with S/H Function and Input Multiplexer ..... Section 2 Data Acquisition

Additional Available Linear Devices (Continued)

ADC08131 8-Bit High-Speed Serial I/O A/D Converter with Multiplexer Options, Voltage Reference, and Track/Hold Function ..... Section 2 Data Acquisition
ADC08134 8-Bit High-Speed Serial I/O A/D Converter with Multiplexer Options, Voltage Reference, and Track/Hold Function ..... Section 2 Data Acquisition
ADC08138 8-Bit High-Speed Serial I/O A/D Converter with Multiplexer Options, Voltage Reference, and Track/Hold Function ..... Section 2 Data Acquisition
ADC08161 500 ns A/D Converter with S/H Function and 2.5V Bandgap Reference ..... Section 2 Data Acquisition
ADC08231 8-Bit 2 μs Serial I/O A/D Converter with MUX, Reference, and Track/Hold ..... Section 2 Data Acquisition
ADC08234 8-Bit 2 μs Serial I/O A/D Converter with MUX, Reference, and Track/Hold ..... Section 2 Data Acquisition
ADC08238 8-Bit 2 μs Serial I/O A/D Converter with MUX, Reference, and Track/Hold ..... Section 2 Data Acquisition
ADC12H030 Self-Calibrating 12-Bit Plus Sign Serial I/O A/D Converter with MUX and Sample/Hold ..... Section 2 Data Acquisition
ADC12H032 Self-Calibrating 12-Bit Plus Sign Serial I/O A/D Converter with MUX and Sample/Hold ..... Section 2 Data Acquisition
ADC12H034 Self-Calibrating 12-Bit Plus Sign Serial I/O A/D Converter with MUX and Sample/Hold ..... Section 2 Data Acquisition
ADC12H038 Self-Calibrating 12-Bit Plus Sign Serial I/O A/D Converter with MUX and Sample/Hold ..... Section 2 Data Acquisition
ADC12L030 3.3V Self-Calibrating 12-Bit Plus Sign Serial I/O A/D Converter with MUX and Sample/Hold ..... Section 2 Data Acquisition
ADC12L032 3.3V Self-Calibrating 12-Bit Plus Sign Serial I/O A/D Converter with MUX and Sample/Hold ..... Section 2 Data Acquisition
ADC12L034 3.3V Self-Calibrating 12-Bit Plus Sign Serial I/O A/D Converter with MUX and Sample/Hold ..... Section 2 Data Acquisition
ADC12L038 3.3V Self-Calibrating 12-Bit Plus Sign Serial I/O A/D Converter with MUX and Sample/Hold ..... Section 2 Data Acquisition
ADC1001 10-Bit μP Compatible A/D Converter ..... Section 2 Data Acquisition
ADC1005 10-Bit μP Compatible A/D Converter ..... Section 2 Data Acquisition
ADC1031 10-Bit Serial I/O A/D Converter with Analog Multiplexer and Track/Hold Function ..... Section 2 Data Acquisition
ADC1034 10-Bit Serial I/O A/D Converter with Analog Multiplexer and Track/Hold Function ..... Section 2 Data Acquisition
ADC1038 10-Bit Serial I/O A/D Converter with Analog Multiplexer and Track/Hold Function ..... Section 2 Data Acquisition
ADC1061 10-Bit High-Speed μP-Compatible A/D Converter with Track/Hold Function ..... Section 2 Data Acquisition
ADC1205 12-Bit Plus Sign μP Compatible A/D Converter ..... Section 2 Data Acquisition
ADC1225 12-Bit Plus Sign μP Compatible A/D Converter ..... Section 2 Data Acquisition
ADC1241 Self-Calibrating 12-Bit Plus Sign μP-Compatible A/D Converter with Sample/Hold ..... Section 2 Data Acquisition
ADC1242 12-Bit Plus Sign Sampling A/D Converter ..... Section 2 Data Acquisition
ADC1251 Self-Calibrating 12-Bit Plus Sign A/D Converter with Sample/Hold ..... Section 2 Data Acquisition

Additional Available Linear Devices (Continued)

ADC10061 10-Bit 600 ns A/D Converter with Input Multiplexer and Sample/Hold ..... Section 2 Data Acquisition
ADC10062 10-Bit 600 ns A/D Converter with Input Multiplexer and Sample/Hold ..... Section 2 Data Acquisition
ADC10064 10-Bit 600 ns A/D Converter with Input Multiplexer and Sample/Hold ..... Section 2 Data Acquisition
ADC10154 10-Bit Plus Sign 4 μs ADC with 4- or 8-Channel MUX, Track/Hold and Reference ..... Section 2 Data Acquisition
ADC10158 10-Bit Plus Sign 4 μs ADC with 4- or 8-Channel MUX, Track/Hold and Reference ..... Section 2 Data Acquisition
ADC10461 10-Bit 600 ns A/D Converter with Input Multiplexer and Sample/Hold ..... Section 2 Data Acquisition
ADC10462 10-Bit 600 ns A/D Converter with Input Multiplexer and Sample/Hold ..... Section 2 Data Acquisition
ADC10464 10-Bit 600 ns A/D Converter with Input Multiplexer and Sample/Hold ..... Section 2 Data Acquisition
ADC10662 10-Bit 360 ns A/D Converter with Input Multiplexer and Sample/Hold ..... Section 2 Data Acquisition
ADC10664 10-Bit 360 ns A/D Converter with Input Multiplexer and Sample/Hold ..... Section 2 Data Acquisition
ADC10731 10-Bit Plus Sign Serial I/O A/D Converter with MUX, Sample/Hold and Reference ..... Section 2 Data Acquisition
ADC10732 10-Bit Plus Sign Serial I/O A/D Converter with MUX, Sample/Hold and Reference ..... Section 2 Data Acquisition
ADC10734 10-Bit Plus Sign Serial I/O A/D Converter with MUX, Sample/Hold and Reference ..... Section 2 Data Acquisition
ADC10738 10-Bit Plus Sign Serial I/O A/D Converter with MUX, Sample/Hold and Reference ..... Section 2 Data Acquisition
ADC10831 10-Bit Plus Sign Serial I/O A/D Converter with MUX, Sample/Hold and Reference ..... Section 2 Data Acquisition
ADC10832 10-Bit Plus Sign Serial I/O A/D Converter with MUX, Sample/Hold and Reference ..... Section 2 Data Acquisition
ADC10834 10-Bit Plus Sign Serial I/O A/D Converter with MUX, Sample/Hold and Reference ..... Section 2 Data Acquisition
ADC10838 10-Bit Plus Sign Serial I/O A/D Converter with MUX, Sample/Hold and Reference ..... Section 2 Data Acquisition
ADC12030 Self-Calibrating 12-Bit Plus Sign Serial I/O A/D Converter with MUX and Sample/Hold ..... Section 2 Data Acquisition
ADC12032 Self-Calibrating 12-Bit Plus Sign Serial I/O A/D Converter with MUX and Sample/Hold ..... Section 2 Data Acquisition
ADC12034 Self-Calibrating 12-Bit Plus Sign Serial I/O A/D Converter with MUX and Sample/Hold ..... Section 2 Data Acquisition
ADC12038 Self-Calibrating 12-Bit Plus Sign Serial I/O A/D Converter with MUX and Sample/Hold ..... Section 2 Data Acquisition
ADC12062 12-Bit, 1 MHz, 75 mW A/D Converter with Input Multiplexer and Sample/Hold ..... Section 2 Data Acquisition
ADC12130 Self-Calibrating 12-Bit Plus Sign Serial I/O A/D Converter with MUX and Sample/Hold ..... Section 2 Data Acquisition
ADC12132 Self-Calibrating 12-Bit Plus Sign Serial I/O A/D Converter with MUX and Sample/Hold ..... Section 2 Data Acquisition

Additional Available Linear Devices (Continued)

ADC12138 Self-Calibrating 12-Bit Plus Sign Serial I/O A/D Converter with MUX and Sample/Hold ..... Section 2 Data Acquisition
ADC12441 Dynamically-Tested Self-Calibrating 12-Bit Plus Sign A/D Converter with Sample/Hold ..... Section 2 Data Acquisition
ADC12451 Dynamically-Tested Self-Calibrating 12-Bit Plus Sign A/D Converter with Sample/Hold ..... Section 2 Data Acquisition
ADC12662 12-Bit, 1.5 MHz, 200 mW A/D Converter with Input Multiplexer and Sample/Hold ..... Section 2 Data Acquisition
ADC16071 16-Bit Delta-Sigma 192 ks/s Analog-to-Digital Converter .. Section 2 Data Acquisition
ADC16471 16-Bit Delta-Sigma 192 ks/s Analog-to-Digital Converter .. Section 2 Data Acquisition
AH0014 Dual DPDT-TTL/DTL Compatible MOS Analog Switch ..... Section 8 Data Acquisition
AH0015 Quad SPST-TTL/DTL Compatible MOS Analog Switch ..... Section 8 Data Acquisition
AH0019 Dual DPST-TTL/DTL Compatible MOS Analog Switch ..... Section 8 Data Acquisition
AH5010 Monolithic Analog Current Switch ..... Section 8 Data Acquisition
AH5011 Monolithic Analog Current Switch ..... Section 8 Data Acquisition
AH5012 Monolithic Analog Current Switch ..... Section 8 Data Acquisition
AH5020C Monolithic Analog Current Switch ..... Section 8 Data Acquisition
AN-450 Small Outline (SO) Package Surface Mounting Methods—Parameters and Their Effect on Product Reliability ..... Section 9 Data Acquisition
AN-450 Small Outline (SO) Package Surface Mounting Methods—Parameters and Their Effect on Product Reliability ..... Section 5 Power ICs
AN-450 Small Outline (SO) Package Surface Mounting Methods—Parameters and Their Effect on Product Reliability ..... Section 6 Operational Amplifiers
Board Mount of Surface Mount Components ..... Section 6 Operational Amplifiers
Board Mount of Surface Mount Components ..... Section 5 Power ICs
Board Mount of Surface Mount Components ..... Section 9 Data Acquisition
DAC0800 8-Bit D/A Converter ..... Section 3 Data Acquisition
DAC0801 8-Bit D/A Converter ..... Section 3 Data Acquisition
DAC0802 8-Bit D/A Converter ..... Section 3 Data Acquisition
DAC0806 8-Bit D/A Converter ..... Section 3 Data Acquisition
DAC0807 8-Bit D/A Converter ..... Section 3 Data Acquisition
DAC0808 8-Bit D/A Converter ..... Section 3 Data Acquisition
DAC0830 8-Bit μP Compatible Double-Buffered D/A Converter ..... Section 3 Data Acquisition
DAC0831 8-Bit μP Compatible Double-Buffered D/A Converter ..... Section 3 Data Acquisition
DAC0832 8-Bit μP Compatible Double-Buffered D/A Converter ..... Section 3 Data Acquisition
DAC0854 Quad 8-Bit Voltage-Output Serial D/A Converter with Readback ..... Section 3 Data Acquisition
DAC0890 Dual 8-Bit μP-Compatible D/A Converter ..... Section 3 Data Acquisition
DAC1006 μP Compatible, Double-Buffered D/A Converter ..... Section 3 Data Acquisition
DAC1007 μP Compatible, Double-Buffered D/A Converter ..... Section 3 Data Acquisition
DAC1008 μP Compatible, Double-Buffered D/A Converter ..... Section 3 Data Acquisition
DAC1020 10-Bit Binary Multiplying D/A Converter ..... Section 3 Data Acquisition
DAC1021 10-Bit Binary Multiplying D/A Converter ..... Section 3 Data Acquisition
DAC1022 10-Bit Binary Multiplying D/A Converter ..... Section 3 Data Acquisition
DAC1054 Quad 10-Bit Voltage-Output Serial D/A Converter with Readback ..... Section 3 Data Acquisition
DAC1208 12-Bit μP Compatible Double-Buffered D/A Converter ..... Section 3 Data Acquisition
DAC1209 12-Bit μP Compatible Double-Buffered D/A Converter ..... Section 3 Data Acquisition
DAC1210 12-Bit μP Compatible Double-Buffered D/A Converter ..... Section 3 Data Acquisition
DAC1218 12-Bit Binary Multiplying D/A Converter ..... Section 3 Data Acquisition
DAC1219 12-Bit Binary Multiplying D/A Converter ..... Section 3 Data Acquisition

Additional Available Linear Devices (Continued)

DAC1220 12-Bit Binary Multiplying D/A Converter	Section 3	Data Acquisition
DAC1222 12-Bit Binary Multiplying D/A Converter	Section 3	Data Acquisition
DAC1230 12-Bit μP Compatible Double-Buffered D/A Converter	Section 3	Data Acquisition
DAC1231 12-Bit μP Compatible Double-Buffered D/A Converter	Section 3	Data Acquisition
DAC1232 12-Bit μP Compatible Double-Buffered D/A Converter	Section 3	Data Acquisition
DH0006 Current Driver	Section 5	Operational Amplifiers
DH0034 High Speed Dual Level Translator	Section 5	Operational Amplifiers
DH0035 Pin Diode Driver	Section 5	Operational Amplifiers
Land Pattern Recommendations	Section 6	Operational Amplifiers
Land Pattern Recommendations	Section 5	Power ICs
Land Pattern Recommendations	Section 9	Data Acquisition
LF111 Voltage Comparator	Section 3	Operational Amplifiers
LF147 Wide Bandwidth Quad JFET Input Operational Amplifier	Section 1	Operational Amplifiers
LF155 Series Monolithic JFET Input Operational Amplifiers	Section 1	Operational Amplifiers
LF156 Series Monolithic JFET Input Operational Amplifiers	Section 1	Operational Amplifiers
LF157 Series Monolithic JFET Input Operational Amplifiers	Section 1	Operational Amplifiers
LF198 Monolithic Sample and Hold Circuit	Section 6	Data Acquisition
LF211 Voltage Comparator	Section 3	Operational Amplifiers
LF298 Monolithic Sample and Hold Circuit	Section 6	Data Acquisition
LF311 Voltage Comparator	Section 3	Operational Amplifiers
LF347 Wide Bandwidth Quad JFET Input Operational Amplifier	Section 1	Operational Amplifiers
LF351 Wide Bandwidth JFET Input Operational Amplifier	Section 1	Operational Amplifiers
LF353 Wide Bandwidth Dual JFET Input Operational Amplifier	Section 1	Operational Amplifiers
LF398 Monolithic Sample and Hold Circuit	Section 6	Data Acquisition
LF411 Low Offset, Low Drift JFET Input Operational Amplifier	Section 1	Operational Amplifiers
LF412 Low Offset, Low Drift Dual JFET Operational Amplifier	Section 1	Operational Amplifiers
LF441 Low Power JFET Input Operational Amplifier	Section 1	Operational Amplifiers
LF442 Dual Low Power JFET Input Operational Amplifier	Section 1	Operational Amplifiers
LF444 Quad Low Power JFET Input Operational Amplifier	Section 1	Operational Amplifiers
LF451 Wide-Bandwidth JFET Input Operational Amplifier	Section 1	Operational Amplifiers
LF453 Wide-Bandwidth Dual JFET Input Operational Amplifier	Section 1	Operational Amplifiers
LF11201 Quad SPST JFET Analog Switch	Section 8	Data Acquisition
LF11202 Quad SPST JFET Analog Switch	Section 8	Data Acquisition
LF11331 Quad SPST JFET Analog Switch	Section 8	Data Acquisition
LF11332 Quad SPST JFET Analog Switch	Section 8	Data Acquisition
LF11333 Quad SPST JFET Analog Switch	Section 8	Data Acquisition
LF13006 Digital Gain Set	Section 6	Data Acquisition
LF13007 Digital Gain Set	Section 6	Data Acquisition
LF13201 Quad SPST JFET Analog Switch	Section 8	Data Acquisition
LF13202 Quad SPST JFET Analog Switch	Section 8	Data Acquisition
LF13331 Quad SPST JFET Analog Switch	Section 8	Data Acquisition
LF13332 Quad SPST JFET Analog Switch	Section 8	Data Acquisition
LF13333 Quad SPST JFET Analog Switch	Section 8	Data Acquisition
LF13508 8-Channel Analog Multiplexer	Section 8	Data Acquisition
LF13509 4-Channel Differential Analog Multiplexer	Section 8	Data Acquisition
LH0002 Buffer	Section 2	Operational Amplifiers
LH0003 Wide Bandwidth Operational Amplifier	Section 1	Operational Amplifiers
LH0004 High Voltage Operational Amplifier	Section 1	Operational Amplifiers
LH0021 1.0 Amp Power Operational Amplifier	Section 1	Operational Amplifiers
LH0024 High Slew Rate Operational Amplifier	Section 1	Operational Amplifiers
LH0032 Ultra Fast FET-Input Operational Amplifier	Section 1	Operational Amplifiers

Additional Available Linear Devices (Continued)

LH0033 Fast and Ultra Fast Buffers	Section 2	Operational Amplifiers
LH0041 0.2 Amp Power Operational Amplifier	Section 1	Operational Amplifiers
LH0042 Low Cost FET Operational Amplifier	Section 1	Operational Amplifiers
LH0063 Fast and Ultra Fast Buffers	Section 2	Operational Amplifiers
LH0070 Series BCD Buffered Reference	Section 4	Data Acquisition
LH0071 Series Precision Buffered Reference	Section 4	Data Acquisition
LH0094 Multifunction Converter	Section 5	Operational Amplifiers
LH0101 Power Operational Amplifier	Section 1	Operational Amplifiers
LH1605 5 Amp, High Efficiency Switching Regulator	Section 3	Power ICs
LH2111 Dual Voltage Comparator	Section 3	Operational Amplifiers
LH2311 Dual Voltage Comparator	Section 3	Operational Amplifiers
LH4001 Wideband Current Buffer	Section 2	Operational Amplifiers
LH4002 Wideband Video Buffer	Section 2	Operational Amplifiers
LM10 Operational Amplifier and Voltage Reference	Section 1	Operational Amplifiers
LM12 80W Operational Amplifier	Section 4	Power ICs
LM12H454 12-Bit + Sign Data Acquisition System with Self-Calibration	Section 1	Data Acquisition
LM12H458 12-Bit + Sign Data Acquisition System with Self-Calibration	Section 1	Data Acquisition
LM12L438 12-Bit + Sign Data Acquisition System with Serial I/O and Self-Calibration	Section 1	Data Acquisition
LM12L454 12-Bit + Sign Data Acquisition System with Self-Calibration	Section 1	Data Acquisition
LM12L458 12-Bit + Sign Data Acquisition System with Self-Calibration	Section 1	Data Acquisition
LM34 Precision Fahrenheit Temperature Sensor	Section 5	Data Acquisition
LM35 Precision Centigrade Temperature Sensor	Section 5	Data Acquisition
LM45 SOT-23 Precision Centigrade Temperature Sensor	Section 5	Data Acquisition
LM50 Single Supply Precision Centigrade Temperature Sensor	Section 5	Data Acquisition
LM78LXX Series 3-Terminal Positive Regulators	Section 1	Power ICs
LM78MXX Series 3-Terminal Positive Regulator	Section 1	Power ICs
LM78S40 Universal Switching Regulator Subsystem	Section 3	Power ICs
LM78XX Series Voltage Regulators	Section 1	Power ICs
LM79LXXAC Series 3-Terminal Negative Regulator	Section 1	Power ICs
LM79MXX Series 3-Terminal Negative Regulators	Section 1	Power ICs
LM79XX Series 3-Terminal Negative Regulators	Section 1	Power ICs
LM101A Operational Amplifier	Section 1	Operational Amplifiers
LM102 Voltage Follower	Section 2	Operational Amplifiers
LM105 Voltage Regulator	Section 1	Power ICs
LM106 Voltage Comparator	Section 3	Operational Amplifiers
LM107 Operational Amplifier	Section 1	Operational Amplifiers
LM108 Operational Amplifier	Section 1	Operational Amplifiers
LM109 5-Volt Regulator	Section 1	Power ICs
LM110 Voltage Follower	Section 2	Operational Amplifiers
LM111 Voltage Comparator	Section 3	Operational Amplifiers
LM113 Reference Diode	Section 4	Data Acquisition
LM117 3-Terminal Adjustable Regulator	Section 1	Power ICs
LM117HV 3-Terminal Adjustable Regulator	Section 1	Power ICs
LM118 Operational Amplifier	Section 1	Operational Amplifiers
LM119 High Speed Dual Comparator	Section 3	Operational Amplifiers
LM120 Series 3-Terminal Negative Regulator	Section 1	Power ICs

Additional Available Linear Devices (Continued)

LM123 3-Amp, 5-Volt Positive Regulator	Section 1	Power ICs
LM124 Low Power Quad Operational Amplifier	Section 1	Operational Amplifiers
LM125 Dual Voltage Regulator	Section 1	Power ICs
LM129 Precision Reference	Section 4	Data Acquisition
LM131 Precision Voltage-to-Frequency Converter	Section 2	Data Acquisition
LM133 3-Amp Adjustable Negative Regulator	Section 1	Power ICs
LM134 3-Terminal Adjustable Current Source	Section 4	Data Acquisition
LM134 3-Terminal Adjustable Current Source	Section 5	Data Acquisition
LM135 Precision Temperature Sensor	Section 5	Data Acquisition
LM136-2.5V Reference Diode	Section 4	Data Acquisition
LM136-5.0V Reference Diode	Section 4	Data Acquisition
LM137 3-Terminal Adjustable Negative Regulator	Section 1	Power ICs
LM137HV 3-Terminal Adjustable Negative Regulator (High Voltage)	Section 1	Power ICs
LM138 5-Amp Adjustable Regulator	Section 1	Power ICs
LM139 Low Power Low Offset Voltage Quad Comparator	Section 3	Operational Amplifiers
LM140 Series 3-Terminal Positive Regulator	Section 1	Power ICs
LM140L Series 3-Terminal Positive Regulator	Section 1	Power ICs
LM143 High Voltage Operational Amplifier	Section 1	Operational Amplifiers
LM145 Negative 3-Amp Regulator	Section 1	Power ICs
LM146 Programmable Quad Operational Amplifier	Section 1	Operational Amplifiers
LM148 Quad 741 Operational Amplifier	Section 1	Operational Amplifiers
LM149 Wide Band Decompensated (A_V(MIN) = 5)	Section 1	Operational Amplifiers
LM150 3-Amp Adjustable Regulator	Section 1	Power ICs
LM158 Low Power Dual Operational Amplifier	Section 1	Operational Amplifiers
LM160 High Speed Differential Comparator	Section 3	Operational Amplifiers
LM161 High Speed Differential Comparator	Section 3	Operational Amplifiers
LM169 Precision Voltage Reference	Section 4	Data Acquisition
LM185 Adjustable Micropower Voltage Reference	Section 4	Data Acquisition
LM185-1.2 Micropower Voltage Reference Diode	Section 4	Data Acquisition
LM185-2.5 Micropower Voltage Reference Diode	Section 4	Data Acquisition
LM193 Low Power Low Offset Voltage Dual Comparator	Section 3	Operational Amplifiers
LM194 Supermatch Pair	Section 5	Operational Amplifiers
LM195 Ultra Reliable Power Transistor	Section 5	Operational Amplifiers
LM199 Precision Reference	Section 4	Data Acquisition
LM201A Operational Amplifier	Section 1	Operational Amplifiers
LM205 Voltage Regulator	Section 1	Power ICs
LM207 Operational Amplifier	Section 1	Operational Amplifiers
LM208 Operational Amplifier	Section 1	Operational Amplifiers
LM210 Voltage Follower	Section 2	Operational Amplifiers
LM211 Voltage Comparator	Section 3	Operational Amplifiers
LM218 Operational Amplifier	Section 1	Operational Amplifiers
LM219 High Speed Dual Comparator	Section 3	Operational Amplifiers
LM221 Precision Preamplifier	Section 1	Operational Amplifiers
LM224 Low Power Quad Operational Amplifier	Section 1	Operational Amplifiers
LM231 Precision Voltage-to-Frequency Converter	Section 2	Data Acquisition
LM234 3-Terminal Adjustable Current Source	Section 4	Data Acquisition
LM234 3-Terminal Adjustable Current Source	Section 5	Data Acquisition
LM235 Precision Temperature Sensor	Section 5	Data Acquisition
LM236-2.5V Reference Diode	Section 4	Data Acquisition
LM236-5.0V Reference Diode	Section 4	Data Acquisition
LM239 Low Power Low Offset Voltage Quad Comparator	Section 3	Operational Amplifiers

Additional Available Linear Devices (Continued)

LM246 Programmable Quad Operational Amplifier	Section 1	Operational Amplifiers
LM248 Quad 741 Operational Amplifier	Section 1	Operational Amplifiers
LM258 Low Power Dual Operational Amplifier	Section 1	Operational Amplifiers
LM261 High Speed Differential Comparator	Section 3	Operational Amplifiers
LM285 Adjustable Micropower Voltage Reference	Section 4	Data Acquisition
LM285-1.2 Micropower Voltage Reference Diode	Section 4	Data Acquisition
LM285-2.5 Micropower Voltage Reference Diode	Section 4	Data Acquisition
LM293 Low Power Low Offset Voltage Dual Comparator	Section 3	Operational Amplifiers
LM299 Precision Reference	Section 4	Data Acquisition
LM301A Operational Amplifier	Section 1	Operational Amplifiers
LM302 Voltage Follower	Section 2	Operational Amplifiers
LM305 Voltage Regulator	Section 1	Power ICs
LM306 Voltage Comparator	Section 3	Operational Amplifiers
LM307 Operational Amplifier	Section 1	Operational Amplifiers
LM308 Operational Amplifier	Section 1	Operational Amplifiers
LM309 5-Volt Regulator	Section 1	Power ICs
LM310 Voltage Follower	Section 2	Operational Amplifiers
LM311 Voltage Comparator	Section 3	Operational Amplifiers
LM313 Reference Diode	Section 4	Data Acquisition
LM317 3-Terminal Adjustable Regulator	Section 1	Power ICs
LM317HV 3-Terminal Adjustable Regulator	Section 1	Power ICs
LM317L 3-Terminal Adjustable Regulator	Section 1	Power ICs
LM318 Operational Amplifier	Section 1	Operational Amplifiers
LM319 High Speed Dual Comparator	Section 3	Operational Amplifiers
LM320 Series 3-Terminal Negative Regulator	Section 1	Power ICs
LM320L Series 3-Terminal Negative Regulator	Section 1	Power ICs
LM321 Precision Preamplifier	Section 1	Operational Amplifiers
LM323 3-Amp, 5-Volt Positive Regulator	Section 1	Power ICs
LM324 Low Power Quad Operational Amplifier	Section 1	Operational Amplifiers
LM325 Dual Voltage Regulator	Section 1	Power ICs
LM329 Precision Reference	Section 4	Data Acquisition
LM330 3-Terminal Positive Regulator	Section 2	Power ICs
LM331 Precision Voltage-to-Frequency Converter	Section 2	Data Acquisition
LM333 3-Amp Adjustable Negative Regulator	Section 1	Power ICs
LM334 3-Terminal Adjustable Current Source	Section 4	Data Acquisition
LM334 3-Terminal Adjustable Current Source	Section 5	Data Acquisition
LM335 Precision Temperature Sensor	Section 5	Data Acquisition
LM336-2.5V Reference Diode	Section 4	Data Acquisition
LM336-5.0V Reference Diode	Section 4	Data Acquisition
LM337 3-Terminal Adjustable Negative Regulator	Section 1	Power ICs
LM337HV 3-Terminal Adjustable Negative Regulator (High Voltage)	Section 1	Power ICs
LM337L 3-Terminal Adjustable Regulator	Section 1	Power ICs
LM338 5-Amp Adjustable Regulator	Section 1	Power ICs
LM339 Low Power Low Offset Voltage Quad Comparator	Section 3	Operational Amplifiers
LM340 Series 3-Terminal Positive Regulator	Section 1	Power ICs
LM340L Series 3-Terminal Positive Regulator	Section 1	Power ICs
LM341 Series 3-Terminal Positive Regulator	Section 1	Power ICs
LM343 High Voltage Operational Amplifier	Section 1	Operational Amplifiers
LM345 Negative 3-Amp Regulator	Section 1	Power ICs
LM346 Programmable Quad Operational Amplifier	Section 1	Operational Amplifiers
LM348 Quad 741 Operational Amplifier	Section 1	Operational Amplifiers

Additional Available Linear Devices (Continued)

LM349 Wide Band Decompensated (A_V(MIN) = 5) ..... Section 1 Operational Amplifiers
LM350 3-Amp Adjustable Regulator ..... Section 1 Power ICs
LM358 Low Power Dual Operational Amplifier ..... Section 1 Operational Amplifiers
LM359 Dual, High Speed, Programmable Current Mode (Norton) Amplifier ..... Section 1 Operational Amplifiers
LM360 High Speed Differential Comparator ..... Section 3 Operational Amplifiers
LM361 High Speed Differential Comparator ..... Section 3 Operational Amplifiers
LM368-2.5 Precision Voltage Reference ..... Section 4 Data Acquisition
LM368-5.0 Precision Voltage Reference ..... Section 4 Data Acquisition
LM368-10 Precision Voltage Reference ..... Section 4 Data Acquisition
LM369 Precision Voltage Reference ..... Section 4 Data Acquisition
LM376 Voltage Regulator ..... Section 1 Power ICs
LM385 Adjustable Micropower Voltage Reference ..... Section 4 Data Acquisition
LM385-1.2 Micropower Voltage Reference Diode ..... Section 4 Data Acquisition
LM385-2.5 Micropower Voltage Reference Diode ..... Section 4 Data Acquisition
LM392 Low Power Operational Amplifier/Voltage Comparator ..... Section 1 Operational Amplifiers
LM393 Low Power Low Offset Voltage Dual Comparator ..... Section 3 Operational Amplifiers
LM394 Supermatch Pair ..... Section 5 Operational Amplifiers
LM395 Ultra Reliable Power Transistor ..... Section 5 Operational Amplifiers
LM399 Precision Reference ..... Section 4 Data Acquisition
LM431A Adjustable Precision Zener Shunt Regulator ..... Section 3 Power ICs
LM611 Operational Amplifier and Adjustable Reference ..... Section 1 Operational Amplifiers
LM612 Dual-Channel Comparator and Reference ..... Section 3 Operational Amplifiers
LM613 Dual Operational Amplifier, Dual Comparator, and Adjustable Reference ..... Section 3 Operational Amplifiers
LM613 Dual Operational Amplifier, Dual Comparator, and Adjustable Reference ..... Section 1 Operational Amplifiers
LM614 Quad Operational Amplifier and Adjustable Reference ..... Section 1 Operational Amplifiers
LM615 Quad Comparator and Adjustable Reference ..... Section 3 Operational Amplifiers
LM628 Precision Motion Controller ..... Section 4 Power ICs
LM629 Precision Motion Controller ..... Section 4 Power ICs
LM675 Power Operational Amplifier ..... Section 1 Operational Amplifiers
LM709 Operational Amplifier ..... Section 1 Operational Amplifiers
LM710 Voltage Comparator ..... Section 3 Operational Amplifiers
LM723 Voltage Regulator ..... Section 1 Power ICs
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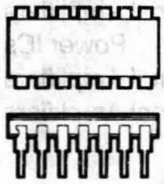
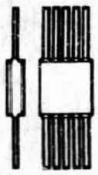
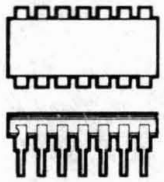
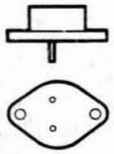
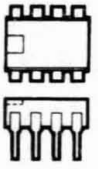
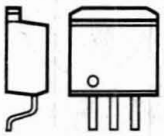
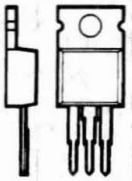
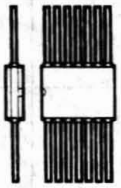
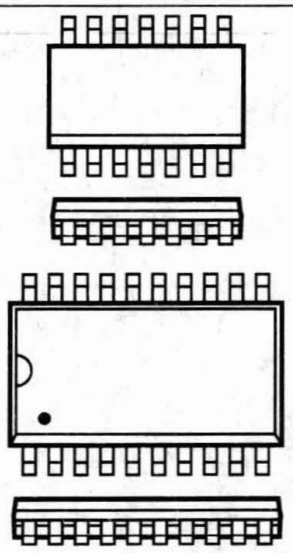
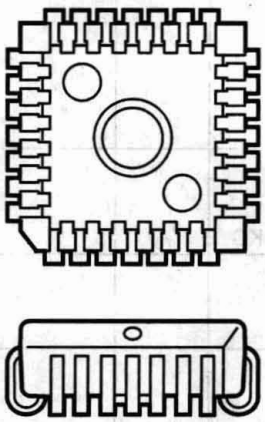
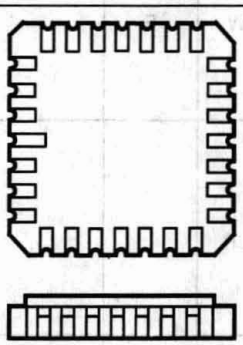
Industry Package Cross-Reference Guide

	NSC	NSC μA	Signetics	Motorola	TI	AMD	Sprague
 4/16 Lead Glass/Metal DIP	D	D	I	L		D	R
 Glass/Metal Flat Pack	F	F	Q	F	F, S	F	
TO-99, TO-100, TO-5	H	H	T, K, L, DB	G	L	H	
 8-, 14- and 16-Lead Low Temperature Ceramic DIP	J	R, D	F	U	J	D	H
 TO-3 (Steel)	K			KS			
TO-3 (Aluminum)	KC	K	DA	K	K		
 8-, 14- and 16-Lead Plastic DIP	N	T, P	N, V	P	P, N	P	A, B, M

	NSC	NSC μA	Signetics	Motorola	TI	AMD	Sprague
 TO-263 3- & 5-Lead	S						
 TO-220 3- & 5-Lead	T	U	U		KC		
TO-220 11-, 15- & 23-Lead	T						
 Low Temperature Glass Hermetic Flat Pack	W	F		F	W	F	
TO-92 (Plastic)	Z	W	S	P	LP		
 SO (Narrow Body)	M	S	S, D	D	D		L
(Wide Body)	WM				DW		LW
SOT-23 5-Lead	M5						

	NSC	NSC μA	Signetics	Motorola	TI	AMD	Sprague
 PCC	V	Q	A	FN	FN	L	EP
 LCC Leadless Ceramic Chip Carrier	E	L1	G	U	FK/ FG/FH	L	EK

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Audio Circuits

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Audio Power Amp Selection Guide

Supply Voltage	Part Number	Power (THD ≤ 1% Typ) Power Specified as Continuous RMS			Power (THD ≤ 10% Typ) Power Specified as Continuous RMS		
		4Ω	8Ω	16Ω	4Ω	8Ω	16Ω
3V	LM4860	0.6W	0.4W	0.2W	0.76W	0.5W	0.3W
	LM4861	0.6W	0.4W	0.2W	0.76W	0.5W	0.3W
	LM831	0.1W	0.07W	NA	0.15W	0.44W	NA
5V	LM4860	1.55W	1.15W	0.6W	1.9W	1.45W	0.85W
	LM4861	1.3W	1.15W	0.6W	1.75W	1.45W	0.85W
	LM4862	NA	0.350W	NA	NA	0.5W	NA
	LM4880	NA	0.200W	NA	NA	0.3W	NA
(V_S = 6V)	LM386	0.25W	0.25W	0.15W	0.32W	0.3W	0.2W
(V_S = 6V)	LM388	0.6W	0.35W	0.25W	0.8W	0.5W	0.35W
	LM831	0.25W	0.1W	NA	0.4W	0.44W	NA
(V_S = 6V)	LM1896	0.7W	0.45W	NA	1.1W	1.3W	NA
12V	LM380	1.5W	1W	NA	2.25W	1.5W	NA
	LM383	3.5W	NA	NA	4.7W	NA	NA
	LM384	NA	NA	NA	1.75W	NA	NA
	LM386	0.25W	0.6W	0.6W	0.35W	0.8W	0.95W
	LM1877	1.5W	1W	0.55W	1.75W	1.3W	0.75W
	LM2877	1.5W	1W	0.55W	1.75W	1.3W	0.75W
	LM2878	1.5W	1W	0.55W	2W	1.3W	0.75W
	LM2896	3W	2W	NA	4.25W	2.5W	NA
14V	LM380	2.5W	1.75W	NA	3.25W	2.25W	NA
	LM383	2W	NA	NA	5.5W	NA	NA
	LM384	NA	NA	NA	3.25W	NA	NA
(V_S = 16V)	LM386	NA	0.6W	1W	NA	0.8W	1.6W
	LM1877	2W	1.3W	0.85W	2.5W	1.75W	1W
	LM2877	2W	1.3W	0.85W	2.75W	1.75W	1W
	LM2878	2W	1.3W	0.85W	2.75W	1.75W	1W
	LM2879	NA	1.25W	NA	NA	2W	NA
20V & Above							
(V_S = 20V)	LM1877	2W	2W	NA	2.5W	3W	NA
(V_S = 20V)	LM2877	2.5W	3W	1.75W	3.7W	4.25W	2.3W
(V_S = 20V)	LM2878	NA	4W	NA	NA	4.75W	NA
(V_S = 28V)	LM2879	NA	7W	NA	NA	8W	NA
(V_S = 22V)	LM380	NA	4W	2.5W	NA	5W	3.25W
(V_S = 26V)	LM384	NA	5.5W	NA	2.5W	7W	5W
(V_S = ±40V)	LM391*	NA	80W*	NA	NA	NA	NA
(V_S = ±25V)	LM1875	20W	20W	NA	25W	30W	NA
(V_S = ±22V)	LM1876	15W	15W	NA	NA	20W	NA
(V_S = ±30V)	LM2876	25W	40W	22W	35W	50W	26W
(V_S = ±35V)	LM3875	45W (V_S = ±25V)	56W	30W	56W (V_S = ±25V)	70W	39W
(V_S = ±35V)	LM3876	45W (V_S = ±25V)	56W	30W	56W (V_S = ±25V)	70W	39W
(V_S = ±35V)	LM3886	68W (V_S = ±28V)	63W	33W	87W (V_S = ±28V)	78W	41W

* The LM391 is an Audio Power Driver designed to drive external transistors.

Audio Power Amp Selection Guide (Continued)

Typical THD Ratings	THD Measurement Conditions	Supply Range (V)	Single/ Dual	Package (Pin Count)
0.72%	Po = 1W @ V_S = 5V	2.7V to 5.5V	Single	SO(16)
0.45%	Po = 0.5W @ V_S = 5V	2.7V to 5.5V	Single	SO(8)
0.25%	Po = 0.05W @ V_S = 3V	1.8V to 6V	Dual	DIP(16), SO(16)
0.72%	Po = 1W @ V_S = 5V	2.7V to 5.5V	Single	SO(16)
0.45%	Po = 0.5W @ V_S = 5V	2.7V to 5.5V	Single	SO(8)
0.45%	Po = 0.35W @ V_S = 5V	2.7V to 5V	Single	SO(8)
0.10%	Po = 0.2W @ V_S = 5V	2.7V to 5V	Dual	SO(8)
0.25%	Po = 0.125W @ V_S = 6V	4V to 18V	Single	SO(8), DIP(8)
0.10%	Po = 0.5W @ V_S = 12V	4V to 12V	Single	DIP(14)
0.25%	Po = 0.05 @ V_S = 3V	1.8V to 6V	Dual	DIP(16), SO(16)
0.11%	Po = 0.5W @ V_S = 6V	3V to 10V	Dual	DIP(14)
0.50%	Po = 4W @ V_S = 22V	10V to 22V	Single	DIP(14), DIP(8)
0.20%	Po = 2W @ V_S = 14.4V	5V to 20V	Single	TO-220(5)
0.25%	Po = 4W @ V_S = 22V	12V to 26V	Single	DIP(14)
0.25%	Po = 0.125W @ V_S = 6V	4V to 18V	Single	SO(8), DIP(8)
0.055%	Po = 1W @ V_S = 14V	6V to 24V	Dual	DIP(14), SO(14)
0.07%	Po = 1W @ V_S = 14V	6V to 24V	Dual	SIP(11)
0.14%	Po = 2W @ V_S = 22V	6V to 32V	Dual	SIP(11)
0.14%	Po = 1W @ V_S = 12V	3V to 15V	Dual	SIP(11)
0.20%	Po = 4W @ V_S = 22V	10V to 22V	Single	DIP(14), DIP(8)
0.20%	Po = 2W @ V_S = 14.4V	5V to 20V	Single	TO-220(5)
0.25%	Po = 4W @ V_S = 22V	12V to 26V	Single	DIP(14)
0.25%	Po = 0.125W @ V_S = 6V	4V to 18V	Single	SO(8), DIP(8)
0.055%	Po = 1W @ V_S = 14V	6V to 24V	Dual	DIP(14), SO(14)
0.07%	Po = 1W @ V_S = 1V	6V to 24V	Dual	SIP(11)
0.15%	Po = 2W @ V_S = 22V	6V to 32V	Dual	SIP(11)
0.05%	Po = 1W @ V_S = 12V	6V to 32V	Dual	TO-220(11)
0.055%	Po = 1W @ V_S = 14V	6V to 24V	Dual	DIP(14), SO(14)
0.07%	Po = 1W @ V_S = 1V	6V to 24V	Dual	SIP(11)
0.15%	Po = 2W @ V_S = 22V	6V to 32V	Dual	SIP(11)
0.05%	Po = 1W @ V_S = 12V	6V to 32V	Dual	TO-220(11)
0.20%	Po = 4W @ V_S = 22V	10V to 22V	Single	DIP(14), DIP(8)
0.25%	Po = 4W @ V_S = 22V	12V to 26V	Single	DIP(14)
0.01%	*	±10V to ±50V	Single	DIP(16)
0.02%	Po = 20W @ V_S = ±25V	16V to 60V	Single	TO-220(5)
0.08%	Po = 15W/ch @ V_S = ±22V	20V to 54V	Dual	TO-220(15)**
0.06%	Po = 25W @ V_S = ±30V	20V to 60V	Single	TO-220(11)**
0.06%	Po = 40W @ V_S = ±35V	20V to 84V	Single	TO-220(11)**
0.06%	Po = 40W @ V_S = ±35V	20V to 84V	Single	TO-220(11)**
0.03%	Po = 60W @ V_S = ±28V	20V to 84V	Single	TO-220(11)**

** Isolated packages available.

National Semiconductor

LM380 Audio Power Amplifier

General Description

The LM380 is a power audio amplifier for consumer application. In order to hold system cost to a minimum, gain is internally fixed at 34 dB. A unique input stage allows inputs to be ground referenced. The output is automatically self centering to one half the supply voltage.

The output is short circuit proof with internal thermal limiting. The package outline is standard dual-in-line. A copper lead frame is used with the center three pins on either side comprising a heat sink. This makes the device easy to use in standard p-c layout.

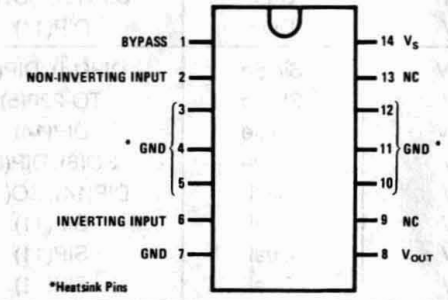
Uses include simple phonograph amplifiers, intercoms, line drivers, teaching machine outputs, alarms, ultrasonic drivers, TV sound systems, AM-FM radio, small servo drivers, power converters, etc.

A selected part for more power on higher supply voltages is available as the LM384. For more information see AN-69.

Features

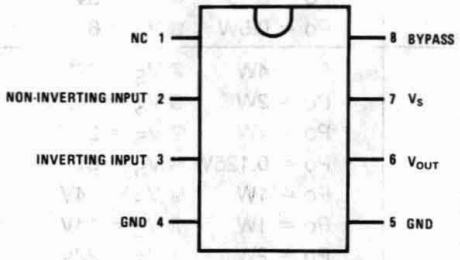
- Wide supply voltage range
- Low quiescent power drain
- Voltage gain fixed at 50
- High peak current capability
- Input referenced to GND
- High input impedance
- Low distortion
- Quiescent output voltage is at one-half of the supply voltage
- Standard dual-in-line package

Connection Diagrams (Dual-In-Line Packages, Top View)



TL/H/6977–1

Order Number LM380N
See NS Package Number N14A

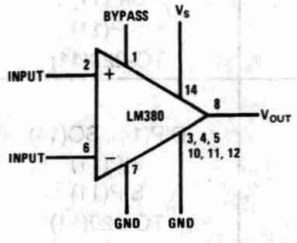


TL/H/6977–2

Order Number LM380N-8
See NS Package Number N08E

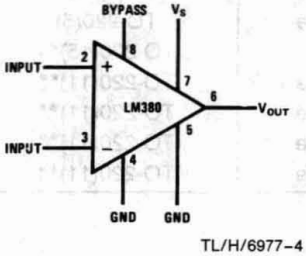
Block and Schematic Diagrams

LM380N

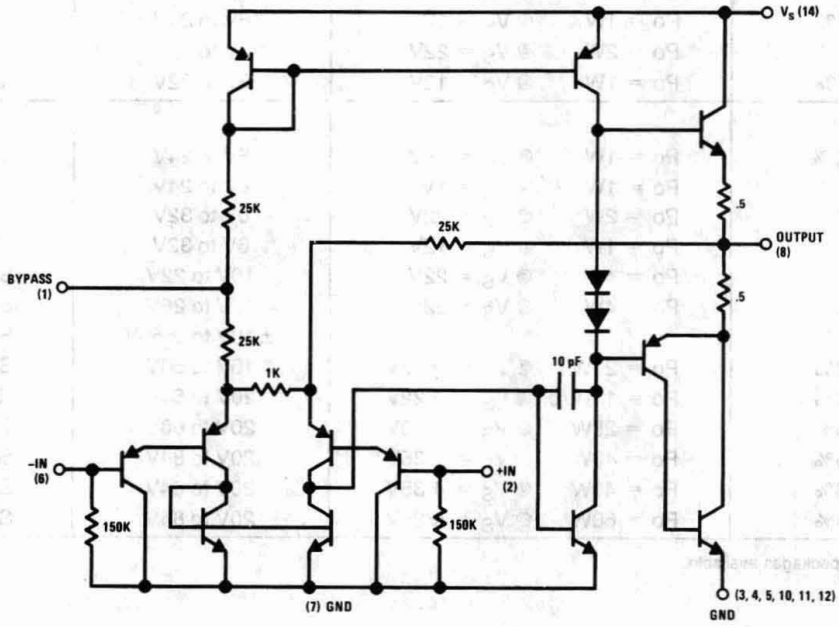


TL/H/6977–3

LM380N-8



TL/H/6977–4



TL/H/6977–5

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	22V
Peak Current	1.3A
Package Dissipation 14-Pin DIP (Notes 6 and 7)	8.3W
Package Dissipation 8-Pin DIP (Notes 6 and 7)	1.67W
Input Voltage	±0.5V
Storage Temperature	−65°C to +150°C
Operating Temperature	0°C to +70°C
Junction Temperature	+150°C
Lead Temperature (Soldering, 10 sec.)	+260°C
ESD rating to be determined	
Thermal Resistance	
θ_{JC} (14-Pin DIP)	30°C/W
θ_{JC} (8-Pin DIP)	37°C/W
θ_{JA} (14-Pin DIP)	79°C/W
θ_{JA} (8-Pin DIP)	107°C/W

Electrical Characteristics (Note 1)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
$P_{OUT(RMS)}$	Output Power	$R_L = 8\Omega$, THD = 3% (Notes 3, 4)	2.5			W
A_V	Gain		40	50	60	V/V
V_{OUT}	Output Voltage Swing	$R_L = 8\Omega$		14		V_{p-p}
Z_{IN}	Input Resistance			150k		Ω
THD	Total Harmonic Distortion	(Notes 4, 5)		0.2		%
PSRR	Power Supply Rejection Ratio	(Note 2)		38		dB
V_S	Supply Voltage		10		22	V
BW	Bandwidth	$P_{OUT} = 2W$, $R_L = 8\Omega$		100k		Hz
I_Q	Quiescent Supply Current			7	25	mA
V_{OUTQ}	Quiescent Output Voltage		8	9.0	10	V
I_{BIAS}	Bias Current	Inputs Floating		100		nA
I_{SC}	Short Circuit Current			1.3		A

Note 1: $V_S = 18V$ and $T_A = 25°C$ unless otherwise specified.

Note 2: Rejection ratio referred to the output with $C_{BYPASS} = 5\ \mu F$.

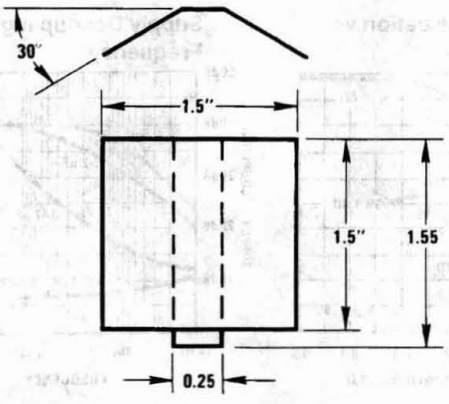
Note 3: With device Pins 3, 4, 5, 10, 11, 12 soldered into a 1/16" epoxy glass board with 2 ounce copper foil with a minimum surface of 6 square inches.

Note 4: $C_{BYPASS} = 0.47\ \mu fd$ on Pin 1.

Note 5: The maximum junction temperature of the LM380 is 150°C.

Note 6: The package is to be derated at 15°C/W junction to heat sink pins for 14-pin pkg; 75°C/W for 8-pin.

Heat Sink Dimensions

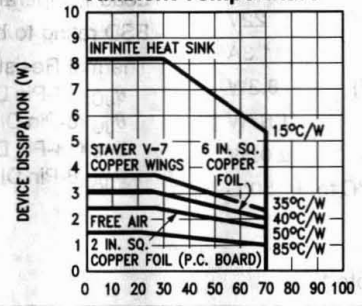


Staver Heat Sink #V-7
Staver Company
41 Saxon Ave.
P.O. Drawer H
Bayshore, NY 11706
Tel: (516) 666-8000
Copper Wings
2 Required
Soldered to
Pins 3, 4, 5,
10, 11, 12
Thickness 0.04
Inches

TL/H/6977–6

Typical Performance Characteristics

Maximum Device Dissipation vs Ambient Temperature



Note: 2 oz. copper foil, single-sided PC board.

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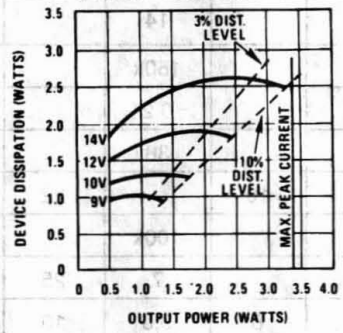
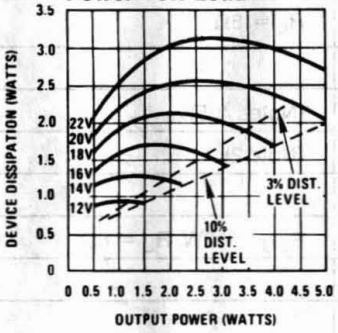
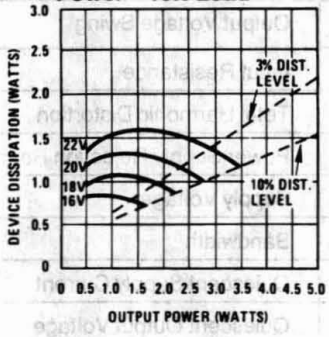
Device Dissipation vs Output Power—4Ω Load



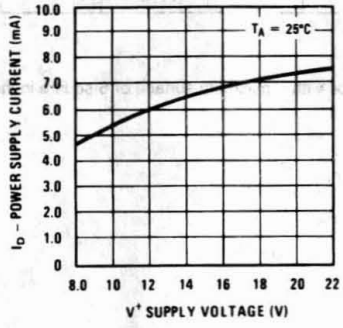
Device Dissipation vs Output Power—8Ω Load



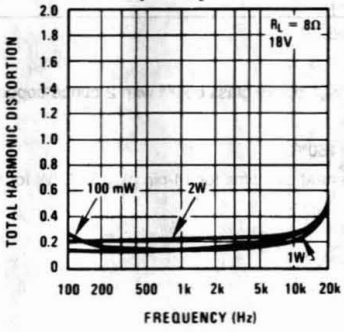
Device Dissipation vs Output Power—16Ω Load



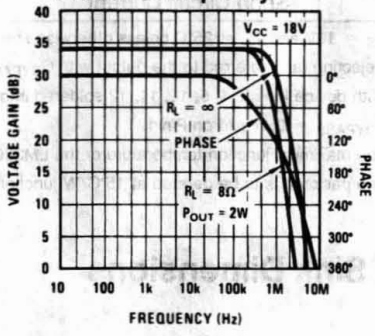
Power Supply Current vs Supply Voltage



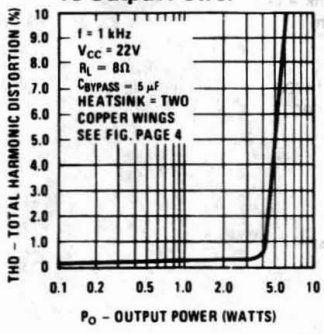
Total Harmonic Distortion vs Frequency



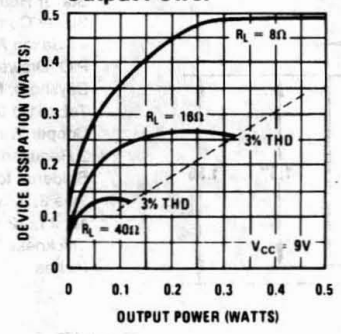
Output Voltage Gain and Phase vs Frequency



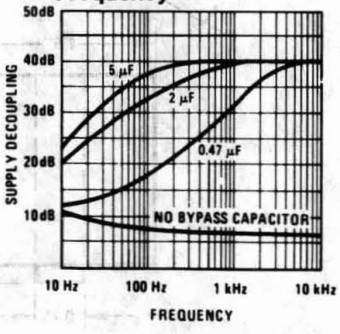
Total Harmonic Distortion vs Output Power


THD – TOTAL HARMONIC DISTORTION (%)
f = 1 kHz
V_{CC} = 22V
R_L = 8Ω
C_{BYPASS} = 5 μF
HEATSINK = TWO COPPER WINGS
SEE FIG. PAGE 4
0.1 0.2 0.5 1.0 2.0 5.0 10
P_O – OUTPUT POWER (WATTS)

Device Dissipation vs Output Power



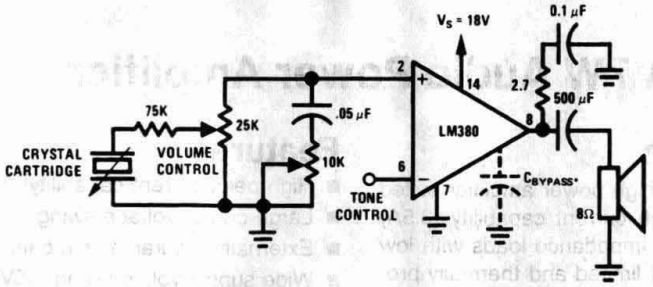
Supply Decoupling vs Frequency



TL/H/6977–7

Typical Applications

Phono Amplifier



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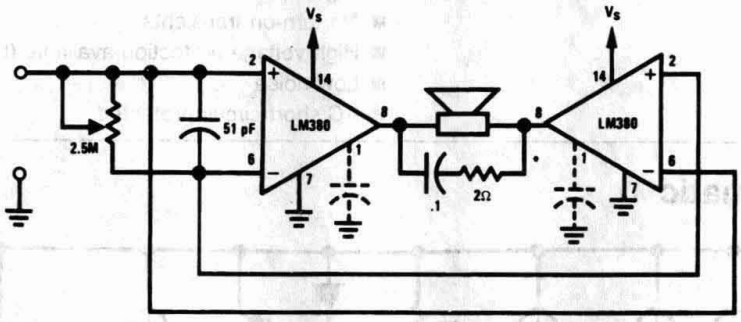
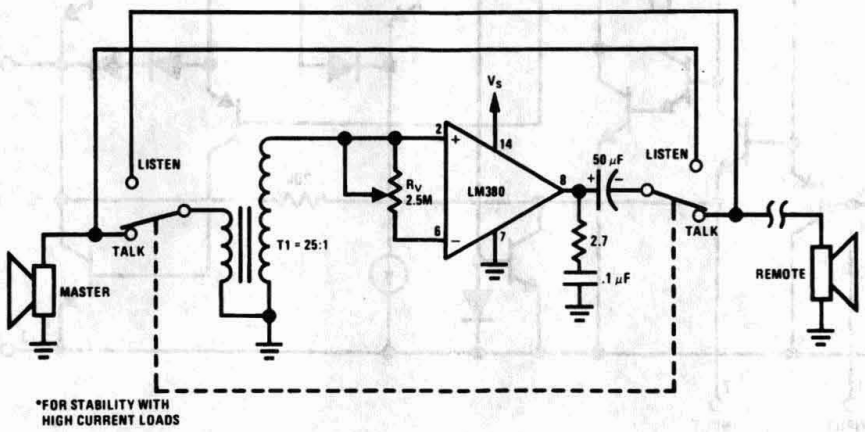
Bridge Amplifier



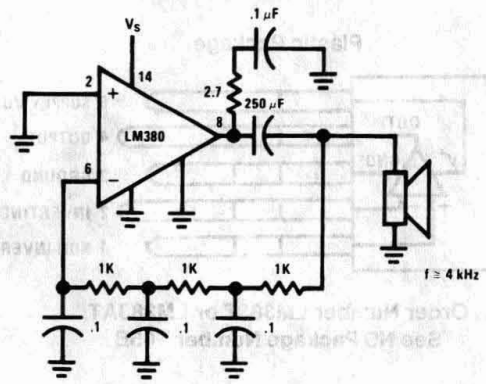
TL/H/6977–9

Intercom



TL/H/6977–10

Phase Shift Oscillator



TL/H/6977–11

National Semiconductor

LM383/LM383A 7W Audio Power Amplifier

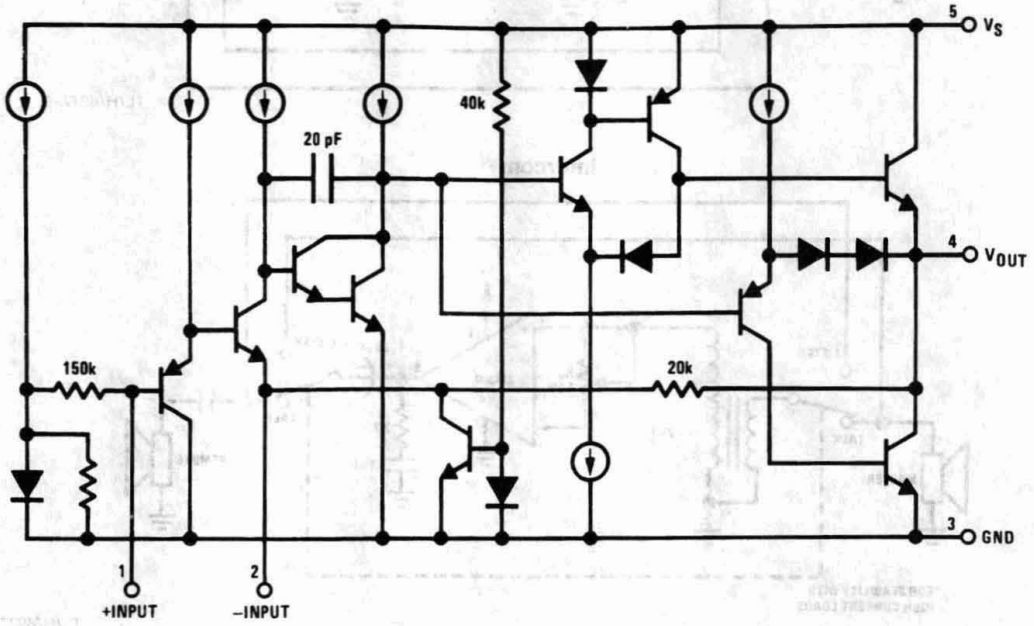
General Description

The LM383 is a cost effective, high power amplifier suited for automotive applications. High current capability (3.5A) enables the device to drive low impedance loads with low distortion. The LM383 is current limited and thermally protected. High voltage protection is available (LM383A) which enables the amplifier to withstand 40V transients on its supply. The LM383 comes in a 5-pin TO-220 package.

Features

- High peak current capability (3.5A)
- Large output voltage swing
- Externally programmable gain
- Wide supply voltage range (5V–20V)
- Few external parts required
- Low distortion
- High input impedance
- No turn-on transients
- High voltage protection available (LM383A)
- Low noise
- AC short circuit protected

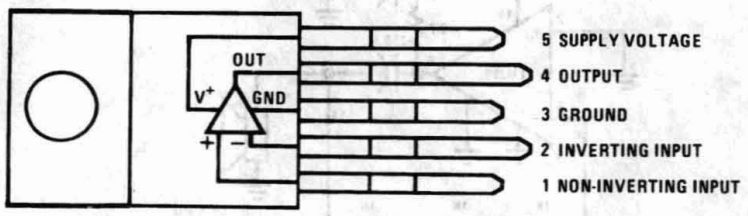
Equivalent Schematic



TL/H/7145–1

Connection Diagram

Plastic Package



TL/H/7145–2

Order Number LM383T or LM383AT
See NS Package Number T05B

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Peak Supply Voltage (50 ms)	
LM383A (Note 2)	40V
LM383	25V
Operating Supply Voltage	20V
Output Current	
Repetitive	3.5A
Non-repetitive	4.5A
Input Voltage	±0.5V
Power Dissipation (Note 3)	15W
Operating Temperature	0°C to +70°C
Storage Temperature	−60°C to +150°C
Lead Temperature (Soldering, 10 sec.)	260°C

Electrical Characteristics $V_S = 14.4V$, $T_{TAB} = 25°C$, $A_V = 100$ (40 dB), $R_L = 4\Omega$, unless otherwise specified

Parameter	Conditions	Min	Typ	Max	Units
DC Output Level		6.4	7.2	8	V
Quiescent Supply Current	Excludes Current in Feedback Resistors		45	80	mA
Supply Voltage Range		5		20	V
Input Resistance			150		kΩ
Bandwidth	Gain = 40 dB		30		kHz
Output Power	$V_S = 13.2V$, f = 1 kHz				
	$R_L = 4\Omega$, THD = 10%		4.7		W
	$R_L = 2\Omega$, THD = 10%		7.2		W
	$V_S = 13.8V$, f = 1 kHz				
	$R_L = 4\Omega$, THD = 10%		5.1		W
	$R_L = 2\Omega$, THD = 10%		7.8		W
	$V_S = 14.4V$, f = 1 kHz				
	$R_L = 4\Omega$, THD = 10%	4.8	5.5		W
	$R_L = 2\Omega$, THD = 10%	7	8.6		W
	$R_L = 1.6\Omega$, THD = 10%		9.3		W
	$V_S = 16V$, f = 1 kHz				
	$R_L = 4\Omega$, THD = 10%		7		W
	$R_L = 2\Omega$, THD = 10%		10.5		W
	$R_L = 1.6\Omega$, THD = 10%		11		W
THD	$P_o = 2W$, $R_L = 4\Omega$, f = 1 kHz		0.2		%
	$P_o = 4W$, $R_L = 2\Omega$, f = 1 kHz		0.2		%
Ripple Rejection	$R_S = 50\Omega$, f = 100 Hz	30	40		dB
	$R_S = 50\Omega$, f = 1 kHz		44		dB
Input Noise Voltage	$R_S = 0$, 15 kHz Bandwidth		2		μV
Input Noise Current	$R_S = 100$ kΩ, 15 kHz Bandwidth		40		pA

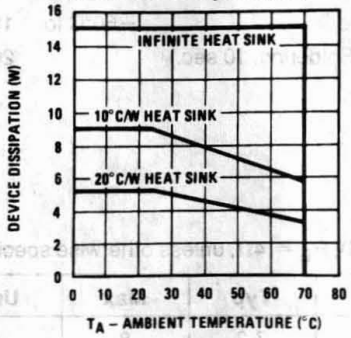
Note 1: A 0.2 μF capacitor in series with a 1Ω resistor should be placed as close as possible to pins 3 and 4 for stability.

Note 2: The LM383 shuts down above 25V.

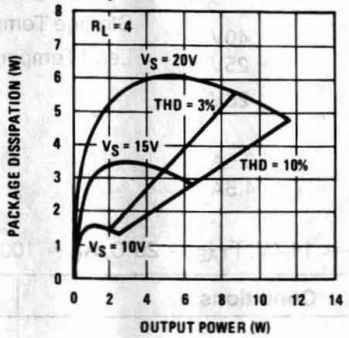
Note 3: For operating at elevated temperatures, the device must be derated based on a 150°C maximum junction temperature and a thermal resistance of 4°C/W junction to case.

Typical Performance Characteristics

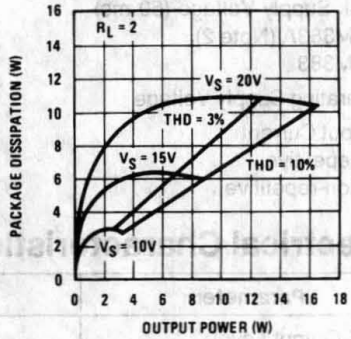
Device Dissipation vs Ambient Temperature



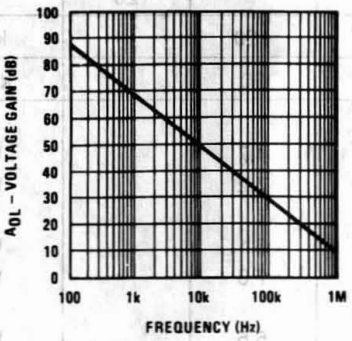
Power Dissipation vs Output Power



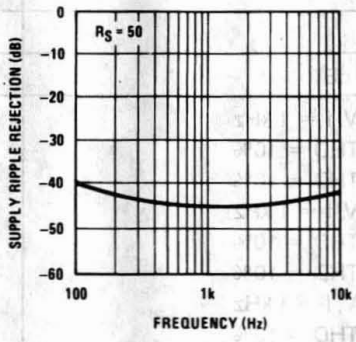
Power Dissipation vs Output Power



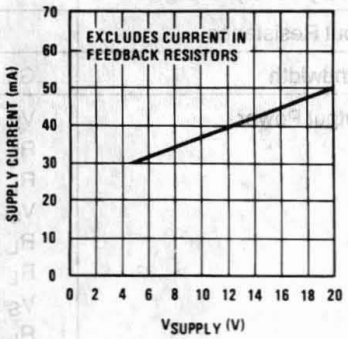
Open Loop Gain vs Frequency



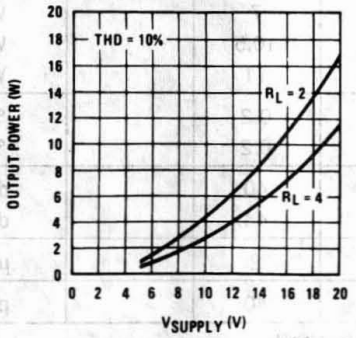
Supply Ripple Rejection vs Frequency



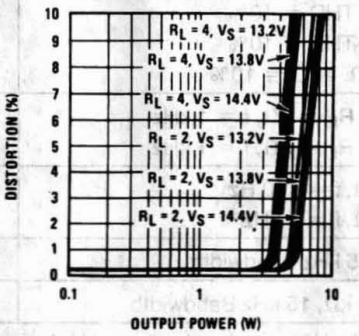
Supply Current vs Supply Voltage



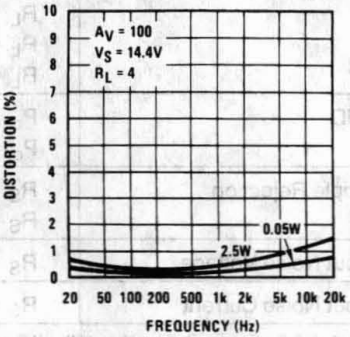
Output Power vs Supply Voltage



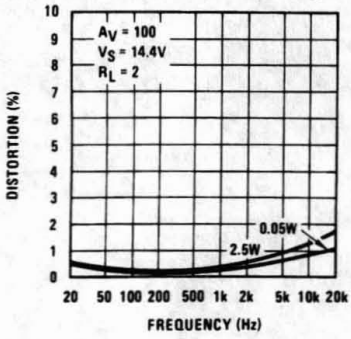
Distortion vs Output Power



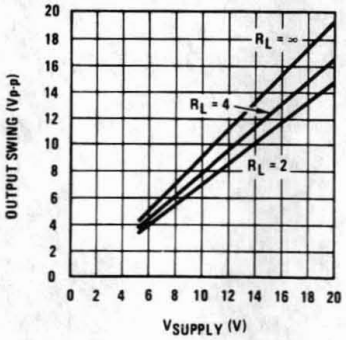
Distortion vs Frequency



Distortion vs Frequency



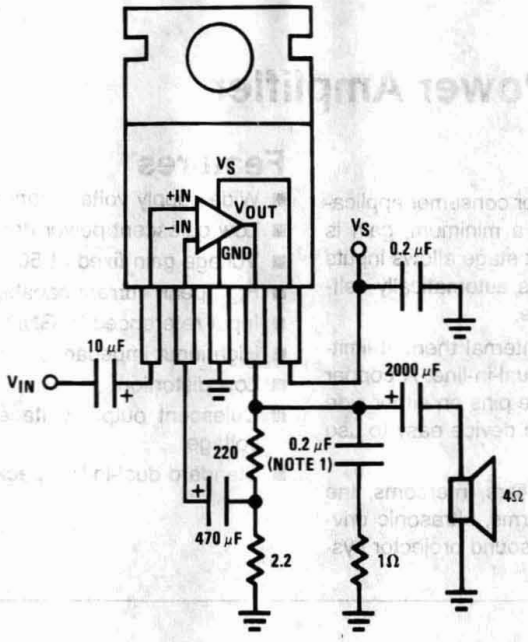
Output Swing vs Supply Voltage



TL/H/7145–4

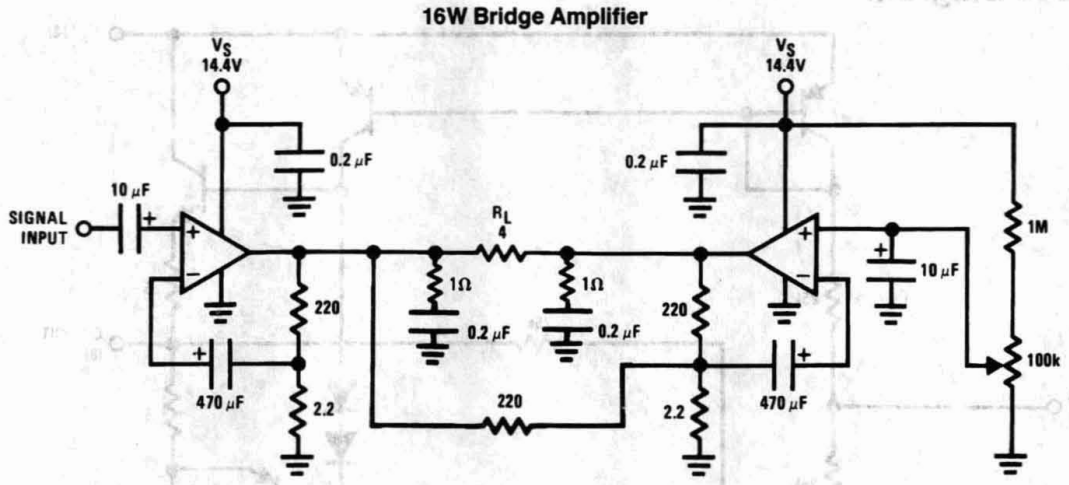
Typical Applications

Single Amplifier



TL/H/7145–3

16W Bridge Amplifier



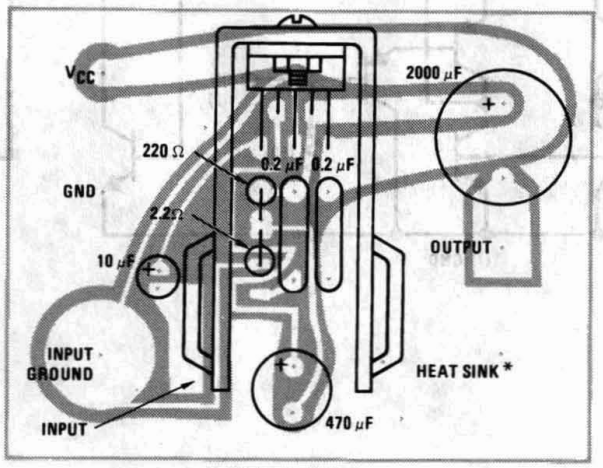
TL/H/7145–5

Component Layout

Single Amplifier

V_S = 20V

R_L = 4Ω



* Staver V-5

Heatsink from:
Staver Company
41 Saxon Ave.
P.O. Drawer H
Bay Shore, NY 11706
Tel: (516) 666-8000

TL/H/7145–6

National Semiconductor

LM384 5W Audio Power Amplifier

General Description

The LM384 is a power audio amplifier for consumer application. In order to hold system cost to a minimum, gain is internally fixed at 34 dB. A unique input stage allows inputs to be ground referenced. The output is automatically self-centering to one half the supply voltage.

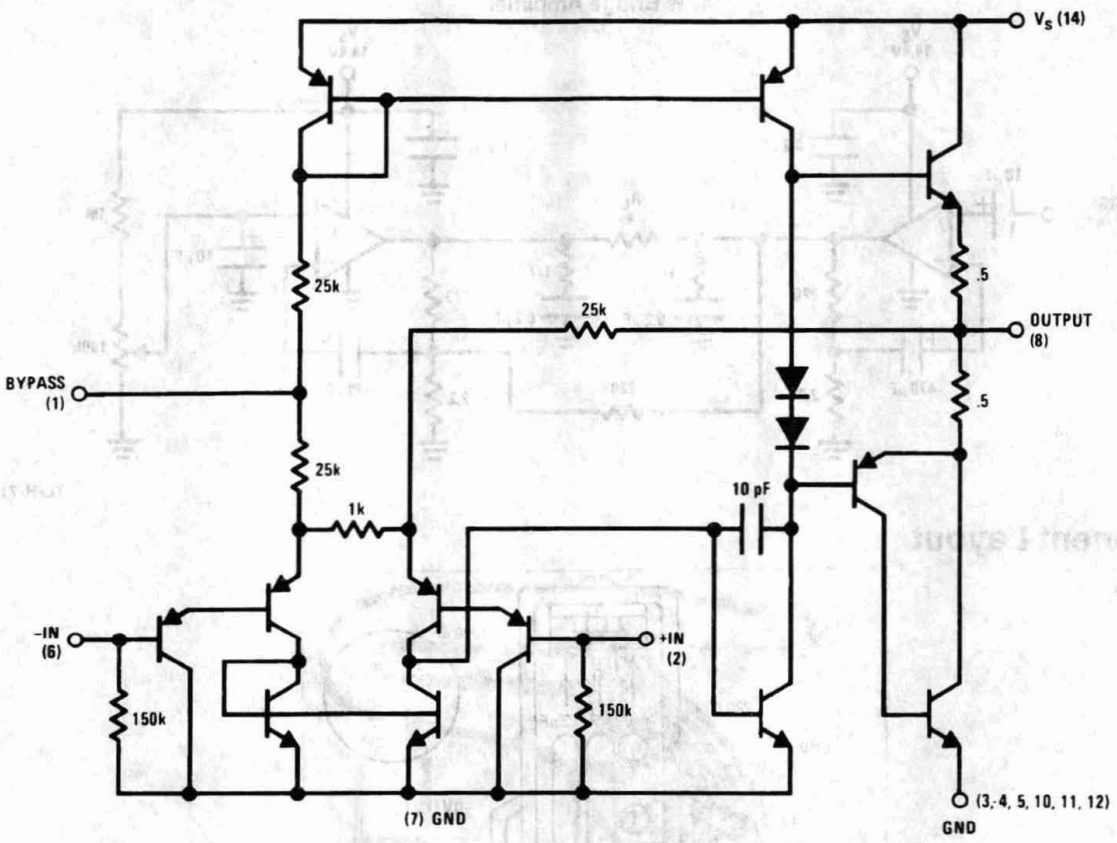
The output is short-circuit proof with internal thermal limiting. The package outline is standard dual-in-line. A copper lead frame is used with the center three pins on either side comprising a heat sink. This makes the device easy to use in standard p-c layout.

Uses include simple phonograph amplifiers, intercoms, line drivers, teaching machine outputs, alarms, ultrasonic drivers, TV sound systems, AM-FM radio, sound projector systems, etc. See AN-69 for circuit details.

Features

- Wide supply voltage range
- Low quiescent power drain
- Voltage gain fixed at 50
- High peak current capability
- Input referenced to GND
- High input impedance
- Low distortion
- Quiescent output voltage is at one half of the supply voltage
- Standard dual-in-line package

Schematic Diagram



TL/H/7843–3

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	28V
Peak Current	1.3A
Power Dissipation (See Notes 3 and 4)	1.67W
Input Voltage	±0.5V

Storage Temperature	−65°C to +150°C
Operating Temperature	0°C to +70°C
Lead Temperature (Soldering, 10 sec.)	260°C
Thermal Resistance	
θ_{JC}	30°C/W
θ_{JA}	79°C/W

Electrical Characteristics (Note 1)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
Z_{IN}	Input Resistance			150		kΩ
I_{BIAS}	Bias Current	Inputs Floating		100		nA
A_V	Gain		40	50	60	V/V
P_{OUT}	Output Power	THD = 10%, R_L = 8Ω	5	5.5		W
I_Q	Quiescent Supply Current			8.5	25	mA
$V_{OUT\,Q}$	Quiescent Output Voltage			11		V
BW	Bandwidth	P_{OUT} = 2W, R_L = 8Ω		450		kHz
V^+	Supply Voltage		12		26	V
I_{SC}	Short Circuit Current (Note 5)			1.3		A
$PSRR_{RTO}$	Power Supply Rejection Ratio (Note 2)			31		dB
THD	Total Harmonic Distortion	P_{OUT} = 4W, R_L = 8Ω		0.25	1.0	%

Note 1: V^+ = 22V and T_A = 25°C operating with a Staver V7 heat sink for 30 seconds.

Note 2: Rejection ratio referred to the output with C_{BYPASS} = 5 μF, freq = 120 Hz.

Note 3: The maximum junction temperature of the LM384 is 150°C.

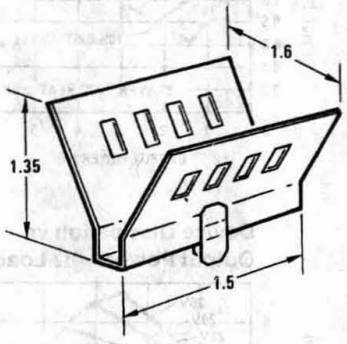
Note 4: The package is to be derated at 15°C/W junction to heat sink pins.

Note 5: Output is fully protected against a shorted speaker condition at all voltages up to 22V.

Heat Sink Dimensions

Staver Company
41 Saxon Ave.
P.O. Drawer H
Bay Shore, N.Y.
Tel: (516) 666-8000

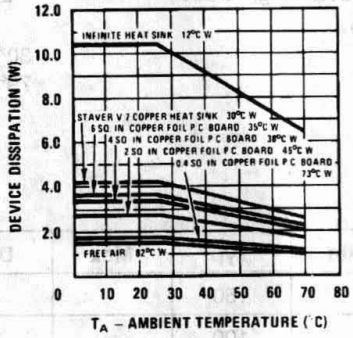
Staver "V7" Heat Sink



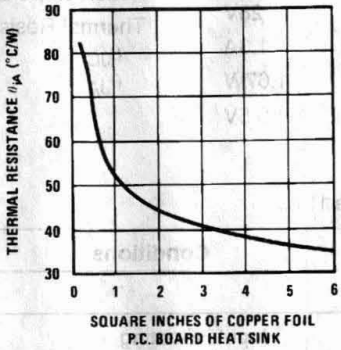
TL/H/7843–4

Typical Performance Characteristics

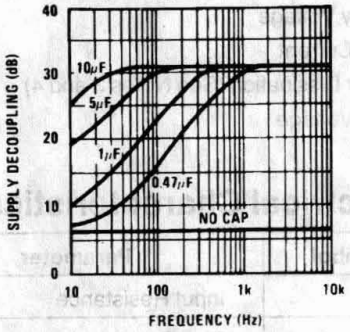
Device Dissipation vs Ambient Temperature


INFINITE HEAT SINK 12°C/W
STAVER V 7 COPPER HEAT SINK 39°C/W
6 SQ IN COPPER FOIL P C BOARD 35°C/W
4 SQ IN COPPER FOIL P C BOARD 38°C/W
2 SQ IN COPPER FOIL P C BOARD 45°C/W
0.4 SQ IN COPPER FOIL P C BOARD 73°C/W
FREE AIR 82°C/W
DEVICE DISSIPATION (W)
T_A – AMBIENT TEMPERATURE (°C)

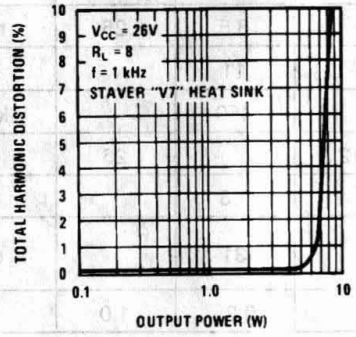
Thermal Resistance vs Square Inches



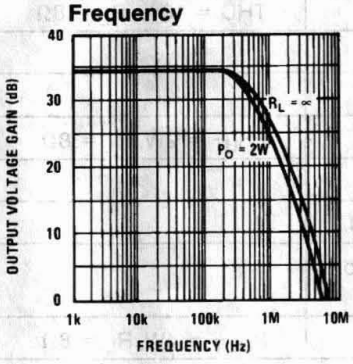
Supply Decoupling vs Frequency



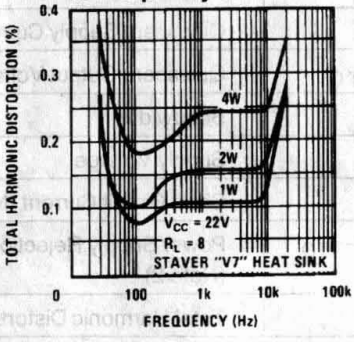
Total Harmonic Distortion vs Output Power



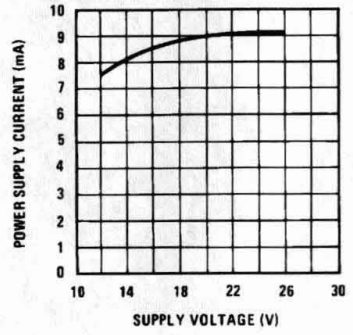
Output Voltage Gain vs Frequency



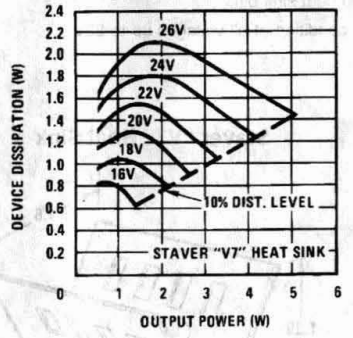
Total Harmonic Distortion vs Frequency



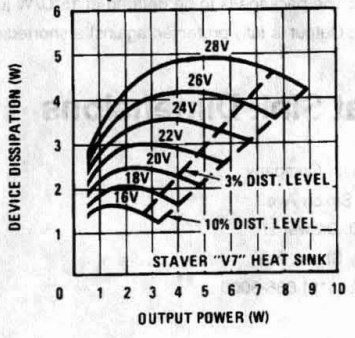
Power Supply Current vs Supply Voltage



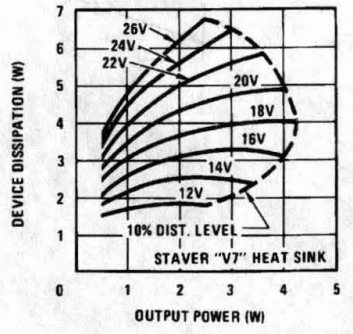
Device Dissipation vs Output Power—16Ω Load



Device Dissipation vs Output Power—8Ω Load

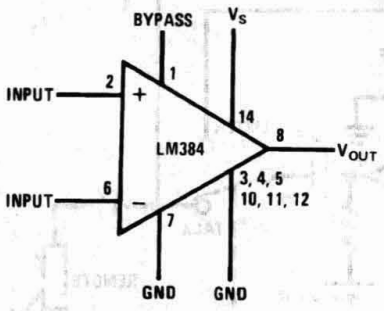


Device Dissipation vs Output Power—4Ω Load



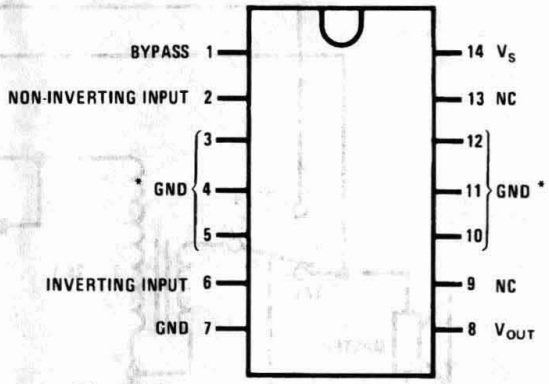
TL/H/7843–5

Block and Connection Diagrams



TL/H/7843–1

Dual-In-Line Package



*Heatsink Pins

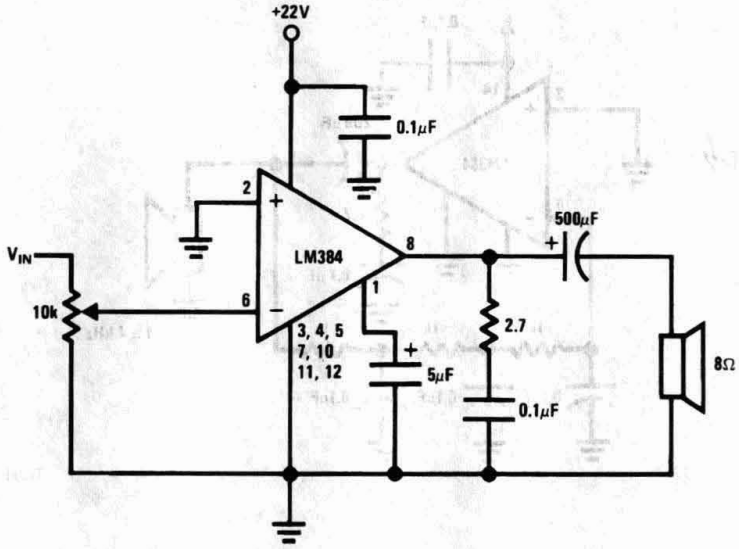
TL/H/7843–2

Top View

Order Number LM384N
See NS Package Number N14A

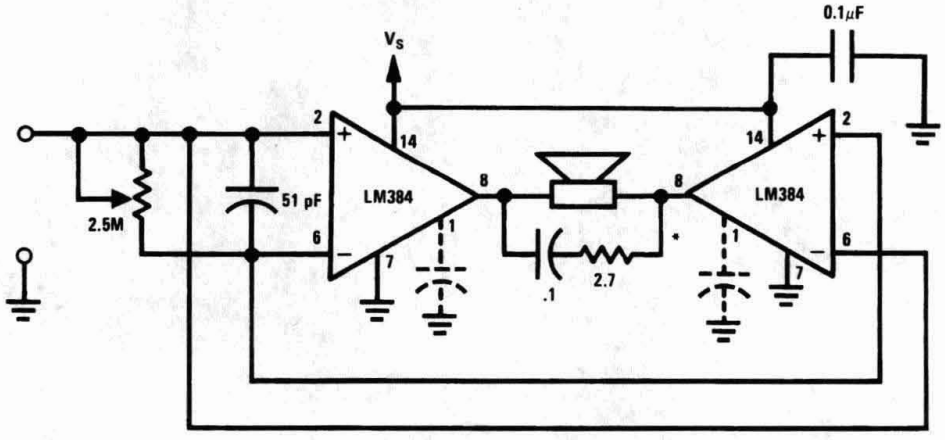
Typical Applications

Typical 5W Amplifier



TL/H/7843–6

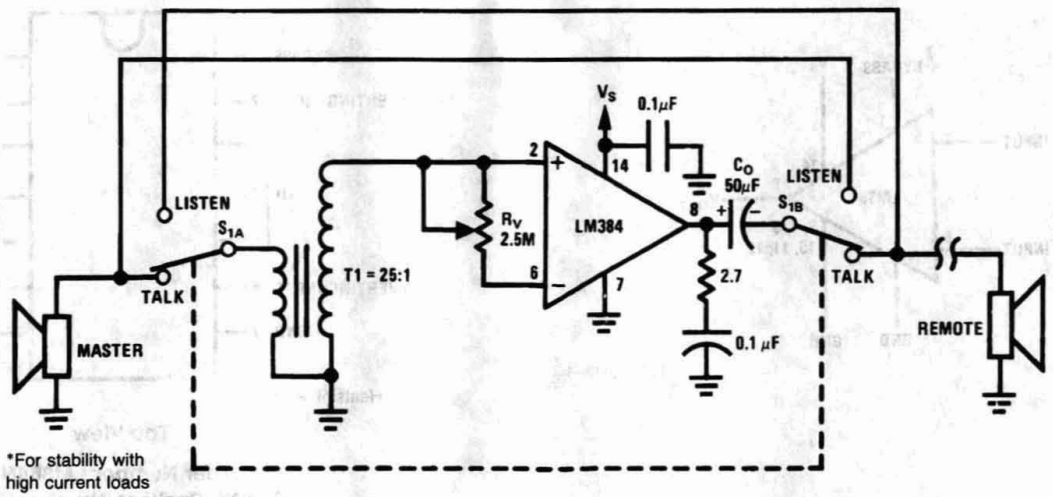
Bridge Amplifier



TL/H/7843–7

Typical Applications (Continued)

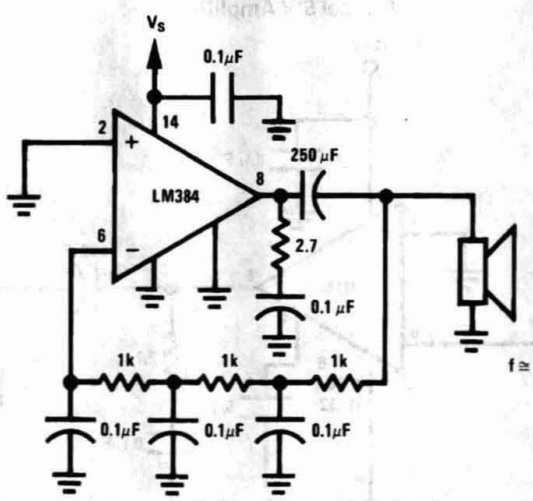
Intercom



*For stability with high current loads

TL/H/7843–8

Phase Shift Oscillator



TL/H/7843–9

National Semiconductor

LM386 Low Voltage Audio Power Amplifier

General Description

The LM386 is a power amplifier designed for use in low voltage consumer applications. The gain is internally set to 20 to keep external part count low, but the addition of an external resistor and capacitor between pins 1 and 8 will increase the gain to any value up to 200.

The inputs are ground referenced while the output is automatically biased to one half the supply voltage. The quiescent power drain is only 24 milliwatts when operating from a 6 volt supply, making the LM386 ideal for battery operation.

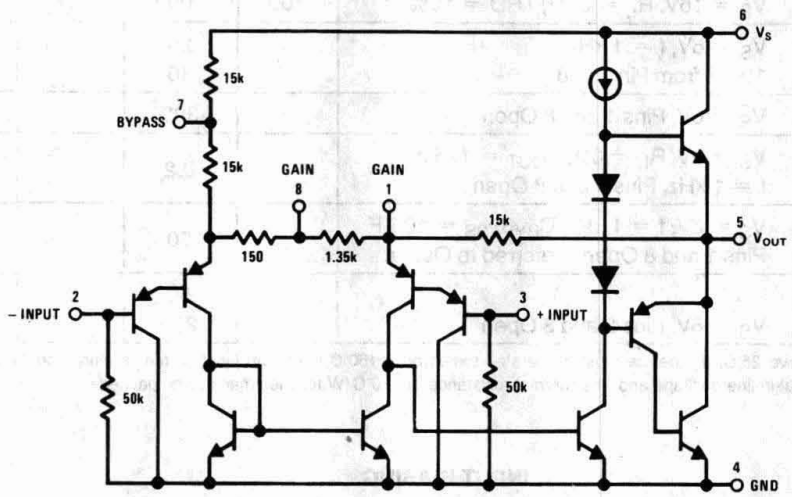
Features

- Battery operation
- Minimum external parts
- Wide supply voltage range — 4V–12V or 5V–18V
- Low quiescent current drain — 4 mA
- Voltage gains from 20 to 200
- Ground referenced input
- Self-centering output quiescent voltage
- Low distortion
- Eight pin dual-in-line package

Applications

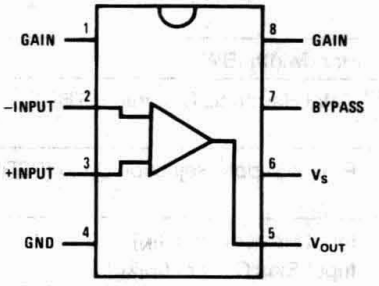
- AM-FM radio amplifiers
- Portable tape player amplifiers
- Intercoms
- TV sound systems
- Line drivers
- Ultrasonic drivers
- Small servo drivers
- Power converters

Equivalent Schematic and Connection Diagrams



TL/H/6976–1

Dual-In-Line and Small Outline Packages



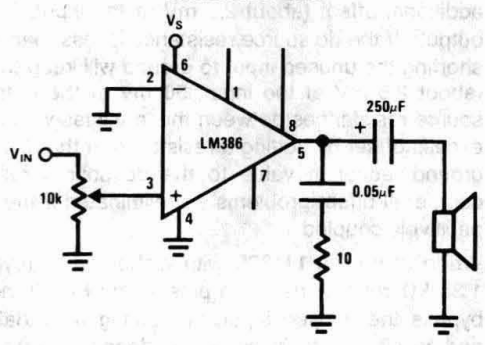
TL/H/6976–2

Top View

Order Number LM386M-1, LM386N-1, LM386N-3 or LM386N-4
See NS Package Number M08A or N08E

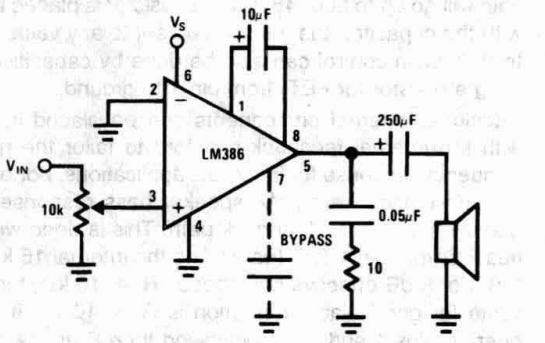
Typical Applications

Amplifier with Gain = 20
Minimum Parts



TL/H/6976–3

Amplifier with Gain = 200



TL/H/6976–4

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (LM386N-1, -3, LM386M-1)	15V
Supply Voltage (LM386N-4)	22V
Package Dissipation (Note 1) (LM386N)	1.25W
(LM386M)	0.73W
Input Voltage	±0.4V
Storage Temperature	−65°C to +150°C
Operating Temperature	0°C to +70°C
Junction Temperature	+150°C

Soldering Information

Dual-In-Line Package	
Soldering (10 sec)	+260°C
Small Outline Package	
Vapor Phase (60 sec)	+215°C
Infrared (15 sec)	+220°C

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.

Thermal Resistance

θ_{JC} (DIP)	37°C/W
θ_{JA} (DIP)	107°C/W
θ_{JC} (SO Package)	35°C/W
θ_{JA} (SO Package)	172°C/W

Electrical Characteristics $T_A = 25°C$

Parameter	Conditions	Min	Typ	Max	Units
Operating Supply Voltage (V_S)					
LM386N-1, -3, LM386M-1		4		12	V
LM386N-4		5		18	V
Quiescent Current (I_Q)	$V_S = 6V$, $V_{IN} = 0$		4	8	mA
Output Power (P_{OUT})					
LM386N-1, LM386M-1	$V_S = 6V$, $R_L = 8\Omega$, THD = 10%	250	325		mW
LM386N-3	$V_S = 9V$, $R_L = 8\Omega$, THD = 10%	500	700		mW
LM386N-4	$V_S = 16V$, $R_L = 32\Omega$, THD = 10%	700	1000		mW
Voltage Gain (A_V)	$V_S = 6V$, f = 1 kHz		26		dB
	10 μF from Pin 1 to 8		46		dB
Bandwidth (BW)	$V_S = 6V$, Pins 1 and 8 Open		300		kHz
Total Harmonic Distortion (THD)	$V_S = 6V$, $R_L = 8\Omega$, $P_{OUT} = 125$ mW f = 1 kHz, Pins 1 and 8 Open		0.2		%
Power Supply Rejection Ratio (PSRR)	$V_S = 6V$, f = 1 kHz, $C_{BYPASS} = 10\ \mu F$ Pins 1 and 8 Open, Referred to Output		50		dB
Input Resistance (R_{IN})			50		kΩ
Input Bias Current (I_{BIAS})	$V_S = 6V$, Pins 2 and 3 Open		250		nA

Note 1: For operation in ambient temperatures above 25°C, the device must be derated based on a 150°C maximum junction temperature and 1) a thermal resistance of 80°C/W junction to ambient for the dual-in-line package and 2) a thermal resistance of 170°C/W for the small outline package.

Application Hints

GAIN CONTROL

To make the LM386 a more versatile amplifier, two pins (1 and 8) are provided for gain control. With pins 1 and 8 open the 1.35 kΩ resistor sets the gain at 20 (26 dB). If a capacitor is put from pin 1 to 8, bypassing the 1.35 kΩ resistor, the gain will go up to 200 (46 dB). If a resistor is placed in series with the capacitor, the gain can be set to any value from 20 to 200. Gain control can also be done by capacitively coupling a resistor (or FET) from pin 1 to ground.

Additional external components can be placed in parallel with the internal feedback resistors to tailor the gain and frequency response for individual applications. For example, we can compensate poor speaker bass response by frequency shaping the feedback path. This is done with a series RC from pin 1 to 5 (paralleling the internal 15 kΩ resistor). For 6 dB effective bass boost: R ≅ 15 kΩ, the lowest value for good stable operation is R = 10 kΩ if pin 8 is open. If pins 1 and 8 are bypassed then R as low as 2 kΩ can be used. This restriction is because the amplifier is only compensated for closed-loop gains greater than 9.

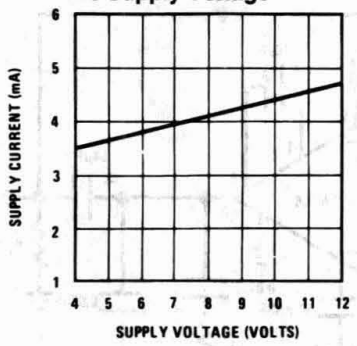
INPUT BIASING

The schematic shows that both inputs are biased to ground with a 50 kΩ resistor. The base current of the input transistors is about 250 nA, so the inputs are at about 12.5 mV when left open. If the dc source resistance driving the LM386 is higher than 250 kΩ it will contribute very little additional offset (about 2.5 mV at the input, 50 mV at the output). If the dc source resistance is less than 10 kΩ, then shorting the unused input to ground will keep the offset low (about 2.5 mV at the input, 50 mV at the output). For dc source resistances between these values we can eliminate excess offset by putting a resistor from the unused input to ground, equal in value to the dc source resistance. Of course all offset problems are eliminated if the input is capacitively coupled.

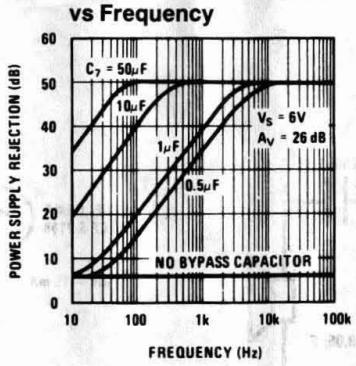
When using the LM386 with higher gains (bypassing the 1.35 kΩ resistor between pins 1 and 8) it is necessary to bypass the unused input, preventing degradation of gain and possible instabilities. This is done with a 0.1 μF capacitor or a short to ground depending on the dc source resistance on the driven input.

Typical Performance Characteristics

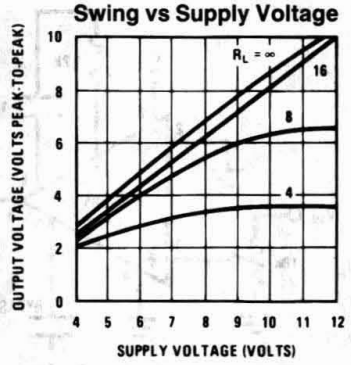
Quiescent Supply Current vs Supply Voltage



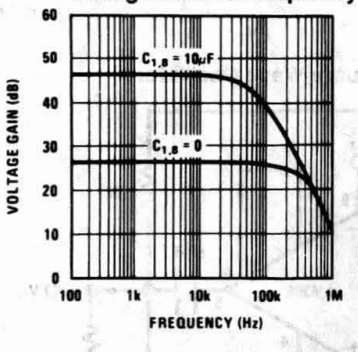
Power Supply Rejection Ratio (Referred to the Output) vs Frequency



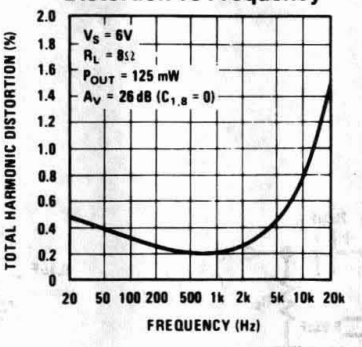
Peak-to-Peak Output Voltage Swing vs Supply Voltage



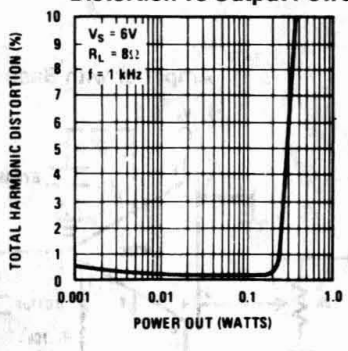
Voltage Gain vs Frequency



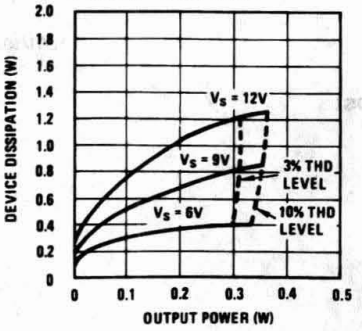
Distortion vs Frequency



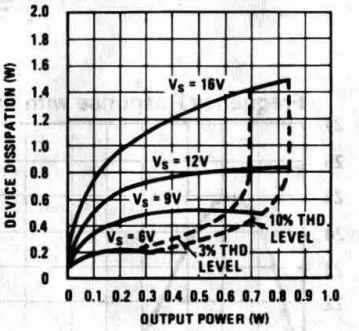
Distortion vs Output Power



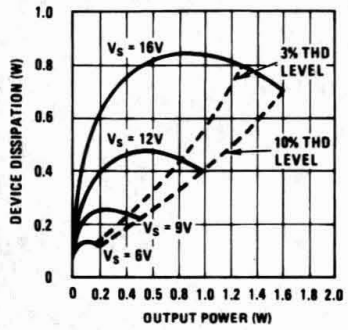
Device Dissipation vs Output Power—4Ω Load



Device Dissipation vs Output Power—8Ω Load



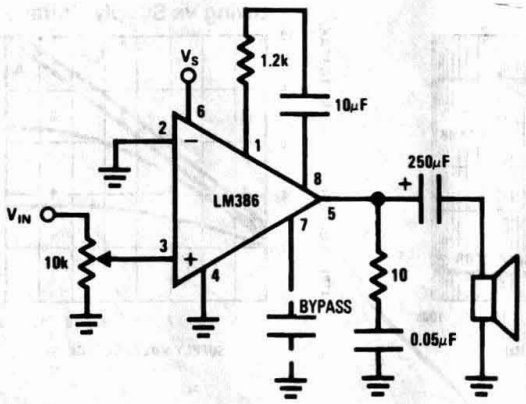
Device Dissipation vs Output Power—16Ω Load



TL/H/6976–5

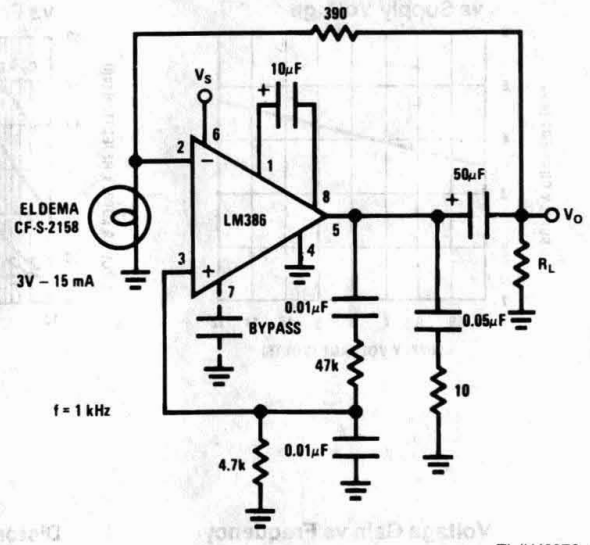
Typical Applications (Continued)

Amplifier with Gain = 50



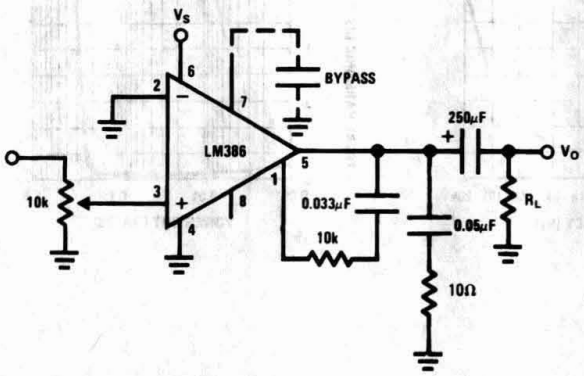
TL/H/6976–6

Low Distortion Power Wienbridge Oscillator



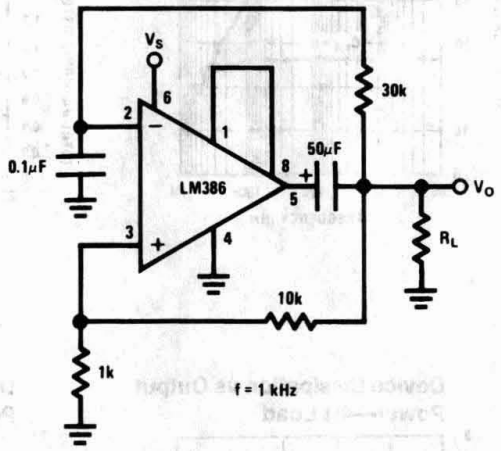
TL/H/6976–7

Amplifier with Bass Boost



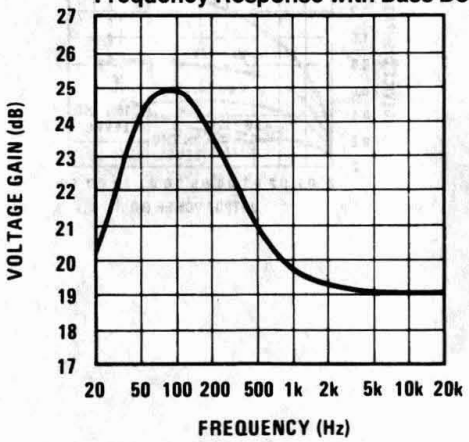
TL/H/6976–8

Square Wave Oscillator



TL/H/6976–9

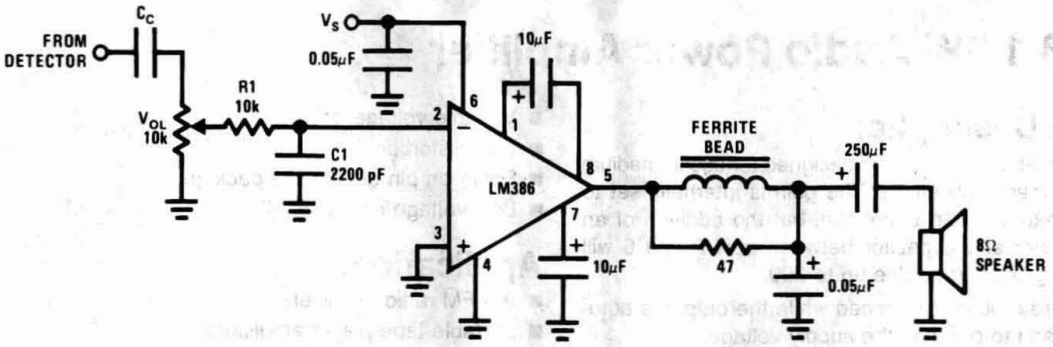
Frequency Response with Bass Boost



TL/H/6976–10

Typical Applications (Continued)

AM Radio Power Amplifier



TL/H/6976–11

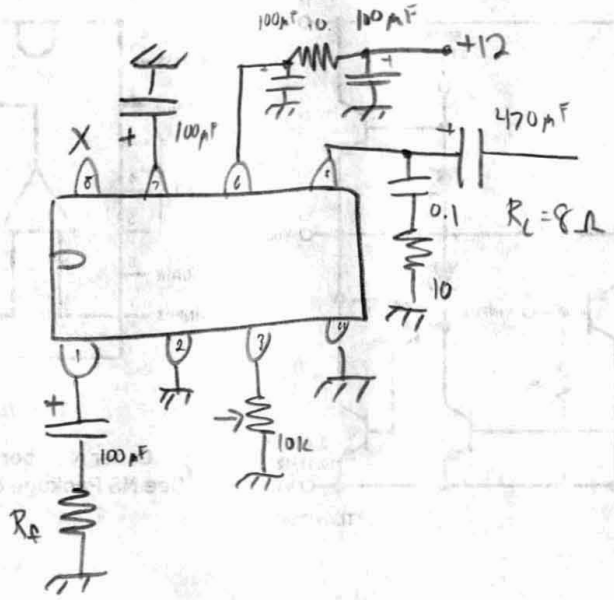
Note 1: Twist supply lead and supply ground very tightly.

Note 2: Twist speaker lead and ground very tightly.

Note 3: Ferrite bead is Ferroxcube K5-001-001/3B with 3 turns of wire.

Note 4: R1C1 band limits input signals.

Note 5: All components must be spaced very close to IC.



R_F	gain (dB)
3.3	74
10	70
33	54
105	44
820	34

National Semiconductor

LM388 1.5W Audio Power Amplifier

General Description

The LM388 is an audio amplifier designed for use in medium power consumer applications. The gain is internally set to 20 to keep external part count low, but the addition of an external resistor and capacitor between pins 2 and 6 will increase the gain to any value up to 200.

The inputs are ground referenced while the output is automatically biased to one half the supply voltage.

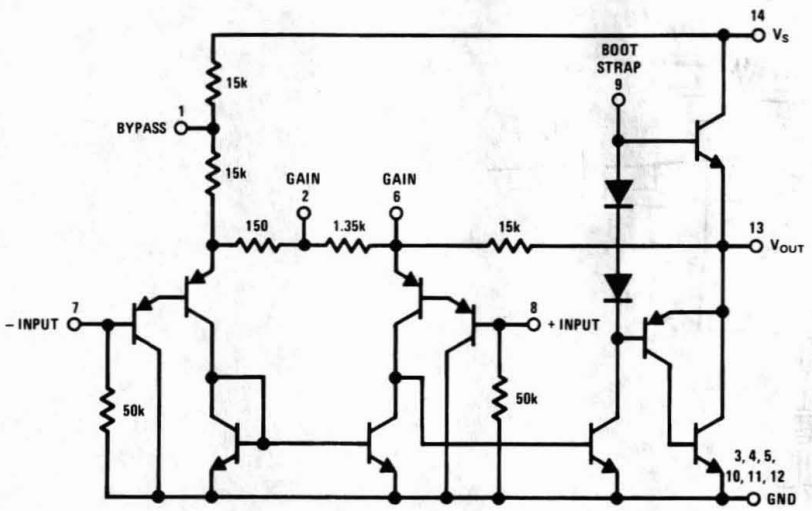
Features

- Minimum external parts
- Wide supply voltage range
- Excellent supply rejection
- Ground referenced input
- Self-centering output quiescent voltage
- Variable voltage gain
- Low distortion
- Fourteen pin dual-in-line package
- Low voltage operation, 4V

Applications

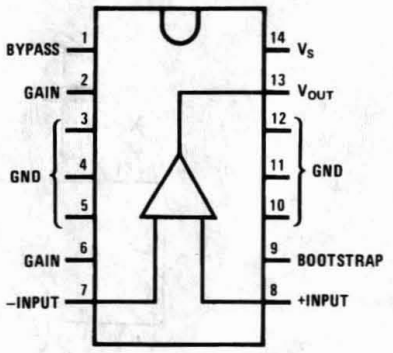
- AM-FM radio amplifiers
- Portable tape player amplifiers
- Intercoms
- TV sound systems
- Lamp drivers
- Line drivers
- Ultrasonic drivers
- Small servo drivers
- Power converters

Equivalent Schematic and Connection Diagrams



TL/H/7846–1

Dual-In-Line Package



TL/H/7846–2

Top View

Order Number LM388N-1
See NS Package Number N14A

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	15V
Package Dissipation 14-Pin DIP (Note 1)	8.3W
Input Voltage	±0.4V
Storage Temperature	−65°C to +150°C
Operating Temperature	0°C to +70°C
Junction Temperature	150°C
Lead Temperature (Soldering, 10 sec.)	260°C
Thermal Resistance	
θ_{JC}	30°C/W
θ_{JA}	79°C/W

Electrical Characteristics T_A = 25°C, *(Figure 1)*

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_S	Operating Supply Voltage LM388		4		12	V
I_Q	Quiescent Current LM388	V_{IN} = 0 V_S = 12V		16	23	mA
P_{OUT}	Output Power (Note 2) LM388N-1	R1 = R2 = 180Ω, THD = 10% V_S = 12V, R_L = 8Ω V_S = 6V, R_L = 4Ω	 1.5 0.6	 2.2 0.8		 W W
A_V	Voltage Gain	V_S = 12V, f = 1 kHz 10 μF from Pins 2 to 6	23	26 46	30	dB dB
BW	Bandwidth	V_S = 12V, Pins 2 and 6 Open		300		kHz
THD	Total Harmonic Distortion	V_S = 12V, R_L = 8Ω, P_{OUT} = 500 mW, f = 1 kHz, Pins 2 and 6 Open		0.1	1	%
PSRR	Power Supply Rejection Ratio (Note 3)	V_S = 12V, f = 1 kHz, C_{BYPASS} = 10 μF, Pins 2 and 6 Open, Referred to Output		50		dB
R_{IN}	Input Resistance		10	50		kΩ
I_{BIAS}	Input Bias Current	V_S = 12V, Pins 7 and 8 Open		250		nA

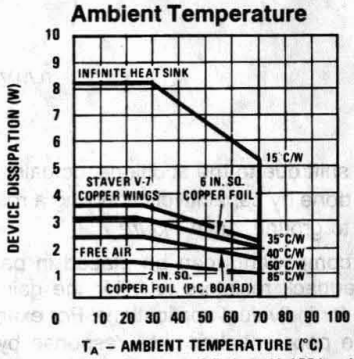
Note 1: Pins 3, 4, 5, 10, 11, 12 at 25°C. Derate at 15°C/W above 25°C case.

Note 2: The amplifier should be in high gain for full swing on higher supplies due to input voltage limitations.

Note 3: If load and bypass capacitor are returned to V_S *(Figure 2)*, rather than ground *(Figure 1)*, PSRR is typically 30 dB.

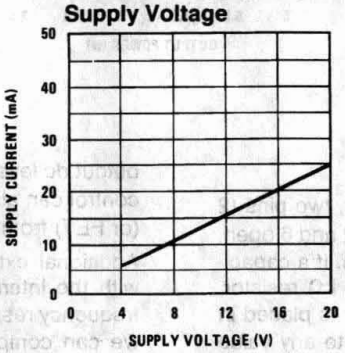
Typical Performance Characteristics

Maximum Device Dissipation vs Ambient Temperature

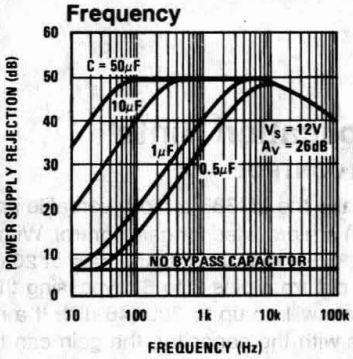


Note: 2 oz. copper foil, single-sided PC board.

Quiescent Supply Current vs Supply Voltage



Power Supply Rejection Ratio (Referred to the Output) vs Frequency



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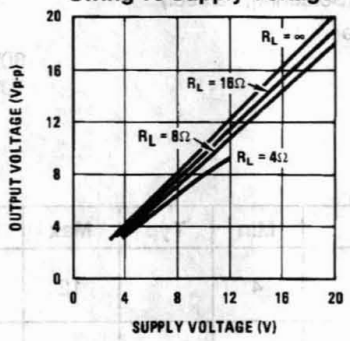
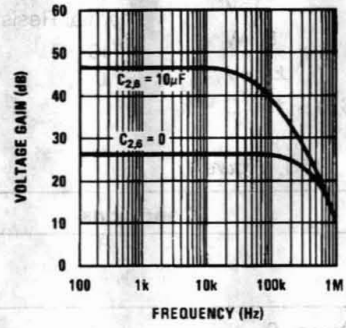
Typical Performance Characteristics (Continued)

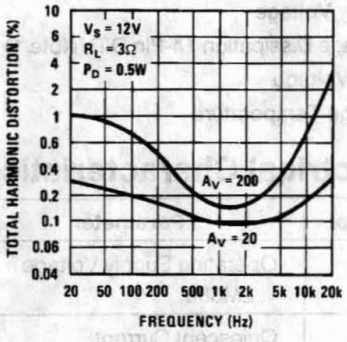
Peak-to-Peak Output Voltage Swing vs Supply Voltage



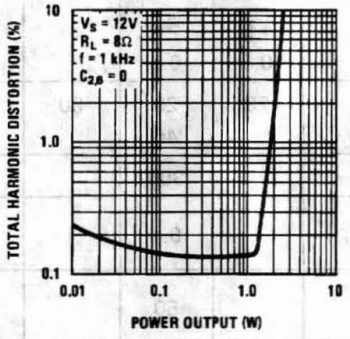
Voltage Gain vs Frequency



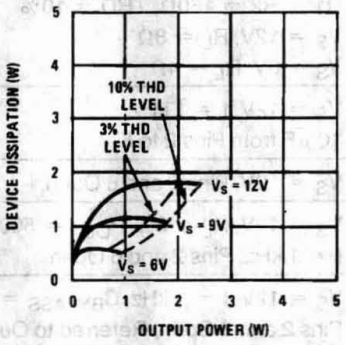
Distortion vs Frequency



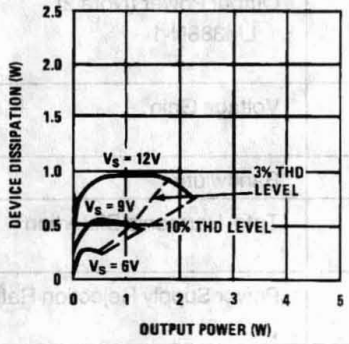
Distortion vs Output Power



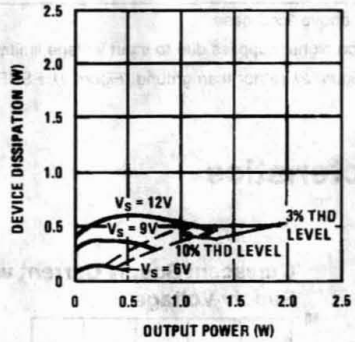
Device Dissipation vs Output Power—4Ω Load



Device Dissipation vs Output Power—8Ω Load



Device Dissipation vs Output Power—16Ω Load



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Application Hints

GAIN CONTROL

To make the LM388 a more versatile amplifier, two pins (2 and 6) are provided for gain control. With pins 2 and 6 open, the 1.35 kΩ resistor sets the gain at 20 (26 dB). If a capacitor is put from pins 2 to 6, bypassing the 1.35 kΩ resistor, the gain will go up to 200 (46 dB). If a resistor is placed in series with the capacitor, the gain can be set to any value from 20 to 200. A low frequency pole in the gain response is caused by the capacitor working against the external resistor in series with the 150Ω internal resistor. If the capacitor is eliminated and a resistor connects pins 2 to 6 then the output dc level may shift due to the additional dc gain. Gain control can also be done by capacitively coupling a resistor (or FET) from pin 6 to ground, as in *Figure 7*.

Additional external components can be placed in parallel with the internal feedback resistors to tailor the gain and frequency response for individual applications. For example, we can compensate poor speaker bass response by frequency shaping the feedback path. This is done with a series RC from pin 6 to 13 (paralleling the internal 15 kΩ resistor). For 6 dB effective bass boost: R ≅ 15 kΩ, the lowest value for good stable operation is R = 10 kΩ if pin 2

Application Hints (Continued)

is open. If pins 2 and 6 are bypassed then R as low as 2 kΩ can be used. This restriction is because the amplifier is only compensated for closed-loop gains greater than 9 V/V.

INPUT BIASING

The schematic shows that both inputs are biased to ground with a 50 kΩ resistor . The base current of the input transistors is about 250 nA, so the inputs are at about 12.5 mV when left open. If the dc source resistance driving the LM388 is higher than 250 kΩ it will contribute very little additional offset (about 2.5 mV at the input, 50 mV at the output). If the dc source resistance is less than 10 kΩ, then shorting the unused input to ground will keep the offset low (about 2.5 mV at the input, 50 mV at the output). For dc source resistances between these values we can eliminate excess offset by putting a resistor from the unused input to ground, equal in value to the dc source resistance. Of course all offset problems are eliminated if the input is capacitively coupled.

When using the LM388 with higher gains (bypassing the 1.35 kΩ resistor between pins 2 and 6) it is necessary to bypass the unused input, preventing degradation of gain and possible instabilities. This is done with a 0.1 μF capacitor or a short to ground depending on the dc source resistance on the driven input.

BOOTSTRAPPING

The base of the output transistor of the LM388 is brought out to pin 9 for Bootstrapping. The output stage of the amplifier during positive swing is shown in *Figure 3* with its external circuitry.

R1 + R2 set the amount of base current available to the output transistor. The maximum output current divided by beta is the value required for the current in R1 and R2:

$$(R1 + R2) = \beta_O \frac{(V_S/2) - V_{BE}}{I_{O\,MAX}}$$

Good design values are $V_{BE} = 0.7V$ and $\beta_O = 100$.

Example: 1 watt into 8Ω load with $V_S = 12V$.

$$I_{O\,MAX} = \sqrt{\frac{2P_O}{R_L}} = 500\ mA$$

$$(R1 + R2) = 100\left(\frac{(12/2) - 0.7}{0.5}\right) = 1060\Omega$$

To keep the current in R2 constant during positive swing capacitor C_B is added. As the output swings positive C_B lifts R1 and R2 above the supply, maintaining a constant voltage across R2. To minimize the value of C_B, R1 = R2. The pole due to C_B and R1 and R2 is usually set equal to the pole due to the output coupling capacitor and the load. This gives:

$$C_B \cong \frac{4C_C}{\beta_O} \cong \frac{C_C}{25}$$

Example: for 100 Hz pole and $R_L = 8\Omega$; $C_C = 200\ \mu F$ and $C_B = 8\ \mu F$, if R1 is made a diode and R2 increased to give the same current, C_B can be decreased by about a factor of 4, as in *Figure 4*.

For reduced component count the load can replace R1. The value of (R1 + R2) is the same, so R2 is increased. Now C_B is both the coupling and the bootstrapping capacitor (see *Figure 2*).

Typical Applications

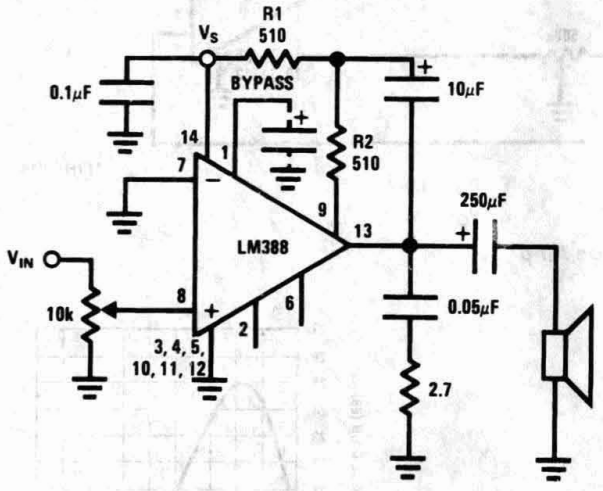

FIGURE 1. Load Returned to Ground (Amplifier with Gain = 20)

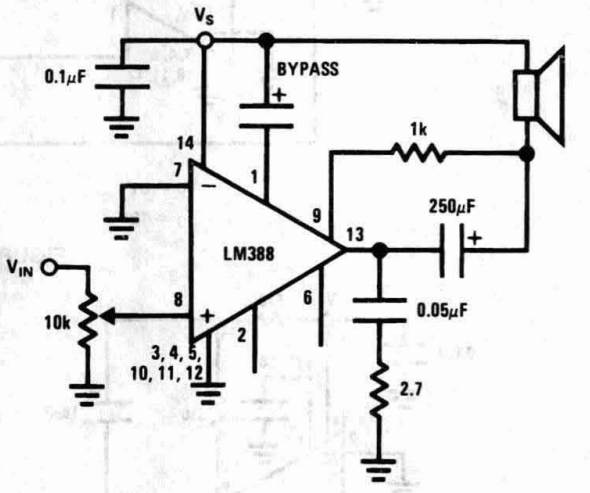

FIGURE 2. Load Returned to V_S (Amplifier with Gain = 20)

Typical Applications (Continued)

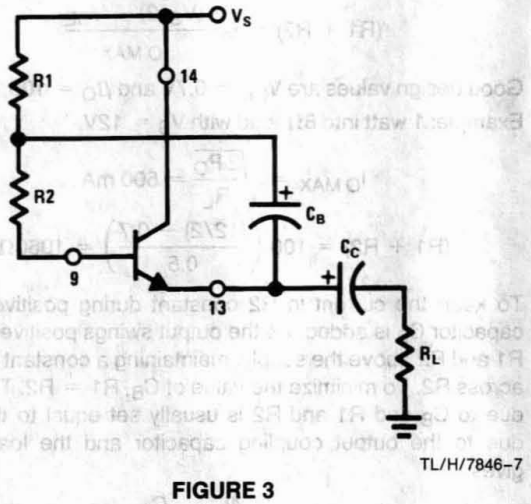

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FIGURE 3

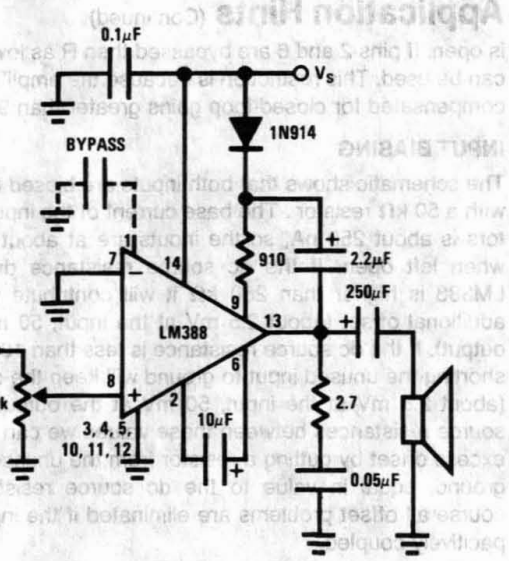

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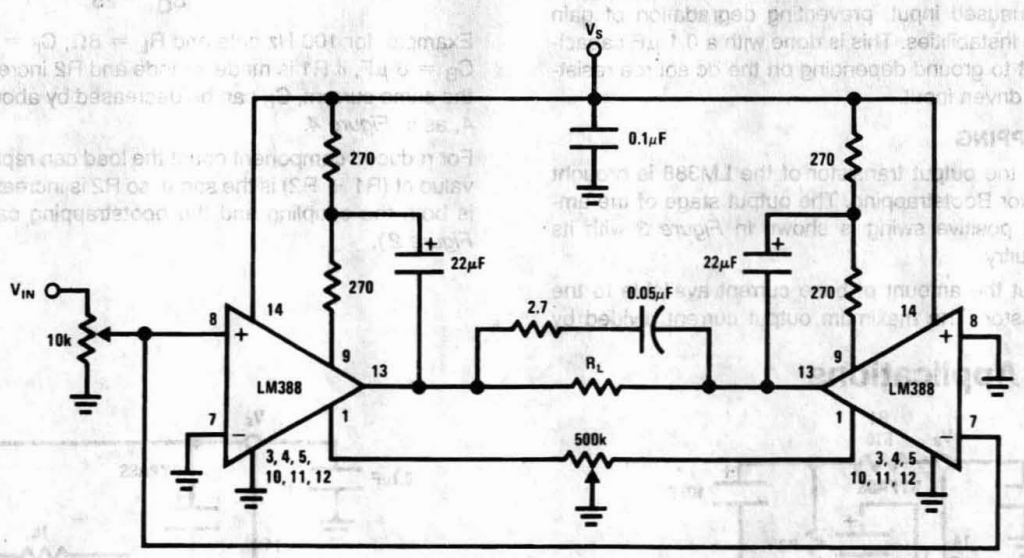
FIGURE 4. Ampifier with Gain = 200 and Minimum C_B



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V_S = 6V R_L = 4Ω P_O = 1.0W
V_S = 12V R_L = 8Ω P_O = 4W

FIGURE 5. Bridge Amp

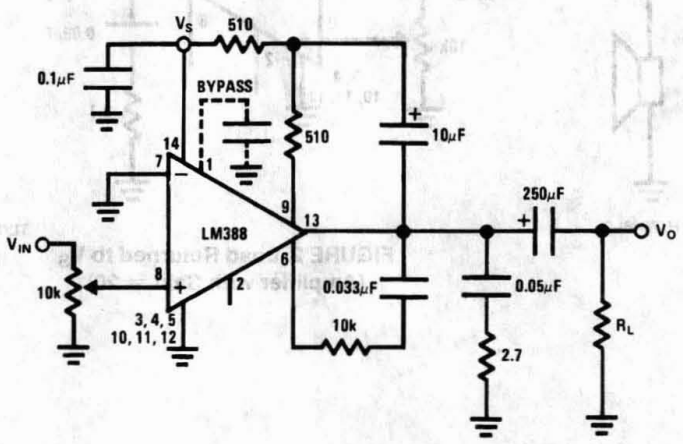

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FIGURE 6a. Amplifier with Bass Boost

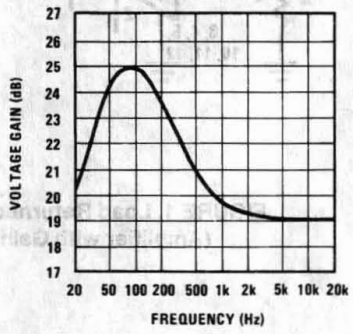

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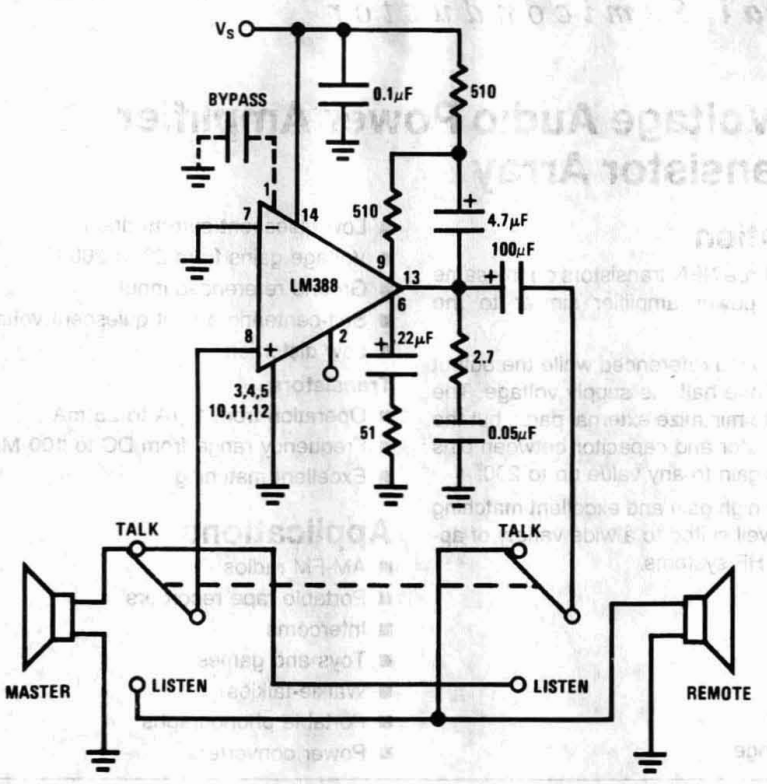
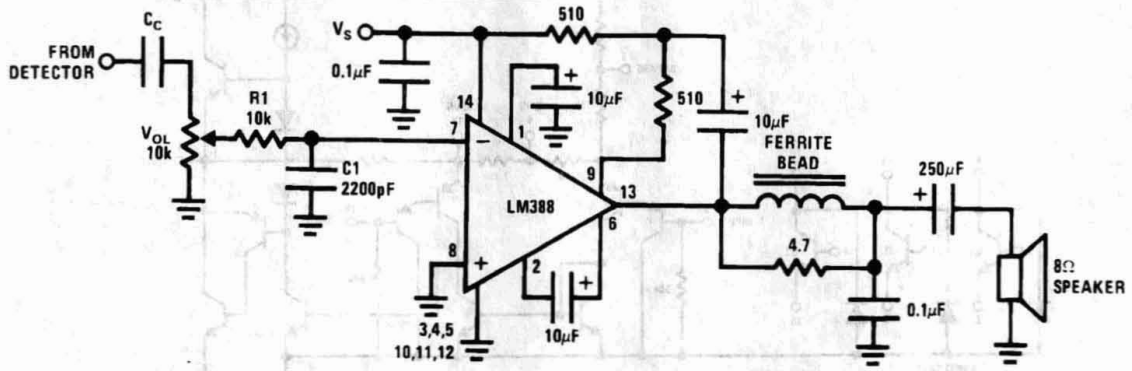
FIGURE 6b. Frequency Response with Bass Boost

Typical Applications (Continued)



TL/H/7846–12

FIGURE 7. Intercom



TL/H/7846–13

FIGURE 8. AM Radio Power Amplifier

Note 1: Twist supply lead and supply ground very tightly.

Note 2: Twist speaker lead and ground very tightly.

Note 3: Ferrite bead is Ferroxcube K5-001-001/3B with 3 turns of wire.

Note 4: R1C1 band limits input signals.

Note 5: All components must be spaced very close to IC.

National Semiconductor

LM389 Low Voltage Audio Power Amplifier with NPN Transistor Array

General Description

The LM389 is an array of three NPN transistors on the same substrate with an audio power amplifier similar to the LM386.

The amplifier inputs are ground referenced while the output is automatically biased to one half the supply voltage. The gain is internally set at 20 to minimize external parts, but the addition of an external resistor and capacitor between pins 4 and 12 will increase the gain to any value up to 200.

The three transistors have high gain and excellent matching characteristics. They are well suited to a wide variety of applications in DC through VHF systems.

Features

Amplifier

- Battery operation
- Minimum external parts
- Wide supply voltage range
- Low quiescent current drain
- Voltage gains from 20 to 200
- Ground referenced input
- Self-centering output quiescent voltage
- Low distortion

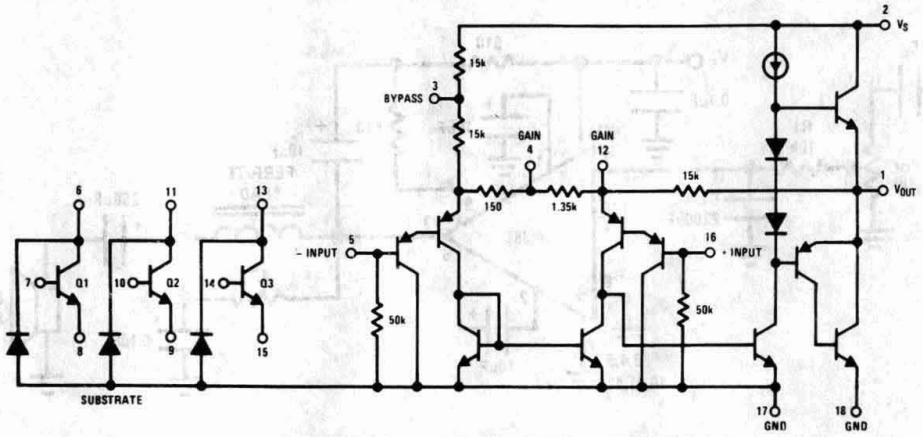
Transistors

- Operation from 1 μA to 25 mA
- Frequency range from DC to 100 MHz
- Excellent matching

Applications

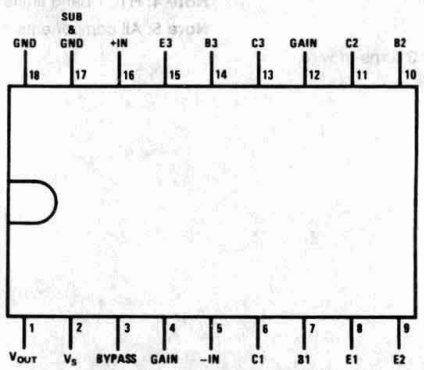
- AM-FM radios
- Portable tape recorders
- Intercoms
- Toys and games
- Walkie-talkies
- Portable phonographs
- Power converters

Equivalent Schematic and Connection Diagrams



TL/H/7847–1

Dual-In-Line Package



TL/H/7847–2

Order Number LM389N
See NS Package Number N18A

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	15V
Package Dissipation (Note 1)	1.89W
Input Voltage	±0.4V
Storage Temperature	−65°C to +150°C
Operating Temperature	0°C to +70°C
Junction Temperature	150°C
Lead Temperature (Soldering, 10 sec.)	260°C
Collector to Emitter Voltage, V_{CEO}	12V
Collector to Base Voltage, V_{CBO}	15V
Collector to Substrate Voltage, V_{CIO} (Note 2)	15V
Collector Current, I_C	25 mA
Emitter Current, I_E	25 mA
Base Current, I_B	5 mA
Power Dissipation (Each Transistor) $T_A \leq +70°C$	150 mW
Thermal Resistance	
θ_{JC}	24°C/W
θ_{JA}	70°C/W

Electrical Characteristics $T_A = 25°C$

Symbol	Parameter	Conditions	Min	Typ	Max	Units
AMPLIFIER						
V_S	Operating Supply Voltage		4		12	V
I_Q	Quiescent Current	$V_S = 6V$, $V_{IN} = 0V$		6	12	mA
P_{OUT}	Output Power (Note 3)	THD = 10% $V_S = 6V$, $R_L = 8\Omega$ $V_S = 9V$, $R_L = 16\Omega$	250	325 500		mW mW
A_V	Voltage Gain	$V_S = 6V$, f = 1 kHz 10 μF from Pins 4 to 12	23	26 46	30	dB dB
BW	Bandwidth	$V_S = 6V$, Pins 4 and 12 Open		250		kHz
THD	Total Harmonic Distortion	$V_S = 6V$, $R_L = 8\Omega$, $P_{OUT} = 125$ mW, f = 1 kHz, Pins 4 and 12 Open		0.2	3.0	%
PSRR	Power Supply Rejection Ratio	$V_S = 6V$, f = 1 kHz, $C_{BYPASS} = 10$ μF, Pins 4 and 12 Open, Referred to Output	30	50		dB
R_{IN}	Input Resistance		10	50		kΩ
I_{BIAS}	Input Bias Current	$V_S = 6V$, Pins 5 and 16 Open		250		nA
TRANSISTORS						
V_{CEO}	Collector to Emitter Breakdown Voltage	$I_C = 1$ mA, $I_B = 0$	12	20		V
V_{CBO}	Collector to Base Breakdown Voltage	$I_C = 10$ μA, $I_E = 0$	15	40		V
V_{CIO}	Collector to Substrate Breakdown Voltage	$I_C = 10$ μA, $I_E = I_B = 0$	15	40		V
V_{EBO}	Emitter to Base Breakdown Voltage	$I_E = 10$ μA, $I_C = 0$	6.4	7.1	7.8	V
H_{FE}	Static Forward Current Transfer Ratio (Static Beta)	$I_C = 10$ μA $I_C = 1$ mA $I_C = 10$ mA	 100	100 275 275		
h_{oe}	Open-Circuit Output Admittance	$I_C = 1$ mA, $V_{CE} = 5V$, f = 1.0 kHz		20		μmho
V_{BE}	Base to Emitter Voltage	$I_E = 1$ mA		0.7	0.85	V
$\lvert V_{BE1} - V_{BE2} \rvert$	Base to Emitter Voltage Offset	$I_E = 1$ mA		1	5	mV
V_{CESAT}	Collector to Emitter Saturation Voltage	$I_C = 10$ mA, $I_B = 1$ mA		0.15	0.5	V
C_{EB}	Emitter to Base Capacitance	$V_{EB} = 3V$		1.5		pF
C_{CB}	Collector to Base Capacitance	$V_{CB} = 3V$		2		pF
C_{CI}	Collector to Substrate Capacitance	$V_{CI} = 3V$		3.5		pF
h_{fe}	High Frequency Current Gain	$I_C = 10$ mA, $V_{CE} = 5V$, f = 100 MHz	1.5	5.5		

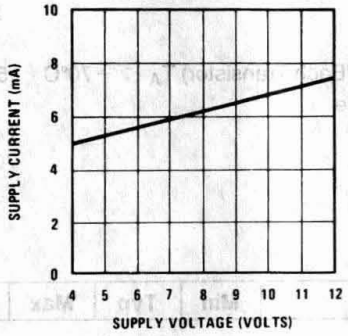
Note 1: For operation in ambient temperatures above 25°C, the device must be derated based on a 150°C maximum junction temperature and a thermal resistance of 66°C/W junction to ambient.

Note 2: The collector of each transistor is isolated from the substrate by an integral diode. Therefore, the collector voltage should remain positive with respect to pin 17 at all times.

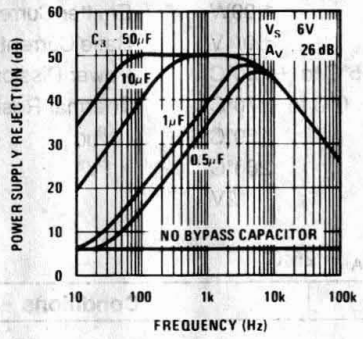
Note 3: If oscillation exists under some load conditions, add 2.7Ω and 0.05 μF series network from pin 1 to ground.

Typical Amplifier Performance Characteristics

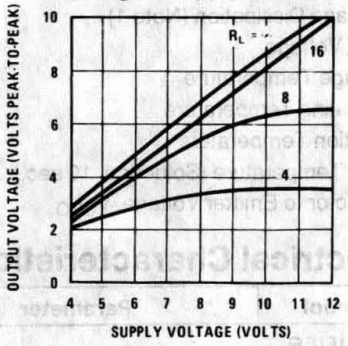
Quiescent Supply Current vs Supply Voltage



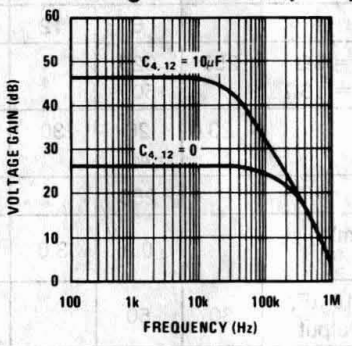
Power Supply Rejection Ratio (Referred to the Output) vs Frequency



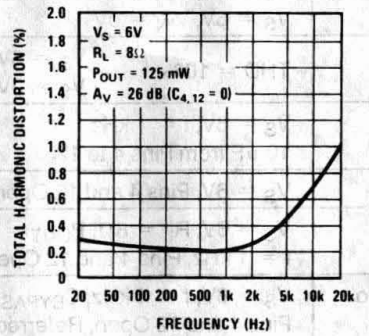
Peak-to-Peak Output Voltage Swing vs Supply Voltage



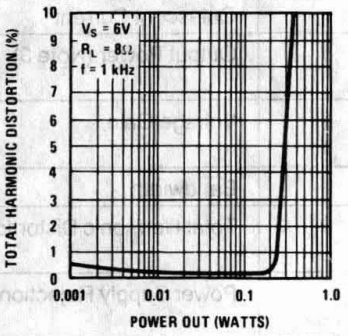
Voltage Gain vs Frequency



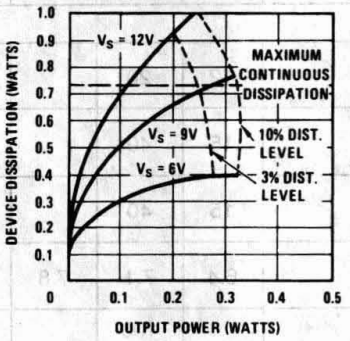
Distortion vs Frequency



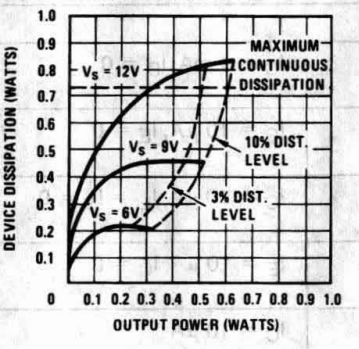
Distortion vs Output Power



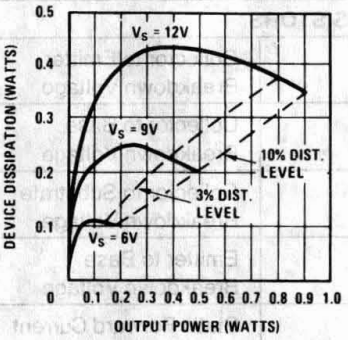
Device Dissipation vs Output Power—4Ω Load



Device Dissipation vs Output Power—8Ω Load



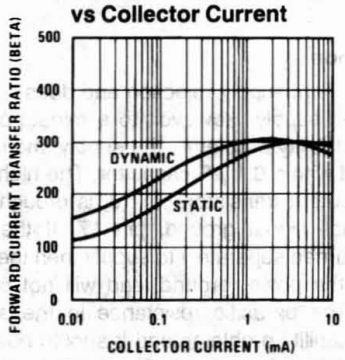
Device Dissipation vs Output Power—16Ω Load



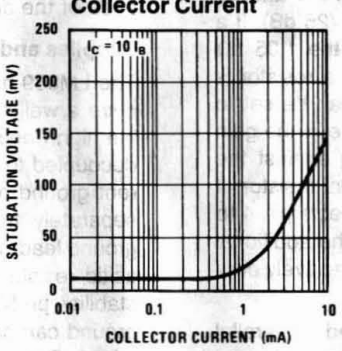
TL/H/7847–3

Typical Transistor Performance Characteristics

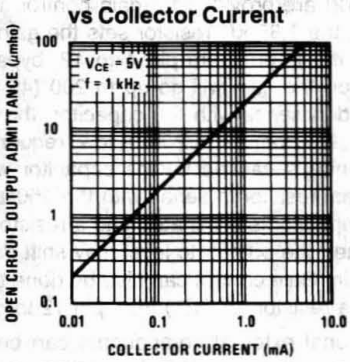
Forward Current Transfer Ratio vs Collector Current



Saturation Voltage vs Collector Current

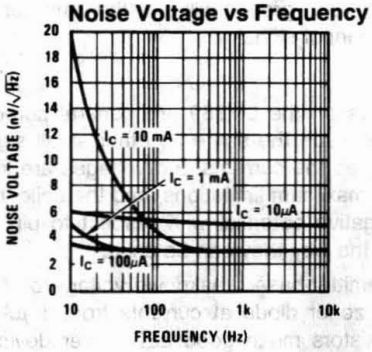


Open Circuit Output Admittance vs Collector Current

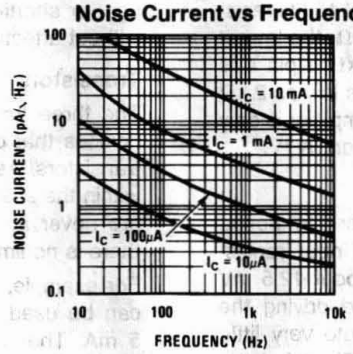


TL/H/7847–4

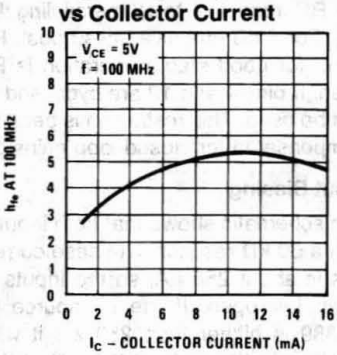
Noise Voltage vs Frequency



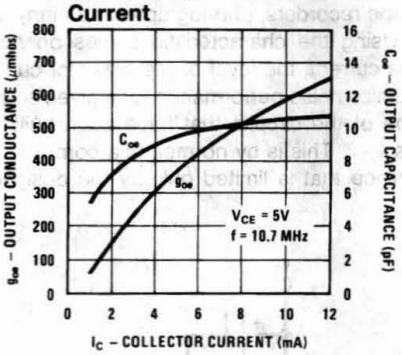
Noise Current vs Frequency



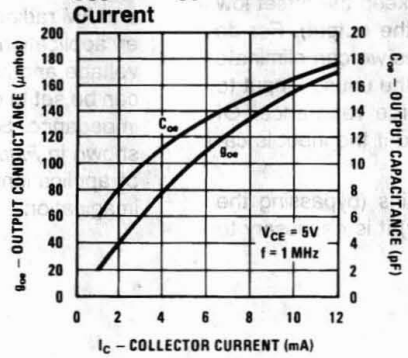
High Frequency Current Gain vs Collector Current



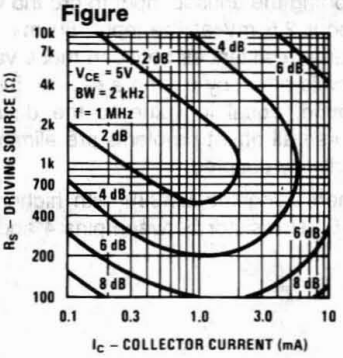
g_{oe} and C_{oe} vs Collector Current



g_{oe} and C_{oe} vs Collector Current



Contours of Constant Noise Figure



TL/H/7847–5

Application Hints

Gain Control

To make the LM389 a more versatile amplifier, two pins (4 and 12) are provided for gain control. With pins 4 and 12 open, the 1.35 kΩ resistor sets the gain at 20 (26 dB). If a capacitor is put from pin 4 to 12, bypassing the 1.35 kΩ resistor, the gain will go up to 200 (46 dB). If a resistor is placed in series with the capacitor, the gain can be set to any value from 20 to 200. A low frequency pole in the gain response is caused by the capacitor working against the external resistor in series with the 150Ω internal resistor. If the capacitor is eliminated and a resistor connects pin 4 to 12, then the output dc level may shift due to the additional dc gain. Gain control can also be done by capacitively coupling a resistor (or FET) from pin 12 to ground.

Additional external components can be placed in parallel with the internal feedback resistors to tailor the gain and frequency response for individual applications. For example, we can compensate poor speaker bass response by frequency shaping the feedback path. This is done with a series RC from pin 1 to 12 (paralleling the internal 15 kΩ resistor). For 6 dB effective bass boost: R ≅ 15 kΩ, the lowest value for good stable operation is R = 10 kΩ if pin 4 is open. If pins 4 and 12 are bypassed then R as low as 2 kΩ can be used. This restriction is because the amplifier is only compensated for closed-loop gains greater than 9V/V.

Input Biasing

The schematic shows that both inputs are biased to ground with a 50 kΩ resistor. The base current of the input transistors is about 250 nA, so the inputs are at about 12.5 mV when left open. If the dc source resistance driving the LM389 is higher than 250 kΩ it will contribute very little additional offset (about 2.5 mV at the input, 50 mV at the output). If the dc source resistance is less than 10 kΩ, then shorting the unused input to ground will keep the offset low (about 2.5 mV at the input, 50 mV at the output). For dc source resistances between these values we can eliminate excess offset by putting a resistor from the unused input to ground, equal in value to the dc source resistance. Of course all offset problems are eliminated if the input is capacitively coupled.

When using the LM389 with higher gains (bypassing the 1.35 kΩ resistor between pins 4 and 12) it is necessary to bypass the unused input, preventing degradation of gain and possible instabilities. This is done with a 0.1 μF capacitor or a short to ground depending on the dc source resistance of the driven input.

Supplies and Grounds

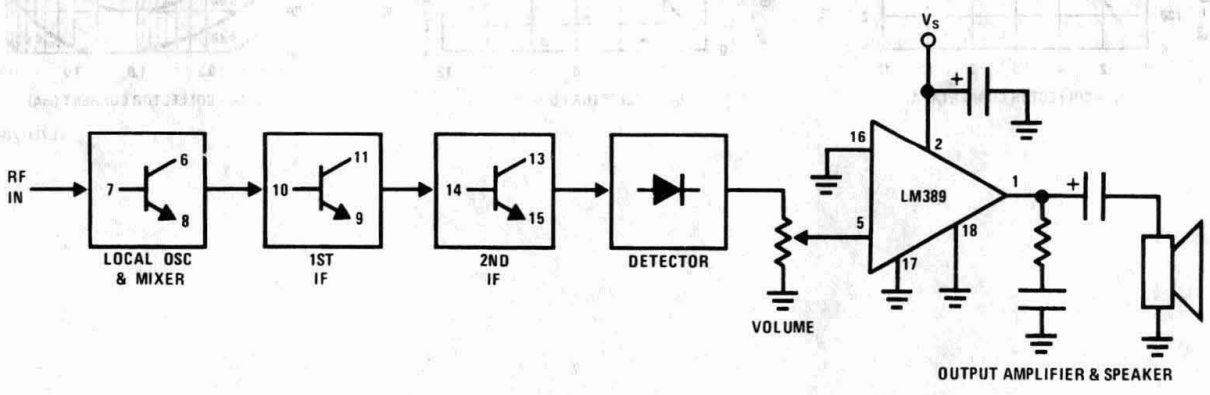
The LM389 has excellent supply rejection and does not require a well regulated supply. However, to eliminate possible high frequency stability problems, the supply should be decoupled to ground with a 0.1 μF capacitor. The high current ground of the output transistor, pin 18, is brought out separately from small signal ground, pin 17. If the two ground leads are returned separately to supply then the parasitic resistance in the power ground lead will not cause stability problems. The parasitic resistance in the signal ground can cause stability problems and it should be minimized. Care should also be taken to insure that the power dissipation does not exceed the maximum dissipation of the package for a given temperature. There are two ways to mute the LM389 amplifier. Shorting pin 3 to the supply voltage, or shorting pin 12 to ground will turn the amplifier off without affecting the input signal.

Transistors

The three transistors on the LM389 are general purpose devices that can be used the same as other small signal transistors. As long as the currents and voltages are kept within the absolute maximum limitations, and the collectors are never at a negative potential with respect to pin 17, there is no limit on the way they can be used.

For example, the emitter-base breakdown voltage of 7.1V can be used as a zener diode at currents from 1 μA to 5 mA. These transistors make good LED driver devices, V_{SAT} is only 150 mV when sinking 10 mA.

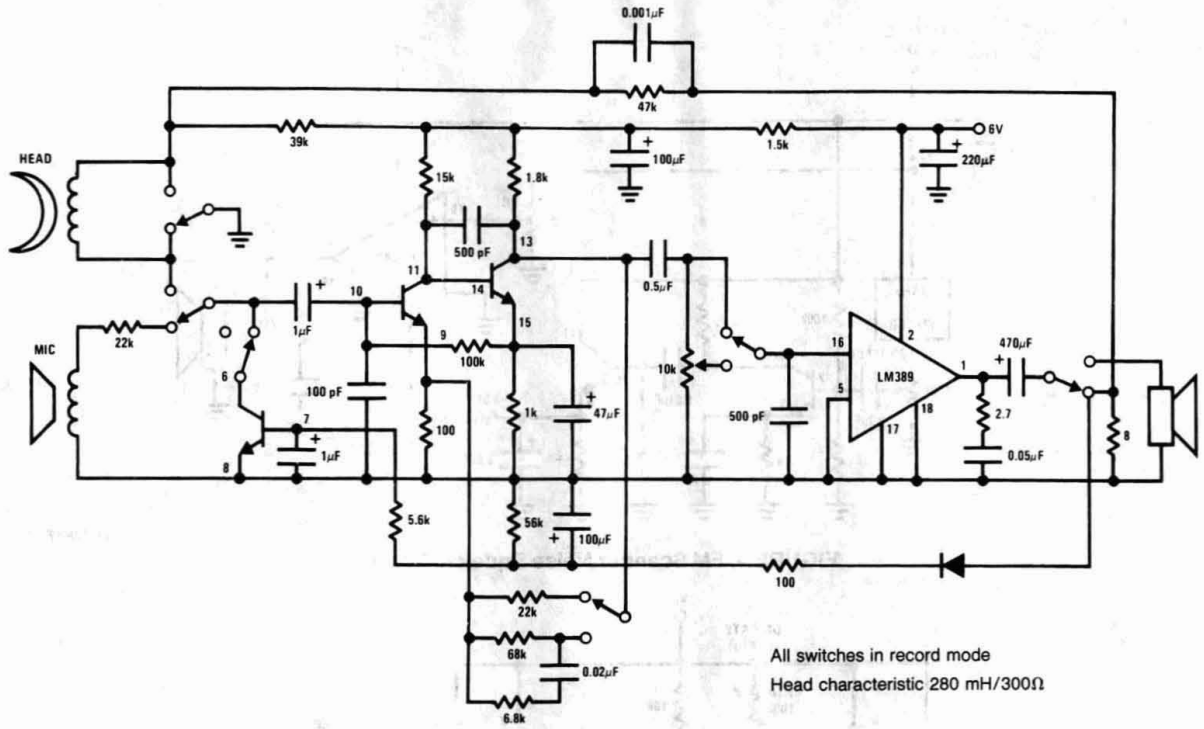
In the linear region, these transistors have been used in AM and FM radios, tape recorders, phonographs and many other applications. Using the characteristic curves on noise voltage and noise current, the level of the collector current can be set to optimize noise performance for a given source impedance. Some of the circuits that have been built are shown in *Figures 1–7*. This is by no means a complete list of applications, since that is limited only by the designers imagination.



TL/H/7847–6

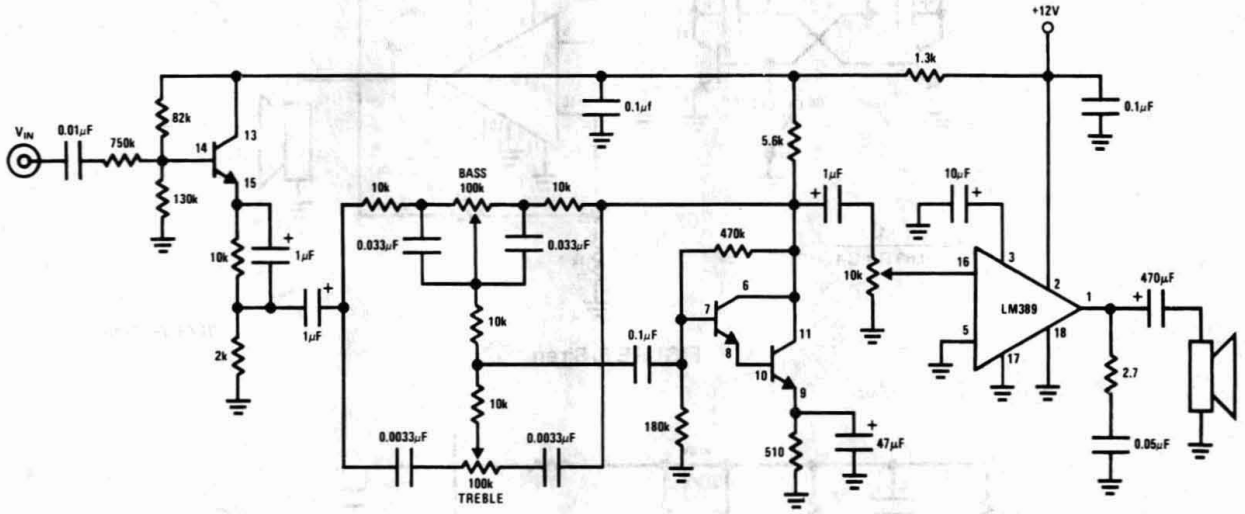
FIGURE 1. AM Radio

Application Hints (Continued)



TL/H/7847–7

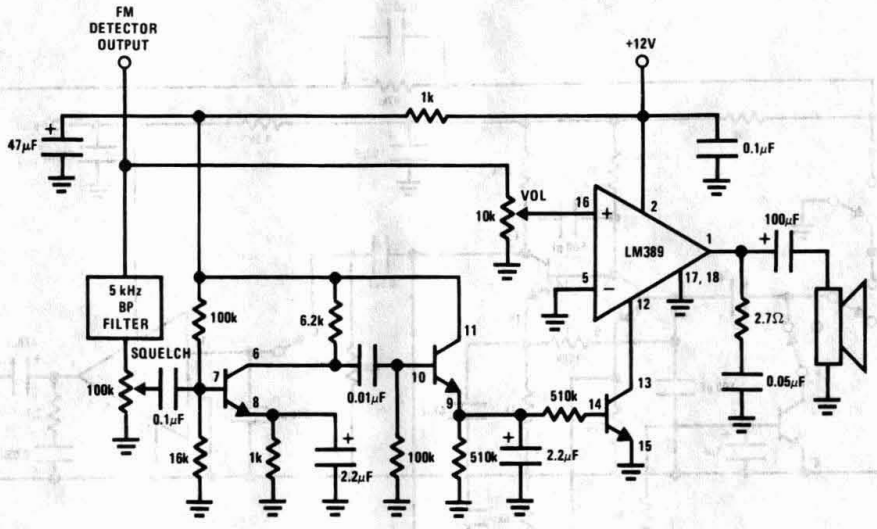
FIGURE 2. Tape Recorder



TL/H/7847–8

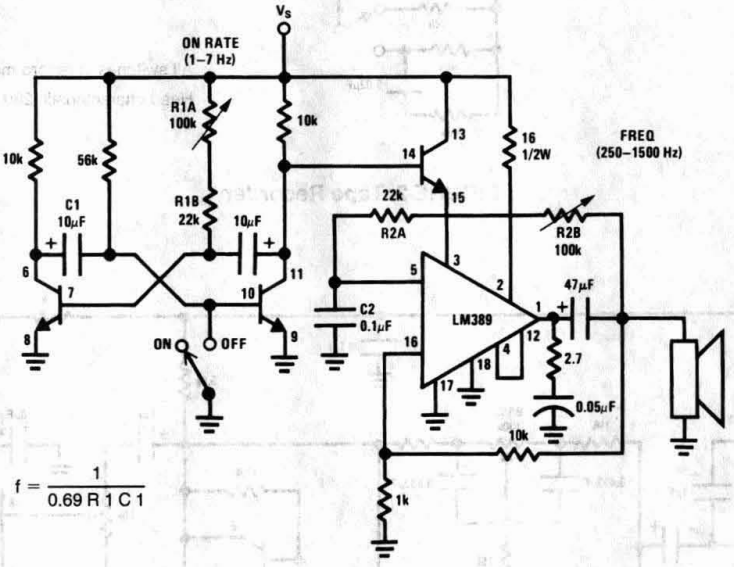
FIGURE 3. Ceramic Phono Amplifier with Tone Controls

Application Hints (Continued)



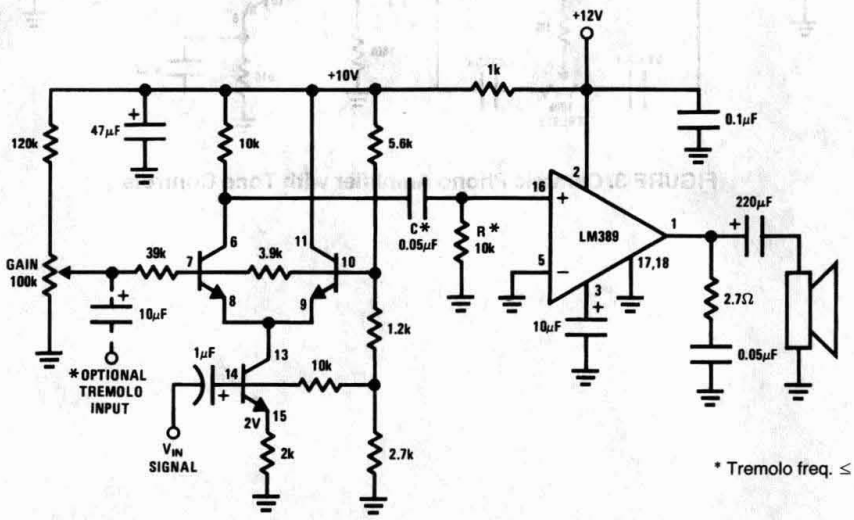
TL/H/7847–9

FIGURE 4. FM Scanner Noise Squelch Circuit



TL/H/7847–10

FIGURE 5. Siren



* Tremolo freq. $\leq \frac{1}{2\pi\ (R + 10k)C}$

TL/H/7847–11

FIGURE 6. Voltage-Controlled Amplifier or Tremolo Circuit

Application Hints (Continued)

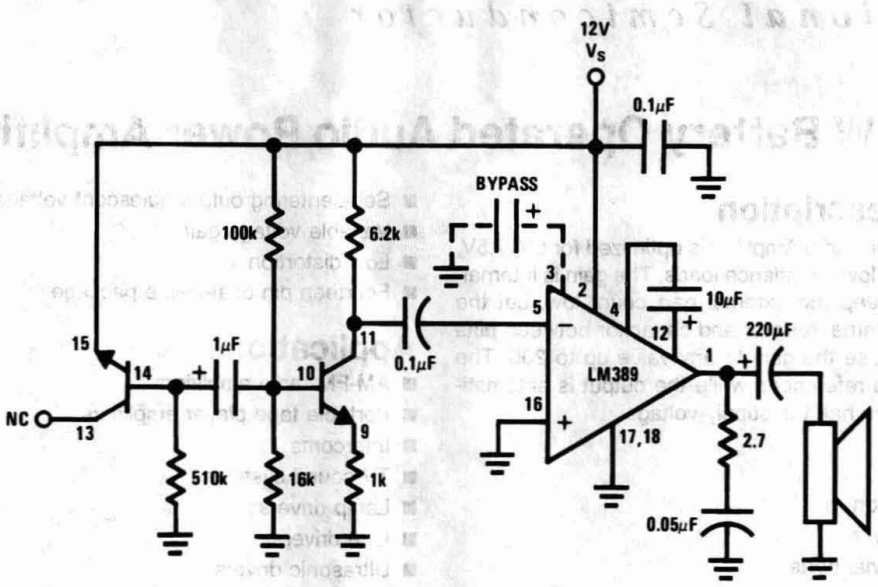


FIGURE 7. Noise Generator Using Zener Diode

National Semiconductor

LM390 1W Battery Operated Audio Power Amplifier

General Description

The LM390 Power Audio Amplifier is optimized for 6V, 7.5V, 9V operation into low impedance loads. The gain is internally set at 20 to keep the external part count low, but the addition of an external resistor and capacitor between pins 2 and 6 wil increase the gain to any value up to 200. The inputs are ground referenced while the output is automatically biased to one half the supply voltage.

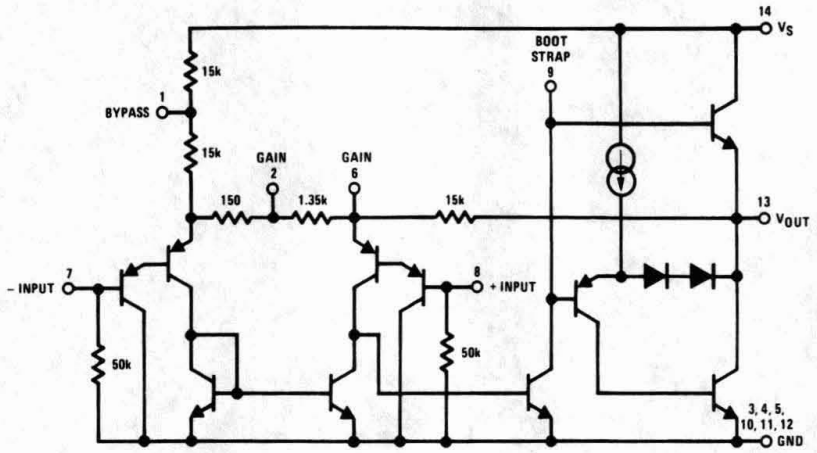
Features

- Battery operation
- 1W output power
- Minimum external parts
- Excellent supply rejection
- Ground referenced input
- Self-centering output quiescent voltage
- Variable voltage gain
- Low distortion
- Fourteen pin dual-in-line package

Applications

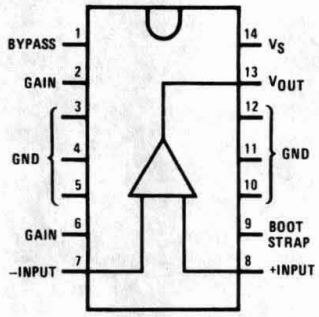
- AM-FM radio amplifiers
- Portable tape player amplifiers
- Intercoms
- TV sound systems
- Lamp drivers
- Line drivers
- Ultrasonic drivers
- Small servo drivers
- Power converters

Equivalent Schematic and Connection Diagrams



TL/H/7848–1

Dual-In-Line Package



TL/H/7848–2

Order Number LM390N
See NS Package Number N14A

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	10V
Package Dissipation 14-Pin DIP (Note 1)	8.3W
Input Voltage	±0.4V
Storage Temperature	−65°C to +150°C
Operating Temperature	0°C to +70°C
Junction Temperature	150°C
Lead Temperature (Soldering, 10 sec.)	260°C
Thermal Resistance	
θ_{JC}	30°C/W
θ_{JA}	79°C/W

Electrical Characteristics T_A = 25°C, *(Figure 1)*

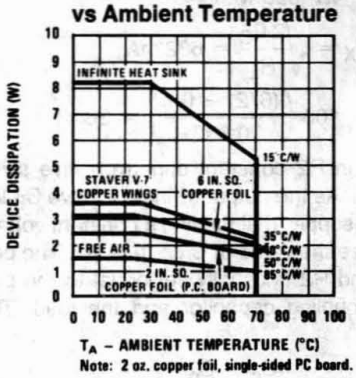
Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_S	Operating Supply Voltage		4		9	V
I_Q	Quiescent Current	V_S = 6V, V_{IN} = 0		10	20	mA
P_{OUT}	Output Power	V_S = 6V, R_L = 4Ω, THD = 10%	0.8	1.0		W
A_V	Voltage Gain	V_S = 6V, f = 1 kHz 10 μF from Pin 2 to 6	23	26 46	30	dB dB
BW	Bandwidth	V_S = 6V, Pins 2 and 6 Open		300		kHz
THD	Total Harmonic Distortion	V_S = 6V, R_L = 4Ω, P_{OUT} = 500 mW f = 1 kHz, Pins 2 and 6 Open		0.2	1	%
PSRR	Power Supply Rejection Ratio	V_S = 6V, f = 1 kHz, C_{BYPASS} = 10 μF, Pins 2 and 6 Open, Referred to Output (Note 2)		50		dB
R_{IN}	Input Resistance		10	50		kΩ
I_{BIAS}	Input Bias Current	V_S = 6V, Pins 7 and 8 Open		250		nA

Note 1: Pins 3, 4, 5, 10, 11, 12 at 25°C. Above 25°C case, derate at 15°C/W junction to case, or 85°C/W junction to ambient.

Note 2: If load and bypass capacitor are returned to V_S *(Figure 2)*, rather than ground *(Figure 1)*, PSRR is typically 30 dB.

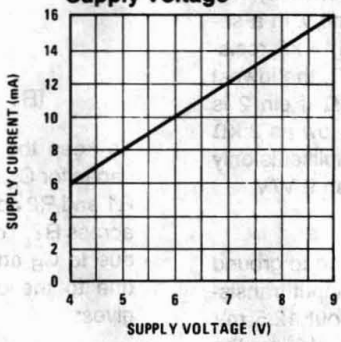
Typical Performance Characteristics

Maximum Device Dissipation vs Ambient Temperature

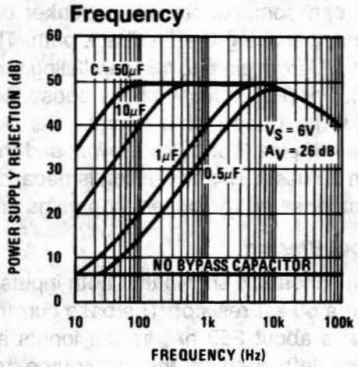


Note: 2 oz. copper foil, single-sided PC board.

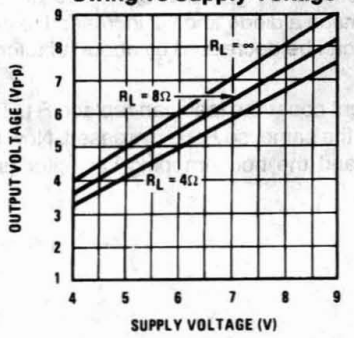
Quiescent Supply Current vs Supply Voltage



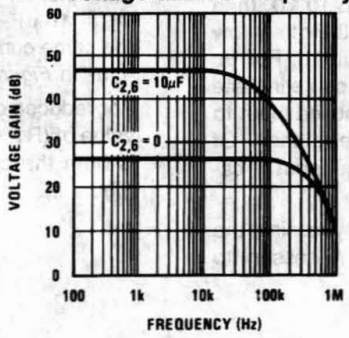
Power Supply Rejection Ratio (Referred to the Output) vs Frequency



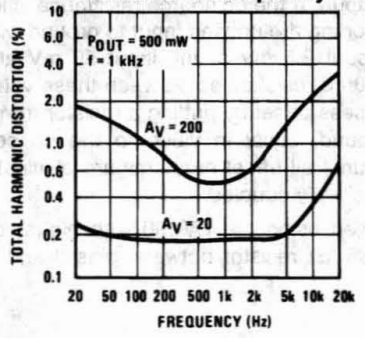
Peak-to-Peak Output Voltage Swing vs Supply Voltage



Voltage Gain vs Frequency



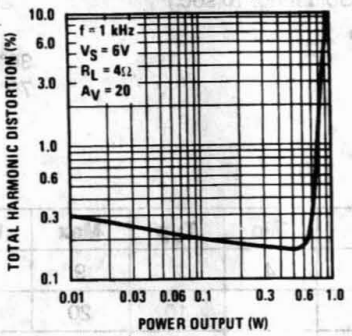
Distortion vs Frequency



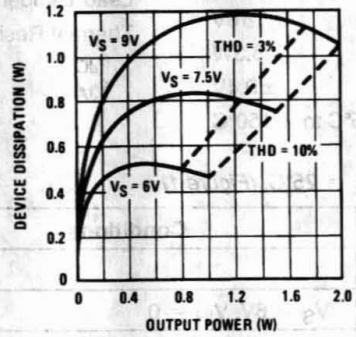
TL/H/7848–5

Typical Performance Characteristics (Continued)

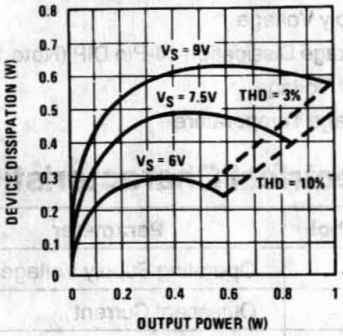
Distortion vs Output Power



Device Dissipation vs Output Power 4Ω Load



Device Dissipation vs Output Power 8Ω Load



TL/H/7848–6

Application Hints

Gain Control

To make the LM390 a more versatile amplifier, two pins (2 and 6) are provided for gain control. With pins 2 and 6 open, the 1.35 kΩ resistor sets the gain at 20 (26 dB). If a capacitor is put from pin 2 to 6, bypassing the 1.35 kΩ resistor, the gain will go up to 200 (46 dB). If a resistor is placed in series with the capacitor, the gain can be set to any value from 20 to 200. A low frequency pole in the gain response is caused by the capacitor working against the external resistor in series with the 150Ω internal resistor. If the capacitor is eliminated and a resistor connects pin 2 to 6 then the output dc level may shift due to the additional dc gain. Gain control can also be done by capacitively coupling a resistor (or FET) from pin 6 to ground, as in *Figure 7*.

Additional external components can be placed in parallel with the internal feedback resistors to tailor the gain and frequency response for individual applications. For example, we can compensate poor speaker bass response by frequency shaping the feedback path. This is done with a series RC from pin 6 to 13 (paralleling the internal 15 kΩ resistor). For 6 dB effective bass boost: R ≅ 15 kΩ, the lowest value for good stable operation is R = 10 kΩ if pin 2 is open. If pins 2 and 6 are bypassed then R as low as 2 kΩ can be used. This restriction is because the amplifier is only compensated for closed-loop gains greater than 9 V/V.

Input Biasing

The schematic shows that both inputs are biased to ground with a 50 kΩ resistor. The base current of the input transistors is about 250 nA, so the inputs are at about 12.5 mV when left open. If the dc source resistance driving the LM390 is higher than 250 kΩ it will contribute very little additional offset (about 2.5 mV at the input, 50 mV at the output). If the dc source resistance is less than 10 kΩ, then shorting the unused input to ground will keep the offset low (about 2.5 mV at the input 50 mV at the output). For dc source resistances between these values we can eliminate excess offset by putting a resistor from the unused input to ground, equal in value to the dc source resistance. Of course all offset problems are eliminated if the input is capacitively coupled.

When using the LM390 with higher gains (bypassing the 1.35 kΩ resistor between pins 2 and 6) it is necessary to bypass the unused input, preventing degradation of gain and possible instabilities. This is done with a 0.1 μF capacitor or a short to ground depending on the dc source resistance on the driven input.

Bootstrapping

The base of the output transistor of the LM390 is brought out to pin 9 for Bootstrapping. The output stage of the amplifier during positive swing is shown in *Figure 3* with its external circuitry.

R1 + R2 set the amount of base current available to the output transistor. The maximum output current divided by beta is the value required for the current in R1 and R2:

$$(R1 + R2) = \beta_O \frac{(V_S/2) - V_{BE}}{I_{O\,MAX}}$$

Good design values are $V_{BE} = 0.7V$ and $\beta_O = 100$.

Example 0.8 watt into 4Ω load with $V_S = 6V$.

$$I_{O\,MAX} = \sqrt{\frac{2P_O}{R_L}} = 632\ mA$$

$$(R1 + R2) = 100\left(\frac{(6/2) - 0.7}{0.632}\right) = 364\Omega$$

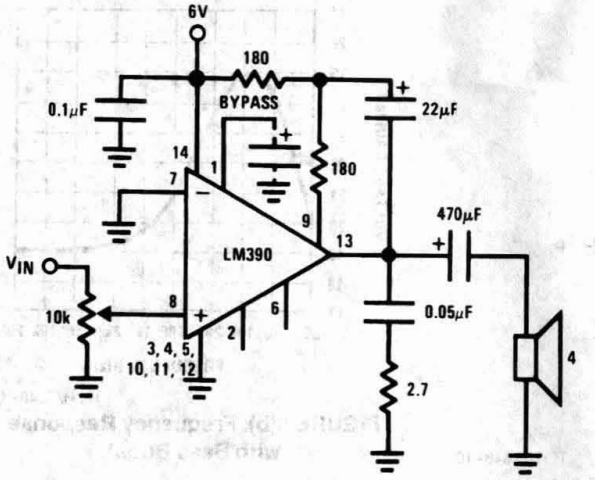
To keep the current in R2 constant during positive swing capacitor C_B is added. As the output swings positive C_B lifts R1 and R2 above the supply, maintaining a constant voltage across R2. To minimize the value of C_B, R1 = R2. The pole due to C_B and R1 and R2 is usually set equal to the pole due to the output coupling capacitor and the load. This gives:

$$C_B \cong \frac{4C_c}{\beta_O} \cong \frac{C_c}{25}$$

Example: for 100 Hz pole and $R_L = 4\Omega$; $C_c = 400\ \mu F$ and $C_B = 16\ \mu F$, if R1 is made a diode and R2 increased to give the same current, C_B can be decreased by about a factor of 4, as in *Figure 4*.

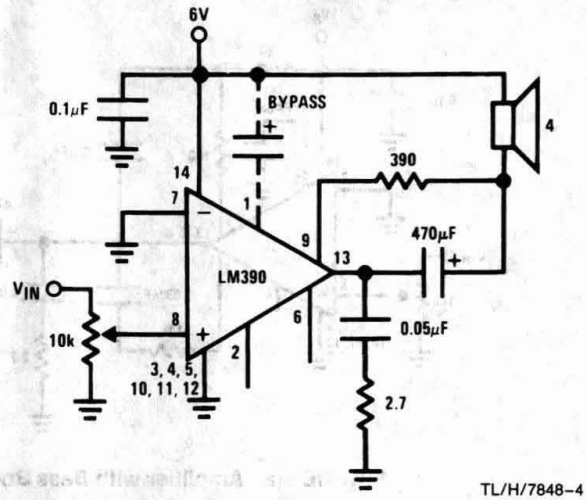
For reduced component count the load can replace R1. The value of (R1 + R2) is the same, so R2 is increased. Now C_B is both the coupling and the bootstrapping capacitor (see *Figure 2*).

Typical Applications



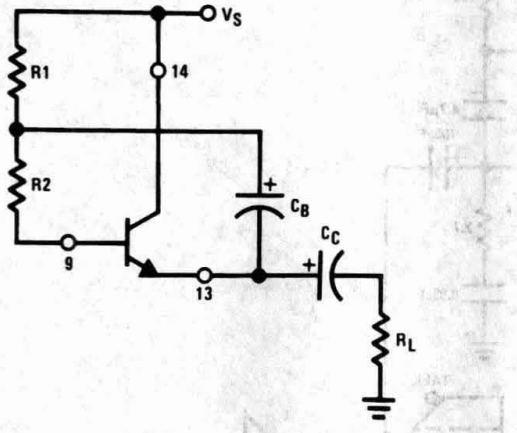
TL/H/7848–3

FIGURE 1. Load Returned to Ground (Amplifier with Gain = 20)



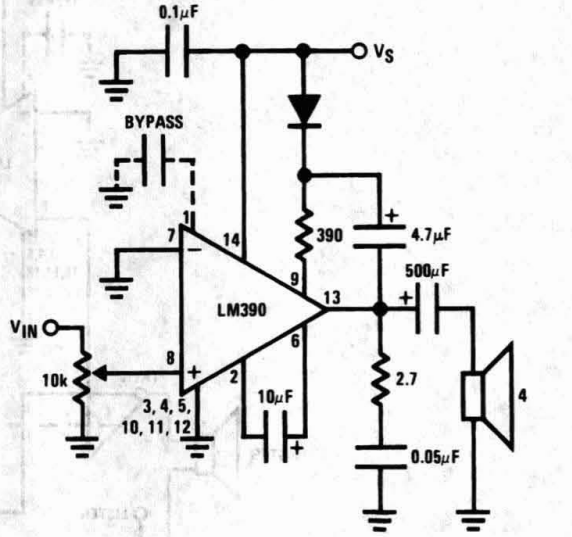
TL/H/7848–4

FIGURE 2. Load Returned to Supply (Amplifier with Gain = 20)



TL/H/7848–7

FIGURE 3



TL/H/7848–8

FIGURE 4. Amplifier with Gain = 200 and Minimum C_B

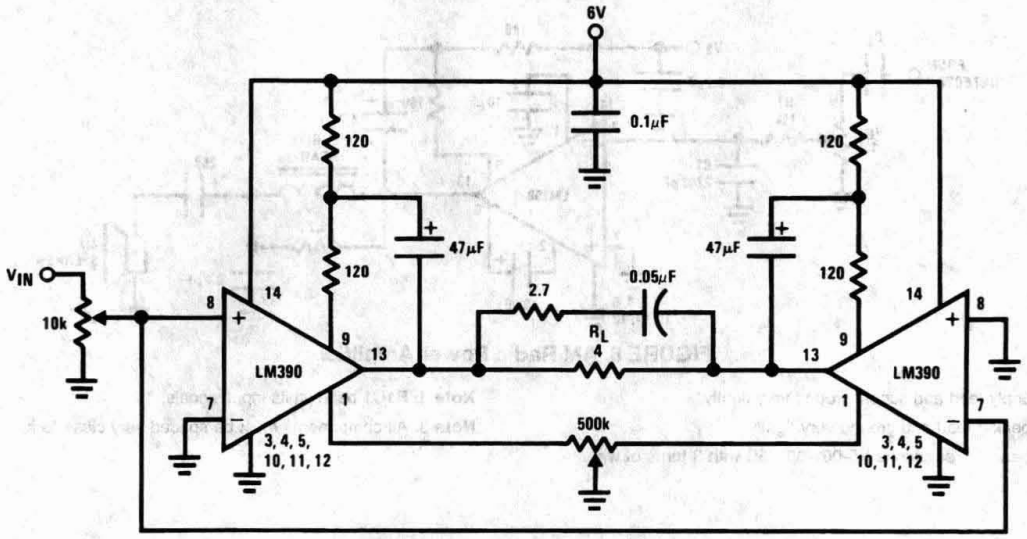


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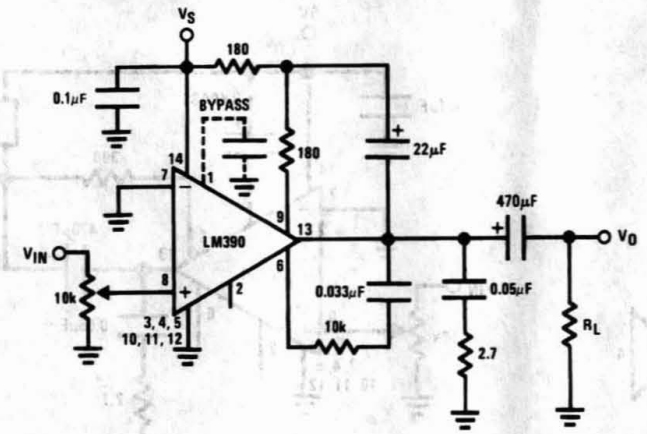
FIGURE 5. 2.5W Bridge Amplifier

Typical Applications (Continued)



TL/H/7848–10

FIGURE 6(a). Amplifier with Bass Boost

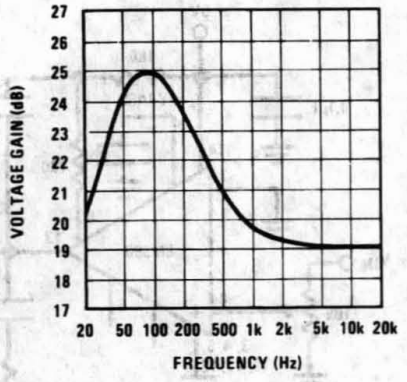


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FIGURE 6(b). Frequency Response with Bass Boost

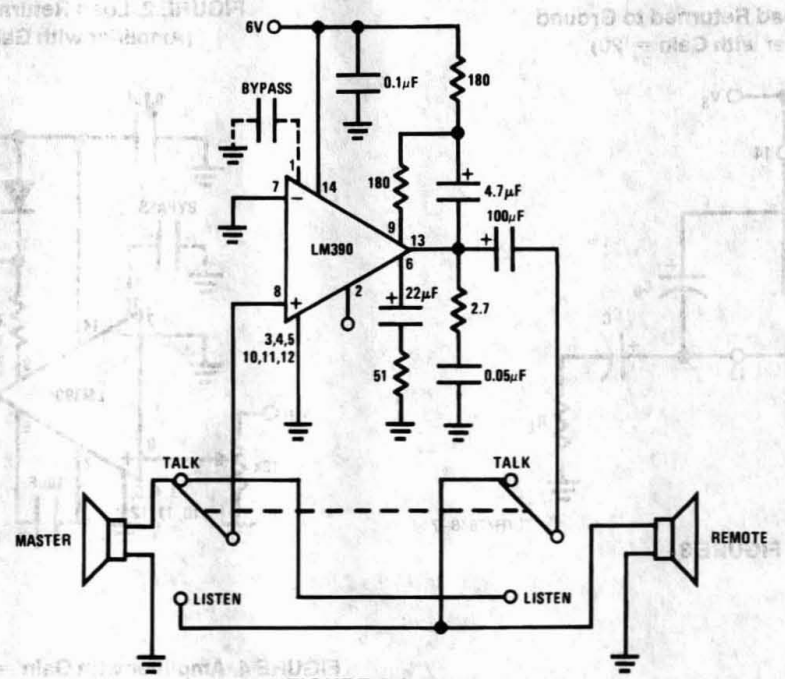

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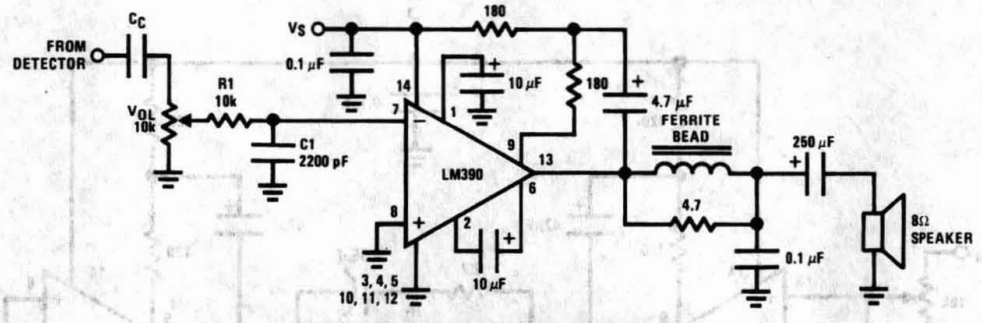
FIGURE 7. Intercom



TL/H/7848–13

FIGURE 8. AM Radio Power Amplifier

Note 1: Twist supply lead and supply ground very tightly.

Note 2: Twist speaker lead and ground very tightly.

Note 3: Ferrite bead is Ferroxcube K5-001-001/3B with 3 turns of wire.

Note 4: R1C1 band limits input signals.

Note 5: All components must be spaced very close to IC.

National Semiconductor

LM391 Audio Power Driver

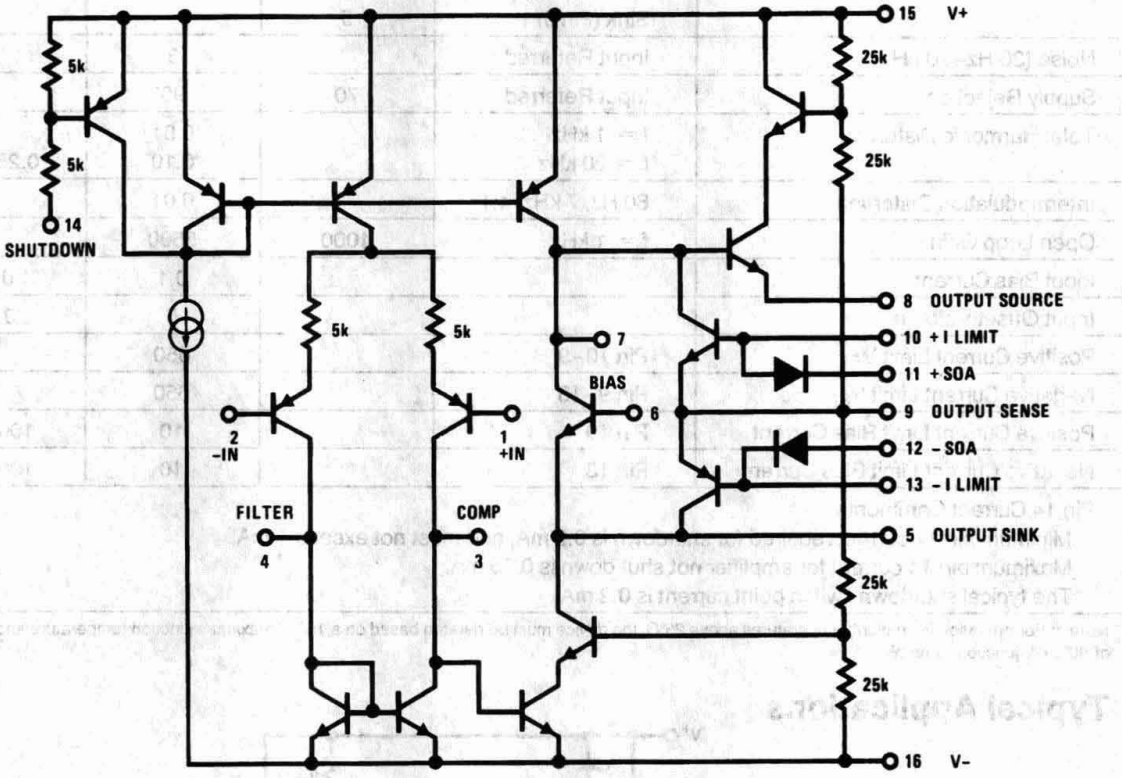
General Description

The LM391 audio power driver is designed to drive external power transistors in 10 to 100 watt power amplifier designs. High power supply voltage operation and true high fidelity performance distinguish this IC. The LM391 is internally protected for output faults and thermal overloads; circuitry providing output transistor protection is user programmable.

Features

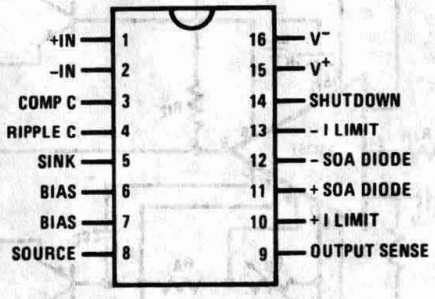
- High Supply Voltage ±50V max
- Low Distortion 0.01%
- Low Input Noise 3 μV
- High Supply Rejection 90 dB
- Gain and Bandwidth Selectable
- Dual Slope SOA Protection
- Shutdown Pin

Equivalent Schematic and Connection Diagram



TL/H/7146–1

Dual-In-Line Package



TL/H/7146–2

Top View

Order Number LM391N-100
See NS Package Number N16A

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	
LM391N-100	±50V or +100V
Input Voltage	Supply Voltage less 5V
Shutdown Current (Pin 14)	1 mA
Package Dissipation (Note 1)	1.39W
Storage Temperature	−65°C to +150°C
Operating Temperature	0°C to +70°C
Lead Temp. (Soldering, 10 sec.)	260°C
Thermal Resistance	
θ_{JC}	20°C/W
θ_{JA}	63°C/W

Electrical Characteristics $T_A = 25°C$ (The following are for $V^+ = 90\%\ V^+_{MAX}$ and $V^- = 90\%\ V^-_{MAX}$.)

Parameter	Conditions	Min	Typ	Max	Units
Quiescent Current LM391N-100	Current in Pin 15 $V_{IN} = 0$		 5	 6	mA
Output Swing	Positive Negative	$V^+ - 7$ $V^- + 7$	$V^+ - 5$ $V^- + 5$		V V
Drive Current	Source (Pin 8) Sink (Pin 5)	5 5			mA mA
Noise (20 Hz–20 kHz)	Input Referred		3		μV
Supply Rejection	Input Referred	70	90		dB
Total Harmonic Distortion	f = 1 kHz f = 20 kHz		0.01 0.10	 0.25	% %
Intermodulation Distortion	60 Hz, 7 kHz, 4:1		0.01		%
Open Loop Gain	f = 1 kHz	1000	5500		V/V
Input Bias Current			0.1	1.0	μA
Input Offset Voltage			5	20	mV
Positive Current Limit V_{BE}	Pin 10–9		650		mV
Negative Current Limit V_{BE}	Pin 9–13		650		mV
Positive Current Limit Bias Current	Pin 10		10	100	μA
Negative Current Limit Bias Current	Pin 13		10	100	μA

Pin 14 Current Comments

Minimum pin 14 current required for shutdown is 0.5 mA, and must not exceed 1 mA.
Maximum pin 14 current for amplifier not shut down is 0.05 mA.
The typical shutdown switch point current is 0.2 mA.

Note 1: For operation in ambient temperatures above 25°C, the device must be derated based on a 150°C maximum junction temperature and a thermal resistance of 90°C/W junction to ambient.

Typical Applications

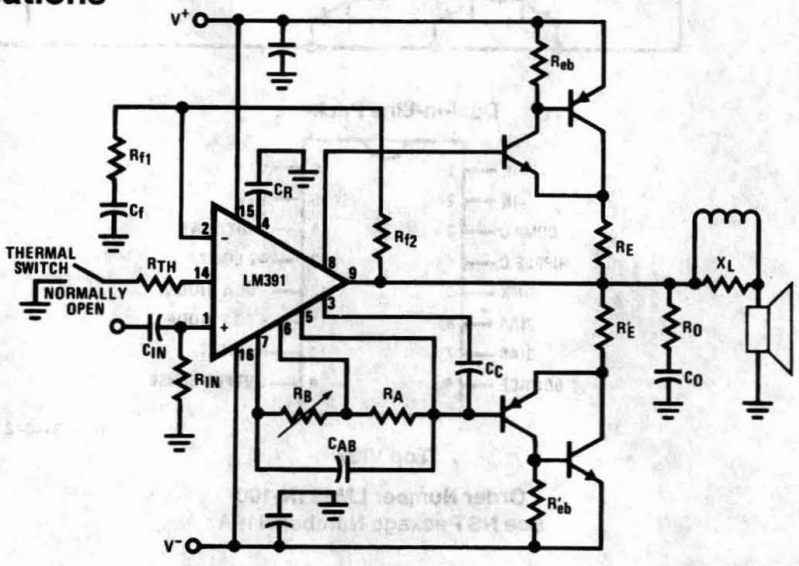


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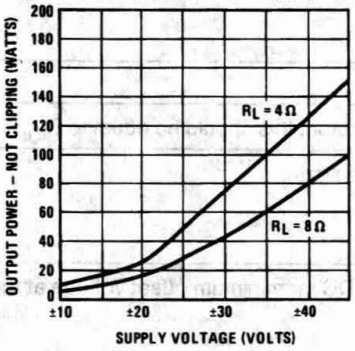
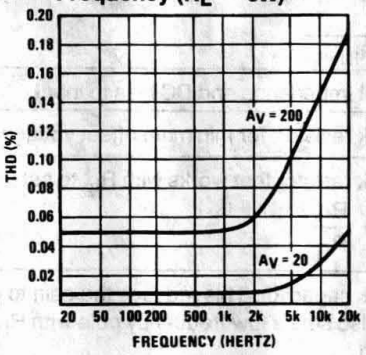
FIGURE 1. LM391 with External Components—Protection Circuitry Not Shown

Typical Performance Characteristics

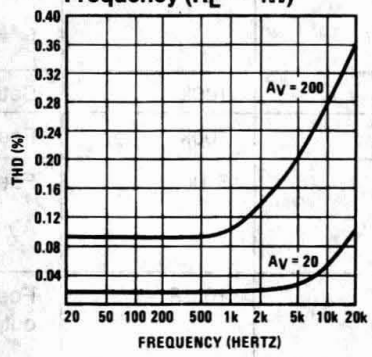
Output Power vs Supply Voltage



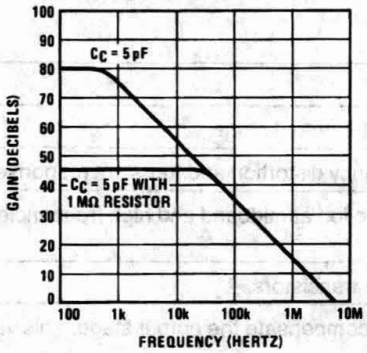
Total Harmonic Distortion vs Frequency ($R_L = 8\Omega$)



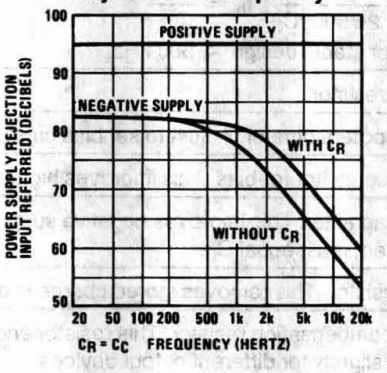
Total Harmonic Distortion vs Frequency ($R_L = 4\Omega$)



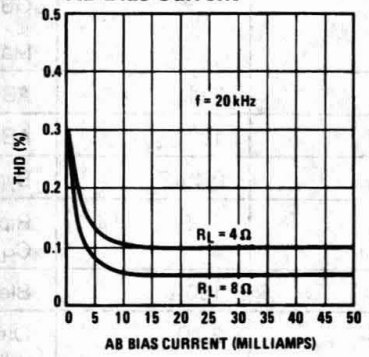
Open Loop Gain vs Frequency



Input Referred Power Supply Rejection vs Frequency



Total Harmonic Distortion vs AB Bias Current



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Pin Descriptions

Pin No.	Pin Name	Comments
1	+ Input	Audio input
2	− Input	Feedback input
3	Compensation	Sets the dominant pole
4	Ripple Filter	Improves negative supply rejection
5	Sink Output	Drives output devices and is emitter of AB bias V_{BE} multiplier
6	BIAS	Base of V_{BE} multiplier
7	BIAS	Collector of V_{BE} multiplier
8	Source Output	Drives output devices
9	Output Sense	Biases the IC and is used in protection circuits
10	+ Current Limit	Base of positive side protection circuit transistor
11	+ SOA Diode	Diode used for dual slope SOA protection
12	− SOA Diode	Diode used for dual slope SOA protection
13	− Current Limit	Base of negative side protection circuit transistor
14	Shutdown	Shuts off amplifier when current is pulled out of pin
15	V+	Positive supply
16	V−	Negative supply

External Components (Figure 1)

Component	Typical Value	Comments
C_{IN}	1 μF	Input coupling capacitor sets a low frequency pole with R_{IN}. $f_L = \frac{1}{2\pi R_{IN} C_{IN}}$
R_{IN}	100k	Sets input impedance and DC bias to input.
R_{f_2}	100k	Feedback resistor; for minimum offset voltage at the output this should be equal to R_{IN}.
R_{f_1}	5.1k	Feedback resistor that works with R_{f_2} to set the voltage gain. $A_V = 1 + \frac{R_{f_2}}{R_{f_1}}$
C_f	10 μF	Feedback capacitor. This reduces the gain to unity at DC for minimum offset voltage at the output. Also sets a low frequency pole with R_{f_1}. $f_L = \frac{1}{2\pi R_{f_1} C_f}$
C_C	5 pF	Compensation capacitor. Sets gain bandwidth product and a high frequency pole. $GBW = \frac{1}{2\pi 5000 C_C}$, $f_h = \frac{GBW}{A_V}$ Max f_h for stable design $\approx$ 500 kHz.
R_A	3.9k	AB bias resistor.
R_B	10k	AB bias potentiometer. Adjust to set bias current in the output stage.
C_{AB}	0.1 μF	Bypass capacitor for bias. This improves high frequency distortion and transient response.
C_R	5 pF	Ripple capacitor. This improves negative supply rejection at midband and high frequencies. C_R, if used, must equal C_C.
R_{eb}	100Ω	Bleed resistor. This removes stored charge in output transistors.
R_O	2.7Ω	Output compensation resistor. This resistor and C_O compensate the output stage. This value will vary slightly for different output devices.
C_O	0.1 μF	Output compensation capacitor. This works with R_O to form a zero that cancels f_β of the output power transistors.
R_E	0.3Ω	Emitter degeneration resistor. This resistor gives thermal stability to the output stage quiescent current. IRC PW5 type.
R_{TH}	39k	Shutdown resistor. Sets the amount of current pulled out of pin 14 during shutdown.
C_2, C'_2	1000 pF	Compensation capacitors for protection circuitry.
X_L	10$\Omega | |$5 μH	Used to isolate capacitive loads, usually 20 turns of wire wrapped around a 10Ω, 2W resistor.

Application Hints

GENERALIZED AUDIO POWER AMP DESIGN

Givens: Power Output
Load Impedance
Input Sensitivity
Input Impedance
Bandwidth

The power output and load impedance determine the power supply requirements. Output signal swing and current are found from:

$$V_{Opeak} = \sqrt{2 R_L P_O} \quad (1)$$

$$I_{Opeak} = \sqrt{\frac{2 P_O}{R_L}} \quad (2)$$

Add 5 volts to the peak output swing (V_{OP}) for transistor voltage to get the supplies, i.e., $\pm$ (V_{OP} + 5V) at a current of I_{peak}. The regulation of the supply determines the unloaded voltage, usually about 15% higher. Supply voltage will also rise 10% during high line conditions.

$$\text{max supplies} \approx \pm(V_{Opeak} + 5)\,(1 + \text{regulation})\,(1.1) \quad (3)$$

The input sensitivity and output power specs determine the required gain.

$$A_V \geq \frac{\sqrt{P_O R_L}}{V_{IN}} = \frac{V_{ORMS}}{V_{INRMS}} \quad (4)$$

Normally the gain is set between 20 and 200; for a 25 watt, 8 ohm amplifier this results in a sensitivity of 710 mV and 71 mV, respectively. The higher the gain, the higher the THD, as can be seen from the characteristics curves. Higher gain also results in more hum and noise at the output.

The desired input impedance is set by R_{IN}. Very high values can cause board layout problems and DC offsets at the output. The bandwidth requirements determine the size of C_f and C_C as indicated in the external component listing.

The output transistors and drivers must have a breakdown voltage greater than the voltage determined by equation (3). The current gain of the drive and output device must be high enough to supply I_{Opeak} with 5 mA of drive from the LM391. The power transistors must be able to dissipate approximately 40% of the maximum output power; the drivers must dissipate this amount divided by the current gain of the outputs. See the output transistor selection guide, Table A.

To prevent thermal runaway of the AB bias current the following equation must be valid:

$$\theta_{JA} \leq \frac{R_E (\beta_{MIN} + 1)}{V_{CEQMAX}\,(K)} \quad (5)$$

where:

θ_{JA} is the thermal resistance of the driver transistor, junction to ambient, in °C/W.

R_E is the emitter degeneration resistance in ohms.

β_{min} is that of the output transistor.

V_{CEQMAX} is the highest possible value of one supply from equation (3).

K is the temperature coefficient of the driver base-emitter voltage, typically 2 mV/°C.

Often the value of R_E is to be determined and equation (5) is rearranged to be:

$$R_E \geq \frac{\theta_{JA}\,(V_{CEQMAX})\,K}{\beta_{MIN} + 1} \quad (6)$$

The maximum average power dissipation in each output transistor is:

$$\overline{P_{DMAX}} = 0.4\,P_{OMAX} \quad (7)$$

The power dissipation in the driver transistor is:

$$\overline{P_{DRIVER(MAX)}} = \frac{\overline{P_{DMAX}}}{\beta_{MIN}} \quad (8)$$

Heat sink requirements are found using the following formulas:

$$\theta_{JA} \leq \frac{T_{JMAX} - T_{AMAX}}{P_D} \quad (9)$$

$$\theta_{SA} \leq \theta_{JA} - \theta_{JC} - \theta_{CS} \quad (10)$$

where:

T_{jMAX} is the maximum transistor junction temperature.

T_{AMAX} is the maximum ambient temperature.

θ_{JA} is thermal resistance junction to ambient.

θ_{SA} is thermal resistance sink to ambient.

θ_{JC} is thermal resistance junction to case.

θ_{CS} is thermal resistance case to sink, typically 1°C/W for most mountings.

Application Hints (Continued)

PROTECTION CIRCUITRY

The protection circuits of the LM391 are very flexible and should be tailored to the output transistor's safe operating area. The protection V-I characteristics, circuitry, and resistor formulas are described below. The diodes from the output to each supply prevent the output voltage from exceeding the supplies and harming the output transistors. The output will do this if the protection circuitry is activated while driving an inductive load.

TURN-ON DELAY

It is often desirable to delay the turn-ON of the power amplifier. This is easily implemented by putting a resistor in series with a capacitor from pin 14 to ground. The value of the resistor is set to limit the current to less than 1 mA (the absolute maximum). This resistor with the capacitor gives a time constant of RC. The turn-ON delay is approximately 2 time constants.

Example:

Amplifier with maximum supply of 30V, like the 20W, 8Ω example in the data sheet, requiring a delay of 1 second.

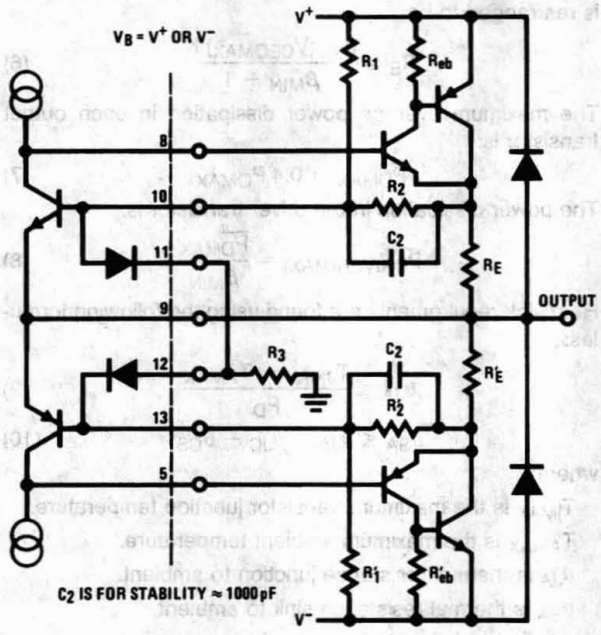
Time delay = 2 RC

$$R = \frac{\text{Max } V^+}{1\text{ mA}}$$

So:

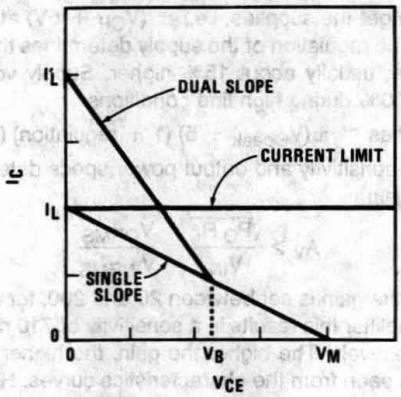
R = 30k. Solving for C gives 16.7 μF. Use C = 20 μF with a 30V rating.

Protection Circuitry with External Components



TL/H/7146–5

Protection Characteristics



TL/H/7146–6

Protection Circuit Resistor Formulas ($V_B = V^+$)

Type of Protection	R_E, R'	R_1, R'_1	R_2, R'_2	R_3, R'_3
Current Limit	$R_E = \frac{\phi}{I_L}$	Not Required	Short	Not Required
Single Slope SOA Protection	$R_E = \frac{\phi}{I_L}$	$R_1 = R_2\left(\frac{V_M - \phi}{\phi}\right)$	1 kΩ	Not Required
Dual Slope SOA Protection ($V_B = V^+$)	$R_E = \frac{\phi}{I_L}$	$R_1 = R_2\left(\frac{V_M - \phi}{\phi}\right)$	1 kΩ	$R_3 = R_2\left[\frac{V^+}{I_L R_E - \phi} - 1\right]$

Note: ϕ is the current limit V_{BE} voltage, 650 mV. Assumptions: $V^+ >> \phi$, $V_M >> \phi$. V^+ is the load supply voltage. V_M is the maximum rated V_{CE} of the output transistors.

Application Hints (Continued)

TRANSIENT INTERMODULATION DISTORTION

There has been a lot of interest in recent years about transient intermodulation distortion. Matti Otala of University of Oulu, Oulu, Finland has published several papers on the subject. The results of these investigations show that the open loop pole of the power amplifier should be above 20 kHz.

To do this with the LM391 is easy. Put a 1 MΩ resistor from pin 3 to the output and the open loop gain is reduced to about 46 dB. Now the open loop pole is at 30 kHz. The current in this resistor causes an offset in the input stage that can be cancelled with a resistor from pin 4 to ground. The resistor from pin 4 to ground should be 910 kΩ rather than 1 MΩ to insure that the shutdown circuitry will operate correctly. The slight difference in resistors results in about 15 mV of offset. The 40W, 8Ω amplifier schematic shows the hookup of these two resistors.

BRIDGE AMPLIFIER

A switch can be added to convert a stereo amplifer to a single bridge amplifer. The diagram below shows where the switch and one resistor are added. When operating in the bridge mode the output load is connected between the two outputs, the input is V_{IN} #1, and V_{IN} #2 is disconnected.

OSCILLATIONS & GROUNDING

Most power amplifiers work the first time they are turned on. They also tend to oscillate and have excess THD. Most oscillation problems are due to inadequate supply bypassing and/or ground loops. A 10 μF, 50V electrolytic on each power supply will stop supply-related oscillations. However, if the signal ground is used for these bypass caps the THD is usually excessive. The signal ground must return to the power supply alone, as must the output load ground. All other grounds—bypass, output R-C, protection, etc., can tie together and then return to supply. This ground is called high frequency ground. On the 40W amplifier schematic all the grounds are labeled.

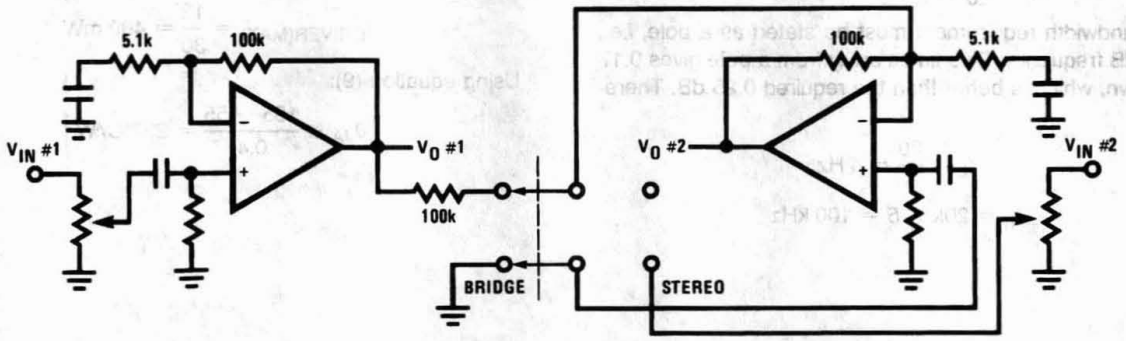
Capacitive loads can cause instabilities, so they are isolated from the amplifier with an inductor and resistor in the output lead.

AB BIAS CURRENT

To reduce distortion in the output stage, all the transistors are biased ON slightly. This results in class AB operation and reduces the crossover (notch) distortion of the class B stage to a low level, (see performance curve, THD vs AB bias). The potentiometer, R_B, from pins 6–7 is adjusted to give about 25 mA of current in the output stage. This current is usually monitored at the supply or by measuring the voltage across R_E.

Typical Applications (Continued)

Bridge Circuit Diagram



TL/H/7146–7

Output Transistors Selection Guide

Table A.

Power Output	Driver Transistor		Output Transistor	
	PNP	NPN	PNP	NPN
20W @ 8Ω 30W @ 4Ω	MJE711 MJE171 D43C8	MJE721 MJE181 D42C8	TIP42A 2N6490	TIP41A 2N6487
40W @ 8Ω 60W @ 4Ω	MJE712 MJE172 D43C11	MJE722 MJE182 D42C11	2N5882	2N5880

Application Hints (Continued)

A 20W, 8Ω; 30W, 4Ω AMPLIFIER

Givens:

Power Output	20W into 8Ω 30W into 4Ω
Input Sensitivity	1V Max
Input Impedance	100k
Bandwidth	20 Hz–20 kHz ± 0.25 dB

Equations (1) and (2) give:

20W/8Ω $V_{OP} = 17.9V$ $I_{OP} = 2.24A$

30W/4Ω $V_{OP} = 15.5V$ $I_{OP} = 3.87A$

Therefore the supply required is:

±23V @ 2.24A, reducing to . . .

±21V @ 3.87A

With 15% regulation and high line we get ±29V from equation (3).

Sensitivity and equation (4) set minimum gain:

$$A_V \geq \frac{\sqrt{20 \times 8}}{1} = 12.65$$

We will use a gain of 20 with resulting sensitivity of 632 mV.

Letting R_{IN} equal 100k gives the required input impedance. For low DC offsets at the output we let $R_{f_2} = 100k$. Solving for R_{f_1} gives:

$$R_{f_2} = 100k$$

$$R_{f_1} = \frac{100k}{20 - 1} = 5.26k; \text{ use } 5.1k$$

The bandwidth requirement must be stated as a pole, i.e., the 3 dB frequency. Five times away from a pole gives 0.17 dB down, which is better than the required 0.25 dB. Therefore:

$$f_L = \frac{20}{5} = 4 \text{ Hz}$$

$$f_h = 20k \times 5 = 100 \text{ kHz}$$

Solving for C_f:

$$C_f \geq \frac{1}{2\pi R_{f_1} f_L} = 7.8\ \mu F; \text{ use } 10\ \mu F$$

The recommended value for C_C is 5 pF for gains of 20 or larger. This gives a gain-bandwidth product of 6.4 MHz and a resulting bandwidth of 320 kHz, better than required.

The breakdown voltage requirement is set by the maximum supply; we need a minimum of 58V and will use 60V. We must now select a 60V power transistor with reasonable beta at I_{Opeak}, 3.87A. The TIP42, TIP41 complementary pair are 60V, 60W transistors with a minimum beta of 30 at 4A. The driver transistor must supply the base drive given 5 mA drive from the LM391. The MJE711, MJE721 complementary driver transistors are 60V devices with a minimum beta of 40 at 200 mA. The driver transistors should be much faster (higher f_T) than the output transistors to insure that the R-C on the output will prevent instability.

To find the heat sink required for each output transistor we use equations (7), (9), and (10):

$$\overline{P_D} = 0.4\,(30) = 12W \quad (7)$$

$$\theta_{JA} \leq \frac{150°C - 55°C}{12} = 7.9°C/W \text{ for } T_{AMAX} = 55°C \quad (9)$$

$$\theta_{SA} \leq 7.9 - 2.1 - 1.0 = 4.8°C/W \quad (10)$$

If both transistors are mounted on one heat sink the thermal resistance should be halved to 2.4°C/W.

The maximum average power dissipation in each driver is found using equation (8):

$$\overline{P_{DRIVER(MAX)}} = \frac{12}{30} = 400 \text{ mW}$$

Using equation (9):

$$\theta_{JA} \leq \frac{155 - 55}{0.4} = 237°C/W$$

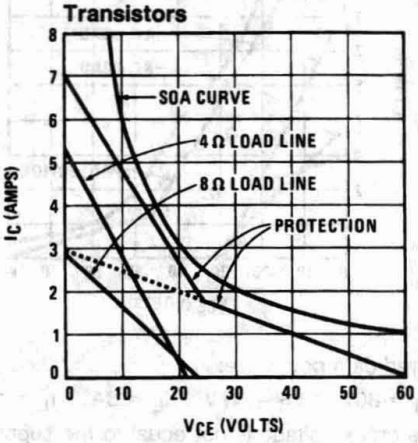
Application Hints (Continued)

Since the free air thermal resistance of the MJE711, MJE721 is 100°C/W, no heat sink is required. Using this information and equation (6) we can find the minimum value of R_E required to prevent thermal runaway.

$$R_E \geq \frac{100\,(30)\,(0.002)}{30+1} = 0.19\Omega \qquad (6)$$

We must now use the SOA data on the TIP42, TIP41 transistors to set up the protection circuit. Below is the SOA curve with the 4Ω and 8Ω load lines. Also shown are the desired protection lines. Note the value of V_B is equal to the supply voltage, so we use the formulas in the table.

D.C. SOA of TIP42, TIP41 Transistors



TL/H/7146–8

The data points from the curve are:

$$V_M = 60V,\ V_B = 23V,\ I_L = 3A,\ I_L' = 7A$$

Using the dual slope protection formulas:

$$R_E = \frac{0.65}{3} = 0.22\Omega$$

$$R_2 = 1k$$

$$R_1 = 1k\left(\frac{60-0.65}{0.65}\right) \approx 91k$$

$$R_3 = 1k\left(\frac{23}{7(0.22)-0.65} - 1\right) \approx 24k$$

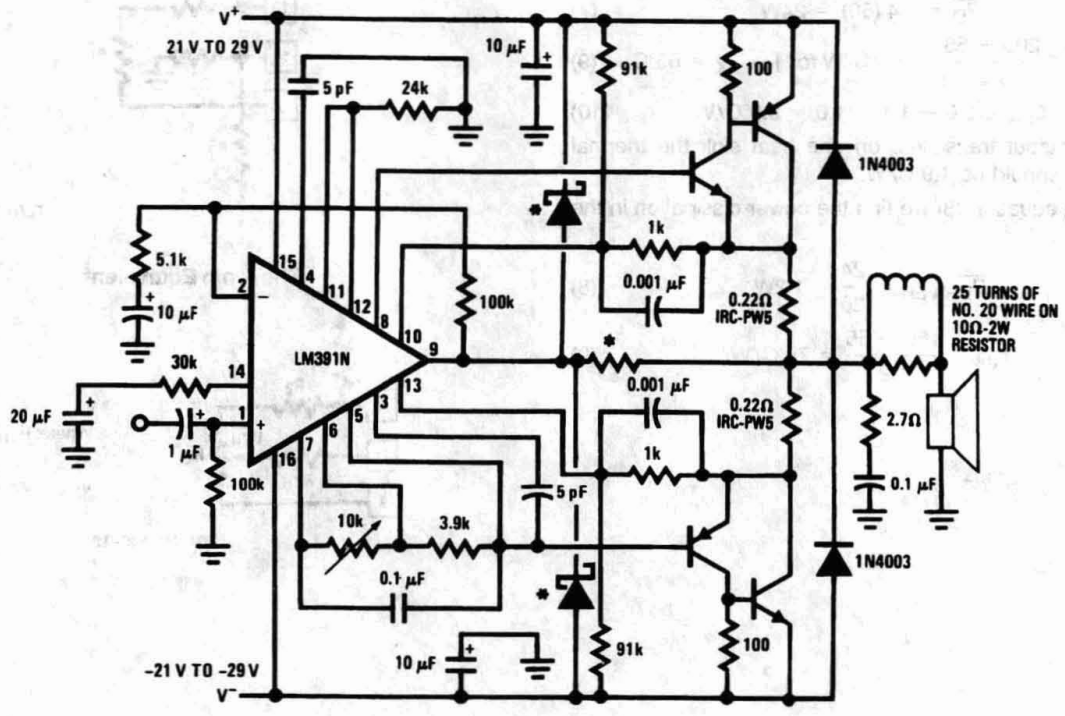
Note that an R_E of 0.22Ω satisfies equation (6). The final schematic of this amplifier is below. If the output is shorted the current will be 1.8A and V_{CE} is 23V. Since the input is AC, the average power is:

$$\text{short } \overline{P_D} = \tfrac{1}{2}(1.8)\,(23) \approx 21W$$

This power is greater than was used in the heat sink calculations, so the transistors will overheat for long-duration shorts unless a larger heat sink is used.

Typical Applications (Continued)

20W-8Ω, 30W-4Ω Amplifier with 1 Second Turn-ON Delay



TL/H/7146–9

*Additional protection for LM391N; Schottky diodes and R ≅ 100Ω.

Application Hints (Continued)

A 40W/8Ω, 60W/4Ω AMPLIFIER

Given:

Power Output	40W/8Ω 60W/4Ω
Input Sensitivity	1V Max
Input Impedance	100k
Bandwidth	20 Hz–20 kHz ± 0.25 dB

Equations (1) and (2) give:

40W/8Ω $V_{OPeak} = 25.3V$ $I_{OPeak} = 3.16A$

60W/4Ω $V_{OPeak} = 21.9V$ $I_{OPeak} = 5.48A$

Therefore the supply required is:

±30.3V @ 3.16A, reducing to . . .

±26.9V @ 5.48A

With 15% regulation and high line we get ±38.3V using equation (3).

The minimum gain from equation (4) is:

$$A_V \geq 18$$

We select a gain of 20; resulting sensitivity is 900 mV.

The input impedance and bandwidth are the same as the 20 watt amplifier so the components are the same.

$R_{f_1} = 5.1k$ $R_{IN} = 100k$ $C_C = 5\ pF$

$R_{f_2} = 100k$ $C_f = 10\ \mu F$

The maximum supplies dictate using 80V devices. The 2N5882, 2N5880 pair are 80V, 160W transistors with a minimum beta of 40 at 2A and 20 at 6A. This corresponds to a minimum beta of 22.5 at 5.5A (I_{Opeak}). The MJE712, MJE722 driver pair are 80V transistors with a minimum beta of 50 at 250 mA. This output combination guarantees I_{Opeak} with 5 mA from the LM391.

Output transistor heat sink requirements are found using equations (7), (9), and (10):

$$\overline{P_D} = 0.4\,(60) = 24W \quad (7)$$

$$\theta_{JA} \leq \frac{200 - 55}{24} = 6.0°C/W \text{ for } T_{AMAX} = 55°C \quad (9)$$

$$\theta_{SA} \leq 6.0 - 1.1 - 1.0 = 3.9°C/W \quad (10)$$

For both output transistors on one heat sink the thermal resistance should be 1.9°C/W.

Now using equation (8) we find the power dissipation in the driver:

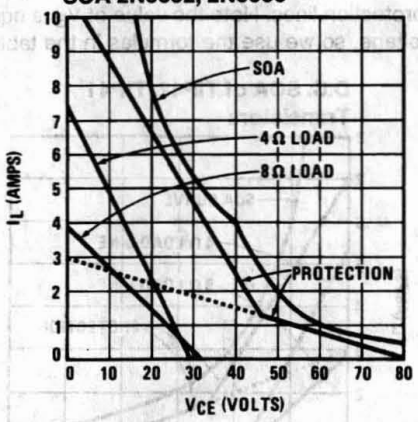
$$\overline{P_{DRIVER}} = \frac{24}{20} = 1.2W \quad (8)$$

$$\theta_{JA} \leq \frac{150 - 55}{1.2} = 79°C/W \quad (9)$$

Since a heat sink is required on the driver, we should investigate the output stage thermal stability at the same time to optimize the design. If we find a value of R_E that is good for the protection circuitry, we can then use equation (5) to find the heat sink required for the drivers.

The SOA characteristics of the 2N5882, 2N5880 transistors are shown in the following curve along with a desired protection line.

SOA 2N5882, 2N5880



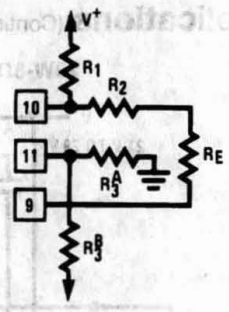
TL/H/7146–10

The desired data points are:

$V_M = 80V$ $V_B = 47V$ $I_L = 3A$ $I_L' = 11A$

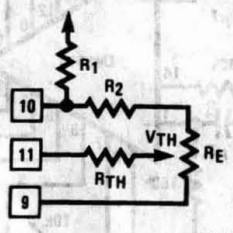
Since the break voltage is not equal to the supply, we will use two resistors to replace R_3 and move V_B.

Circuit Used



TL/H/7146–11

Thevenin Equivalent



Where: $R_{TH} = R_3^A \parallel R_3^B$

$$V_{TH} = V^- \left[\frac{R_3^A}{R_3^A + R_3^B}\right]$$

TL/H/7146–12

Application Hints (Continued)

The formulas for R_E, R_1, and R_2 do not change:

$$R_E = \frac{0.65}{3A} = 0.22\Omega$$

$$R_2 = 1k \qquad R_1 = 1k\frac{80 - 0.65}{0.65} = 120k$$

The formula for R_3 now gives R_{TH} when the V^+ in the formula becomes V_B.

$$R_{TH} = R_2\left[\frac{V_B}{I_L R_E - \phi} - 1\right]$$

$$= 1k\left[\frac{47}{11\,(0.22) - 0.65} - 1\right] = 25.55k$$

V_{TH} is the additional voltage added to the supply voltage to get V_B.

$$V_{TH} = -(V_B - V^+) = -(47 - 30) = -17V$$

Now we must find R_3^A and R_3^B using the Thevenin formulas. Putting V_{TH}, V^-, and R_{TH} into the appropriate formulas reduces to:

$$R_3^B = 0.76\,R_3^A \qquad \text{and} \qquad 25.55k = R_3^A \,||\, R_3^B$$

The easiest way to solve these equations is to iterate with standard values. If we guess $R_3^A = 62k$, then $R_3^B = 47.12k$; use 47k. The Thevenin impedance comes out 26.7k, which is close enough to 25.55k.

Now we will use equation (5) to determine the heat sinking requirements of the drivers to insure thermal stability:

$$\theta_{JA} \le \frac{0.22\,(20 + 1)}{40\,(0.002)} \approx 57°C/W \qquad (5)$$

This value is lower than we got with equation (9), so we will use it in equation (10):

$$\theta_{SA} \le 57 - 6 - 1 = 50°C/W \qquad (10)$$

This is the required heat sink for each driver. For low TIM we add the 1 MΩ resistor from pin 3 to the output and a 910k resistor from pin 4 to ground. The complete schematic is shown below.

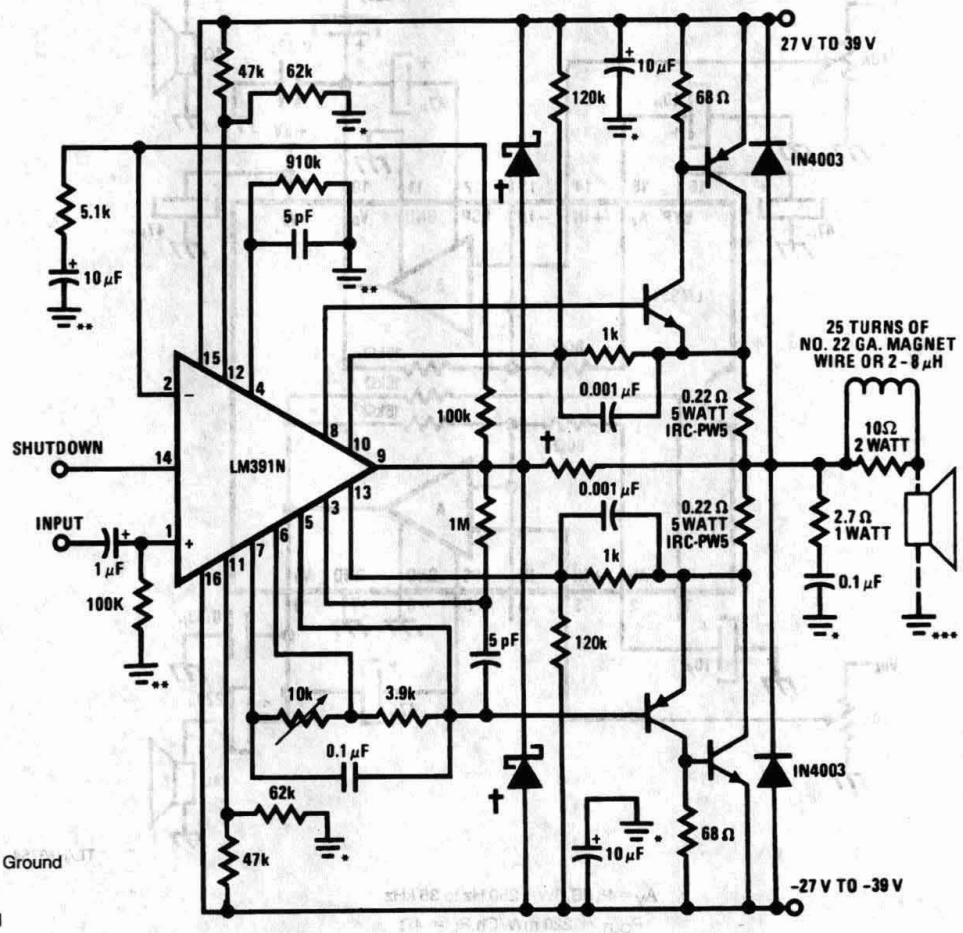
If the output is shorted, the transistor voltage is about 28V and the current is 5A. Therefore the average power is:

$$\text{short } \overline{PD} = \tfrac{1}{2}(28)\,5 = 70W$$

This is much larger than the power used to calculate the heat sinks and the output transistors will overheat if the output is shorted too long.

Typical Applications (Continued)

40W-8Ω, 60W-4Ω Amplifier



TL/H/7146–13

*High Frequency Ground

**Input Ground

***Speaker Ground

Note: All Grounds Should be Tied Together Only at Power Supply Ground.

†Additional protection for LM391N; Schottky diodes and R ≅ 100Ω.

National Semiconductor

LM831 Low Voltage Audio Power Amplifier

General Description

The LM831 is a dual audio power amplifier optimized for very low voltage operation. The LM831 has two independent amplifiers, giving stereo or higher power bridge (BTL) operation from two- or three-cell power supplies.

The LM831 uses a patented compensation technique to reduce high-frequency radiation for optimum performance in AM radio applications. This compensation also results in lower distortion and less wide-band noise.

The input is direct-coupled to the LM831, eliminating the usual coupling capacitor. Voltage gain is adjustable with a single resistor.

Features

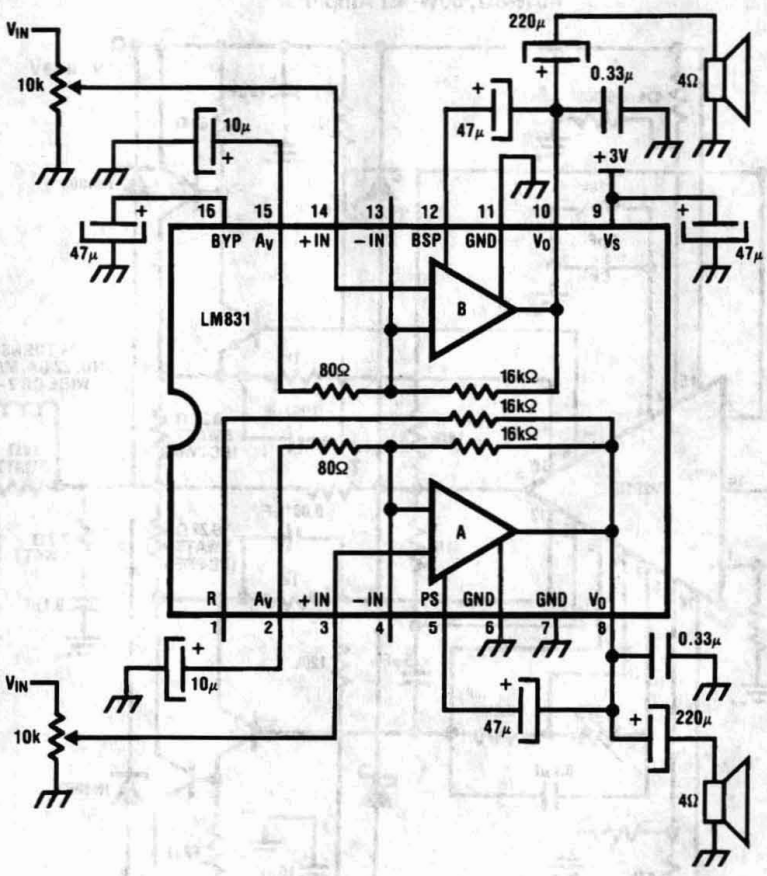
- Low voltage operation, 1.8V to 6.0V
- High power, 440 mW, 8Ω, BTL, 3V
- Low AM radiation
- Low noise
- Low THD

Applications

- Portable tape recorders
- Portable radios
- Headphone stereo
- Portable speakers

Typical Application

Dual Amplifier with Minimum Parts



TL/H/6754–1

A_V = 46 dB, BW = 250 Hz to 35 kHz

P_{OUT} = 220 mW/Ch, R_L = 4Ω

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage, V_S	7.5V
Input Voltage, V_{IN}	±0.4V
Power Dissipation (Note 1), P_D	1.3W (M Package) 1.4W (N Package)
Operating Temperature (Note 1), T_{opr}	−40°C to +85°C
Storage Temperature, T_{stg}	−65°C to +150°C
Junction Temperature, T_j	+150°C
Lead Temp. (Soldering, 10 sec.), T_L	+260°C
Thermal Resistance	
θ_{JC} (DIP)	27°C/W
θ_{JA} (DIP)	75°C/W
θ_{JC} (SO Package)	20°C/W
θ_{JA} (SO Package)	95°C/W

Electrical Characteristics

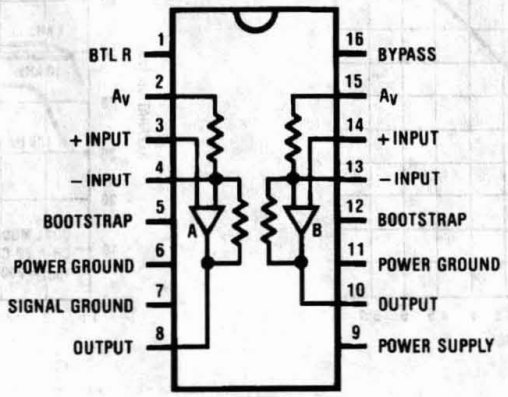
Unless otherwise specified, T_A = 25°C, V_S = 3V, f = 1 kHz, test circuit is dual or BTL amplifier with minimum parts.

Symbol	Parameter	Conditions	Typ	Tested Limit	Unit (Limit)
V_S	Operating Voltage		3 3	1.8 6	V(Min) V(Max)
I_Q	Supply Current	V_{IN} = 0, Dual Mode V_{IN} = 0, BTL Mode	5 6	10 15	mA (Max) mA (Max)
V_{OS}	Output DC Offset	V_{IN} = 0, BTL Mode	10	50	mV (Max)
R_{IN}	Input Resistance		25	15 35	k (Min) k (Max)
A_V	Voltage Gain	V_{IN} = 2.25 mV_{rms}, f = 1 kHz, Dual Mode	46	44 48	dB (Min) dB (Max)
PSRR	Supply Rejection	V_S = 3V + 200 mV_{rms} @ f = 1 kHz	46	30	dB (Min)
P_{OD}	Power Out	V_S = 3V, R_L = 4Ω, 10% THD, Dual Mode	220	150	mW (Min)
P_{ODL}	Power Out Low, V_S	V_S = 1.8V, R_L = 4Ω, 10% THD, Dual Mode	45	10	mW (Min)
P_{OB}	Power Out	V_S = 3V, R_L = 8Ω, 10% THD, BTL Mode	440	300	mW (Min)
P_{OBL}	Power Out Low, V_S	V_S = 1.8V, R_L = 8Ω, 10% THD, BTL Mode	90	20	mW (Min)
Sep	Channel Separation	Referenced to V_O = 200 mV_{rms}	52	40	dB (Min)
I_B	Input Bias Current		1	2	μA (Max)
E_{n0}	Output Noise	Wide Band (250 ~ 35 kHz)	250	500	μV (Max)
THD	Distortion	V_S = 3V, P_O = 50 mW, f = 1 kHz, Dual	0.25	1	% (Max)

Note 1: For operation in ambient temperatures above 25°C, the device must be derated based on a 150°C maximum junction temperature and a thermal resistance of 98°C/W junction to ambient for the M package or 90°C/W junction to ambient for the N package.

Connection Diagram

Dual-In-Line Package



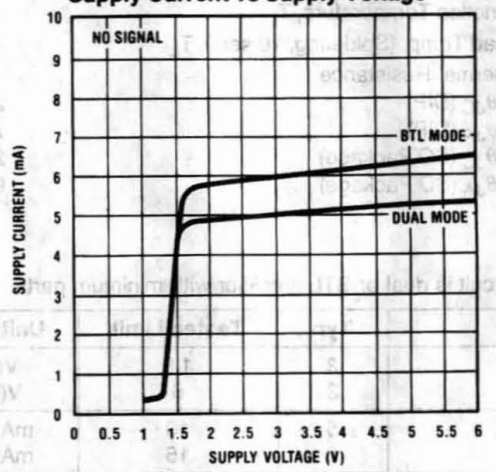
TL/H/6754–2

Top View

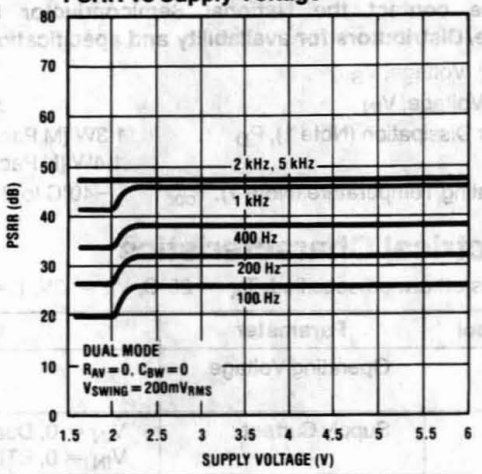
Order Number LM831M or N
See NS Package Number M16B or N16E

Typical Performance Characteristics

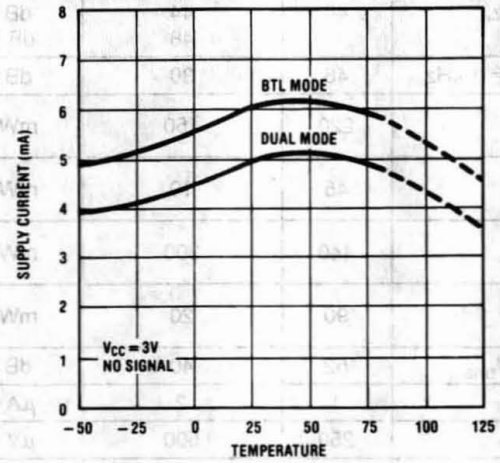
Supply Current vs Supply Voltage



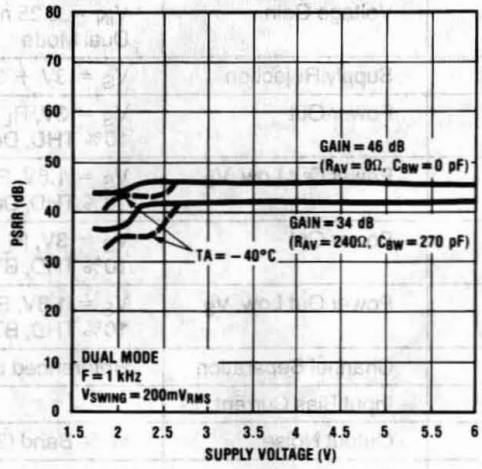
PSRR vs Supply Voltage



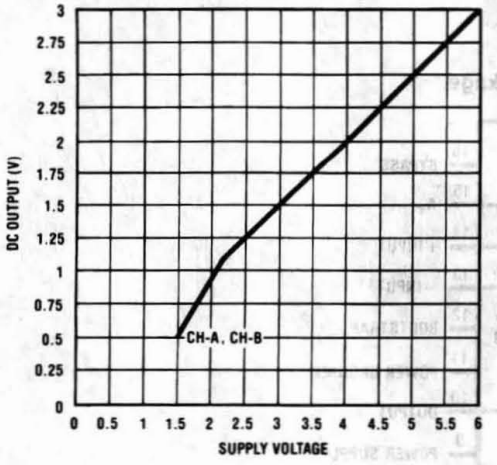
Supply Current vs Temperature



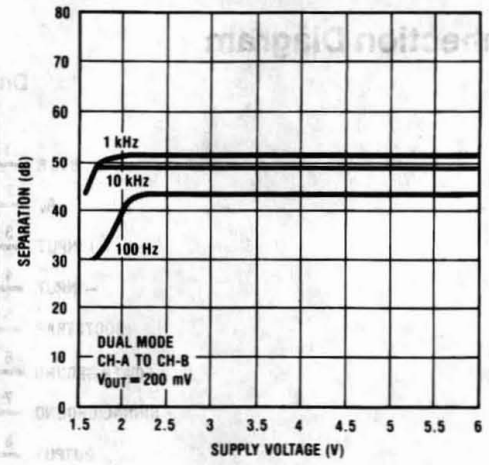
PSRR vs Supply Voltage



DC Output vs Supply Voltage



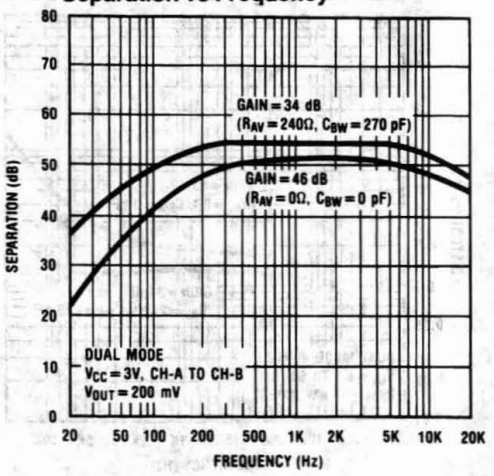
Separation vs Supply Voltage



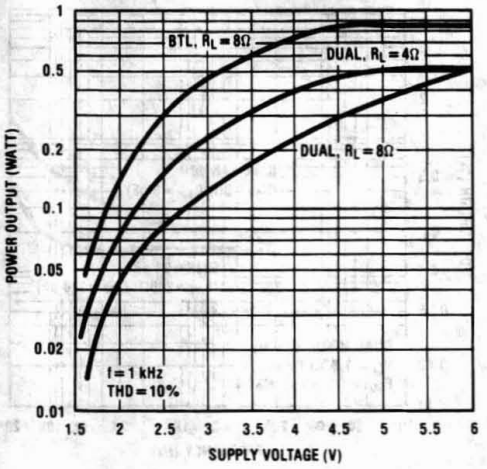
TL/H/6754–4

Typical Performance Characteristics (Continued)

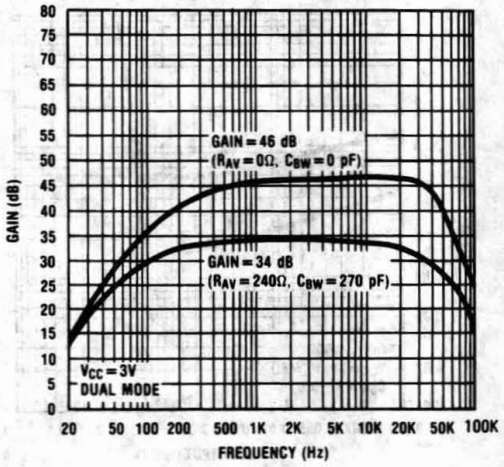
Separation vs Frequency



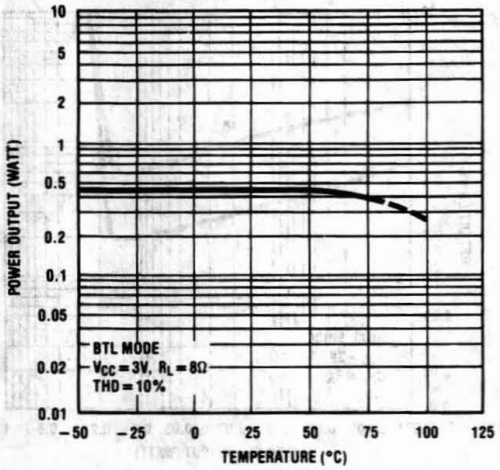
Power Output vs Supply Voltage



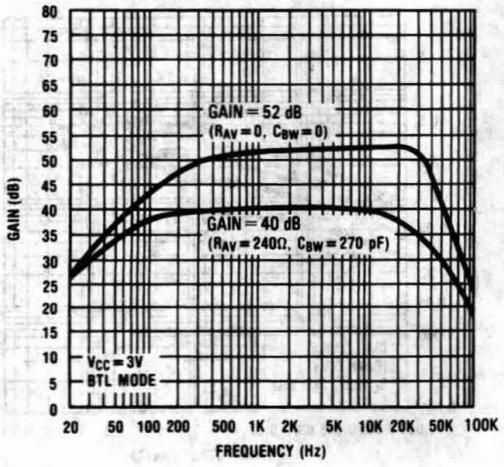
Gain vs Frequency



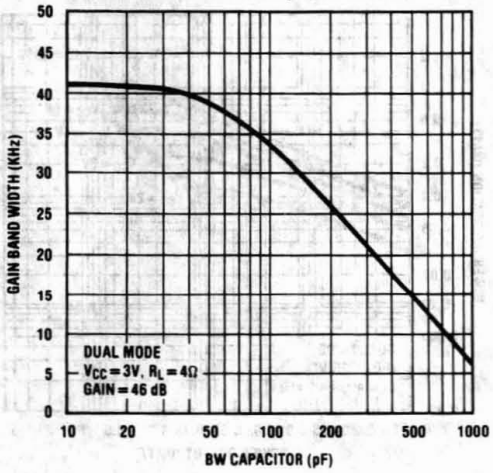
Power Output vs Temperature



Gain vs Frequency



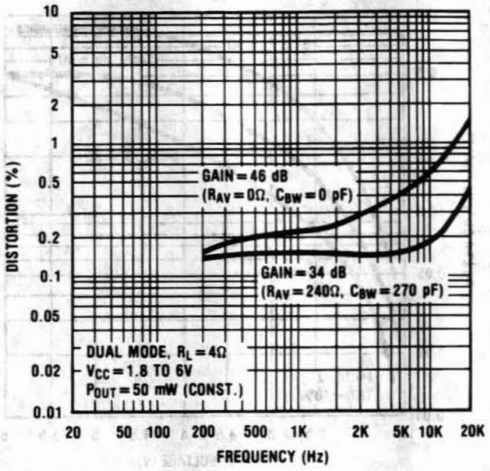
Bandwidth vs BW Capacitance



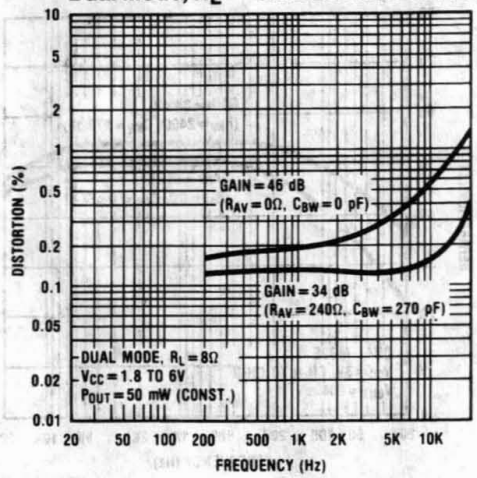
TL/H/6754–5

Typical Performance Characteristics (Continued)

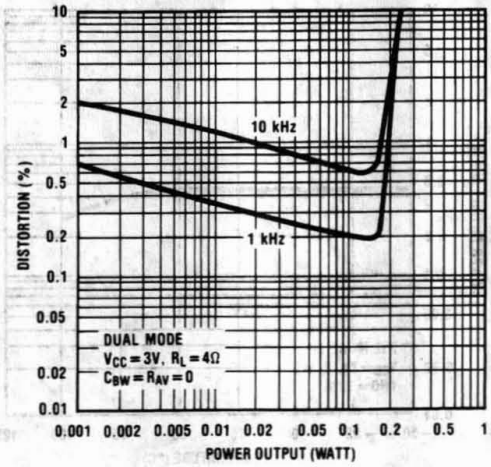
Dual Mode, R_L = 4Ω Distortion vs Frequency



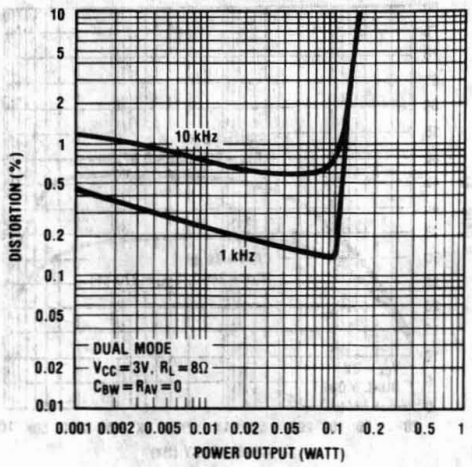
Dual Mode, R_L = 8Ω Distortion vs Frequency



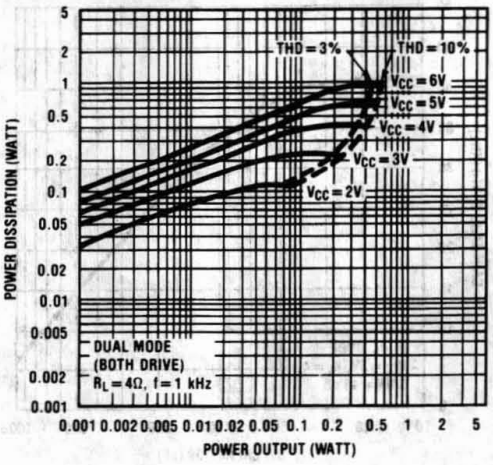
Distortion vs Power Output (Note 2)



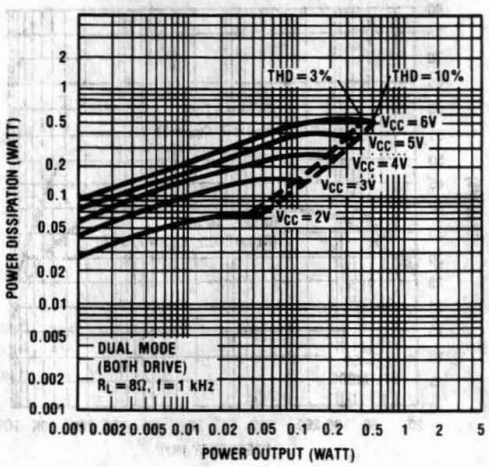
Distortion vs Power Output (Note 2)



Power Dissipation vs Power Output



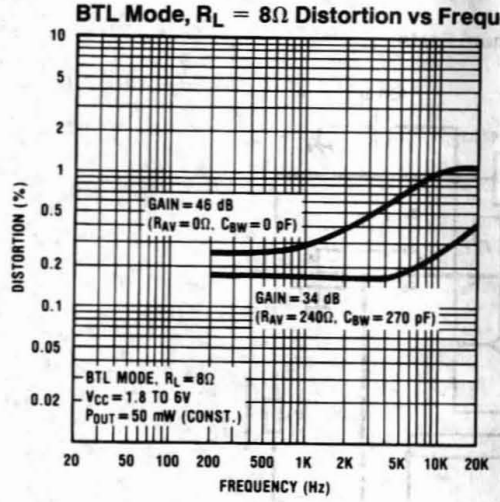
Power Dissipation vs Power Output



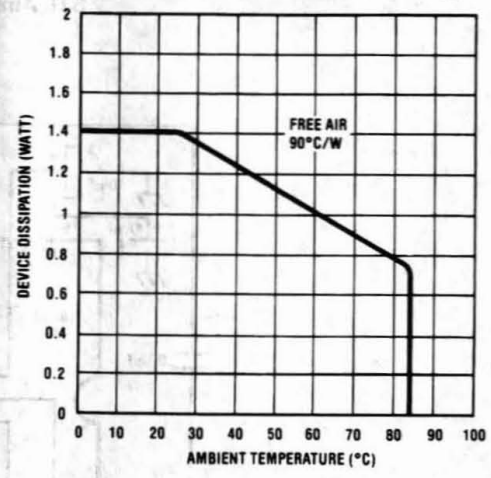
TL/H/6754–6

Typical Performance Characteristics (Continued)

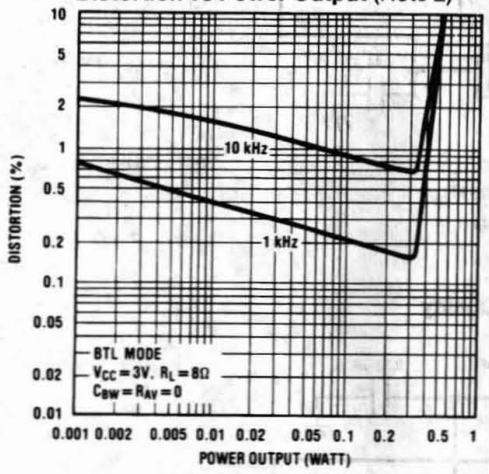
BTL Mode, R_L = 8Ω Distortion vs Frequency



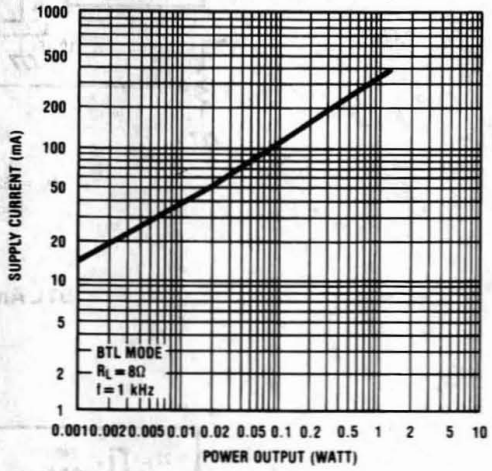
Device Dissipation vs Ambient Temperature



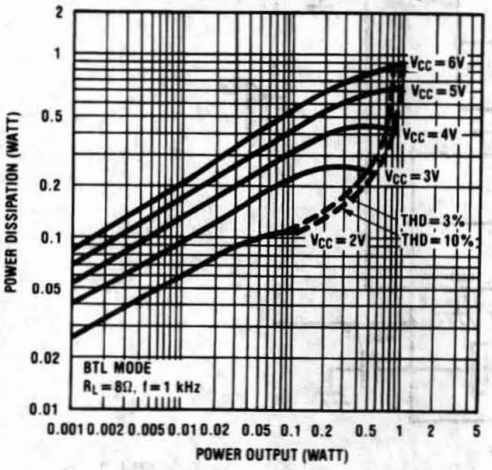
Distortion vs Power Output (Note 2)



Supply Current vs Power Output



Power Dissipation vs Power Output

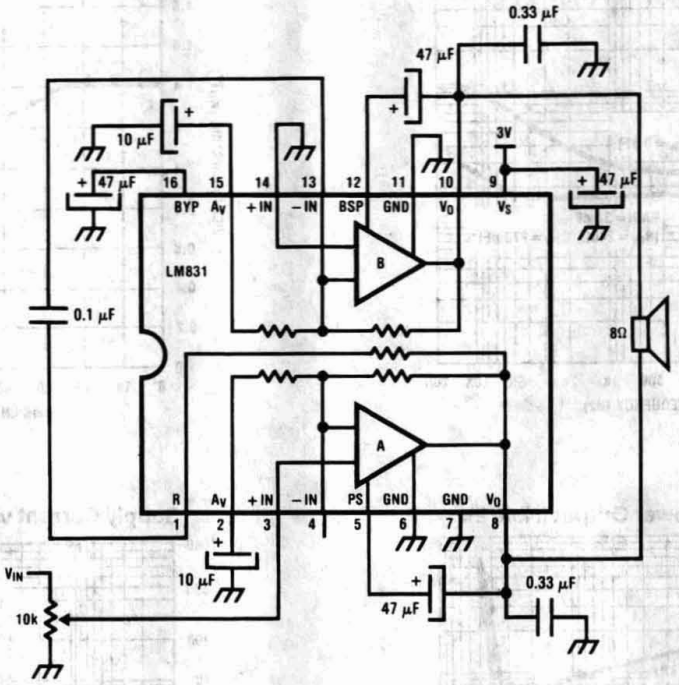


Note 2: 1 kHz curve is measured with 400 Hz–30 kHz Filter.

TL/H/6754–7

Typical Applications

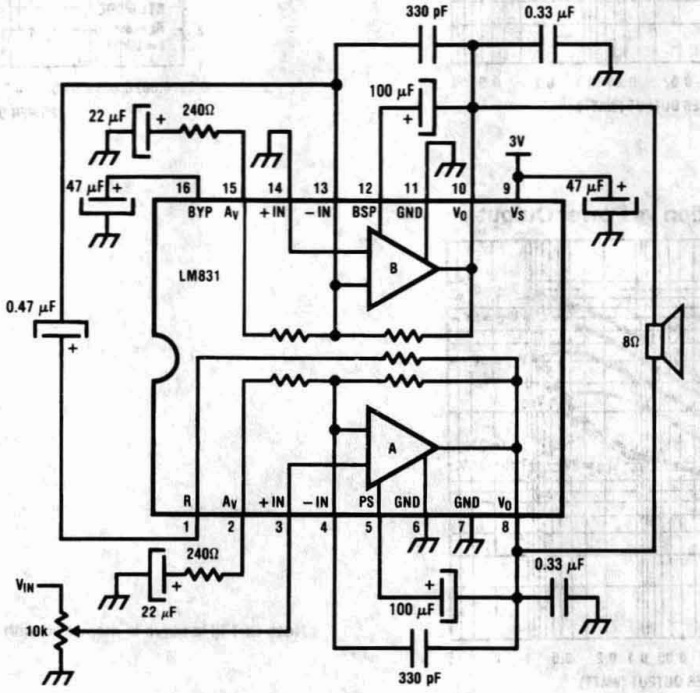
BTL Amplifier with Minimum Parts



TL/H/6754–8

A_V = 52 dB, BW = 250 Hz to 25 kHz
P_{OUT} = 440 mW, R_L = 8Ω

BTL Amplifier for Hi-Fi Quality

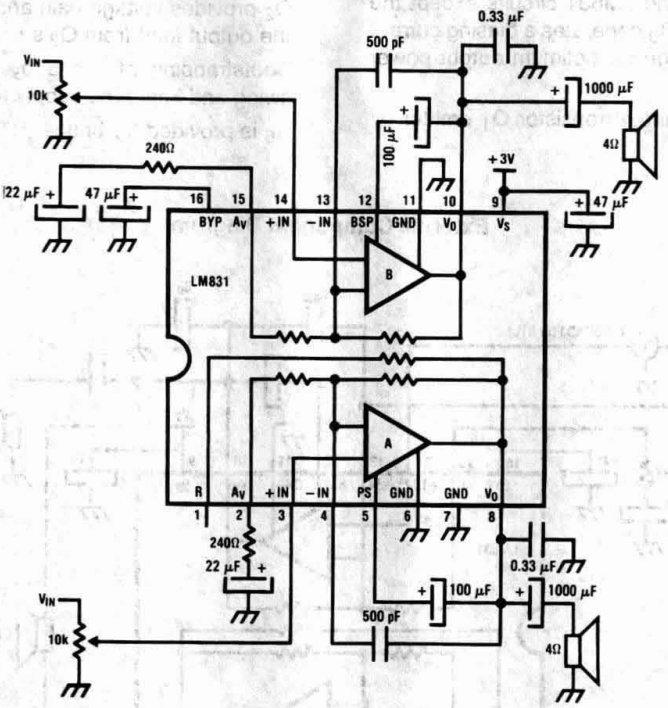


TL/H/6754–9

A_V = 40 dB, BW = 20 Hz to 20 kHz
P_{OUT} = 440 mW, R_L = 8Ω
(Dynamic Range Over 80 dB)

Typical Applications (Continued)

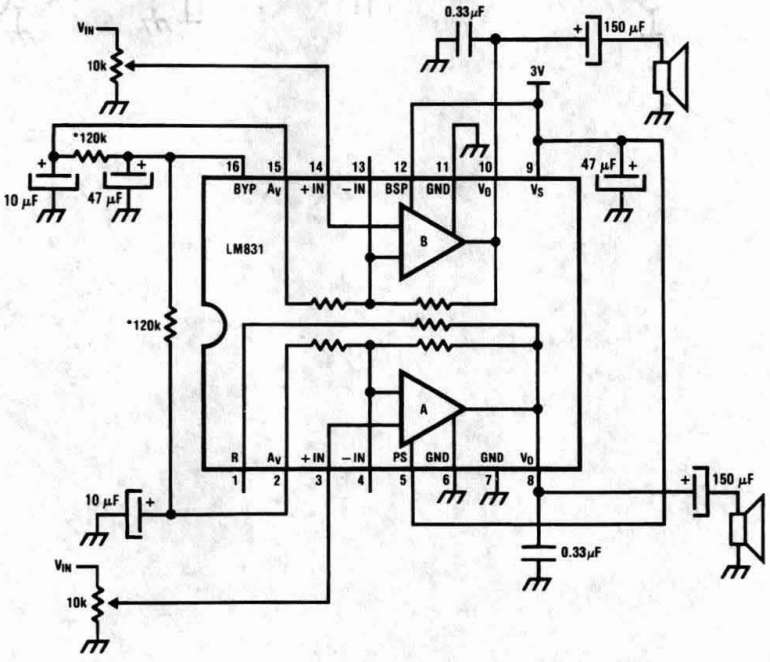
Dual Amplifier for Hi-Fi Quality



TL/H/6754–10

A_V = 34 dB, BW = 50 Hz to 20 kHz
P_{OUT} = 220 mW/Ch, R_L = 4Ω
(Dynamic Range Over 80 dB)

Low-Cost Power Amplifier (No Bootstrap)



TL/H/6754–11

P_{OUT} = 150 mW/Ch, BW = 300 Hz to 35 kHz
BTL Mode is also possible

*For 3-cell applications, the 120k resistor should be changed to 20K.

LM831 Circuit Description Refer to the external component diagram and equivalent schematic.

The power supply is applied to Pin 9 and is filtered by resistor R_1 and capacitor C_{BY} on Pin 16. This filtered voltage at Pin 16 is used to bias all of the LM831 circuits except the power output stage. Resistor R_0 generates a biasing current that sets the output DC voltage for optimum output power for any given supply voltage.

Feedback is provided to the input transistor Q_1 emitter by R_6 and R_7.

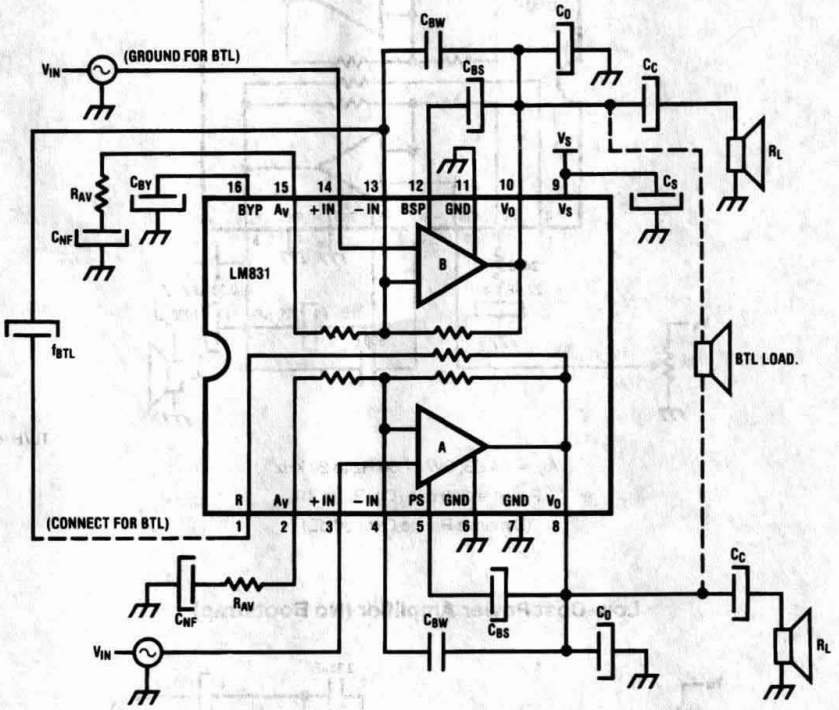
The capacitor C_{NF} on Pin 2 provides unity DC gain for maximum DC accuracy.

Q_2 provides voltage gain and the rest of the devices buffer the output load from Q_2's collector.

Bootstrapping of Pin 5 by C_{BS} allows maximum output swing and improved supply rejection.

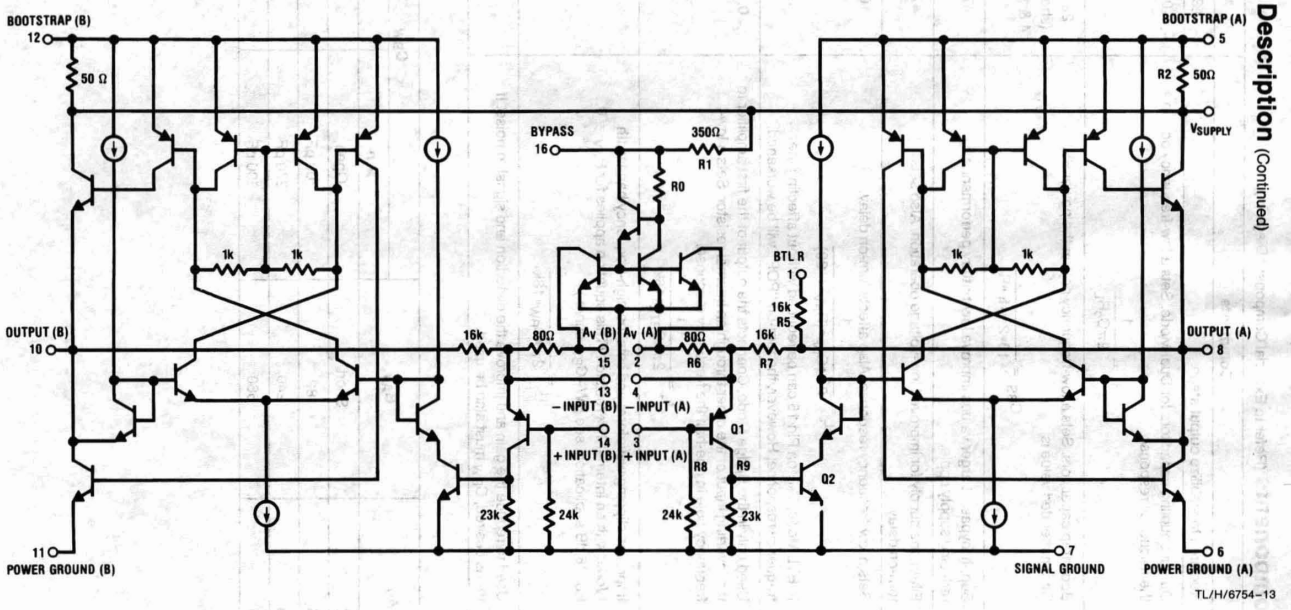
R_5 is provided for bridge (BTL) operation.

External Component Diagram



TL/H/6754–12

LM831 Equivalent Schematic



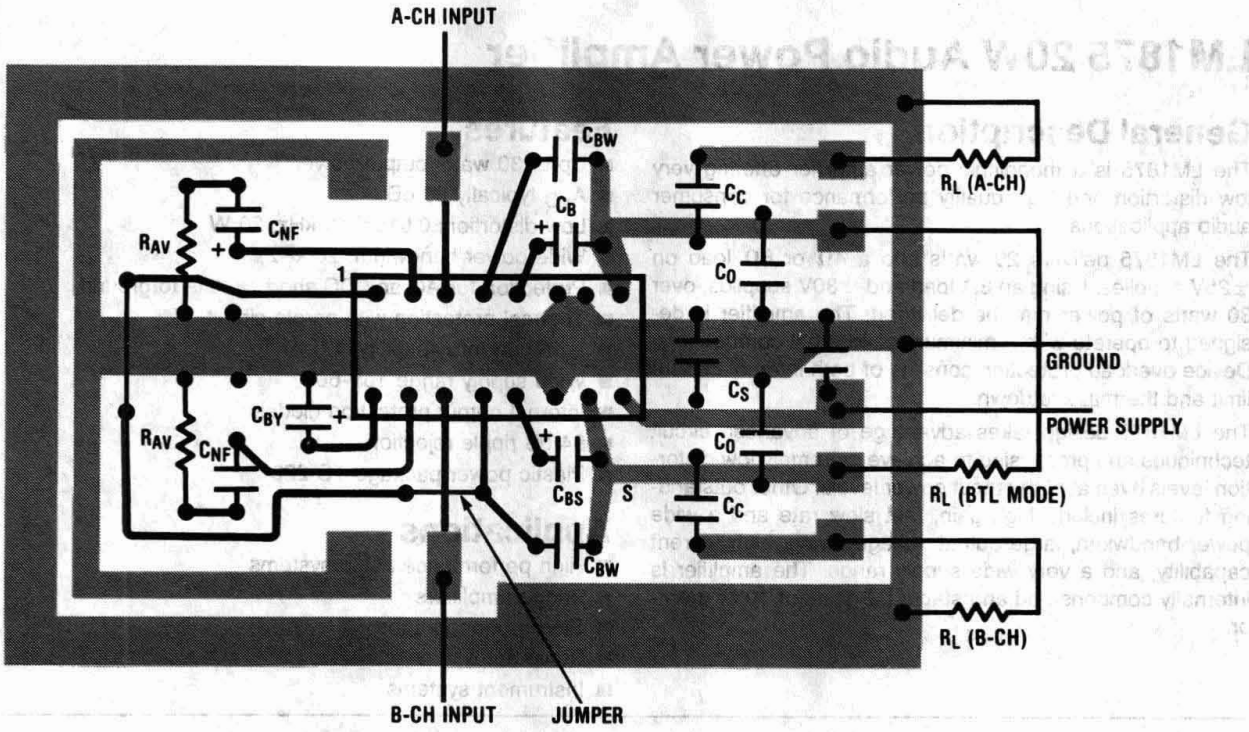
TL/H/6754–13

External Components (Refer to External Component Diagram)

Component	Comments	Min	Max
C_O	Required to stabilize output stage.	0.33 μF	1 μF
C_c	Output coupling capacitors for Dual Mode. Sets a low-frequency pole in the frequency response. $f_L = \frac{1}{2\pi C_c R_L}$	100 μF	10,000 μF
C_{BS}	Bootstrap capacitors. Sets a low-frequency pole in the power BW. Recommended value is $C_{BS} = \frac{1}{10 \bullet 2\pi \bullet f_L \bullet R_L}$	22 μF or (short Pins 4 & 12 to 9)	470 μF
C_S	Supply bypass. Larger values improve low-battery performance by reducing supply ripple.	47 μF	10,000 μF
C_{BY}	Filters the supply for improved low-voltage operation. Also sets turn-on delay.	47 μF	470 μF
C_{NF}	Sets a low-frequency response. Also affects turn-on delay. $f_L = \frac{1}{2\pi \bullet C_{NF} \bullet (R_{AV} + 80)}$ In BTL Mode, C_{NF} on Pin 15 can be reduced without affecting the frequency response. However, the turn-on "POP" will be worsened.	10 μF	100 μF
C_{BTL}	Used only in the Bridge Mode. Connects the output of the first amplifier to the inverting input of the other through an internal resistor. Sets a low-frequency pole in one-half the frequency response. $f_L = \frac{1}{2\pi \bullet C_{BTL} \bullet 16k}$	0.1 μF	1 μF
C_{BW}	Improves clipping waveform and sets the high-frequency bandwidth. Works with an internal 16k resistor. (This equation applies for $R_{AV} \neq 0$. For 46 dB application, see BW–C_{BW} curve.) $f_H = \frac{1}{2\pi \bullet C_{BW} \bullet 16k}$	See table below	
R_{AV}	Used to reduce the gain and improve the distortion and signal to noise. If this is desired, C_{BW} must also be used.	See table below	

Typical A_V	R_{AV}	C_{BW}	
		Min	Max
46 dB	Short	Open	4700 pF
40 dB	82	100 pF	4700 pF
34 dB	240	270 pF	4700 pF
28 dB	560	500 pF	4700 pF

Printed Circuit Layout for LM831N (Foil Side View) Refer to External Component Diagram



TL/H/6754–14

Note: Power ground pattern should be as wide as possible. Supply bypass capacitor should be as close to the IC as possible. Output compensation capacitors should also be close to the IC.

National Semiconductor

LM1875 20W Audio Power Amplifier

General Description

The LM1875 is a monolithic power amplifier offering very low distortion and high quality performance for consumer audio applications.

The LM1875 delivers 20 watts into a 4Ω or 8Ω load on ±25V supplies. Using an 8Ω load and ±30V supplies, over 30 watts of power may be delivered. The amplifier is designed to operate with a minimum of external components. Device overload protection consists of both internal current limit and thermal shutdown.

The LM1875 design takes advantage of advanced circuit techniques and processing to achieve extremely low distortion levels even at high output power levels. Other outstanding features include high gain, fast slew rate and a wide power bandwidth, large output voltage swing, high current capability, and a very wide supply range. The amplifier is internally compensated and stable for gains of 10 or greater.

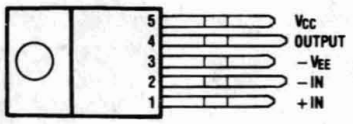
Features

- Up to 30 watts output power
- A_{VO} typically 90 dB
- Low distortion: 0.015%, 1 kHz, 20 W
- Wide power bandwidth: 70 kHz
- Protection for AC and DC short circuits to ground
- Thermal protection with parole circuit
- High current capability: 4A
- Wide supply range 16V-60V
- Internal output protection diodes
- 94 dB ripple rejection
- Plastic power package TO-220

Applications

- High performance audio systems
- Bridge amplifiers
- Stereo phonographs
- Servo amplifiers
- Instrument systems

Connection Diagram

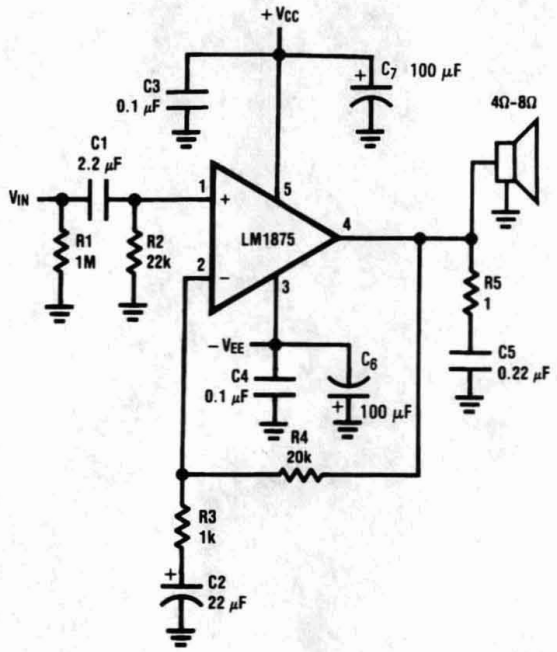


TL/H/5030–1

Front View

Order Number LM1875T
See NS Package Number T05B

Typical Applications



TL/H/5030–2

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	60V
Input Voltage	$-V_{EE}$ to V_{CC}
Storage Temperature	−65°C to + 150°C
Junction Temperature	150°C
Lead Temperature (Soldering, 10 seconds)	260°C
θ_{JC}	3°C
θ_{JA}	73°C

Electrical Characteristics

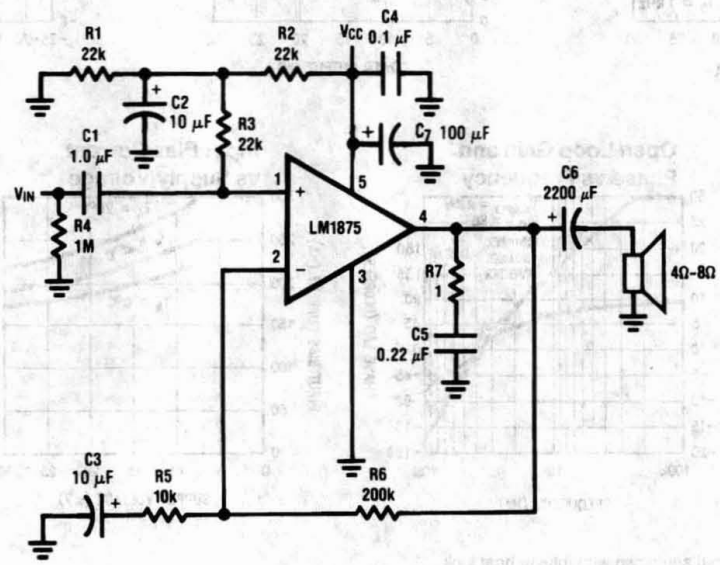
$V_{CC} = +25V$, $-V_{EE} = -25V$, $T_{AMBIENT} = 25°C$, $R_L = 8\Omega$, $A_V = 20$ (26 dB), $f_o = 1$ kHz, unless otherwise specified.

Parameter	Conditions	Typical	Tested Limits	Units
Supply Current	$P_{OUT} = 0W$	70	100	mA
Output Power (Note 1)	THD = 1%	25		W
THD (Note 1)	$P_{OUT} = 20W$, $f_o = 1$ kHz	0.015		%
	$P_{OUT} = 20W$, $f_o = 20$ kHz	0.05	0.4	%
	$P_{OUT} = 20W$, $R_L = 4\Omega$, $f_o = 1$ kHz	0.022		%
	$P_{OUT} = 20W$, $R_L = 4\Omega$, $f_o = 20$ kHz	0.07	0.6	%
Offset Voltage		±1	±15	mV
Input Bias Current		±0.2	±2	μA
Input Offset Current		0	±0.5	μA
Gain-Bandwidth Product	$f_o = 20$ kHz	5.5		MHz
Open Loop Gain	DC	90		dB
PSRR	V_{CC}, 1 kHz, 1 Vrms	95	52	dB
	V_{EE}, 1 kHz, 1 Vrms	83	52	dB
Max Slew Rate	20W, 8Ω, 70 kHz BW	8		V/μs
Current Limit	$V_{OUT} = V_{SUPPLY} - 10V$	4	3	A
Equivalent Input Noise Voltage	$R_S = 600\Omega$, CCIR	3		μVrms

Note 1: Assumes the use of a heat sink having a thermal resistance of 1°C/W and no insulator with an ambient temperature of 25°C. Because the output limiting circuitry has a negative temperature coefficient, the maximum output power delivered to a 4Ω load may be slightly reduced when the tab temperature exceeds 55°C.

Typical Applications (Continued)

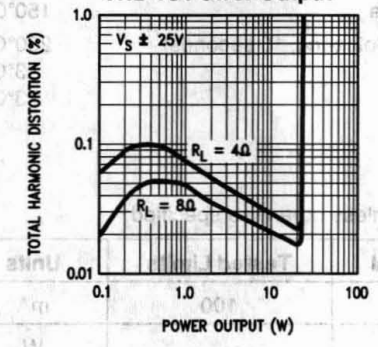
Typical Single Supply Operation



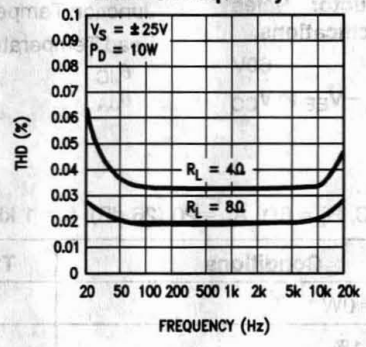
TL/H/5030–3

Typical Performance Characteristics

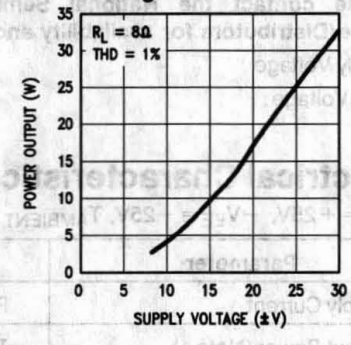
THD vs Power Output



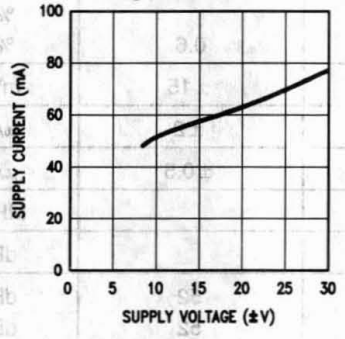
THD vs Frequency



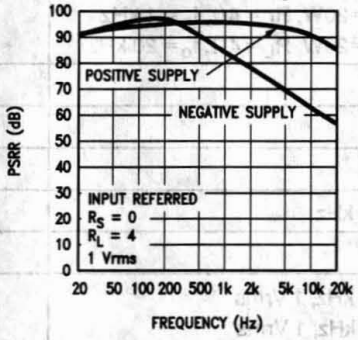
Power Output vs Supply Voltage



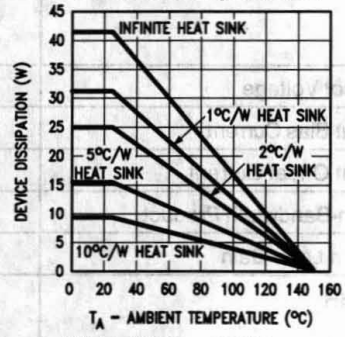
Supply Current vs Supply Voltage



PSRR vs Frequency

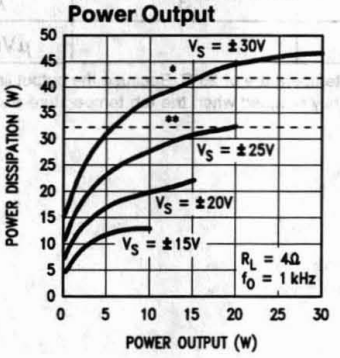


Device Dissipation vs Ambient Temperature†

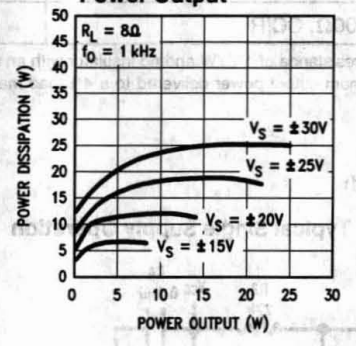


†ϕINTERFACE = 1°C/W.
See Application Hints.

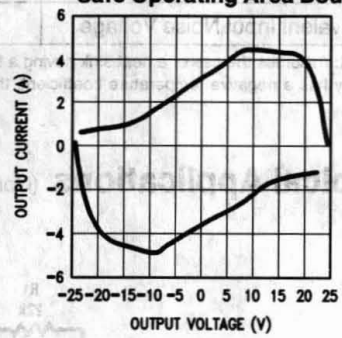
Power Dissipation vs Power Output



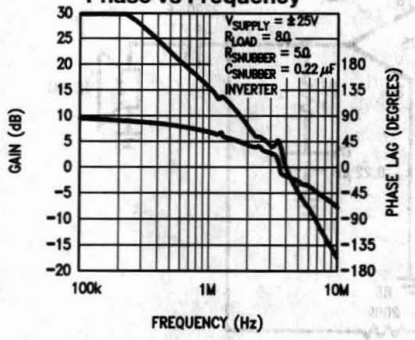
Power Dissipation vs Power Output



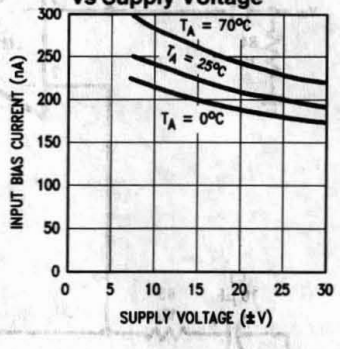
I_{OUT} vs V_{OUT}-Current Limit/ Safe Operating Area Boundary



Open Loop Gain and Phase vs Frequency



Input Bias Current vs Supply Voltage

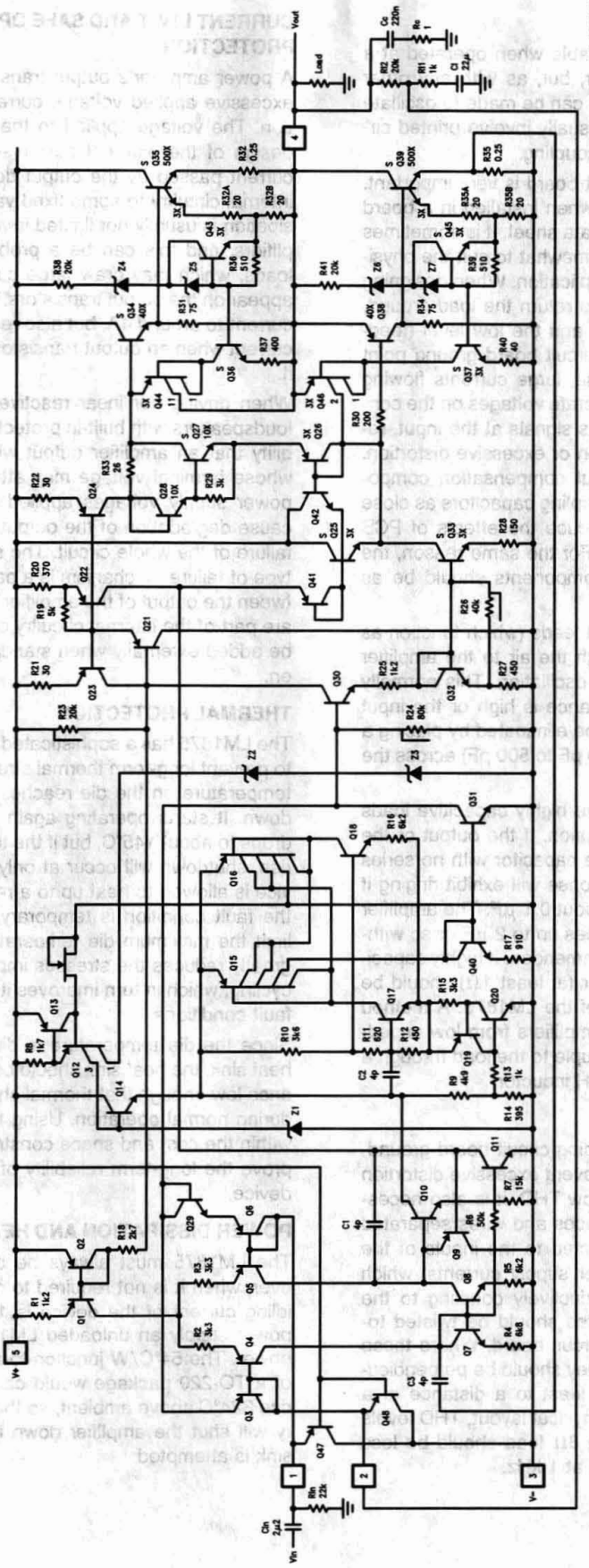


TL/H/5030–4

*Thermal shutdown with infinite heat sink

**Thermal shutdown with 1°C/W heat sink

Schematic Diagram



TL/H/5030–5

Application Hints

STABILITY

The LM1875 is designed to be stable when operated at a closed-loop gain of 10 or greater, but, as with any other high-current amplifier, the LM1875 can be made to oscillate under certain conditions. These usually involve printed circuit board layout or output/input coupling.

Proper layout of the printed circuit board is very important. While the LM1875 will be stable when installed in a board similar to the ones shown in this data sheet, it is sometimes necessary to modify the layout somewhat to suit the physical requirements of a particular application. When designing a different layout, it is important to return the load ground, the output compensation ground, and the low level (feedback and input) grounds to the circuit board ground point through separate paths. Otherwise, large currents flowing along a ground conductor will generate voltages on the conductor which can effectively act as signals at the input, resulting in high frequency oscillation or excessive distortion. It is advisable to keep the output compensation components and the 0.1 μF supply decoupling capacitors as close as possible to the LM1875 to reduce the effects of PCB trace resistance and inductance. For the same reason, the ground return paths for these components should be as short as possible.

Occasionally, current in the output leads (which function as antennas) can be coupled through the air to the amplifier input, resulting in high-frequency oscillation. This normally happens when the source impedance is high or the input leads are long. The problem can be eliminated by placing a small capacitor (on the order of 50 pF to 500 pF) across the circuit input.

Most power amplifiers do not drive highly capacitive loads well, and the LM1875 is no exception. If the output of the LM1875 is connected directly to a capacitor with no series resistance, the square wave response will exhibit ringing if the capacitance is greater than about 0.1 μF. The amplifier can typically drive load capacitances up to 2 μF or so without oscillating, but this is not recommended. If highly capacitive loads are expected, a resistor (at least 1Ω) should be placed in series with the output of the LM1875. A method commonly employed to protect amplifiers from low impedances at high frequencies is to couple to the load through a 10Ω resistor in parallel with a 5 μH inductor.

DISTORTION

The preceding suggestions regarding circuit board grounding techniques will also help to prevent excessive distortion levels in audio applications. For low THD, it is also necessary to keep the power supply traces and wires separated from the traces and wires connected to the inputs of the LM1875. This prevents the power supply currents, which are large and nonlinear, from inductively coupling to the LM1875 inputs. Power supply wires should be twisted together and separated from the circuit board. Where these wires are soldered to the board, they should be perpendicular to the plane of the board at least to a distance of a couple of inches. With a proper physical layout, THD levels at 20 kHz with 10W output to an 8Ω load should be less than 0.05%, and less than 0.02% at 1 kHz.

CURRENT LIMIT AND SAFE OPERATING AREA (SOA) PROTECTION

A power amplifier's output transistors can be damaged by excessive applied voltage, current flow, or power dissipation. The voltage applied to the amplifier is limited by the design of the external power supply, while the maximum current passed by the output devices is usually limited by internal circuitry to some fixed value. Short-term power dissipation is usually not limited in monolithic audio power amplifiers, and this can be a problem when driving reactive loads, which may draw large currents while high voltages appear on the output transistors. The LM1875 not only limits current to around 4A, but also reduces the value of the limit current when an output transistor has a high voltage across it.

When driving nonlinear reactive loads such as motors or loudspeakers with built-in protection relays, there is a possibility that an amplifier output will be connected to a load whose terminal voltage may attempt to swing beyond the power supply voltages applied to the amplifier. This can cause degradation of the output transistors or catastrophic failure of the whole circuit. The standard protection for this type of failure mechanism is a pair of diodes connected between the output of the amplifier and the supply rails. These are part of the internal circuitry of the LM1875, and needn't be added externally when standard reactive loads are driven.

THERMAL PROTECTION

The LM1875 has a sophisticated thermal protection scheme to prevent long-term thermal stress to the device. When the temperature on the die reaches 170°C, the LM1875 shuts down. It starts operating again when the die temperature drops to about 145°C, but if the temperature again begins to rise, shutdown will occur at only 150°C. Therefore, the device is allowed to heat up to a relatively high temperature if the fault condition is temporary, but a sustained fault will limit the maximum die temperature to a lower value. This greatly reduces the stresses imposed on the IC by thermal cycling, which in turn improves its reliability under sustained fault conditions.

Since the die temperature is directly dependent upon the heat sink, the heat sink should be chosen for thermal resistance low enough that thermal shutdown will not be reached during normal operation. Using the best heat sink possible within the cost and space constraints of the system will improve the long-term reliability of any power semiconductor device.

POWER DISSIPATION AND HEAT SINKING

The LM1875 must always be operated with a heat sink, even when it is not required to drive a load. The maximum idling current of the device is 100 mA, so that on a 60V power supply an unloaded LM1875 must dissipate 6W of power. The 54°C/W junction-to-ambient thermal resistance of a TO-220 package would cause the die temperature to rise 324°C above ambient, so the thermal protection circuitry will shut the amplifier down if operation without a heat sink is attempted.

Application Hints (Continued)

In order to determine the appropriate heat sink for a given application, the power dissipation of the LM1875 in that application must be known. When the load is resistive, the maximum average power that the IC will be required to dissipate is approximately:

$$P_{D(MAX)} \approx \frac{V_S^2}{2\pi^2 R_L} + P_Q$$

where V_S is the total power supply voltage across the LM1875, R_L is the load resistance, and P_Q is the quiescent power dissipation of the amplifier. The above equation is only an approximation which assumes an "ideal" class B output stage and constant power dissipation in all other parts of the circuit. The curves of "Power Dissipation vs Power Output" give a better representation of the behavior of the LM1875 with various power supply voltages and resistive loads. As an example, if the LM1875 is operated on a 50V power supply with a resistive load of 8Ω, it can develop up to 19W of internal power dissipation. If the die temperature is to remain below 150°C for ambient temperatures up to 70°C, the total junction-to-ambient thermal resistance must be less than

$$\frac{150°C - 70°C}{19W} = 4.2°C/W.$$

Using $\theta_{JC} = 2°C/W$, the sum of the case-to-heat-sink interface thermal resistance and the heat-sink-to-ambient thermal resistance must be less than 2.2°C/W. The case-to-heat-sink thermal resistance of the TO-220 package varies with the mounting method used. A metal-to-metal interface will be about 1°C/W if lubricated, and about 1.2°C/W if dry.

If a mica insulator is used, the thermal resistance will be about 1.6°C/W lubricated and 3.4°C/W dry. For this example, we assume a lubricated mica insulator between the LM1875 and the heat sink. The heat sink thermal resistance must then be less than

4.2°C/W − 2°C/W − 1.6°C/W = 0.6°C/W.

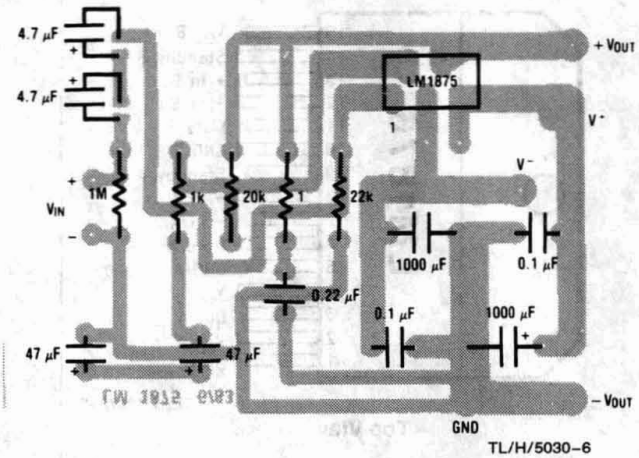
This is a rather large heat sink and may not be practical in some applications. If a smaller heat sink is required for reasons of size or cost, there are two alternatives. The maximum ambient operating temperature can be reduced to 50°C (122°F), resulting in a 1.6°C/W heat sink, or the heat sink can be isolated from the chassis so the mica washer is not needed. This will change the required heat sink to a 1.2°C/W unit if the case-to-heat-sink interface is lubricated.

Note: When using a single supply, maximum transfer of heat away from the LM1875 can be achieved by mounting the device directly to the heat sink (tab is at ground potential); this avoids the use of a mica or other type insulator.

The thermal requirements can become more difficult when an amplifier is driving a reactive load. For a given magnitude of load impedance, a higher degree of reactance will cause a higher level of power dissipation within the amplifier. As a general rule, the power dissipation of an amplifier driving a 60° reactive load (usually considered to be a worst-case loudspeaker load) will be roughly that of the same amplifier driving the resistive part of that load. For example, a loudspeaker may at some frequency have an impedance with a magnitude of 8Ω and a phase angle of 60°. The real part of this load will then be 4Ω, and the amplifier power dissipation will roughly follow the curve of power dissipation with a 4Ω load.

Component Layouts

Split Supply



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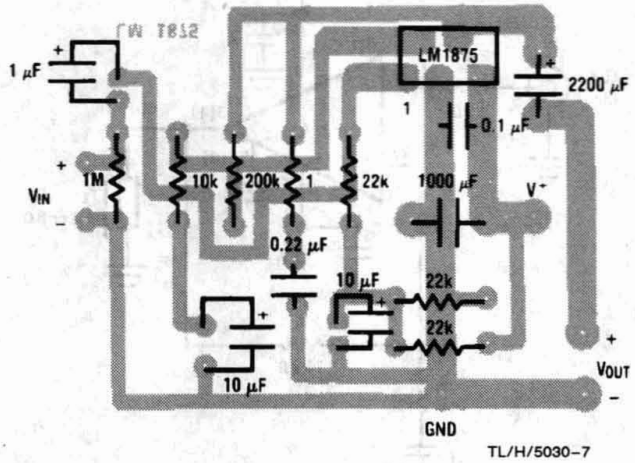
Single Supply



TL/H/5030–7

National Semiconductor

PRELIMINARY

LM1876 *Overture*™ Audio Power Amplifier Series
Dual 20W Audio Power Amplifier with Mute and Standby Modes

General Description

The LM1876 is a stereo audio amplifier capable of delivering typically 20W per channel of continuous average output power into a 4Ω or 8Ω load with less than 0.1% (THD + N).

Each amplifier has an independent smooth transition fade-in/out mute and a power conserving standby mode which can be controlled by external logic.

The performance of the LM1876, utilizing its Self Peak Instantaneous Temperature (°Ke) **(SPiKe™)** Protection Circuitry, places it in a class above discrete and hybrid amplifiers by providing an inherently, dynamically protected Safe Operating Area (SOA). **SPiKe** Protection means that these parts are safeguarded at the output against overvoltage, undervoltage, overloads, including thermal runaway and instantaneous temperature peaks.

Key Specifications

- THD+N at 1 kHz at 2 x 15W continuous average output power into 4Ω or 8Ω — 0.1% (max)
- THD+N at 1 kHz at continuous average output power of 2 x 20W into 8Ω — 0.009% (typ)
- Standby current — 4.2 mA (typ)

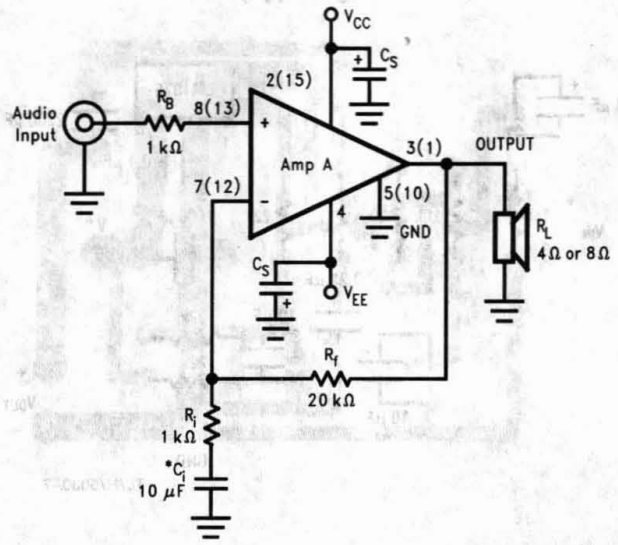
Features

- SPiKe Protection
- Minimal amount of external components necessary
- Quiet fade-in/out mute mode
- Standby-mode
- Isolated 15-lead TO-220 package

Applications

- High-end stereo TVs
- Component stereo
- Compact stereo

Typical Application



TL/H/12072–1

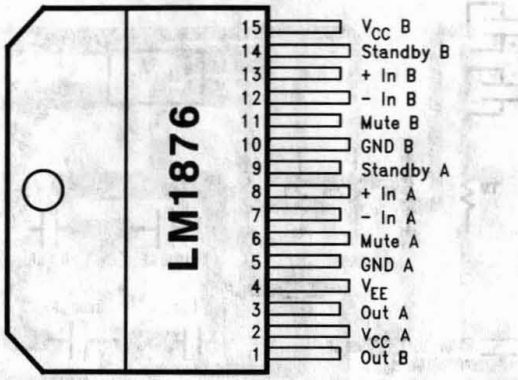
FIGURE 1. Typical Audio Amplifier Application Circuit

Note: Numbers in parentheses represent pinout for amplifier B.

*Optional component dependent upon specific design requirements.

Connection Diagram

Isolated Plastic Package



TL/H/12072–2

Top View

Order Number LM1876TF
See NS Package Number TF15B

National Semiconductor

LM1877 Dual Audio Power Amplifier

General Description

The LM1877 is a monolithic dual power amplifier designed to deliver 2W/channel continuous into 8Ω loads. The LM1877 is designed to operate with a low number of external components, and still provide flexibility for use in stereo phonographs, tape recorders and AM-FM stereo receivers, etc. Each power amplifier is biased from a common internal regulator to provide high power supply rejection, and output Q point centering. The LM1877 is internally compensated for all gains greater than 10.

Features

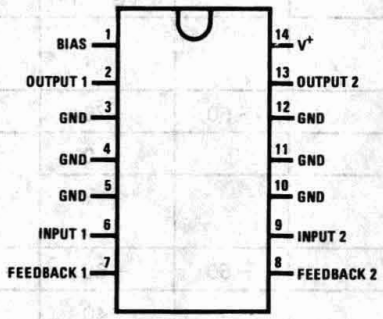
- 2W/channel
- −65 dB ripple rejection, output referred
- −65 dB channel separation, output referred
- Wide supply range, 6V–24V
- Very low cross-over distortion
- Low audio band noise
- AC short circuit protected
- Internal thermal shutdown

Applications

- Multi-channel audio systems
- Stereo phonographs
- Tape recorders and players
- AM-FM radio receivers
- Servo amplifiers
- Intercom systems
- Automotive products

Connection Diagram

Dual-In-Line Package
or Surface Mount Package

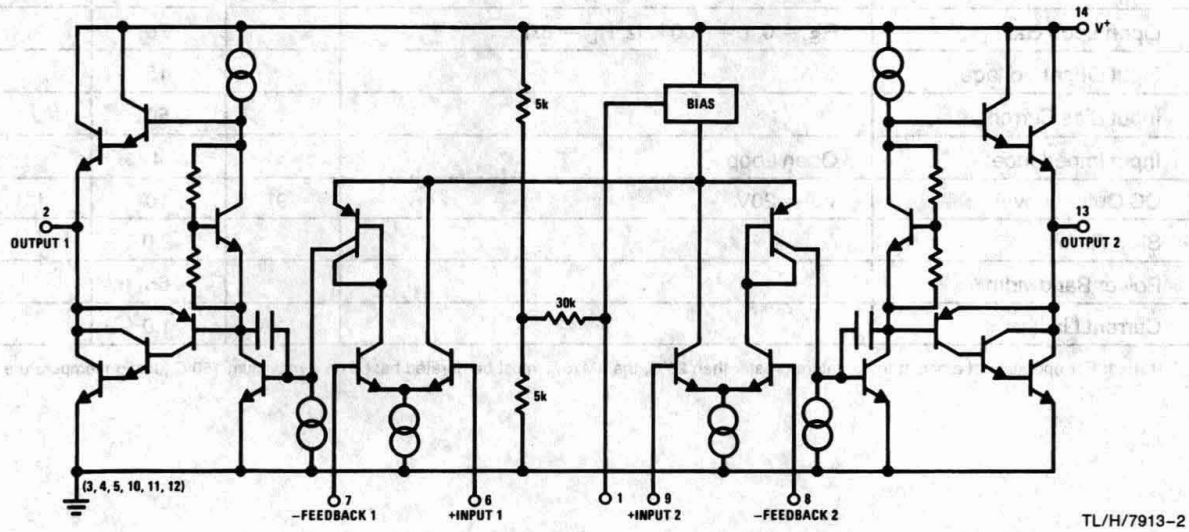


TL/H/7913–1

Top View

Order Number LM1877M-9 or LM1877N-9
See NS Package Number M14B or N14A

Equivalent Schematic Diagram



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Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	26V
Input Voltage	±0.7V
Operating Temperature	0°C to +70°C
Storage Temperature	−65°C to +150°C
Junction Temperature	150°C

Lead Temperature

N-Package Soldering (10 sec.)	260°C
M-Package Infared (15 sec.)	220°C
M-Package Vapor Phase (60 sec.)	215°C

Thermal Resistance

θ_{JC} (N-Package)	30°C/W
θ_{JA} (N-Package)	79°C/W
θ_{JC} (M-Package)	27°C/W
θ_{JA} (M-Package)	114°C/W

Electrical Characteristics

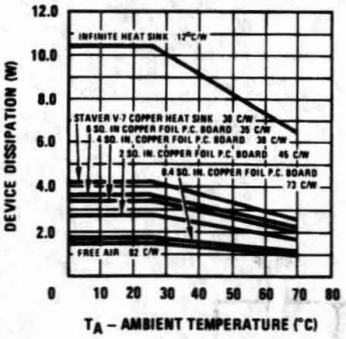
V_S = 20V, T_A = 25°C, (See Note 1) R_L = 8Ω, A_V = 50 (34 dB) unless otherwise specified

Parameter	Conditions	Min	Typ	Max	Units
Total Supply Current	P_O = 0W		25	50	mA
Output Power LM1877	THD = 10% V_S = 20V, R_L = 8Ω V_S = 12V, R_L = 8Ω	2.0	 1.3		 W/Ch W/Ch
Total Harmonic Distortion LM1877	f = 1 kHz, V_S = 14V				
	P_O = 50 mW/Channel		0.075		%
	P_O = 500 mW/Channel		0.045		%
	P_O = 1 W/Channel		0.055		%
Output Swing	R_L = 8Ω		V_S −6		Vp-p
Channel Separation	C_F = 50 µF, C_{IN} = 0.1 µF, f = 1 kHz, Output Referred				
	V_S = 20V, V_O = 4 Vrms	−50	−70		dB
	V_S = 7V, V_O = 0.5 Vrms		−60		dB
PSRR Power Supply Rejection Ratio	C_F = 50 µF, C_{IN} = 0.1 µF, f = 120 Hz, Output Referred				
	V_S = 20V, V_{RIPPLE} = 1 Vrms	−50	−65		dB
	V_S = 7V, V_{RIPPLE} = 0.5 Vrms		−40		dB
Noise	Equivalent Input Noise				
	R_S = 0, C_{IN} = 0.1 µF, BW = 20 Hz–20 kHz, Output Noise Wideband		2.5		µV
	R_S = 0, C_N = 0.1 µF, A_V 200		0.80		mV
Open Loop Gain	R_S = 0, f = 100 kHz, R_L = 8Ω		70		dB
Input Offset Voltage			15		mV
Input Bias Current			50		nA
Input Impedance	Open Loop		4		MΩ
DC Output Level	V_S = 20V	9	10	11	V
Slew Rate			2.0		V/µs
Power Bandwidth			65		kHz
Current Limit			1.0		A

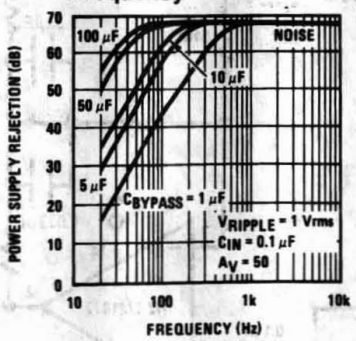
Note 1: For operation at ambient temperature greater than 25°C, the LM1877 must be derated based on a maximum 150°C junction temperature.

Typical Performance Characteristics

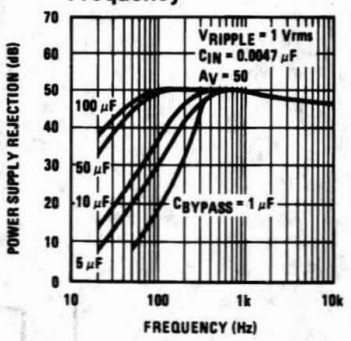
Device Dissipation vs Ambient Temperature


DEVICE DISSIPATION (W)
INFINITE HEAT SINK 12°C/W
STAVER V-7 COPPER HEAT SINK 38 C/W
6 SQ. IN COPPER FOIL P.C. BOARD 35 C/W
4 SQ. IN. COPPER FOIL P.C. BOARD 38 C/W
2 SQ. IN. COPPER FOIL P.C. BOARD 45 C/W
0.4 SQ. IN. COPPER FOIL P.C. BOARD 73 C/W
FREE AIR 92 C/W
T_A – AMBIENT TEMPERATURE (°C)

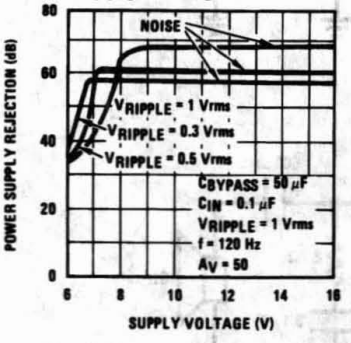
Power Supply Rejection Ratio (Referred to the Output) vs Frequency



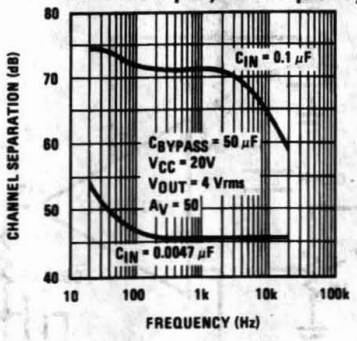
Power Supply Rejection Ratio (Referred to the Output) vs Frequency



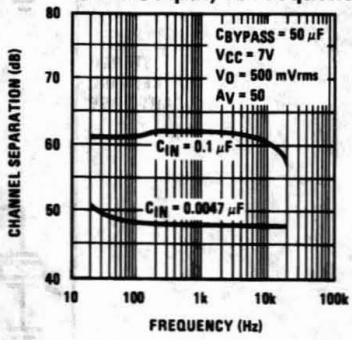
Power Supply Rejection Ratio (Referred to the Output) vs Supply Voltage



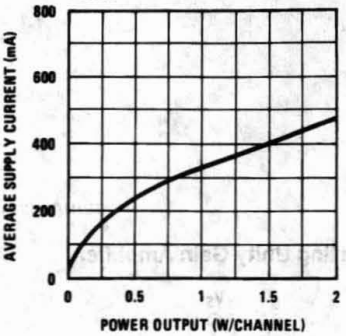
Channel Separation (Referred to the Output) vs Frequency



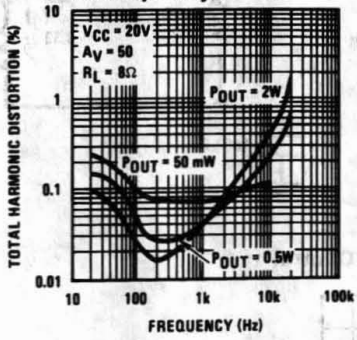
Channel Separation (Referred to the Output) vs Frequency



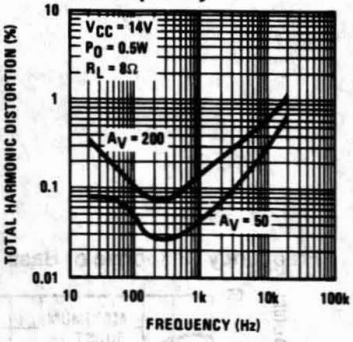
Average Supply Current vs P_{OUT}



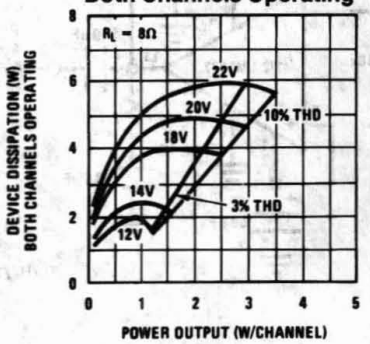
Total Harmonic Distortion vs Frequency



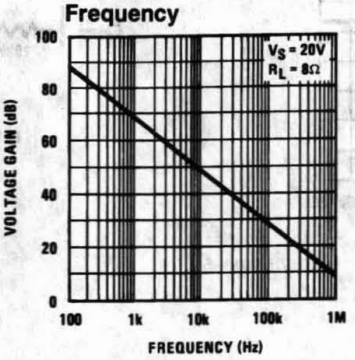
Total Harmonic Distortion vs Frequency



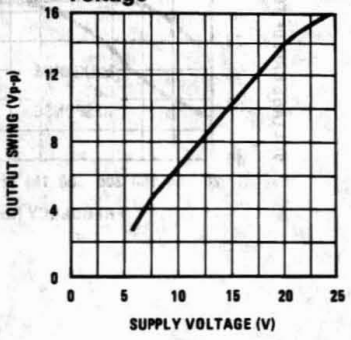
Power Dissipation (W) Both Channels Operating



Open Loop Gain vs Frequency



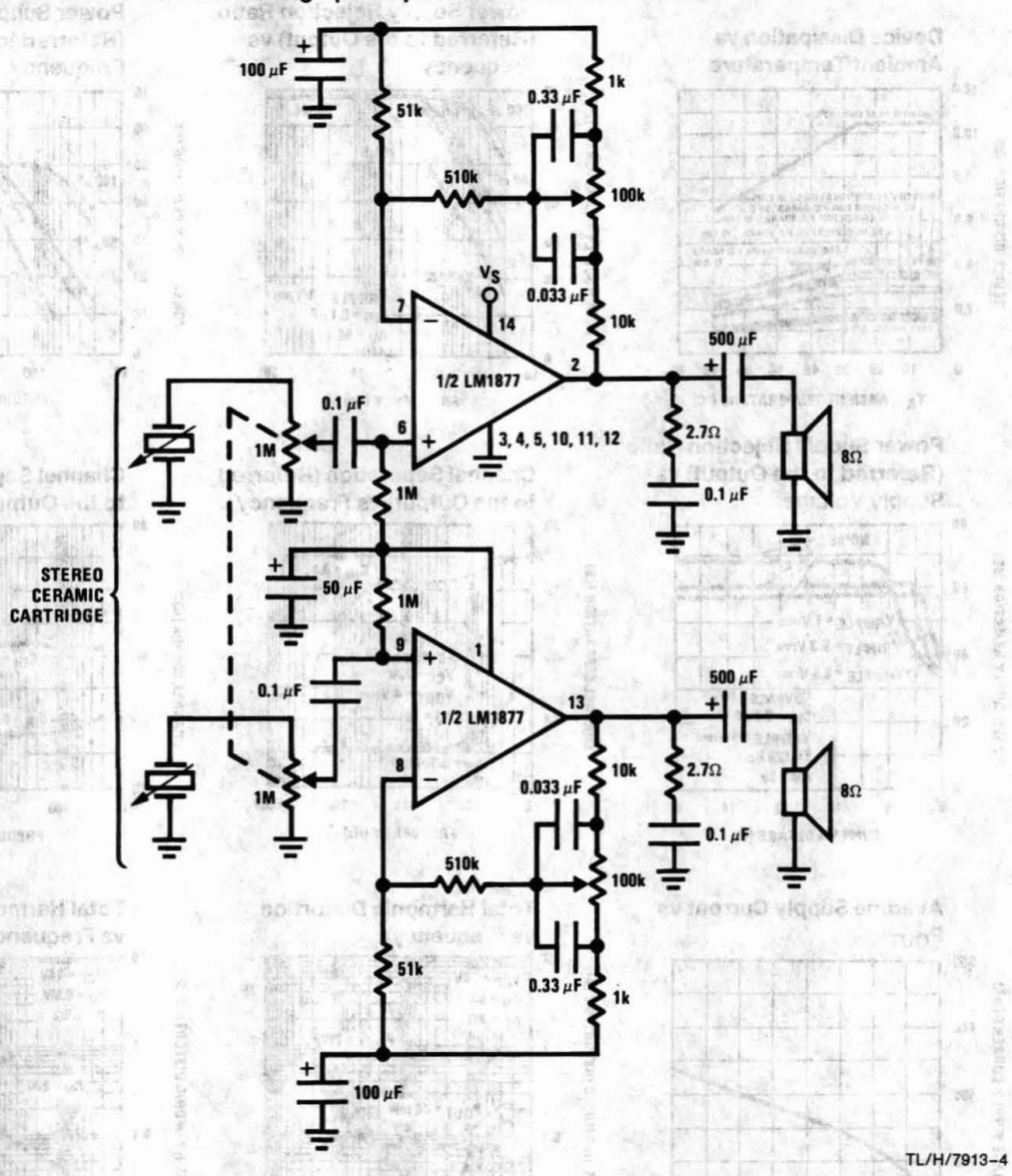
Output Swing vs Supply Voltage



TL/H/7913–3

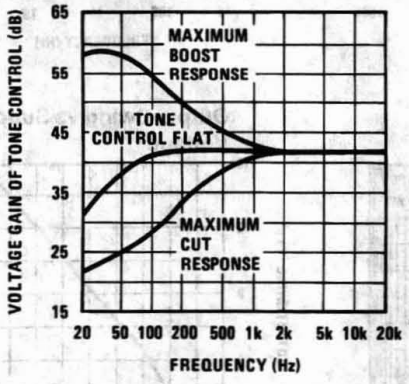
Typical Applications

Stereo Phonograph Amplifier with Bass Tone Control



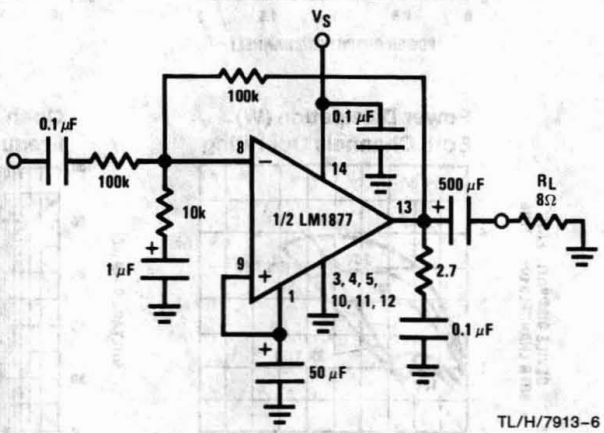
TL/H/7913–4

Frequency Response of Bass Tone Control



TL/H/7913–5

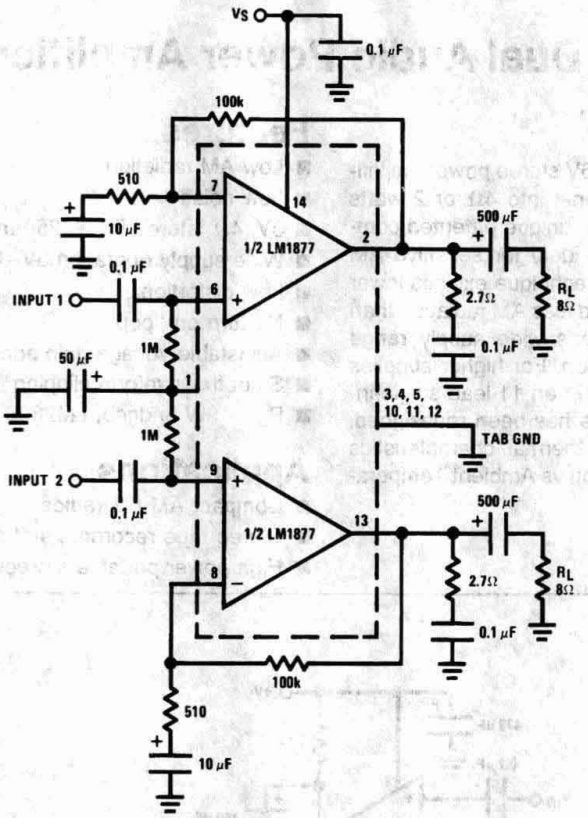
Inverting Unity Gain Amplifier



TL/H/7913–6

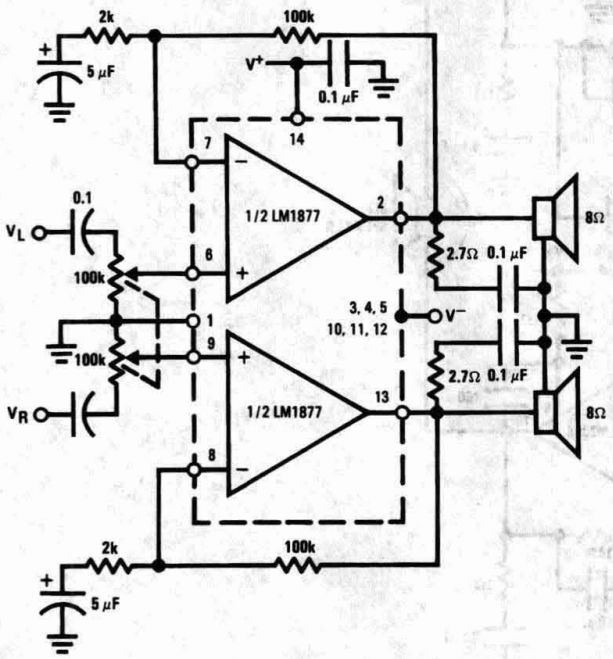
Typical Applications (Continued)

Stereo Amplifier with $A_V = 200$



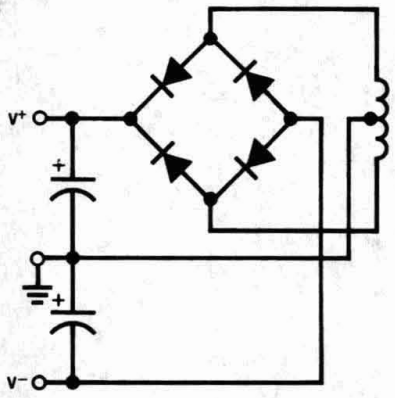
TL/H/7913–7

Non-Inverting Amplifier Using Split Supply



TL/H/7913–8

Typical Split Supply



TL/H/7913–9

National Semiconductor

LM1896/LM2896 Dual Audio Power Amplifier

General Description

The LM1896 is a high performance 6V stereo power amplifier designed to deliver 1 watt/channel into 4Ω or 2 watts bridged monaural into 8Ω. Utilizing a unique patented compensation scheme, the LM1896 is ideal for sensitive AM radio applications. This new circuit technique exhibits lower wideband noise, lower distortion, and less AM radiation than conventional designs. The amplifier's wide supply range (3V–9V) is ideal for battery operation. For higher supplies (V_S > 9V) the LM2896 is available in an 11-lead single-in-line package. The LM2896 package has been redesigned, resulting in the slightly degraded thermal characteristics shown in the figure Device Dissipation vs Ambient Temperature.

Features

- Low AM radiation
- Low noise
- 3V, 4Ω, stereo P_O = 250 mW
- Wide supply operation 3V–15V (LM2896)
- Low distortion
- No turn on "pop"
- Adjustable voltage gain and bandwidth
- Smooth waveform clipping
- P_O = 9W bridged, LM2896

Applications

- Compact AM-FM radios
- Stereo tape recorders and players
- High power portable stereos

Typical Applications

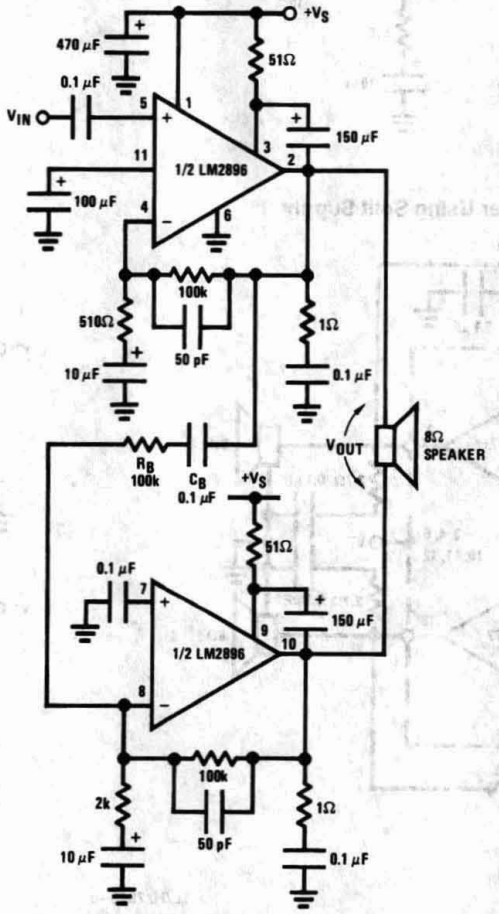


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FIGURE 1. LM2896 in Bridge Configuration (A_V = 400, BW = 20 kHz)

Order Number LM1896N **See NS Package Number N14A**

Order Number LM2896P **See NS Package Number P11A**

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage
- LM1896 $V_S = 12V$
- LM2896 $V_S = 18V$

Operating Temperature (Note 1) 0°C to +70°C

Storage Temperature −65°C to +150°C

Junction Temperature 150°C

Lead Temperature (Soldering, 10 sec.) 260°C

Thermal Resistance
- θ_{JC} (DIP) 30°C/W
- θ_{JA} (DIP) 137°C/W
- θ_{JC} (SIP) 10°C/W
- θ_{JA} (SIP) 55°C/W

Electrical Characteristics

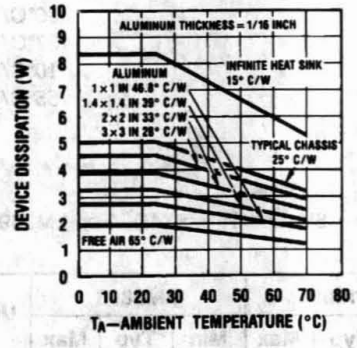
Unless otherwise specified, $T_A = 25°C$, $A_V = 200$ (46 dB). For the LM1896; $V_S = 6V$ and $R_L = 4\Omega$. For LM2896, $T_{TAB} = 25°C$, $V_S = 12V$ and $R_L = 8\Omega$. Test circuit shown in *Figure 2*.

Parameter	Conditions	LM1896			LM2896			Units
		Min	Typ	Max	Min	Typ	Max	
Supply Current	P_o = 0W, Dual Mode		15	25		25	40	mA
Operating Supply Voltage		3		10	3		15	V
Output Power	THD = 10%, f = 1 kHz							
LM1896N-1	$V_S = 6V$, $R_L = 4\Omega$ Dual Mode, $T_A = 25°C$	0.9	1.1					W/ch
LM1896N-2	$V_S = 6V$, $R_L = 8\Omega$ Bridge Mode, $T_A = 25°C$		1.8	2.1				W
	$V_S = 9V$, $R_L = 8\Omega$ Dual Mode, $T_A = 25°C$		1.3					W/ch
LM2896P-1	$V_S = 12V$, $R_L = 8\Omega$ Dual Mode, $T_{TAB} = 25°C$				2.0	2.5		W/ch
LM2896P-2	$V_S = 12V$, $R_L = 8\Omega$ Bridge Mode, $T_{TAB} = 25°C$				7.2	9.0		W
	$V_S = 9V$, $R_L = 4\Omega$ Bridge Mode, $T_{TAB} = 25°C$					7.8		W
	$V_S = 9V$, $R_L = 4\Omega$ Dual Mode, $T_{TAB} = 25°C$					2.5		W/ch
Distortion	f = 1 kHz							
	P_o = 50 mW		0.09			0.09		%
	P_o = 0.5W		0.11			0.11		%
	P_o = 1W					0.14		%
Power Supply Rejection Ratio (PSRR)	$C_{BY} = 100\ \mu F$, f = 1 kHz, $C_{IN} = 0.1\ \mu F$, Output Referred, $V_{RIPPLE} = 250$ mV	−40	−54		−40	−54		dB
Channel Separation	$C_{BY} = 100\ \mu F$, f = 1 kHz, $C_{IN} = 0.1\ \mu F$, Output Referred	−50	−64		−50	−64		dB
Noise	Equivalent Input Noise $R_S = 0$,							
	$C_{IN} = 0.1\ \mu F$, BW = 20 − 20 kHz		1.4			1.4		μV
	CCIR/ARM		1.4			1.4		μV
	Wideband		2.0			2.0		μV
DC Output Level		2.8	3	3.2	5.6	6	6.4	V
Input Impedance		50	100	350	50	100	350	kΩ
Input Offset Voltage			5			5		mV
Voltage Difference between Outputs	LM1896N-2, LM2896P-2		10	20		10	20	mV
Input Bias Current			120			120		nA

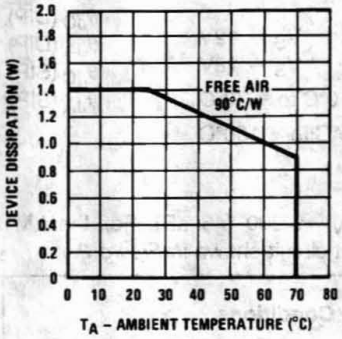
Note 1: For operation at ambient temperature greater than 25°C, the LM1896/LM2896 must be derated based on a maximum 150°C junction temperature using a thermal resistance which depends upon mounting techniques.

Typical Performance Curves

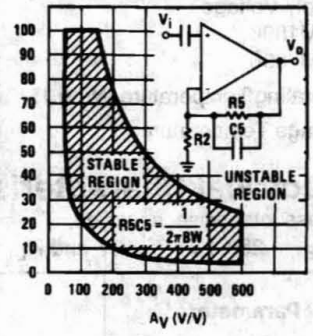
LM2896 Device Dissipation vs Ambient Temperature



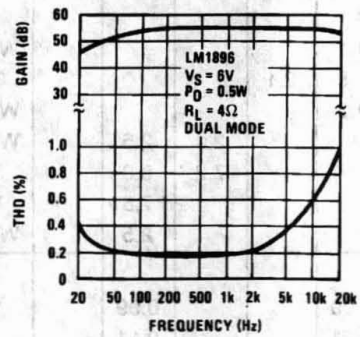
LM1896 Maximum Device Dissipation vs Ambient Temperature



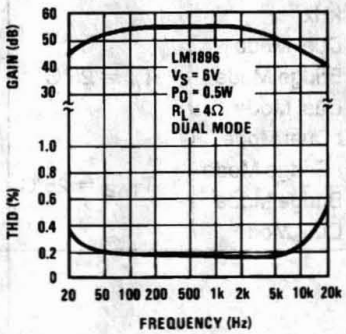
−3 dB Bandwidth vs Voltage Gain for Stable Operation



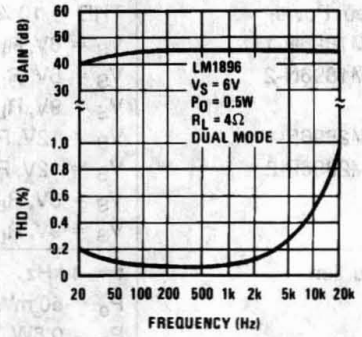
THD and Gain vs Frequency
AV = 54 dB, BW = 30 kHz



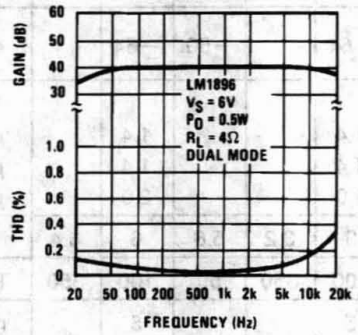
THD and Gain vs Frequency
AV = 54 dB, BW = 5 kHz



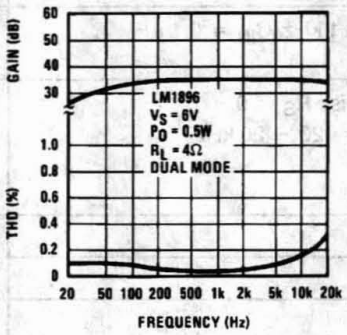
THD and Gain vs Frequency
AV = 46 dB, BW = 50 kHz



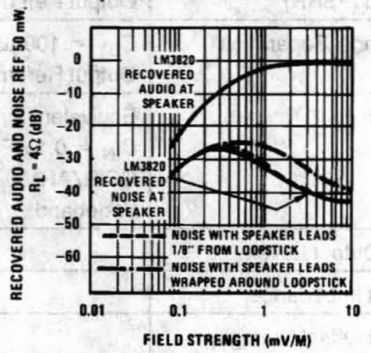
THD and Gain vs Frequency
AV = 40 dB, BW = 20 kHz



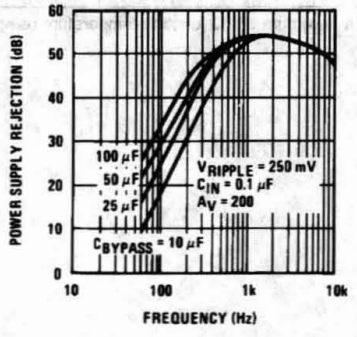
THD and Gain vs Frequency
AV = 34 dB, BW = 50 kHz



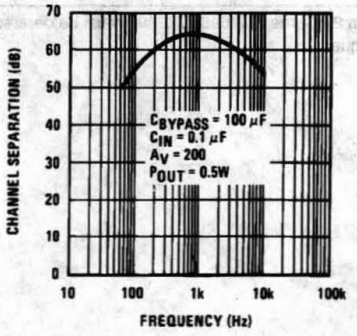
AM Recovered Audio and Noise vs Field Strength for Different Speaker Lead Placement


LM3820 RECOVERED AUDIO AT SPEAKER
LM3820 RECOVERED NOISE AT SPEAKER
NOISE WITH SPEAKER LEADS 1/8" FROM LOOPSTICK
NOISE WITH SPEAKER LEADS WRAPPED AROUND LOOPSTICK
RECOVERED AUDIO AND NOISE REF 50 mW, RL = 4Ω (dB)
FIELD STRENGTH (mV/M)

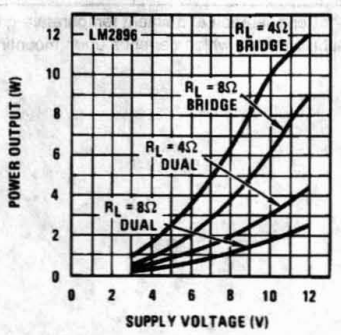
Power Supply Rejection Ratio (Referred to the Output) vs Frequency



Channel Separation (Referred to the Output) vs Frequency



Power Output vs Supply Voltage



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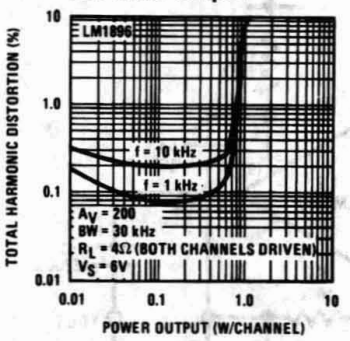
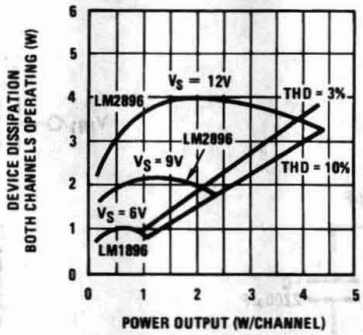
Typical Performance Curves (Continued)

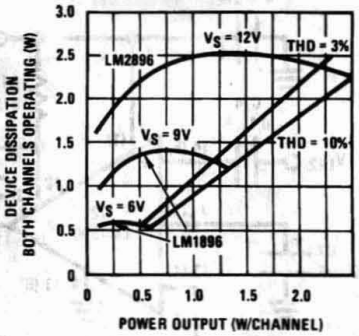
Total Harmonic Distortion vs Power Output



Power Dissipation vs Power Output R_L = 4Ω



Power Dissipation vs Power Output R_L = 8Ω



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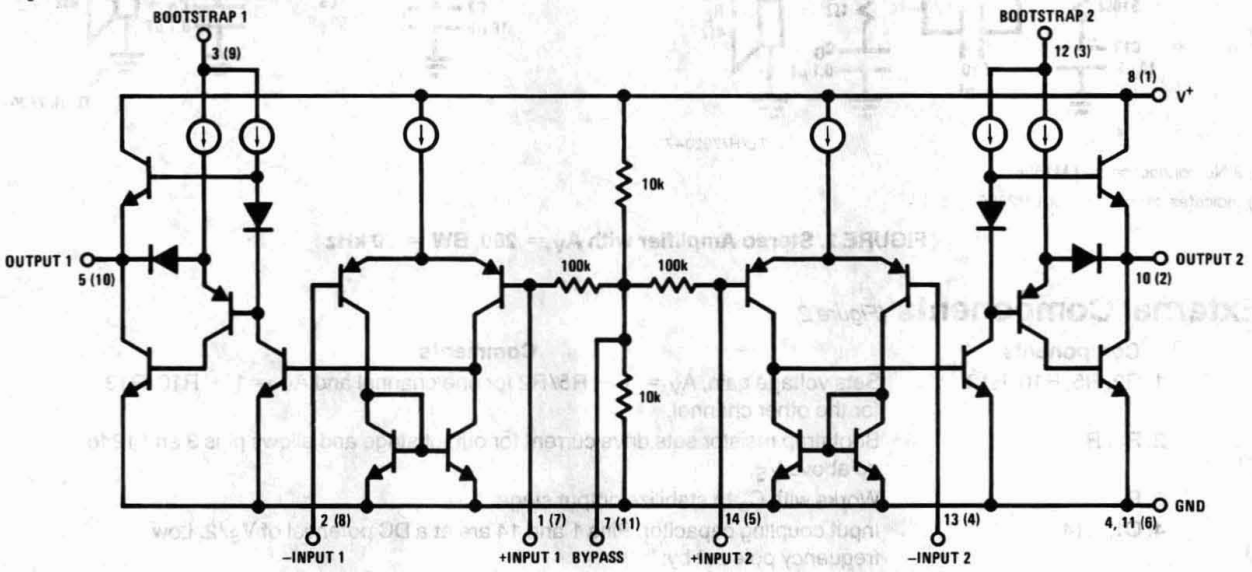
Equivalent Schematic



6, 9 No connection on LM1896

( ) indicates pin number for LM2896

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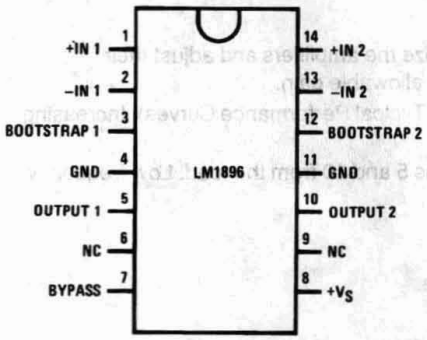
Connection Diagrams

Dual-In-Line Package



Top View

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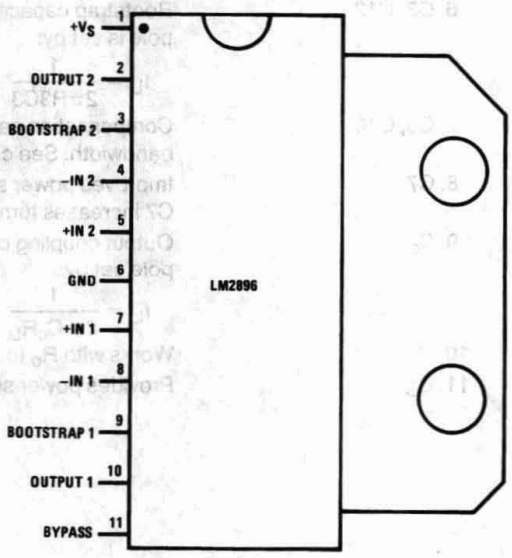
Single-In-Line Package



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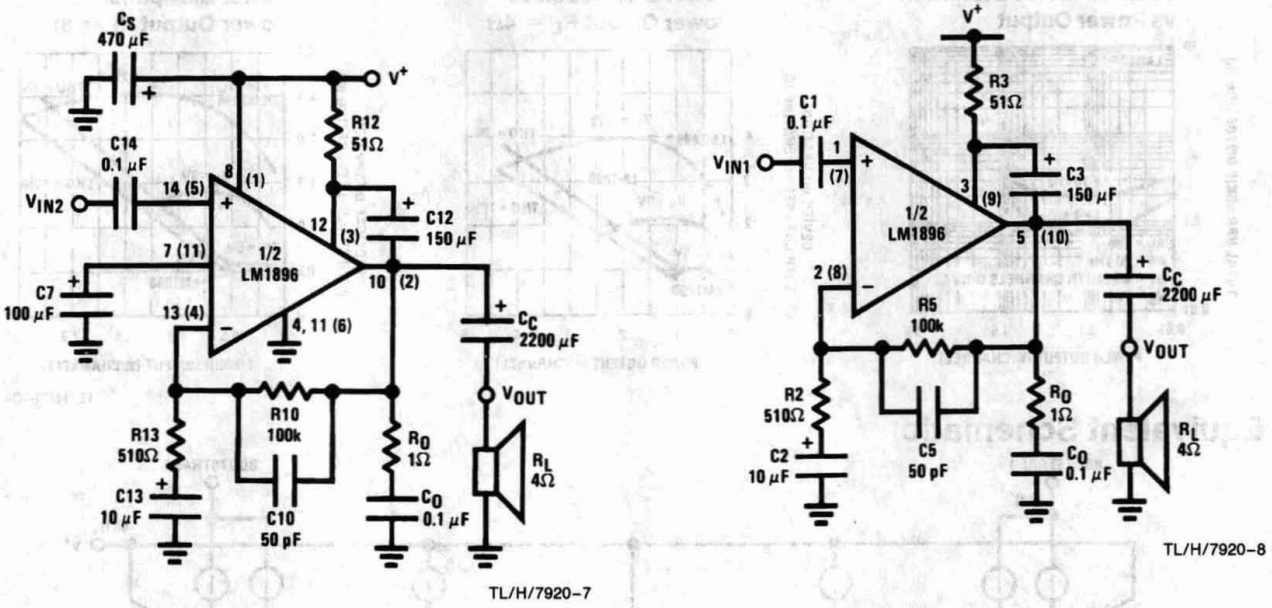
Top View

Typical Applications (Continued)



6, 9 No connection on LM1896

( ) Indicates pin number for LM2896

FIGURE 2. Stereo Amplifier with A_V = 200, BW = 30 kHz

External Components *(Figure 2)*

Components	Comments
1. R2, R5, R10, R13	Sets voltage gain, $A_V = 1 + R5/R2$ for one channel and $A_V = 1 + R10/R13$ for the other channel.
2. R3, R12	Bootstrap resistor sets drive current for output stage and allows pins 3 and 12 to go above V_S.
3. R_o	Works with C_o to stabilize output stage.
4. C1, C14	Input coupling capacitor. Pins 1 and 14 are at a DC potential of $V_S/2$. Low frequency pole set by: $f_L = \frac{1}{2\pi R_{IN} C1}$
5. C2, C13	Feedback capacitors. Ensure unity gain at DC. Also a low frequency pole at: $f_L = \frac{1}{2\pi R2C2}$
6. C3, C12	Bootstrap capacitors, used to increase drive to output stage. A low frequency pole is set by: $f_L = \frac{1}{2\pi R3C3}$
7. C5, C10	Compensation capacitor. These stabilize the amplifiers and adjust their bandwidth. See curve of bandwidth vs allowable gain.
8. C7	Improves power supply rejection (See Typical Performance Curves). Increasing C7 increases turn-on delay.
9. C_c	Output coupling capacitor. Isolates pins 5 and 10 from the load. Low frequency pole set by: $f_L = \frac{1}{2\pi C_c R_L}$
10. C_o	Works with R_o to stabilize output stage.
11. C_S	Provides power supply filtering.

Application Hints

AM Radios

The LM1896/LM2896 has been designed fo fill a wide range of audio power applications. A common problem with IC audio power amplifiers has been poor signal-to-noise performance when used in AM radio applications. In a typical radio application, the loopstick antenna is in close proximity to the audio amplifer. Current flowing in the speaker and power supply leads can cause electromagnetic coupling to the loopstick, resulting in system oscillation. In addition, most audio power amplifiers are not optimized for lowest noise because of compensation requirements. If noise from the audio amplifier radiates into the AM section, the sensitivity and signal-to-noise ratio will be degraded.

The LM1896 exhibits extremely low wideband noise due in part to an external capacitor C5 which is used to tailor the bandwidth. The circuit shown in *Figure 2* is capable of a signal-to-noise ratio in excess of 60 dB referred to 50 mW. Capacitor C5 not only limits the closed loop bandwidth, it also provides overall loop compensation. Neglecting C2 in *Figure 2*, the gain is:

$$A_V(S) = \frac{S + A_V\,\omega_o}{S + \omega_o}$$

$$\text{where } A_V = \frac{R2 + R5}{R2},\quad \omega_o = \frac{1}{R5C5}$$

A curve of −3 dB BW (ω_o) vs A_V is shown in the Typical Performance Curves.

Figure 3 shows a plot of recovered audio as a function of field strength in μV/M. The receiver section in this example is an LM3820. The power amplifier is located about two inches from the loopstick antenna. Speaker leads run parallel to the loopstick and are 1/8 inch from it. Referenced to a 20 dB S/N ratio, the improvement in noise performance over conventional designs is about 10 dB. This corresponds to an increase in usable sensitivity of about 8.5 dB.

Bridge Amplifiers

The LM1896/LM2896 can be used in the bridge mode as a monaural power amplifier. In addition to much higher power output, the bridge configuration does not require output coupling capacitors. The load is connected directly between the amplifier outputs as shown in *Figure 4*.

Amp 1 has a voltage gain set by 1 + R5/R2. The output of amp 1 drives amp 2 which is configured as an inverting amplifier with unity gain. Because of this phase inversion in amp 2, there is a 6 dB increase in voltage gain referenced to V_i. The voltage gain in bridge is:

$$\frac{V_o}{V_i} = 2\left(1 + \frac{R5}{R2}\right)$$

C_B is used to prevent DC voltage on the output of amp 1 from causing offset in amp 2. Low frequency response is influenced by:

$$f_L = \frac{1}{2\pi\, R_B C_B}$$

Several precautions should be observed when using the LM1896/LM2896 in bridge configuration. Because the amplifiers are driving the load out of phase, an 8Ω speaker will appear as a 4Ω load, and a 4Ω speaker will appear as a 2Ω load. Power dissipation is twice as severe in this situation. For example, if V_S = 6V and R_L = 8Ω bridged, then the maximum dissipation is:

$$P_D = \frac{V_S^2}{20\,R_L} \times 2 = \frac{6^2}{20 \times 4} \times 2$$

$$P_D = 0.9 \text{ Watts}$$

This amount of dissipation is equivalent to driving two 4Ω loads in the stereo configuration.

When adjusting the frequency response in the bridge configuration, R5C5 and R10C10 form a 2 pole cascade and the −3 dB bandwidth is actually shifted to a lower frequency:

$$BW = \frac{0.707}{2\pi RC}$$

where R = feedback resistor

C = feedback capacitor

To measure the output voltage, a floating or differential meter should be used because a prolonged output short will over dissipate the package. *Figure 1* shows the complete bridge amplifier.

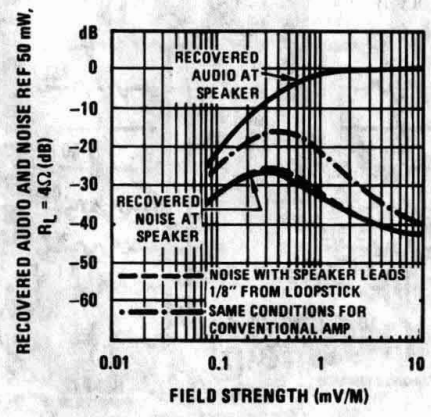


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FIGURE 3. Improved AM Sensitivity over Conventional Design

Application Hints (Continued)

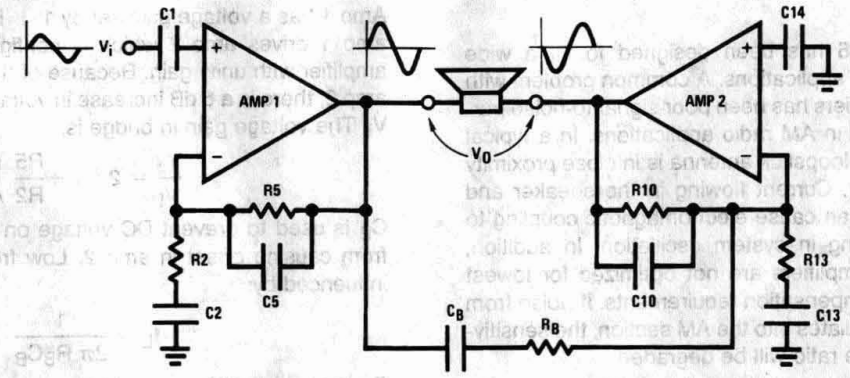

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Figure 4. Bridge Amplifier Connection

Printed Circuit Layout

Printed Circuit Board Layout

Figure 5 and *Figure 6* show printed circuit board layouts for the LM1896 and LM2896. The circuits are wired as stereo amplifiers. The signal source ground should return to the input ground shown on the boards. Returning the loads to power supply ground through a separate wire will keep the THD at its lowest value. The inputs should be terminated in less than 50 kΩ to prevent an input-output oscillation. This oscillation is dependent on the gain and the proximity of the bridge elements R_B and C_B to the (+) input. If the bridge mode is not used, do not insert R_B, C_B into the PCB.

To wire the amplifer into the bridge configuration, short the capacitor on pin 7 (pin 1 of the LM1896) to ground. Connect together the nodes labeled BRIDGE and drive the capacitor connected to pin 5 (pin 14 of the LM1896).

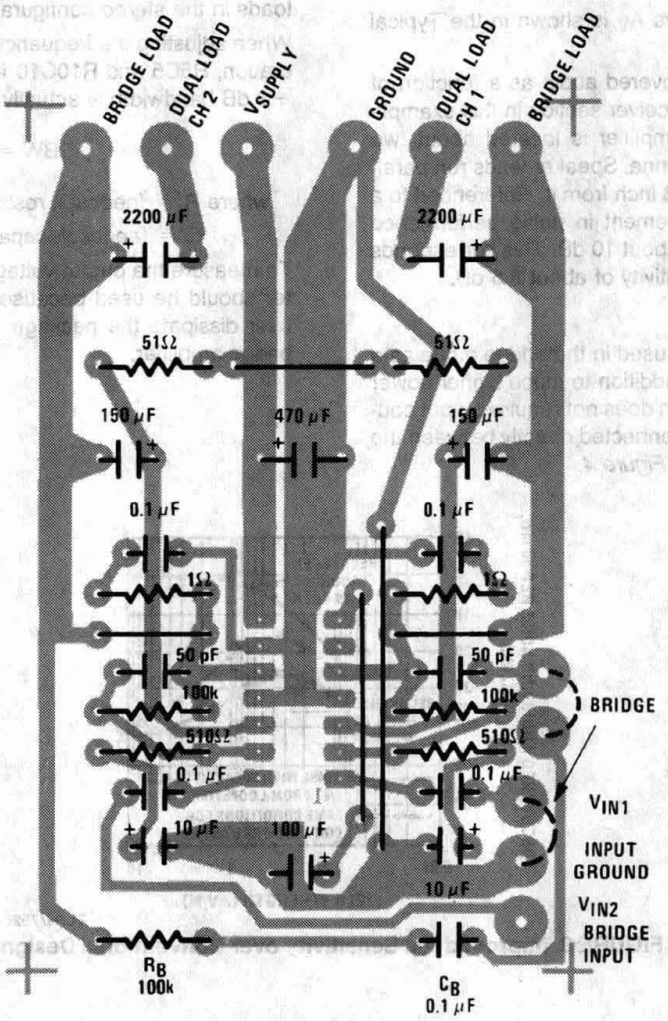

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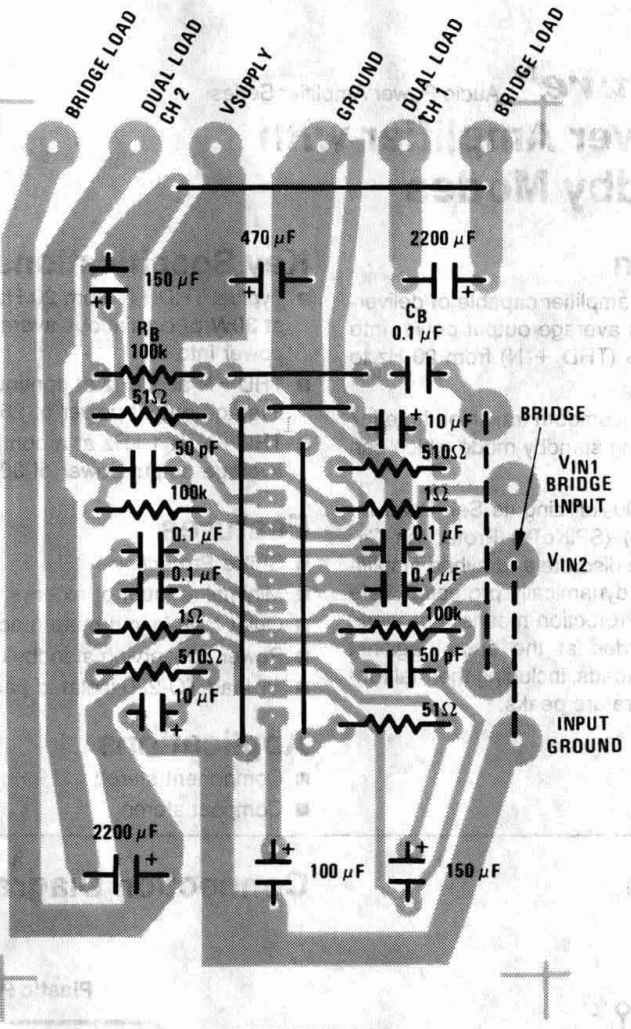
FIGURE 5. Printed Circuit Board Layout for the LM1896

Printed Circuit Layout (Continued)



COMPONENT SIDE

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FIGURE 6. Printed Circuit Board Layout for the LM2896

National Semiconductor

PRELIMINARY

LM4700 *Overture*™ Audio Power Amplifier Series
30W Audio Power Amplifier with Mute and Standby Modes

General Description

The LM4700 is an audio power amplifier capable of delivering typically 30W of continuous average output power into an 8Ω load with less than 0.8% (THD + N) from 20 Hz to 20 kHz.

The LM4700 has an independent smooth transition fade-in/out mute and a power conserving standby mode which can be controlled by external logic.

The performance of the LM4700, utilizing its Self Peak Instantaneous Temperature (°Ke) (SPiKe™) Protection Circuitry, places it in a class above discrete and hybrid amplifiers by providing an inherently, dynamically protected Safe Operating Area (SOA). SPiKe Protection means that these parts are completely safeguarded at the output against overvoltage, undervoltage, overloads, including thermal runaway and instantaneous temperature peaks.

Key Specifications

- Typical THD+N from 20 Hz to 20 kHz at 30W of continuous average output power into 8Ω — 0.08% (typ)
- THD+N at 1 kHz at continuous average output power of 25W into 8Ω — 0.1% (max)
- THD+N at 1 kHz at a continuous average output power of 30W into 8Ω — 0.009% (typ)

Features

- SPiKe Protection
- Minimal amount of external components necessary
- Quiet fade-in/out mute function
- Power conserving standby-mode
- 11-lead TO-220 isolated package

Applications

- Component stereo
- Compact stereo

Typical Application

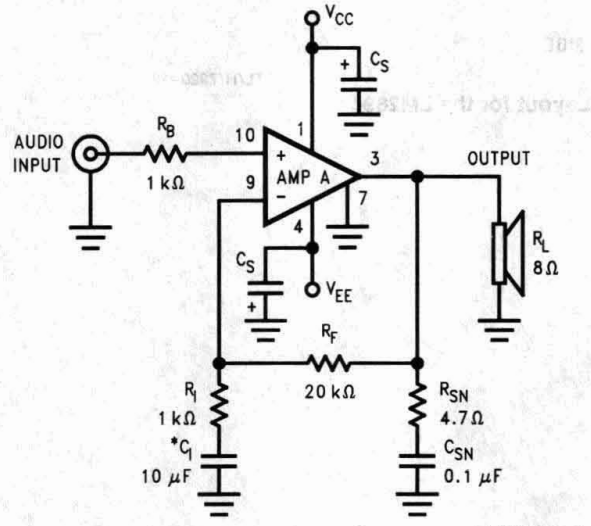

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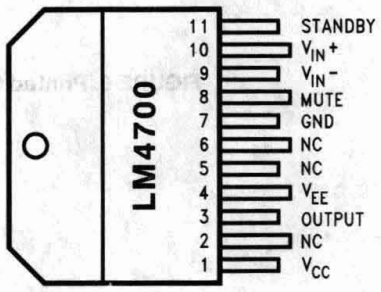
FIGURE 1. Typical Audio Amplifier Application Circuit

Connection Diagram

Plastic Package



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Top View

Order Number LM4700TF
See NS Package Number TF11B

National Semiconductor

LM2876 *Overture*™ Audio Power Amplifier Series
High-Performance 40W Audio Power Amplifier w/Mute

General Description

The LM2876 is a high-performance audio power amplifier capable of delivering 40W of continuous average power to an 8Ω load with 0.1% (THD + N) from 20 Hz–20 kHz.

The performance of the LM2876, utilizing its Self Peak Instantaneous Temperature (°Ke) (**SPiKe**™) Protection Circuitry, puts it in a class above discrete and hybrid amplifiers by providing an inherently, dynamically protected Safe Operating Area (SOA). **SPiKe** Protection means that these parts are completely safeguarded at the output against overvoltage, undervoltage, overloads, including shorts to the supplies, thermal runaway, and instantaneous temperature peaks.

The LM2876 maintains an excellent Signal-to-Noise Ratio of greater than 95 dB(min) with a typical low noise floor of 2.0 μV. It exhibits extremely low (THD + N) values of 0.06% at the rated output into the rated load over the audio spectrum, and provides excellent linearity with an IMD (SMPTE) typical rating of 0.004%.

Features

- 40W continuous average output power into 8Ω
- 75W instantaneous peak output power capability
- Signal-to-Noise Ratio ≥ 95 dB(min)
- An input mute function
- Output protection from a short to ground or to the supplies via internal current limiting circuitry
- Output over-voltage protection against transients from inductive loads
- Supply under-voltage protection, not allowing internal biasing to occur when $|V_{EE}| + |V_{CC}| \leq 12V$, thus eliminating turn-on and turn-off transients
- 11-lead TO-220 package

Applications

- Component stereo
- Compact stereo
- Self-powered speakers
- Surround-sound amplifiers
- High-end stereo TVs

Typical Application

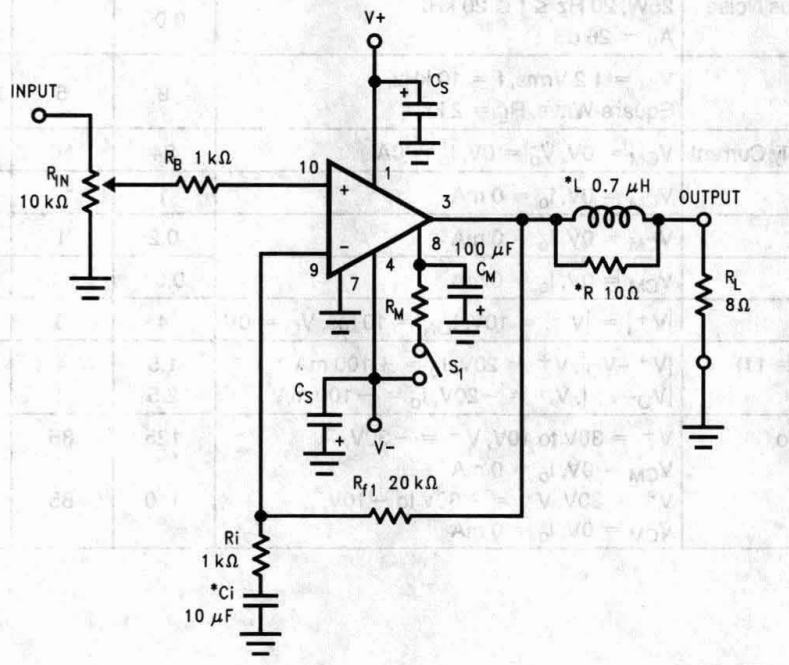

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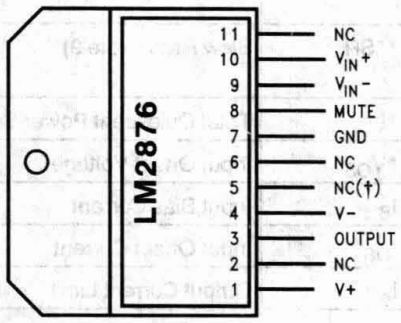
FIGURE 1. Typical Audio Amplifier Application Circuit

*Optional components dependent upon specific design requirements. Refer to the External Components Description section for a component functional description.

Connection Diagram

Plastic Package (Note 8)



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Top View
Order Number LM2876T or LM2876TF
See NS Package Number TA11B for Staggered Lead Non-Isolated Package or TF11B* for Staggered Lead Isolated Package

†Connect Pin 5 to V+ for Compatibility with LM3886.

*Preliminary: Call your local National sales rep. or distributor for availability.

Absolute Maximum Ratings (Notes 1, 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage $\|V^+\| + \|V^-\|$ (No Signal)	72V
Supply Voltage $\|V^+\| + \|V^-\|$ (Input Signal)	70V
Common Mode Input Voltage	(V^+ or V^-) and $\|V^+\| + \|V^-\| \leq 60V$
Differential Input Voltage	60V
Output Current	Internally Limited
Power Dissipation (Note 3)	125W
ESD Susceptibility (Note 4)	3000V
Junction Temperature (Note 5)	150°C
Soldering Information T Package (10 seconds)	260°C
Storage Temperature	−40°C to +150°C
Thermal Resistance	
θ_{JC}	1°C/W
θ_{JA}	43°C/W

Operating Ratings (Notes 1 and 2)

Temperature Range	
$T_{MIN} \leq T_A \leq T_{MAX}$	$-20°C \leq T_A \leq +85°C$
Supply Voltage $\|V^+\| + \|V^-\|$	20V to 60V

Note: Operation is guaranteed up to 60V, however, distortion may be introduced from **SPiKe** Protection Circuitry if proper thermal considerations are not taken into account. Refer to the **Thermal Considerations** section for more information.

(See **SPiKe** Protection Response)

Electrical Characteristics (Notes 1, 2) The following specifications apply for $V^+ = +30V$, $V^- = -30V$, $I_{MUTE} = -0.5$ mA with $R_L = 8\Omega$ unless otherwise specified. Limits apply for $T_A = 25°C$.

Symbol	Parameter	Conditions	LM2876 Typical (Note 6)	LM2876 Limit (Note 7)	Units (Limits)
$\|V^+\| + \|V^-\|$	Power Supply Voltage (Note 10)	$V_{pin7} - V^- \geq 9V$	18	20 60	V (min) V (max)
A_M	Mute Attenuation	Pin 8 Open or at 0V, Mute: On Current out of Pin 8 > 0.5 mA, Mute: Off	115	80	dB (min)
**P_O	Output Power (Continuous Average)	THD + N = 0.1% (max) f = 1 kHz; f = 20 kHz	40	25	W (min)
Peak P_O	Instantaneous Peak Output Power		75		W
THD + N	Total Harmonic Distortion Plus Noise	25W, 20 Hz ≤ f ≤ 20 kHz A_V = 26 dB	0.06		%
**SR	Slew Rate (Note 9)	V_{IN} = 1.2 Vrms, f = 10 kHz, Square-Wave, R_L = 2 kΩ	9	5	V/μs (min)
*I^+	Total Quiescent Power Supply Current	V_{CM} = 0V, V_O = 0V, I_O = 0A	24	50	mA (max)
*V_{OS}	Input Offset Voltage	V_{CM} = 0V, I_O = 0 mA	1	10	mV (max)
I_B	Input Bias Current	V_{CM} = 0V, I_O = 0 mA	0.2	1	μA (max)
I_{OS}	Input Offset Current	V_{CM} = 0V, I_O = 0 mA	0.01	0.2	μA (max)
I_O	Output Current Limit	$\|V^+\| = \|V^-\|$ = 10V, t_{ON} = 10 ms, V_O = 0V	4	3	A (min)
*V_{od}	Output Dropout Voltage (Note 11)	$\|V^+ - V_O\|$, V^+ = 20V, I_O = +100 mA $\|V_O - V^-\|$, V^- = −20V, I_O = −100 mA	1.5 2.5	4 4	V (max) V (max)
*PSRR	Power Supply Rejection Ratio	V^+ = 30V to 10V, V^- = −30V, V_{CM} = 0V, I_O = 0 mA V^+ = 30V, V^- = −30V to −10V, V_{CM} = 0V, I_O = 0 mA	125 110	85 85	dB (min) dB (min)

*DC Electrical Test; refer to Test Circuit #1.

**AC Electrical Test; refer to Test Circuit #2.

Electrical Characteristics (Notes 1, 2)

The following specifications apply for $V^+ = +30V$, $V^- = -30V$, $I_{MUTE} = -0.5$ mA with $R_L = 8\Omega$ unless otherwise specified. Limits apply for $T_A = 25°C$. (Continued)

Symbol	Parameter	Conditions	LM2876		Units (Limits)
			Typical (Note 6)	Limit (Note 7)	
*CMRR	Common Mode Rejection Ratio	$V^+ = 50V$ to $10V$, $V^- = -10V$ to $-50V$, $V_{CM} = 20V$ to $-20V$, $I_o = 0$ mA	110	75	dB (min)
*A_{VOL}	Open Loop Voltage Gain	$\|V^+\| = \|V^-\| = 30V$, $R_L = 2$ kΩ, $\Delta V_O = 40V$	115	80	dB (min)
GBWP	Gain-Bandwidth Product	$\|V^+\| = \|V^-\| = 30V$ $f_O = 100$ kHz, $V_{IN} = 50$ mVrms	8	2	MHz (min)
**eIN	Input Noise	IHF—A Weighting Filter $R_{IN} = 600\Omega$ (Input Referred)	2.0	8	μV (max)
SNR	Signal-to-Noise Ratio	$P_O = 1W$, A-Weighted, Measured at 1 kHz, $R_S = 25\Omega$	98		dB
		$P_O = 25W$, A-Weighted, Measured at 1 kHz, $R_S = 25\Omega$	112		dB
		Ppk = 75W, A-Weighted, Measured at 1 kHz, $R_S = 25\Omega$	117		dB
IMD	Intermodulation Distortion Test	60 Hz, 7 kHz, 4:1 (SMPTE) 60 Hz, 7 kHz, 1:1 (SMPTE)	0.004 0.006		%

*DC Electrical Test; refer to Test Circuit #1.

**AC Electrical Test; refer to Test Circuit #2.

Note 1: All voltages are measured with respect to the GND pin (pin 7), unless otherwise specified.

Note 2: *Absolute Maximum Ratings* indicate limits beyond which damage to the device may occur. *Operating Ratings* indicate conditions for which the device is functional, but do not guarantee specific performance limits. *Electrical Characteristics* state DC and AC electrical specifications under particular test conditions which guarantee specific performance limits. This assumes that the device is within the Operating Ratings. Specifications are not guaranteed for parameters where no limit is given, however, the typical value is a good indication of device performance.

Note 3: For operating at case temperatures above 25°C, the device must be derated based on a 150°C maximum junction temperature and a thermal resistance of $\theta_{JC} = 1.0$ °C/W (junction to case). Refer to the Thermal Resistance figure in the Application Information section under **Thermal Considerations**.

Note 4: Human body model, 100 pF discharged through a 1.5 kΩ resistor.

Note 5: The operating junction temperature maximum is 150°C, however, the instantaneous Safe Operating Area temperature is 250°C.

Note 6: Typicals are measured at 25°C and represent the parametric norm.

Note 7: Limits are guaranteed to National's AOQL (Average Outgoing Quality Level).

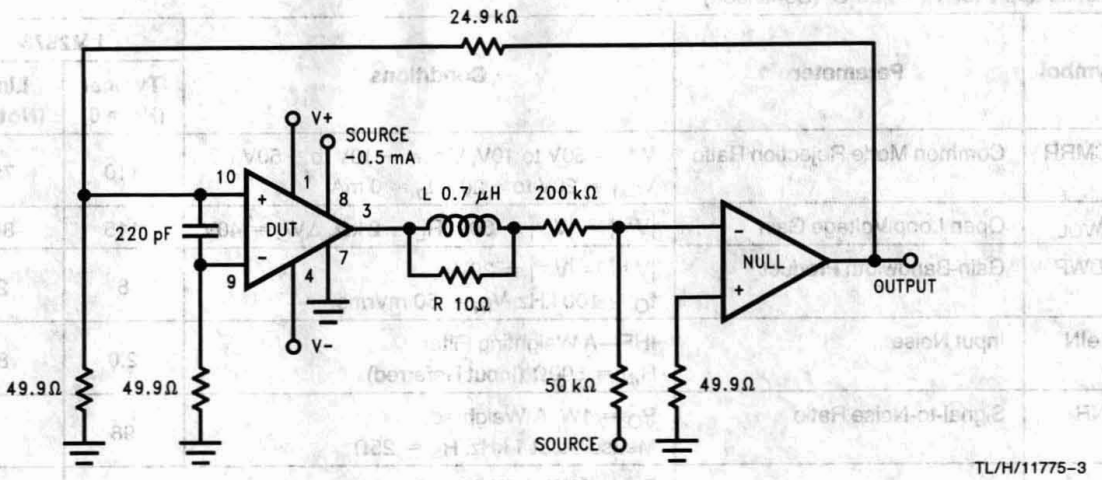
Note 8: The LM2876T package TA11B is a non-isolated package, setting the tab of the device and the heat sink at V^- potential when the LM2876 is directly mounted to the heat sink using only thermal compound. If a mica washer is used in addition to thermal compound, θ_{CS} (case to sink) is increased, but the heat sink will be isolated from V^-.

Note 9: The feedback compensation network limits the bandwidth of the closed-loop response and so the slew rate will be reduced due to the high frequency roll-off. Without feedback compensation, the slew rate is typically larger.

Note 10: V^- must have at least $-9V$ at its pin with reference to ground in order for the under-voltage protection circuitry to be disabled.

Note 11: The output dropout voltage is the supply voltage minus the clipping voltage. Refer to the Clipping Voltage vs Supply Voltage graph in the **Typical Performance Characteristics section.**

Test Circuit # 1 *(DC Electrical Test Circuit)



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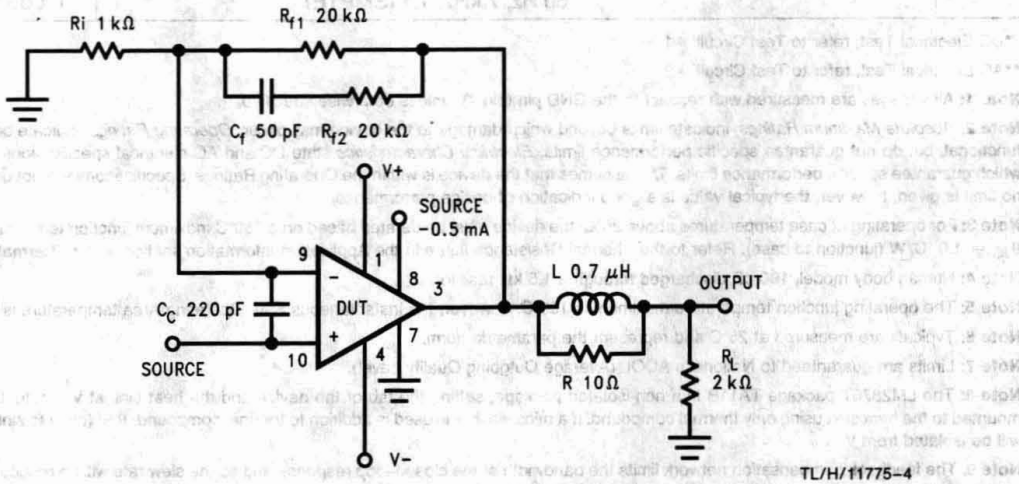
Test Circuit # 2 **(AC Electrical Test Circuit)



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Single Supply Application Circuit

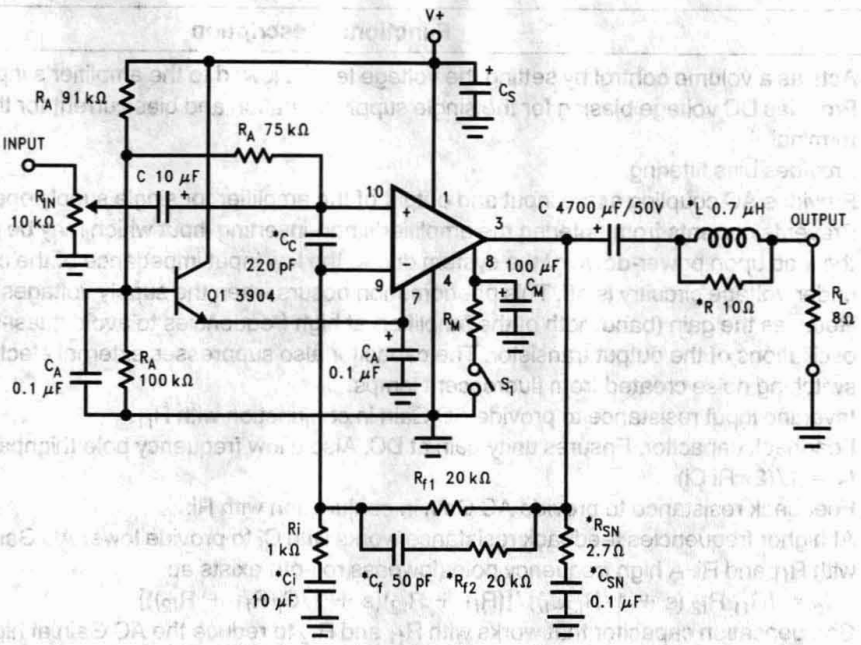

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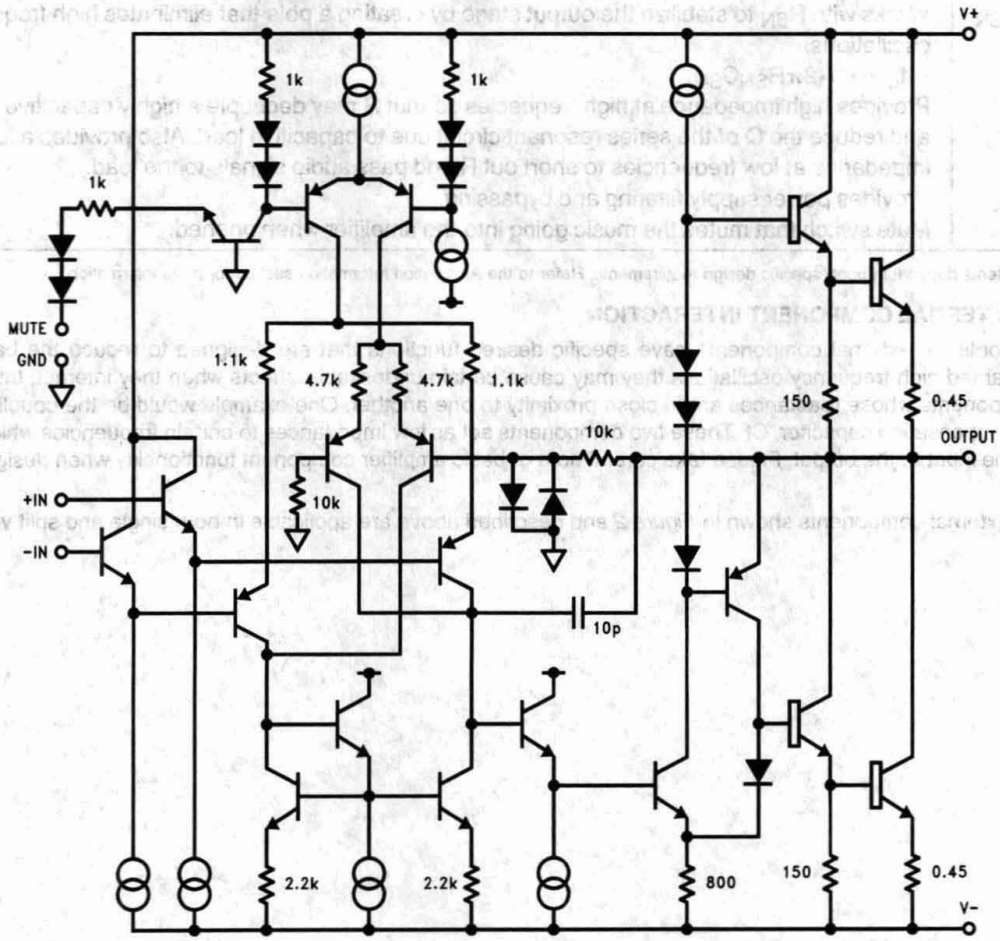
FIGURE 2. Typical Single Supply Audio Amplifier Application Circuit

*Optional components dependent upon specific design requirements. Refer to the External Components Description section for a component functional description.

Equivalent Schematic (excluding active protection circuitry)



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External Components Description (Figures 1 and 2)

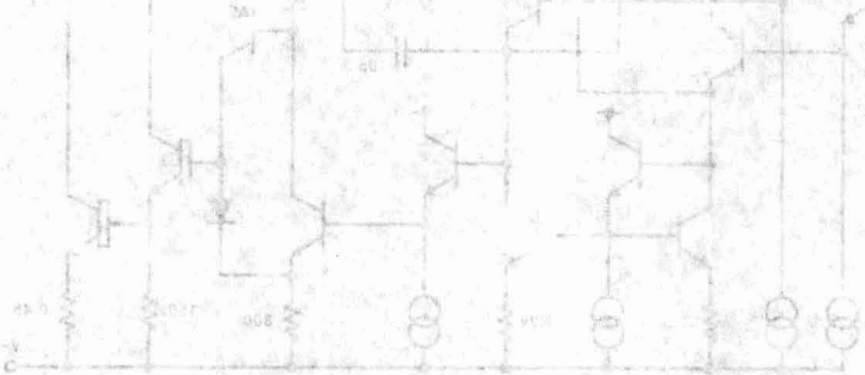
Components		Functional Description
1.	R_{IN}	Acts as a volume control by setting the voltage level allowed to the amplifier's input terminals.
2.	R_A	Provides DC voltage biasing for the single supply operation and bias current for the positive input terminal.
3.	C_A	Provides bias filtering.
4.	C	Provides AC coupling at the input and output of the amplifier for single supply operation.
5.	R_B	Prevents currents from entering the amplifier's non-inverting input which may be passed through to the load upon power-down of the system due to the low input impedance of the circuitry when the under-voltage circuitry is off. This phenomenon occurs when the supply voltages are below 1.5V.
6.	$*C_C$	Reduces the gain (bandwidth of the amplifier) at high frequencies to avoid quasi-saturation oscillations of the output transistor. The capacitor also suppresses external electromagnetic switching noise created from fluorescent lamps.
7.	Ri	Inverting input resistance to provide AC Gain in conjunction with R_{f1}.
8.	*Ci	Feedback capacitor. Ensures unity gain at DC. Also a low frequency pole (highpass roll-off) at: $f_c = 1/(2\pi Ri\ Ci)$
9.	R_{f1}	Feedback resistance to provide AC Gain in conjunction with Ri.
10.	$*R_{f2}$	At higher frequencies feedback resistance works with C_f to provide lower AC Gain in conjunction with R_{f1} and Ri. A high frequency pole (lowpass roll-off) exists at: $f_c = [R_{f1}\ R_{f2}\ (s + 1/R_{f2}C_f)]/[(R_{f1} + R_{f2})(s + 1/C_f(R_{f1} + R_{f2}))]$
11.	$*C_f$	Compensation capacitor that works with R_{f1} and R_{f2} to reduce the AC Gain at higher frequencies.
12.	R_M	Mute resistance set up to allow 0.5 mA to be drawn from pin 8 to turn the muting function off. → R_M is calculated using: $R_M \leq (\lvert V_{EE}\rvert - 2.6V)/I8$ where $I8 \geq 0.5$ mA. Refer to the Mute Attenuation vs Mute Current curves in the Typical Performance Characteristics section.
13.	C_M	Mute capacitance set up to create a large time constant for turn-on and turn-off muting.
14.	$*R_{SN}$	Works with C_{SN} to stabilize the output stage by creating a pole that eliminates high frequency oscillations.
15.	$*C_{SN}$	Works with R_{SN} to stabilize the output stage by creating a pole that eliminates high frequency oscillations. $f_c = 1/(2\pi R_{SN}C_{SN})$
16.	*L	Provides high impedance at high frequecies so that R may decouple a highly capacitive load
17.	*R	and reduce the Q of the series resonant circuit due to capacitive load. Also provides a low impedance at low frequencies to short out R and pass audio signals to the load.
18.	C_S	Provides power supply filtering and bypassing.
19.	S1	Mute switch that mutes the music going into the amplifier when opened.

*Optional components dependent upon specific design requirements. Refer to the Application Information section for more information.

OPTIONAL EXTERNAL COMPONENT INTERACTION

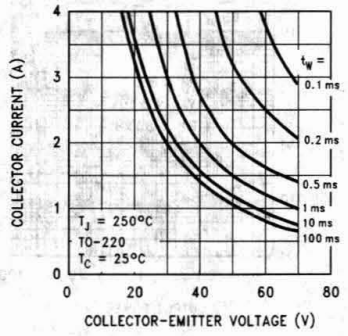
Although the optional external components have specific desired functions that are designed to reduce the bandwidth and eliminate unwanted high frequency oscillations they may cause certain undesirable effects when they interact. Interaction may occur for components whose reactances are in close proximity to one another. One example would be the coupling capacitor, C_C, and the compensation capacitor, Cf. These two components act as low impedances to certain frequencies which will couple signals from the input to the output. Please take careful note of basic amplifier component functionality when designing in these components.

The optional external components shown in *Figure 2* and described above are applicable in both single and split voltage supply configurations.

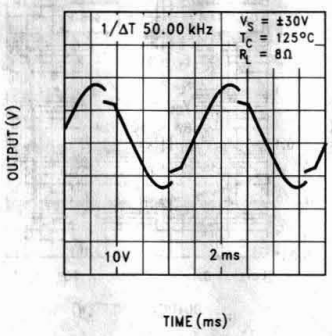


Typical Performance Characteristics

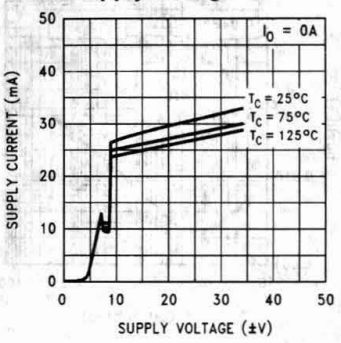
Safe Area



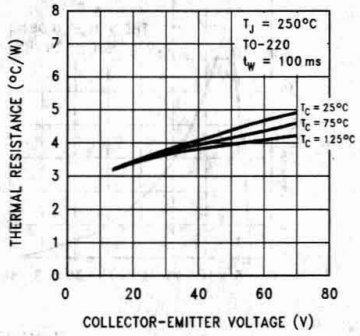
SPiKe™ Protection Response



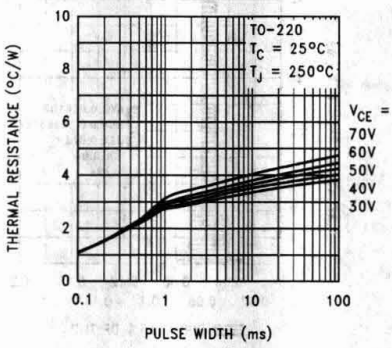
Supply Current vs Supply Voltage



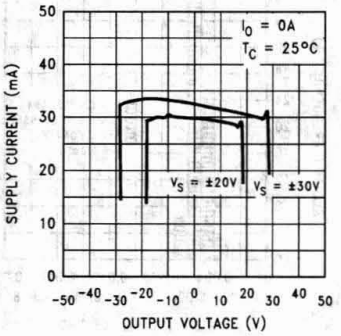
Pulse Thermal Resistance



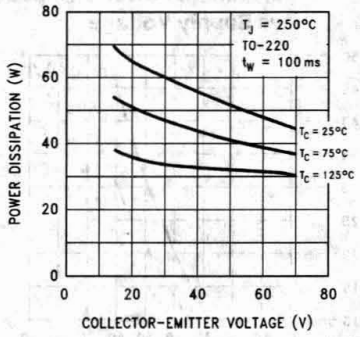
Pulse Thermal Resistance



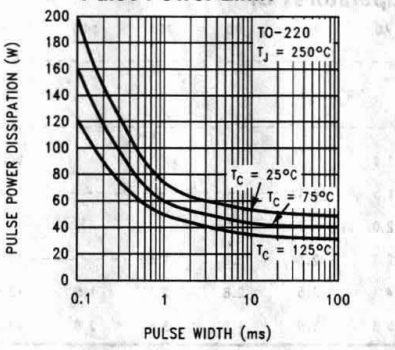
Supply Current vs Output Voltage



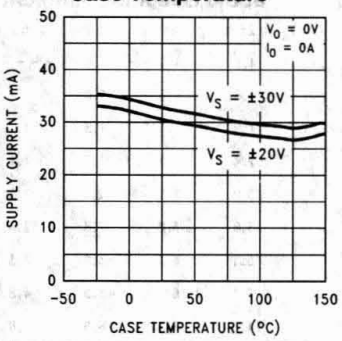
Pulse Power Limit



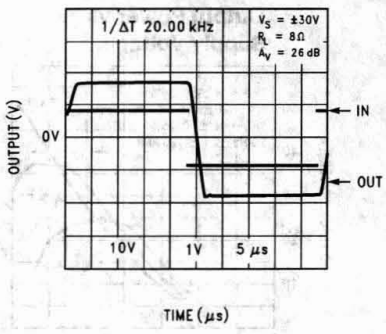
Pulse Power Limit



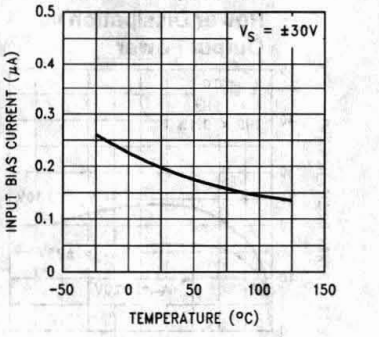
Supply Current vs Case Temperature



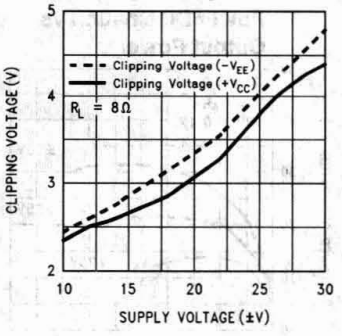
Pulse Response



Input Bias Current vs Case Temperature



Clipping Voltage vs Supply Voltage



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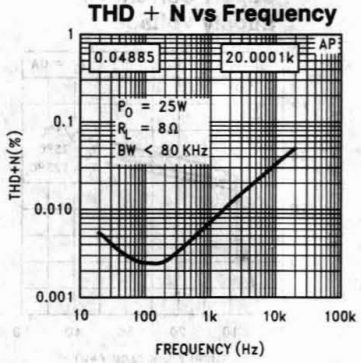
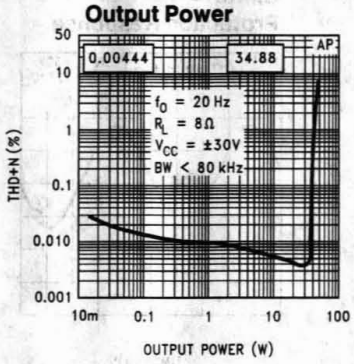
Typical Performance Characteristics (Continued)

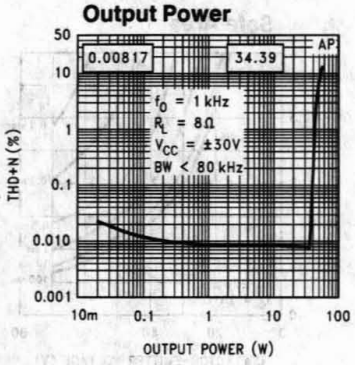
THD + N vs Frequency



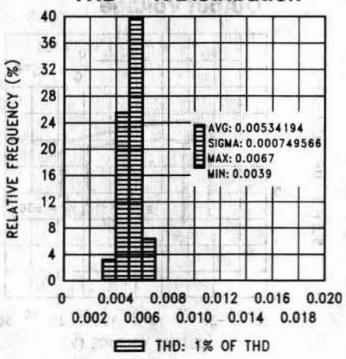
THD + N vs Output Power



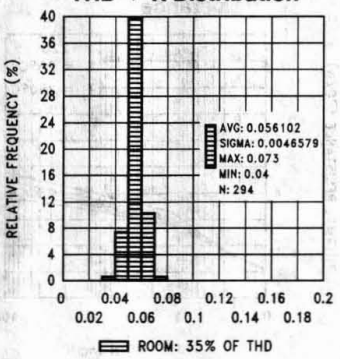
THD + N vs Output Power



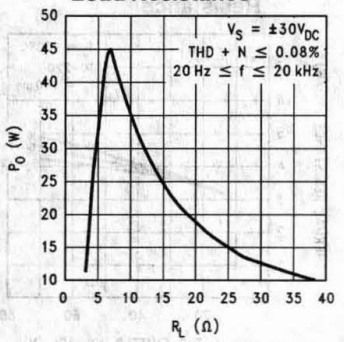
THD + N Distribution



THD + N Distribution



Output Power vs Load Resistance



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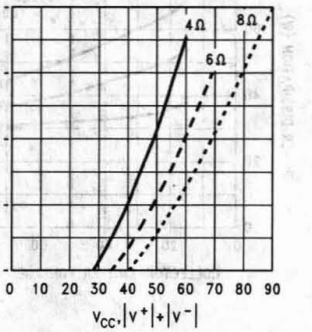
Max Heatsink Thermal Resistance (°C/W) at the Specified Ambient Temperature (°C)

T_A = 25°C	40	50	60	70	80	90	100	110	T_C, °C	P_D, W
1.3	1.0								90	50
1.6	1.2	1.0							96	45
1.9	1.6	1.3	1.1						102	40
2.4	1.9	1.7	1.4	1.1					108	35
3.0	2.5	2.1	1.8	1.5	1.1				114	30
3.8	3.2	2.8	2.4	2.0	1.6	1.2			120	25
5.1	4.3	3.8	3.3	2.8	2.3	1.8	1.3		126	20
7.1	6.1	5.5	4.8	4.1	3.5	2.8	2.1	1.5	132	15
11.3	9.8	8.8	7.8	6.8	5.8	4.8	3.8	2.8	138	10

Note: The maximum heat sink thermal resistance values, $\varnothing_{SA}$, in the table above were calculated using a $\varnothing_{CS}$ = 0.2°C/W due to thermal compound.

Maximum Power Dissipation vs Supply Voltage



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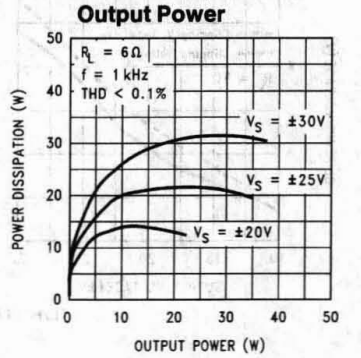
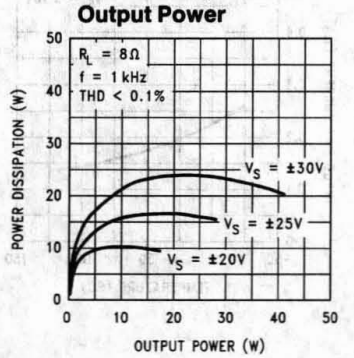
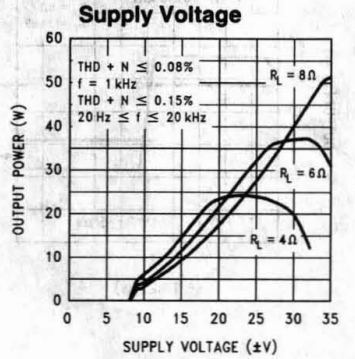
Power Dissipation vs Output Power



Power Dissipation vs Output Power



Output Power vs Supply Voltage



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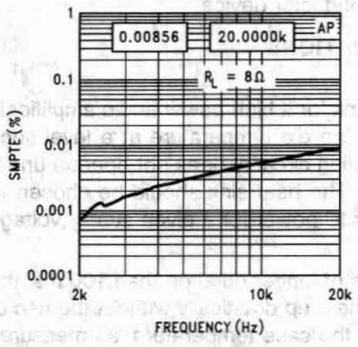
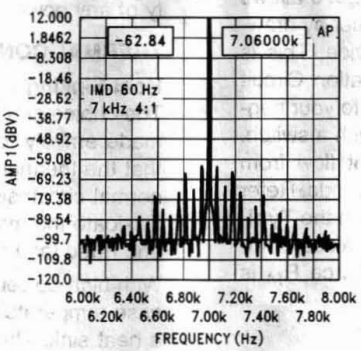
Typical Performance Characteristics (Continued)

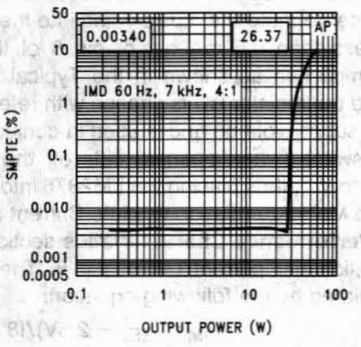
IMD 60 Hz, 4:1



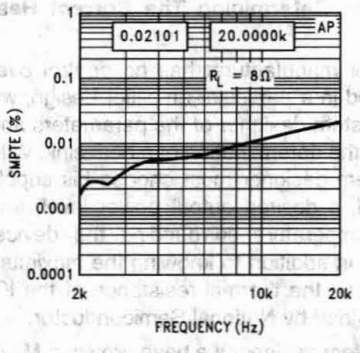
IMD 60 Hz, 7 kHz, 4:1



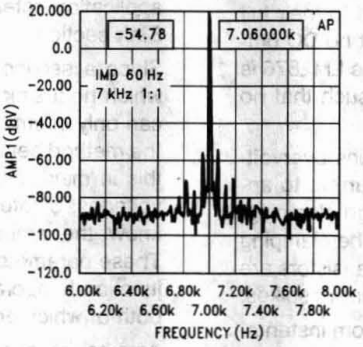
IMD 60 Hz, 7 kHz, 4:1



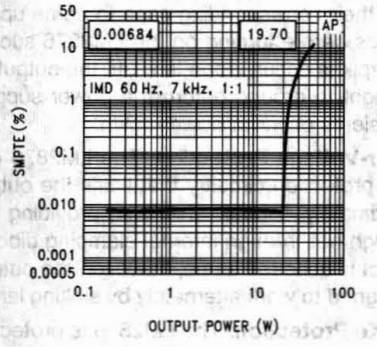
IMD 60 Hz, 1:1



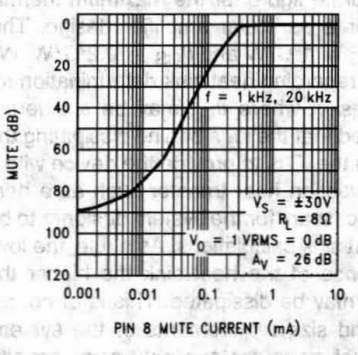
IMD 60 Hz, 7 kHz 1:1



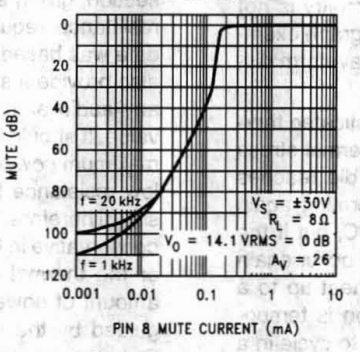
IMD 60 Hz, 7 kHz, 1:1



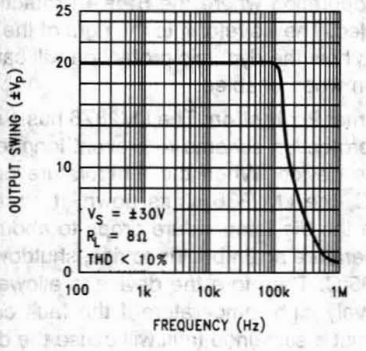
Mute Attenuation vs Mute Current



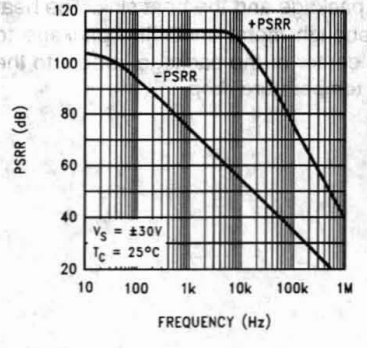
Mute Attenuation vs Mute Current



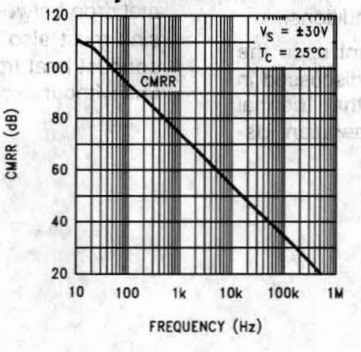
Large Signal Response



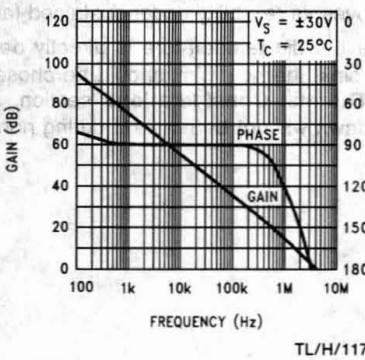
Power Supply Rejection Ratio



Common-Mode Rejection Ratio



Open Loop Frequency Response



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Application Information

GENERAL FEATURES

Mute Function: The muting function of the LM2876 allows the user to mute the music going into the amplifier by drawing less than 0.5 mA out of pin 8 of the device. This is accomplished as shown in the Typical Application Circuit where the resistor R_M is chosen with reference to your negative supply voltage and is used in conjuction with a switch. The switch (when opened) cuts off the current flow from pin 8 to V^-, thus placing the LM2876 into mute mode. Refer to the Mute Attenuation vs Mute Current curves in the **Typical Performance Characteristics** section for values of attenuation per current out of pin 8. The resistance R_M is calculated by the following equation:

$$R_M\,(|V_{EE}| - 2.6V)/I8$$

where $I8 \geq 0.5$ mA.

Under-Voltage Protection: Upon system power-up the under-voltage protection circuitry allows the power supplies and their corresponding caps to come up close to their full values before turning on the LM2876 such that no DC output spikes occur. Upon turn-off, the output of the LM2876 is brought to ground before the power supplies such that no transients occur at power-down.

Over-Voltage Protection: The LM2876 contains overvoltage protection circuitry that limits the output current to approximately 4Apeak while also providing voltage clamping, though not through internal clamping diodes. The clamping effect is quite the same, however, the output transistors are designed to work alternately by sinking large current spikes.

SPiKe Protection: The LM2876 is protected from instantaneous peak-temperature stressing by the power transistor array. The Safe Operating Area graph in the **Typical Performance Characteristics** section shows the area of device operation where the **SPiKe** Protection Circuitry is not enabled. The waveform to the right of the SOA graph exemplifies how the dynamic protection will cause waveform distortion when enabled.

Thermal Protection: The LM2876 has a sophisticated thermal protection scheme to prevent long-term thermal stress to the device. When the temperature on the die reaches 165°C, the LM2876 shuts down. It starts operating again when the die temperature drops to about 155°C, but if the temperature again begins to rise, shutdown will occur again at 165°C. Therefore the device is allowed to heat up to a relatively high temperature if the fault condition is temporary, but a sustained fault will cause the device to cycle in a Schmitt Trigger fashion between the thermal shutdown temperature limits of 165°C and 155°C. This greatly reduces the stress imposed on the IC by thermal cycling, which in turn improves its reliability under sustained fault conditions.

Since the die temperature is directly dependent upon the heat sink, the heat sink should be chosen as discussed in the **Thermal Considerations** section, such that thermal shutdown will not be reached during normal operation. Using the best heat sink possible within the cost and space constraints of the system will improve the long-term reliability of any power semiconductor device.

THERMAL CONSIDERATIONS

Heat Sinking

The choice of a heat sink for a high-power audio amplifier is made entirely to keep the die temperature at a level such that the thermal protection circuitry does not operate under normal circumstances. The heat sink should be chosen to dissipate the maximum IC power for a given supply voltage and rated load.

With high-power pulses of longer duration than 100 ms, the case temperature will heat up drastically without the use of a heat sink. Therefore the case temperature, as measured at the center of the package bottom, is entirely dependent on heat sink design and the mounting of the IC to the heat sink. For the design of a heat sink for your audio amplifier application refer to the **Determining The Correct Heat Sink** section.

Since a semiconductor manufacturer has no control over which heat sink is used in a particular amplifier design, we can only inform the system designer of the parameters and the method needed in the determination of a heat sink. With this in mind, the system designer must choose his supply voltages, a rated load, a desired output power level, and know the ambient temperature surrounding the device. These parameters are in addition to knowing the maximum junction temperature and the thermal resistance of the IC, both of which are provided by National Semiconductor.

As a benefit to the system designer we have provided Maximum Power Dissipation vs Supply Voltages curves for various loads in the **Typical Performance Characteristics** section, giving an accurate figure for the maximum thermal resistance required for a particular amplifier design. This data was based on $\theta_{JC} = 1°C/W$ and $\theta_{CS} = 0.2°C/W$. We also provide a section regarding heat sink determination for any audio amplifier design where θ_{CS} may be a different value. It should be noted that the idea behind dissipating the maximum power within the IC is to provide the device with a low resistance to convection heat transfer such as a heat sink. Therefore, it is necessary for the system designer to be conservative in his heat sink calculations. As a rule, the lower the thermal resistance of the heat sink the higher the amount of power that may be dissipated. This is of course guided by the cost and size requirements of the system. Convection cooling heat sinks are available commercially, and their manufacturers should be consulted for ratings.

Proper mounting of the IC is required to minimize the thermal drop between the package and the heat sink. The heat sink must also have enough metal under the package to conduct heat from the center of the package bottom to the fins without excessive temperature drop.

Application Information (Continued)

A thermal grease such as Wakefield type 120 or Thermalloy Thermacote should be used when mounting the package to the heat sink. Without this compound, thermal resistance will be no better than 0.5°C/W, and probably much worse. With the compound, thermal resistance will be 0.2°C/W or less, assuming under 0.005 inch combined flatness runout for the package and heat sink. Proper torquing of the mounting bolts is important and can be determined from heat sink manufacturer's specification sheets.

Should it be necessary to isolate V^- from the heat sink, an insulating washer is required. Hard washers like beryluum oxide, anodized aluminum and mica require the use of thermal compound on both faces. Two-mil mica washers are most common, giving about 0.4°C/W interface resistance with the compound.

Silicone-rubber washers are also available. A 0.5°C/W thermal resistance is claimed without thermal compound. Experience has shown that these rubber washers deteriorate and must be replaced should the IC be dismounted.

Determining Maximum Power Dissipation

Power dissipation within the integrated circuit package is a very important parameter requiring a thorough understanding if optimum power output is to be obtained. An incorrect maximum power dissipation (P_D) calculation may result in inadequate heat sinking, causing thermal shutdown circuitry to operate and limit the output power.

The following equations can be used to acccurately calculate the maximum and average integrated circuit power dissipation for your amplifier design, given the supply voltage, rated load, and output power. These equations can be directly applied to the Power Dissipation vs Output Power curves in the **Typical Performance Characteristics** section.

Equation (1) exemplifies the maximum power dissipation of the IC and equations (2) and (3) exemplify the average IC power dissipation expressed in different forms.

$$P_{DMAX} = V_{CC}^2/2\pi^2R_L \quad (1)$$

where V_{CC} is the total supply voltage

$$P_{DAVE} = (V_{Opk}/R_L)[V_{CC}/\pi - V_{Opk}/2] \quad (2)$$

where V_{CC} is the total supply voltage and $V_{Opk} = V_{CC}/\pi$

$$P_{DAVE} = V_{CC}\,V_{Opk}/\pi R_L - V_{Opk}^2/2R_L \quad (3)$$

where V_{CC} is the total supply voltage.

Determining the Correct Heat Sink

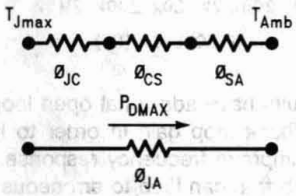
Once the maximum IC power dissipation is known for a given supply voltage, rated load, and the desired rated output power the maximum thermal resistance (in °C/W) of a heat sink can be calculated. This calculation is made using equation (4) and is based on the fact that thermal heat flow parameters are analogous to electrical current flow properties.

It is also known that typically the thermal resistance, θ_{JC} (junction to case), of the LM2876 is 1°C/W and that using Thermalloy Thermacote thermal compound provides a thermal resistance, θ_{CS} (case to heat sink), of about 0.2°C/W as explained in the **Heat Sinking** section.

Referring to the figure below, it is seen that the thermal resistance from the die (junction) to the outside air (ambient) is a combination of three thermal resistances, two of which are known, θ_{JC} and θ_{CS}. Since convection heat flow (power dissipation) is analogous to current flow, thermal resistance is analogous to electrical resistance, and temperature drops are analogous to voltage drops, the power dissipation out of the LM2876 is equal to the following:

$$P_{DMAX} = (T_{Jmax} - T_{Amb})/\theta_{JA}$$

where $\theta_{JA} = \theta_{JC} + \theta_{CS} + \theta_{SA}$



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But since we know P_{DMAX}, θ_{JC}, and θ_{SC} for the application and we are looking for θ_{SA}, we have the following:

$$\theta_{SA} = [(T_{Jmax} - T_{Amb}) - P_{DMAX}(\theta_{JC} + \theta_{CS})]/P_{DMAX} \quad (4)$$

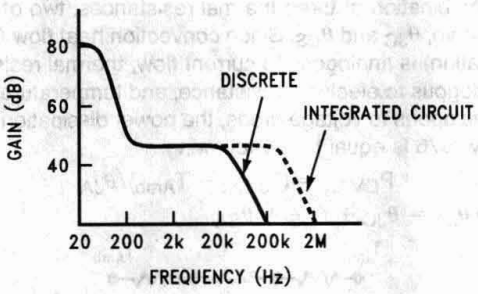
Again it must be noted that the value of θ_{SA} is dependent upon the system designer's amplifier application and its corresponding parameters as described previously. If the ambient temperature that the audio amplifier is to be working under is higher than the normal 25°C, then the thermal resistance for the heat sink, given all other things are equal, will need to be smaller.

Equations (1) and (4) are the only equations needed in the determination of the maximum heat sink thermal resistance. This is of course given that the system designer knows the required supply voltages to drive his rated load at a particular power output level and the parameters provided by the semiconductor manufacturer. These parameters are the junction to case thermal resistance, θ_{JC}, $T_{Jmax} = 150°C$, and the recommended Thermalloy Thermacote thermal compound resistance, θ_{CS}.

Application Information (Continued)

SIGNAL-TO-NOISE RATIO

In the measurement of the signal-to-noise ratio, misinterpretations of the numbers actually measured are common. One amplifier may sound much quieter than another, but due to improper testing techniques, they appear equal in measurements. This is often the case when comparing integrated circuit designs to discrete amplifier designs. Discrete transistor amps often "run out of gain" at high frequencies and therefore have small bandwidths to noise as indicated below.



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Integrated circuits have additional open loop gain allowing additional feedback loop gain in order to lower harmonic distortion and improve frequency response. It is this additional bandwidth that can lead to erroneous signal-to-noise measurements if not considered during the measurement process. In the typical example above, the difference in bandwidth appears small on a log scale but the factor of 10 in bandwidth, (200 kHz to 2 MHz) can result in a 10 dB theoretical difference in the signal-to-noise ratio (white noise is proportional to the square root of the bandwidth in a system).

In comparing audio amplifiers it is necessary to measure the magnitude of noise in the audible bandwidth by using a "weighting" filter.[1] A "weighting" filter alters the frequency response in order to compensate for the average human ear's sensitivity to the frequency spectra. The weighting filters at the same time provide the bandwidth limiting as discussed in the previous paragraph.

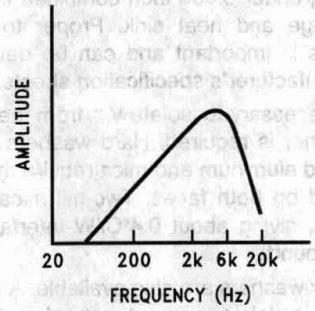
In addition to noise filtering, differing meter types give different noise readings. Meter responses include:

1. RMS reading,
2. average responding,
3. peak reading, and
4. quasi peak reading.

Although theoretical noise analysis is derived using true RMS based calculations, most actual measurements are taken with ARM (Average Responding Meter) test equipment.

Reference 1: CCIR/ARM: *A Practical Noise Measurement Method;* by Ray Dolby, David Robinson and Kenneth Gundry, AES Preprint No. 1353 (F-3).

Typical signal-to-noise figures are listed for an A-weighted filter which is commonly used in the measurement of noise. The shape of all weighting filters is similar, with the peak of the curve usually occurring in the 3 kHz–7 kHz region as shown below.



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SUPPLY BYPASSING

The LM2876 has excellent power supply rejection and does not require a regulated supply. However, to eliminate possible oscillations all op amps and power op amps should have their supply leads bypassed with low-inductance capacitors having short leads and located close to the package terminals. Inadequate power supply bypassing will manifest itself by a low frequency oscillation known as "motorboating" or by high frequency instabilities. These instabilities can be eliminated through multiple bypassing utilizing a large tantalum or electrolytic capacitor (10 μF or larger) which is used to absorb low frequency variations and a small ceramic capacitor (0.1 μF) to prevent any high frequency feedback through the power supply lines.

If adequate bypassing is not provided the current in the supply leads which is a rectified component of the load current may be fed back into internal circuitry. This signal causes low distortion at high frequencies requiring that the supplies be bypassed at the package terminals with an electrolytic capacitor of 470 μF or more.

LEAD INDUCTANCE

Power op amps are sensitive to inductance in the output lead, particularly with heavy capacitive loading. Feedback to the input should be taken directly from the output terminal, minimizing common inductance with the load.

Lead inductance can also cause voltage surges on the supplies. With long leads to the power supply, energy is stored in the lead inductance when the output is shorted. This energy can be dumped back into the supply bypass capacitors when the short is removed. The magnitude of this transient is reduced by increasing the size of the bypass capacitor near the IC. With at least a 20 μF local bypass, these voltage surges are important only if the lead length exceeds a couple feet ($>$ 1 μH lead inductance). Twisting together the supply and ground leads minimizes the effect.

Application Information (Continued)

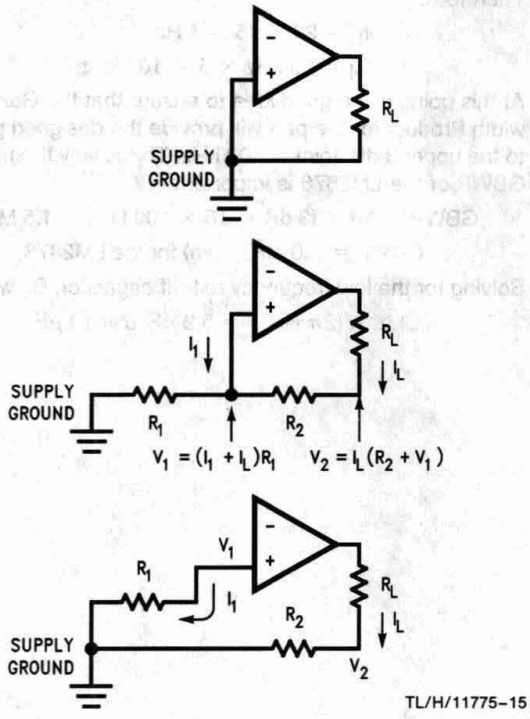
LAYOUT, GROUND LOOPS AND STABILITY

The LM2876 is designed to be stable when operated at a closed-loop gain of 10 or greater, but as with any other high-current amplifier, the LM2876 can be made to oscillate under certain conditions. These usually involve printed circuit board layout or output/input coupling.

When designing a layout, it is important to return the load ground, the output compensation ground, and the low level (feedback and input) grounds to the circuit board common ground point through separate paths. Otherwise, large currents flowing along a ground conductor will generate voltages on the conductor which can effectively act as signals at the input, resulting in high frequency oscillation or excessive distortion. It is advisable to keep the output compensation components and the 0.1 μF supply decoupling capacitors as close as possible to the LM2876 to reduce the effects of PCB trace resistance and inductance. For the same reason, the ground return paths should be as short as possible.

In general, with fast, high-current circuitry, all sorts of problems can arise from improper grounding which again can be avoided by returning all grounds separately to a common point. Without isolating the ground signals and returning the grounds to a common point, ground loops may occur.

"Ground Loop" is the term used to describe situations occurring in ground systems where a difference in potential exists between two ground points. Ideally a ground is a ground, but unfortunately, in order for this to be true, ground conductors with zero resistance are necessary. Since real world ground leads possess finite resistance, currents running through them will cause finite voltage drops to exist. If two ground return lines tie into the same path at different points there will be a voltage drop between them. The first figure below shows a common ground example where the positive input ground and the load ground are returned to the supply ground point via the same wire. The addition of the finite wire resistance, R_2, results in a voltage difference between the two points as shown below.



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The load current I_L will be much larger than input bias current I_I, thus V_1 will follow the output voltage directly, i.e. in phase. Therefore the voltage appearing at the non-inverting input is effectively positive feedback and the circuit may oscillate. If there were only one device to worry about then the values of R_1 and R_2 would probably be small enough to be ignored; however, several devices normally comprise a total system. Any ground return of a separate device, whose output is in phase, can feedback in a similar manner and cause instabilities. Out of phase ground loops also are troublesome, causing unexpected gain and phase errors.

The solution to most ground loop problems is to always use a single-point ground system, although this is sometimes impractical. The third figure below is an example of a single-point ground system.

The single-point ground concept should be applied rigorously to all components and all circuits when possible. Violations of single-point grounding are most common among printed circuit board designs, since the circuit is surrounded by large ground areas which invite the temptation to run a device to the closest ground spot. As a final rule, make all ground returns low resistance and low inductance by using large wire and wide traces.

Occasionally, current in the output leads (which function as antennas) can be coupled through the air to the amplifier input, resulting in high-frequency oscillation. This normally happens when the source impedance is high or the input leads are long. The problem can be eliminated by placing a small capacitor, C_C, (on the order of 50 pF to 500 pF) across the LM2876 input terminals. Refer to the **External Components Description** section relating to component interaction with C_f.

REACTIVE LOADING

It is hard for most power amplifiers to drive highly capacitive loads very effectively and normally results in oscillations or ringing on the square wave response. If the output of the LM2876 is connected directly to a capacitor with no series resistance, the square wave response will exhibit ringing if the capacitance is greater than about 0.2 μF. If highly capacitive loads are expected due to long speaker cables, a method commonly employed to protect amplifiers from low impedances at high frequencies is to couple to the load through a 10Ω resistor in parallel with a 0.7 μH inductor. The inductor-resistor combination as shown in the **Typical Application Circuit** isolates the feedback amplifier from the load by providing high output impedance at high frequencies thus allowing the 10Ω resistor to decouple the capacitive load and reduce the Q of the series resonant circuit. The LR combination also provides low output impedance at low frequencies thus shorting out the 10Ω resistor and allowing the amplifier to drive the series RC load (large capacitive load due to long speaker cables) directly.

Application Information (Continued)

GENERALIZED AUDIO POWER AMPLIFIER DESIGN

The system designer usually knows some of the following parameters when starting an audio amplifier design:

Desired Power Output	Input Level
Input Impedance	Load Impedance
Maximum Supply Voltage	Bandwidth

The power output and load impedance determine the power supply requirements, however, depending upon the application some system designers may be limited to certain maximum supply voltages. If the designer does have a power supply limitation, he should choose a practical load impedance which would allow the amplifier to provide the desired output power, keeping in mind the current limiting capabilities of the device. In any case, the output signal swing and current are found from (where P_O is the average output power):

$$V_{opeak} = \sqrt{2\, R_L\, P_O} \quad (1)$$

$$I_{opeak} = \sqrt{(2\, P_O)/R_L} \quad (2)$$

To determine the maximum supply voltage the following parameters must be considered. Add the dropout voltage (4V for LM2876) to the peak output swing, V_{opeak}, to get the supply rail value (i.e. $\pm$ (V_{opeak} + Vod) at a current of I_{opeak}). The regulation of the supply determines the unloaded voltage, usually about 15% higher. Supply voltage will also rise 10% during high line conditions. Therefore, the maximum supply voltage is obtained from the following equation:

$$\text{Max. supplies} \approx \pm\, (V_{opeak} + \text{Vod})(1 + \text{regulation})(1.1) \quad (3)$$

The input sensitivity and the output power specs determine the minimum required gain as depicted below:

$$A_V \geq (\sqrt{P_O\, R_L})/(V_{IN}) = V_{orms}/V_{inrms} \quad (4)$$

Normally the gain is set between 20 and 200; for a 40W, 8Ω audio amplifier this results in a sensitivity of 894 mV and 89 mV, respectively. Although higher gain amplifiers provide greater output power and dynamic headroom capabilities, there are certain shortcomings that go along with the so called "gain." The input referred noise floor is increased and hence the SNR is worse. With the increase in gain, there is also a reduction of the power bandwidth which results in a decrease in feedback thus not allowing the amplifier to respond quickly enough to nonlinearities. This decreased ability to respond to nonlinearities increases the THD + N specification.

The desired input impedance is set by R_{IN}. Very high values can cause board layout problems and DC offsets at the output. The value for the feedback resistance, R_{f1}, should be chosen to be a relatively large value (10 kΩ–100 kΩ), and the other feedback resistance, Ri, is calculated using standard op amp configuration gain equations. Most audio amplifiers are designed from the non-inverting amplifier configuration.

DESIGN A 25W/8Ω AUDIO AMPLIFIER

Given:

Power Output	25W
Load Impedance	8Ω
Input Level	1V(max)
Input Impedance	100 kΩ
Bandwidth	20 Hz–20 kHz ± 0.25 dB

Equations (1) and (2) give:

25W/8Ω $V_{opeak} = 20.0V$ $I_{opeak} = 2.5A$

Therefore the supply required is: ±24.0V @ 2.5A

With 15% regulation and high line the final supply voltage is ±30.36V using equation (3). At this point it is a good idea to check the Power Output vs Supply Voltage to ensure that the required output power is obtainable from the device while maintaining low THD + N. It is also good to check the Power Dissipation vs Supply Voltage to ensure that the device can handle the internal power dissipation. At the same time designing in a relatively practical sized heat sink with a low thermal resistance is also important. Refer to **Typical Performance Characteristics** graphs and the **Thermal Considerations** section for more information.

The minimum gain from equation (4) is: $A_V \geq 14$

We select a gain of 15 (Non-Inverting Amplifier); resulting in a sensitivity of 942.8 mV.

Letting R_{IN} equal 100 kΩ gives the required input impedance, however, this would eliminate the "volume control" unless an additional input impedance was placed in series with the 10 kΩ potentiometer that is depicted in *Figure 1*. Adding the additional 100 kΩ resistor would ensure the minumum required input impedance.

For low DC offsets at the output we let $R_{f1} = 100\ k\Omega$. Solving for Ri (Non-Inverting Amplifier) gives the following:

$Ri = R_{f1}/(A_V - 1) = 100k/(15 - 1) = 7.1\ k\Omega$; use 6.8 kΩ

The bandwidth requirement must be stated as a pole, i.e., the 3 dB frequency. Five times away from a pole gives 0.17 dB down, which is better than the required 0.25 dB. Therefore:

$$f_L = 20\ Hz/5 = 4\ Hz$$

$$f_H = 20\ kHz \times 5 = 100\ kHz$$

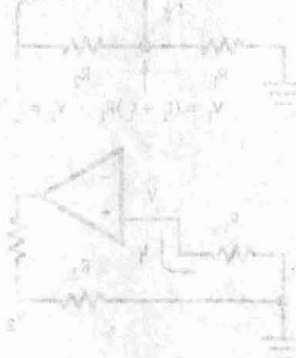
At this point, it is a good idea to ensure that the Gain-Bandwidth Product for the part will provide the designed gain out to the upper 3 dB point of 100 kHz. This is why the minimum GBWP of the LM2876 is important.

$$GBWP \geq A_V \times f3\ dB = 15 \times 100\ kHz = 1.5\ MHz$$

GBWP = 2.0 MHz (min) for the LM2876

Solving for the low frequency roll-off capacitor, Ci, we have:

$$Ci \geq 1/(2\pi\, Ri\, f_L) = 5.9\ \mu F;\ \text{use } 10\ \mu F.$$



Definition of Terms

Input Offset Voltage: The absolute value of the voltage which must be applied between the input terminals through two equal resistances to obtain zero output voltage and current.

Input Bias Current: The absolute value of the average of the two input currents with the output voltage and current at zero.

Input Offset Current: The absolute value of the difference in the two input currents with the output voltage and current at zero.

Input Common-Mode Voltage Range (or Input Voltage Range): The range of voltages on the input terminals for which the amplifier is operational. Note that the specifications are not guaranteed over the full common-mode voltage range unless specifically stated.

Common-Mode Rejection: The ratio of the input common-mode voltage range to the peak-to-peak change in input offset voltage over this range.

Power Supply Rejection: The ratio of the change in input offset voltage to the change in power supply voltages producing it.

Quiescent Supply Current: The current required from the power supply to operate the amplifier with no load and the output voltage and current at zero.

Slew Rate: The internally limited rate of change in output voltage with a large amplitude step function applied to the input.

Class B Amplifier: The most common type of audio power amplifier that consists of two output devices each of which conducts for 180° of the input cycle. The LM2876 is a Quasi − AB type amplifier.

Crossover Distortion: Distortion caused in the output stage of a class B amplifier. It can result from inadequate bias current providing a dead zone where the output does not respond to the input as the input cycle goes through its zero crossing point. Also for ICs an inadequate frequency response of the output PNP device can cause a turn-on delay giving crossover distortion on the negative going transition through zero crossing at the higher audio frequencies.

THD + N: Total Harmonic Distortion plus Noise refers to the measurement technique in which the fundamental component is removed by a bandreject (notch) filter and all remaining energy is measured including harmonics and noise.

Signal-to-Noise Ratio: The ratio of a system's output signal level to the system's output noise level obtained in the absence of a signal. The output reference signal is either specified or measured at a specified distortion level.

Continuous Average Output Power: The minimum sine wave continuous average power output in watts (or dBW) that can be delivered into the rated load, over the rated bandwidth, at the rated maximum total harmonic distortion.

Music Power: A measurement of the peak output power capability of an amplifier with either a signal duration sufficiently short that the amplifier power supply does not sag during the measurement, or when high quality external power supplies are used. This measurement (an IHF standard) assumes that with normal music program material the amplifier power supplies will sag insignificantly.

Peak Power: Most commonly referred to as the power output capability of an amplifier that can be delivered to the load; specified by the part's maximum voltage swing.

Headroom: The margin between an actual signal operating level (usually the power rating of the amplifier with particular supply voltages, a rated load value, and a rated THD + N figure) and the level just before clipping distortion occurs, expressed in decibels.

Large Signal Voltage Gain: The ratio of the output voltage swing to the differential input voltage required to drive the output from zero to either swing limit. The output swing limit is the supply voltage less a specified quasi-saturation voltage. A pulse of short enough duration to minimize thermal effects is used as a measurement signal.

Output-Current Limit: The output current with a fixed output voltage and a large input overdrive. The limiting current drops with time once **SPiKe** protection circuitry is activated.

Output Saturation Threshold (Clipping Point): The output swing limit for a specified input drive beyond that required for zero output. It is measured with respect to the supply to which the output is swinging.

Output Resistance: The ratio of the change in output voltage to the change in output current with the output around zero.

Power Dissipation Rating: The power that can be dissipated for a specified time interval without activating the protection circuitry. For time intervals in excess of 100 ms, dissipation capability is determined by heat sinking of the IC package rather than by the IC itself.

Thermal Resistance: The peak, junction-temperature rise, per unit of internal power dissipation (units in °C/W), above the case temperature as measured at the center of the package bottom.

The DC thermal resistance applies when one output transistor is operating continuously. The AC thermal resistance applies with the output transistors conducting alternately at a high enough frequency that the peak capability of neither transistor is exceeded.

Power Bandwidth: The power bandwidth of an audio amplifier is the frequency range over which the amplifier voltage gain does not fall below 0.707 of the flat band voltage gain specified for a given load and output power.

Power bandwidth also can be measured by the frequencies at which a specified level of distortion is obtained while the amplifier delivers a power output 3 dB below the rated output. For example, an amplifier rated at 60W with ≤ 0.25% THD + N, would make its power bandwidth measured as the difference between the upper and lower frequencies at which 0.25% distortion was obtained while the amplifier was delivering 30W.

Gain-Bandwidth Product: The Gain-Bandwidth Product is a way of predicting the high-frequency usefulness of an op amp. The Gain-Bandwidth Product is sometimes called the unity-gain frequency or unity-gain cross frequency because the open-loop gain characteristic passes through or crosses unity gain at this frequency. Simply, we have the following relationship: $A_{CL1} \times f_1 = A_{CL2} \times f_2$

Assuming that at unity-gain ($A_{CL1} = 1$ or (0 dB)) fu = fi = GBWP, then we have the following: GBWP = $A_{CL2} \times f_2$

This says that once fu (GBWP) is known for an amplifier, then the open-loop gain can be found at any frequency. This is also an excellent equation to determine the 3 dB point of a closed-loop gain, assuming that you know the GBWP of the device. Refer to the diagram on the following page.

Definition of Terms (Continued)

Biamplification: The technique of splitting the audio frequency spectrum into two sections and using individual power amplifiers to drive a separate woofer and tweeter. Crossover frequencies for the amplifiers usually vary between 500 Hz and 1600 Hz. "Biamping" has the advantages of allowing smaller power amps to produce a given sound pressure level and reducing distortion effects produsedby overdrive in one part of the frequency spectrum affecting the other part.

C.C.I.R./A.R.M.:

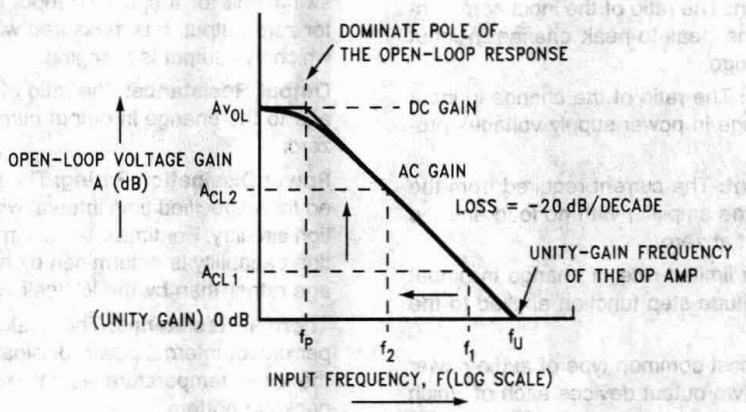
Literally: International Radio Consultative Committee
Average Responding Meter

This refers to a weighted noise measurement for a Dolby B type noise reduction system. A filter characteristic is used that gives a closer correlation of the measurement with the subjective annoyance of noise to the ear. Measurements made with this filter cannot necessarily be related to unweighted noise measurements by some fixed conversion factor since the answers obtained will depend on the spectrum of the noise source.

S.P.L.: Sound Pressure Level—usually measured with a microphone/meter combination calibrated to a pressure level of 0.0002 μBars (approximately the threshold hearing level).

$$S.P.L. = 20 \text{ Log } 10P/0.0002 \text{ dB}$$

where P is the R.M.S. sound pressure in microbars.
(1 Bar = 1 atmosphere = 14.5 lb/in^2 = 194 dB S.P.L.).



TL/H/11775–16

National Semiconductor

LM2877 Dual 4W Audio Power Amplifier

General Description

The LM2877 is a monolithic dual power amplifier designed to deliver 4W/channel continuous into 8Ω loads. The LM2877 is designed to operate with a low number of external components, and still provide flexibility for use in stereo phonographs, tape recorders and AM-FM stereo receivers, etc. Each power amplifier is biased from a common internal regulator to provide high power supply rejection and output Q point centering. The LM2877 is internally compensated for all gains greater than 10, and comes in an 11-lead single-in-line package.

Features

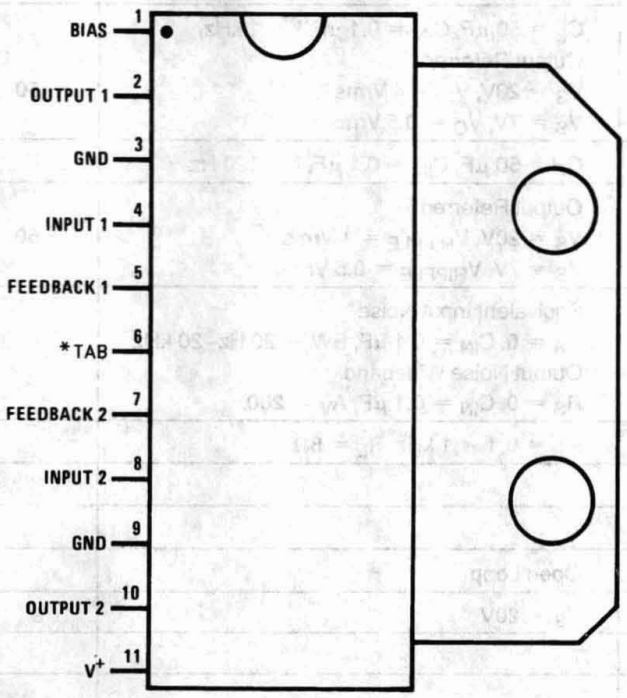
- 4W/channel
- −68 dB ripple rejection, output referred
- −70 dB channel separation, output referred
- Wide supply range, 6-24V
- Very low cross-over distortion
- Low audio band noise
- AC short circuit protected
- Internal thermal shutdown

Applications

- Multi-channel audio systems
- Stereo phonographs
- Tape recorders and players
- AM-FM radio receivers
- Servo amplifiers
- Intercom systems
- Automotive products

Connection Diagram

(Single-In-Line Package)



TL/H/7933–1

Top View

Order Number LM2877P
See NS Package Number P11A

*Pin 6 must be connected to GND.

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	26V
Input Voltage	±0.7V
Operating Temperature	0°C to +70°C
Storage Temperature	−65°C to +150°C
Junction Temperature	150°C
Lead Temperature (Soldering, 10 sec.)	260°C
Thermal Resistance	
θ_{JC}	10°C/W
θ_{JA}	55°C/W

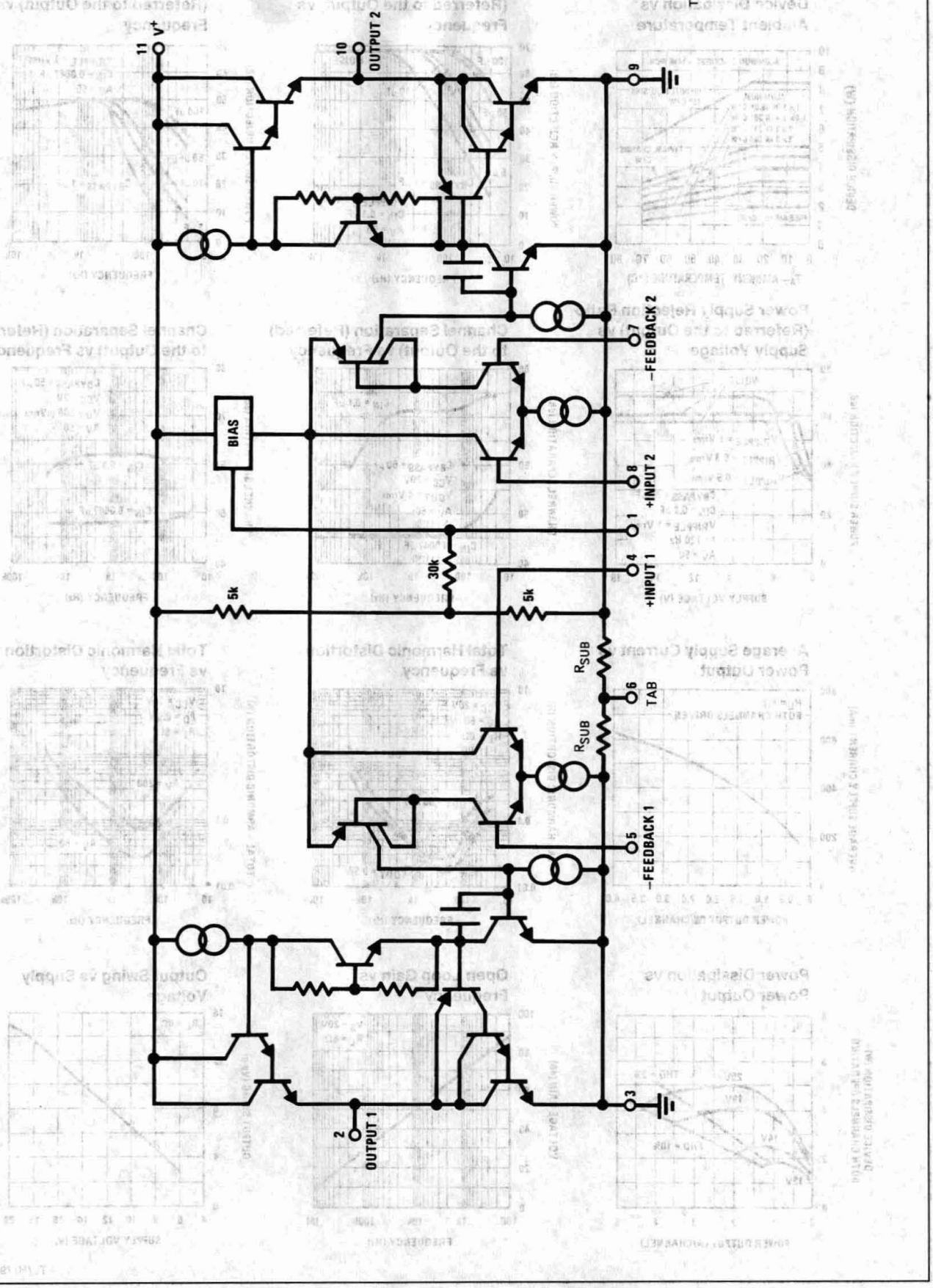
Electrical Characteristics

V_S = 20V, T_{TAB} = 25°C, R_L = 8Ω, A_V = 50 (34 dB) unless otherwise specified.

Parameter	Conditions	Min	Typ	Max	Units
Total Supply Current	P_O = 0W		25	50	mA
Operating Supply Voltage		6		24	V
Output Power/Channel	f = 1 kHz, THD = 10%, T_{TAB} = 25°C				
	V_S = 20V	4.0	4.5		W
	V_S = 18V		3.6		W
	V_S = 12V, R_L = 4Ω	1.5	1.9		W
	V_S = 12V, R_L = 8Ω		1.0		W
Distortion, THD	f = 1 kHz, V_S = 20V				
	P_O = 50 mW/Channel		0.1		%
	P_O = 1W/Channel		0.07	1	%
	P_O = 2W/Channel		0.07		%
	f = 1 kHz, V_S = 12V, R_L = 4Ω				
	P_O = 50 mW/Channel		0.25		%
	P_O = 500 mW/Channel		0.20		%
	P_O = 1W/Channel		0.15	1	%
Output Swing	R_L = 8Ω		V_S−4		V_{p-p}
Channel Separation	C_F = 50 μF, C_{IN} = 0.1 μF, f = 1 kHz, Output Referred				
	V_S = 20V, V_O = 4 Vrms	−50	−70		dB
	V_S = 7V, V_O = 0.5 Vrms		−60		dB
PSRR Power Supply	C_F = 50 μF, C_{IN} = 0.1 μF, f = 120 Hz				
Rejection Ratio	Output Referred				
	V_S = 20V, V_{RIPPLE} = 1 Vrms	−50	−68		dB
	V_S = 7V, V_{RIPPLE} = 0.5 Vrms		−40		dB
Noise	Equivalent Input Noise				
	R_S = 0, C_{IN} = 0.1 μF, BW = 20 Hz–20 kHz		2.5		μV
	Output Noise Wideband				
	R_S = 0, C_{IN} = 0.1 μF, A_V = 200		0.80		mV
Open Loop Gain	R_S = 0, f = 1 kHz, R_L = 8Ω		70		dB
Input Offset Voltage			15		mV
Input Bias Current			50		nA
Input Impedance	Open Loop		4		MΩ
DC Output Level	V_S = 20V	9	10	11	V
Slew Rate			2.0		V/μs
Power Bandwidth			65		kHz
Current Limit			1.0		A

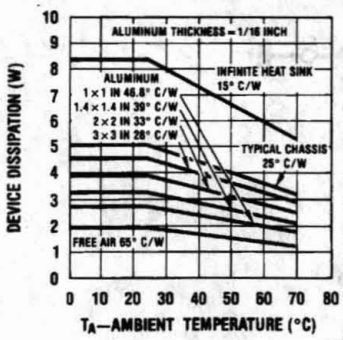
Note 1: For operation at ambient temperature greater than 25°C, the LM2877 must be derated based on a maximum 150°C junction temperature using a thermal resistance which depends upon device mounting techniques.

Equivalent Schematic Diagram

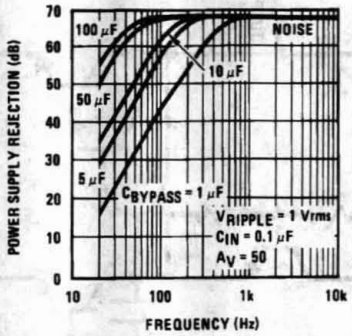


Typical Performance Characteristics

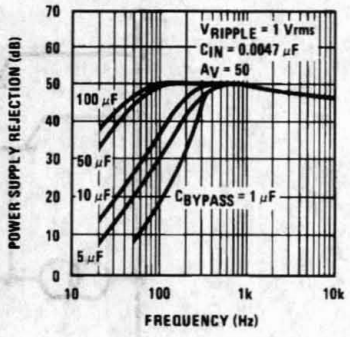
Device Dissipation vs Ambient Temperature



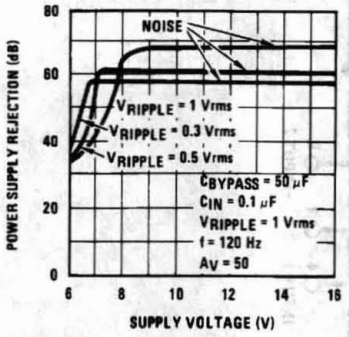
Power Supply Rejection Ratio (Referred to the Output) vs Frequency



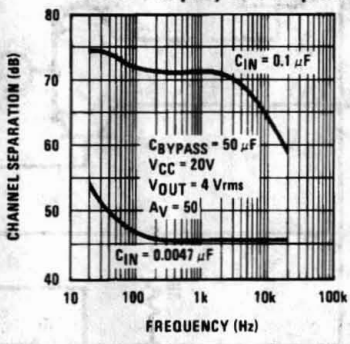
Power Supply Rejection Ratio (Referred to the Output) vs Frequency



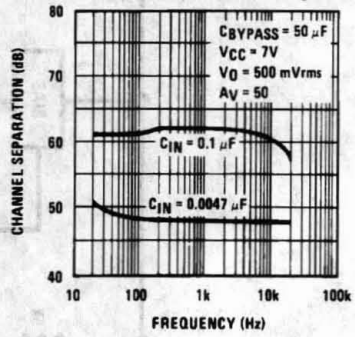
Power Supply Rejection Ratio (Referred to the Output) vs Supply Voltage



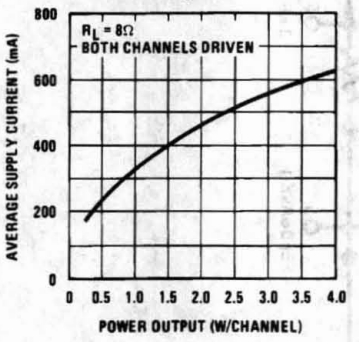
Channel Separation (Referred) to the Output) vs Frequency



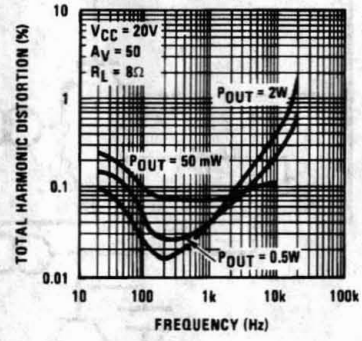
Channel Separation (Referred) to the Output) vs Frequency



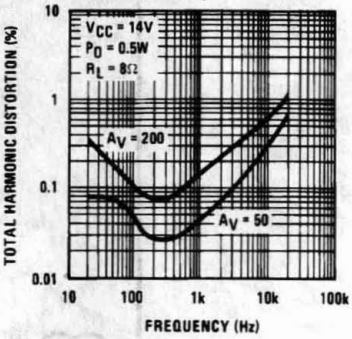
Average Supply Current vs Power Output



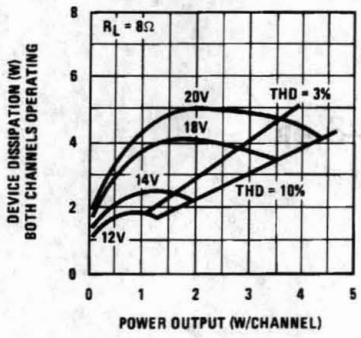
Total Harmonic Distortion vs Frequency



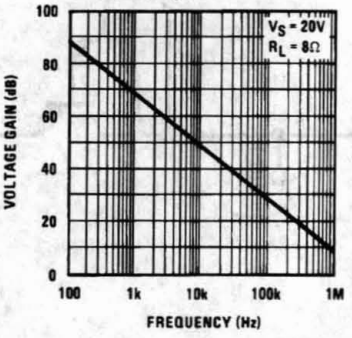
Total Harmonic Distortion vs Frequency



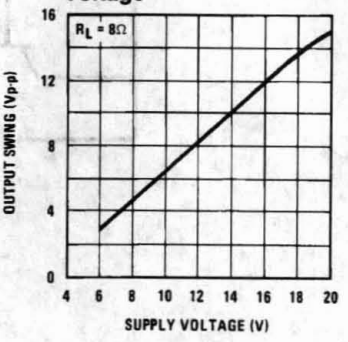
Power Dissipation vs Power Output



Open Loop Gain vs Frequency



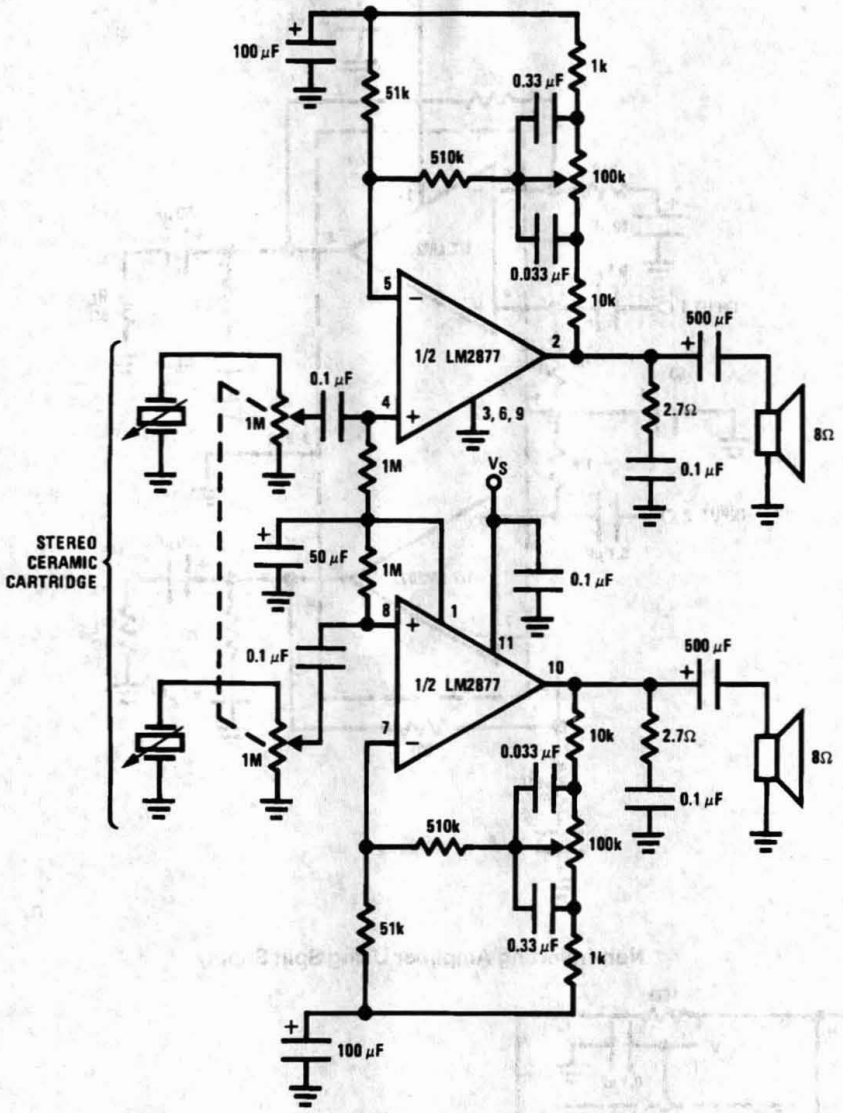
Output Swing vs Supply Voltage



TL/H/7933–3

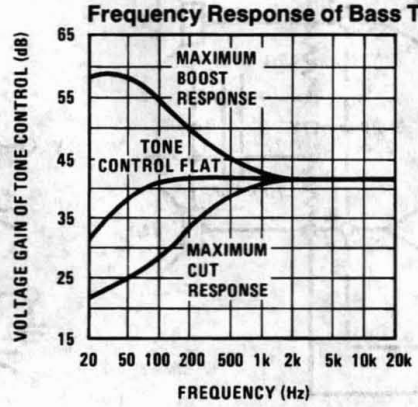
Typical Applications

Stereo Phonograph Amplifier with Bass Tone Control



TL/H/7933–4

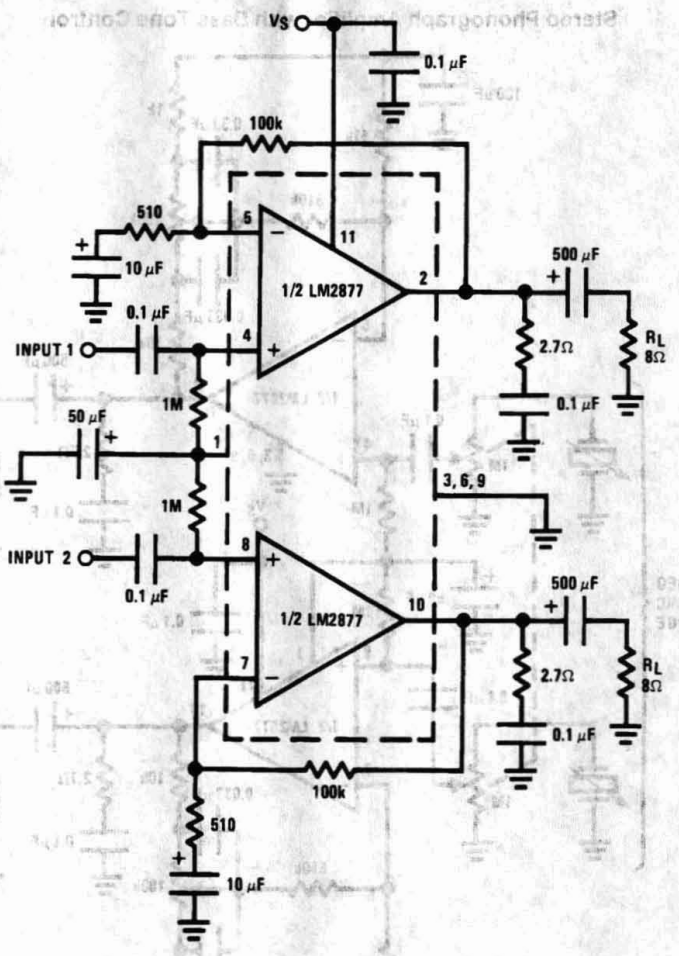
Frequency Response of Bass Tone Control



TL/H/7933–5

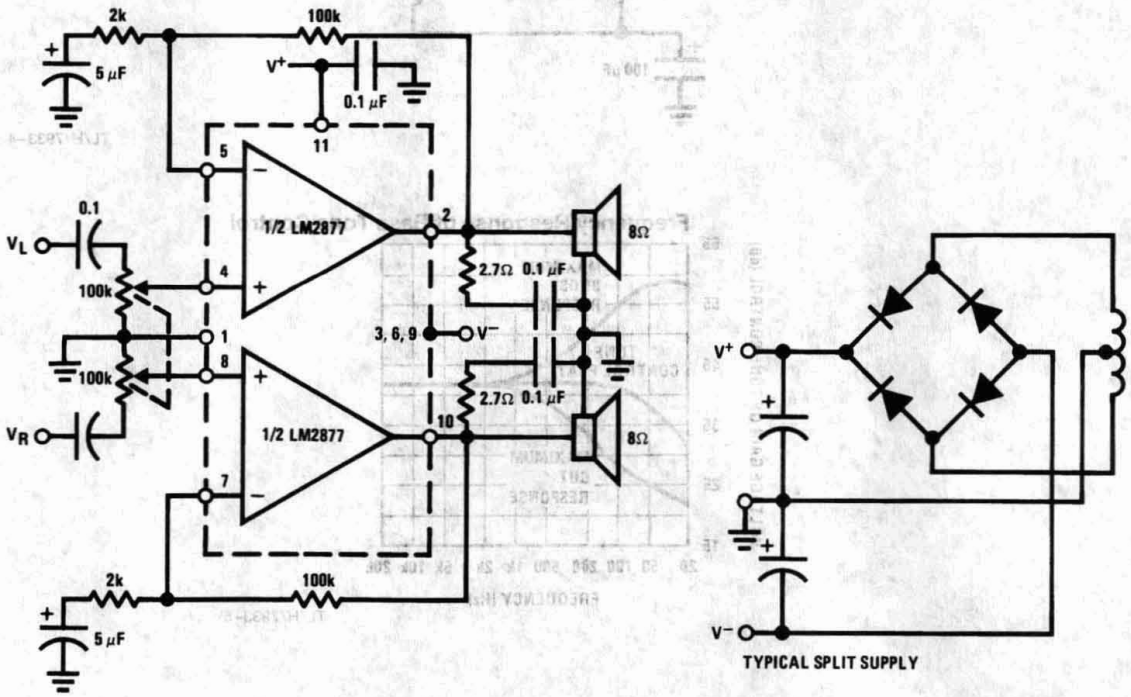
Typical Applications (Continued)

Stereo Amplifier with $A_V = 200$



TL/H/7933–6

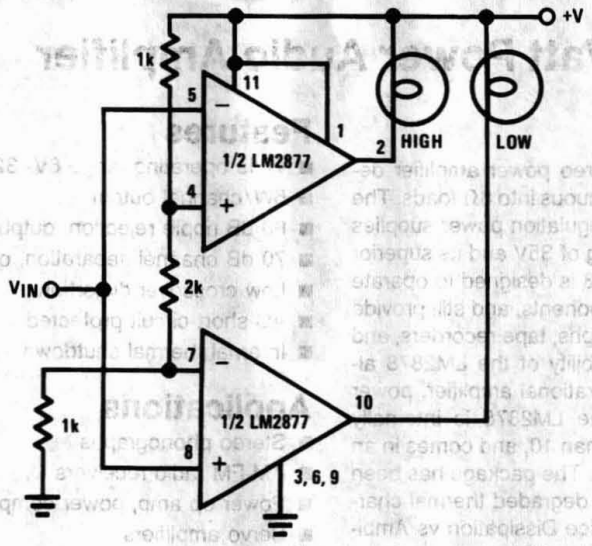
Non-Inverting Amplifier Using Split Supply



TL/H/7933–7

Typical Applications (Continued)

Window Comparator Driving High, Low Lamps



TL/H/7933–8

Truth Table

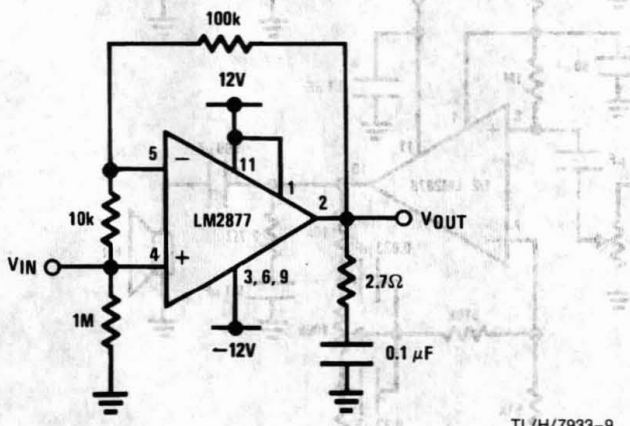
V_{IN}	High	Low
$< 1/4\ V^+$	Off	On
$1/4\ V^+$ to $3/4\ V^+$	Off	Off
$> 3/4\ V^+$	On	Off

Application Hints

The LM2877 is an improved LM377 in typical audio applications. In the LM2877, the internal voltage regulator for the input stage is generated from the voltage on pin 1. Normally, the input common-mode range is within ±0.7V of this pin 1 voltage. Nevertheless, the common-mode range can be increased by externally forcing the voltage on pin 1. One way to do this is to short pin 1 to the positive supply, pin 11.

The only special care required with the LM2877 is to limit the maximum input differential voltage to ±7V. If this differential voltage is exceeded, the input characteristics may change.

Figure 1 shows a power op amp application with $A_V = 1$. The 100k and 10k resistors set a noise gain of 10 and are dictated by amplifier stability. The 10k resistor is bootstrapped by the feedback so the input resistance is dominated by the 1 MΩ resistor.



TL/H/7933–9

FIGURE 1

National Semiconductor

LM2878 Dual 5 Watt Power Audio Amplifier

General Description

The LM2878 is a high voltage stereo power amplifier designed to deliver 5W/channel continuous into 8Ω loads. The amplifier is ideal for use with low regulation power supplies due to the absolute maximum rating of 35V and its superior power supply rejection. The LM2878 is designed to operate with a low number of external components, and still provide flexibility for use in stereo phonographs, tape recorders, and AM-FM stereo receivers. The flexibility of the LM2878 allows it to be used as a power operational amplifier, power comparator or servo amplifier. The LM2878 is internally compensated for all gains greater than 10, and comes in an 11-lead single-in-line package (SIP). The package has been redesigned, resulting in the slightly degraded thermal characteristics shown in the figure Device Dissipation vs Ambient Temperature.

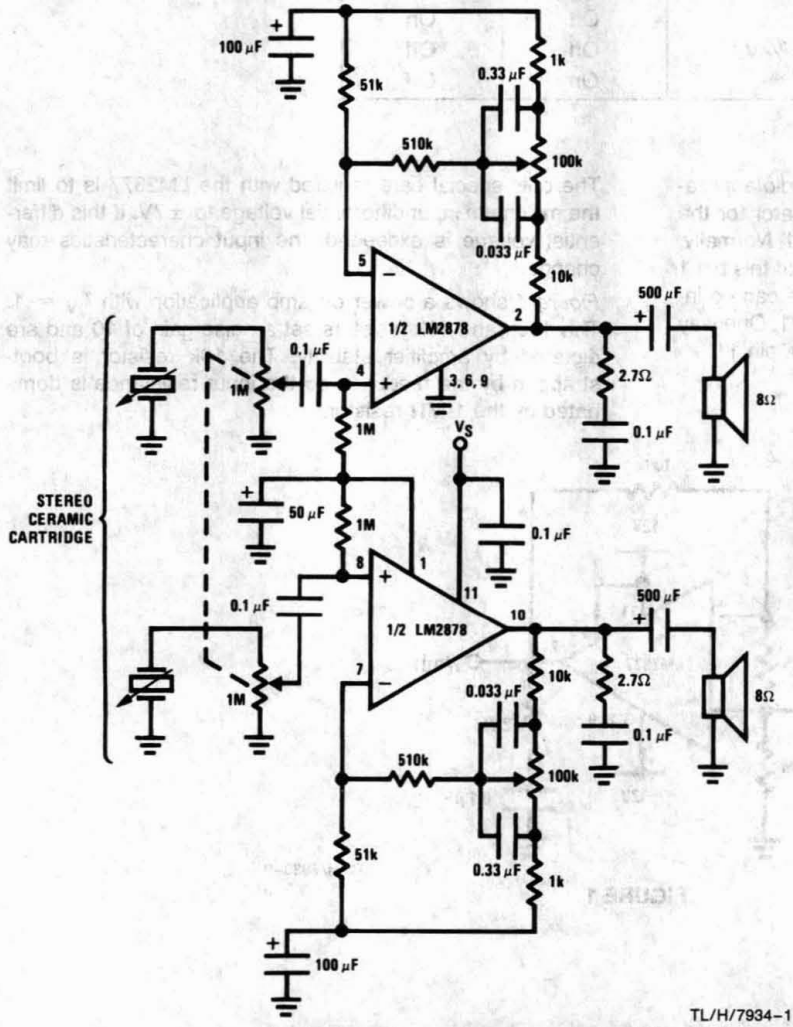
Features

- Wide operating range 6V–32V
- 5W/channel output
- 60 dB ripple rejection, output referred
- 70 dB channel separation, output referred
- Low crossover distortion
- AC short circuit protected
- Internal thermal shutdown

Applications

- Stereo phonographs
- AM-FM radio receivers
- Power op amp, power comparator
- Servo amplifiers

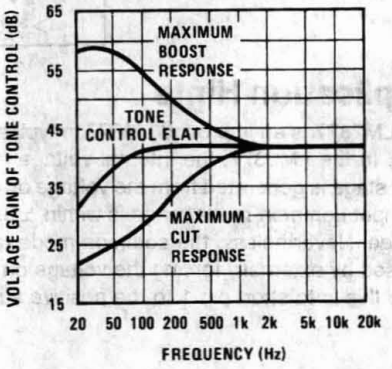
Typical Applications



TL/H/7934–1

FIGURE 1. Stereo Phonograph Amplifier with Bass Tone Control

Frequency Response of Bass Tone Control



TL/H/7934–2

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	35V
Input Voltage (Note 1)	±0.7V
Operating Temperature (Note 2)	0°C to +70°C
Storage Temperature	−65°C to +150°C
Junction Temperature	+150°C
Lead Temperature (Soldering, 10 sec.)	+260°C
Thermal Resistance	
θ_{JC}	10°C/W
θ_{JA}	55°C/W

Electrical Characteristics

V_S = 22V, T_{TAB} = 25°C, R_L = 8Ω, A_V = 50 (34 dB) unless otherwise specified.

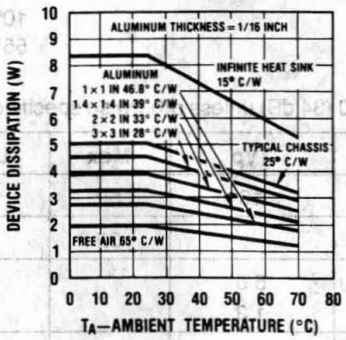
Parameter	Conditions	Min	Typ	Max	Units
Total Supply Current	P_O = 0W		10	50	mA
Operating Supply Voltage		6		32	V
Output Power/Channel	f = 1 kHz, THD = 10%, T_{TAB} = 25°C f = 1 kHz, THD = 10%, V_S = 12V	5	5.5 1.3		W W
Distortion	f = 1 kHz, R_L = 8Ω P_O = 50 mW		0.20		%
	P_O = 0.5W		0.15		%
	P_O = 2W		0.14		%
Output Swing	R_L = 8Ω		V_S − 6V		Vp-p
Channel Separation	C_{BYPASS} = 50 μF, C_{IN} = 0.1 μF f = 1 kHz, Output Referred V_O = 4 Vrms	−50	−70		dB
PSRR Power Supply Rejection Ratio	C_{BYPASS} = 50 μF, C_{IN} = 0.1 μF f = 120 Hz, Output Referred V_{ripple} = 1 Vrms	−50	−60		dB
PSRR Negative Supply	Measured at DC, Input Referred		−60		dB
Common-Mode Range	Split Supplies ±15V, Pin 1 Tied to Pin 11		±13.5		V
Input Offset Voltage			10		mV
Noise	Equivalent Input Noise R_S = 0, C_{IN} = 0.1 μF BW = 20 − 20 kHz		2.5		μV
	CCIR•ARM		3.0		μV
	Output Noise Wideband R_S = 0, C_{IN} = 0.1 μF, A_V = 200		0.8		mV
Open Loop Gain	R_S = 51Ω, f = 1 kHz, R_L = 8Ω		70		dB
Input Bias Current			100		nA
Input Impedance	Open Loop		4		MΩ
DC Output Voltage	V_S = 22V	10	11	12	V
Slew Rate			2		V/μS
Power Bandwidth	3 dB Bandwidth at 2.5W		65		kHz
Current Limit			1.5		A

Note 1: ±0.7V applies to audio applications; for extended range, see Application Hints.

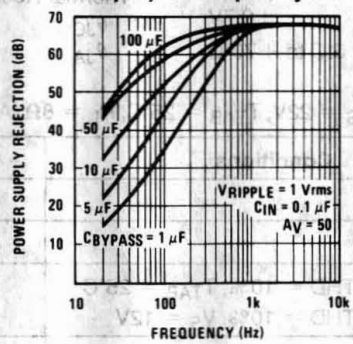
Note 2: For operation at ambient temperature greater than 25°C, the LM2878 must be derated based on a maximum 150°C junction temperature using a thermal resistance which depends upon device mounting techniques.

Typical Performance Characteristics

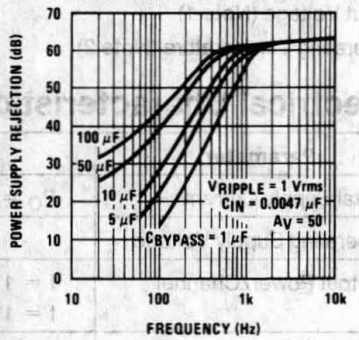
Device Dissipation vs Ambient Temperature



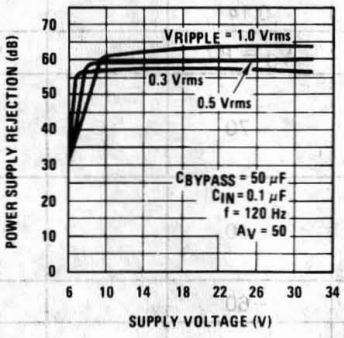
Power Supply Rejection Ratio (Referred to the Output) vs Frequency



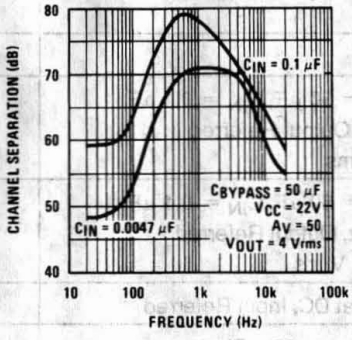
Power Supply Rejection Ratio (Referred to the Output) vs Frequency



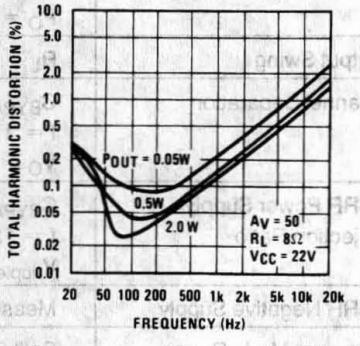
Power Supply Rejection Ratio (Referred to the Output) vs Supply Voltage



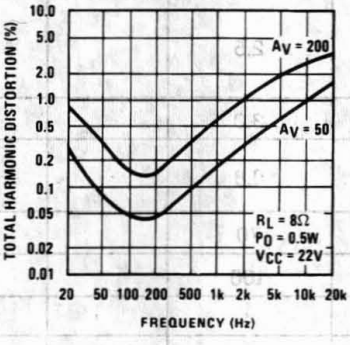
Channel Separation (Referred to the Output) vs Frequency



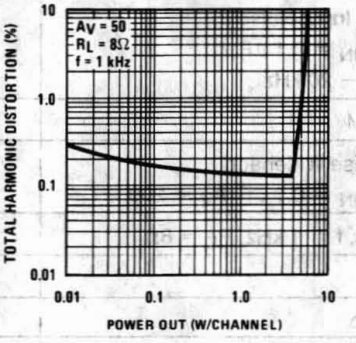
Total Harmonic Distortion vs Frequency



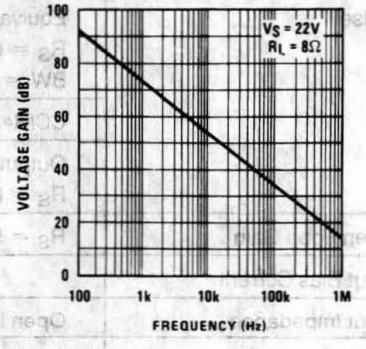
Total Harmonic Distortion vs Frequency



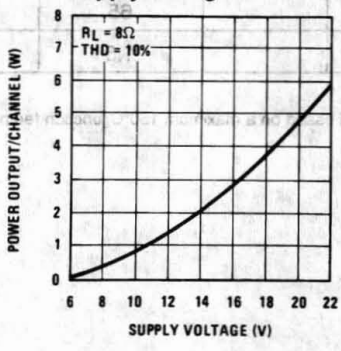
Total Harmonic Distortion vs Power Out



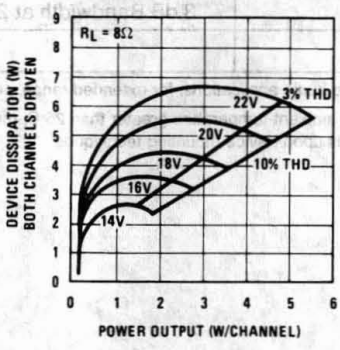
Open Loop Gain vs Frequency



Power Output/Channel vs Supply Voltage

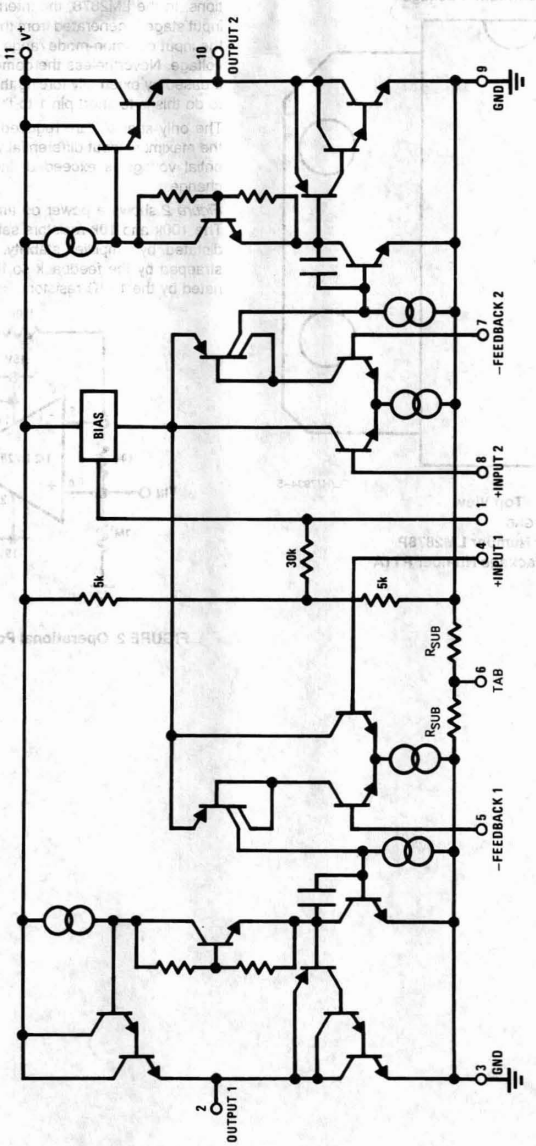


Power Dissipation vs Power Out



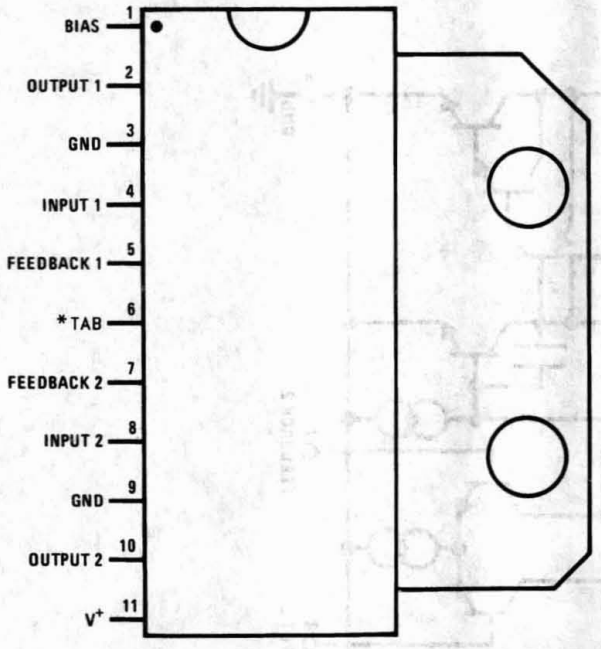
TL/H/7934–3

Equivalent Schematic Diagram



Connection Diagram

Single-In-Line Package



TL/H/7934-5

Top View

*Pin 6 must be connected to GND.

Order Number LM2878P
See NS Package Number P11A

Application Hints

The LM2878 is an improved LM378 in typical audio applications. In the LM2878, the internal voltage regulator for the input stage is generated from the voltage on pin 1. Normally, the input common-mode range is within ±0.7V of this pin 1 voltage. Nevertheless the common-mode range can be increased by externally forcing the voltage on pin 1. One way to do this is to short pin 1 to the positive supply, pin 11.

The only special care required with the LM2878 is to limit the maximum input differential voltage to ±7V. If this differential voltage is exceeded, the input characteristics may change.

Figure 2 shows a power op amp application with $A_V = 1$. The 100k and 10k resistors set a noise gain of 10 and are dictated by amplifier stability. The 10k resistor is bootstrapped by the feedback so the input resistance is dominated by the 1 MΩ resistor.

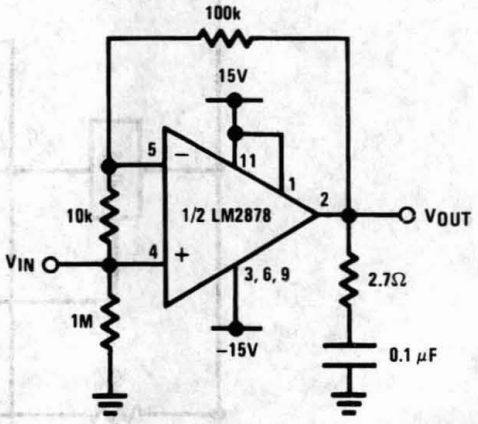


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FIGURE 2. Operational Power Amplifier, $A_V = 1$

External Components *(Figure 3)*

1. R2, R5, R7, R10 Sets voltage gain $A_V = 1 + R2/R5$ for one channel and $A_V = 1 + R10/R7$ for the other channel.
2. R4, R8 Resistors set input impedance and supply bias current for the positive input.
3. R_O Works with C_O to stabilize output stage.
4. C1 Improves power supply rejection (see Typical Performance Characteristics).
5. C11 Stabilizes amplifier, may need to be larger depending on power supply filtering.
6. C4, C8 Input coupling capacitor. Pins 4 and 8 are at a DC potential of $V_S/2$. Low frequency pole set by:

$$f_L = \frac{1}{2\pi R4C4}$$

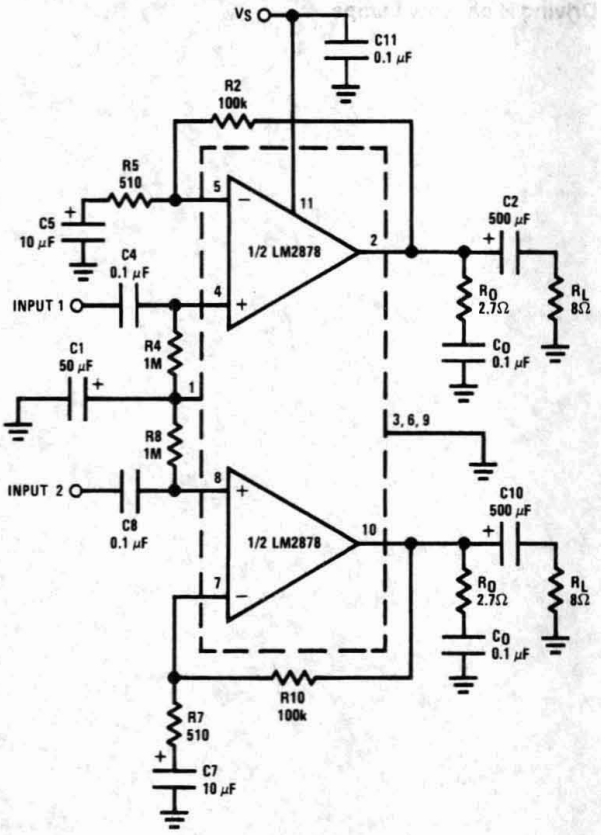
7. C5, C7 Feedback capacitors. Ensure unity gain at DC. Also low frequency pole at:

$$f_L = \frac{1}{2\pi R5C5}$$

8. C_O Works with R_O to stabilize output stage.
9. C2, C10 Output coupling capacitor. Low frequency pole given by:

$$f_L = \frac{1}{R\pi RLC2}$$

Typical Applications (Continued)



TL/H/7934–7

FIGURE 3. Stereo Amplifier with $A_V = 200$

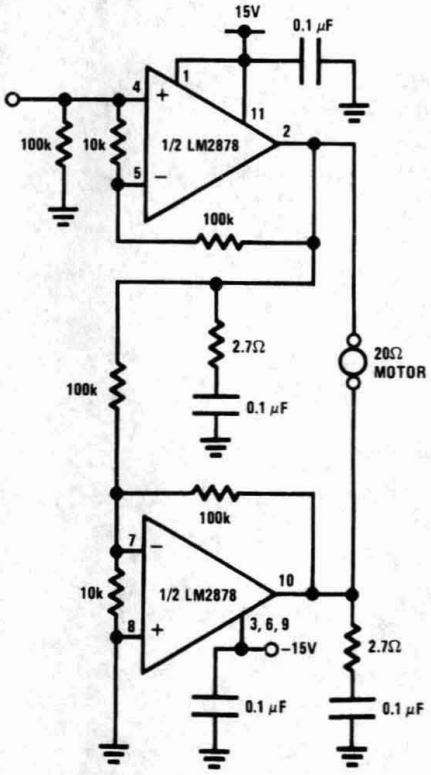


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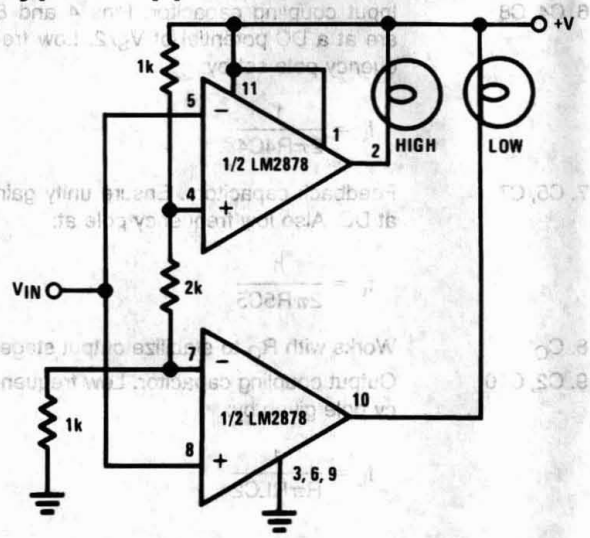
FIGURE 4. LM2878 Servo Amplifier in Bridge Configuration

Typical Applications (Continued)



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Truth Table

V_{IN}	High	Low
$< \frac{1}{4}V^+$	Off	On
$\frac{1}{4}V^+$ to $\frac{3}{4}V^+$	Off	Off
$> \frac{3}{4}V^+$	On	Off

FIGURE 5. Window Comparator Driving High, Low Lamps

National Semiconductor

LM2879 Dual 8W Audio Amplifier

General Description

The LM2879 is a monolithic dual power amplifier which offers high quality performance for stereo phonographs, tape players, recorders, AM-FM stereo receivers, etc.

The LM2879 will deliver 8W/channel to an 8Ω load. The amplifier is designed to operate with a minimum of external components and contains an internal bias regulator to bias each amplifier. Device overload protection consists of both internal current limit and thermal shutdown.

Features

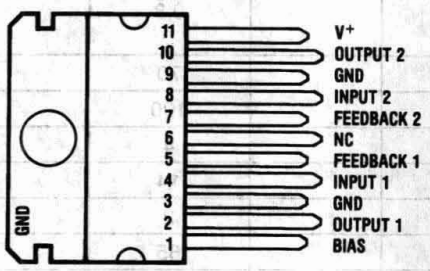
- A_{VO} typical 90 dB
- 9W per channel (typical)
- 60 dB ripple rejection
- 70 dB channel separation
- Self-centering biasing
- 4 MΩ input impedance
- Internal current limiting
- Internal thermal protection

Applications

- Multi-channel audio systems
- Tape recorders and players
- Movie projectors
- Automotive systems
- Stereo phonographs
- Bridge output stages
- AM-FM radio receivers
- Intercoms
- Servo amplifiers
- Instrument systems

Connection Diagram and Typical Application

Plastic Package

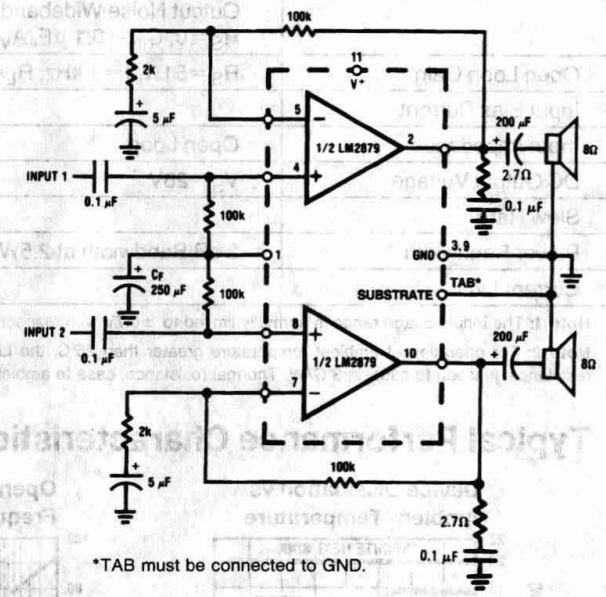


TOP VIEW

TL/H/5291–1

Order Number LM2879T
See NS Package Number TA11B

Stereo Amplifier



*TAB must be connected to GND.

TL/H/5291–2

FIGURE 1

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	35V
Input Voltage (Note 1)	±0.7V
Operating Temperature (Note 2)	0°C to + 70°C
Storage Temperature	−65°C to +150°C
Junction Temperature	150°C
Lead Temp. (Soldering, 10 seconds)	260°C
ESD rating to be determined.	
Thermal Resistance	
θ_{JC}	1°C/W
θ_{JA}	43°C/W

Electrical Characteristics

$V_S = 28V$, $T_{TAB} = 25°C$, $R_L = 8\Omega$, $A_V = 50$ (34 dB), unless otherwise specified.

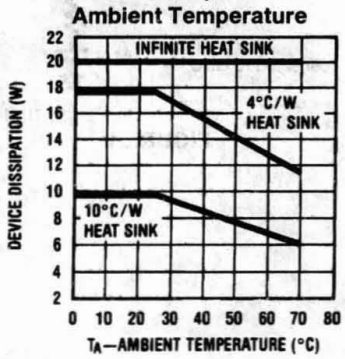
Parameter	Conditions	Min	Typ	Max	Units
Total Supply Current	$P_O = 0W$		12	65	mA
Operating Supply Voltage		6		32	V
Output Power/Channel	f = 1 kHz, THD = 10%, $T_{TAB} = 25°C$	6	8		W
Distortion	f = 1 kHz, $R_L = 8\Omega$ P_O = 1 W/Channel		0.05	1	%
Output Swing	$R_L = 8\Omega$		$V_S - 6V$		Vp-p
Channel Separation	$C_{BYPASS} = 50\ \mu F$, $C_{IN} = 0.1\ \mu F$ f = 1 kHz, Output Referred V_O = 4 Vrms	−50	−70		dB
PSRR Positive Supply	$C_{BYPASS} = 50\ \mu F$, $C_{IN} = 0.1\ \mu F$ f = 120 Hz, Output Referred V_{ripple} = 1 Vrms	−50	−60		dB
PSRR Negative Supply	Measured at DC, Input Referred		−60		dB
Common-Mode Range	Split Supplies ±15V, Pin 1 Tied to Pin 11		±13.5		V
Input Offset Voltage			10		mV
Noise	Equivalent Input Noise $R_S = 0$, $C_{IN} = 0.1\ \mu F$ BW = 20 − 20 kHz CCIR•ARM Output Noise Wideband $R_S = 0$, $C_{IN} = 0.1\ \mu F$, $A_V = 200$		 2.5 3.0 0.8		 μV μV mV
Open Loop Gain	$R_S = 51\Omega$, f = 1 kHz, $R_L = 8\Omega$		70		dB
Input Bias Current			100		nA
Input Impedance	Open Loop		4		MΩ
DC Output Voltage	$V_S = 28V$		14		V
Slew Rate			2		V/μs
Power Bandwidth	3 dB Bandwidth at 2.5W		65		kHz
Current Limit			1.5		A

Note 1: The input voltage range is normally limited to ±0.7V with respect to pin 1. This range may be extended by shorting pin 1 to the positive supply.

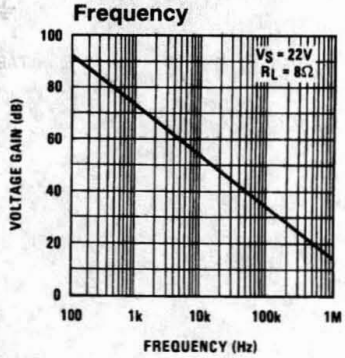
Note 2: For operation at ambient temperature greater than 25°C, the LM2879 must be derated based on a maximum 150°C junction temperature. Thermal resistance, junction to case, is 3°C/W. Thermal resistance, case to ambient, is 40°C/W.

Typical Performance Characteristics

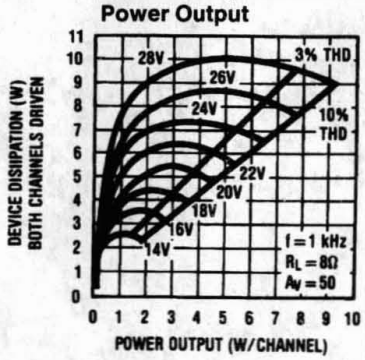
Device Dissipation vs Ambient Temperature



Open Loop Gain vs Frequency



Power Dissipation vs Power Output



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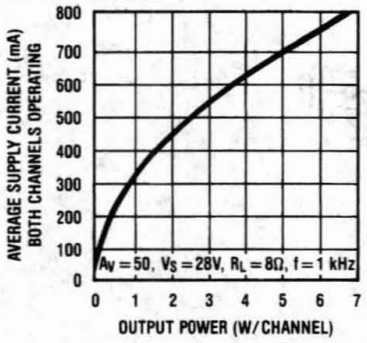
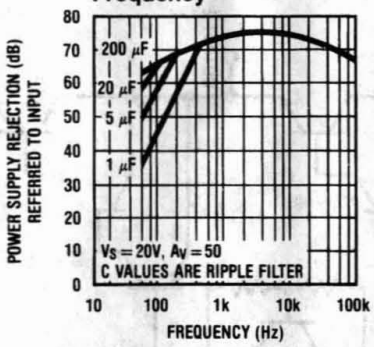
Typical Performance Characteristics (Continued)

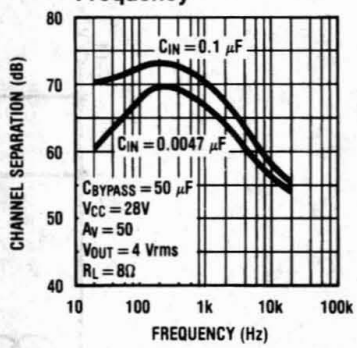
Supply Current vs Output Power



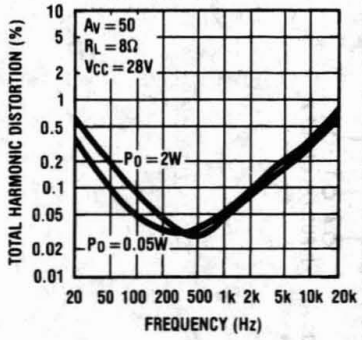
Supply Rejection vs Frequency



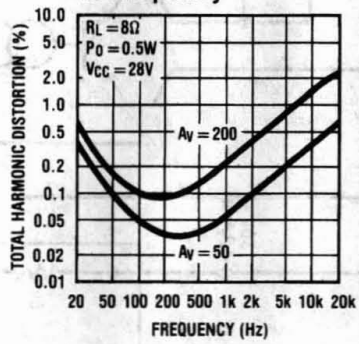
Channel Separation (Referred to the Output) Frequency



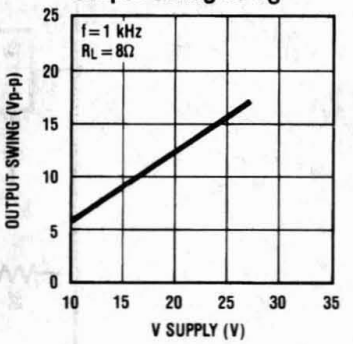
Total Harmonic Distortion vs Frequency



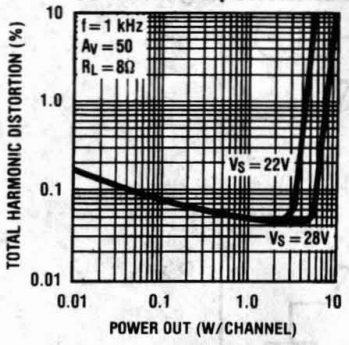
Total Harmonic Distortion vs Frequency



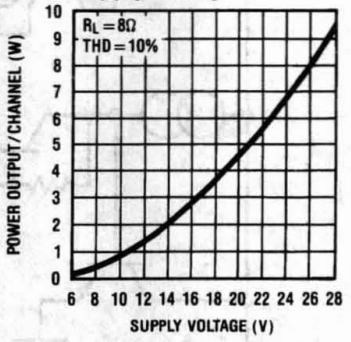
Output Swing vs V_S



Total Harmonic Distortion vs Power Output

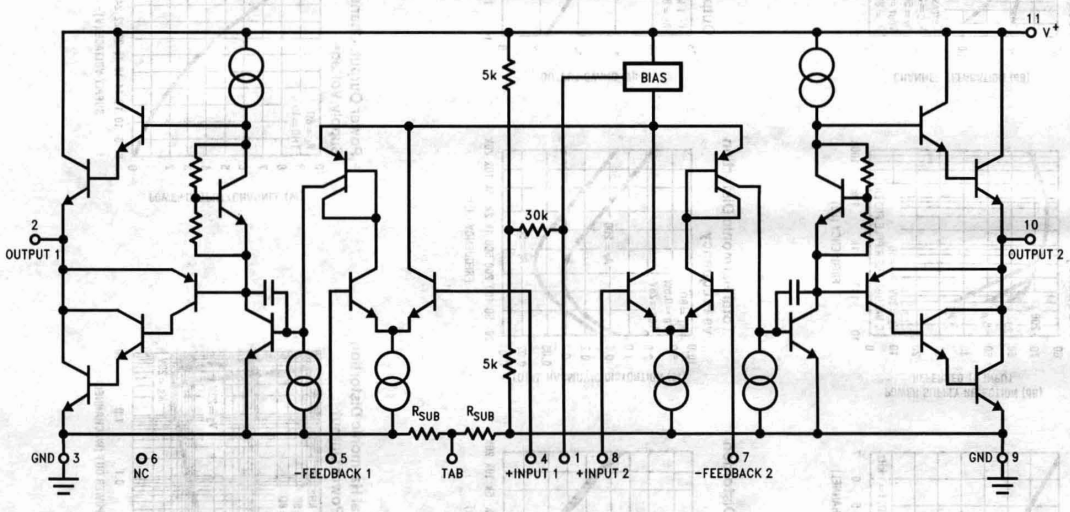


Power Output/Channel vs Supply Voltage



TL/H/5291–4

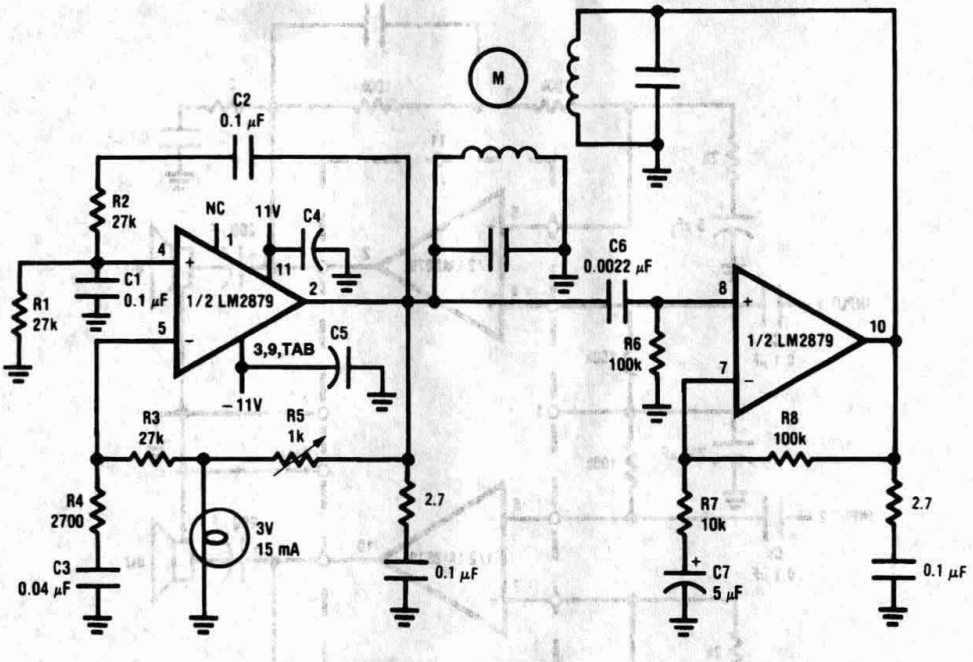
Equivalent Schematic Diagram



TL/H/5291–5

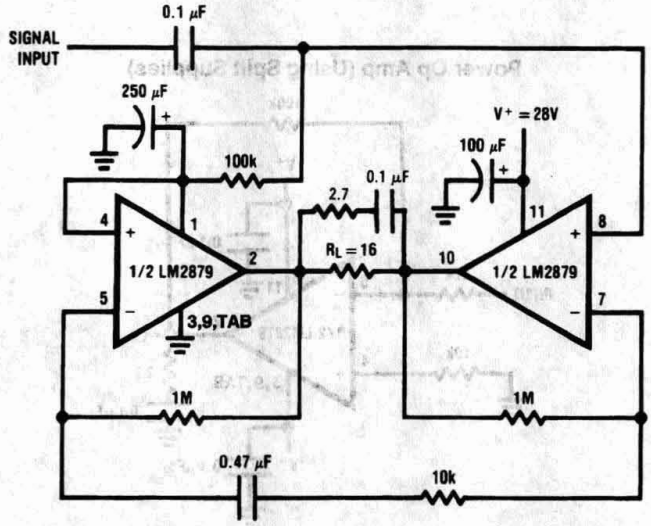
Typical Applications

Two-Phase Motor Drive



TL/H/5291–6

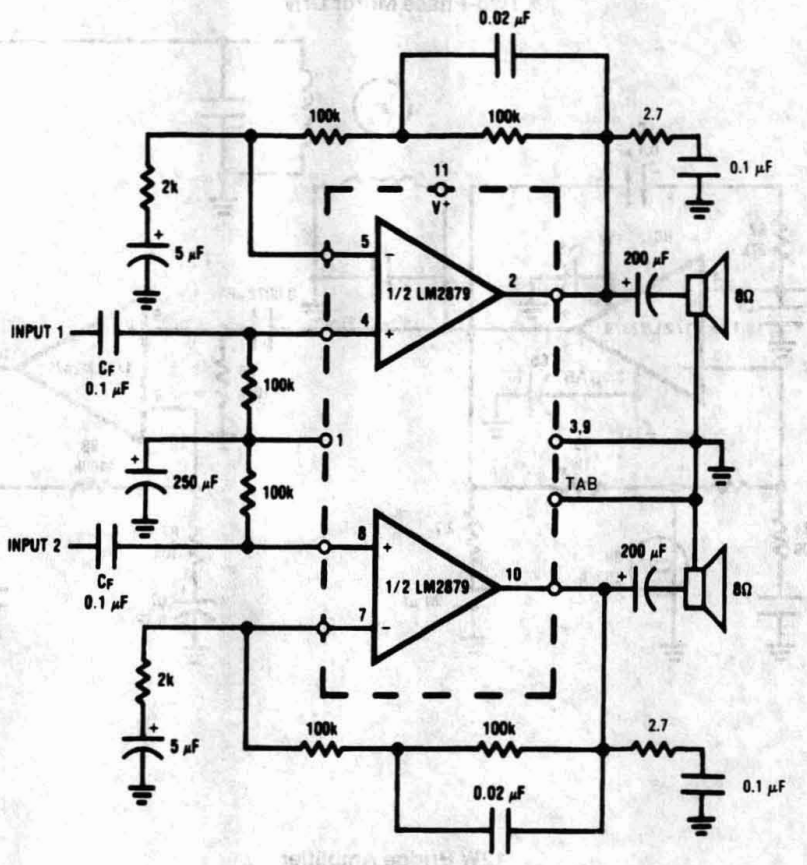
12W Bridge Amplifier



TL/H/5291–7

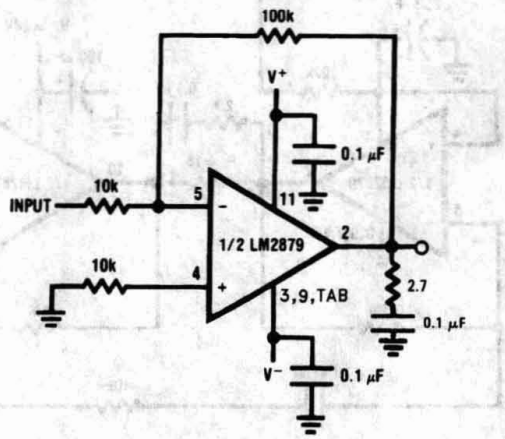
Typical Applications (Continued)

Simple Stereo Amplifier with Bass Boost



TL/H/5291–8

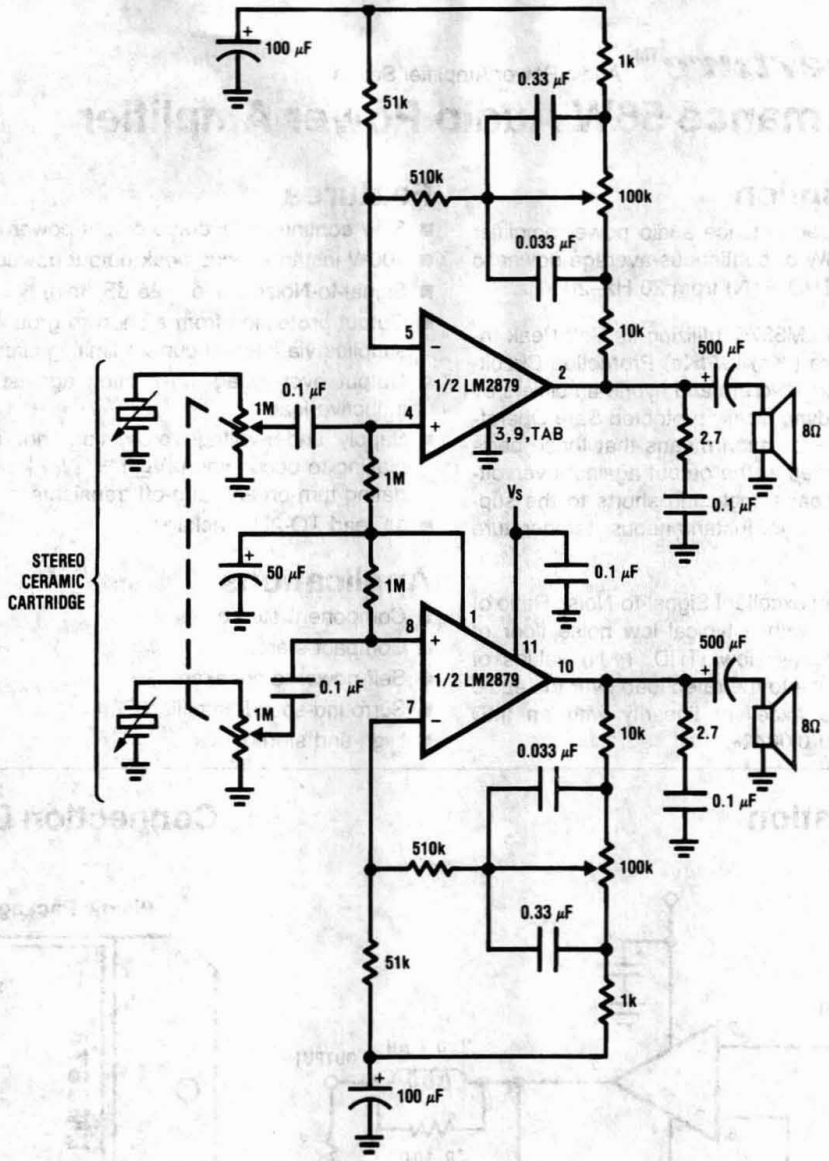
Power Op Amp (Using Split Supplies)



TL/H/5291–9

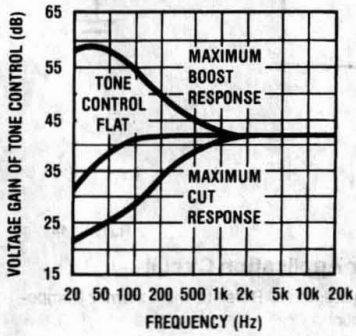
Typical Applications (Continued)

Stereo Phonograph Amplifier with Bass Tone Control



TL/H/5291–10

Frequency Response of Bass Tone Control



TL/H/5291–11

National Semiconductor

LM3875 *Overture*™ Audio Power Amplifier Series
High-Performance 56W Audio Power Amplifier

General Description

The LM3875 is a high-performance audio power amplifier capable of delivering 56W of continuous average power to an 8Ω load with 0.1% (THD + N) from 20 Hz–20 kHz.

The performance of the LM3875, utilizing its Self Peak Instantaneous Temperature (°Ke) (**SPiKe**) Protection Circuitry, puts it in a class above discrete and hybrid amplifiers by providing an inherently, dynamically protected Safe Operating Area (SOA). **SPiKe** Protection means that these parts are completely safeguarded at the output against overvoltage, undervoltage, overloads, including shorts to the supplies, thermal runaway, and instantaneous temperature peaks.

The LM3875 maintains an excellent Signal-to-Noise Ratio of greater than 95 dB(min) with a typical low noise floor of 2.0 μV. It exhibits extremely low (THD + N) values of 0.06% at the rated output into the rated load over the audio spectrum, and provides excellent linearity with an IMD (SMPTE) typical rating of 0.004%.

Features

- 56W continuous average output power into 8Ω
- 100W instantaneous peak output power capability
- Signal-to-Noise Ratio >95 dB (min)
- Output protection from a short to ground or to the supplies via internal current limiting circuitry
- Output over-voltage protection against transients from inductive loads
- Supply under-voltage protection, not allowing internal biasing to occur when $|V_{EE}| + |V_{CC}| \leq 12V$, thus eliminating turn-on and turn-off transients
- 11 lead TO-220 package

Applications

- Component stereo
- Compact stereo
- Self-powered speakers
- Surround-sound amplifiers
- High-end stereo TVs

Typical Application

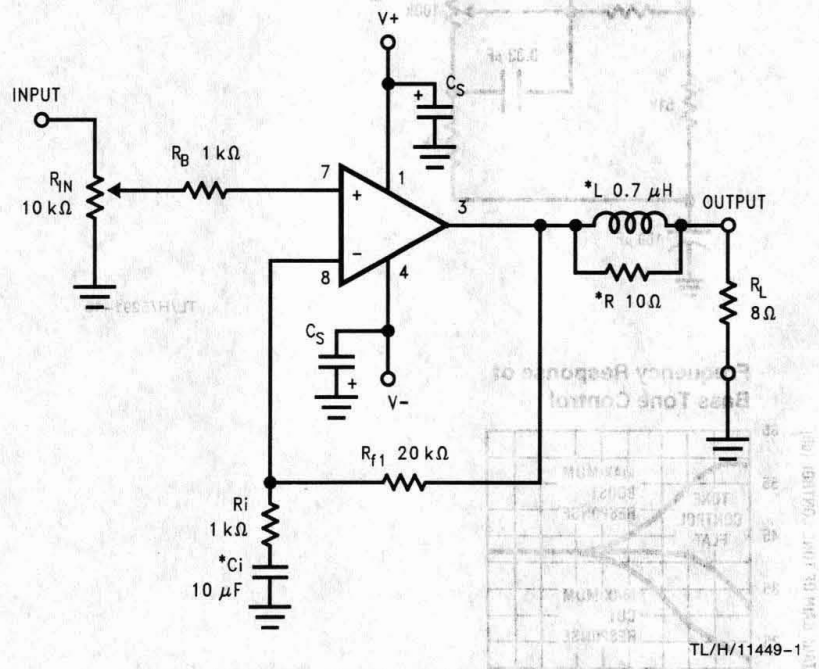
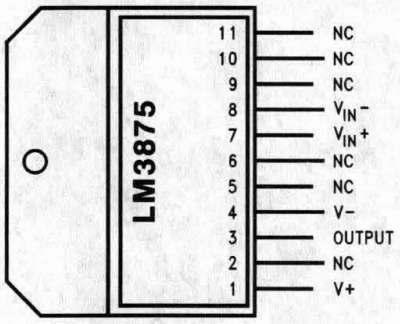


FIGURE 1. Typical Audio Amplifier Application Circuit

*Optional components dependent upon specific design requirements. Refer to the External Components Description section for a component function description.

Connection Diagram

Plastic Package (Note 8)



Top View

Order Number LM3875T or LM3875TF
See NS Package Number TA11B for Staggered Lead Non-Isolated Package or TF11B for Staggered Lead Isolated Package

Absolute Maximum Ratings (Notes 1, 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage $\|V^+\| + \|V^-\|$ (No Signal)	94V
Supply Voltage $\|V^+\| + \|V^-\|$ (Input Signal)	84V
Common Mode Input Voltage	(V^+ or V^-) and $\|V^+\| + \|V^-\| \leq 80V$
Differential Input Voltage	60V
Output Current	Internally Limited
Power Dissipation (Note 3)	125W
ESD Susceptibility (Note 4)	2500V
Junction Temperature (Note 5)	150°C
Soldering Information T package (10 seconds)	260°C
Storage Temperature	−40°C to +150°C
Thermal Resistance θ_{JC}	1°C/W
Thermal Resistance θ_{JA}	43°C/W

Operating Ratings (Notes 1, 2)

Temperature Range $T_{MIN} \leq T_A \leq T_{MAX}$	$-20°C \leq T_A \leq +85°C$
Supply Voltage $\|V^+\| + \|V^-\|$	20V to 84V

Note: Operation is guaranteed up to 84V, however, distortion may be introduced from the **SPiKe** Protection Circuitry when operating above 70V if proper thermal considerations are not taken into account. Refer to the Thermal Considerations section for more information. (See **SPiKe** Protection Response)

Electrical Characteristics (Notes 1, 2) The following specifications apply for $V^+ = +35V$, $V^- = -35V$ with $R_L = 8\Omega$ unless otherwise specified. Limits apply for $T_A = 25°C$.

Symbol	Parameter	Conditions	LM3875 Typical (Note 6)	LM3875 Limit (Note 7)	Units (Limits)
$\|V^+\| + \|V^-\|$	Power Supply Voltage			20 84	V (Min) V (Max)
**P_O	Output Power (Continuous Average)	THD + N = 0.1% (Max) f = 1 kHz, f = 20 kHz	56	40	W (Min)
Peak P_O	Instantaneous Peak Output Power		100		W
THD + N	Total Harmonic Distortion Plus Noise	40W, 20 Hz ≤ f ≤ 20 kHz A_V = 26 dB	0.06		%
**SR	Slew Rate (Note 9)	V_{IN} = 1.414 Vrms, f = 10 kHz Square-wave, $R_L = 2 k\Omega$	11	5	V/μs (Min)
*I+	Total Quiescent Power Supply Current	V_{CM} = 0V, V_O = 0V, I_o = 0 mA	30	70	mA (Max)
*V_{OS}	Input Offset Voltage	V_{CM} = 0V, I_o = 0 mA	1	10	mV (Max)
I_B	Input Bias Current	V_{CM} = 0V, I_o = 0 mA	0.2	1	μA (Max)
I_{OS}	Input Offset Current	V_{CM} = 0V, I_o = 0 mA	0.01	0.2	μA (Max)
I_o	Output Current Limit	$\|V^+\| = \|V^-\| = 10V$, t_{on} = 10 ms, V_O = 0V	6	4	A (Min)
*V_{od}	Output Dropout Voltage (Note 10)	$\|V^+ - V_o\|$, $V^+ = 20V$, $I_o = +100$ mA $\|V_o - V^-\|$, $V^- = -20V$, $I_o = -100$ mA	1.6 2.7	5 5	V (Max) V (Max)
*PSRR	Power Supply Rejection Ratio	V^+ = 40V to 20V, V^- = −40V, V_{cm} = 0V, I_o = 0 mA V^+ = 40V, V^- = −40V to −20V, V_{cm} = 0V, I_o = 0 mA	120 120	85 85	dB (Min)
*CMRR	Common Mode Rejection Ratio	V^+ = 60V to 20V, V^- = −20V to −60V, V_{cm} = 20V to −20V, I_o = 0 mA	120	80	dB (Min)
*A_{VOL}	Open Loop Voltage Gain	$\|V^+\| = \|V^-\| = 40V$, $R_L = 2 k\Omega$, $\Delta V_O = 60V$	120	90	dB (Min)
GBWP	Gain-Bandwidth Product	$\|V^+\| = \|V^-\| = 40V$ f_O = 100 kHz, V_{IN} = 50 mVrms	8	2	MHz (Min)
**e_{IN}	Input Noise	IHF − A Weighting Filter $R_{IN} = 600\Omega$ (Input Referred)	2.0	8.0	μV (Max)

*DC Electricat Test; refer to Test Circuit #1.

**AC Electrical Test; refer to Test Circuit #2.

1

Electrical Characteristics (Notes 1, 2) The following specifications apply for $V^+ = +35V$, $V^- = -35V$ with $R_L = 8\Omega$ unless otherwise specified. Limits apply for $T_A = 25°C$. (Continued)

Symbol	Parameter	Conditions	LM3875		Units (Limits)
			Typical (Note 6)	Limit (Note 7)	
SNR	Signal-to-Noise Ratio	$P_O = 1W$, A-Weighted, Measured at 1 kHz, $R_S = 25\Omega$	98 dB		dB
		$P_O = 40W$, A-Weighted, Measured at 1 kHz, $R_S = 25\Omega$	114 dB		dB
		$P_{pk} = 100W$, A-Weighted, Measured at 1 kHz, $R_S = 25\Omega$	122 dB		dB
IMD	Intermodulation Distortion Test	60 Hz, 7 kHz, 4:1 (SMPTE) 60 Hz, 7 kHz, 1:1 (SMPTE)	0.004 0.006		%

*DC Electrical Test; refer to Test Circuit #1.

**AC Electrical Test; refer to Test Circuit #2.

Note 1: All voltages are measured with respect to supply GND, unless otherwise specified.

Note 2: *Absolute Maximum Ratings* indicate limits beyond which damage to the device may occur. *Operating Ratings* indicate conditions for which the device is functional, but do not guarantee specific performance limits. *Electrical Characteristics* state DC and AC electrical specifications under particular test conditions which guarantee specific performance limits. This assumes that the device is within the Operating Ratings. Specifications are not guaranteed for parameters where no limit is given, however, the typical value is a good indication of device performance.

Note 3: For operating at case temperatures above 25°C, the device must be derated based on a 150°C maximum junction temperature and a thermal resistance of $\theta_{JC} = 1.0°C/W$ (junction to case). Refer to the Thermal Resistance figure in the Application Information section under **Thermal Considerations**.

Note 4: Human body model, 100 pF discharged through a 1.5 kΩ resistor.

Note 5: The operating junction temperature maximum is 150°C, however, the instantaneous Safe Operating Area temperature is 250°C.

Note 6: Typicals are measured at 25°C and represent the parametric norm.

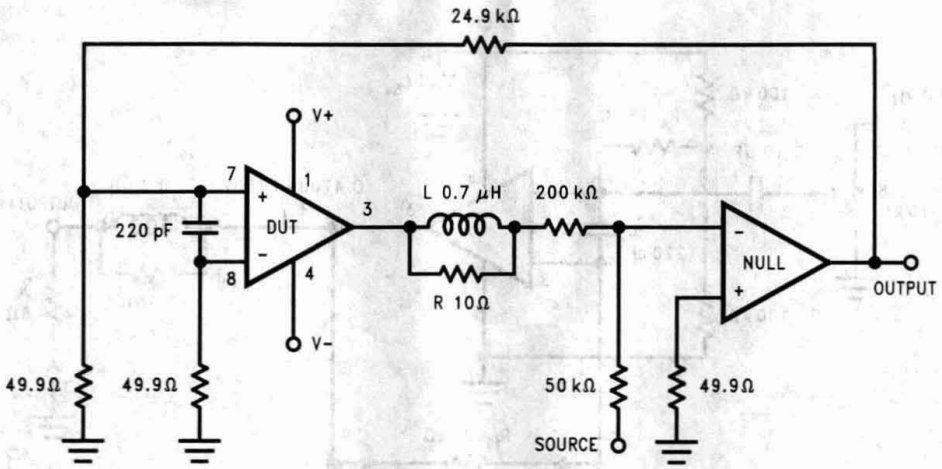
Note 7: Limits are guaranteed to National's AOQL (Average Outgoing Quality Level).

Note 8: The LM3875T package TA11B is a non-isolated package, setting the tab of the device and the heat sink at V^- potential when the LM3875 is directly mounted to the heat sink using only thermal compound. If a mica washer is used in addition to thermal compound, θ_{CS} (case to sink) is increased, but the heat sink will be isolated from V^-.

Note 9: The feedback compensation network limits the bandwidth of the closed-loop response and so the slew rate will be reduced due to the high frequency roll-off. Without feedback compensation, the slew rate is typically $16V/\mu s$.

Note 10: The output dropout voltage is the supply voltage minus the clipping voltage. Refer to the Clipping Voltage vs. Supply Voltage graph in the **Typical Performance Characteristics** section.

Test Circuit #1 *(DC Electrical Test Circuit)



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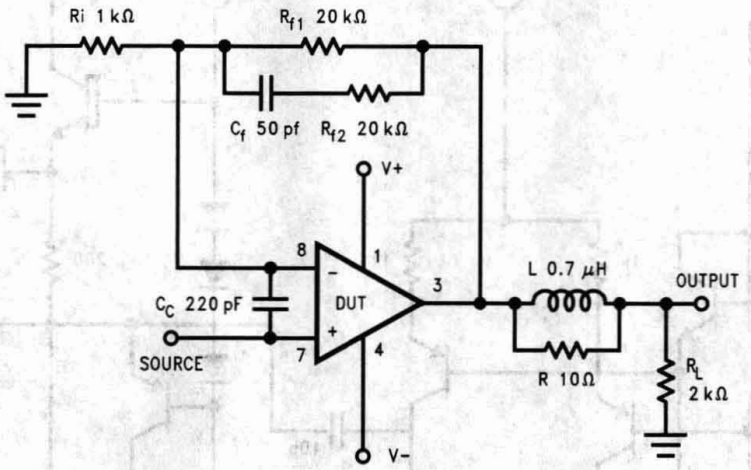
Test Circuit #2 (** AC Electrical Test Circuit)



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Single Supply Application Circuit

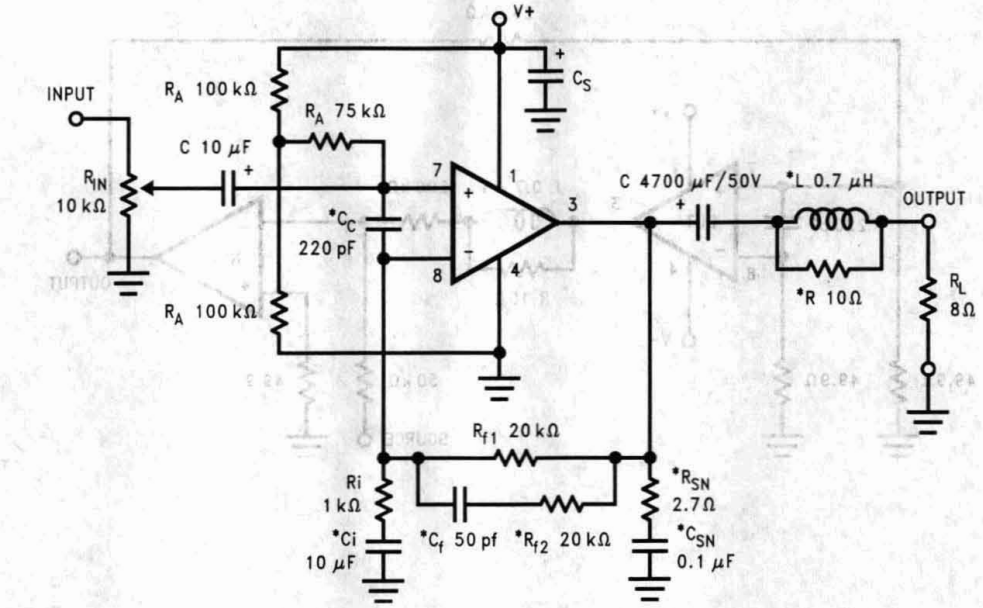

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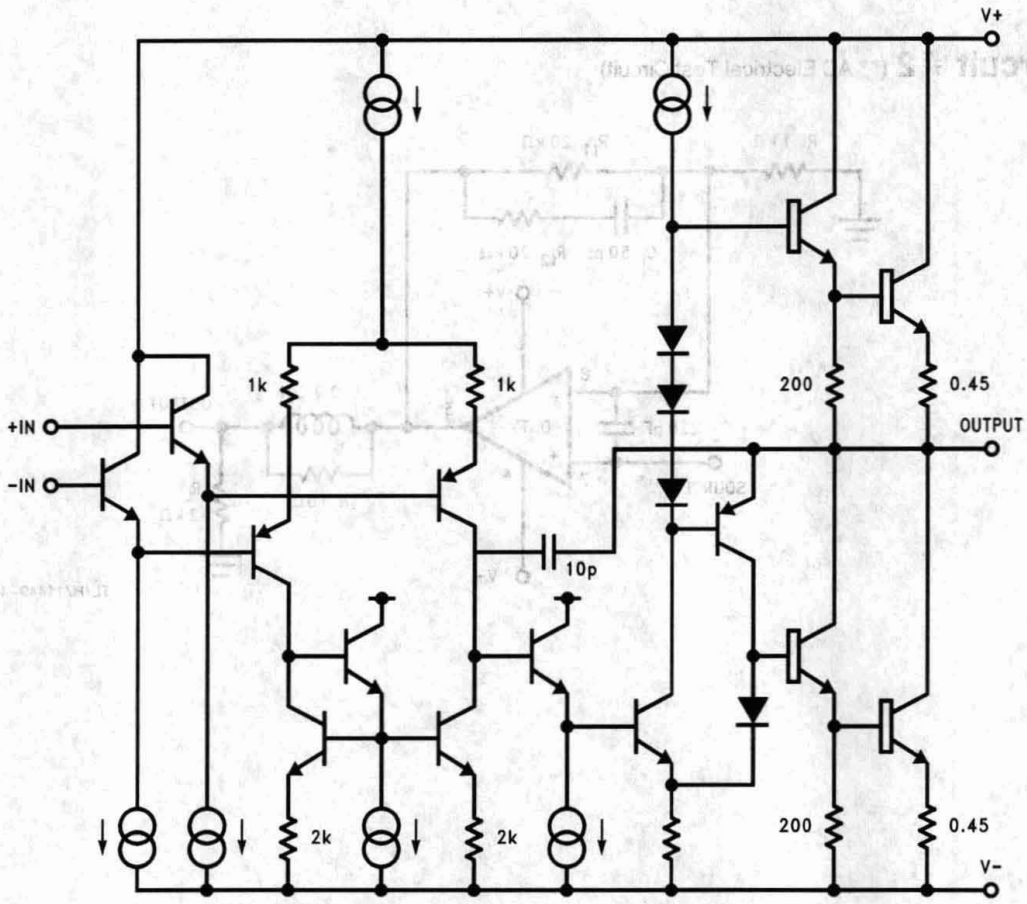
FIGURE 2. Typical Single Supply Audio Amplifier Application Circuit

*Optional components dependent upon specific design requirements. Refer to the External Components Description section for a component function description.

Equivalent Schematic (Excluding active protection circuitry)



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External Components Description (*Figures 1* and *2*)

Components		Functional Description
1.	R_{IN}	Acts as a volume control by setting the voltage level allowed to the amplifier's input terminals.
2.	R_A	Provides DC voltage biasing for the single supply operation and bias current for the positive input terminal.
3.	C_A	Provides bias filtering.
4.	C	Provides AC coupling at the input and output of the amplifier for single supply operation.
5.	R_B	Prevents currents from entering the amplifier's non-inverting input which may be passed through to the load upon power-down of the system due to the low input impedance of the circuitry when the under-voltage circuitry is off. This phenomenon occurs when the supply voltages are below 1.5V.
6.	*C_C	Reduces the gain (bandwidth of the amplifier) at high frequencies to avoid quasi-saturation oscillations of the output transistor. The capacitor also suppresses external electromagnetic switching noise created from fluorescent lamps.
7.	Ri	Inverting input resistance to provide AC Gain in conjunction with R_{f1}.
8.	*Ci	Feedback capacitor. Ensures unity gain at DC. Also a low frequency pole (highpass roll-off) at: $f_c = 1/(2\pi\ Ri\ Ci)$.
9.	R_{f1}	Feedback resistance to provide AC Gain in conjunction with Ri.
10.	*R_{f2}	At higher frequencies feedback resistance works with C_f to provide lower AC Gain in conjunction with R_{f1} and Ri. A high frequency pole (lowpass roll-off) exists at: $f_c = [R_{f1}\ R_{f2}]\ (s + 1/R_{f2}\ C_f]/[(R_{f1} + R_{f2})\ (s + 1/C_f\ (R_{f1} + R_{f2}))]$.
11.	*C_f	Compensation capacitor that works with R_{f1} and R_{f2} to reduce the AC Gain at higher frequencies.
12.	*R_{SN}	Works with C_{SN} to stabilize the output stage by creating a pole that eliminates high frequency oscillations.
13.	*C_{SN}	Works with R_{SN} to stabilize the output stage by creating a pole that eliminates high frequency oscillations. $f_c = 1/(2\pi R_{SN}\ C_{SN})$.
14.	*L	Provides high impedance at high frequencies so that R may decouple a highly capacitive load and reduce the
15.	*R	Q of the series resonant circuit due to capacitive load. Also provides a low impedance at low frequencies to short out R and pass audio signals to the load.
16.	C_S	Provides power supply filtering and bypassing.

*Optional components dependent upon specific design requirements. Refer to the Application Information section for more information.

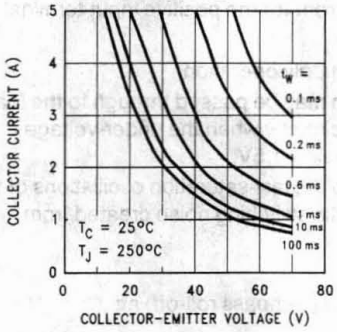
OPTIONAL EXTERNAL COMPONENT INTERACTION

Although the optional external components have specific desired functions that are designed to reduce the bandwidth and eliminate unwanted high frequency oscillations they may cause certain undesirable effects when they interact. Interaction may occur for components whose reactances are in close proximity to one another. One example would be the coupling capacitor, C_C, and the compensation capacitor, C_f. These two components act as low impedances to certain frequencies which will couple signals from the input to the output. Please take careful note of basic amplifier component functionality when designing in these components.

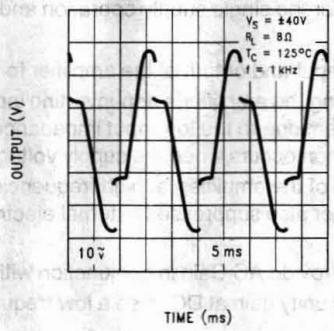
The optional external components shown in *Figure 2* and described above are applicable in both single and split voltage supply configurations.

Typical Performance Characteristics

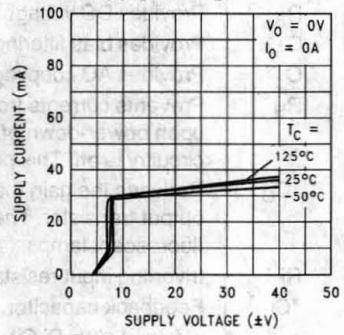
Safe Area



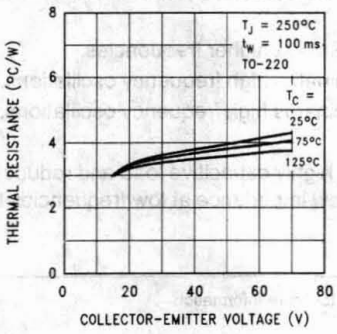
SPiKe Protection Response



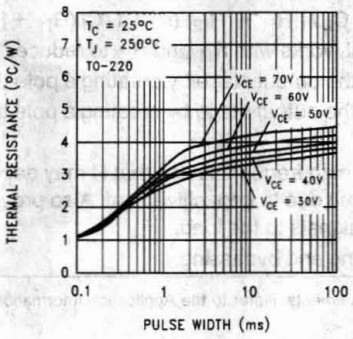
Supply Current vs Supply Voltage



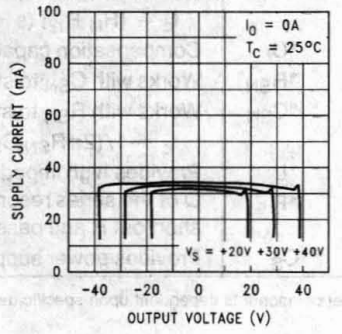
Pulse Thermal Resistance



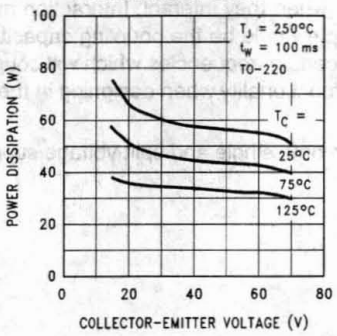
Pulse Thermal Resistance



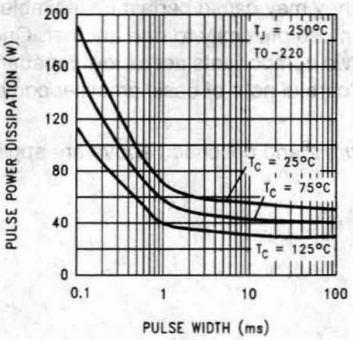
Supply Current vs Output Voltage



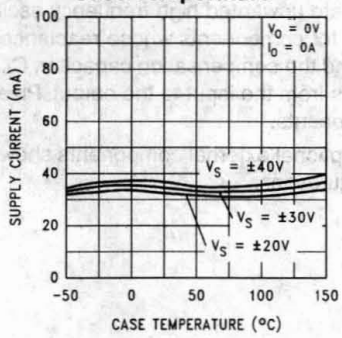
Pulse Power Limit



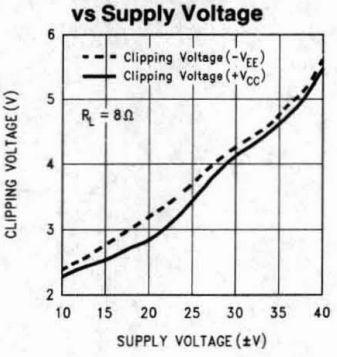
Pulse Power Limit



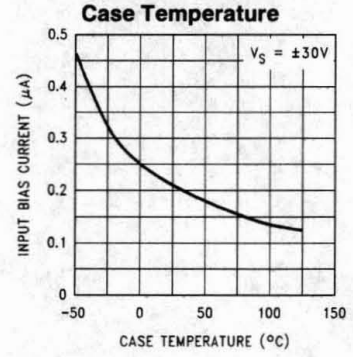
Supply Current vs Case Temperature



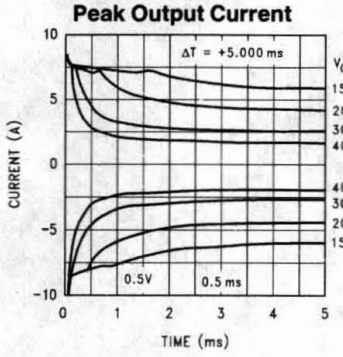
Clipping Voltage vs Supply Voltage



Input Bias Current vs Case Temperature



Peak Output Current



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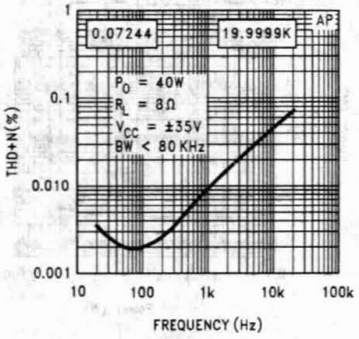
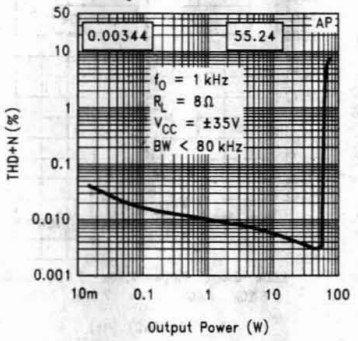
Typical Performance Characteristics (Continued)

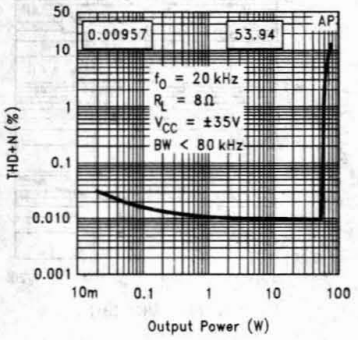
THD + N vs Frequency



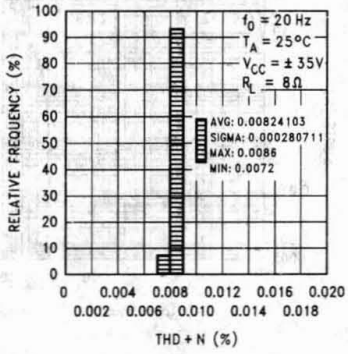
THD + N vs Output Power



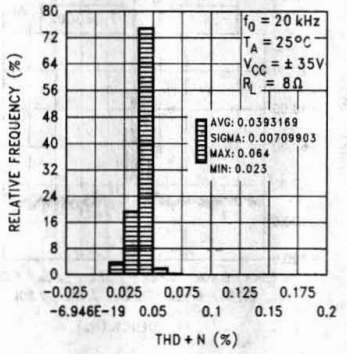
THD + N vs Output Power



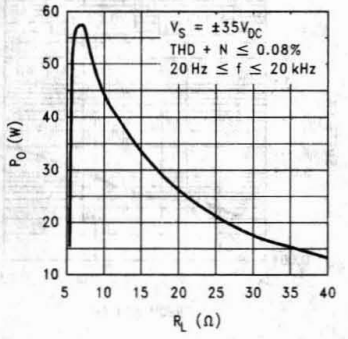
THD Distribution



THD Distribution



Output Power vs Load Resistance



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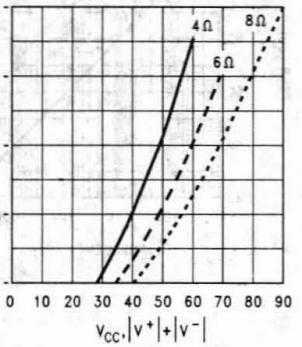
Max Heatsink Thermal Resistance (°C/W) at the Specified Ambient Temperature (°C)

T_A = 25°C	40	50	60	70	80	90	100	110	T_C, °C	P_D, W
1.3	1.0								90	50
1.6	1.2	1.0							96	45
1.9	1.6	1.3	1.1						102	40
2.4	1.9	1.7	1.4	1.1					108	35
3.0	2.5	2.1	1.8	1.5	1.1				114	30
3.8	3.2	2.8	2.4	2.0	1.6	1.2			120	25
5.1	4.3	3.8	3.3	2.8	2.3	1.8	1.3		126	20
7.1	6.1	5.5	4.8	4.1	3.5	2.8	2.1	1.5	132	15
11.3	9.8	8.8	7.8	6.8	5.8	4.8	3.8	2.8	138	10

Note: The maximum heat sink thermal resistance values, $\varnothing_{SA}$, in the table above were calculated using a $\varnothing_{CS}$ = 0.2°C/W due to thermal compound.

Maximum Power Dissipation vs Supply Voltage



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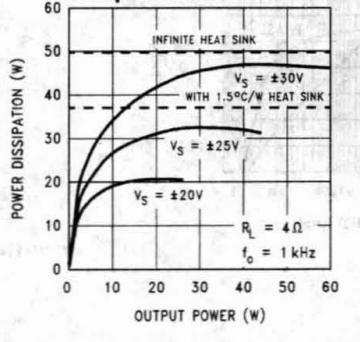
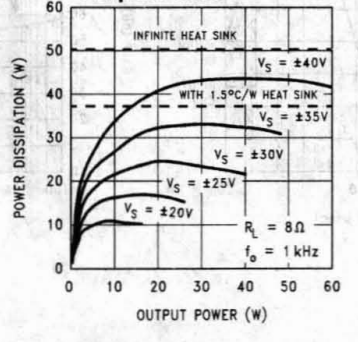
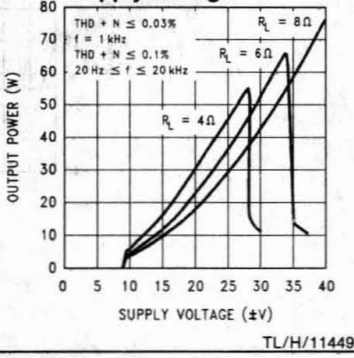
Power Dissipation vs Output Power



Power Dissipation vs Output Power



Output Power vs Supply Voltage



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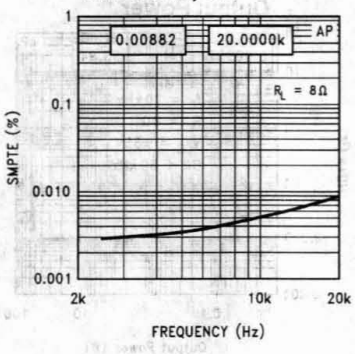
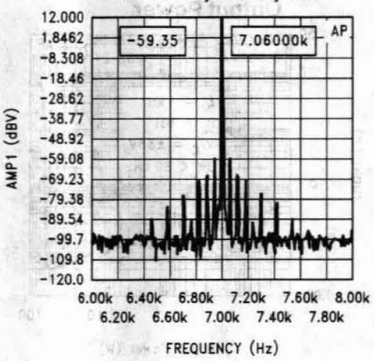
Typical Performance Characteristics (Continued)

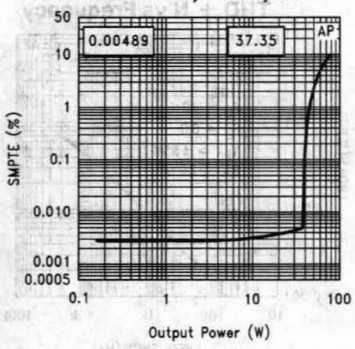
IMD 60 Hz, 4:1



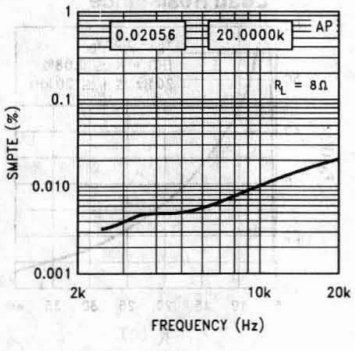
IMD 60 Hz, 7 kHz, 4:1



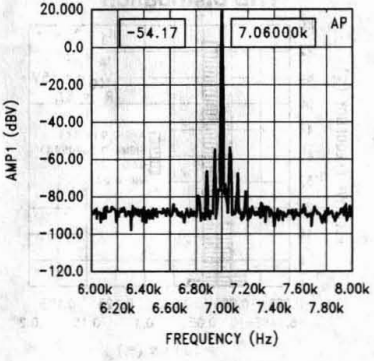
IMD 60 Hz, 7 kHz, 4:1



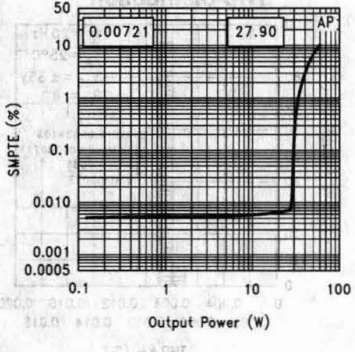
IMD 60 Hz, 1:1



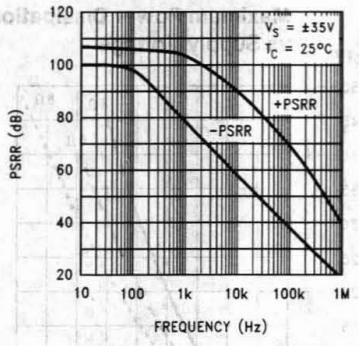
IMD 60 Hz, 7 kHz, 1:1



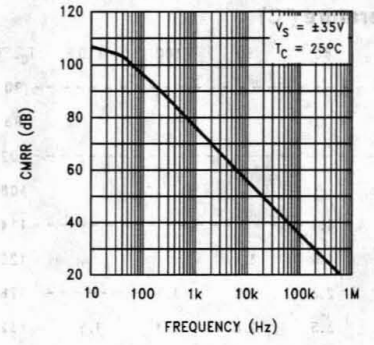
IMD 60 Hz, 7 kHz, 1:1



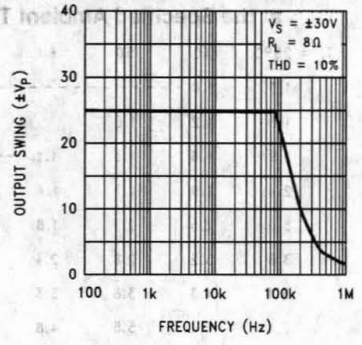
Power Supply Rejection Ratio



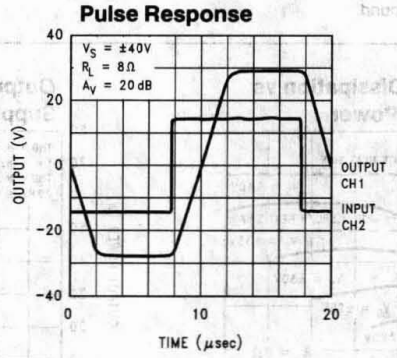
Common-Mode Rejection Ratio



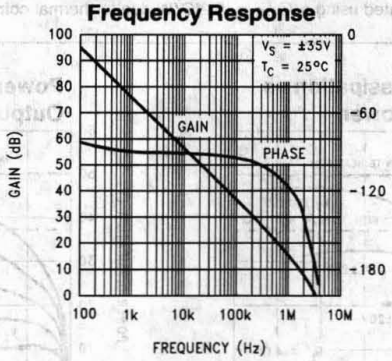
Large Signal Response



Pulse Response



Open Loop Frequency Response



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Application Information

GENERAL FEATURES

Under-Voltage Protection: Upon system power-up the under-voltage Protection Circuitry allows the power supplies and their corresponding caps to come up close to their full values before turning on the LM3875 such that no DC output spikes occur. Upon turn-off, the output of the LM3875 is brought to ground before the power supplies such that no transients occur at power-down.

Over-Voltage Protection: The LM3875 contains overvoltage protection circuitry that limits the output current to approximately 4Apeak while also providing voltage clamping, though not through internal clamping diodes. The clamping effect is quite the same, however, the output transistors are designed to work alternately by sinking large current spikes.

SPiKe Protection: The LM3875 is protected from instantaneous peak-temperature stressing by the power transistor array. The Safe Operating Area graph in the **Typical Performance Characteristics** section shows the area of device operation where the **SPiKe** Protection Circuitry is not enabled. The waveform to the right of the SOA graph exemplifies how the dynamic protection will cause waveform distortion when enabled.

Thermal Protection: The LM3875 has a sophisticated thermal protection scheme to prevent long-term thermal stress to the device. When the temperature on the die reaches 165°C, the LM3875 shuts down. It starts operating again when the die temperature drops to about 155°C, but if the temperature again begins to rise, shutdown will occur again at 165°C. Therefore the device is allowed to heat up to a relatively high temperature if the fault condition is temporary, but a sustained fault will cause the device to cycle in a Schmitt Trigger fashion between the thermal shutdown temperature limits of 165°C and 155°C. This greatly reduces the stress imposed on the IC by thermal cycling, which in turn improves its reliability under sustained fault conditions.

Since the die temperature is directly dependent upon the heat sink, the heat sink should be chosen as discussed in the **Thermal Considerations** section, such that thermal shutdown will not be reached during normal operation. Using the best heat sink possible within the cost and space constraints of the system will improve the long-term reliability of any power semiconductor device.

THERMAL CONSIDERATIONS

Heat Sinking

The choice of a heat sink for a high-power audio amplifier is made entirely to keep the die temperature at a level such that the thermal protection circuitry does not operate under normal circumstances. The heat sink should be chosen to dissipate the maximum IC power for a given supply voltage and rated load.

With high-power pulses of longer duration than 100 ms, the case temperature will heat up drastically without the use of a heat sink. Therefore the case temperature, as measured at the center of the package bottom, is entirely dependent on heat sink design and the mounting of the IC to the heat sink. For the design of a heat sink for your audio amplifier application refer to the **Determining the Correct Heat Sink** section.

Since a semiconductor manufacturer has no control over which heat sink is used in a particular amplifier design, we can only inform the system designer of the parameters and the method needed in the determination of a heat sink. With this in mind, the system designer must choose his supply voltages, a rated load, a desired output power level, and know the ambient temperature surrounding the device. These parameters are in addition to knowing the maximum junction temperature and the thermal resistance of the IC, both of which are provided by National Semiconductor.

As a benefit to the system designer we have provided Maximum Power Dissipation vs Supply Voltages curves for various loads in the **Typical Performance Characteristics** section, giving an accurate figure for the maximum thermal resistance required for a particular amplifier design. This data was based on θ_{JC} = 1°C/W and θ_{CS} = 0.2°C/W. We also provide a section regarding heat sink determination for any audio amplifier design where θ_{CS} may be a different value. It should be noted that the idea behind dissipating the maximum power within the IC is to provide the device with a low resistance to convection heat transfer such as a heat sink. Therefore, it is necessary for the system designer to be conservative in his heat sink calculations. As a rule, the lower the thermal resistance of the heat sink the higher the amount of power that may be dissipated. This is, of course, guided by the cost and size requirements of the system. Convection cooling heat sinks are available commercially, and their manufacturers should be consulted for ratings.

Proper mounting of the IC is required to minimize the thermal drop between the package and the heat sink. The heat sink must also have enough metal under the package to conduct heat from the center of the package bottom to the fins without excessive temperature drop.

A thermal grease such as Wakefield type 120 or Thermalloy Thermacote should be used when mounting the package to the heat sink. Without this compound, the thermal resistance will be no better than 0.5°C/W, and probably much worse. With the compound, thermal resistance will be 0.2°C/W or less, assuming under 0.005 inch combined flatness runout for the package and heat sink. Proper torquing of the mounting bolts is important and can be determined from heat sink manufacturer's specification sheets.

Should it be necessary to isolate V^- from the heat sink, an insulating washer is required. Hard washers like berylum oxide, anodized aluminum and mica require the use of thermal compound on both faces. Two-mil mica washers are most common, giving about 0.4°C/W interface resistance with the compound.

Silicone-rubber washers are also available. A 0.5°C/W thermal resistance is claimed without thermal compound. Experience has shown that these rubber washers deteriorate and must be replaced should the IC be dismounted.

Determining Maximum Power Dissipation

Power dissipation within the integrated circuit package is a very important parameter requiring a thorough understanding if optimum power output is to be obtained. An incorrect maximum power dissipation (P_D) calculation may result in inadequate heatsinking, causing thermal shutdown circuitry to operate and limit the output power.

Application Information (Continued)

The following equations can be used to accurately calculate the maximum and average integrated circuit power dissipation for your amplifier design, given the supply voltage, rated load, and output power. These equations can be directly applied to the Power Dissipation vs Output Power curves in the **Typical Performance Characteristics** section.

Equation (1) exemplifies the maximum power dissipation of the IC and equations (2) and (3) exemplify the average IC power dissipation expressed in different forms.

$$P_{DMAX} = V_{CC}^2/2\pi^2 R_L \quad (1)$$

where V_{CC} is the total supply voltage

$$P_{DAVE} = (V_{Opk}/R_L)\,[V_{CC}/\pi - V_{Opk}/2] \quad (2)$$

where V_{CC} is the total supply voltage and $V_{Opk} = V_{CC}/\pi$

$$P_{DAVE} = V_{CC}\,V_{Opk}/\pi\,R_L - V_{Opk}^2/2\,R_L \quad (3)$$

where V_{CC} is the total supply voltage.

Determining the Correct Heat Sink

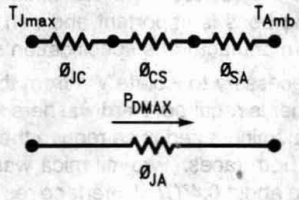
Once the maximum IC power dissipation is known for a given supply voltage, rated load, and the desired rated output power the maximum thermal resistance (in °C/W) of a heat sink can be calculated. This calculation is made using equation (4) and is based on the fact that thermal heat flow parameters are analogous to electrical current flow properties.

It is also known that typically the thermal resistance, θ_{JC} (junction to case), of the LM3875 is 1°C/W and that using Thermalloy Thermacote thermal compound provides a thermal resistance, θ_{CS} (case to heat sink), of about 0.2°C/W as explained in the **Heat Sinking** section.

Referring to the figure below, it is seen that the thermal resistance from the die (junction) to the outside air (ambient) is a combination of three thermal resistances, two of which are known, θ_{JC} and θ_{CS}. Since convection heat flow (power dissipation) is analogous to current flow, thermal resistance is analogous to electrical resistance, and temperature drops are analogous to voltage drops, the power dissipation out of the LM3875 is equal to the following:

$$P_{DMAX} = (T_{Jmax} - T_{Amb})/\theta_{JA}$$

where $\theta_{JA} = \theta_{JC} + \theta_{CS} + \theta_{SA}$



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But since we know P_{DMAX}, θ_{JC}, and θ_{SC} for the application and we are looking for θ_{SA}, we have the following:

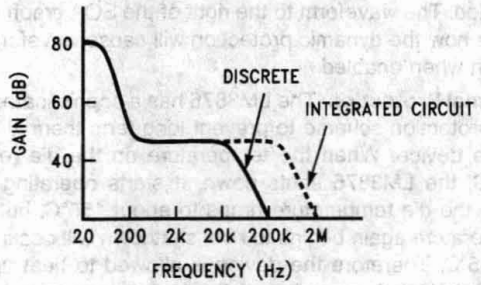
$$\theta_{SA} = [(T_{Jmax} - T_{Amb}) - P_{DMAX}\,(\theta_{JC} + \theta_{CS})]/P_{DMAX} \quad (4)$$

Again it must be noted that the value of θ_{SA} is dependent upon the system designer's amplifier application and its corresponding parameters as described previously. If the ambient temperature that the audio amplifier is to be working under is higher than the normal 25°C, then the thermal resistance for the heat sink, given all other things are equal, will need to be smaller.

Equations (1) and (4) are the only equations needed in the determination of the maximum heat sink thermal resistance. This is, of course, given that the system designer knows the required supply voltages to drive his rated load at a particular power output level and the parameters provided by the semiconductor manufacturer. These parameters are the junction to case thermal resistance, θ_{JC}, T_{Jmax} = 150°C, and the recommended Thermalloy Thermacote thermal compound resistance, θ_{CS}.

SIGNAL-TO-NOISE RATIO

In the measurement of the signal-to-noise ratio, misinterpretations of the numbers actually measured are common. One amplifier may sound much quieter than another, but due to improper testing techniques, they appear equal in measurements. This is often the case when comparing integrated circuit designs to discrete amplifier designs. Discrete transistor amps often "run out of gain" at high frequencies and therefore have small bandwidths to noise as indicated below.



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Integrated circuits have additional open loop gain allowing additional feedback loop gain in order to lower harmonic distortion and improve frequency response. It is this additional bandwidth that can lead to erroneous signal-to-noise measurements if not considered during the measurement process. In the typical example above, the difference in bandwidth appears small on a log scale but the factor of 10 in bandwidth, (200 kHz to 2 MHz) can result in a 10 dB theoretical difference in the signal-to-noise ratio (white noise is proportional to the square root of the bandwidth in a system).

In comparing audio amplifiers it is necessary to measure the magnitude of noise in the audible bandwidth by using a "weighting" filter.[1] A "weighting" filter alters the frequency response in order to compensate for the average human ear's sensitivity to the frequency spectra. The weighting filters at the same time provide the bandwidth limiting as discussed in the previous paragraph.

In addition to noise filtering, differing meter types give different noise readings. Meter responses include:

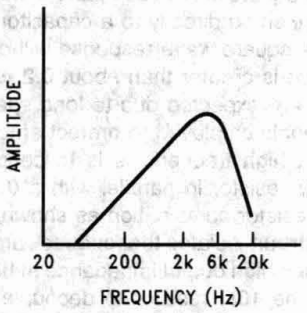
1. RMS reading,
2. average responding,
3. peak reading, and
4. quasi peak reading.

Reference 1: CCIR/ARM: *A Practical Noise Measurement Method*; by Ray Dolby, David Robinson and Kenneth Gundry, AES Preprint No. 1353 (F-3).

Application Information (Continued)

Although theoretical noise analysis is derived using true RMS based calculations, most actual measurements are taken with ARM (Average Responding Meter) test equipment.

Typical signal-to-noise figures are listed for an A-weighted filter which is commonly used in the measurement of noise. The shape of all weighting filters is similar, with the peak of the curve usually occurring in the 3 kHz–7 kHz region as shown below.



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SUPPLY BYPASSING

The LM3875 has excellent power supply rejection and does not require a regulated supply. However, to eliminate possible oscillations all op amps and power op amps should have their supply leads bypassed with low-inductance capacitors having short leads and located close to the package terminals. Inadequate power supply bypassing will manifest itself by a low frequency oscillation known as "motorboating" or by high frequency instabilities. These instabilities can be eliminated through multiple bypassing utilizing a large tantalum or electrolytic capacitor (10 μF or larger) which is used to absorb low frequency variations and a small ceramic capacitor (0.1 μF) to prevent any high frequency feedback through the power supply lines.

If adequate bypassing is not provided the current in the supply leads which is a rectified component of the load current may be fed back into internal circuitry. This signal causes low distortion at high frequencies requiring that the supplies be bypassed at the package terminals with an electrolytic capacitor of 470 μF or more.

LEAD INDUCTANCE

Power op amps are sensitive to inductance in the output lead, particularly with heavy capacitive loading. Feedback to the input should be taken directly from the output terminal, minimizing common inductance with the load.

Lead inductance can also cause voltage surges on the supplies. With long leads to the power supply, energy is stored in the lead inductance when the output is shorted. This energy can be dumped back into the supply bypass capacitors when the short is removed. The magnitude of this transient is reduced by increasing the size of the bypass capacitor near the IC. With at least a 20 μF local bypass, these voltage surges are important only if the lead length exceeds a couple feet (>1 μH lead inductance). Twisting together the supply and ground leads minimizes the effect.

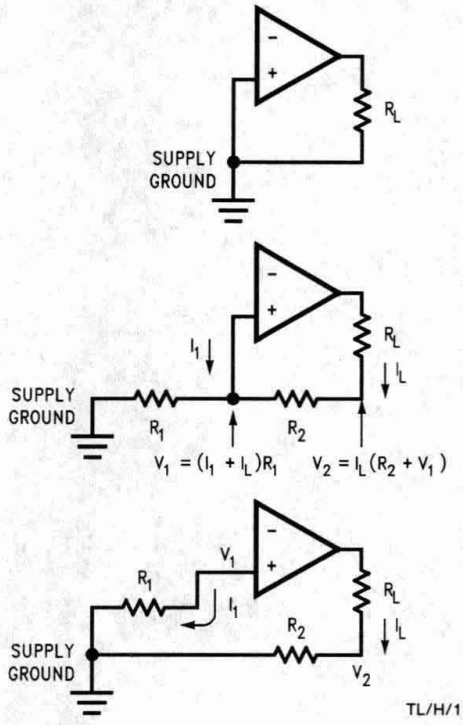
LAYOUT, GROUND LOOPS AND STABILITY

The LM3875 is designed to be stable when operated at a closed-loop gain of 10 or greater, but as with any other high-current amplifier, the LM3875 can be made to oscillate under certain conditions. These usually involve printed circuit board layout or output/input coupling.

When designing a layout, it is important to return the load ground, the output compensation ground, and the low level (feedback and input) grounds to the circuit board common ground point through separate paths. Otherwise, large currents flowing along a ground conductor will generate voltages on the conductor which can effectively act as signals at the input, resulting in high frequency oscillation or excessive distortion. It is advisable to keep the output compensation components and the 0.1 μF supply decoupling capacitors as close as possible to the LM3875 to reduce the effects of PCB trace resistance and inductance. For the same reason, the ground return paths should be as short as possible.

In general, with fast, high-current circuitry, all sorts of problems can arise from improper grounding which again can be avoided by returning all grounds separately to a common point. Without isolating the ground signals and returning the grounds to a common point, ground loops may occur.

"Ground Loop" is the term used to describe situations occurring in ground systems where a difference in potential exists between two ground points. Ideally a ground is a ground, but unfortunately, in order for this to be true, ground conductors with zero resistance are necessary. Since real world ground leads possess finite resistance, currents running through them will cause finite voltage drops to exist. If two ground return lines tie into the same path at different points there will be a voltage drop between them. The first figure below shows a common ground example where the positive input ground and the load ground are returned to the supply ground point via the same wire. The addition of the finite wire resistance, R_2, results in a voltage difference between the two points as shown below.



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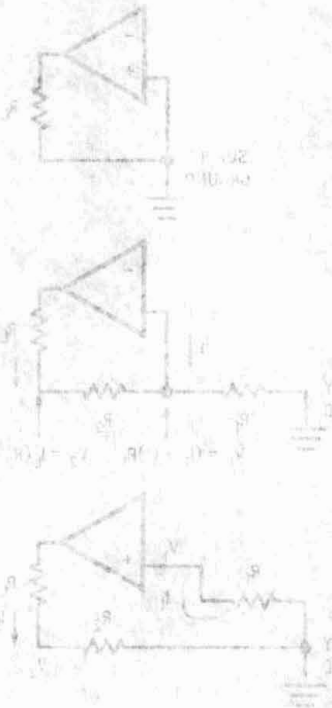
Application Information (Continued)

The load current I_L will be much larger than input bias current I_1, thus V_1 will follow the output voltage directly, i.e., in phase. Therefore the voltage appearing at the non-inverting input is effectively positive feedback and the circuit may oscillate. If there were only one device to worry about then the values of R_1 and R_2 would probably be small enough to be ignored; however, several devices normally comprise a total system. Any ground return of a separate device, whose output is in phase, can feedback in a similar manner and cause instabilities. Out of phase ground loops also are troublesome, causing unexpected gain and phase errors.

The solution to most ground loop problems is to always use a single-point ground system, although this is sometimes impractical. The third figure above is an example of a single-point ground system.

The single-point ground concept should be applied rigorously to all components and all circuits when possible. Violations of single-point grounding are most common among printed circuit board designs, since the circuit is surrounded by large ground areas which invite the temptation to run a device to the closest ground spot. As a final rule, make all ground returns low resistance and low inductance by using large wire and wide traces.

Occasionally, current in the output leads (which function as antennas) can be coupled through the air to the amplifier input, resulting in high-frequency oscillation. This normally happens when the source impedance is high or the input leads are long. The problem can be eliminated by placing a small capacitor, C_C, (on the order of 50 pF–500 pF) across the LM3875 input terminals. Refer to the **External Components Description** section relating to component interaction with C_f.



REACTIVE LOADING

It is hard for most power amplifiers to drive highly capacitive loads very effectively and normally results in oscillations or ringing on the square wave response. If the output of the LM3875 is connected directly to a capacitor with no series resistance, the square wave response will exhibit ringing if the capacitance is greater than about 0.2 μF. If highly capacitive loads are expected due to long speaker cables, a method commonly employed to protect amplifiers from low impedances at high frequencies is to couple to the load through a 10Ω resistor in parallel with a 0.7 μH inductor. The inductor-resistor combination as shown in the **Typical Application Circuit** isolates the feedback amplifier from the load by providing high output impedance at high frequencies thus allowing the 10Ω resistor to decouple the capacitive load and reduce the Q of the series resonant circuit. The LR combination also provides low output impedance at low frequencies thus shorting out the 10Ω resistor and allowing the amplifier to drive the series RC load (large capacitive load due to long speaker cables) directly.

Application Information (Continued)

GENERALIZED AUDIO POWER AMPLIFIER DESIGN

The system designer usually knows some of the following parameters when starting an audio amplifier design:

Desired Power Output	Input Level
Input Impedance	Load Impedance
Maximum Supply Voltage	Bandwidth

The power output and load impedance determine the power supply requirements, however, depending upon the application some system designers may be limited to certain maximum supply voltages. If the designer does have a power supply limitation, he should choose a practical load impedance which would allow the amplifier to provide the desired output power, keeping in mind the current limiting capabilities of the device. In any case, the output signal swing and current are found from (where P_O is the average output power):

$$V_{opeak} = \sqrt{2 R_L P_O} \quad (1)$$

$$I_{opeak} = \sqrt{(2 P_O)/R_L} \quad (2)$$

To determine the maximum supply voltage the following parameters must be considered. Add the dropout voltage (5 volts for LM3875) to the peak output swing, V_{opeak}, to get the supply rail value, (i.e. + V_{opeak} + Vod) at a current of I_{opeak}). The regulation of the supply determines the unloaded voltage, usually about 15% higher. Supply voltage will also rise 10% during high line conditions. Therefore, the maximum supply voltage is obtained from the following equation:

$$\text{max. supplies} \approx \pm (V_{opeak} + \text{Vod}(1 + \text{regulation})(1.1) \quad (3)$$

The input sensitivity and the output power specs determine the minimum required gain as depicted below:

$$A_V \geq (\sqrt{P_O R_L})/(V_{IN}) = V_{orms}/V_{inrms} \quad (4)$$

Normally the gain is set between 20 and 200; for a 40W, 8Ω audio amplifier this results in a sensitivity of 894 mV and 89 mV, respectively. Although higher gain amplifiers provide greater output power and dynamic headroom capabilities, there are certain shortcomings that go along with the so called "gain". The input referred noise floor is increased and hence the SNR is worse. With the increase in gain, there is also a reduction of the power bandwidth which results in a decrease in feedback thus not allowing the amplifier to respond as quickly to nonlinearities. This decreased ability to respond to nonlinearities increases the THD + N specification.

The desired input impedance is set by R_{IN}. Very high values can cause board layout problems and DC offsets at the output. The value for the feedback resistance, R_{f1}, should be chosen to be a relatively large value (10 kΩ–100 kΩ), and the other feedback resistance, Ri, is calculated using standard op amp configuration gain equations. Most audio amplifiers are designed from the non-inverting amplifier configuration.

DESIGN A 40W/8Ω AUDIO AMPLIFIER

Given:

Power Output	40W
Load Impedance	8Ω
Input Level	$1V_{(max)}$
Input Impedance	100 kΩ
Bandwidth	20 Hz–20 kHz ±0.25 dB

Equation (1) and (2) give:

40W/8Ω $V_{opeak} = 25.3V$ $I_{opeak} = 3.16A$

Therefore the supply required is: ±30.3V @3.16A

With 15% regulation and high line the final supply voltage is ±38.3V using equation (3). At this point it is a good idea to check the Power Output vs Supply Voltage to ensure that the required output power is obtainable from the device while maintaining low THD + N. It is also good to check the Power Dissipation vs Supply Voltage to ensure that the device can handle the internal power dissipation. At the same time designing in a relatively practical sized heat sink with a low thermal resistance is also important. Refer to **Typical Performance Characteristics** graphs and the **Thermal Considerations** section for more information.

The minimum gain from equation (4) is: $A_V \geq 18$

We select a gain of 21 (Non-Inverting Amplifier); resulting in a sensitivity of 894 mV.

Letting R_{IN} equal 100 kΩ gives the required input impedance, however, this would eliminate the "volume control" unless an additional input impedance was placed in series with the 10 kΩ potentiometer that is depicted in *Figure 1*. Adding the additional 100 kΩ resistor would ensure the minimum required input impedance.

For low DC offsets at the output we let $R_{f1} = 100\ k\Omega$. Solving for Ri (Non-Inverting Amplifier) gives the following:

$$Ri = R_{f1}/(A_V - 1) = 100k/(21 - 1) = 5\ k\Omega; \text{ use } 5.1\ k\Omega$$

The bandwidth requirement must be stated as a pole, i.e., the 3 dB frequency. Five times away from a pole give 0.17 dB down, which is better than the required 0.25 dB. Therefore:

$$f_L = 20\ Hz/5 = 4\ Hz$$

$$f_H = 20\ kHz \times 5 = 100\ kHz$$

At this point, it is a good idea to ensure that the Gain Bandwidth Product for the part will provide the designed gain out to the upper 3 dB point of 100 kHz. This is why the minimum GBWP of the LM3875 is important.

$$GBWP = A_V \times f3\ dB = 21 \times 100\ kHz = 2.1\ MHz$$

$$GBWP = 2.0\ MHz\ (min)\ for\ LM3875$$

Solving for the low frequency roll-off capacitor, Ci, we have:

$$Ci > 1/(2\pi\ Ri\ f_L) = 7.8\ \mu F; \text{ use } 10\ \mu F.$$

Definition of Terms

Input Offset Voltage: The absolute value of the voltage which must be applied between the input terminals through two equal resistances to obtain zero output voltage and current.

Input Bias Current: The absolute value of the average of the two input currents with the output voltage and current at zero.

Input Offset Current: The absolute value of the difference in the two input currents with the output voltage and current at zero.

Input Common-Mode Voltage Range (or Input Voltage Range): The range of voltages on the input terminals for which the amplifier is operational. Note that the specifications are not guaranteed over the full common-mode voltage range unless specifically stated.

Common-Mode Rejection: The ratio of the input common-mode voltage range to the peak-to-peak change in input offset voltage over this range.

Power Supply Rejection: The ratio of the change in input offset voltage to the change in power supply voltages producing it.

Quiescent Supply Current: The current required from the power supply to operate the amplifier with no load and the output voltage and current at zero.

Slew Rate: The internally limited rate of change in output voltage with a large amplitude step function applied to the input.

Class B Amplifier: The most common type of audio power amplifier that consists of two output devices each of which conducts for 180° of the input cycle. The LM3875 is a Quasi-AB type amplifier.

Crossover Distortion: Distortion caused in the output stage of a class B amplifier. It can result from inadequate bias current providing a dead zone where the output does not respond to the input as the input cycle goes through its zero crossing point. Also for ICs an inadequate frequency response of the output PNP device can cause a turn-on delay giving crossover distortion on the negative going transistion through zero crossing at the higher audio frequencies.

THD + N: Total Harmonic Distortion plus Noise refers to the measurement technique in which the fundamental component is removed by a bandreject (notch) filter and all remaining energy is measured including harmonics and noise.

Signal-to-Noise Ratio: The ratio of a system's output signal level to the system's output noise level obtained in the absence of a signal. The output reference signal is either specified or measured at a specified distortion level.

Continuous Average Output Power: The minimum sine wave continuous average power output in watts (or dBW) that can be delivered into the rated load, over the rated bandwidth, at the rated maximum total harmonic distortion.

Music Power: A measurement of the peak output power capability of an amplifier with either a signal duration sufficiently short that the amplifier power supply does not sag during the measurement, or when high quality external power supplies are used. This measurement (an IHF standard) assumes that with normal music program material the amplifier power supplies will sag insignificantly.

Peak Power: Most commonly referred to as the power output capability of an amplifier that can be delivered to the load; specified by the part's maximum voltage swing.

Headroom: The margin between an actual signal operating level (usually the power rating of the amplifier with particular supply voltages, a rated load value, and a rated THD + N figure) and the level just before clipping distortion occurs, expressed in decibels.

Large Signal Voltage Gain: The ratio of the output voltage swing to the differential input voltage required to drive the output from zero to either swing limit. The output swing limit is the supply voltage less a specified quasi-saturation voltage. A pulse of short enough duration to minimize thermal effects is used as a measurement signal.

Output-Current Limit: The output current with a fixed output voltage and a large input overdrive. The limiting current drops with time once SPiKe protection circuitry is activated.

Output Saturation Threshold (Clipping Point): The output swing limit for a specified input drive beyond that required for zero output. It is measured with respect to the supply to which the output is swinging.

Output Resistance: The ratio of the change in output voltage to the change in output current with the output around zero.

Power Dissipation Rating: The power that can be dissipated for a specified time interval without activating the protection circuitry. For time intervals in excess of 100 ms, dissipation capability is determined by heat sinking of the IC package rather than by the IC itself.

Thermal Resistance: The peak, junction-temperature rise, per unit of internal power dissipation (units in °C/W), above the case temperature as measured at the center of the package bottom.

The DC thermal resistance applies when one output transistor is operating continuously. The AC thermal resistance applies with the output transistors conducting alternately at a high enough frequency that the peak capability of neither transistor is exceeded.

Power Bandwidth: The power bandwidth of an audio amplifier is the frequency range over which the amplifier voltage gain does not fall below 0.707 of the flat band voltage gain specified for a given load and output power.

Power bandwidth also can be measured by the frequencies at which a specified level of distortion is obtained while the amplifier delivers a power output 3 dB below the rated output. For example, an amplifier rated at 60W with ≤0.25% THD + N, would make its power bandwidth measured as the difference between the upper and lower frequencies at which 0.25% distortion was obtained while the amplifier was delivering 30W.

Gain-Bandwidth Product: The Gain-Bandwidth Product is a way of predicting the high-frequency usefulness of an op amp. The Gain-Bandwidth Product is sometimes called the unity-gain frequency or unity-gain cross frequency because the open-loop gain characteristic passes through or crosses unity gain at this frequency. Simply, we have the following relationship:

$$A_{CL1} \times f_1 = A_{CL2} \times f_2$$

Assuming that at unity-gain

$$(A_{CL1} = 1 \text{ or } 0 \text{ dB})\ fu = f_1 = GBWP,$$

then we have the following:

$$GBWP = A_{CL2} \times f_2$$

Definition of Terms (Continued)

This says that once fu (GBWP) is known for an amplifier, then the open-loop gain can be found at any frequency. This is also an excellent equation to determine the 3 dB point of a closed-loop gain, assuming that you know the GBWP of the device. Refer to the diagram below.

Bi-amplification: The technique of splitting the audio frequency spectrum into two sections and using individual power amplifiers to drive a separate woofer and tweeter. Crossover frequencies for the amplifiers usually vary between 500 Hz and 1600 Hz. "Biamping" has the advantages of allowing smaller power amps to produce a given sound pressure level and reducing distortion effects produced by overdrive in one part of the frequency spectrum affecting the other part.

C.C.I.R./A.R.M.:

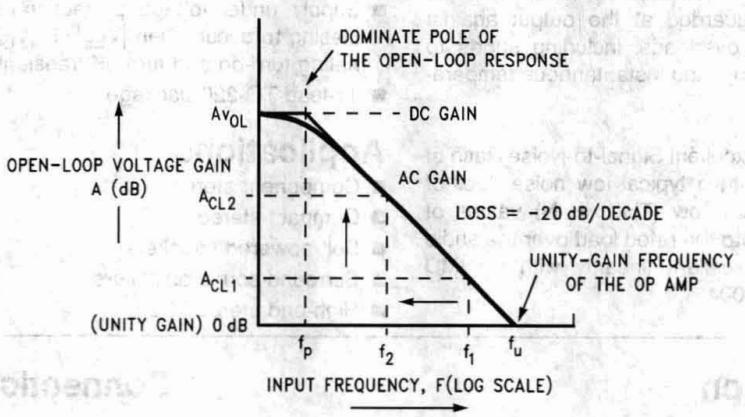
Literally: International Radio Consultative Committee
Average Responding Meter

This refers to a weighted noise measurement for a Dolby B type noise reduction system. A filter characteristic is used that gives a closer correlation of the measurement with the subjective annoyance of noise to the ear. Measurements made with this filter cannot necessarily be related to unweighted noise measurements by some fixed conversion factor since the answers obtained will depend on the spectrum of the noise source.

S.P.L.: Sound Pressure Level—usually measured with a microphone/meter combination calibrated to a pressure level of 0.0002 μBars (approximately the threshold hearing level).

$$S.P.L. = 20 \text{ Log } 10P/0.0002 \text{ dB}$$

Where P is the R.M.S sound pressure in microbars. (1 Bar = 1 atmosphere = 14.5 lb./in^2 = 194 dB S.P.L.).



TL/H/11449–14

National Semiconductor

LM3876 *Overture*™ Audio Power Amplifier Series
High-Performance 56W Audio Power Amplifier w/Mute

General Description

The LM3876 is a high-performance audio power amplifier capable of delivering 56W of continuous average power to an 8Ω load with 0.1% (THD + N) from 20 Hz–20 kHz.

The performance of the LM3876, utilizing its Self Peak Instantaneous Temperature (°Ke) (**SPiKe**™) Protection Circuitry, puts it in a class above discrete and hybrid amplifiers by providing an inherently, dynamically protected Safe Operating Area (SOA). **SPiKe** Protection means that these parts are completely safeguarded at the output against overvoltage, undervoltage, overloads, including shorts to the supplies, thermal runaway, and instantaneous temperature peaks.

The LM3876 maintains an excellent Signal-to-Noise Ratio of greater than 95 dB(min) with a typical low noise floor of 2.0 μV. It exhibits extremely low (THD + N) values of 0.06% at the rated output into the rated load over the audio spectrum, and provides excellent linearity with an IMD (SMPTE) typical rating of 0.004%.

Features

- 56W continuous average output power into 8Ω
- 100W instantaneous peak output power capability
- Signal-to-Noise Ratio ≥ 95 dB(min)
- An input mute function
- Output protection from a short to ground or to the supplies via internal current limiting circuitry
- Output over-voltage protection against transients from inductive loads
- Supply under-voltage protection, not allowing internal biasing to occur when $|V_{EE}| + |V_{CC}| \leq 12V$, thus eliminating turn-on and turn-off transients
- 11-lead TO-220 package

Applications

- Component stereo
- Compact stereo
- Self-powered speakers
- Surround-sound amplifiers
- High-end stereo TVs

Typical Application

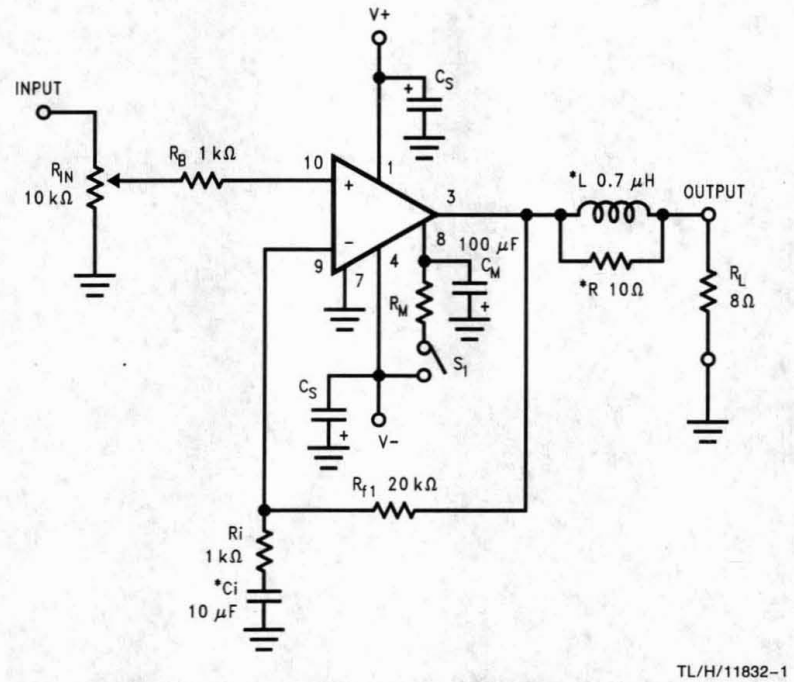


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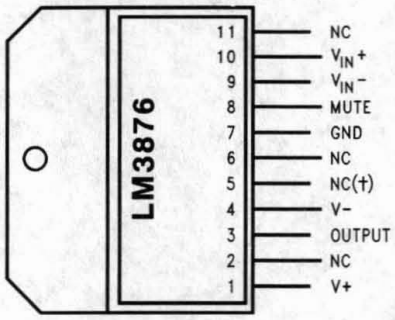
FIGURE 1. Typical Audio Amplifier Application Circuit

*Optional components dependent upon specific design requirements. Refer to the External Components Description section for a component functional description.

Connection Diagram

Plastic Package (Note 8)



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Top View
Order Number LM3876T
or LM3876TF
See NS Package Number TA11B for Staggered Lead Non-Isolated Package or TF11B for Staggered Lead Isolated Package

†Connect Pin 5 to V+ for Compatibility with LM3886.

Absolute Maximum Ratings (Notes 1, 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage $\|V^+\| + \|V^-\|$ (No Signal)	94V
Supply Voltage $\|V^+\| + \|V^-\|$ (Input Signal)	84V
Common Mode Input Voltage	(V^+ or V^-) and $\|V^+\| + \|V^-\| \leq 80V$
Differential Input Voltage	60V
Output Current	Internally Limited
Power Dissipation (Note 3)	125W
ESD Susceptibility (Note 4)	3000V
Junction Temperature (Note 5)	150°C
Soldering Information	
T Package (10 seconds)	260°C
Storage Temperature	−40°C to +150°C
Thermal Resistance	
θ_{JC}	1°C/W
θ_{JA}	43°C/W

Operating Ratings (Notes 1, 2)

Temperature Range	
$T_{MIN} \leq T_A \leq T_{MAX}$	$-20°C \leq T_A \leq +85°C$
Supply Voltage $\|V^+\| + \|V^-\|$	24V to 84V

Note: Operation is guaranteed up to 84V, however, distortion may be introduced from **SPiKe** Protection Circuitry when operating above 70V if proper thermal considerations are not taken into account. Refer to the **Thermal Considerations** section for more information.

(See **SPiKe** Protection Response)

Electrical Characteristics (Notes 1, 2) The following specifications apply for $V^+ = +35V$, $V^- = -35V$, $I_{MUTE} = -0.5$ mA with $R_L = 8\Omega$ unless otherwise specified. Limits apply for $T_A = 25°C$.

Symbol	Parameter	Conditions	LM3876		Units (Limits)
			Typical (Note 6)	Limit (Note 7)	
$\|V^+\| + \|V^-\|$	Power Supply Voltage (Note 10)	$V_{pin7} - V^- \geq 9V$	18	24 84	V (min) V (max)
A_M	Mute Attenuation	Pin 8 Open or at 0V, Mute: On Current out of Pin 8 > 0.5 mA, Mute: Off	120	80	dB (min)
**P_O	Output Power (Continuous Average)	THD + N = 0.1% (max) f = 1 kHz; f = 20 kHz	56	40	W (min)
Peak P_O	Instantaneous Peak Output Power		100		W
THD + N	Total Harmonic Distortion Plus Noise	40W, 20 Hz ≤ f ≤ 20 kHz A_V = 26 dB	0.06		%
**SR	Slew Rate (Note 9)	V_{IN} = 1.2 Vrms, f = 10 kHz, Square-Wave, $R_L = 2 k\Omega$	11	5	V/μs (min)
*I^+	Total Quiescent Power Supply Current	$V_{CM} = 0V$, $V_o = 0V$, $I_o = 0A$, $I_{mute} = 0A$	30	70	mA (max)
*V_{OS}	Input Offset Voltage	$V_{CM} = 0V$, $I_o = 0$ mA	1	15	mV (max)
I_B	Input Bias Current	$V_{CM} = 0V$, $I_o = 0$ mA	0.2	1	μA (max)
I_{OS}	Input Offset Current	$V_{CM} = 0V$, $I_o = 0$ mA	0.01	0.2	μA (max)
I_o	Output Current Limit	$\|V^+\| = \|V^-\| = 12V$, $t_{ON} = 10$ ms, $V_O = 0V$	6	4	A (min)
*V_{od}	Output Dropout Voltage (Note 11)	$\|V^+ - V_O\|$, $V^+ = 20V$, $I_o = +100$ mA $\|V_O - V^-\|$, $V^- = -20V$, $I_o = -100$ mA	1.6 2.7	5 5	V (max) V (max)
*PSRR	Power Supply Rejection Ratio	$V^+ = 40V$ to 20V, $V^- = -40V$, $V_{CM} = 0V$, $I_o = 0$ mA	120	85	dB (min)
		$V^+ = 40V$, $V^- = -40V$ to $-20V$, $V_{CM} = 0V$, $I_o = 0$ mA	120	85	dB (min)

*DC Electrical Test; refer to Test Circuit #1.

**AC Electrical Test; refer to Test Circuit #2.

Electrical Characteristics (Notes 1, 2)

The following specifications apply for $V^+ = +35V$, $V^- = -35V$, $I_{MUTE} = -0.5$ mA with $R_L = 8\Omega$ unless otherwise specified. Limits apply for $T_A = 25°C$. (Continued)

Symbol	Parameter	Conditions	LM3876		Units (Limits)
			Typical (Note 6)	Limit (Note 7)	
*CMRR	Common Mode Rejection Ratio	$V^+ = 60V$ to $20V$, $V^- = -20V$ to $-60V$, $V_{CM} = 20V$ to $-20V$, $I_o = 0$ mA	120	80	dB (min)
*A_{VOL}	Open Loop Voltage Gain	$\|V^+\| = \|V^-\| = 40V$, $R_L = 2\ k\Omega$, $\Delta V_O = 60V$	120	90	dB (min)
GBWP	Gain-Bandwidth Product	$\|V^+\| = \|V^-\| = 40V$ $f_O = 100$ kHz, $V_{IN} = 50$ mVrms	8	2	MHz (min)
**e_{IN}	Input Noise	IHF—A Weighting Filter $R_{IN} = 600\Omega$ (Input Referred)	2.0	8	μV (max)
SNR	Signal-to-Noise Ratio	$P_O = 1W$, A-Weighted, Measured at 1 kHz, $R_S = 25\Omega$	98		dB
		$P_O = 40W$, A-Weighted, Measured at 1 kHz, $R_S = 25\Omega$	114		dB
		Ppk = 100W, A-Weighted, Measured at 1 kHz, $R_S = 25\Omega$	122		dB
IMD	Intermodulation Distortion Test	60 Hz, 7 kHz, 4:1 (SMPTE) 60 Hz, 7 kHz, 1:1 (SMPTE)	0.004 0.006		%

*DC Electrical Test; refer to Test Circuit #1.

**AC Electrical Test; refer to Test Circuit #2.

Note 1: All voltages are measured with respect to the GND pin (pin 7), unless otherwise specified.

Note 2: *Absolute Maximum Ratings* indicate limits beyond which damage to the device may occur. *Operating Ratings* indicate conditions for which the device is functional, but do not guarantee specific performance limits. *Electrical Characteristics* state DC and AC electrical specifications under particular test conditions which guarantee specific performance limits. This assumes that the device is within the Operating Ratings. Specifications are not guaranteed for parameters where no limit is given, however, the typical value is a good indication of device performance.

Note 3: For operating at case temperatures above 25°C, the device must be derated based on a 150°C maximum junction temperature and a thermal resistance of $\theta_{JC} = 1.0$ °C/W (junction to case). Refer to the Thermal Resistance figure in the Application Information section under **Thermal Considerations**.

Note 4: Human body model, 100 pF discharged through a 1.5 kΩ resistor.

Note 5: The operating junction temperature maximum is 150°C, however, the instantaneous Safe Operating Area temperature is 250°C.

Note 6: Typicals are measured at 25°C and represent the parametric norm.

Note 7: Limits are guaranteed to National's AOQL (Average Outgoing Quality Level).

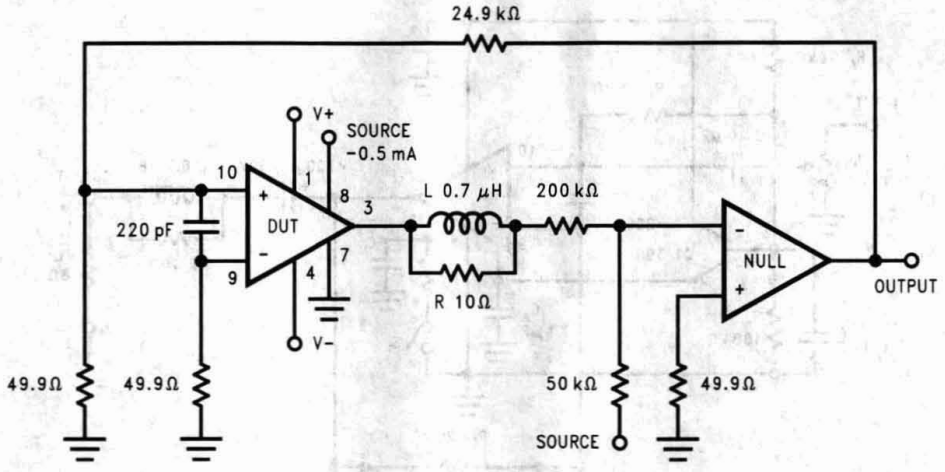
Note 8: The LM3876T package TA11B is a non-isolated package, setting the tab of the device and the heat sink at V^- potential when the LM3876 is directly mounted to the heat sink using only thermal compound. If a mica washer is used in addition to thermal compound, θ_{CS} (case to sink) is increased, but the heat sink will be isolated from V^-.

Note 9: The feedback compensation network limits the bandwidth of the closed-loop response and so the slew rate will be reduced due to the high frequency roll-off. Without feedback compensation, the slew rate is typically 16V/μs.

Note 10: V^- must have at least $-9V$ at its pin with reference to ground in order for the under-voltage protection circuitry to be disabled.

Note 11: The output dropout voltage is the supply voltage minus the clipping voltage. Refer to the Clipping Voltage vs Supply Voltage graph in the **Typical Performance Characteristics** section.

Test Circuit # 1 *(DC Electrical Test Circuit)



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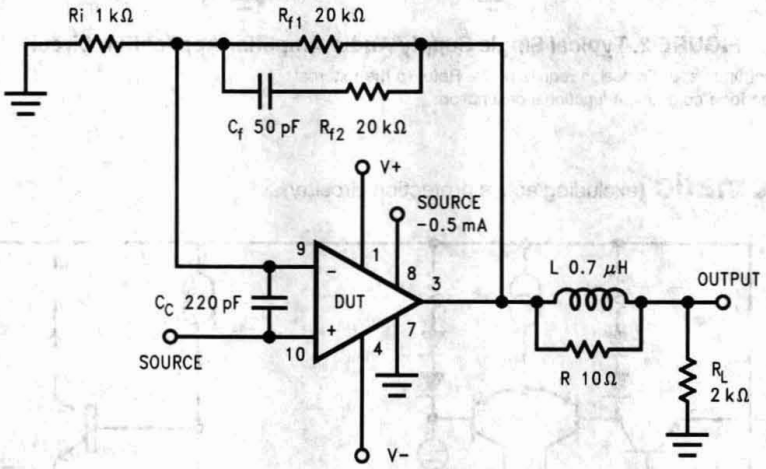
Test Circuit # 2 **(AC Electrical Test Circuit)



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Single Supply Application Circuit

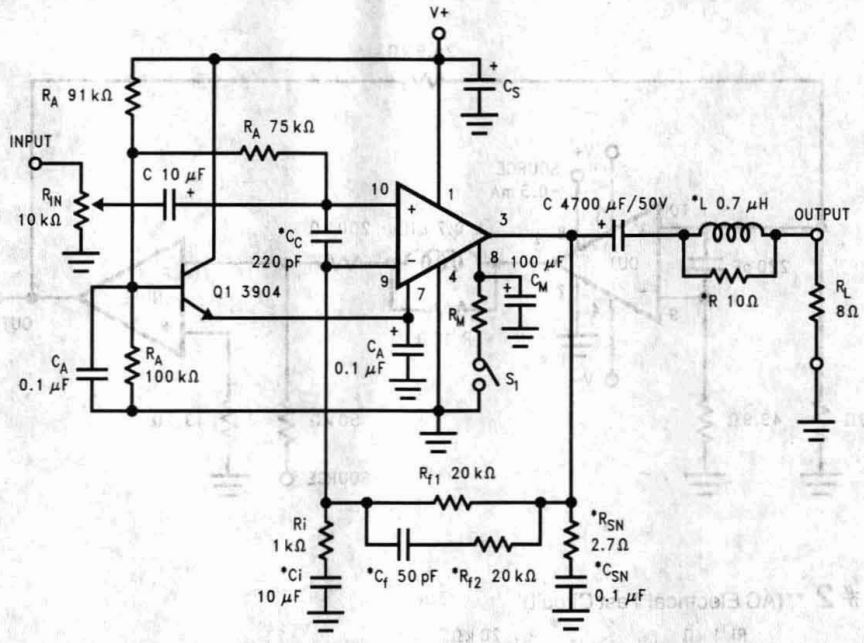

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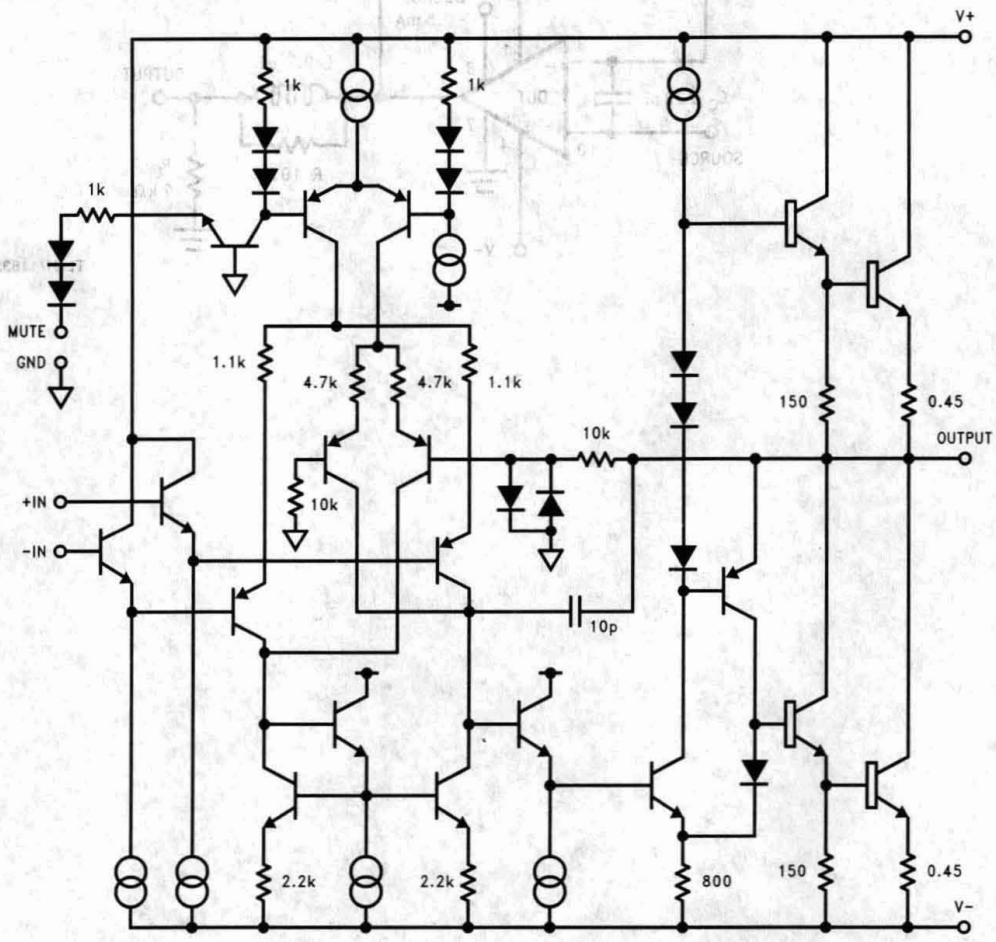
FIGURE 2. Typical Single Supply Audio Amplifier Application Circuit

*Optional components dependent upon specific design requirements. Refer to the External Components Description section for a component functional description.

Equivalent Schematic (excluding active protection circuitry)



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External Components Description (*Figures 1* and *2*)

Components		Functional Description
1.	R_{IN}	Acts as a volume control by setting the voltage level allowed to the amplifier's input terminals.
2.	R_A	Provides DC voltage biasing for the single supply operation and bias current for the positive input terminal.
3.	C_A	Provides bias filtering.
4.	C	Provides AC coupling at the input and output of the amplifier for single supply operation.
5.	R_B	Prevents currents from entering the amplifier's non-inverting input which may be passed through to the load upon power-down of the system due to the low input impedance of the circuitry when the under-voltage circuitry is off. This phenomenon occurs when the supply voltages are below 1.5V.
6.	*C_C	Reduces the gain (bandwidth of the amplifier) at high frequencies to avoid quasi-saturation oscillations of the output transistor. The capacitor also suppresses external electromagnetic switching noise created from fluorescent lamps.
7.	Ri	Inverting input resistance to provide AC Gain in conjunction with R_{f1}.
8.	*Ci	Feedback capacitor. Ensures unity gain at DC. Also a low frequency pole (highpass roll-off) at: $f_c = 1/(2\pi Ri\ Ci)$
9.	R_{f1}	Feedback resistance to provide AC Gain in conjunction with Ri.
10.	*R_{f2}	At higher frequencies feedback resistance works with C_f to provide lower AC Gain in conjunction with R_{f1} and Ri. A high frequency pole (lowpass roll-off) exists at: $f_c = [R_{f1}\ R_{f2}\ (s + 1/R_{f2}C_f)]/[(R_{f1} + R_{f2})(s + 1/C_f(R_{f1} + R_{f2}))]$
11.	*C_f	Compensation capacitor that works with R_{f1} and R_{f2} to reduce the AC Gain at higher frequencies.
12.	R_M	Mute resistance set up to allow 0.5 mA to be drawn from pin 8 to turn the muting function off. → R_M is calculated using: $R_M \leq (\lvert V_{EE}\rvert - 2.6V)/I8$ where $I8 \geq 0.5$ mA. Refer to the Mute Attenuation vs Mute Current curves in the Typical Performance Characteristics section.
13.	C_M	Mute capacitance set up to create a large time constant for turn-on and turn-off muting.
14.	*R_{SN}	Works with C_{SN} to stabilize the output stage by creating a pole that eliminates high frequency oscillations.
15.	*C_{SN}	Works with R_{SN} to stabilize the output stage by creating a pole that eliminates high frequency oscillations. $f_c = 1/(2\pi R_{SN}C_{SN})$
16.	*L	Provides high impedance at high frequecies so that R may decouple a highly capacitive load
17.	*R	and reduce the Q of the series resonant circuit due to capacitive load. Also provides a low impedance at low frequencies to short out R and pass audio signals to the load.
18.	C_S	Provides power supply filtering and bypassing.
19.	S1	Mute switch that mutes the music going into the amplifier when opened.

*Optional components dependent upon specific design requirements. Refer to the Application Information section for more information.

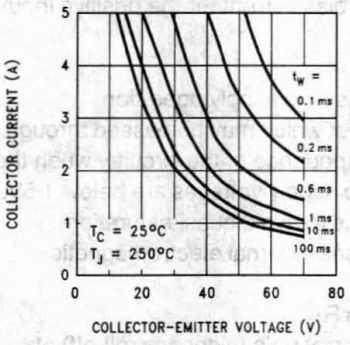
OPTIONAL EXTERNAL COMPONENT INTERACTION

Although the optional external components have specific desired functions that are designed to reduce the bandwidth and eliminate unwanted high frequency oscillations they may cause certain undesirable effects when they interact. Interaction may occur for components whose reactances are in close proximity to one another. One example would be the coupling capacitor, C_C, and the compensation capacitor, Cf. These two components act as low impedances to certain frequencies which will couple signals from the input to the output. Please take careful note of basic amplifier component functionality when designing in these components.

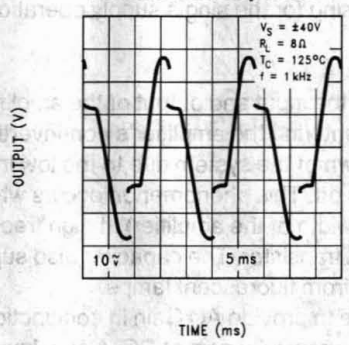
The optional external components shown in *Figure 2* and described above are applicable in both single and split voltage supply configurations.

Typical Performance Characteristics

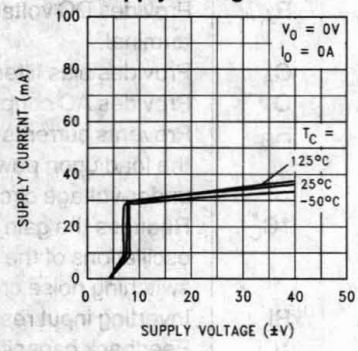
Safe Area



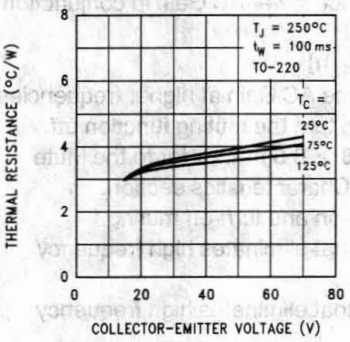
SPiKe Protection Response



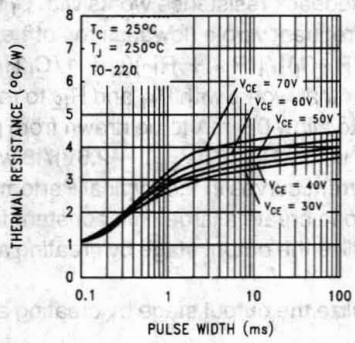
Supply Current vs Supply Voltage



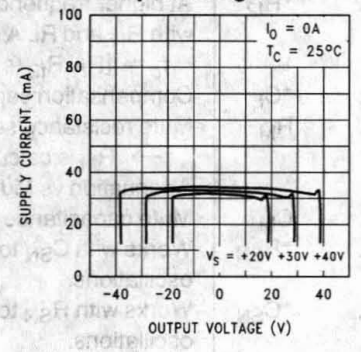
Pulse Thermal Resistance



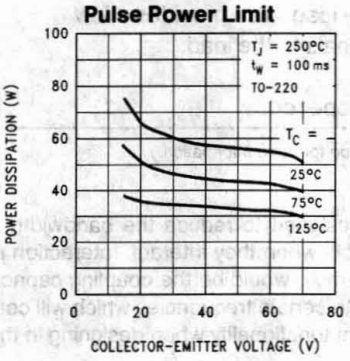
Pulse Thermal Resistance



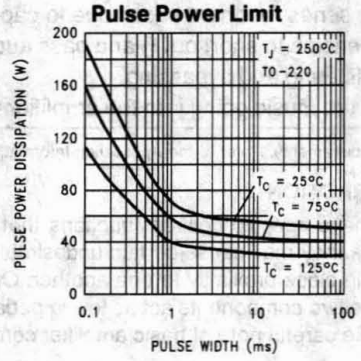
Supply Current vs Output Voltage



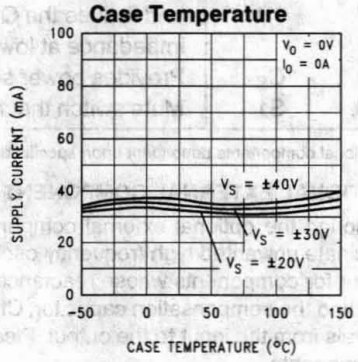
Pulse Power Limit



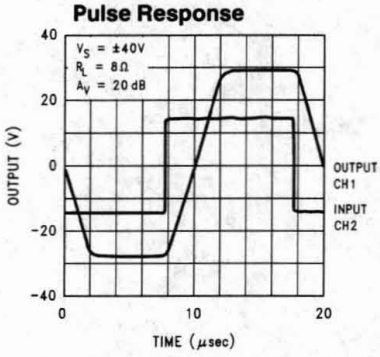
Pulse Power Limit



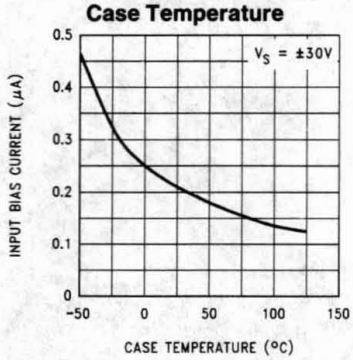
Supply Current vs Case Temperature



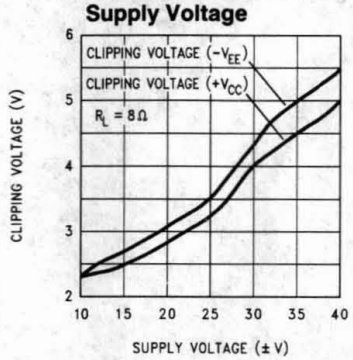
Pulse Response



Input Bias Current vs Case Temperature



Clipping Voltage vs Supply Voltage



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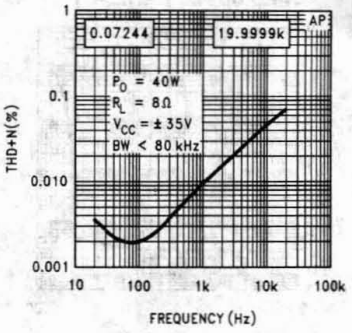
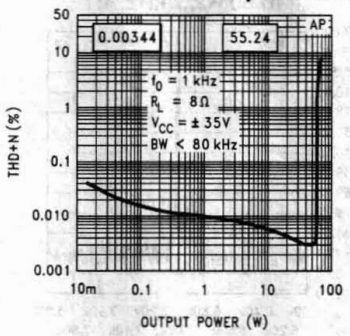
Typical Performance Characteristics (Continued)

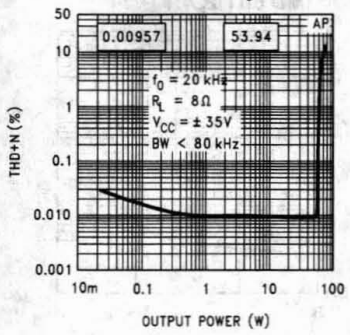
THD + N vs Frequency



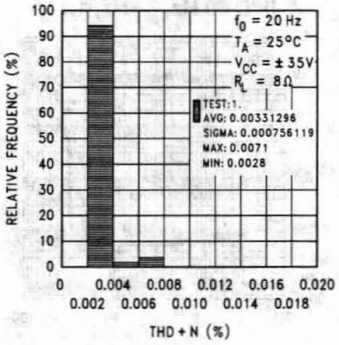
THD + N vs Output Power



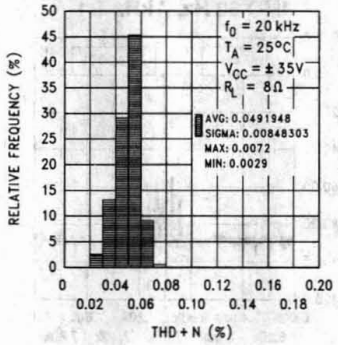
THD + N vs Output Power



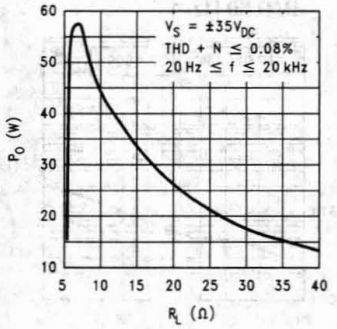
THD + N Distribution



THD + N Distribution



Output Power vs Load Resistance



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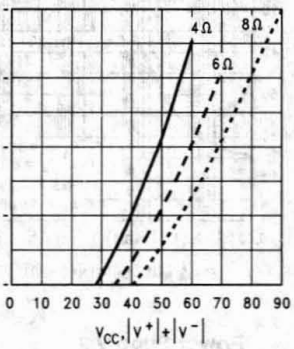
Max Heatsink Thermal Resistance (°C/W) at the Specified Ambient Temperature (°C)

T_A = 25°C	40	50	60	70	80	90	100	110	T_C, °C	P_D, W
1.3	1.0								90	50
1.6	1.2	1.0							96	45
1.9	1.6	1.3	1.1						102	40
2.4	1.9	1.7	1.4	1.1					108	35
3.0	2.5	2.1	1.8	1.5	1.1				114	30
3.8	3.2	2.8	2.4	2.0	1.6	1.2			120	25
5.1	4.3	3.8	3.3	2.8	2.3	1.8	1.3		126	20
7.1	6.1	5.5	4.8	4.1	3.5	2.8	2.1	1.5	132	15
11.3	9.8	8.8	7.8	6.8	5.8	4.8	3.8	2.8	138	10

Note: The maximum heat sink thermal resistance values, $\varnothing_{SA}$, in the table above were calculated using a $\varnothing_{CS}$ = 0.2°C/W due to thermal compound.

P_{Dmax} vs Supply Voltage



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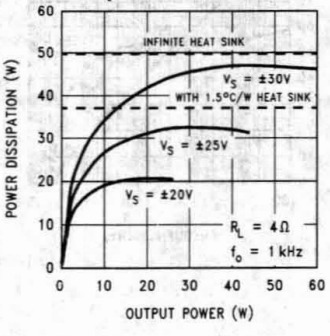
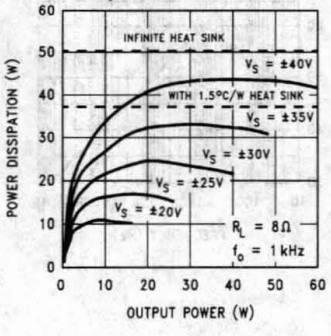
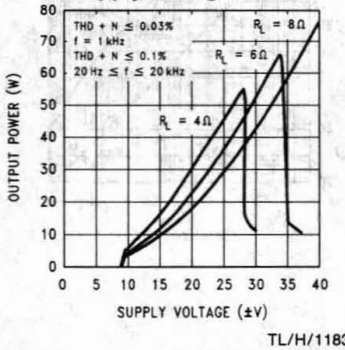
Power Dissipation vs Output Power



Power Dissipation vs Output Power



Output Power vs Supply Voltage



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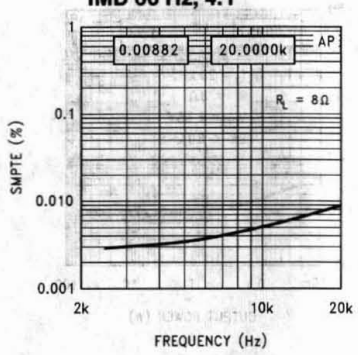
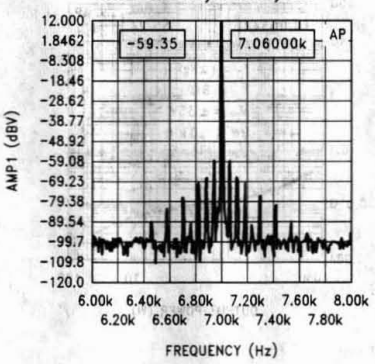
Typical Performance Characteristics (Continued)

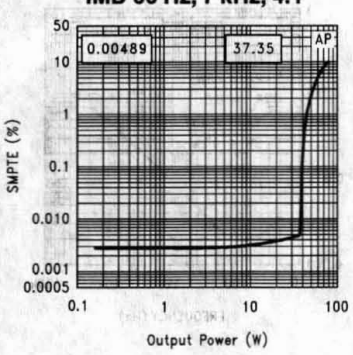
IMD 60 Hz, 4:1



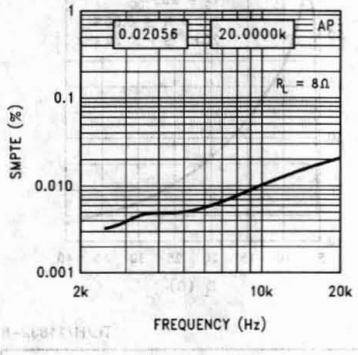
IMD 60 Hz, 7 kHz, 4:1



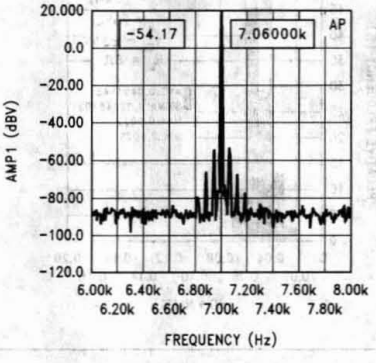
IMD 60 Hz, 7 kHz, 4:1



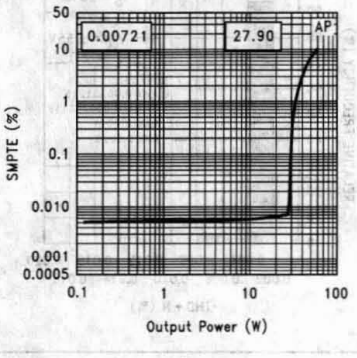
IMD 60 Hz, 1:1



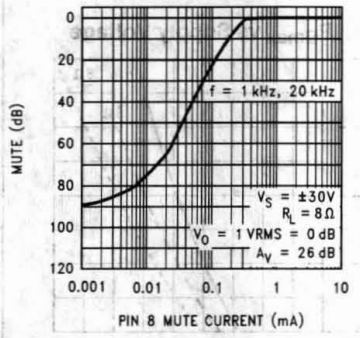
IMD 60 Hz, 7 kHz 1:1



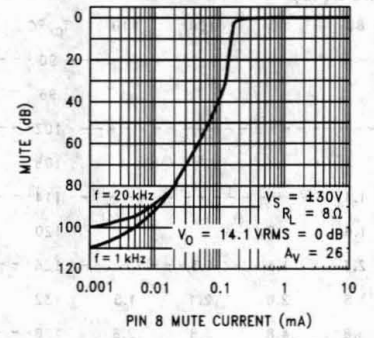
IMD 60 Hz, 7 kHz, 1:1



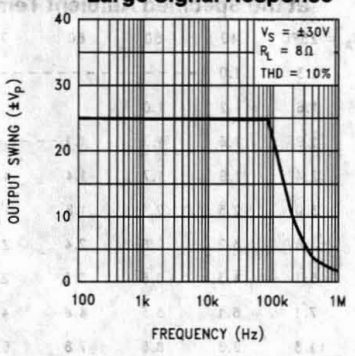
Mute Attenuation vs Mute Current



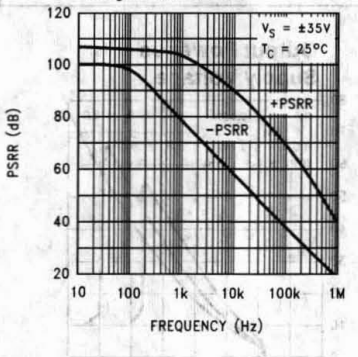
Mute Attenuation vs Mute Current



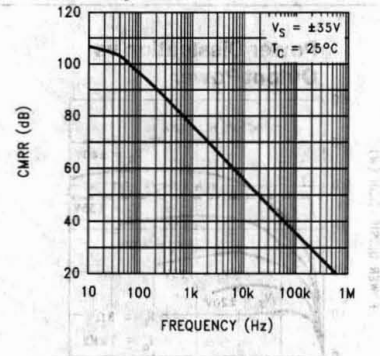
Large Signal Response



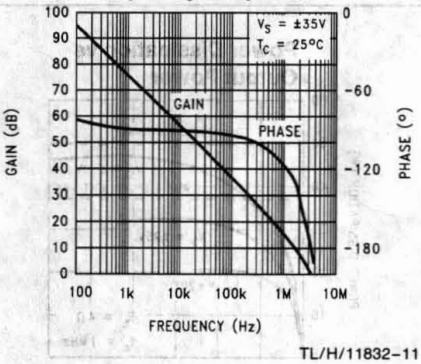
Power Supply Rejection Ratio



Common-Mode Rejection Ratio



Open Loop Frequency Response



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Application Information

GENERAL FEATURES

Mute Function: The muting function of the LM3876 allows the user to mute the music going into the amplifier by drawing less than 0.5 mA out of pin 8 of the device. This is accomplished as shown in the Typical Application Circuit where the resistor R_M is chosen with reference to your negative supply voltage and is used in conjuction with a switch. The switch (when opened) cuts off the current flow from pin 8 to V^-, thus placing the LM3876 into mute mode. Refer to the Mute Attenuation vs Mute Current curves in the **Typical Performance Characteristics** section for values of attenuation per current out of pin 8. The resistance R_M is calculated by the following equation:

R_M ($|V_{EE}| - 2.6V$)/I8 where I8 $\geq$ 0.5 mA.

Under-Voltage Protection: Upon system power-up the under-voltage protection circuitry allows the power supplies and their corresponding caps to come up close to their full values before turning on the LM3876 such that no DC output spikes occur. Upon turn-off, the output of the LM3876 is brought to ground before the power supplies such that no transients occur at power-down.

Over-Voltage Protection: The LM3876 contains overvoltage protection circuitry that limits the output current to approximately 6Apeak while also providing voltage clamping, though not through internal clamping diodes. The clamping effect is quite the same, however, the output transistors are designed to work alternately by sinking large current spikes.

SPiKe Protection: The LM3876 is protected from instantaneous peak-temperature stressing by the power transistor array. The Safe Operating Area graph in the **Typical Performance Characteristics** section shows the area of device operation where the **SPiKe** Protection Circuitry is not enabled. The waveform to the right of the SOA graph exemplifies how the dynamic protection will cause waveform distortion when enabled.

Thermal Protection: The LM3876 has a sophisticated thermal protection scheme to prevent long-term thermal stress to the device. When the temperature on the die reaches 165°C, the LM3876 shuts down. It starts operating again when the die temperature drops to about 155°C, but if the temperature again begins to rise, shutdown will occur again at 165°C. Therefore the device is allowed to heat up to a relatively high temperature if the fault condition is temporary, but a sustained fault will cause the device to cycle in a Schmitt Trigger fashion between the thermal shutdown temperature limits of 165°C and 155°C. This greatly reduces the stress imposed on the IC by thermal cycling, which in turn improves its reliability under sustained fault conditions.

Since the die temperature is directly dependent upon the heat sink, the heat sink should be chosen as discussed in the **Thermal Considerations** section, such that thermal shutdown will not be reached during normal operation. Using the best heat sink possible within the cost and space constraints of the system will improve the long-term reliability of any power semiconductor device.

THERMAL CONSIDERATIONS

Heat Sinking

The choice of a heat sink for a high-power audio amplifier is made entirely to keep the die temperature at a level such that the thermal protection circuitry does not operate under normal circumstances. The heat sink should be chosen to dissipate the maximum IC power for a given supply voltage and rated load.

With high-power pulses of longer duration than 100 ms, the case temperature will heat up drastically without the use of a heat sink. Therefore the case temperature, as measured at the center of the package bottom, is entirely dependent on heat sink design and the mounting of the IC to the heat sink. For the design of a heat sink for your audio amplifier application refer to the **Determining The Correct Heat Sink** section.

Since a semiconductor manufacturer has no control over which heat sink is used in a particular amplifier design, we can only inform the system designer of the parameters and the method needed in the determination of a heat sink. With this in mind, the system designer must choose his supply voltages, a rated load, a desired output power level, and know the ambient temperature surrounding the device. These parameters are in addition to knowing the maximum junction temperature and the thermal resistance of the IC, both of which are provided by National Semiconductor.

As a benefit to the system designer we have provided Maximum Power Dissipation vs Supply Voltages curves for various loads in the **Typical Performance Characteristics** section, giving an accurate figure for the maximum thermal resistance required for a particular amplifier design. This data was based on θ_{JC} = 1°C/W and θ_{CS} = 0.2°C/W. We also provide a section regarding heat sink determination for any audio amplifier design where θ_{CS} may be a different value. It should be noted that the idea behind dissipating the maximum power within the IC is to provide the device with a low resistance to convection heat transfer such as a heat sink. Therefore, it is necessary for the system designer to be conservative in his heat sink calculations. As a rule, the lower the thermal resistance of the heat sink the higher the amount of power that may be dissipated. This is of course guided by the cost and size requirements of the system. Convection cooling heat sinks are available commercially, and their manufacturers should be consulted for ratings.

Proper mounting of the IC is required to minimize the thermal drop between the package and the heat sink. The heat sink must also have enough metal under the package to conduct heat from the center of the package bottom to the fins without excessive temperature drop.

Application Information (Continued)

A thermal grease such as Wakefield type 120 or Thermalloy Thermacote should be used when mounting the package to the heat sink. Without this compound, thermal resistance will be no better than 0.5°C/W, and probably much worse. With the compound, thermal resistance will be 0.2°C/W or less, assuming under 0.005 inch combined flatness runout for the package and heat sink. Proper torquing of the mounting bolts is important and can be determined from heat sink manufacturer's specification sheets.

Should it be necessary to isolate V^- from the heat sink, an insulating washer is required. Hard washers like beryluum oxide, anodized aluminum and mica require the use of thermal compound on both faces. Two-mil mica washers are most common, giving about 0.4°C/W interface resistance with the compound.

Silicone-rubber washers are also available. A 0.5°C/W thermal resistance is claimed without thermal compound. Experience has shown that these rubber washers deteriorate and must be replaced should the IC be dismounted.

Determining Maximum Power Dissipation

Power dissipation within the integrated circuit package is a very important parameter requiring a thorough understanding if optimum power output is to be obtained. An incorrect maximum power dissipation (P_D) calculation may result in inadequate heat sinking, causing thermal shutdown circuitry to operate and limit the output power.

The following equations can be used to acccurately calculate the maximum and average integrated circuit power dissipation for your amplifier design, given the supply voltage, rated load, and output power. These equations can be directly applied to the Power Dissipation vs Output Power curves in the **Typical Performance Characteristics** section.

Equation (1) exemplifies the maximum power dissipation of the IC and equations (2) and (3) exemplify the average IC power dissipation expressed in different forms.

$$P_{DMAX} = V_{CC}^2/2\pi^2R_L \quad (1)$$

where V_{CC} is the total supply voltage

$$P_{DAVE} = (V_{Opk}/R_L)[V_{CC}/\pi - V_{Opk}/2] \quad (2)$$

where V_{CC} is the total supply voltage and $V_{Opk} = V_{CC}/\pi$

$$P_{DAVE} = V_{CC}\,V_{Opk}/\pi R_L - V_{Opk}^2/2R_L \quad (3)$$

where V_{CC} is the total supply voltage.

Determining the Correct Heat Sink

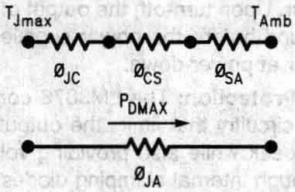
Once the maximum IC power dissipation is known for a given supply voltage, rated load, and the desired rated output power the maximum thermal resistance (in °C/W) of a heat sink can be calculated. This calculation is made using equation (4) and is based on the fact that thermal heat flow parameters are analogous to electrical current flow properties.

It is also known that typically the thermal resistance, θ_{JC} (junction to case), of the LM3876 is 1°C/W and that using Thermalloy Thermacote thermal compound provides a thermal resistance, θ_{CS} (case to heat sink), of about 0.2°C/W as explained in the **Heat Sinking** section.

Referring to the figure below, it is seen that the thermal resistance from the die (junction) to the outside air (ambient) is a combination of three thermal resistances, two of which are known, θ_{JC} and θ_{CS}. Since convection heat flow (power dissipation) is analogous to current flow, thermal resistance is analogous to electrical resistance, and temperature drops are analogous to voltage drops, the power dissipation out of the LM3876 is equal to the following:

$$P_{DMAX} = (T_{Jmax} - T_{Amb})/\theta_{JA}$$

where $\theta_{JA} = \theta_{JC} + \theta_{CS} + \theta_{SA}$



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But since we know P_{DMAX}, θ_{JC}, and θ_{SC} for the application and we are looking for θ_{SA}, we have the following:

$$\theta_{SA} = [(T_{Jmax} - T_{Amb}) - P_{DMAX}(\theta_{JC} + \theta_{CS})]/P_{DMAX} \quad (4)$$

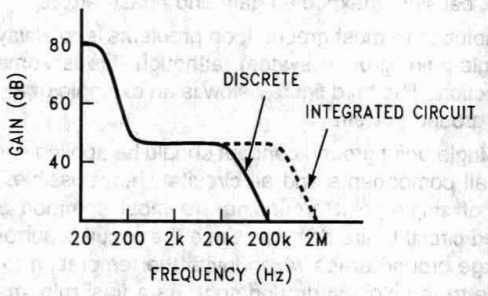
Again it must be noted that the value of θ_{SA} is dependent upon the system designer's amplifier application and its corresponding parameters as described previously. If the ambient temperature that the audio amplifier is to be working under is higher than the normal 25°C, then the thermal resistance for the heat sink, given all other things are equal, will need to be smaller.

Equations (1) and (4) are the only equations needed in the determination of the maximum heat sink thermal resistance. This is of course given that the system designer knows the required supply voltages to drive his rated load at a particular power output level and the parameters provided by the semiconductor manufacturer. These parameters are the junction to case thermal resistance, θ_{JC}, T_{Jmax} = 150°C, and the recommended Thermalloy Thermacote thermal compound resistance, θ_{CS}.

Application Information (Continued)

SIGNAL-TO-NOISE RATIO

In the measurement of the signal-to-noise ratio, misinterpretations of the numbers actually measured are common. One amplifier may sound much quieter than another, but due to improper testing techniques, they appear equal in measurements. This is often the case when comparing integrated circuit designs to discrete amplifier designs. Discrete transistor amps often "run out of gain" at high frequencies and therefore have small bandwidths to noise as indicated below.



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Integrated circuits have additional open loop gain allowing additional feedback loop gain in order to lower harmonic distortion and improve frequency response. It is this additional bandwidth that can lead to erroneous signal-to-noise measurements if not considered during the measurement process. In the typical example above, the difference in bandwidth appears small on a log scale but the factor of 10 in bandwidth, (200 kHz to 2 MHz) can result in a 10 dB theoretical difference in the signal-to-noise ratio (white noise is proportional to the square root of the bandwidth in a system).

In comparing audio amplifiers it is necessary to measure the magnitude of noise in the audible bandwidth by using a "weighting" filter.[1] A "weighting" filter alters the frequency response in order to compensate for the average human ear's sensitivity to the frequency spectra. The weighting filters at the same time provide the bandwidth limiting as discussed in the previous paragraph.

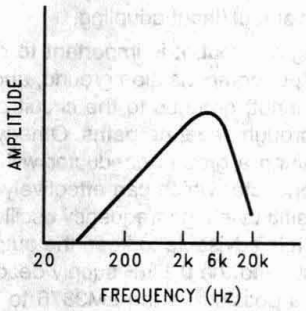
In addition to noise filtering, differing meter types give different noise readings. Meter responses include:

1. RMS reading,
2. average responding,
3. peak reading, and
4. quasi peak reading.

Although theoretical noise analysis is derived using true RMS based calculations, most actual measurements are taken with ARM (Average Responding Meter) test equipment.

Reference 1: CCIR/ARM: *A Practical Noise Measurement Method;* by Ray Dolby, David Robinson and Kenneth Gundry, AES Preprint No. 1353 (F-3).

Typical signal-to-noise figures are listed for an A-weighted filter which is commonly used in the measurement of noise. The shape of all weighting filters is similar, with the peak of the curve usually occurring in the 3 kHz–7 kHz region as shown below.



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SUPPLY BYPASSING

The LM3876 has excellent power supply rejection and does not require a regulated supply. However, to eliminate possible oscillations all op amps and power op amps should have their supply leads bypassed with low-inductance capacitors having short leads and located close to the package terminals. Inadequate power supply bypassing will manifest itself by a low frequency oscillation known as "motorboating" or by high frequency instabilities. These instabilities can be eliminated through multiple bypassing utilizing a large tantalum or electrolytic capacitor (10 μF or larger) which is used to absorb low frequency variations and a small ceramic capacitor (0.1 μF) to prevent any high frequency feedback through the power supply lines.

If adequate bypassing is not provided the current in the supply leads which is a rectified component of the load current may be fed back into internal circuitry. This signal causes low distortion at high frequencies requiring that the supplies be bypassed at the package terminals with an electrolytic capacitor of 470 μF or more.

LEAD INDUCTANCE

Power op amps are sensitive to inductance in the output lead, particularly with heavy capacitive loading. Feedback to the input should be taken directly from the output terminal, minimizing common inductance with the load.

Lead inductance can also cause voltage surges on the supplies. With long leads to the power supply, energy is stored in the lead inductance when the output is shorted. This energy can be dumped back into the supply bypass capacitors when the short is removed. The magnitude of this transient is reduced by increasing the size of the bypass capacitor near the IC. With at least a 20 μF local bypass, these voltage surges are important only if the lead length exceeds a couple feet ($>$ 1 μH lead inductance). Twisting together the supply and ground leads minimizes the effect.

Application Information (Continued)

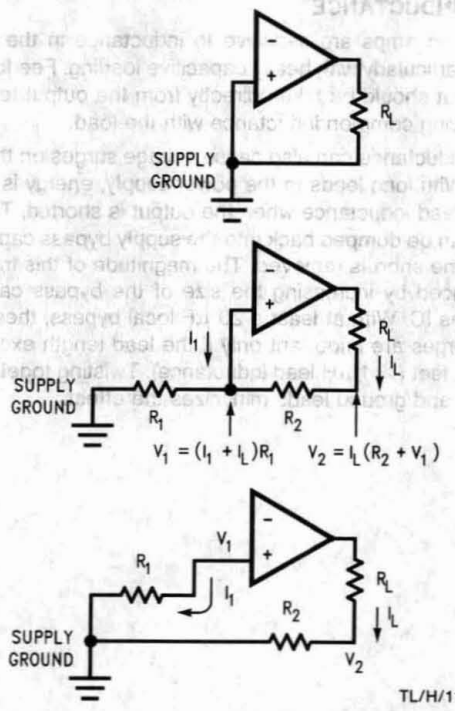
LAYOUT, GROUND LOOPS AND STABILITY

The LM3876 is designed to be stable when operated at a closed-loop gain of 10 or greater, but as with any other high-current amplifier, the LM3876 can be made to oscillate under certain conditions. These usually involve printed circuit board layout or output/input coupling.

When designing a layout, it is important to return the load ground, the output compensation ground, and the low level (feedback and input) grounds to the circuit board common ground point through separate paths. Otherwise, large currents flowing along a ground conductor will generate voltages on the conductor which can effectively act as signals at the input, resulting in high frequency oscillation or excessive distortion. It is advisable to keep the output compensation components and the 0.1 μF supply decoupling capacitors as close as possible to the LM3876 to reduce the effects of PCB trace resistance and inductance. For the same reason, the ground return paths should be as short as possible.

In general, with fast, high-current circuitry, all sorts of problems can arise from improper grounding which again can be avoided by returning all grounds separately to a common point. Without isolating the ground signals and returning the grounds to a common point, ground loops may occur.

"Ground Loop" is the term used to describe situations occurring in ground systems where a difference in potential exists between two ground points. Ideally a ground is a ground, but unfortunately, in order for this to be true, ground conductors with zero resistance are necessary. Since real world ground leads possess finite resistance, currents running through them will cause finite voltage drops to exist. If two ground return lines tie into the same path at different points there will be a voltage drop between them. The first figure below shows a common ground example where the positive input ground and the load ground are returned to the supply ground point via the same wire. The addition of the finite wire resistance, R_2, results in a voltage difference between the two points as shown below.



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The load current I_L will be much larger than input bias current I_I, thus V_1 will follow the output voltage directly, i.e. in phase. Therefore the voltage appearing at the non-inverting input is effectively positive feedback and the circuit may oscillate. If there were only one device to worry about then the values of R_1 and R_2 would probably be small enough to be ignored; however, several devices normally comprise a total system. Any ground return of a separate device, whose output is in phase, can feedback in a similar manner and cause instabilities. Out of phase ground loops also are troublesome, causing unexpected gain and phase errors.

The solution to most ground loop problems is to always use a single-point ground system, although this is sometimes impractical. The third figure below is an example of a single-point ground system.

The single-point ground concept should be applied rigorously to all components and all circuits when possible. Violations of single-point grounding are most common among printed circuit board designs, since the circuit is surrounded by large ground areas which invite the temptation to run a device to the closest ground spot. As a final rule, make all ground returns low resistance and low inductance by using large wire and wide traces.

Occasionally, current in the output leads (which function as antennas) can be coupled through the air to the amplifier input, resulting in high-frequency oscillation. This normally happens when the source impedance is high or the input leads are long. The problem can be eliminated by placing a small capacitor, C_C, (on the order of 50 pF to 500 pF) across the LM3876 input terminals. Refer to the **External Components Description** section relating to component interaction with C_f.

REACTIVE LOADING

It is hard for most power amplifiers to drive highly capacitive loads very effectively and normally results in oscillations or ringing on the square wave response. If the output of the LM3876 is connected directly to a capacitor with no series resistance, the square wave response will exhibit ringing if the capacitance is greater than about 0.2 μF. If highly capacitive loads are expected due to long speaker cables, a method commonly employed to protect amplifiers from low impedances at high frequencies is to couple to the load through a 10Ω resistor in parallel with a 0.7 μH inductor. The inductor-resistor combination as shown in the **Typical Application Circuit** isolates the feedback amplifier from the load by providing high output impedance at high frequencies thus allowing the 10Ω resistor to decouple the capacitive load and reduce the Q of the series resonant circuit. The LR combination also provides low output impedance at low frequencies thus shorting out the 10Ω resistor and allowing the amplifier to drive the series RC load (large capacitive load due to long speaker cables) directly.

Application Information (Continued)

GENERALIZED AUDIO POWER AMPLIFIER DESIGN

The system designer usually knows some of the following parameters when starting an audio amplifier design:

Desired Power Output	Input Level
Input Impedance	Load Impedance
Maximum Supply Voltage	Bandwidth

The power output and load impedance determine the power supply requirements, however, depending upon the application some system designers may be limited to certain maximum supply voltages. If the designer does have a power supply limitation, he should choose a practical load impedance which would allow the amplifier to provide the desired output power, keeping in mind the current limiting capabilities of the device. In any case, the output signal swing and current are found from (where P_O is the average output power):

$$V_{opeak} = \sqrt{2 R_L P_O} \quad (1)$$

$$I_{opeak} = \sqrt{(2 P_O)/R_L} \quad (2)$$

To determine the maximum supply voltage the following parameters must be considered. Add the dropout voltage (5V for LM3876) to the peak output swing, V_{opeak}, to get the supply rail value (i.e. $\pm$ (V_{opeak} + Vod) at a current of I_{opeak}). The regulation of the supply determines the unloaded voltage, usually about 15% higher. Supply voltage will also rise 10% during high line conditions. Therefore, the maximum supply voltage is obtained from the following equation:

$$\text{Max. supplies} \approx \pm (V_{opeak} + \text{Vod})(1 + \text{regulation})(1.1) \quad (3)$$

The input sensitivity and the output power specs determine the minimum required gain as depicted below:

$$A_V \geq (\sqrt{P_O R_L})/(V_{IN}) = V_{orms}/V_{inrms} \quad (4)$$

Normally the gain is set between 20 and 200; for a 40W, 8Ω audio amplifier this results in a sensitivity of 894 mV and 89 mV, respectively. Although higher gain amplifiers provide greater output power and dynamic headroom capabilities, there are certain shortcomings that go along with the so called "gain." The input referred noise floor is increased and hence the SNR is worse. With the increase in gain, there is also a reduction of the power bandwidth which results in a decrease in feedback thus not allowing the amplifier to respond quickly enough to nonlinearities. This decreased ability to respond to nonlinearities increases the THD + N specification.

The desired input impedance is set by R_{IN}. Very high values can cause board layout problems and DC offsets at the output. The value for the feedback resistance, R_{f1}, should be chosen to be a relatively large value (10 kΩ–100 kΩ), and the other feedback resistance, Ri, is calculated using standard op amp configuration gain equations. Most audio amplifiers are designed from the non-inverting amplifier configuration.

DESIGN A 40W/8Ω AUDIO AMPLIFIER

Given:

Power Output	40W
Load Impedance	8Ω
Input Level	1V(max)
Input Impedance	100 kΩ
Bandwidth	20 Hz–20 kHz ± 0.25 dB

Equations (1) and (2) give:

40W/8Ω $V_{opeak} = 25.3V$ $I_{opeak} = 3.16A$

Therefore the supply required is: ±30.3V @ 3.16A

With 15% regulation and high line the final supply voltage is ±38.3V using equation (3). At this point it is a good idea to check the Power Output vs Supply Voltage to ensure that the required output power is obtainable from the device while maintaining low THD + N. It is also good to check the Power Dissipation vs Supply Voltage to ensure that the device can handle the internal power dissipation. At the same time designing in a relatively practical sized heat sink with a low thermal resistance is also important. Refer to **Typical Performance Characteristics** graphs and the **Thermal Considerations** section for more information.

The minimum gain from equation (4) is: $A_V \geq 18$

We select a gain of 21 (Non-Inverting Amplifier); resulting in a sensitivity of 894 mV.

Letting R_{IN} equal 100 kΩ gives the required input impedance, however, this would eliminate the "volume control" unless an additional input impedance was placed in series with the 10 kΩ potentiometer that is depicted in *Figure 1*. Adding the additional 100 kΩ resistor would ensure the minumum required input impedance.

For low DC offsets at the output we let R_{f1} = 100 kΩ. Solving for Ri (Non-Inverting Amplifier) gives the following:

$$Ri = R_{f1}/(A_V - 1) = 100k/(21 - 1) = 5\ k\Omega; \text{ use } 5.1\ k\Omega$$

The bandwidth requirement must be stated as a pole, i.e., the 3 dB frequency. Five times away from a pole gives 0.17 dB down, which is better than the required 0.25 dB. Therefore:

$$f_L = 20\ Hz/5 = 4\ Hz$$

$$f_H = 20\ kHz \times 5 = 100\ kHz$$

At this point, it is a good idea to ensure that the Gain-Bandwidth Product for the part will provide the designed gain out to the upper 3 dB point of 100 kHz. This is why the minimum GBWP of the LM3876 is important.

$$GBWP \geq A_V \times f3\ dB = 21 \times 100\ kHz = 2.1\ MHz$$

$$GBWP = 2.0\ MHz\ (min)\ for\ the\ LM3876$$

Solving for the low frequency roll-off capacitor, Ci, we have:

$$Ci \geq 1/(2\pi\ Ri\ f_L) = 7.8\ \mu F; \text{ use } 10\ \mu F.$$

Definition of Terms

Input Offset Voltage: The absolute value of the voltage which must be applied between the input terminals through two equal resistances to obtain zero output voltage and current.

Input Bias Current: The absolute value of the average of the two input currents with the output voltage and current at zero.

Input Offset Current: The absolute value of the difference in the two input currents with the output voltage and current at zero.

Input Common-Mode Voltage Range (or Input Voltage Range): The range of voltages on the input terminals for which the amplifier is operational. Note that the specifications are not guaranteed over the full common-mode voltage range unless specifically stated.

Common-Mode Rejection: The ratio of the input common-mode voltage range to the peak-to-peak change in input offset voltage over this range.

Power Supply Rejection: The ratio of the change in input offset voltage to the change in power supply voltages producing it.

Quiescent Supply Current: The current required from the power supply to operate the amplifier with no load and the output voltage and current at zero.

Slew Rate: The internally limited rate of change in output voltage with a large amplitude step function applied to the input.

Class B Amplifier: The most common type of audio power amplifier that consists of two output devices each of which conducts for 180° of the input cycle. The LM3876 is a Quasi-AB type amplifier.

Crossover Distortion: Distortion caused in the output stage of a class B amplifier. It can result from inadequate bias current providing a dead zone where the output does not respond to the input as the input cycle goes through its zero crossing point. Also for ICs an inadequate frequency response of the output PNP device can cause a turn-on delay giving crossover distortion on the negative going transition through zero crossing at the higher audio frequencies.

THD + N: Total Harmonic Distortion plus Noise refers to the measurement technique in which the fundamental component is removed by a bandreject (notch) filter and all remaining energy is measured including harmonics and noise.

Signal-to-Noise Ratio: The ratio of a system's output signal level to the system's output noise level obtained in the absence of a signal. The output reference signal is either specified or measured at a specified distortion level.

Continuous Average Output Power: The minimum sine wave continuous average power output in watts (or dBW) that can be delivered into the rated load, over the rated bandwidth, at the rated maximum total harmonic distortion.

Music Power: A measurement of the peak output power capability of an amplifier with either a signal duration sufficiently short that the amplifier power supply does not sag during the measurement, or when high quality external power supplies are used. This measurement (an IHF standard) assumes that with normal music program material the amplifier power supplies will sag insignificantly.

Peak Power: Most commonly referred to as the power output capability of an amplifier that can be delivered to the load; specified by the part's maximum voltage swing.

Headroom: The margin between an actual signal operating level (usually the power rating of the amplifier with particular supply voltages, a rated load value, and a rated THD + N figure) and the level just before clipping distortion occurs, expressed in decibels.

Large Signal Voltage Gain: The ratio of the output voltage swing to the differential input voltage required to drive the output from zero to either swing limit. The output swing limit is the supply voltage less a specified quasi-saturation voltage. A pulse of short enough duration to minimize thermal effects is used as a measurement signal.

Output-Current Limit: The output current with a fixed output voltage and a large input overdrive. The limiting current drops with time once **SPiKe** protection circuitry is activated.

Output Saturation Threshold (Clipping Point): The output swing limit for a specified input drive beyond that required for zero output. It is measured with respect to the supply to which the output is swinging.

Output Resistance: The ratio of the change in output voltage to the change in output current with the output around zero.

Power Dissipation Rating: The power that can be dissipated for a specified time interval without activating the protection circuitry. For time intervals in excess of 100 ms, dissipation capability is determined by heat sinking of the IC package rather than by the IC itself.

Thermal Resistance: The peak, junction-temperature rise, per unit of internal power dissipation (units in °C/W), above the case temperature as measured at the center of the package bottom.

The DC thermal resistance applies when one output transistor is operating continuously. The AC thermal resistance applies with the output transistors conducting alternately at a high enough frequency that the peak capability of neither transistor is exceeded.

Power Bandwidth: The power bandwidth of an audio amplifier is the frequency range over which the amplifier voltage gain does not fall below 0.707 of the flat band voltage gain specified for a given load and output power.

Power bandwidth also can be measured by the frequencies at which a specified level of distortion is obtained while the amplifier delivers a power output 3 dB below the rated output. For example, an amplifier rated at 60W with ≤ 0.25% THD + N, would make its power bandwidth measured as the difference between the upper and lower frequencies at which 0.25% distortion was obtained while the amplifier was delivering 30W.

Gain-Bandwidth Product: The Gain-Bandwidth Product is a way of predicting the high-frequency usefulness of an op amp. The Gain-Bandwidth Product is sometimes called the unity-gain frequency or unity-gain cross frequency because the open-loop gain characteristic passes through or crosses unity gain at this frequency. Simply, we have the following relationship: $A_{CL1} \times f_1 = A_{CL2} \times f_2$

Assuming that at unity-gain ($A_{CL1} = 1$ or (0 dB)) fu = fi = GBWP, then we have the following: GBWP = $A_{CL2} \times f2$

This says that once fu (GBWP) is known for an amplifier, then the open-loop gain can be found at any frequency. This is also an excellent equation to determine the 3 dB point of a closed-loop gain, assuming that you know the GBWP of the device. Refer to the diagram on the following page.

Definition of Terms (Continued)

Biamplification: The technique of splitting the audio frequency spectrum into two sections and using individual power amplifiers to drive a separate woofer and tweeter. Crossover frequencies for the amplifiers usually vary between 500 Hz and 1600 Hz. "Biamping" has the advantages of allowing smaller power amps to produce a given sound pressure level and reducing distortion effects produsedby overdrive in one part of the frequency spectrum affecting the other part.

C.C.I.R./A.R.M.:

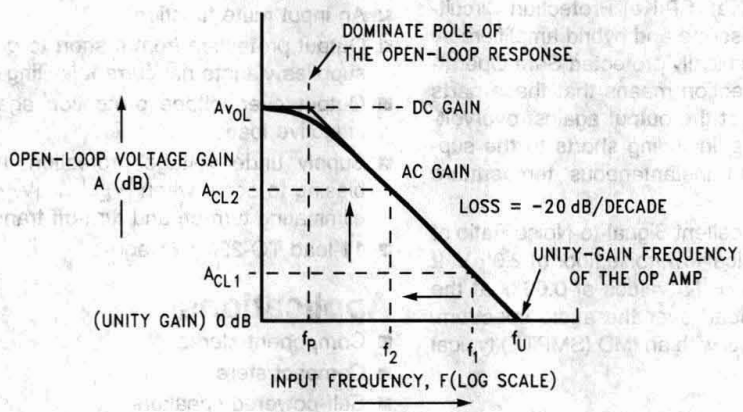
Literally: International Radio Consultative Committee
Average Responding Meter

This refers to a weighted noise measurement for a Dolby B type noise reduction system. A filter characteristic is used that gives a closer correlation of the measurement with the subjective annoyance of noise to the ear. Measurements made with this filter cannot necessarily be related to unweighted noise measurements by some fixed conversion factor since the answers obtained will depend on the spectrum of the noise source.

S.P.L.: Sound Pressure Level—usually measured with a microphone/meter combination calibrated to a pressure level of 0.0002 μBars (approximately the threshold hearing level).

$$S.P.L. = 20 \text{ Log } 10P/0.0002 \text{ dB}$$

where P is the R.M.S. sound pressure in microbars.
(1 Bar = 1 atmosphere = 14.5 lb/in^2 = 194 dB S.P.L.).



TL/H/11832–16

National Semiconductor

LM3886 *Overture*™ Audio Power Amplifier Series
High-Performance 68W Audio Power Amplifier w/Mute

General Description

The LM3886 is a high-performance audio power amplifier capable of delivering 68W of continuous average power to a 4Ω load and 38W into 8Ω with 0.1% (THD + N) from 20 Hz–20 kHz.

The performance of the LM3886, utilizing its Self Peak Instantaneous Temperature (°Ke) (**SPiKe**) Protection Circuitry, puts it in a class above discrete and hybrid amplifiers by providing an inherently, dynamically protected Safe Operating Area (SOA). **SPiKe** Protection means that these parts are completely safeguarded at the output against overvoltage, undervoltage, overloads, including shorts to the supplies, thermal runaway, and instantaneous temperature peaks.

The LM3886 maintains an excellent Signal-to-Noise Ratio of greater than 92 dB with a typical low noise floor of 2.0 μV. It exhibits extremely low (THD + N) values of 0.03% at the rated output into the rated load over the audio spectrum, and provides excellent linearity with an IMD (SMPTE) typical rating of 0.004%.

Features

- 68W cont. avg. output power into 4Ω at V_{CC} = ±28V
- 38W cont. avg. output power into 8Ω at V_{CC} = ±28V
- 50W cont. avg. output power into 8Ω at V_{CC} = ±35V
- 135W instantaneous peak output power capability
- Signal-to-Noise Ratio ≥ 92 dB
- An input mute function
- Output protection from a short to ground or to the supplies via internal current limiting circuitry
- Output over-voltage protection against transients from inductive loads
- Supply under-voltage protection, not allowing internal biasing to occur when $|V_{EE}| + |V_{CC}| \leq 12V$, thus eliminating turn-on and turn-off transients
- 11-lead TO-220 package

Applications

- Component stereo
- Compact stereo
- Self-powered speakers
- Surround-sound amplifiers
- High-end stereo TVs

Typical Application

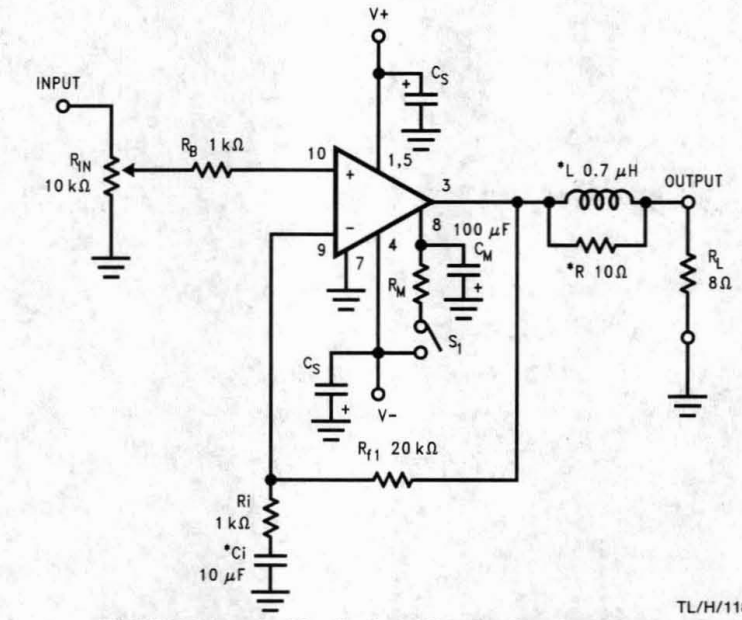
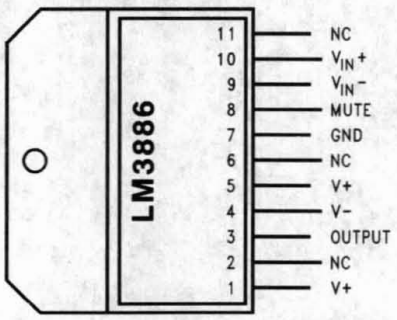


FIGURE 1. Typical Audio Amplifier Application Circuit

*Optional components dependent upon specific design requirements. Refer to the External Components Description section for a component functional description.

Connection Diagram

Plastic Package (Note 8)



Top View

Order Number LM3886T or LM3886TF
See NS Package Number TA11B for Staggered Lead Non-Isolated Package or TF11B* for Staggered Lead Isolated Package

*Preliminary: call you local National Sales Rep. or distributor for availability

Absolute Maximum Ratings (Notes 1, 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage $\|V^+\| + \|V^-\|$ (No Signal)	94V
Supply Voltage $\|V^+\| + \|V^-\|$ (Input Signal)	84V
Common Mode Input Voltage	(V^+ or V^-) and $\|V^+\| + \|V^-\| \leq 80V$
Differential Input Voltage (Note 12)	60V
Output Current	Internally Limited
Power Dissipation (Note 3)	125W
ESD Susceptibility (Note 4)	3000V
Junction Temperature (Note 5)	150°C
Soldering Information	
T Package (10 seconds)	260°C
Storage Temperature	−40°C to +150°C
Thermal Resistance	
θ_{JC}	1°C/W
θ_{JA}	43°C/W

Operating Ratings (Notes 1, 2)

Temperature Range	
$T_{MIN} \leq T_A \leq T_{MAX}$	$-20°C \leq T_A \leq +85°C$
Supply Voltage $\|V^+\| + \|V^-\|$	20V to 84V

Note: Operation is guaranteed up to 84V, however, distortion may be introduced from **SPiKe** Protection Circuitry if proper thermal considerations are not taken into account. Refer to the **Thermal Considerations** section for more information.

(See **SPiKe**™ Protection Response)

Electrical Characteristics (Notes 1, 2) The following specifications apply for $V^+ = +28V$, $V^- = -28V$, $I_{MUTE} = -0.5$ mA with $R_L = 4\Omega$ unless otherwise specified. Limits apply for $T_A = 25°C$.

Symbol	Parameter	Conditions	LM3886 Typical (Note 6)	LM3886 Limit (Note 7)	Units (Limits)
$\|V^+\| + \|V^-\|$	Power Supply Voltage (Note 10)	$V_{pin7} - V^- \geq 9V$	18	20	V (min)
				84	V (max)
A_M	Mute Attenuation	Pin 8 Open or at 0V, Mute: On Current out of Pin 8 > 0.5 mA, Mute: Off	115	80	dB (min)
**P_O	Output Power (Continuous Average)	THD + N = 0.1% (max) f = 1 kHz; f = 20 kHz			
		$\|V^+\| = \|V^-\| = 28V$, $R_L = 4\Omega$	68	60	W (min)
		$\|V^+\| = \|V^-\| = 28V$, $R_L = 8\Omega$	38	30	W (min)
		$\|V^+\| = \|V^-\| = 35V$, $R_L = 8\Omega$	50		W
Peak P_O	Instantaneous Peak Output Power		135		W
THD + N	Total Harmonic Distortion Plus Noise	60W, $R_L = 4\Omega$,	0.03		%
		30W, $R_L = 8\Omega$,	0.03		%
		20 Hz ≤ f ≤ 20 kHz $A_V = 26$ dB			
**SR	Slew Rate (Note 9)	$V_{IN} = 2.0$Vp-p, $t_{RISE} = 2$ ns	19	8	V/μs (min)
*I^+	Total Quiescent Power Supply Current	$V_{CM} = 0V$, $V_o = 0V$, $I_o = 0A$	50	85	mA (max)
*V_{OS}	Input Offset Voltage	$V_{CM} = 0V$, $I_o = 0$ mA	1	10	mV (max)
I_B	Input Bias Current	$V_{CM} = 0V$, $I_o = 0$ mA	0.2	1	μA (max)
I_{OS}	Input Offset Current	$V_{CM} = 0V$, $I_o = 0$ mA	0.01	0.2	μA (max)
I_o	Output Current Limit	$\|V^+\| = \|V^-\| = 20V$, $t_{ON} = 10$ ms, $V_O = 0V$	11.5	7	A (min)
*V_{od}	Output Dropout Voltage (Note 11)	$\|V^+ - V_O\|$, $V^+ = 28V$, $I_o = +100$ mA	1.6	2.0	V (max)
		$\|V_O - V^-\|$, $V^- = -28V$, $I_o = -100$ mA	2.5	3.0	V (max)
*PSRR	Power Supply Rejection Ratio	$V^+ = 40V$ to 20V, $V^- = -40V$, $V_{CM} = 0V$, $I_o = 0$ mA	120	85	dB (min)
		$V^+ = 40V$, $V^- = -40V$ to $-20V$, $V_{CM} = 0V$, $I_o = 0$ mA	105	85	dB (min)

*DC Electrical Test; refer to Test Circuit #1.

**AC Electrical Test; refer to Test Circuit #2.

Electrical Characteristics (Notes 1, 2)

The following specifications apply for $V^+ = +28V$, $V^- = -28V$, $I_{MUTE} = -0.5$ mA with $R_L = 4\Omega$ unless otherwise specified. Limits apply for $T_A = 25°C$. (Continued)

Symbol	Parameter	Conditions	LM3886		Units (Limits)
			Typical (Note 6)	Limit (Note 7)	
*CMRR	Common Mode Rejection Ratio	$V^+ = 60V$ to $20V$, $V^- = -20V$ to $-60V$, $V_{CM} = 20V$ to $-20V$, $I_o = 0$ mA	110	85	dB (min)
*A_{VOL}	Open Loop Voltage Gain	$\|V^+\| = \|V^-\| = 28V$, $R_L = 2\,k\Omega$, $\Delta V_O = 40V$	115	90	dB (min)
GBWP	Gain-Bandwidth Product	$\|V^+\| = \|V^-\| = 30V$ $f_O = 100$ kHz, $V_{IN} = 50$ mVrms	8	2	MHz (min)
**e_{IN}	Input Noise	IHF—A Weighting Filter $R_{IN} = 600\Omega$ (Input Referred)	2.0	10	μV (max)
SNR	Signal-to-Noise Ratio	$P_O = 1$W, A-Weighted, Measured at 1 kHz, $R_S = 25\Omega$	92.5		dB
		$P_O = 60$W, A-Weighted, Measured at 1 kHz, $R_S = 25\Omega$	110		dB
IMD	Intermodulation Distortion Test	60 Hz, 7 kHz, 4:1 (SMPTE) 60 Hz, 7 kHz, 1:1 (SMPTE)	0.004 0.009		%

*DC Electrical Test; refer to Test Circuit #1.

**AC Electrical Test; refer to Test Circuit #2.

Note 1: All voltages are measured with respect to the GND pin (pin 7), unless otherwise specified.

Note 2: *Absolute Maximum Ratings* indicate limits beyond which damage to the device may occur. *Operating Ratings* indicate conditions for which the device is functional, but do not guarantee specific performance limits. *Electrical Characteristics* state DC and AC electrical specifications under particular test conditions which guarantee specific performance limits. This assumes that the device is within the Operating Ratings. Specifications are not guaranteed for parameters where no limit is given, however, the typical value is a good indication of device performance.

Note 3: For operating at case temperatures above 25°C, the device must be derated based on a 150°C maximum junction temperature and a thermal resistance of $\theta_{JC} = 1.0$ °C/W (junction to case). Refer to the Thermal Resistance figure in the Application Information section under **Thermal Considerations**.

Note 4: Human body model, 100 pF discharged through a 1.5 kΩ resistor.

Note 5: The operating junction temperature maximum is 150°C, however, the instantaneous Safe Operating Area temperature is 250°C.

Note 6: Typicals are measured at 25°C and represent the parametric norm.

Note 7: Limits are guaranteed to National's AOQL (Average Outgoing Quality Level).

Note 8: The LM3886T package TA11B is a non-isolated package, setting the tab of the device and the heat sink at V^- potential when the LM3886 is directly mounted to the heat sink using only thermal compound. If a mica washer is used in addition to thermal compound, θ_{CS} (case to sink) is increased, but the heat sink will be isolated from V^-.

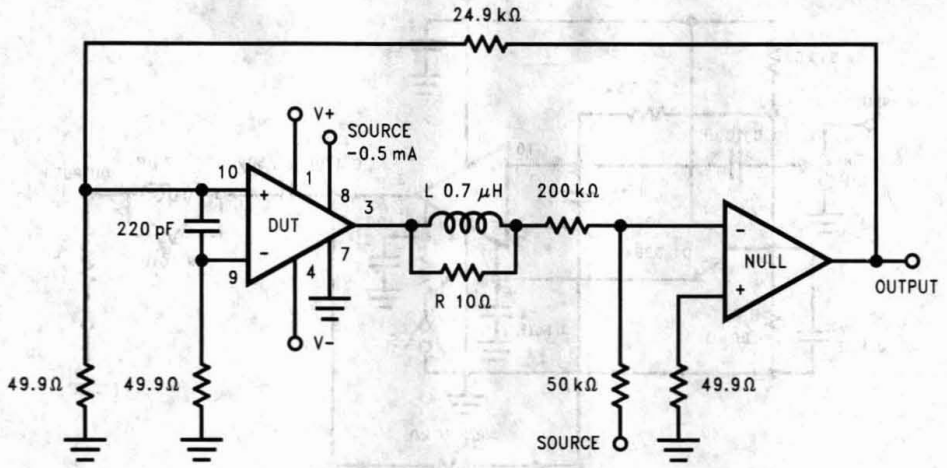
Note 9: The feedback compensation network limits the bandwidth of the closed-loop response and so the slew rate will be reduced due to the high frequency roll-off. Without feedback compensation, the slew rate is typically larger.

Note 10: V^- must have at least $-9V$ at its pin with reference to ground in order for the under-voltage protection circuitry to be disabled.

Note 11: The output dropout voltage is the supply voltage minus the clipping voltage. Refer to the Clipping Voltage vs Supply Voltage graph in the **Typical Performance Characteristics** section.

Note 12: The Differential Input Voltage Absolute Maximum Rating is based on supply voltages of $V^+ = +40V$ and $V^- = -40V$.

Test Circuit #1 *(DC Electrical Test Circuit)



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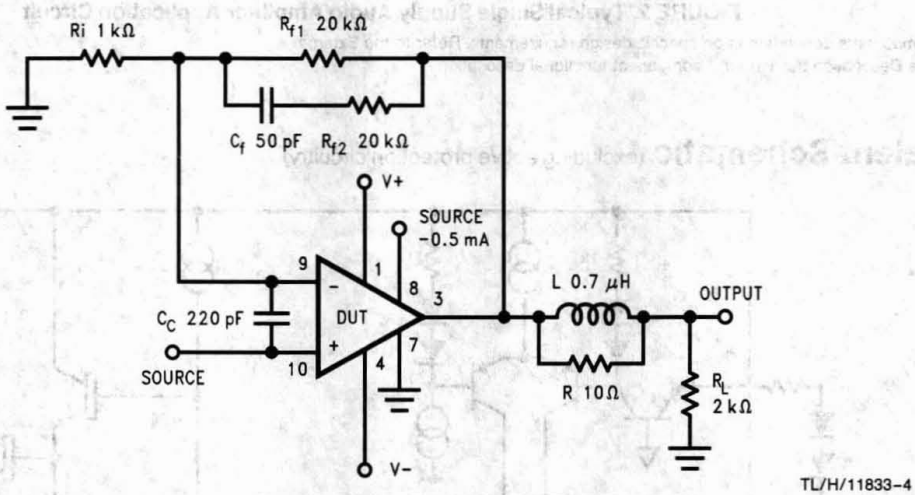
Test Circuit #2 **(AC Electrical Test Circuit)



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Single Supply Application Circuit

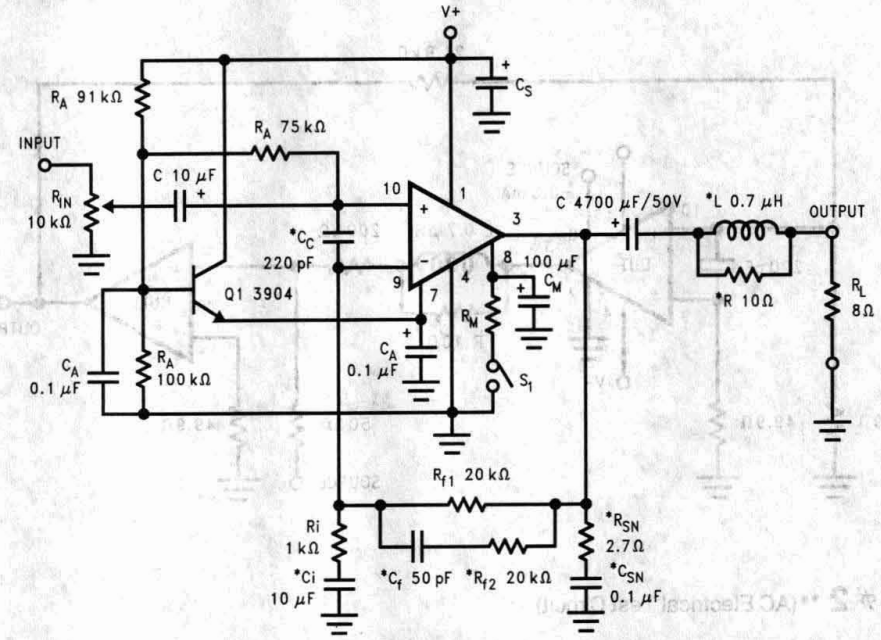

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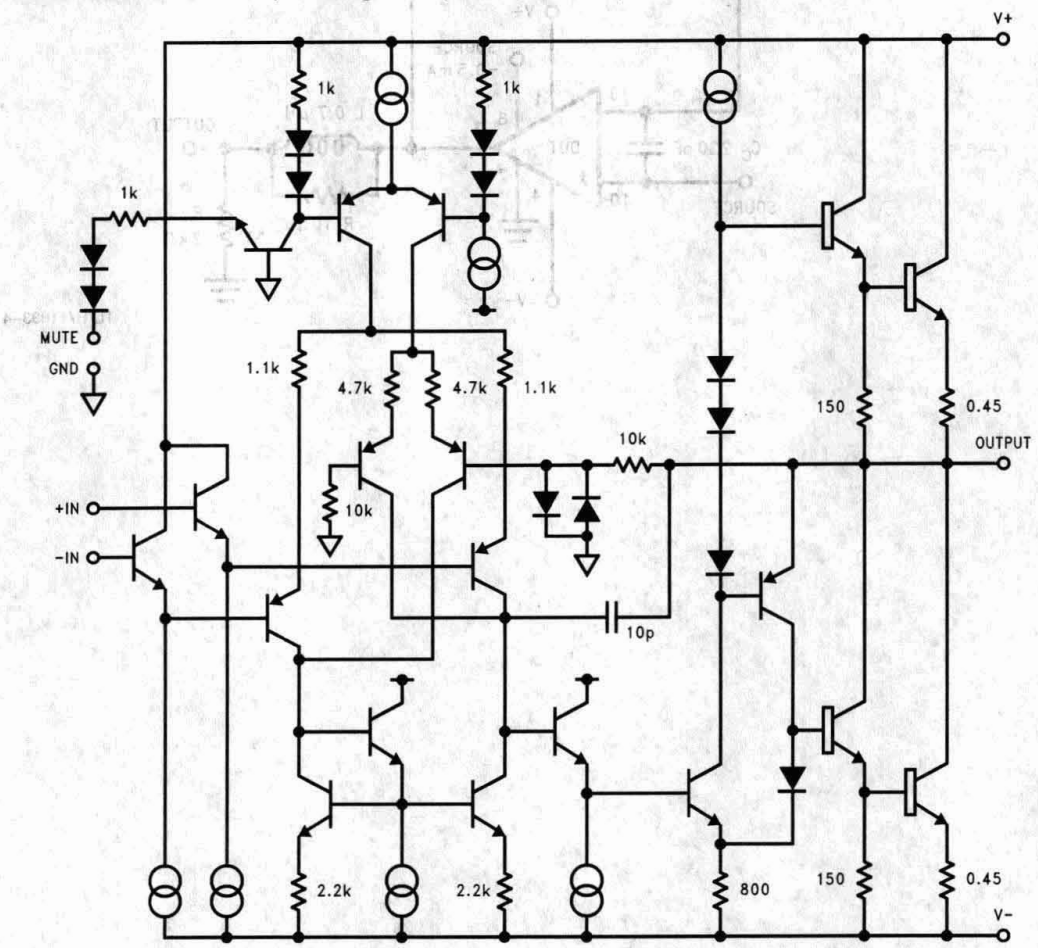
FIGURE 2. Typical Single Supply Audio Amplifier Application Circuit

*Optional components dependent upon specific design requirements. Refer to the External Components Description section for a component functional description.

Equivalent Schematic (excluding active protection circuitry)



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External Components Description (*Figures 1* and *2*)

Components		Functional Description
1.	R_{IN}	Acts as a volume control by setting the voltage level allowed to the amplifier's input terminals.
2.	R_A	Provides DC voltage biasing for the single supply operation and bias current for the positive input terminal.
3.	C_A	Provides bias filtering.
4.	C	Provides AC coupling at the input and output of the amplifier for single supply operation.
5.	R_B	Prevents currents from entering the amplifier's non-inverting input which may be passed through to the load upon power-down of the system due to the low input impedance of the circuitry when the under-voltage circuitry is off. This phenomenon occurs when the supply voltages are below 1.5V.
6.	*C_C	Reduces the gain (bandwidth of the amplifier) at high frequencies to avoid quasi-saturation oscillations of the output transistor. The capacitor also suppresses external electromagnetic switching noise created from fluorescent lamps.
7.	Ri	Inverting input resistance to provide AC Gain in conjunction with R_{f1}.
8.	*Ci	Feedback capacitor. Ensures unity gain at DC. Also a low frequency pole (highpass roll-off) at: $f_c = 1/(2\pi Ri\ Ci)$
9.	R_{f1}	Feedback resistance to provide AC Gain in conjunction with Ri.
10.	*R_{f2}	At higher frequencies feedback resistance works with C_f to provide lower AC Gain in conjunction with R_{f1} and Ri. A high frequency pole (lowpass roll-off) exists at: $f_c = [R_{f1}\ R_{f2}\ (s + 1/R_{f2}C_f)]/[(R_{f1} + R_{f2})(s + 1/C_f(R_{f1} + R_{f2}))]$
11.	*C_f	Compensation capacitor that works with R_{f1} and R_{f2} to reduce the AC Gain at higher frequencies.
12.	R_M	Mute resistance set up to allow 0.5 mA to be drawn from pin 8 to turn the muting function off. → R_M is calculated using: $R_M \leq (\lvert V_{EE}\rvert - 2.6V)/I8$ where $I8 \geq 0.5$ mA. Refer to the Mute Attenuation vs. Mute Current curves in the Typical Performance Characteristics section.
13.	C_M	Mute capacitance set up to create a large time constant for turn-on and turn-off muting.
14.	*R_{SN}	Works with C_{SN} to stabilize the output stage by creating a pole that eliminates high frequency oscillations.
15.	*C_{SN}	Works with R_{SN} to stabilize the output stage by creating a pole that eliminates high frequency oscillations. $f_c = 1/(2\pi R_{SN}C_{SN})$
16.	*L	Provides high impedance at high frequecies so that R may decouple a highly capacitive load
17.	*R	and reduce the Q of the series resonant circuit due to capacitive load. Also provides a low impedance at low frequencies to short out R and pass audio signals to the load.
18.	C_S	Provides power supply filtering and bypassing.
19.	S1	Mute switch that mutes the music going into the amplifier when opened.

*Optional components dependent upon specific design requirements. Refer to the Application Information section for more information.

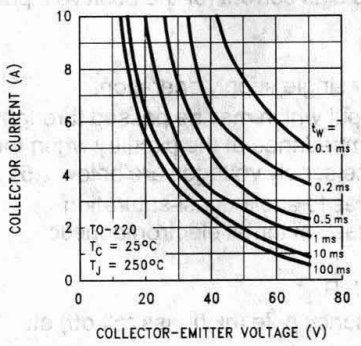
OPTIONAL EXTERNAL COMPONENT INTERACTION

Although the optional external components have specific desired functions that are designed to reduce the bandwidth and eliminate unwanted high frequency oscillations they may cause certain undesirable effects when they interact. Interaction may occur for components whose reactances are in close proximity to one another. One example would be the coupling capacitor, C_C, and the compensation capacitor, C_f. These two components act as low impedances to certain frequencies which will couple signals from the input to the output. Please take careful note of basic amplifier component functionality when designing in these components.

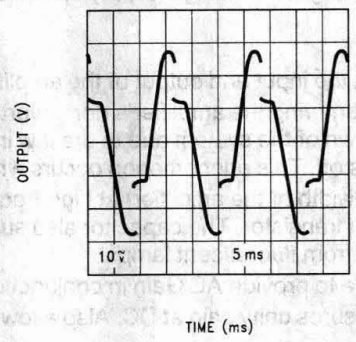
The optional external components shown in *Figure 2* and described above are applicable in both single and split voltage supply configurations.

Typical Performance Characteristics

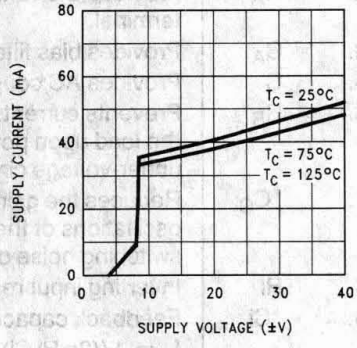
Safe Area



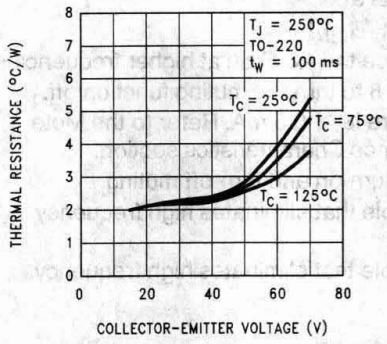
SPiKe Protection Response



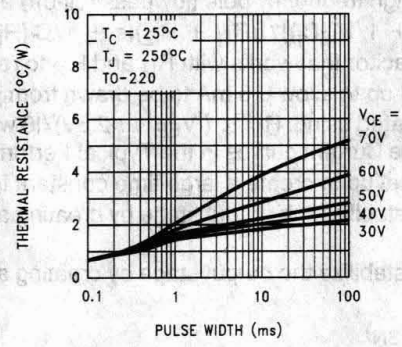
Supply Current vs Supply Voltage



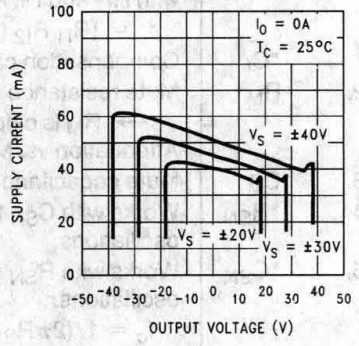
Pulse Thermal Resistance



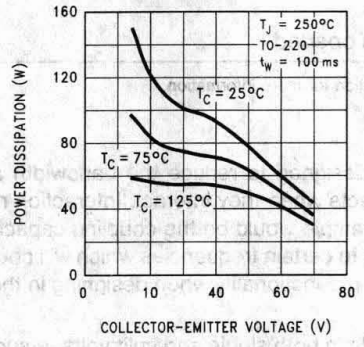
Pulse Thermal Resistance



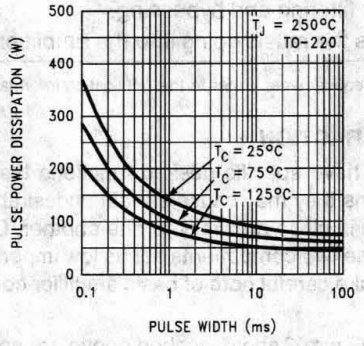
Supply Current vs Output Voltage



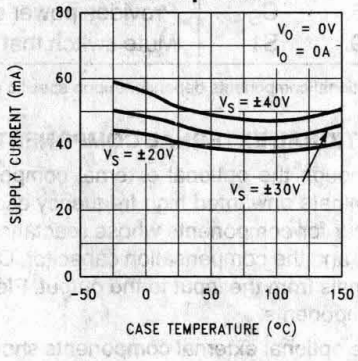
Pulse Power Limit



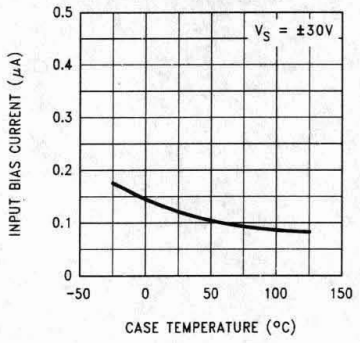
Pulse Power Limit



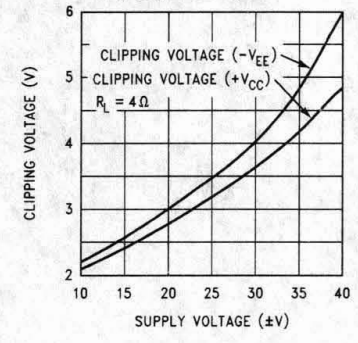
Supply Current vs Case Temperature



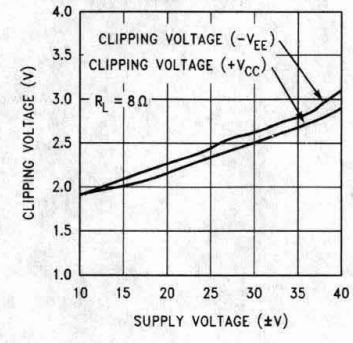
Input Bias Current vs Case Temperature



Clipping Voltage vs Supply Voltage



Clipping Voltage vs Supply Voltage



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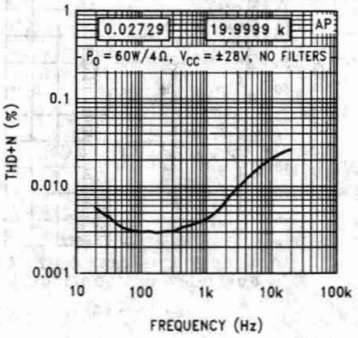
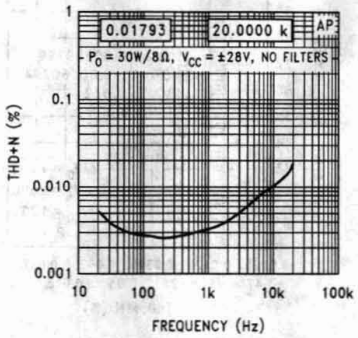
Typical Performance Characteristics (Continued)

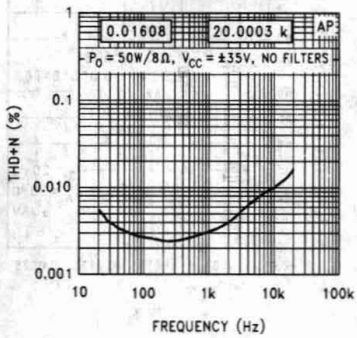
THD + N vs Frequency



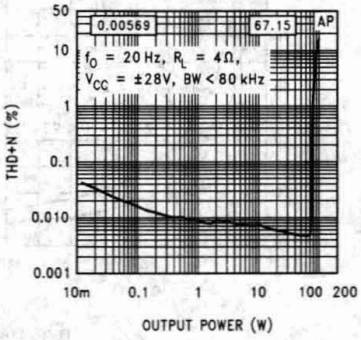
THD + N vs Frequency



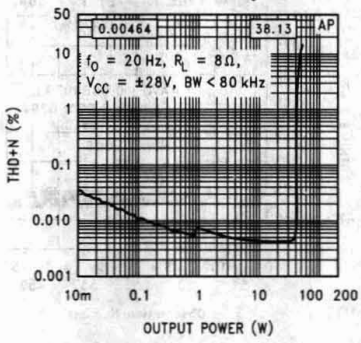
THD + N vs Frequency



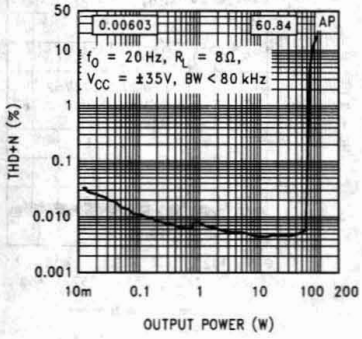
THD + N vs Output Power



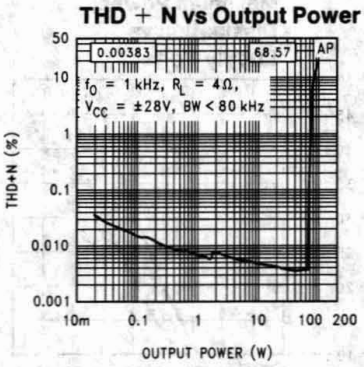
THD + N vs Output Power



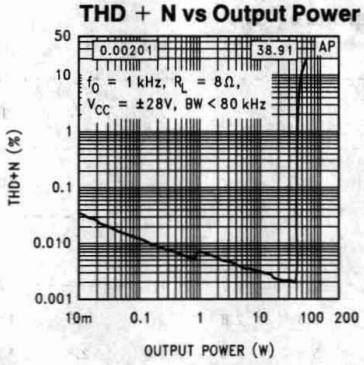
THD + N vs Output Power



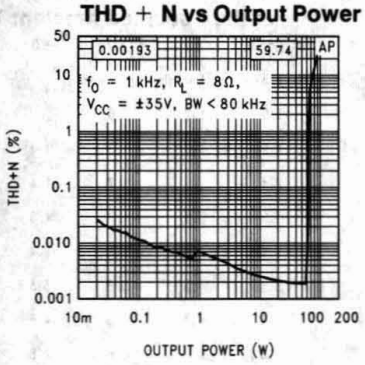
THD + N vs Output Power



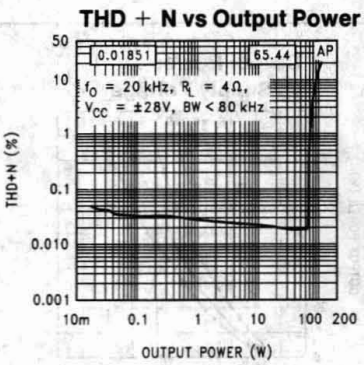
THD + N vs Output Power



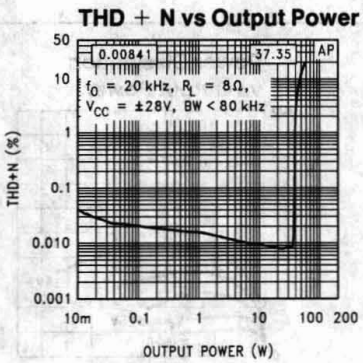
THD + N vs Output Power



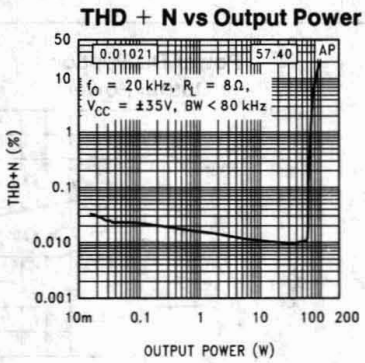
THD + N vs Output Power



THD + N vs Output Power



THD + N vs Output Power



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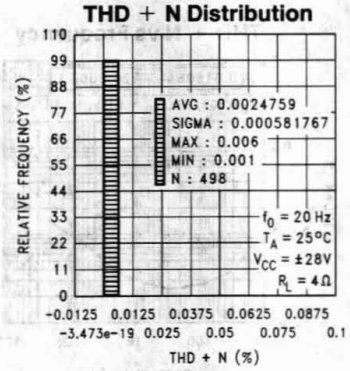
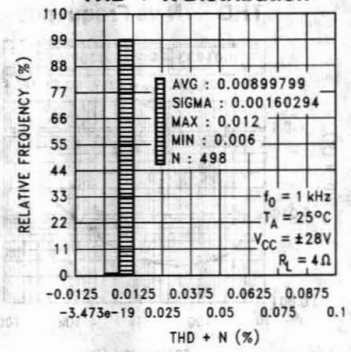
Typical Performance Characteristics (Continued)

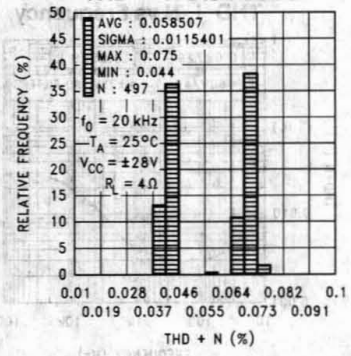
THD + N Distribution



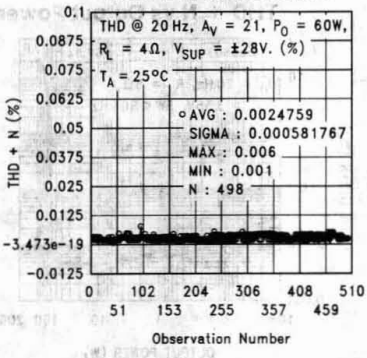
THD + N Distribution



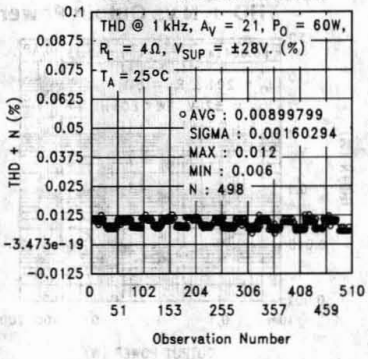
THD + N Distribution



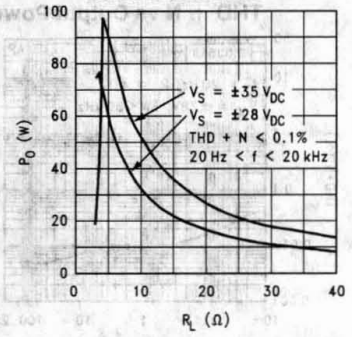
THD + N Distribution



THD + N Distribution



Output Power vs Load Resistance



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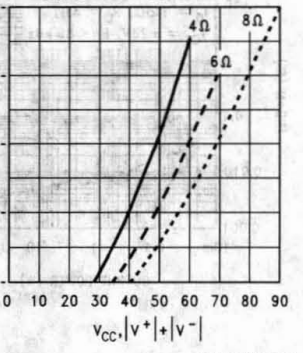
Max Heatsink Thermal Resistance (°C/W) at the Specified Ambient Temperature (°C)

T_A = 25°C	40	50	60	70	80	90	100	110	T_C, °C	P_D, W
1.3	1.0								90	50
1.6	1.2	1.0							96	45
1.9	1.6	1.3	1.1						102	40
2.4	1.9	1.7	1.4	1.1					108	35
3.0	2.5	2.1	1.8	1.5	1.1				114	30
3.8	3.2	2.8	2.4	2.0	1.6	1.2			120	25
5.1	4.3	3.8	3.3	2.8	2.3	1.8	1.3		126	20
7.1	6.1	5.5	4.8	4.1	3.5	2.8	2.1	1.5	132	15
11.3	9.8	8.8	7.8	6.8	5.8	4.8	3.8	2.8	138	10

Note: The maximum heat sink thermal resistance values, $\varnothing_{SA}$, in the table above were calculated using a $\varnothing_{CS}$ = 0.2°C/W due to thermal compound.

Maximum Power Dissipation vs Supply Voltage



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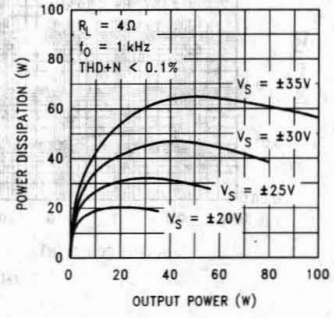
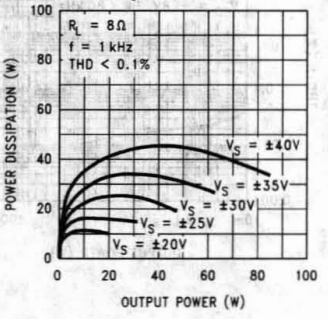
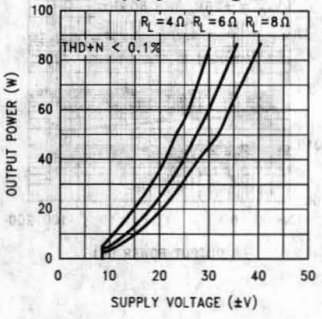
Power Dissipation vs Output Power



Power Dissipation vs Output Power



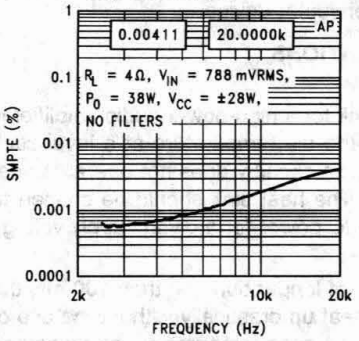
Output Power vs Supply Voltage



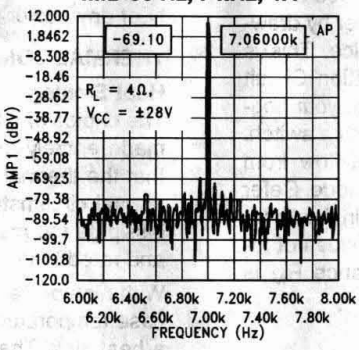
TL/H/11833-10

Typical Performance Characteristics (Continued)

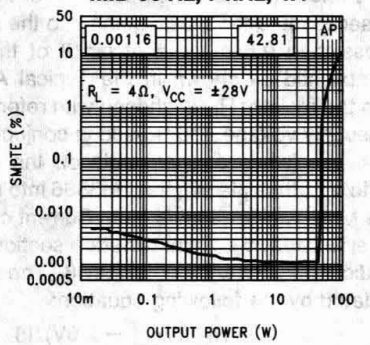
IMD 60 Hz, 4:1



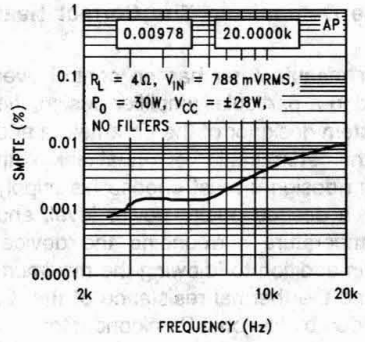
IMD 60 Hz, 7 kHz, 4:1



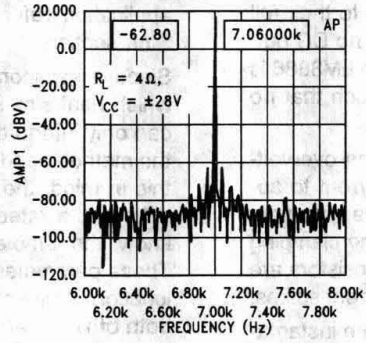
IMD 60 Hz, 7 kHz, 4:1



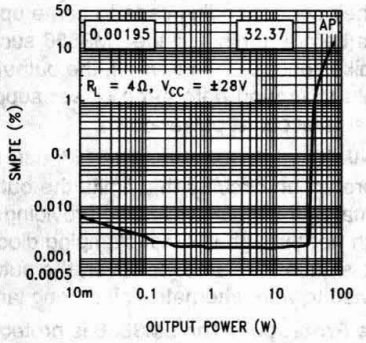
IMD 60 Hz, 1:1



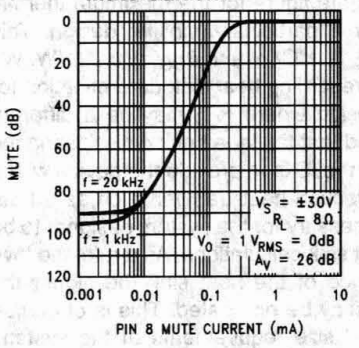
IMD 60 Hz, 7 kHz 1:1



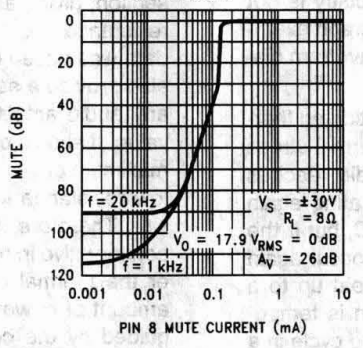
IMD 60 Hz, 7 kHz, 1:1



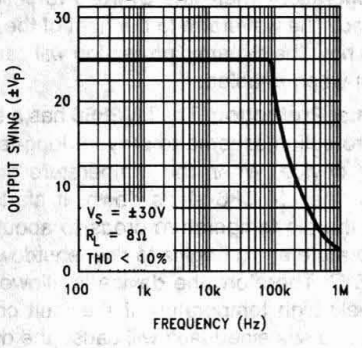
Mute Attenuation vs Mute Current



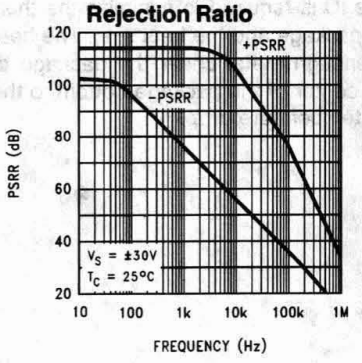
Mute Attenuation vs Mute Current



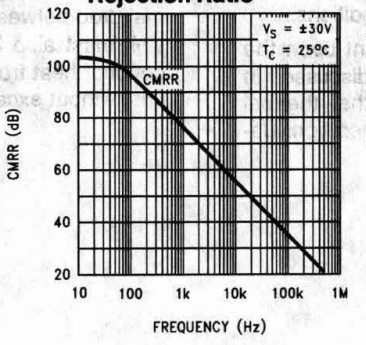
Large Signal Response



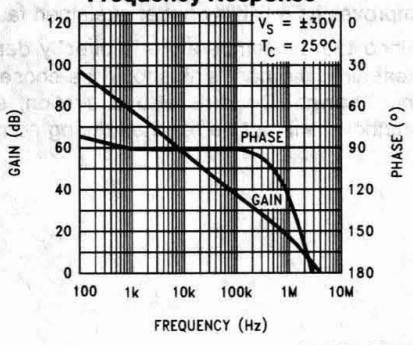
Power Supply Rejection Ratio



Common-Mode Rejection Ratio



Open Loop Frequency Response



TL/H/11833–11

Application Information

GENERAL FEATURES

Mute Function: The muting function of the LM3886 allows the user to mute the music going into the amplifier by drawing less than 0.5 mA out of pin 8 of the device. This is accomplished as shown in the Typical Application Circuit where the resistor R_M is chosen with reference to your negative supply voltage and is used in conjuction with a switch. The switch (when opened) cuts off the current flow from pin 8 to V^-, thus placing the LM3886 into mute mode. Refer to the Mute Attenuation vs Mute Current curves in the **Typical Performance Characteristics** section for values of attenuation per current out of pin 8. The resistance R_M is calculated by the following equation:

$$R_M (|V_{EE}| - 2.6V)/I8$$

where $I8 \geq 0.5$ mA.

Under-Voltage Protection: Upon system power-up the under-voltage protection circuitry allows the power supplies and their corresponding caps to come up close to their full values before turning on the LM3886 such that no DC output spikes occur. Upon turn-off, the output of the LM3886 is brought to ground before the power supplies such that no transients occur at power-down.

Over-Voltage Protection: The LM3886 contains overvoltage protection circuitry that limits the output current to approximately 11Apeak while also providing voltage clamping, though not through internal clamping diodes. The clamping effect is quite the same, however, the output transistors are designed to work alternately by sinking large current spikes.

SPiKe Protection: The LM3886 is protected from instantaneous peak-temperature stressing by the power transistor array. The Safe Operating Area graph in the **Typical Performance Characteristics** section shows the area of device operation where the **SPiKe** Protection Circuitry is not enabled. The waveform to the right of the SOA graph exemplifies how the dynamic protection will cause waveform distortion when enabled.

Thermal Protection: The LM3886 has a sophisticated thermal protection scheme to prevent long-term thermal stress to the device. When the temperature on the die reaches 165°C, the LM3886 shuts down. It starts operating again when the die temperature drops to about 155°C, but if the temperature again begins to rise, shutdown will occur again at 165°C. Therefore the device is allowed to heat up to a relatively high temperature if the fault condition is temporary, but a sustained fault will cause the device to cycle in a Schmitt Trigger fashion between the thermal shutdown temperature limits of 165°C and 155°C. This greatly reduces the stress imposed on the IC by thermal cycling, which in turn improves its reliability under sustained fault conditions.

Since the die temperature is directly dependent upon the heat sink, the heat sink should be chosen as discussed in the **Thermal Considerations** section, such that thermal shutdown will not be reached during normal operation. Using the best heat sink possible within the cost and space constraints of the system will improve the long-term reliability of any power semiconductor device.

THERMAL CONSIDERATIONS

Heat Sinking

The choice of a heat sink for a high-power audio amplifier is made entirely to keep the die temperature at a level such that the thermal protection circuitry does not operate under normal circumstances. The heat sink should be chosen to dissipate the maximum IC power for a given supply voltage and rated load.

With high-power pulses of longer duration than 100 ms, the case temperature will heat up drastically without the use of a heat sink. Therefore the case temperature, as measured at the center of the package bottom, is entirely dependent on heat sink design and the mounting of the IC to the heat sink. For the design of a heat sink for your audio amplifier application refer to the **Determining The Correct Heat Sink** section.

Since a semiconductor manufacturer has no control over which heat sink is used in a particular amplifier design, we can only inform the system designer of the parameters and the method needed in the determination of a heat sink. With this in mind, the system designer must choose his supply voltages, a rated load, a desired output power level, and know the ambient temperature surrounding the device. These parameters are in addition to knowing the maximum junction temperature and the thermal resistance of the IC, both of which are provided by National Semiconductor.

As a benefit to the system designer we have provided Maximum Power Dissipation vs Supply Voltages curves for various loads in the **Typical Performance Characteristics** section, giving an accurate figure for the maximum thermal resistance required for a particular amplifier design. This data was based on $\theta_{JC} = 1°C/W$ and $\theta_{CS} = 0.2°C/W$. We also provide a section regarding heat sink determination for any audio amplifier design where θ_{CS} may be a different value. It should be noted that the idea behind dissipating the maximum power within the IC is to provide the device with a low resistance to convection heat transfer such as a heat sink. Therefore, it is necessary for the system designer to be conservative in his heat sink calculations. As a rule, the lower the thermal resistance of the heat sink the higher the amount of power that may be dissipated. This is of course guided by the cost and size requirements of the system. Convection cooling heat sinks are available commercially, and their manufacturers should be consulted for ratings.

Proper mounting of the IC is required to minimize the thermal drop between the package and the heat sink. The heat sink must also have enough metal under the package to conduct heat from the center of the package bottom to the fins without excessive temperature drop.

Application Information (Continued)

A thermal grease such as Wakefield type 120 or Thermalloy Thermacote should be used when mounting the package to the heat sink. Without this compound, thermal resistance will be no better than 0.5°C/W, and probably much worse. With the compound, thermal resistance will be 0.2°C/W or less, assuming under 0.005 inch combined flatness runout for the package and heat sink. Proper torquing of the mounting bolts is important and can be determined from heat sink manufacturer's specification sheets.

Should it be necessary to isolate V^- from the heat sink, an insulating washer is required. Hard washers like beryluum oxide, anodized aluminum and mica require the use of thermal compound on both faces. Two-mil mica washers are most common, giving about 0.4°C/W interface resistance with the compound.

Silicone-rubber washers are also available. A 0.5°C/W thermal resistance is claimed without thermal compound. Experience has shown that these rubber washers deteriorate and must be replaced should the IC be dismounted.

Determining Maximum Power Dissipation

Power dissipation within the integrated circuit package is a very important parameter requiring a thorough understanding if optimum power output is to be obtained. An incorrect maximum power dissipation (P_D) calculation may result in inadequate heat sinking, causing thermal shutdown circuitry to operate and limit the output power.

The following equations can be used to acccurately calculate the maximum and average integrated circuit power dissipation for your amplifier design, given the supply voltage, rated load, and output power. These equations can be directly applied to the Power Dissipation vs Output Power curves in the **Typical Performance Characteristics** section.

Equation (1) exemplifies the maximum power dissipation of the IC and equations (2) and (3) exemplify the average IC power dissipation expressed in different forms.

$$P_{DMAX} = V_{CC}^2/2\pi^2R_L \quad (1)$$

where V_{CC} is the total supply voltage

$$P_{DAVE} = (V_{Opk}/R_L)[V_{CC}/\pi - V_{Opk}/2] \quad (2)$$

where V_{CC} is the total supply voltage and $V_{Opk} = V_{CC}/\pi$

$$P_{DAVE} = V_{CC}\,V_{Opk}/\pi R_L - V_{Opk}^2/2R_L \quad (3)$$

where V_{CC} is the total supply voltage.

Determining the Correct Heat Sink

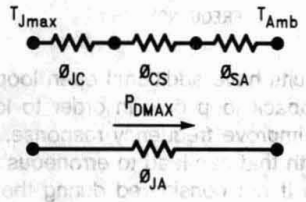
Once the maximum IC power dissipation is known for a given supply voltage, rated load, and the desired rated output power the maximum thermal resistance (in °C/W) of a heat sink can be calculated. This calculation is made using equation (4) and is based on the fact that thermal heat flow parameters are analogous to electrical current flow properties.

It is also known that typically the thermal resistance, θ_{JC} (junction to case), of the LM3886 is 1°C/W and that using Thermalloy Thermacote thermal compound provides a thermal resistance, θ_{CS} (case to heat sink), of about 0.2°C/W as explained in the **Heat Sinking** section.

Referring to the figure below, it is seen that the thermal resistance from the die (junction) to the outside air (ambient) is a combination of three thermal resistances, two of which are known, θ_{JC} and θ_{CS}. Since convection heat flow (power dissipation) is analogous to current flow, thermal resistance is analogous to electrical resistance, and temperature drops are analogous to voltage drops, the power dissipation out of the LM3886 is equal to the following:

$$P_{DMAX} = (T_{Jmax} - T_{Amb})/\theta_{JA}$$

where $\theta_{JA} = \theta_{JC} + \theta_{CS} + \theta_{SA}$



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But since we know P_{DMAX}, θ_{JC}, and θ_{SC} for the application and we are looking for θ_{SA}, we have the following:

$$\theta_{SA} = [(T_{Jmax} - T_{Amb}) - P_{DMAX}(\theta_{JC} + \theta_{CS})]/P_{DMAX} \quad (4)$$

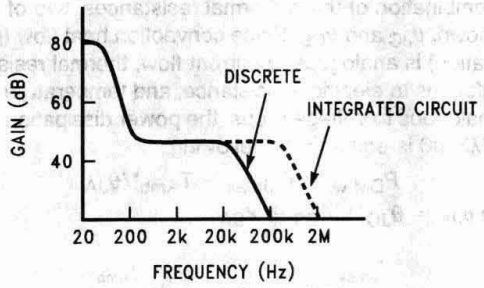
Again it must be noted that the value of θ_{SA} is dependent upon the system designer's amplifier application and its corresponding parameters as described previously. If the ambient temperature that the audio amplifier is to be working under is higher than the normal 25°C, then the thermal resistance for the heat sink, given all other things are equal, will need to be smaller.

Equations (1) and (4) are the only equations needed in the determination of the maximum heat sink thermal resistance. This is of course given that the system designer knows the required supply voltages to drive his rated load at a particular power output level and the parameters provided by the semiconductor manufacturer. These parameters are the junction to case thermal resistance, θ_{JC}, T_{Jmax} = 150°C, and the recommended Thermalloy Thermacote thermal compound resistance, θ_{CS}.

Application Information (Continued)

SIGNAL-TO-NOISE RATIO

In the measurement of the signal-to-noise ratio, misinterpretations of the numbers actually measured are common. One amplifier may sound much quieter than another, but due to improper testing techniques, they appear equal in measurements. This is often the case when comparing integrated circuit designs to discrete amplifier designs. Discrete transistor amps often "run out of gain" at high frequencies and therefore have small bandwidths to noise as indicated below.



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Integrated circuits have additional open loop gain allowing additional feedback loop gain in order to lower harmonic distortion and improve frequency response. It is this additional bandwidth that can lead to erroneous signal-to-noise measurements if not considered during the measurement process. In the typical example above, the difference in bandwidth appears small on a log scale but the factor of 10 in bandwidth, (200 kHz to 2 MHz) can result in a 10 dB theoretical difference in the signal-to-noise ratio (white noise is proportional to the square root of the bandwidth in a system).

In comparing audio amplifiers it is necessary to measure the magnitude of noise in the audible bandwidth by using a "weighting" filter.[1] A "weighting" filter alters the frequency response in order to compensate for the average human ear's sensitivity to the frequency spectra. The weighting filters at the same time provide the bandwidth limiting as discussed in the previous paragraph.

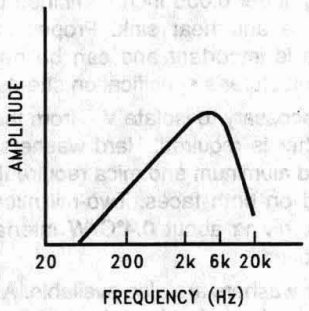
In addition to noise filtering, differing meter types give different noise readings. Meter responses include:

1. RMS reading,
2. average responding,
3. peak reading, and
4. quasi peak reading.

Although theoretical noise analysis is derived using true RMS based calculations, most actual measurements are taken with ARM (Average Responding Meter) test equipment.

Reference 1: CCIR/ARM: *A Practical Noise Measurement Method;* by Ray Dolby, David Robinson and Kenneth Gundry, AES Preprint No. 1353 (F-3).

Typical signal-to-noise figures are listed for an A-weighted filter which is commonly used in the measurement of noise. The shape of all weighting filters is similar, with the peak of the curve usually occurring in the 3 kHz–7 kHz region as shown below.



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SUPPLY BYPASSING

The LM3886 has excellent power supply rejection and does not require a regulated supply. However, to eliminate possible oscillations all op amps and power op amps should have their supply leads bypassed with low-inductance capacitors having short leads and located close to the package terminals. Inadequate power supply bypassing will manifest itself by a low frequency oscillation known as "motorboating" or by high frequency instabilities. These instabilities can be eliminated through multiple bypassing utilizing a large tantalum or electrolytic capacitor (10 μF or larger) which is used to absorb low frequency variations and a small ceramic capacitor (0.1 μF) to prevent any high frequency feedback through the power supply lines.

If adequate bypassing is not provided the current in the supply leads which is a rectified component of the load current may be fed back into internal circuitry. This signal causes low distortion at high frequencies requiring that the supplies be bypassed at the package terminals with an electrolytic capacitor of 470 μF or more.

LEAD INDUCTANCE

Power op amps are sensitive to inductance in the output lead, particularly with heavy capacitive loading. Feedback to the input should be taken directly from the output terminal, minimizing common inductance with the load.

Lead inductance can also cause voltage surges on the supplies. With long leads to the power supply, energy is stored in the lead inductance when the output is shorted. This energy can be dumped back into the supply bypass capacitors when the short is removed. The magnitude of this transient is reduced by increasing the size of the bypass capacitor near the IC. With at least a 20 μF local bypass, these voltage surges are important only if the lead length exceeds a couple feet (>1 μH lead inductance). Twisting together the supply and ground leads minimizes the effect.

Application Information (Continued)

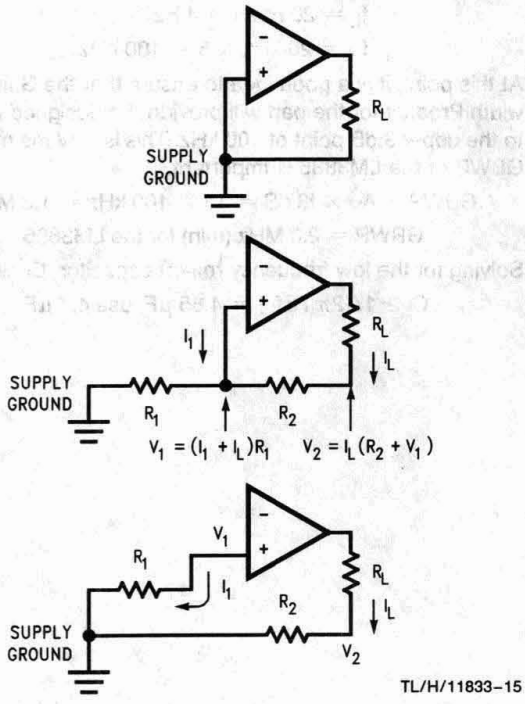
LAYOUT, GROUND LOOPS AND STABILITY

The LM3886 is designed to be stable when operated at a closed-loop gain of 10 or greater, but as with any other high-current amplifier, the LM3886 can be made to oscillate under certain conditions. These usually involve printed circuit board layout or output/input coupling.

When designing a layout, it is important to return the load ground, the output compensation ground, and the low level (feedback and input) grounds to the circuit board common ground point through separate paths. Otherwise, large currents flowing along a ground conductor will generate voltages on the conductor which can effectively act as signals at the input, resulting in high frequency oscillation or excessive distortion. It is advisable to keep the output compensation components and the 0.1 μF supply decoupling capacitors as close as possible to the LM3886 to reduce the effects of PCB trace resistance and inductance. For the same reason, the ground return paths should be as short as possible.

In general, with fast, high-current circuitry, all sorts of problems can arise from improper grounding which again can be avoided by returning all grounds separately to a common point. Without isolating the ground signals and returning the grounds to a common point, ground loops may occur.

"Ground Loop" is the term used to describe situations occurring in ground systems where a difference in potential exists between two ground points. Ideally a ground is a ground, but unfortunately, in order for this to be true, ground conductors with zero resistance are necessary. Since real world ground leads possess finite resistance, currents running through them will cause finite voltage drops to exist. If two ground return lines tie into the same path at different points there will be a voltage drop between them. The first figure below shows a common ground example where the positive input ground and the load ground are returned to the supply ground point via the same wire. The addition of the finite wire resistance, R_2, results in a voltage difference between the two points as shown below.



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The load current I_L will be much larger than input bias current I_I, thus V_1 will follow the output voltage directly, i.e. in phase. Therefore the voltage appearing at the non-inverting input is effectively positive feedback and the circuit may oscillate. If there were only one device to worry about then the values of R_1 and R_2 would probably be small enough to be ignored; however, several devices normally comprise a total system. Any ground return of a separate device, whose output is in phase, can feedback in a similar manner and cause instabilities. Out of phase ground loops also are troublesome, causing unexpected gain and phase errors.

The solution to most ground loop problems is to always use a single-point ground system, although this is sometimes impractical. The third figure below is an example of a single-point ground system.

The single-point ground concept should be applied rigorously to all components and all circuits when possible. Violations of single-point grounding are most common among printed circuit board designs, since the circuit is surrounded by large ground areas which invite the temptation to run a device to the closest ground spot. As a final rule, make all ground returns low resistance and low inductance by using large wire and wide traces.

Occasionally, current in the output leads (which function as antennas) can be coupled through the air to the amplifier input, resulting in high-frequency oscillation. This normally happens when the source impedance is high or the input leads are long. The problem can be eliminated by placing a small capacitor, C_C, (on the order of 50 pF to 500 pF) across the LM3886 input terminals. Refer to the **External Components Description** section relating to component interaction with C_f.

REACTIVE LOADING

It is hard for most power amplifiers to drive highly capacitive loads very effectively and normally results in oscillations or ringing on the square wave response. If the output of the LM3886 is connected directly to a capacitor with no series resistance, the square wave response will exhibit ringing if the capacitance is greater than about 0.2 μF. If highly capacitive loads are expected due to long speaker cables, a method commonly employed to protect amplifiers from low impedances at high frequencies is to couple to the load through a 10Ω resistor in parallel with a 0.7 μH inductor. The inductor-resistor combination as shown in the **Typical Application Circuit** isolates the feedback amplifier from the load by providing high output impedance at high frequencies thus allowing the 10Ω resistor to decouple the capacitive load and reduce the Q of the series resonant circuit. The LR combination also provides low output impedance at low frequencies thus shorting out the 10Ω resistor and allowing the amplifier to drive the series RC load (large capacitive load due to long speaker cables) directly.

Application Information (Continued)

GENERALIZED AUDIO POWER AMPLIFIER DESIGN

The system designer usually knows some of the following parameters when starting an audio amplifier design:

Desired Power Output	Input Level
Input Impedance	Load Impedance
Maximum Supply Voltage	Bandwidth

The power output and load impedance determine the power supply requirements, however, depending upon the application some system designers may be limited to certain maximum supply voltages. If the designer does have a power supply limitation, he should choose a practical load impedance which would allow the amplifier to provide the desired output power, keeping in mind the current limiting capabilities of the device. In any case, the output signal swing and current are found from (where P_O is the average output power):

$$V_{opeak} = \sqrt{2\,R_L\,P_O} \quad (1)$$

$$I_{opeak} = \sqrt{(2\,P_O)/R_L} \quad (2)$$

To determine the maximum supply voltage the following parameters must be considered. Add the dropout voltage (4V for LM3886) to the peak output swing, V_{opeak}, to get the supply rail value (i.e. $\pm$ (V_{opeak} + Vod) at a current of I_{opeak}). The regulation of the supply determines the unloaded voltage, usually about 15% higher. Supply voltage will also rise 10% during high line conditions. Therefore, the maximum supply voltage is obtained from the following equation:

Max. supplies $\approx \pm$ (V_{opeak} + Vod)(1 + regulation)(1.1) (3)

The input sensitivity and the output power specs determine the minimum required gain as depicted below:

$$A_V \geq (\sqrt{P_O\,R_L})/(V_{IN}) = V_{orms}/V_{inrms} \quad (4)$$

Normally the gain is set between 20 and 200; for a 40W, 8Ω audio amplifier this results in a sensitivity of 894 mV and 89 mV, respectively. Although higher gain amplifiers provide greater output power and dynamic headroom capabilities, there are certain shortcomings that go along with the so called "gain." The input referred noise floor is increased and hence the SNR is worse. With the increase in gain, there is also a reduction of the power bandwidth which results in a decrease in feedback thus not allowing the amplifier to respond quickly enough to nonlinearities. This decreased ability to respond to nonlinearities increases the THD + N specification.

The desired input impedance is set by R_{IN}. Very high values can cause board layout problems and DC offsets at the output. The value for the feedback resistance, R_{f1}, should be chosen to be a relatively large value (10 kΩ–100 kΩ), and the other feedback resistance, Ri, is calculated using standard op amp configuration gain equations. Most audio amplifiers are designed from the non-inverting amplifier configuration.

DESIGN A 40W/4Ω AUDIO AMPLIFIER

Given:

Power Output	40W
Load Impedance	4Ω
Input Level	1V(max)
Input Impedance	100 kΩ
Bandwidth	20 Hz–20 kHz ± 0.25 dB

Equations (1) and (2) give:

40W/4Ω V_{opeak} = 17.9V I_{opeak} = 4.5A

Therefore the supply required is: ±21.0V @ 4.5A

With 15% regulation and high line the final supply voltage is ±26.6V using equation (3). At this point it is a good idea to check the Power Output vs Supply Voltage to ensure that the required output power is obtainable from the device while maintaining low THD + N. It is also good to check the Power Dissipation vs Supply Voltage to ensure that the device can handle the internal power dissipation. At the same time designing in a relatively practical sized heat sink with a low thermal resistance is also important. Refer to **Typical Performance Characteristics** graphs and the **Thermal Considerations** section for more information.

The minimum gain from equation (4) is: $A_V \geq 12.6$

We select a gain of 13 (Non-Inverting Amplifier); resulting in a sensitivity of 973 mV.

Letting R_{IN} equal 100 kΩ gives the required input impedance, however, this would eliminate the "volume control" unless an additional input impedance was placed in series with the 10 kΩ potentiometer that is depicted in *Figure 1*. Adding the additional 100 kΩ resistor would ensure the minumum required input impedance.

For low DC offsets at the output we let R_{f1} = 100 kΩ. Solving for Ri (Non-Inverting Amplifier) gives the following:

$Ri = R_{f1}/(A_V - 1) = 100k/(13 - 1) = 8.3\ k\Omega$; use 8.2 kΩ

The bandwidth requirement must be stated as a pole, i.e., the 3 dB frequency. Five times away from a pole gives 0.17 dB down, which is better than the required 0.25 dB. Therefore:

$$f_L = 20\ Hz/5 = 4\ Hz$$

$$f_H = 20\ kHz \times 5 = 100\ kHz$$

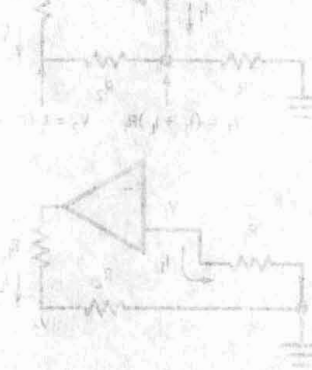
At this point, it is a good idea to ensure that the Gain-Bandwidth Product for the part will provide the designed gain out to the upper 3 dB point of 100 kHz. This is why the minimum GBWP of the LM3886 is important.

$$GBWP \geq A_V \times f3\ dB = 13 \times 100\ kHz = 1.3\ MHz$$

GBWP = 2.0 MHz (min) for the LM3886

Solving for the low frequency roll-off capacitor, Ci, we have:

$$Ci \geq 1/(2\pi\ Ri\ f_L) = 4.85\ \mu F;\ \text{use } 4.7\ \mu F.$$



Definition of Terms

Input Offset Voltage: The absolute value of the voltage which must be applied between the input terminals through two equal resistances to obtain zero output voltage and current.

Input Bias Current: The absolute value of the average of the two input currents with the output voltage and current at zero.

Input Offset Current: The absolute value of the difference in the two input currents with the output voltage and current at zero.

Input Common-Mode Voltage Range (or Input Voltage Range): The range of voltages on the input terminals for which the amplifier is operational. Note that the specifications are not guaranteed over the full common-mode voltage range unless specifically stated.

Common-Mode Rejection: The ratio of the input common-mode voltage range to the peak-to-peak change in input offset voltage over this range.

Power Supply Rejection: The ratio of the change in input offset voltage to the change in power supply voltages producing it.

Quiescent Supply Current: The current required from the power supply to operate the amplifier with no load and the output voltage and current at zero.

Slew Rate: The internally limited rate of change in output voltage with a large amplitude step function applied to the input.

Class B Amplifier: The most common type of audio power amplifier that consists of two output devices each of which conducts for 180° of the input cycle. The LM3886 is a Quasi-AB type amplifier.

Crossover Distortion: Distortion caused in the output stage of a class B amplifier. It can result from inadequate bias current providing a dead zone where the output does not respond to the input as the input cycle goes through its zero crossing point. Also for ICs an inadequate frequency response of the output PNP device can cause a turn-on delay giving crossover distortion on the negative going transition through zero crossing at the higher audio frequencies.

THD + N: Total Harmonic Distortion plus Noise refers to the measurement technique in which the fundamental component is removed by a bandreject (notch) filter and all remaining energy is measured including harmonics and noise.

Signal-to-Noise Ratio: The ratio of a system's output signal level to the system's output noise level obtained in the absence of a signal. The output reference signal is either specified or measured at a specified distortion level.

Continuous Average Output Power: The minimum sine wave continuous average power output in watts (or dBW) that can be delivered into the rated load, over the rated bandwidth, at the rated maximum total harmonic distortion.

Music Power: A measurement of the peak output power capability of an amplifier with either a signal duration sufficiently short that the amplifier power supply does not sag during the measurement, or when high quality external power supplies are used. This measurement (an IHF standard) assumes that with normal music program material the amplifier power supplies will sag insignificantly.

Peak Power: Most commonly referred to as the power output capability of an amplifier that can be delivered to the load; specified by the part's maximum voltage swing.

Headroom: The margin between an actual signal operating level (usually the power rating of the amplifier with particular supply voltages, a rated load value, and a rated THD + N figure) and the level just before clipping distortion occurs, expressed in decibels.

Large Signal Voltage Gain: The ratio of the output voltage swing to the differential input voltage required to drive the output from zero to either swing limit. The output swing limit is the supply voltage less a specified quasi-saturation voltage. A pulse of short enough duration to minimize thermal effects is used as a measurement signal.

Output-Current Limit: The output current with a fixed output voltage and a large input overdrive. The limiting current drops with time once **SPiKe** protection circuitry is activated.

Output Saturation Threshold (Clipping Point): The output swing limit for a specified input drive beyond that required for zero output. It is measured with respect to the supply to which the output is swinging.

Output Resistance: The ratio of the change in output voltage to the change in output current with the output around zero.

Power Dissipation Rating: The power that can be dissipated for a specified time interval without activating the protection circuitry. For time intervals in excess of 100 ms, dissipation capability is determined by heat sinking of the IC package rather than by the IC itself.

Thermal Resistance: The peak, junction-temperature rise, per unit of internal power dissipation (units in °C/W), above the case temperature as measured at the center of the package bottom.

The DC thermal resistance applies when one output transistor is operating continuously. The AC thermal resistance applies with the output transistors conducting alternately at a high enough frequency that the peak capability of neither transistor is exceeded.

Power Bandwidth: The power bandwidth of an audio amplifier is the frequency range over which the amplifier voltage gain does not fall below 0.707 of the flat band voltage gain specified for a given load and output power.

Power bandwidth also can be measured by the frequencies at which a specified level of distortion is obtained while the amplifier delivers a power output 3 dB below the rated output. For example, an amplifier rated at 60W with ≤ 0.25% THD + N, would make its power bandwidth measured as the difference between the upper and lower frequencies at which 0.25% distortion was obtained while the amplifier was delivering 30W.

Gain-Bandwidth Product: The Gain-Bandwidth Product is a way of predicting the high-frequency usefulness of an op amp. The Gain-Bandwidth Product is sometimes called the unity-gain frequency or unity-gain cross frequency because the open-loop gain characteristic passes through or crosses unity gain at this frequency. Simply, we have the following relationship: $A_{CL1} \times f_1 = A_{CL2} \times f_2$

Assuming that at unity-gain ($A_{CL1} = 1$ or (0 dB)) fu = fi = GBWP, then we have the following: GBWP = $A_{CL2} \times f2$

This says that once fu (GBWP) is known for an amplifier, then the open-loop gain can be found at any frequency. This is also an excellent equation to determine the 3 dB point of a closed-loop gain, assuming that you know the GBWP of the device. Refer to the diagram on the following page.

Definition of Terms (Continued)

Biamplification: The technique of splitting the audio frequency spectrum into two sections and using individual power amplifiers to drive a separate woofer and tweeter. Crossover frequencies for the amplifiers usually vary between 500 Hz and 1600 Hz. "Biamping" has the advantages of allowing smaller power amps to produce a given sound pressure level and reducing distortion effects produsedby overdrive in one part of the frequency spectrum affecting the other part.

C.C.I.R./A.R.M.:

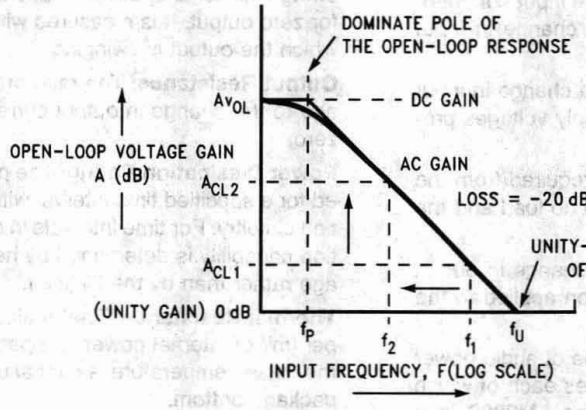
Literally: International Radio Consultative Committee
Average Responding Meter

This refers to a weighted noise measurement for a Dolby B type noise reduction system. A filter characteristic is used that gives a closer correlation of the measurement with the subjective annoyance of noise to the ear. Measurements made with this filter cannot necessarily be related to unweighted noise measurements by some fixed conversion factor since the answers obtained will depend on the spectrum of the noise source.

S.P.L.: Sound Pressure Level—usually measured with a microphone/meter combination calibrated to a pressure level of 0.0002 μBars (approximately the threshold hearing level).

$$S.P.L. = 20 \text{ Log } 10P/0.0002 \text{ dB}$$

where P is the R.M.S. sound pressure in microbars.
(1 Bar = 1 atmosphere = 14.5 lb/in^2 = 194 dB S.P.L.).



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National Semiconductor

LM4860 Boomer® Audio Power Amplifier Series
1W Audio Power Amplifier with Shutdown Mode

General Description

The LM4860 is a bridge-connected audio power amplifier capable of delivering 1W of continuous average power to an 8Ω load with less than 1% (THD+N) over the audio spectrum from a 5V power supply.

Boomer audio power amplifiers were designed specifically to provide high quality output power with a minimal amount of external components using surface mount packaging. Since the LM4860 does not require output coupling capacitors, bootstrap capacitors or snubber networks, it is optimally suited for low-power portable systems.

The LM4860 features an externally controlled, low-power consumption shutdown mode, as well as an internal thermal shutdown protection mechanism. It also includes two headphone control inputs and a headphone sense output for external monitoring.

The unity-gain stable LM4860 can be configured by external gain setting resistors for differential gains of 1 to 10 without the use of external compensation components.

Key Specifications

- THD+N at 1W continuous average output power into 8Ω — 1% (max)
- Instantaneous peak output power — >2W
- Shutdown current — 0.6 μA (typ)

Features

- No output coupling capacitors, bootstrap capacitors, or snubber circuits are necessary
- Small Outline (SO) power packaging
- Compatible with PC power supplies
- Thermal shutdown protection circuitry
- Unity-gain stable
- External gain configuration capability
- Two headphone control inputs and headphone sensing output

Applications

- Personal computers
- Portable consumer products
- Cellular phones
- Self-powered speakers
- Toys and games

Typical Application

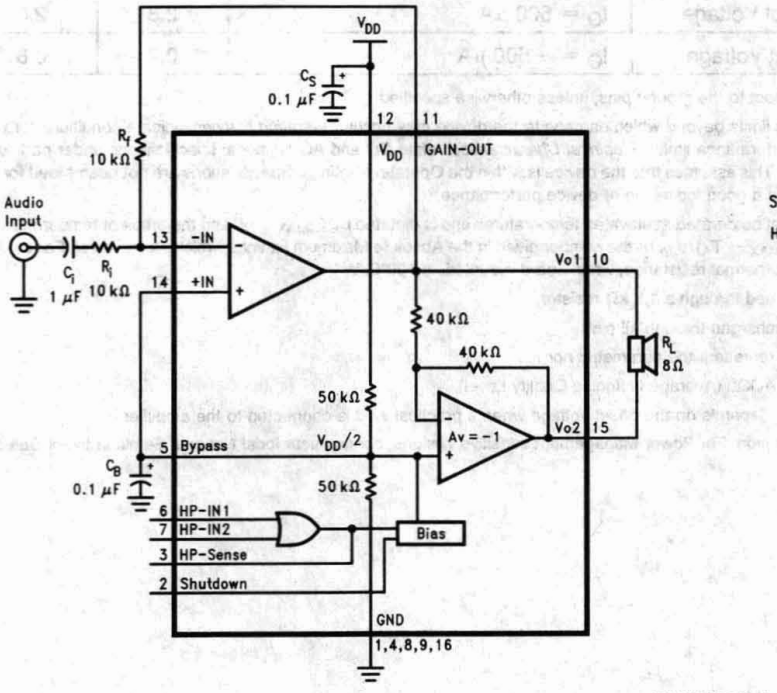

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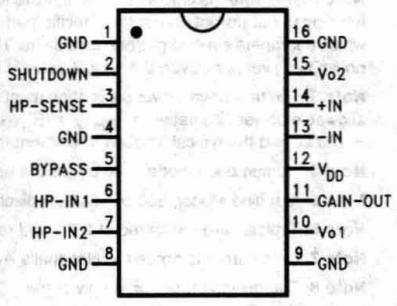
FIGURE 1. Typical Audio Amplifier Application Circuit

Connection Diagram

Small Outline Package



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Top View

Order Number LM4860M
See NS Package Number M16A

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	6.0V
Storage Temperature	−65°C to +150°C
Input Voltage	−0.3V to V_{DD} + 0.3V
Power Dissipation	Internally limited
ESD Susceptibility (Note 4)	3000V
ESD Susceptibility (Note 5)	250V
Junction Temperature	150°C
Soldering Information	
Small Outline Package	
Vapor Phase (60 sec.)	215°C
Infrared (15 sec.)	220°C

See AN-450 *"Surface Mounting and their Effects on Product Reliability" for other methods of soldering surface mount devices.*

Operating Ratings

Temperature Range	
$T_{MIN} \le T_A \le T_{MAX}$	$-20°C \le T_A \le +85°C$
Supply Voltage	$2.7V \le V_{DD} \le 5.5V$

Electrical Characteristics (Notes 1, 2)

The following specifications apply for V_{DD} = 5V, R_L = 8Ω unless otherwise specified. Limits apply for T_A = 25°C.

Symbol	Parameter	Conditions	LM4860		Units (Limits)
			Typical (Note 6)	Limit (Note 7)	
V_{DD}	Supply Voltage			2.7 5.5	V (min) V (max)
I_{DD}	Quiescent Power Supply Current	V_O = 0V, I_O = 0A (Note 8)	7.0	15.0	mA (max)
I_{SD}	Shutdown Current	$V_{pin2} = V_{DD}$ (Note 9)	0.6		μA
V_{OS}	Output Offset Voltage	V_{IN} = 0V	5.0	50.0	mV (max)
P_O	Output Power	THD+N = 1% (max); f = 1 kHz	1.15	1.0	W (min)
THD+N	Total Harmonic Distortion + Noise	P_O = 1 Wrms; 20 Hz ≤ f ≤ 20 kHz	0.72		%
PSRR	Power Supply Rejection Ratio	V_{DD} = 4.9V to 5.1V	65		dB
V_{od}	Output Dropout Voltage	V_{IN} = 0V to 5V, $V_{od} = (V_{o1} - V_{o2})$	0.6	1.0	V (max)
V_{IH}	HP-IN High Input Voltage	HP-SENSE = 0V to 4V	2.5		V
V_{IL}	HP-IN Low Input Voltage	HP-SENSE = 4V to 0V	2.5		V
V_{OH}	HP-SENSE High Output Voltage	I_O = 500 μA	2.8	2.5	V (min)
V_{OL}	HP-SENSE Low Output Voltage	I_O = −500 μA	0.2	0.8	V (max)

Note 1: All voltages are measured with respect to the ground pins, unless otherwise specified.

Note 2: *Absolute Maximum Ratings* indicate limits beyond which damage to the device may occur. *Operating Ratings* indicate conditions for which the device is functional, but do not guarantee specific performance limits. *Electrical Characteristics* state DC and AC electrical specifications under particular test conditions which guarantee specific performance limits. This assumes that the device is within the Operating Ratings. Specifications are not guaranteed for parameters where no limit is given, however, the typical value is a good indication of device performance.

Note 3: The maximum power dissipation must be derated at elevated temperatures and is dictated by T_{JMAX}, θ_{JA}, and the ambient temperature T_A. The maximum allowable power dissipation is $P_{DMAX} = (T_{JMAX} - T_A)/\theta_{JA}$ or the number given in the Absolute Maximum Ratings, whichever is lower. For the LM4860, T_{JMAX} = +150°C, and the typical junction-to-ambient thermal resistance, when board mounted, is 100°C/W.

Note 4: Human body model, 100 pF discharged through a 1.5 kΩ resistor.

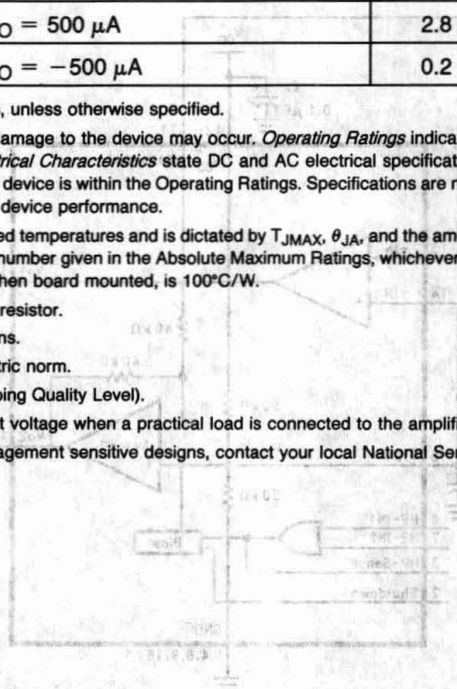
Note 5: Machine Model, 200 pF–240 pF discharged through all pins.

Note 6: Typicals are measured at 25°C and represent the parametric norm.

Note 7: Limits are guaranteed to National's AOQL (Average Outgoing Quality Level).

Note 8: The quiescent power supply current depends on the offset voltage when a practical load is connected to the amplifier.

Note 9: Shutdown current has a wide distribution. For Power Management sensitive designs, contact your local National Semiconductor Sales Office.



High Gain Application Circuit

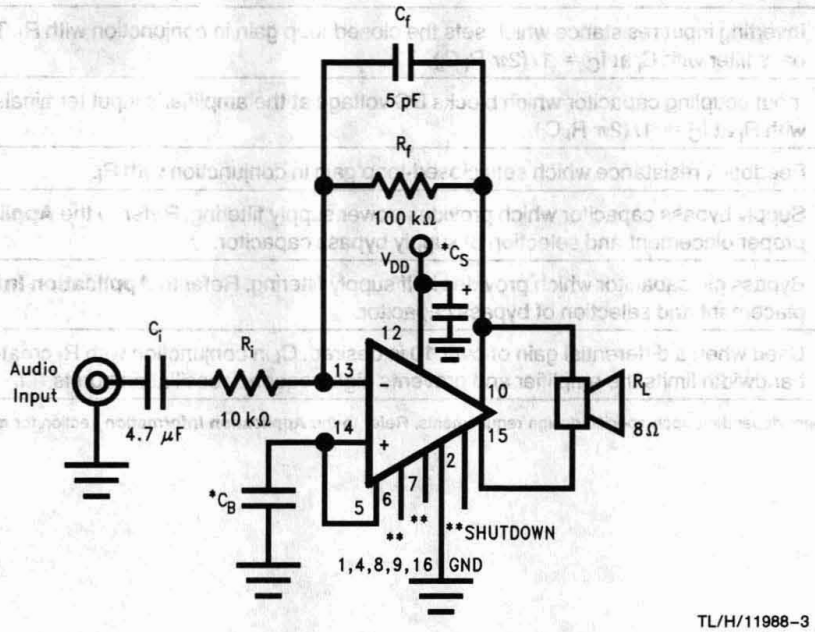


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FIGURE 2. Stereo Amplifier with $A_{VD} = 20$

Single Ended Application Circuit

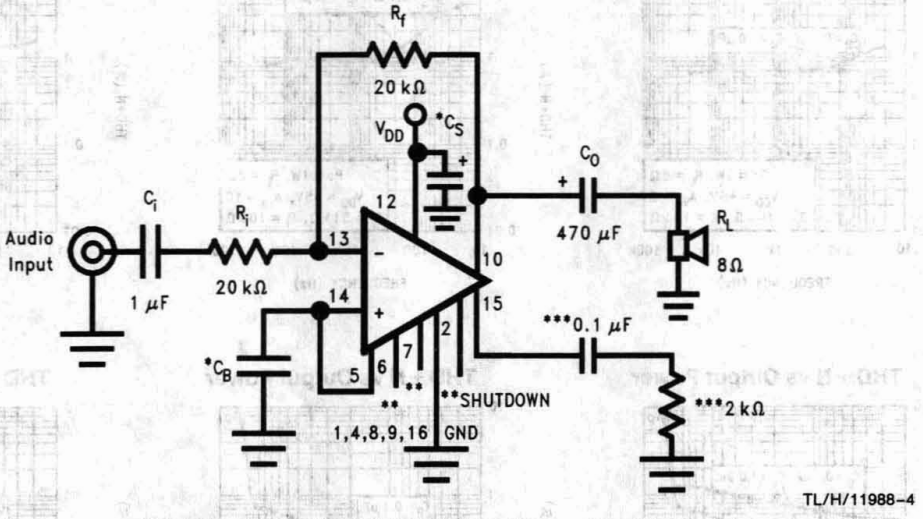

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FIGURE 3. Single-Ended Amplifier with $A_V = -1$

*C_S and C_B size depend on specific application requirements and constraints. Typical values of C_S and C_B are 0.1 μF.

**Pin 2, 6, or 7 should be connected to V_{DD} to disable the amplifier or to GND to enable the amplifier. These pins should not be left floating.

***These components create a "dummy" load for pin 8 for stability purposes.

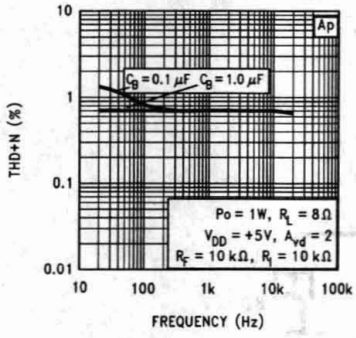
External Components Description *(Figures 1, 2)*

Components	Functional Description
1. R_i	Inverting input resistance which sets the closed-loop gain in conjunction with R_f. This resistor also forms a high pass filter with C_i at $f_C = 1/(2\pi R_i C_i)$.
2. C_i	Input coupling capacitor which blocks DC voltage at the amplifier's input terminals. Also creates a highpass filter with R_i at $f_C = 1/(2\pi R_i C_i)$.
3. R_f	Feedback resistance which sets closed-loop gain in conjunction with R_i.
4. C_S	Supply bypass capacitor which provides power supply filtering. Refer to the **Application Information** section for proper placement and selection of supply bypass capacitor.
5. C_B	Bypass pin capacitor which provides half supply filtering. Refer to **Application Information** section for proper placement and selection of bypass capacitor.
6. C_f*	Used when a differential gain of over 10 is desired. C_f in conjunction with R_f creates a low-pass filter which bandwidth limits the amplifier and prevents high frequency oscillation bursts. $f_C = 1/(2\pi R_f C_f)$

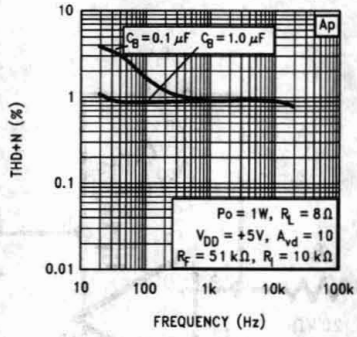
*Optional component dependent upon specific design requirements. Refer to the **Application Information** section for more in formation.

Typical Performance Characteristics

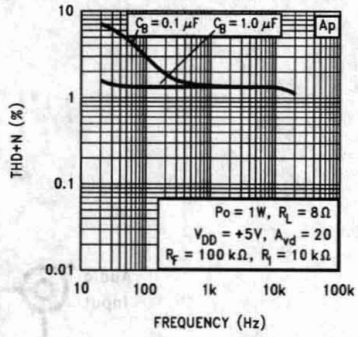
THD + N vs Frequency



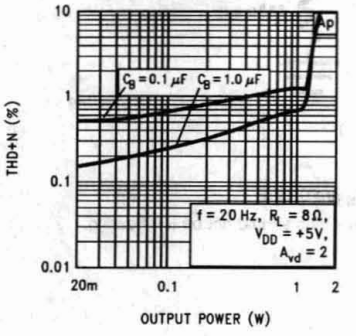
THD + N vs Frequency



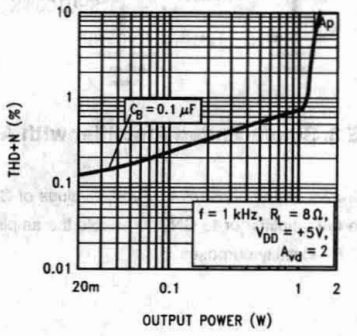
THD + N vs Frequency



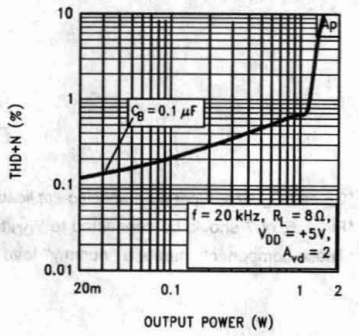
THD + N vs Output Power



THD + N vs Output Power



THD + N vs Output Power



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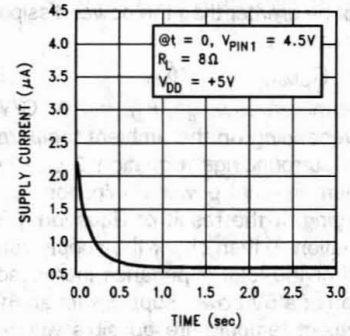
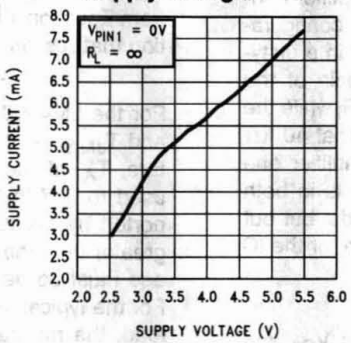
Typical Performance Characteristics (Continued)

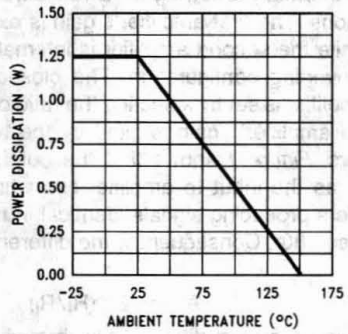
Supply Current vs Time in Shutdown Mode



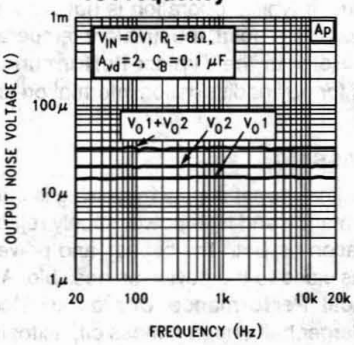
Supply Current vs Supply Voltage



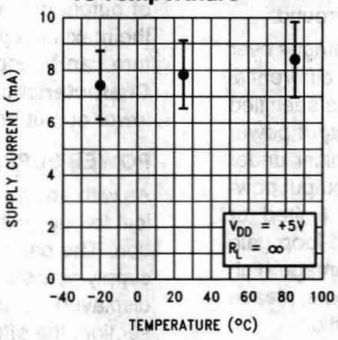
Power Derating Curve



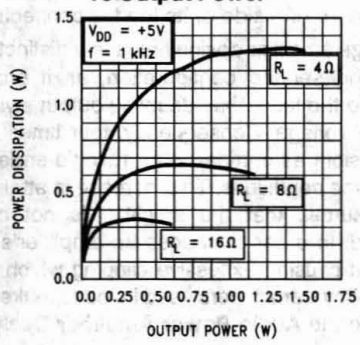
LM4860 Noise Floor vs Frequency



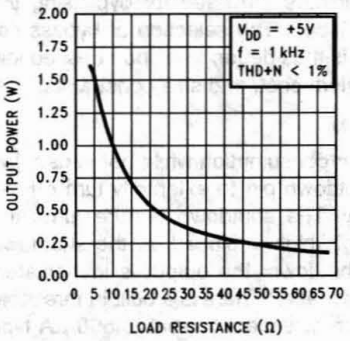
Supply Current Distribution vs Temperature



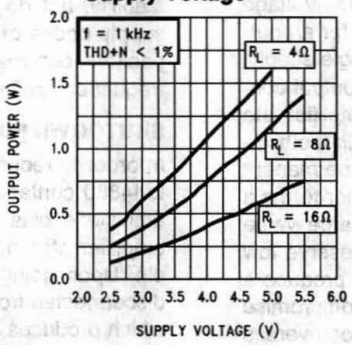
Power Dissipation vs Output Power



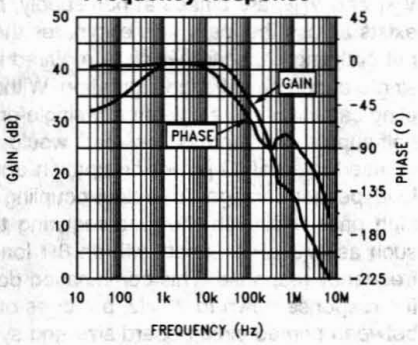
Output Power vs Load Resistance



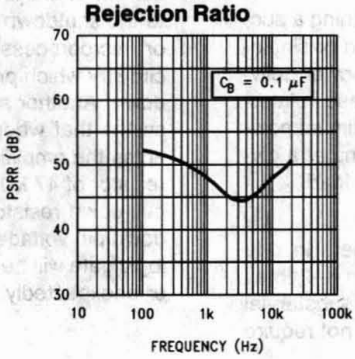
Output Power vs Supply Voltage



Open Loop Frequency Response



Power Supply Rejection Ratio



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Application Information

BRIDGE CONFIGURATION EXPLANATION

As shown in *Figure 1*, the LM4860 has two operational amplifiers internally, allowing for a few different amplifier configurations. The first amplifier's gain is externally configurable, while the second amplifier is internally fixed in a unity-gain, inverting configuration. The closed-loop gain of the first amplifier is set by selecting the ratio of R_f to R_i while the second amplifier's gain is fixed by the two internal 40 kΩ resistors. *Figure 1* shows that the output of amplifier one serves as the input to amplifier two which results in both amplifiers producing signals identical in magnitude, but out of phase 180°. Consequently, the differential gain for the IC is:

$$A_{vd} = 2 * (R_f/R_i)$$

By driving the load differentially through outputs V_{O1} and V_{O2}, an amplifier configuration commonly referred to as "bridged mode" is established. Bridged mode operation is different from the classical single-ended amplifier configuration where one side of its load is connected to ground.

A bridge amplifier design has a few distinct advantages over the single-ended configuration, as it provides differential drive to the load, thus doubling output swing for a specified supply voltage. Consequently, four times the output power is possible as compared to a single-ended amplifier under the same conditions. This increase in attainable output power assumes that the amplifier is not current limited or clipped. In order to choose an amplifier's closed-loop gain without causing excessive clipping which will damage high frequency transducers used in loudspeaker systems, please refer to the **Audio Power Amplifier Design** section.

A bridge configuration, such as the one used in Boomer Audio Power Amplifiers, also creates a second advantage over single-ended amplifiers. Since the differential outputs, V_{O1} and V_{O2}, are biased at half-supply, no net DC voltage exists across the load. This eliminates the need for an output coupling capacitor which is required in a single supply, single-ended amplifier configuration. Without an output coupling capacitor in a single supply single-ended amplifier, the half-supply bias across the load would result in both increased internal IC power dissipation and also permanent loudspeaker damage. An output coupling capacitor forms a high pass filter with the load requiring that a large value such as 470 μF be used with an 8Ω load to preserve low frequency response. This combination does not produce a flat response down to 20 Hz, but does offer a compromise between printed circuit board size and system cost, versus low frequency response.

POWER DISSIPATION

Power dissipation is a major concern when designing a successful amplifier, whether the amplifier is bridged or single-ended. A direct consequence of the increased power delivered to the load by a bridge amplifier is an increase in internal power dissipation. Equation 1 states the maximum power dissipation point for a bridge amplifier operating at a given supply voltage and driving a specified output load.

$$P_{DMAX} = 4 * (V_{DD})^2/(2\pi^2 R_L) \quad (1)$$

Since the LM4860 has two operational amplifiers in one package, the maximum internal power dissipation is 4 times that of a single-ended amplifier. Even with this substantial increase in power dissipation, the LM4860 does not require heatsinking. From Equation 1, assuming a 5V power supply and an 8Ω load, the maximum power dissipation point is 625 mW. The maximum power dissipation point obtained from Equation 1 must not be greater than the power dissipation that results from Equation 2:

$$P_{DMAX} = (T_{JMAX} - T_A)/\theta_{JA} \quad (2)$$

For the LM4860 surface mount package, θ_{JA} = 100°C/W and T_{JMAX} = 150°C. Depending on the ambient temperature, T_A, of the system surroundings, Equation 2 can be used to find the maximum internal power dissipation supported by the IC packaging. If the result of Equation 1 is greater than that of Equation 2, then either the supply voltage must be decreased or the load impedance increased. For the typical application of a 5V power supply, with an 8Ω load, the maximum ambient temperature possible without violating the maximum junction temperature is approximately 88°C, provided that device operation is around the maximum power dissipation point. Power dissipation is a function of output power and thus, if typical operation is not around the maximum power dissipation point, the ambient temperature can be increased. Refer to the **Typical Performance Characteristics** curves for power dissipation information for lower output powers.

POWER SUPPLY BYPASSING

As with any power amplifier, proper supply bypassing is critical for low noise performance and high power supply rejection. The capacitor location on both the bypass and power supply pins should be as close to the device as possible. As displayed in the **Typical Performance Characteristics** section, the effect of a larger half-supply bypass capacitor is improved low frequency THD + N due to increased half-supply stability. Typical applications employ a 5V regulator with 10 μF and a 0.1 μF bypass capacitors which aid in supply stability, but do not eliminate the need for bypassing the supply nodes of the LM4860. The selection of bypass capacitors, especially C_B, is thus dependant upon desired low frequency THD + N, system cost, and size constraints.

SHUTDOWN FUNCTION

In order to reduce power consumption while not in use, the LM4860 contains a shutdown pin to externally turn off the amplifier's bias circuitry. The shutdown feature turns the amplifier off when a logic high is placed on the shutdown pin. Upon going into shutdown, the output is immediately disconnected from the speaker. There is a built-in threshold which produces a drop in quiescent current to 500 μA typically. For a 5V power supply, this threshold occurs when 2V–3V is applied to the shutdown pin. A typical quiescent current of 0.6 μA results when the supply voltage is applied to the shutdown pin. In many applications, a microcontroller or microprocessor output is used to control the shutdown circuitry which provides a quick, smooth transition into shutdown. Another solution is to use a single-pole, single-throw switch that when closed, is connected to ground and enables the amplifier. If the switch is open, then a soft pull-up resistor of 47 kΩ will disable the LM4860. There are no soft pull-down resistors inside the LM4860, so a definite shutdown pin voltage must be appliied externally, or the internal logic gate will be left floating which could disable the amplifier unexpectedly.

Application Information (Continued)

HEADPHONE CONTROL INPUTS

The LM4860 possesses two headphone control inputs that disable the amplifier and reduce I_{DD} to less than 1 mA when either one or both of these inputs have a logic-high voltage placed on their pins.

Unlike the shutdown function, the headphone control function does not provide the level of current conservation that is required for battery powered systems. Since the quiescent current resulting from the headphone control function is 1000 times more than the shutdown function, the residual currents in the device may create a pop at the output when coming out of the headphone control mode. The pop effect may be eliminated by connecting the headphone sensing output to the shutdown pin input as shown in *Figure 4.* This solution will not only eliminate the output pop, but will also utilize the full current conservation of the shutdown function by reducing I_{DD} to 0.6 μA. The amplifier will then be fully shutdown. This configuration also allows the designer to use the control inputs as either two headphone control pins or a headphone control pin and a shutdown pin where the lowest level of current consumption is obtained from either function.

Figure 5 shows the implementation of the LM4860's headphone control function using a single-supply headphone amplifier. The voltage divider of R1 and R2 sets the voltage at the HP-IN1 pin to be approximately 50 mV when there are no headphones plugged into the system. This logic-low voltage at the HP-IN1 pin enables the LM4860 to amplify AC signals. Resistor R3 limits the amount of current flowing out of the HP-IN1 pin when the voltage at that pin goes below ground resulting from the music coming from the headphone amplifier. The output coupling cap protects the headphones by blocking the amplifier's half-supply DC voltage. The capacitor also protects the headphone amplifier from the low voltage set up by resistors R1 and R2 when there aren't any headphones plugged into the system. The tricky point to this setup is that the AC output voltage of the headphone amplifier cannot exceed the 2.0V HP-IN1 voltage threshold when there aren't any headphones plugged into the system, assuming that R1 and R2 are 100k and 1k, respectively. The LM4860 may not be fully shutdown when this level is exceeded momentarily, due to the discharging time constant of the bias-pin voltage. This time constant is established by the two 50k resistors (in parallel) with the series bypass capacitor value.

When a set of headphones are plugged into the system, the contact pin of the headphone jack is disconnected from the signal pin, interrupting the voltage divider set up by resistors R1 and R2. Resistor R1 then pulls up the HP-IN1 pin, enabling the headphone function and disabling the LM4860 amplifier. The headphone amplifier then drives the headphones, whose impedance is in parallel with resistor R2. Since the typical impedance of headphones are 32Ω, resistor R2 has negligible effect on the output drive capability. Also shown in *Figure 5* are the electrical connections for the headphone jack and plug. A 3-wire plug consists of a Tip, Ring, and Sleave, where the Tip and Ring are signal carrying conductors and the Sleave is the common ground return. One control pin contact for each headphone jack is sufficient to indicate to control inputs that the user has inserted a plug into a jack and that another mode of operation is desired.

For a system implementation where the headphone amplifier is designed using a split supply, the output coupling cap, C_C and resistor R2 of *Figure 5,* can be eliminated. The functionality described earlier remains the same, however.

In addition, the HP-SENSE pin, although it may be connected to the SHUTDOWN pin as shown in *Figure 4,* may still be used as a control flag. It is capable of driving the input to another logic gate or approximately 2 mA without serious loading.

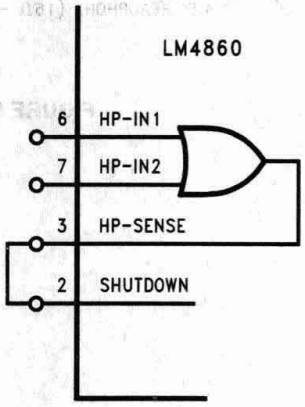

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FIGURE 4. HP-SENSE Pin to SHUTDOWN Pin Connection

Application Information (Continued)

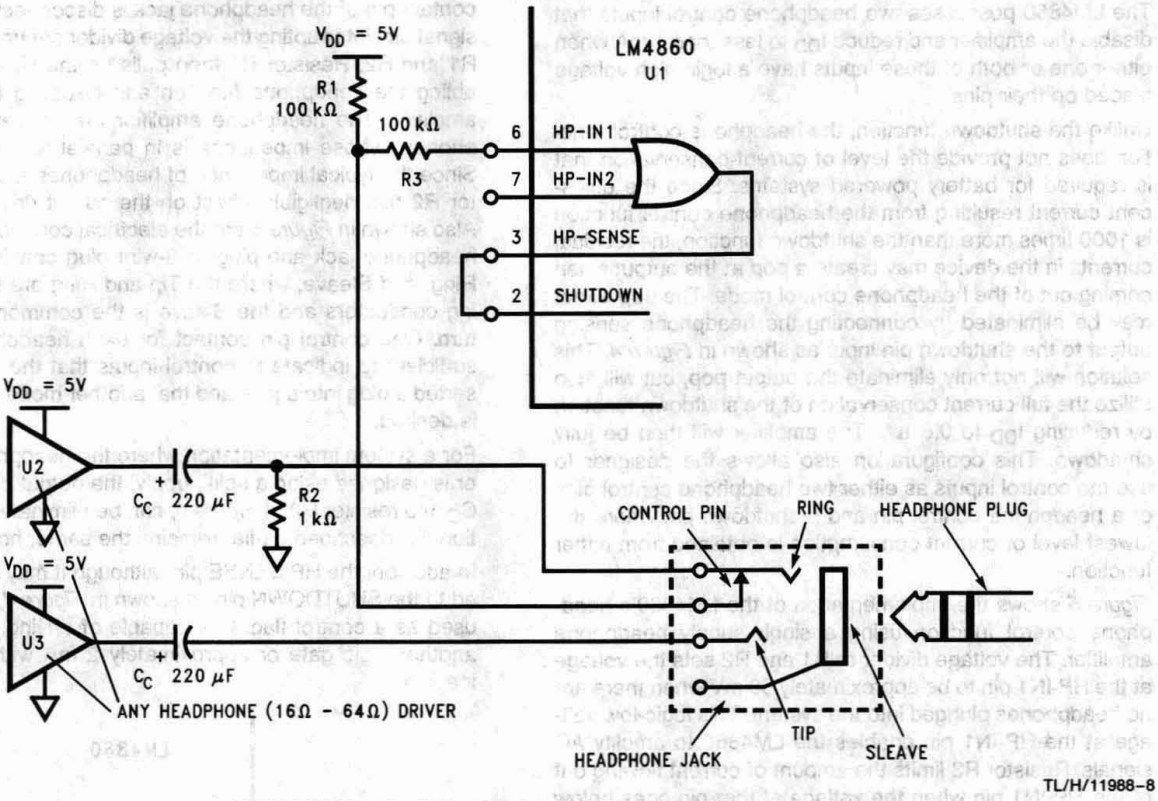

FIGURE 5. Typical Headphone Control Input Circuitry

Application Information (Continued)

HIGHER GAIN AUDIO AMPLIFIER

The LM4860 is unity-gain stable and requires no external components besides gain-setting resistors, an input coupling capacitor, and proper supply bypassing in the typical application. However if a closed-loop differential gain of greater than 10 is required, then a feedback capacitor is needed, as shown in *Figure 2,* to bandwidth limit the amplifier. The feedback capacitor creates a low pass filter that eliminates unwanted high frequency oscillations. Care should be taken when calculating the −3 dB frequency in that an incorrect combination of R_f and C_f will cause rolloff before 20 kHz. A typical combination of feedback resistor and capacitor that will not produce audio band high frequency rolloff is R_f = 100 kΩ and C_f = 5 pF. These components result in a −3 dB point of approximately 320 kHz. Once the differential gain of the amplifier has been calculated, a choice of R_f will result, and C_f can then be calculated from the formula stated in the **External Components Description** section.

VOICE-BAND AUDIO AMPLIFIER

Many applications, such as telephony, only require a voice-band frequency response. Such an application usually requires a flat frequency response from 300 Hz to 3.5 kHz. By adjusting the component values of *Figure 2,* this common application requirement can be implemented. The combination of R_i and C_i form a highpass filter while R_f and C_f form a lowpass filter. Using the typical voice-band frequency range, with a passband differential gain of approximately 100, the following values of R_i, C_i, R_f, and C_f follow from the equations stated in the **External Components Description** section.

R_i = 10 kΩ, R_f = 510k, C_i = 0.22 µF, and C_f = 15 pF

Five times away from a −3 dB point is 0.17 dB down from the flatband response. With this selection of components, the resulting −3 dB points, f_L and f_H, are 72 Hz and 20 kHz, respectively, resulting in a flatband frequency response of better than ±0.25 dB with a rolloff of 6 dB/octave outside of the passband. If a steeper rolloff is required, other common bandpass filtering techniques can be used to achieve higher order filters.

SINGLE-ENDED AUDIO AMPLIFIER

Although the typical application for the LM4860 is a bridged monoaural amp, it can also be used to drive a load single-endedly in applications, such as PC cards, which require that one side of the load is tied to ground. *Figure 3* shows a common single-ended application, where V_{O1} is used to drive the speaker. This output is coupled through a 470 µF capacitor, which blocks the half-supply DC bias that exists in all single-supply amplifier configurations. This capacitor, designated C_O in *Figure 3,* in conjunction with R_L, forms a highpass filter. The −3 dB point of this highpass filter is $1/(2\pi R_L C_O)$, so care should be taken to make sure that the product of R_L and C_O is large enough to pass low frequencies to the load. When driving an 8Ω load, and if a full audio spectrum reproduction is required, C_O should be at least 470 µF. V_{O2}, the output that is not used, is connected through a 0.1 µF capacitor to a 2 kΩ load to prevent instability. While such an instability will not affect the waveform of V_{O1}, it is good design practice to load the second output.

AUDIO POWER AMPLIFIER DESIGN

Design a 500 mW/8Ω Audio Amplifier

Given:

Power Output	500 mWrms
Load Impedance	8Ω
Input Level	1 Vrms(max)
Input Impedance	20 kΩ
Bandwidth	20 Hz-20 kHz ±0.25 dB

A designer must first determine the needed supply rail to obtain the specified output power. Calculating the required supply rail involves knowing two parameters, V_{opeak} and also the dropout voltage. The latter is typically 0.7V. V_{opeak} can be determined from equation 3.

$$V_{opeak} = \sqrt{(2\, R_L\, P_O)} \qquad (3)$$

For 500 mW of output power into an 8Ω load, the required V_{opeak} is 2.83V. A minimum supply rail of 3.53V results from adding V_{opeak} and V_{od}. But 3.53V is not a standard voltage that exists in many applications and for this reason, a supply rail of 5V is designated. Extra supply voltage creates dynamic headroom that allows the LM4860 to reproduce peaks in excess of 500 mW without clipping the signal. At this time, the designer must make sure that the power supply choice along with the output impedance does not violate the conditions explained in the **Power Dissipation** section.

Once the power dissipation equations have been addressed, the required differential gain can be determined from Equation 4.

$$A_{vd} \geq 2 * \sqrt{(P_O\, R_L)}\,/(V_{IN}) = V_{orms}/V_{inrms} \qquad (4)$$

$$R_f/R_j = A_{vd}/2 \qquad (5)$$

From equation 4, the minimum A_{vd} is: A_{vd} = 2

Since the desired input impedance was 20 kΩ, and with an A_{vd} of 2, a ratio of 1:1 of R_f to R_i results in an allocation of R_i = R_f = 20 kΩ. Since the A_{vd} was less than 10, a feedback capacitor is not needed. The final design step is to address the bandwidth requirements which must be stated as a pair of −3 dB frequency points. Five times away from a −3 dB point is 0.17 dB down from passband response which is better than the required ±0.25 dB specified. This fact results in a low and high frequency pole of 4 Hz and 100 kHz respectively. As stated in the **External Components** section, R_i in conjunction with C_i create a highpass filter.

$$C_i \geq 1/(2\pi * 20\ k\Omega * 4\ Hz) = 1.98\ \mu F;\quad \text{use } 2.2\ \mu F.$$

The high frequency pole is determined by the product of the desired high frequency pole, f_H, and the differential gain, A_{vd}. With a A_{vd} = 2 and f_H = 100 kHz, the resulting GBWP = 100 kHz which is much smaller than the LM4860 GBWP of 7 MHz. This figure displays that if a designer has a need to design an amplifier with a higher differential gain, the LM4860 can still be used without running into bandwidth problems.

National Semiconductor

LM4861 Boomer® Audio Power Amplifier Series
½W Audio Power Amplifier with Shutdown Mode

General Description

The LM4861 is a bridge-connected audio power amplifier capable of delivering 500 mW of continuous average power to an 8Ω load with less than 1% (THD+N) over the audio spectrum using a 5V power supply.

Boomer audio power amplifiers were designed specifically to provide high quality output power with a minimal amount of external components using surface mount packaging. Since the LM4861 does not require output coupling capacitors, bootstrap capacitors, or snubber networks, it is optimally suited for low-power portable systems.

The LM4861 features an externally controlled, low-power consumption shutdown mode, as well as an internal thermal shutdown protection mechanism.

The unity-gain stable LM4861 can be configured by external gain-setting resistors for differential gains of 1 to 10 without the use of external compensation components.

Key Specifications

- THD+N at 500 mW continuous average output power into 8Ω — 1% (max)
- Instantaneous peak output power — >1W
- Shutdown current — 0.6 μA (typ)

Features

- No output coupling capacitors, bootstrap capacitors, or snubber circuits are necessary
- Small Outline (SO) packaging
- Compatible with PC power supplies
- Thermal shutdown protection circuitry
- Unity-gain stable
- External Gain Configuration Capability

Applications

- Personal computers
- Portable consumer products
- Cellular phones
- Self-powered speakers
- Toys and games

Typical Application

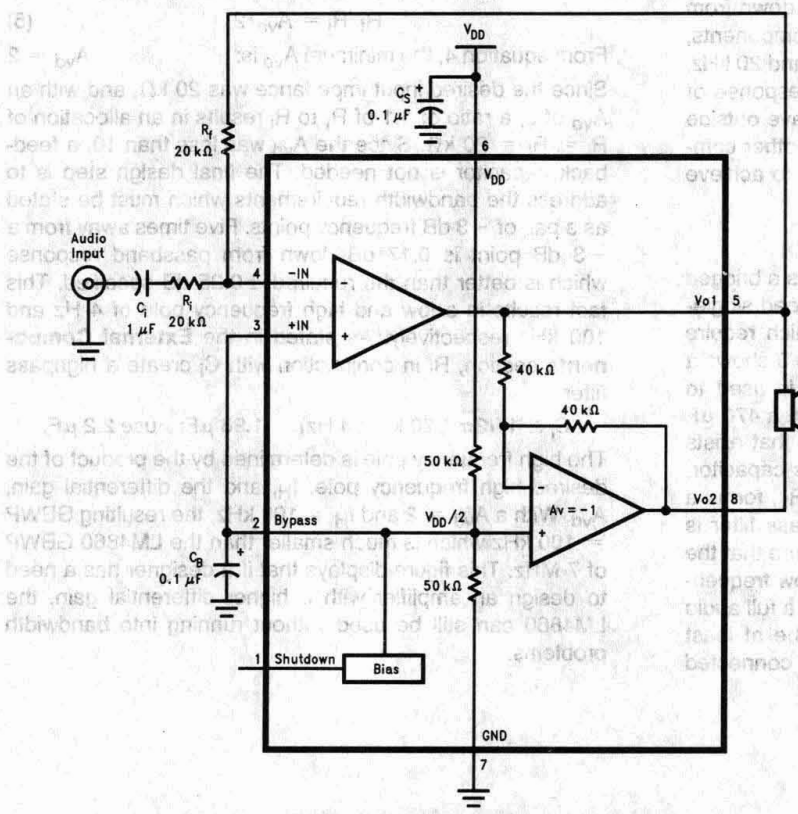

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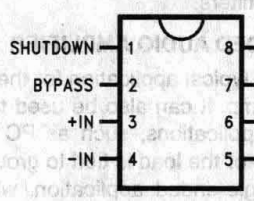
FIGURE 1. Typical Audio Amplifier Application Circuit

Connection Diagram

Small Outline Package



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Top View

Order Number LM4861M
See NS Package Number M08A

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	6.0V
Storage Temperature	−65°C to +150°C
Input Voltage	−0.3V to V_{DD} + 0.3V
Power Dissipation (Note 3)	Internally limited
ESD Susceptibility (Note 4)	3000V
ESD Susceptibility (Note 5)	250V
Junction Temperature	150°C

Soldering Information

Small Outline Package	
Vapor Phase (60 sec.)	215°C
Infrared (15 sec.)	220°C

See AN-450 *"Surface Mounting and their Effects on Product Reliability"* for other methods of soldering surface mount devices.

Operating Ratings

Temperature Range	
$T_{MIN} \le T_A \le T_{MAX}$	$-20°C \le T_A \le +85°C$
Supply Voltage	$2.7V \le V_{DD} \le 5.5V$

Electrical Characteristics (Notes 1, 2)

The following specifications apply for V_{DD} = 5V, R_L = 8Ω unless otherwise specified. Limits apply for T_A = 25°C.

Symbol	Parameter	Conditions	LM4861		Units (Limits)
			Typical (Note 6)	Limit (Note 7)	
V_{DD}	Supply Voltage			2.7 5.5	V (min) V (max)
I_{DD}	Quiescent Power Supply Current	V_{IN} = 0V, I_O = 0A (Note 8)	6.5	10.0	mA (max)
I_{SD}	Shutdown Current	$V_{pin1} = V_{DD}$ (Note 9)	0.6		μA
V_{OS}	Output Offset Voltage	V_{IN} = 0V	5.0	50.0	mV (max)
P_O	Output Power	THD+N = 1% (max); f = 1 kHz		0.50	W (min)
THD+N	Total Harmonic Distortion + Noise	P_O = 500 mWrms; 20 Hz ≤ f ≤ 20 kHz	0.45		%
PSRR	Power Supply Rejection Ratio	V_{DD} = 4.9V to 5.1V	65		dB

Note 1: All voltages are measured with respect to the ground pin, unless otherwise specified.

Note 2: *Absolute Maximum Ratings* indicate limits beyond which damage to the device may occur. *Operating Ratings* indicate conditions for which the device is functional, but do not guarantee specific performance limits. *Electrical Characteristics* state DC and AC electrical specifications under particular test conditions which guarantee specific performance limits. This assumes that the device is within the Operating Ratings. Specifications are not guaranteed for parameters where no limit is given, however, the typical value is a good indication of device performance.

Note 3: The maximum power dissipation must be derated at elevated temperatures and is dictated by T_{JMAX}, θ_{JA}, and the ambient temperature T_A. The maximum allowable power dissipation is $P_{DMAX} = (T_{JMAX} - T_A)/\theta_{JA}$ or the number given in the Absolute Maximum Ratings, whichever is lower. For the LM4861, T_{JMAX} = 150°C, and the typical junction-to-ambient thermal resistance, when board mounted, is 170°C/W.

Note 4: Human body model, 100 pF discharged through a 1.5 kΩ resistor.

Note 5: Machine Model, 220 pF–240 pF discharged through all pins.

Note 6: Typicals are measured at 25°C and represent the parametric norm.

Note 7: Limits are guaranteed to National's AOQL (Average Outgoing Quality Level).

Note 8: The quiescent power supply current depends on the offset voltage when a practical load is connected to the amplifier.

Note 9: Shutdown current has a wide distribution. For power management sensitive designs, contact your local National Semiconductor Sales Office.

High Gain Application Circuit

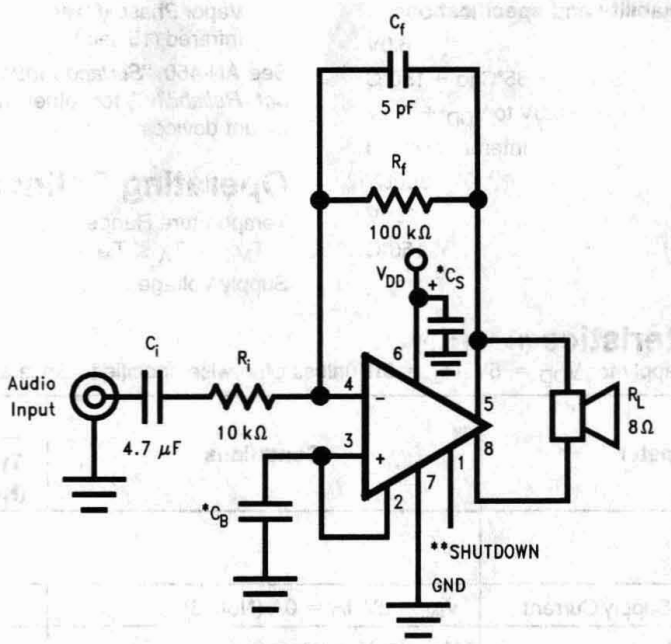


FIGURE 2. Audio Amplifier with $A_{VD} = 20$

Single Ended Application Circuit

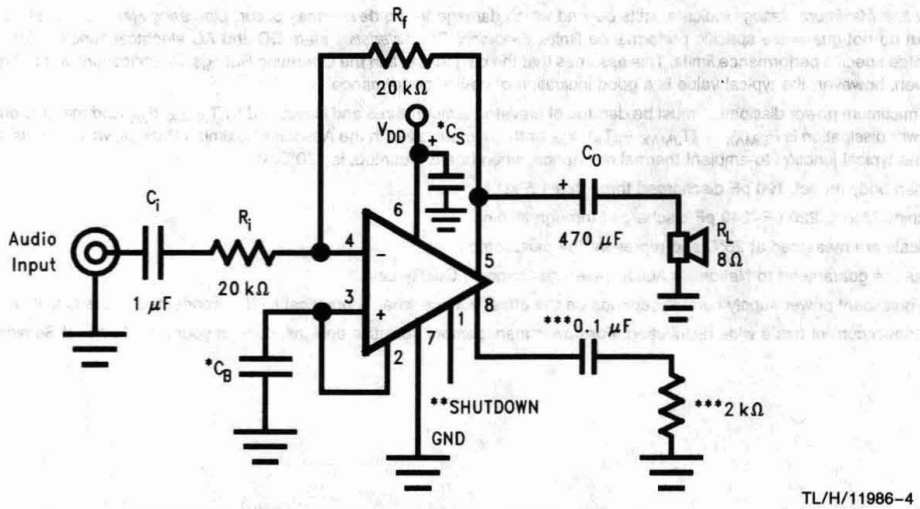


FIGURE 3. Single-Ended Amplifier with $A_V = -1$

*C_S and C_B size depend on specific application requirements and constraints. Typical vaiues of C_S and C_B are 0.1 μF.

**Pin 1 should be connected to V_{DD} to disable the amplifier or to GND to enable the amplifier. This pin should not be left floating.

***These components create a "dummy" load for pin 8 for stability purposes.

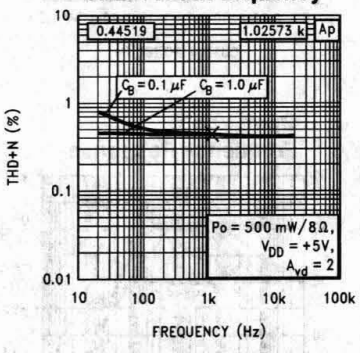
External Components Description *(Figures 1, 2)*

Components	Functional Description
1. R_i	Inverting input resistance which sets the closed-loop gain in conjunction with R_f. This resistor also forms a high pass filter with C_i at $f_C = 1/(2\pi R_i C_i)$.
2. C_i	Input coupling capacitor which blocks DC voltage at the amplifier's input terminals. Also creates a highpass filter with R_i at $f_C = 1/(2\pi R_i C_i)$.
3. R_f	Feedback resistance which sets closed-loop gain in conjunctien with R_i.
4. C_S	Supply bypass capacitor which provides power supply filtering. Refer to the **Application Information** section for proper placement and selection of supply bypass capacitor.
5. C_B	Bypass pin capacitor which provides half supply filtering. Refer to the **Application Information** section for proper placement and selection of bypass capacitor.
6. C_f*	Used when a differential gain of over 10 is desired. C_f in conjunction with R_f creates a low-pass filter which bandwidth limits the amplifier and prevents high frequency oscillation bursts. $f_C = 1/(2\pi R_f C_f)$

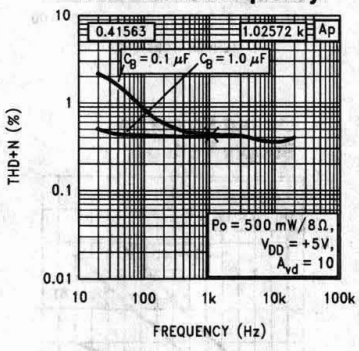
*Optional component dependent upon specific design requirements. Refer to the **Application Information** section for more information.

Typical Performance Characteristics

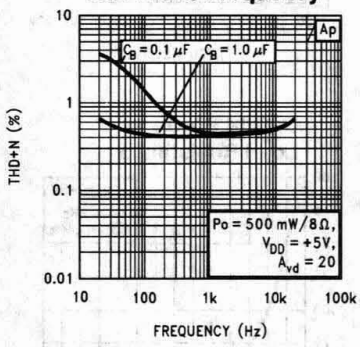
THD + N vs Frequency



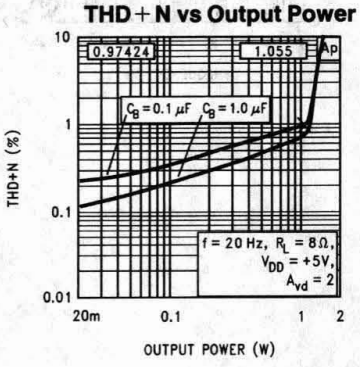
THD + N vs Frequency



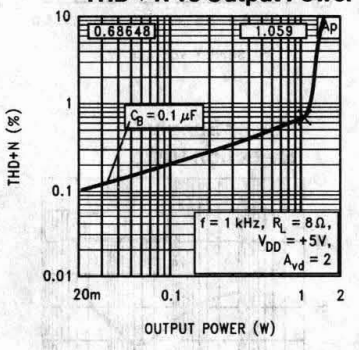
THD + N vs Frequency



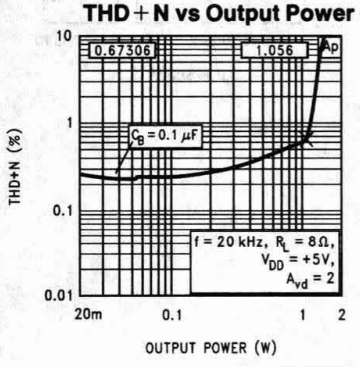
THD + N vs Output Power



THD + N vs Output Power



THD + N vs Output Power



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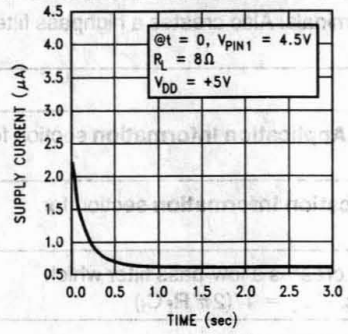
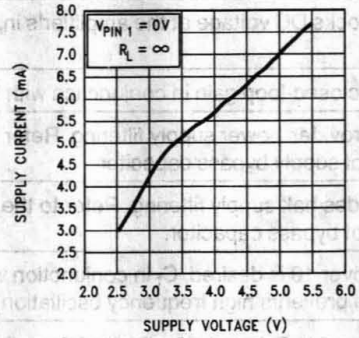
Typical Performance Characteristics (Continued)

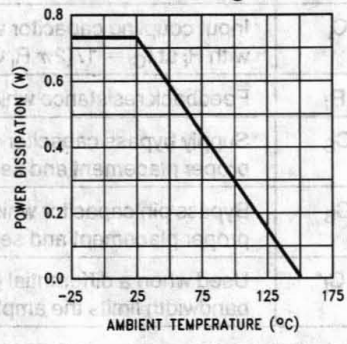
Supply Current vs Time in Shutdown Mode



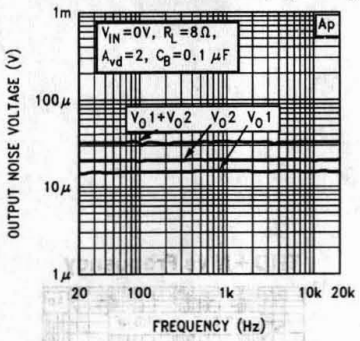
Supply Current vs Supply Voltage



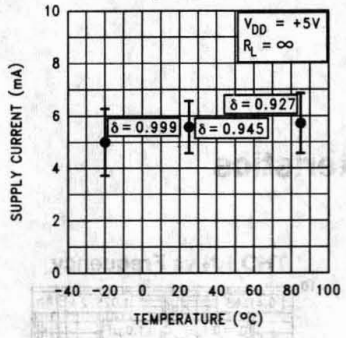
Power Derating Curve



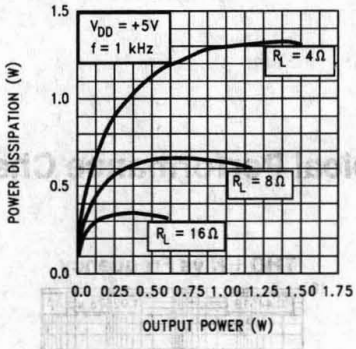
Noise Floor vs Frequency



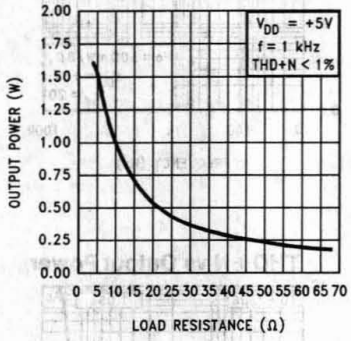
Supply Current Distribution vs Temperature



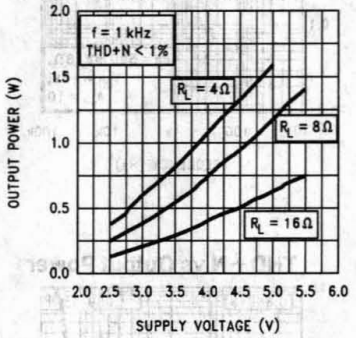
Power Dissipation vs Output Power



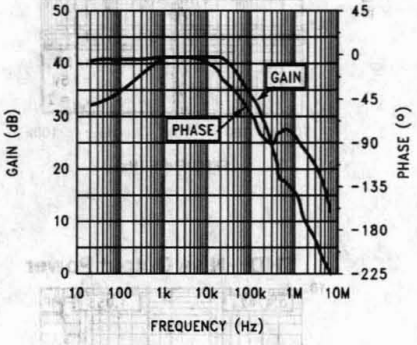
Output Power vs Load Resistance



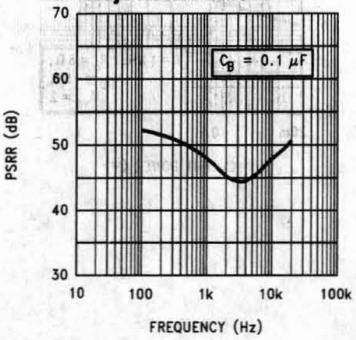
Output Power vs Supply Voltage



Open Loop Frequency Response



Power Supply Rejection Ratio



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Application Information

BRIDGE CONFIGURATION EXPLANATION

As shown in *Figure 1*, the LM4861 has two operational amplifiers internally, allowing for a few different amplifier configurations. The first amplifier's gain is externally configurable, while the second amplifier is internally fixed in a unity-gain, inverting configuration. The closed-loop gain of the first amplifier is set by selecting the ratio of R_f to R_i while the second amplifier's gain is fixed by the two internal 40 kΩ resistors. *Figure 1* shows that the output of amplifier one serves as the input to amplifier two which results in both amplifiers producing signals identical in magnitude, but out of phase 180°. Consequently, the differential gain for the IC is:

$$A_{vd} = 2 * (R_f/R_i)$$

By driving the load differentially through outputs V_{O1} and V_{O2}, an amplifier configuration commonly referred to as "bridged mode" is established. Bridged mode operation is different from the classical single-ended amplifier configuration where one side of its load is connected to ground.

A bridge amplifier design has a few distinct advantages over the single-ended configuration, as it provides differential drive to the load, thus doubling output swing for a specified supply voltage. Consequently, four times the output power is possible as compared to a single-ended amplifier under the same conditions. This increase in attainable output power assumes that the amplifier is not current limited or clipped. In order to choose an amplifier's closed-loop gain without causing excessive clipping which will damage high frequency transducers used in loudspeaker systems, please refer to the **Audio Power Amplifier Design** section.

A bridge configuration, such as the one used in Boomer Audio Power Amplifiers, also creates a second advantage over single-ended amplifiers. Since the differential outputs, V_{O1} and V_{O2}, are biased at half-supply, no net DC voltage exists across the load. This eliminates the need for an output coupling capacitor which is required in a single supply, single-ended amplifier configuration. Without an output coupling capacitor in a single supply, single-ended amplifier, the half-supply bias across the load would result in both increased internal IC power dissipation and also permanent loudspeaker damage. An output coupling capacitor forms a high pass filter with the load requiring that a large value such as 470 μF be used with an 8Ω load to preserve low frequency response. This combination does not produce a flat response down to 20 Hz, but does offer a compromise between printed circuit board size and system cost, versus low frequency response.

POWER DISSIPATION

Power dissipation is a major concern when designing a successful amplifier, whether the amplifier is bridged or single-ended. A direct consequence of the increased power delivered to the load by a bridge amplifier is an increase in internal power dissipation. Equation 1 states the maximum power dissipation point for a bridge amplifier operating at a given supply voltage and driving a specified output load.

$$P_{DMAX} = 4*(V_{DD})^2/(2\pi^2 R_L) \quad (1)$$

Since the LM4861 has two operational amplifiers in one package, the maximum internal power dissipation is 4 times that of a single-ended amplifier. Even with this substantial increase in power dissipation, the LM4861 does not require heatsinking. From Equation 1, assuming a 5V power supply and an 8Ω load, the maximum power dissipation point is 625 mW. The maximum power dissipation point obtained from Equation 1 must not be greater than the power dissipation that results from Equation 2:

$$P_{DMAX} = (T_{JMAX} - T_A)/\theta_{JA} \quad (2)$$

For the LM4861 surface mount package, θ_{JA} = 170°C/W and T_{JMAX} = 150°C. Depending on the ambient temperature, T_A, of the system surroundings, Equation 2 can be used to find the maximum internal power dissipation supported by the IC packaging. If the result of Equation 1 is greater than that of Equation 2, then either the supply voltage must be decreased or the load impedance increased. For the typical application of a 5V power supply, with an 8Ω load, the maximum ambient temperature possible without violating the maximum junction temperature is approximately 44°C provided that device operation is around the maximum power dissipation point. Power dissipation is a function of output power and thus, if typical operation is not around the maximum power dissipation point, the ambient temperature can be increased. Refer to the **Typical Performance Characteristics** curves for power dissipation information for lower output powers.

POWER SUPPLY BYPASSING

As with any power amplifier, proper supply bypassing is critical for low noise performance and high power supply rejection. The capacitor location on both the bypass and power supply pins should be as close to the device as possible. As displayed in the **Typical Performance Characteristics** section, the effect of a larger half supply bypass capacitor is improved low frequency THD + N due to increased half-supply stability. Typical applications employ a 5V regulator with 10 μF and a 0.1 μF bypass capacitors which aid in supply stability, but do not eliminate the need for bypassing the supply nodes of the LM4861. The selection of bypass capacitors, especially C_B, is thus dependant upon desired low frequency THD + N, system cost, and size constraints.

SHUTDOWN FUNCTION

In order to reduce power consumption while not in use, the LM4861 contains a shutdown pin to externally turn off the amplifier's bias circuitry. The shutdown feature turns the amplifier off when a logic high is placed on the shutdown pin. Upon going into shutdown, the output is immediately disconnected from the speaker. There is a built-in threshold which produces a drop in quiescent current to 500 μA typically. For a 5V power supply, this threshold occurs when 2V-3V is applied to the shutdown pin. A typical quiescent current of 0.6 μA results when the supply voltage is applied to the shutdown pin. In many applications, a microcontroller or microprocessor output is used to control the shutdown circuitry which provides a quick, smooth transition into shutdown. Another solution is to use a single-pole, single-throw switch that when closed, is connected to ground and enables the amplifier. If the switch is open, then a soft pull-up resistor of 47 kΩ will disable the LM4861. There are no soft pull-down resistors inside the LM4861, so a definite shutdown pin voltage must be applied externally, or the internal logic gate will be left floating which could disable the amplifier unexpectedly.

Application Information (Continued)

HIGHER GAIN AUDIO AMPLIFIER

The LM4861 is unity-gain stable and requires no external components besides gain-setting resistors, an input coupling capacitor, and proper supply bypassing in the typical application. However, if a closed-loop differential gain of greater than 10 is required, then a feedback capacitor is needed, as shown in *Figure 2*, to bandwidth limit the amplifier. This feedback capacitor creates a low pass filter that eliminates unwanted high frequency oscillations. Care should be taken when calculating the −3 dB frequency in that an incorrect combination of R_f and C_f will cause rolloff before 20 kHz. A typical combination of feedback resistor and capacitor that will not produce audio band high frequency rolloff is $R_f = 100\ k\Omega$ and $C_f = 5\ pF$. These components result in a −3 dB point of approximately 320 kHz. Once the differential gain of the amplifier has been calculated, a choice of R_f will result, and C_f can then be calculated from the formula stated in the **External Components Description** section.

VOICE-BAND AUDIO AMPLIFIER

Many applications, such as telephony, only require a voice-band frequency response. Such an application usually requires a flat frequency response from 300 Hz to 3.5 kHz. By adjusting the component values of *Figure 2*, this common application requirement can be implemented. The combination of R_i and C_i form a highpass filter while R_f and C_f form a lowpass filter. Using the typical voice-band frequency range, with a passband differential gain of approximately 100, the following values of R_i, C_i, R_f, and C_f follow from the equations stated in the **External Components Description** section.

$R_i = 10\ k\Omega$, $R_f = 510k$,$C_i = 0.22\ \mu F$, and $C_f = 15\ pF$

Five times away from a −3 dB point is 0.17 dB down from the flatband response. With this selection of components, the resulting −3 dB points, f_L and f_H, are 72 Hz and 20 kHz, respectively, resulting in a flatband frequency response of better than ±0.25 dB with a rolloff of 6 dB/octave outside of the passband. If a steeper rolloff is required, other common bandpass filtering techniques can be used to achieve higher order filters.

SINGLE-ENDED AUDIO AMPLIFIER

Although the typical application for the LM4861 is a bridged monoaural amp, it can also be used to drive a load single-endedly in applications, such as PC cards, which require that one side of the load is tied to ground. *Figure 3* shows a common single-ended application, where V_{O1} is used to drive the speaker. This output is coupled through a 470 µF capacitor, which blocks the half-supply DC bias that exists in all single-supply amplifier configurations. This capacitor, designated C_O in *Figure 3*, in conjunction with R_L, forms a highpass filter. The −3 dB point of this high pass filter is $1/(2\pi R_L C_O)$, so care should be taken to make sure that the product of R_L and C_O is large enough to pass low frequencies to the load. When driving an 8Ω load, and if a full audio spectrum reproduction is required, C_O should be at least 470 µF. V_{O2}, the output that is not used, is connected through a 0.1 µF capacitor to a 2 kΩ load to prevent instability. While such an instability will not affect the waveform of V_{O1}, it is good design practice to load the second output.

AUDIO POWER AMPLIFIER DESIGN

Design a 500 mW / 8Ω Audio Amplifier

Given:

Power Output	500 mWrms
Load Impedance	8Ω
Input Level	1 Vrms(max)
Input Impedance	20 kΩ
Bandwidth	20 Hz–20 kHz ±0.25 dB

A designer must first determine the needed supply rail to obtain the specified output power. Calculating the required supply rail involves knowing two parameters, V_{opeak} and also the dropout voltage. The latter is typically 0.7V. V_{opeak} can be determined from equation 3.

$$V_{opeak} = \sqrt{(2R_L P_O)} \quad (3)$$

For 500 mW of output power into an 8Ω load, the required V_{opeak} is 2.83V. A minumum supply rail of 3.53V results from adding V_{opeak} and V_{od}. But 3.53V is not a standard voltage that exists in many applications and for this reason, a supply rail of 5V is designated. Extra supply voltage creates dynamic headroom that allows the LM4861 to reproduce peaks in excess of 500 mW without clipping the signal. At this time, the designer must make sure that the power supply choice along with the output impedance does not violate the conditions explained in the **Power Dissipation** section.

Once the power dissipation equations have been addressed, the required differential gain can be determined from Equation 4.

$$A_{vd} \geq 2^* \sqrt{(P_O R_L)}/(V_{IN}) = V_{orms}/V_{inrms} \quad (4)$$

$$R_f/R_i = A_{vd}/2 \quad (5)$$

From equation 4, the minimum A_{vd} is: $A_{vd} = 2$

Since the desired input impedance was 20 kΩ, and with a A_{vd} of 2, a ratio of 1:1 of R_f to R_i results in an allocation of $R_i = R_f = 20\ k\Omega$. Since the A_{vd} was less than 10, a feedback capacitor is not needed. The final design step is to address the bandwidth requirements which must be stated as a pair of −3 dB frequency points. Five times away from a −3 db point is 0.17 dB down from passband response which is better than the required ±0.25 dB specified. This fact results in a low and high frequency pole of 4 Hz and 100 kHz respectively. As stated in the **External Components** section, R_i in conjunction with C_i create a highpass filter.

$C_i \geq 1 / (2\pi^*20\ k\Omega^*4\ Hz) = 1.98\ \mu F$; use 2.2 µF.

The high frequency pole is determined by the product of the desired high frequency pole, f_H, and the differential gain, A_{vd}. With a $A_{vd} = 2$ and $f_H = 100$ kHz, the resulting GBWP = 100 kHz which is much smaller than the LM4861 GBWP of 7 MHz. This figure displays that if a designer has a need to design an amplifier with a higher differential gain, the LM4861 can still be used without running into bandwidth problems.

National Semiconductor

PRELIMINARY

LM4862 Boomer® Audio Power Amplifier Series
350 mW Audio Power Amplifier with Shutdown Mode

General Description

The LM4862 is a bridge-connected audio power amplifier capable of delivering 350 mW of continuous average power to an 8Ω load with less than 1% (THD + N) over the audio spectrum using a 5V power supply.

Boomer audio power amplifiers were designed specifically to provide high quality output power with a minimal amount of external components. Since the LM4862 does not require output coupling capacitors, bootstrap capacitors, or snubber networks, it is optimally suited for low-power portable systems.

The LM4862 features an externally controlled, low-power consumption shutdown mode, as well as an internal thermal shutdown protection mechanism.

The unity-gain stable LM4862 can be configured by external gain-setting resistors.

Key Specifications

- THD + N at 350 mW continuous average output power into 8Ω — 1% (max)
- Instantaneous peak output power — >0.5W
- Shutdown Current — 0.7 μA (typ)

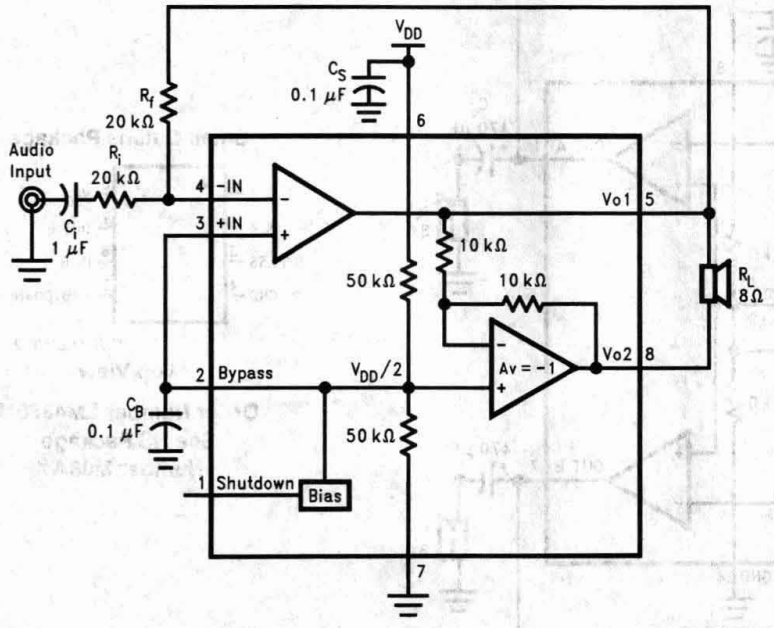
Features

- No output coupling capacitors, bootstrap capacitors or snubber circuits are necessary
- Small Outline or DIP packaging
- Unity-gain stable
- External gain configuration capability
- Pin compatible with LM4861

Applications

- Portable Computers
- Cellular Phones
- Toys and Games

Typical Application

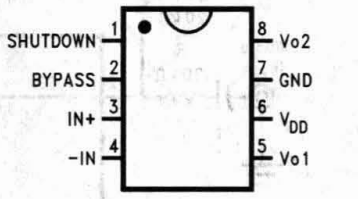


TL/H/12342–1

FIGURE 1. Typical Audio Amplifier Application Circuit

Connection Diagram

Small Outline and DIP Package



TL/H/12342–2

Top View

Order Number LM4862M, LM4862N
See NS Package Number M08A or N08E

1

National Semiconductor

PRELIMINARY

LM4880 Boomer® Audio Power Amplifier Series
Dual 200 mW Audio Power Amplifier with Shutdown Mode

General Description

The LM4880 is a dual audio power amplifier capable of delivering 200 mW of continuous average power to an 8Ω load with less than 0.1% (THD + N) using a 5V power supply.

Boomer audio power amplifiers were designed specifically to provide high quality output power with a minimal amount of external components using surface mount packaging. Since the LM4880 does not require bootstrap capacitors or snubber networks, it is optimally suited for low-power portable systems.

The LM4880 features an externally controlled, low-power consumption shutdown mode, as well as an internal thermal shutdown protection mechanism.

The unity-gain stable LM4880 can be configured by external gain-setting resistors.

Key Specifications

- THD + N at 200 mW continuous average output power into 8Ω — 0.1% (max)
- THD + N at 75 mW continuous average output power into 32Ω — 0.1% (max)
- Shutdown Current — 0.7 μA (typ)

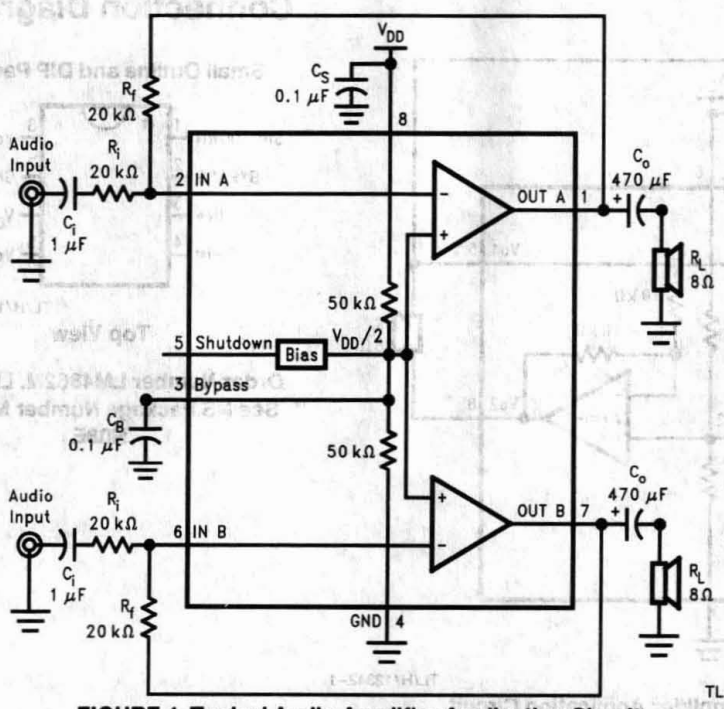
Features

- No bootstrap capacitors, or snubber circuits are necessary
- Small Outline (SO) packaging
- Unity-gain stable
- External gain configuration capability

Applications

- Headphone Amplifier
- Personal Computers
- CD-ROM Players

Typical Application

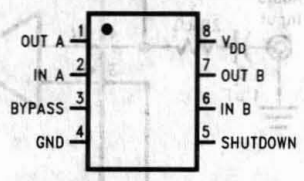


TL/H/12343-1

FIGURE 1. Typical Audio Amplifier Application Circuit

Connection Diagram

Small Outline Package



TL/H/12343-2

Top View

Order Number LM4880M
See NS Package Number M08A

National Semiconductor

Audio Control Selection Guide

Part Number	Description	# of Audio Channels	Supply Range	SNR (Typ)	THD (Typ)	Separation (Typ)	Package (Pin Count)	Communication Interface	Additional Comments
LM1036	Dual DC Operated Tone/Volume/ Balance Circuit	2	8V to 18V	80 dB	0.05%	75 dB	Dip(20)	DC Control	Few External Components Required
LM1971	1-Channel Digitally-Controlled Audio Attenuator	1	4.5V to 12V	64 dB	0.001%	NA	SO(8)	Serial MICROWIRE	"Clickless" Transitions
LM1972N	2-Channel Digitally-Controlled Audio Attenuator	2	4.5V to 12V	120 dB	0.0008%	110 dB	Dip(20), SO(20)	Serial MICROWIRE	Daisy Chain Capability, "Clickless" Transitions
LM1973N	3-Channel Digitally-Controlled Audio Attenuator	3	4.5V to 12V	120 dB	0.0008%	110 dB	Dip(20), SO(20)	Serial MICROWIRE	Daisy Chain Capability, "Clickless" Transitions
LMC1982	Digitally-Controlled Stereo Tone/ Volume/Balance Control	4	6V to 12V	95 dB	0.008%	80 dB	Dip(28), PLCC(28)	Serial Intermetal Bus (IM)	Two Selectable Stereo Inputs w/Stereo Enhance and Loudness Control
LMC1983	Digitally-Controlled Stereo Tone/ Volume/Balance Control	6	6V to 12V	95 dB	0.008%	80 dB	Dip(28), PLCC(28)	Serial Intermetal Bus (IM)	Three Selectable Stereo Inputs w/Loudness Control
LMC1992	Digitally-Controlled Stereo Tone/ Volume/Balance Control	8	6V to 12V	105 dB	0.03%	95 dB	Dip(28), PLCC(28)	Serial MICROWIRE	Four Selectable Stereo Inputs w/Fader Control
LMC835	Digitally-Controlled 7-Band Stereo Graphic Equalizer	2	5V to 16V	114 dB	0.0015%	NA	Dip(28), PLCC(28)	Serial	±6 dB or ±12 dB Gain Ranges w/25 Steps Each

National Semiconductor

LM1036 Dual DC Operated Tone/Volume/Balance Circuit

General Description

The LM1036 is a DC controlled tone (bass/treble), volume and balance circuit for stereo applications in car radio, TV and audio systems. An additional control input allows loudness compensation to be simply effected.

Four control inputs provide control of the bass, treble, balance and volume functions through application of DC voltages from a remote control system or, alternatively, from four potentiometers which may be biased from a zener regulated supply provided on the circuit.

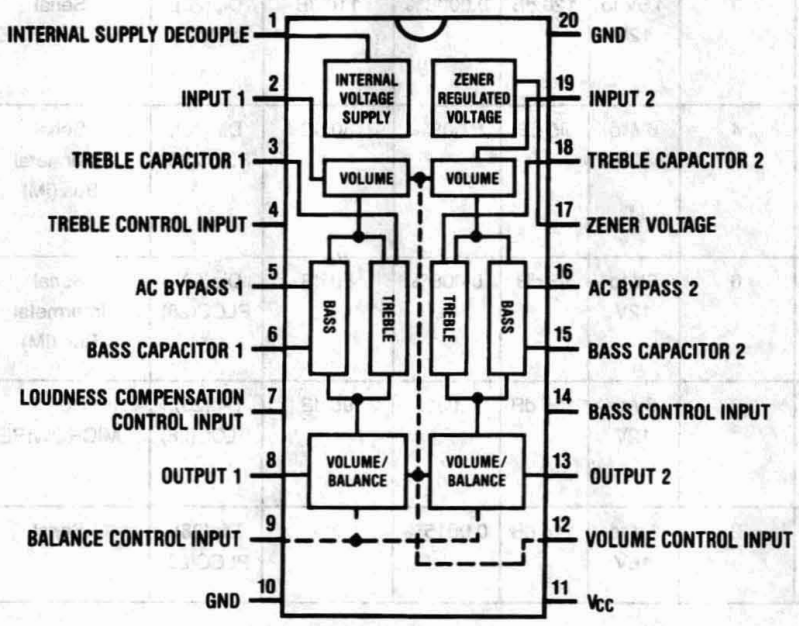
Each tone response is defined by a single capacitor chosen to give the desired characteristic.

Features

- Wide supply voltage range, 9V to 16V
- Large volume control range, 75 dB typical
- Tone control, ±15 dB typical
- Channel separation, 75 dB typical
- Low distortion, 0.06% typical for an input level of 0.3 Vrms
- High signal to noise, 80 dB typical for an input level of 0.3 Vrms
- Few external components required

Block and Connection Diagram

Dual-In-Line Package



TOP VIEW

TL/H/5142–1

Order Number LM1036N
See NS Package Number N20A

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	16V
Control Pin Voltage (Pins 4, 7, 9, 12, 14)	V_{CC}
Operating Temperature Range	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Power Dissipation	1W
Lead Temp. (Soldering, 10 seconds)	260°C

Electrical Characteristics $V_{CC}=12V$, $T_A=25°C$ (unless otherwise stated)

Parameter	Conditions	Min	Typ	Max	Units
Supply Voltage Range	Pin 11	9		16	V
Supply Current			35	45	mA
Zener Regulated Output	Pin 17				
Voltage			5.4		V
Current				5	mA
Maximum Output Voltage	Pins 8, 13; f = 1 kHz				
	$V_{CC}=9V$, Maximum Gain		0.8		Vrms
	$V_{CC}=12V$	0.8	1.0		Vrms
Maximum Input Voltage (Note 1)	Pins 2, 19; f = 1 kHz, $V_{CC}=9V$		1.1		Vrms
	Flat Response, $V_{CC}=12V$	1.3	1.6		Vrms
	Gain = −10 dB				
Input Resistance	Pins 2, 19; f = 1 kHz	20	30		kΩ
Output Resistance	Pins 8, 13; f = 1 kHz		20		Ω
Maximum Gain	V(Pin 12) = V(Pin 17); f = 1 kHz	−2	0	2	dB
Volume Control Range	f = 1 kHz	70	75		dB
Gain Tracking	f = 1 kHz				
Channel 1–Channel 2	0 dB through −40 dB		1	3	dB
	−40 dB through −60 dB		2		dB
Balance Control Range	Pins 8, 13; f = 1 kHz		1		dB
			−26	−20	dB
Bass Control Range (Note 2)	f = 40 Hz, $C_b=0.39\ \mu F$				
	V(Pin 14) = V(Pin 17)	12	15	18	dB
	V(Pin 14) = 0V	−12	−15	−18	dB
Treble Control Range (Note 2)	f = 16 kHz, $C_t=0.01\ \mu F$				
	V(Pin 4) = V(Pin 17)	12	15	18	dB
	V(Pin 4) = 0V	−12	−15	−18	dB
Total Harmonic Distortion	f = 1 kHz, $V_{IN}=0.3$ Vrms				
	Gain = 0 dB		0.06	0.3	%
	Gain = −30 dB		0.03		%
Channel Separation	f = 1 kHz, Maximum Gain	60	75		dB
Signal/Noise Ratio	Unweighted 100 Hz–20 kHz		80		dB
	Maximum Gain, 0 dB = 0.3 Vrms				
	CCIR/ARM (Note 3)				
	Gain = 0 dB, $V_{IN}=0.3$ Vrms	75	79		dB
	Gain = −20 dB, $V_{IN}=1.0$ Vrms		72		dB
Output Noise Voltage at Minimum Gain	CCIR/ARM (Note 3)		10	16	μV
Supply Ripple Rejection	200 mVrms, 1 kHz Ripple	35	50		dB
Control Input Currents	Pins 4, 7, 9, 12, 14 (V = 0V)		−0.6	−2.5	μA
Frequency Response	−1 dB (Flat Response 20 Hz–16 kHz)		250		kHz

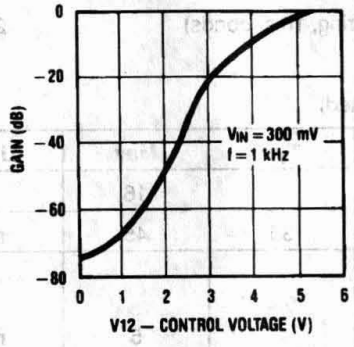
Note 1: The maximum permissible input level is dependent on tone and volume settings. See Application Notes.

Note 2: The tone control range is defined by capacitors C_b and C_t. See Application Notes.

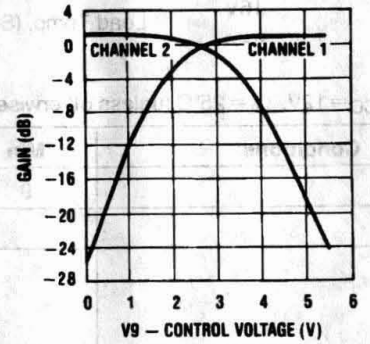
Note 3: Gaussian noise, measured over a period of 50 ms per channel, with a CCIR filter referenced to 2 kHz and an average-responding meter.

Typical Performance Characteristics

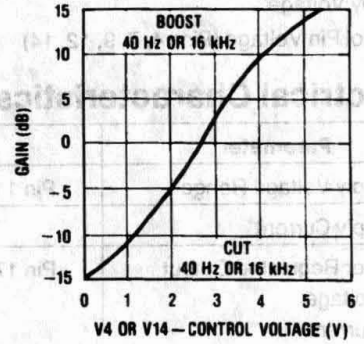
Volume Control Characteristics



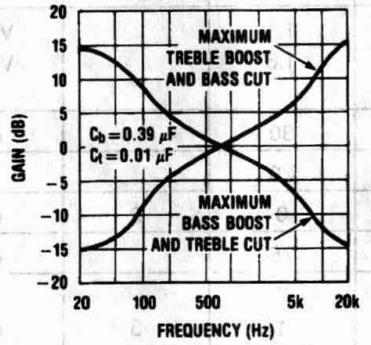
Balance Control Characteristic



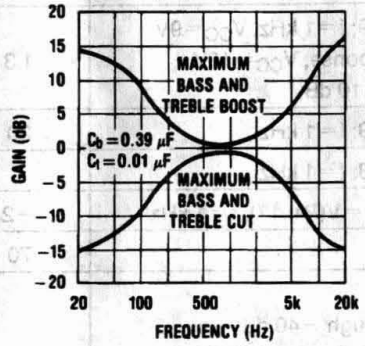
Tone Control Characteristic



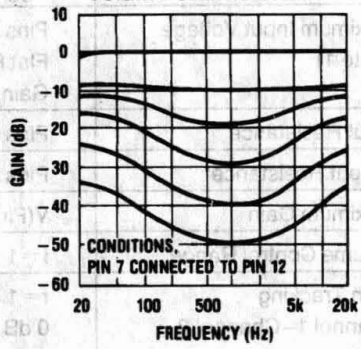
Tone Characteristic (Gain vs Frequency)



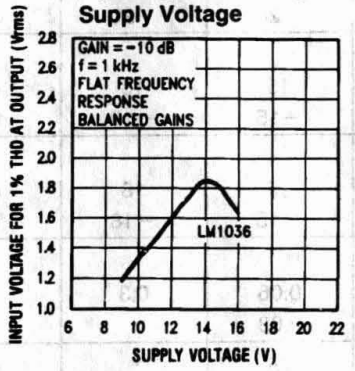
Tone Characteristic (Gain vs Frequency)



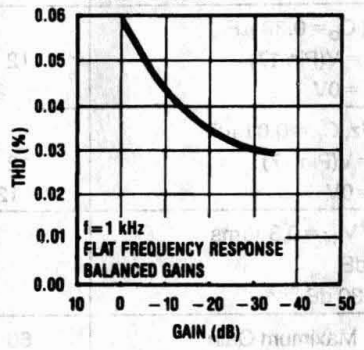
Loudness Compensated Volume Characteristic



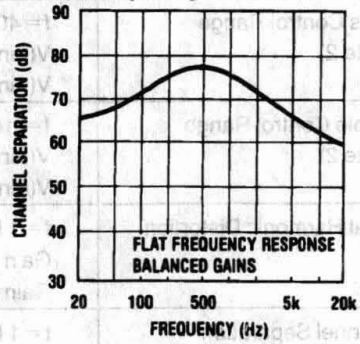
Input Signal Handling vs Supply Voltage



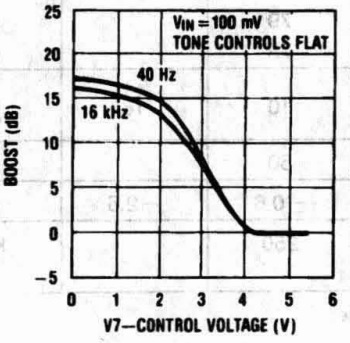
THD vs Gain



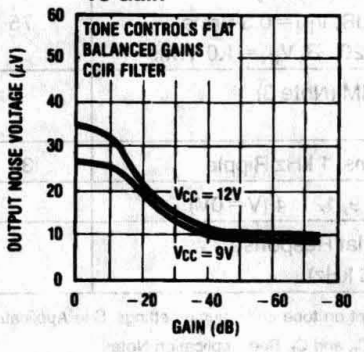
Channel Separation vs Frequency



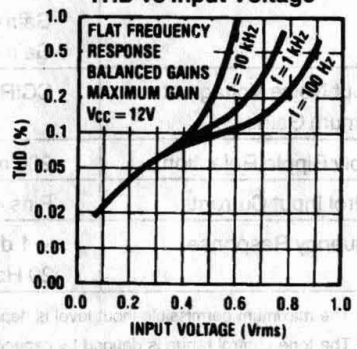
Loudness Control Characteristic



Output Noise Voltage vs Gain



THD vs Input Voltage



TL/H/5142–2

Application Notes

TONE RESPONSE

The maximum boost and cut can be optimized for individual applications by selection of the appropriate values of C_t (treble) and C_b (bass).

The tone responses are defined by the relationships:

$$\text{Bass Response} = \frac{1 + \dfrac{0.00065\,(1 - a_b)}{j\omega C_b}}{1 + \dfrac{0.00065 a_b}{j\omega C_b}}$$

$$\text{Treble Response} = \frac{1 + j\omega 5500(1 - a_t)C_t}{1 + j\omega 5500 a_t C_t}$$

Where $a_b = a_t = 0$ for maximum bass and treble boost respectively and $a_b = a_t = 1$ for maximum cut.

For the values of C_b and C_t of 0.39 μF and 0.01 μF as shown in the Application Circuit, 15 dB of boost or cut is obtained at 40 Hz and 16 kHz.

ZENER VOLTAGE

A zener voltage (pin 17 = 5.4V) is provided which may be used to bias the control potentiometers. Setting a DC level of one half of the zener voltage on the control inputs, pins 4, 9, and 14, results in the balanced gain and flat response condition. Typical spread on the zener voltage is ±100 mV and this must be taken into account if control signals are used which are not referenced to the zener voltage. If this is the case, then they will need to be derived with similar accuracy.

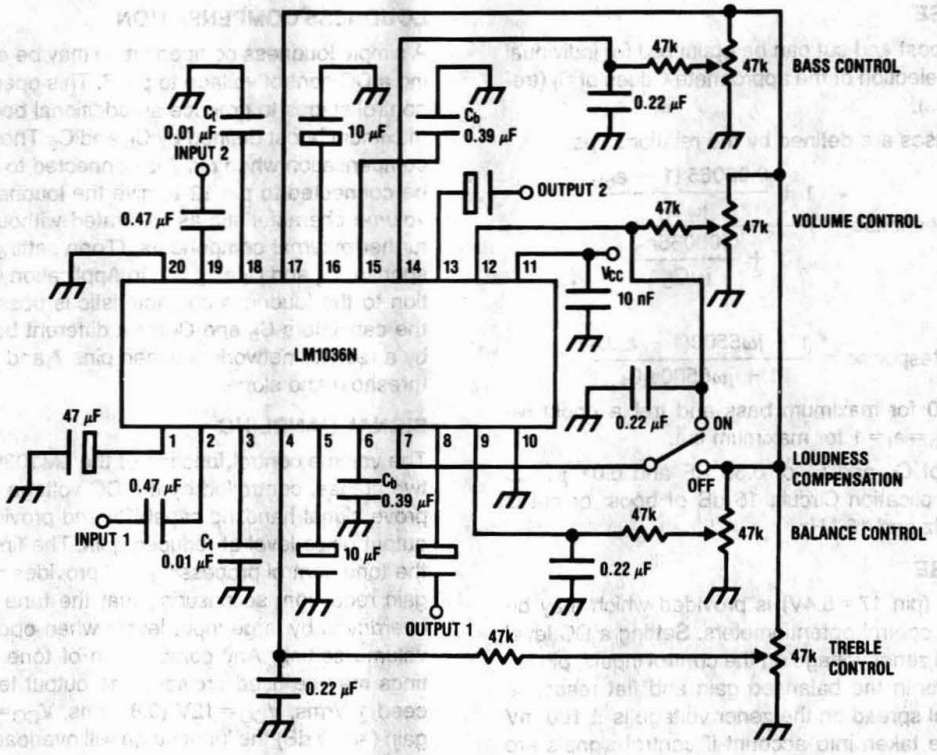
LOUDNESS COMPENSATION

A simple loudness compensation may be effected by applying a DC control voltage to pin 7. This operates on the tone control stages to produce an additional boost limited by the maximum boost defined by C_b and C_t. There is no loudness compensation when pin 7 is connected to pin 17. Pin 7 can be connected to pin 12 to give the loudness compensated volume characteristic as illustrated without the addition of further external components. (Tone settings are for flat response, C_b and C_t as given in Application Circuit.) Modification to the loudness characteristic is possible by changing the capacitors C_b and C_t for a different basic response or, by a resistor network between pins 7 and 12 for a different threshold and slope.

SIGNAL HANDLING

The volume control function of the LM1036 is carried out in two stages, controlled by the DC voltage on pin 12, to improve signal handling capability and provide a reduction of output noise level at reduced gain. The first stage is before the tone control processing and provides an initial 15 dB of gain reduction, so ensuring that the tone sections are not overdriven by large input levels when operating with a low volume setting. Any combination of tone and volume settings may be used provided the output level does not exceed 1 Vrms, $V_{CC} = 12V$ (0.8 Vrms, $V_{CC} = 9V$). At reduced gain (< -6 dB) the input stage will overload if the input level exceeds 1.6 Vrms, $V_{CC} = 12V$ (1.1 Vrms, $V_{CC} = 9V$). As there is volume control on the input stages, the inputs may be operated with a lower overload margin than would otherwise be acceptable, allowing a possible improvement in signal to noise ratio.

Application Circuit



TL/H/5142–3

Applications Information

OBTAINING MODIFIED RESPONSE CURVES

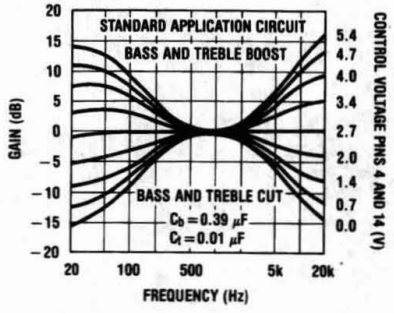
The LM1036 is a dual DC controlled bass, treble, balance and volume integrated circuit ideal for stereo audio systems.

In the various applications where the LM1036 can be used, there may be requirements for responses different to those of the standard application circuit given in the data sheet. This application section details some of the simple variations possible on the standard responses, to assist the choice of optimum characteristics for particular applications.

TONE CONTROLS

Summarizing the relationship given in the data sheet, basically for an increase in the treble control range C_t must be increased, and for increased bass range C_b must be reduced.

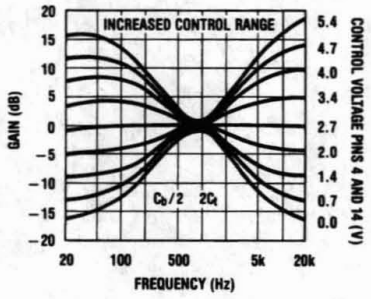
Figure 1 shows the typical tone response obtained in the standard application circuit. ($C_t = 0.01\ \mu F$, $C_b = 0.39\ \mu F$). Response curves are given for various amounts of boost and cut.


STANDARD APPLICATION CIRCUIT
BASS AND TREBLE BOOST
BASS AND TREBLE CUT
$C_b = 0.39\ \mu F$
$C_t = 0.01\ \mu F$
GAIN (dB)
20 15 10 5 0 −5 −10 −15 −20
20 100 500 5k 20k
FREQUENCY (Hz)
CONTROL VOLTAGE PINS 4 AND 14 (V)
5.4 4.7 4.0 3.4 2.7 2.0 1.4 0.7 0.0

TL/H/5142–4

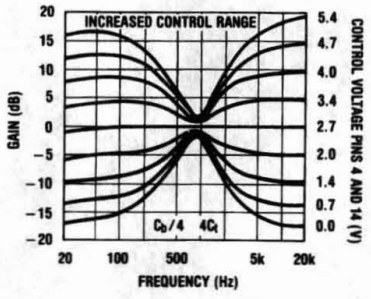
FIGURE 1. Tone Characteristic (Gain vs Frequency)

Figures 2 and *3* show the effect of changing the response defining capacitors C_t and C_b to 2Ct, $C_b/2$ and $4C_t$, $C_b/4$ respectively, giving increased tone control ranges. The values of the bypass capacitors may become significant and affect the lower frequencies in the bass response curves.


INCREASED CONTROL RANGE
$C_b/2$ 2C_t
GAIN (dB)
20 15 10 5 0 −5 −10 −15 −20
20 100 500 5k 20k
FREQUENCY (Hz)
CONTROL VOLTAGE PINS 4 AND 14 (V)
5.4 4.7 4.0 3.4 2.7 2.0 1.4 0.7 0.0

TL/H/5142–5

FIGURE 2. Tone Characteristic (Gain vs Frequency)


INCREASED CONTROL RANGE
$C_b/4$ 4C_t
GAIN (dB)
20 15 10 5 0 −5 −10 −15 −20
20 100 500 5k 20k
FREQUENCY (Hz)
CONTROL VOLTAGE PINS 4 AND 14 (V)
5.4 4.7 4.0 3.4 2.7 2.0 1.4 0.7 0.0

TL/H/5142–6

FIGURE 3. Tone Characteristic (Gain vs Frequency)

Applications Information (Continued)

Figure 4 shows the effect of changing C_t and C_b in the opposite direction to $C_t/2$, $2C_b$ respectively giving reduced control ranges. The various results corresponding to the different C_t and C_b values may be mixed if it is required to give a particular emphasis to, for example, the bass control. The particular case with $C_b/2$, C_t is illustrated in *Figure 5*.

Restriction of Tone Control Action at High or Low Frequencies

It may be desired in some applications to level off the tone responses above or below certain frequencies for example to reduce high frequence noise.

This may be achieved for the treble response by including a resistor in series with C_t. The treble boost and cut will be 3 dB less than the standard circuit when $R = X_C$.

A similar effect may be obtained for the bass response by reducing the value of the AC bypass capacitors on pins 5 (channel 1) and 16 (channel 2). The internal resistance at these pins is 1.3 kΩ and the bass boost/cut will be approximately 3 dB less with X_C at this value. An example of such modified response curves is shown in *Figure 6*. The input coupling capacitors may also modify the low frequency response.

It will be seen from *Figures 2* and *3* that modifying C_t and C_b for greater control range also has the effect of flattening the tone control extremes and this may be utilized, with or without additional modification as outlined above, for the most suitable tone control range and response shape.

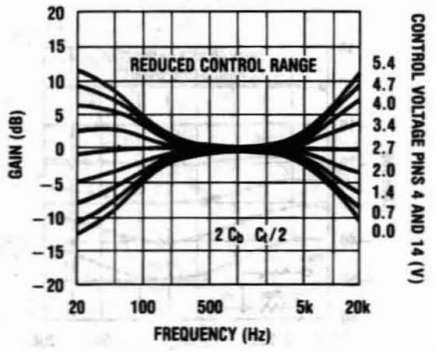
Other Advantages of DC Controls

The DC controls make the addition of other features easy to arrange. For example, the negative-going peaks of the output amplifiers may be detected below a certain level, and used to bias back the bass control from a high boost condition, to prevent overloading the speaker with low frequency components.

LOUDNESS CONTROL

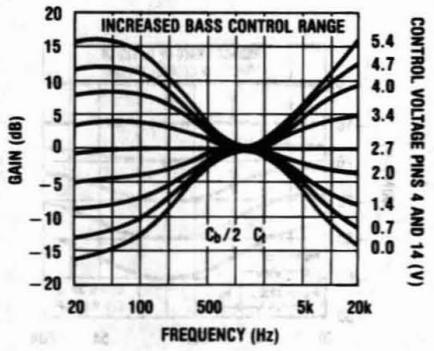
The loudness control is achieved through control of the tone sections by the voltage applied to pin 7; therefore, the tone and loudness functions are not independent. There is normally 1 dB more bass than treble boost (40 Hz–16 kHz) with loudness control in the standard circuit. If a greater difference is desired, it is necessary to introduce an offset by means of C_t or C_b or by changing the nominal control voltage ranges.

Figure 7 shows the typical loudness curves obtained in the standard application circuit at various volume levels ($C_b = 0.39\ \mu F$).



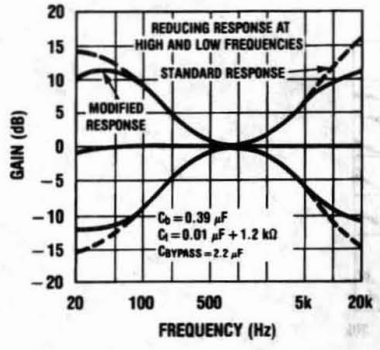
TL/H/5142–7

FIGURE 4. Tone Characteristic (Gain vs Frequency)



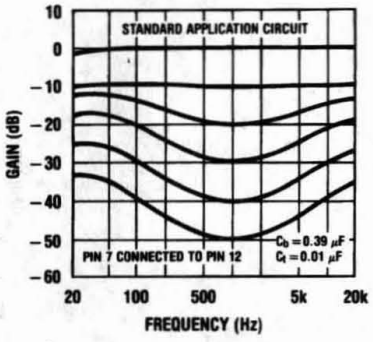
TL/H/5142–8

FIGURE 5. Tone Characteristic (Gain vs Frequency)



TL/H/5142–9

FIGURE 6. Tone Characteristic (Gain vs Frequency)



TL/H/5142–10

FIGURE 7. Loudness Compensated Volume Characteristic

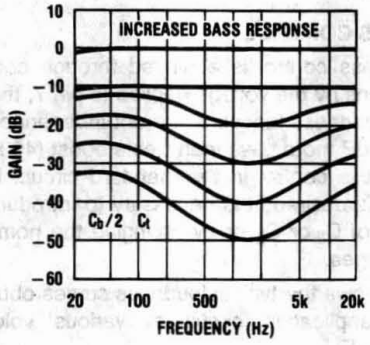
Applications Information (Continued)

Figures 8 and *9* illustrate the loudness characteristics obtained with C_b changed to $C_b/2$ and $C_b/4$ respectively, C_t being kept at the nominal 0.01 μF. These values naturally modify the bass tone response as in *Figures 2* and *3*.

With pins 7 (loudness) and 12 (volume) directly connected, loudness control starts at typically −8 dB volume, with most of the control action complete by −30 dB.

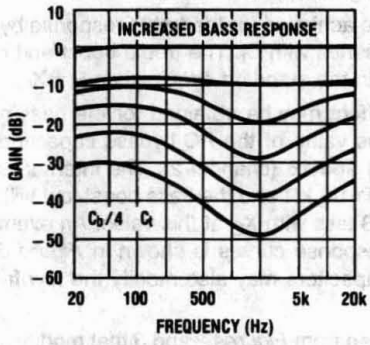
Figures 10 and *11* show the effect of resistively offsetting the voltage applied to pin 7 towards the control reference voltage (pin 17). Because the control inputs are high impedance, this is easily done and high value resistors may be used for minimal additional loading. It is possible to reduce the rate of onset of control to extend the active range to −50 dB volume control and below.

The control on pin 7 may also be divided down towards ground bringing the control action on earlier. This is illustrated in *Figure 12*. With a suitable level shifting network between pins 12 and 7, the onset of loudness control and its rate of change may be readily modified.



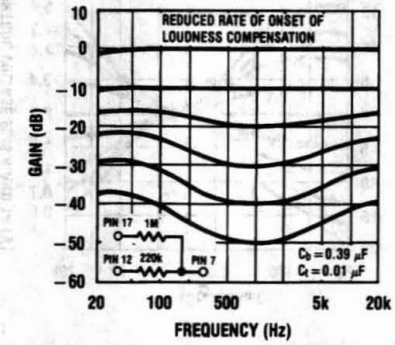
TL/H/5142–11

FIGURE 8. Loudness Compensated Volume Characteristic



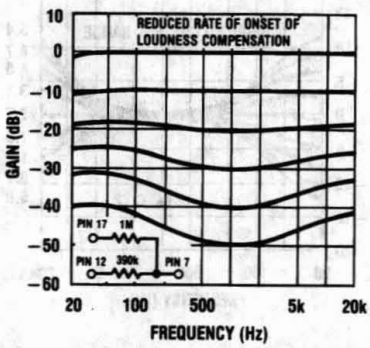
TL/H/5142–12

FIGURE 9. Loudness Compensated Volume Characteristic



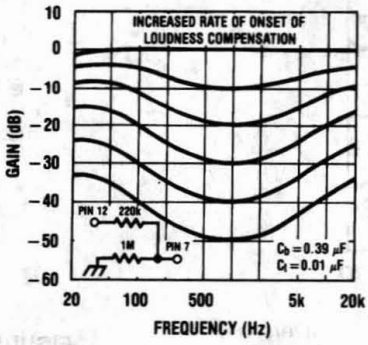
TL/H/5142–13

FIGURE 10. Loudness Compensated Volume Characteristic



TL/H/5142–14

FIGURE 11. Loudness Compensated Volume Characteristic



TL/H/5142–15

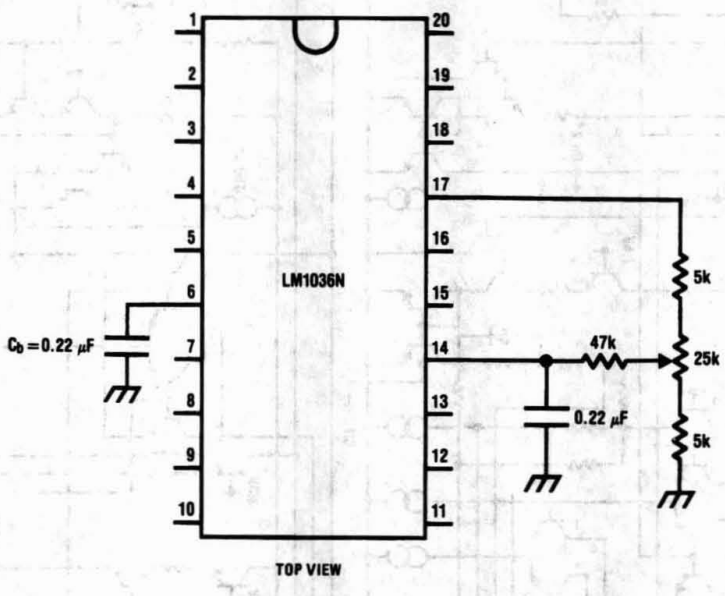
FIGURE 12. Loudness Compensated Volume Characteristic

Applications Information (Continued)

When adjusted for maximum boost in the usual application circuit, the LM1036 cannot give additional boost from the loudness control with reducing gain. If it is required, some additional boost can be obtained by restricting the tone control range and modifying C_t, C_b, to compensate. A circuit illustrating this for the case of bass boost is shown in *Figure 13*. The resulting responses are given in *Figure 14* showing the continuing loudness control action possible with bass boost previously applied.

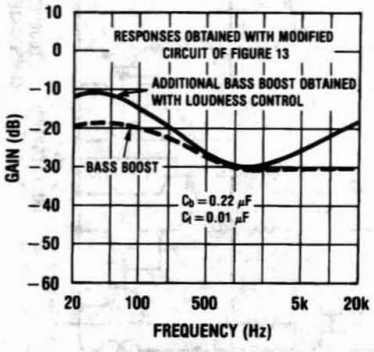
USE OF THE LM1036 ABOVE AUDIO FREQUENCIES

The LM1036 has a basic response typically 1 dB down at 250 kHz (tone controls flat) and therefore by scaling C_b and C_t, it is possible to arrange for operation over a wide frequency range for possible use in wide band equalization applications. As an example *Figure 15* shows the responses obtained centered on 10 kHz with $C_b = 0.039\ \mu F$ and $C_t = 0.001\ \mu F$.



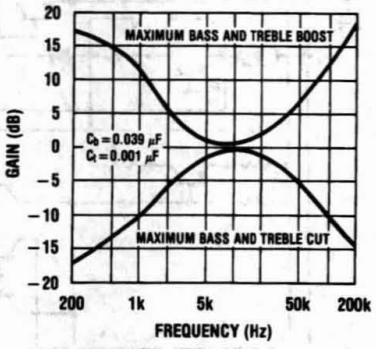
TL/H/5142–16

FIGURE 13. Modified Application Circuit for Additional Bass Boost with Loudness Control



TL/H/5142–17

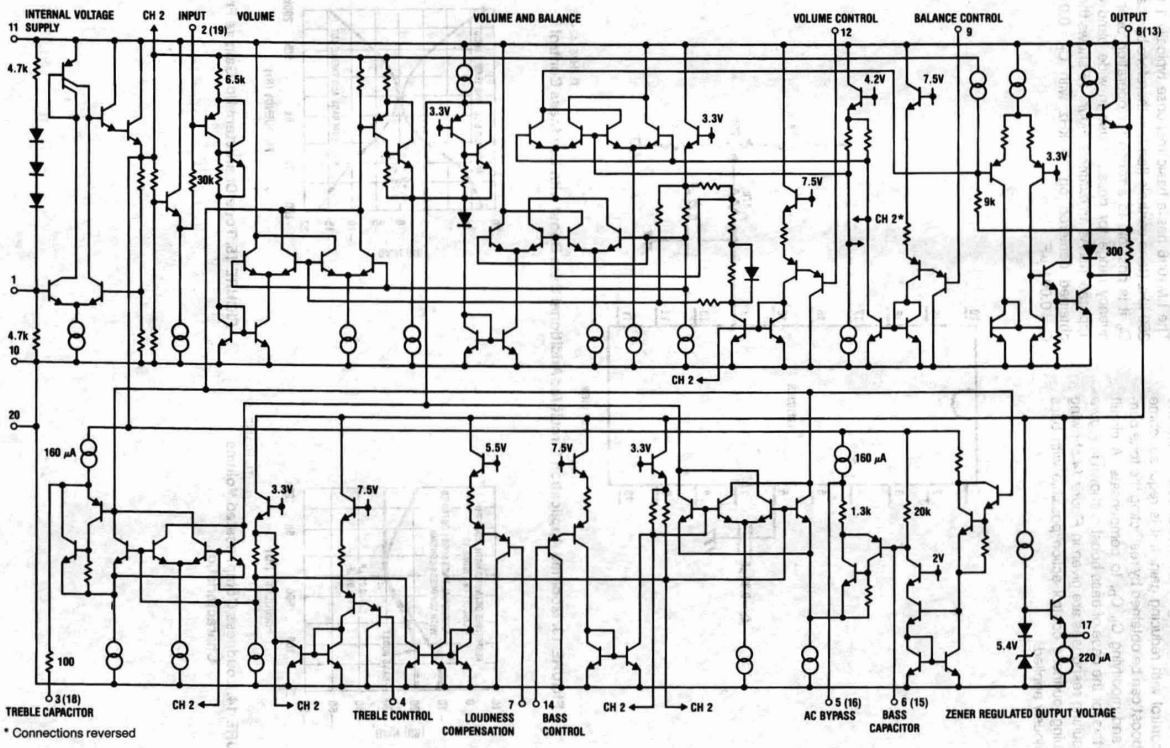
FIGURE 14. Loudness Compensated Volume Characteristic



TL/H/5142–18

FIGURE 15. Tone Characteristic (Gain vs Frequency)

Simplified Schematic Diagram (One Channel)



National Semiconductor

PRELIMINARY

LM1971
μPot™ Digitally Controlled 62 dB Audio Attenuator with Mute

General Description

The LM1971 is a digitally controlled single channel audio attenuator fabricated on a CMOS process. Attenuation is variable in 1 dB steps from 0 dB–62 dB. A mute function disconnects the input signal from the output, providing a minimum of 80 dB of attenuation. The attenuation curve can be customized through software to fit the desired application.

The performance of a μPot is demonstrated through its ability to instantly change attenuation levels without audible clicks or pops, excellent signal-to-noise ratio (80 dB minimum), and low Total Harmonic Distortion plus noise (THD + N) of 0.01%.

The LM1971 is controlled by a 3-wire serial digital interface which is TTL and CMOS compatible. The LM1971 receives data that selects the desired attenuation setting on the DATA line. The LOAD/SHIFT line enables the data input registers and the CLOCK line provides system timing. Additionally, the interface is compatible with National Semiconductor's HPC line of microcontrollers.

Key Specifications

- Total harmonic distortion + noise 0.01% (typ)
- Frequency response 20 kHz (−3 dB) (min)
- Attenuation range (excluding mute) 62 dB (min)
- Signal-to-noise ratio 80 dB (min)

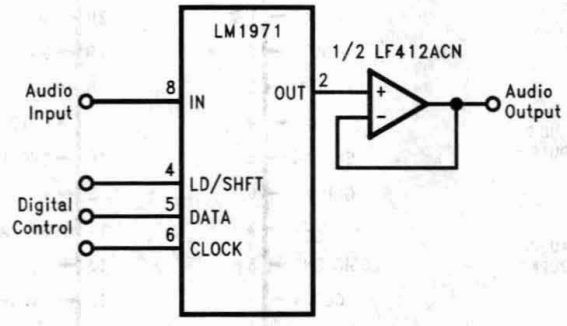
Features

- 3-wire serial interface
- 80 dB mute attenuation
- Pop and click free attenuation changes

Applications

- Music reproduction systems
- Sound reinforcement systems
- Electronic music (MIDI)
- Personal computer audio control
- Communication systems

Typical Application

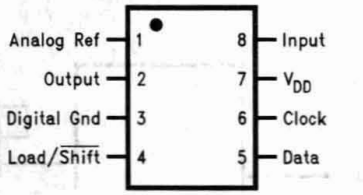


TL/H/12353–1

FIGURE 1. Typical Audio Attenuator Application Circuit

Connection Diagram

Small Outline Molded Package or Dual-In-Line Plastic Package



TL/H/12353–2

Top View

Order Number LM1971M or LM1971N
See NS Package Number M08A or N08E

National Semiconductor

LM1972
μPot™ 2-Channel 78dB Audio Attenuator with Mute

General Description

The LM1972 is a digitally controlled 2-channel 78dB audio attenuator fabricated on a CMOS process. Each channel has attenuation steps of 0.5dB from 0dB–47.5dB, 1.0dB steps from 48dB–78dB, with a mute function attenuating 104dB. Its logarithmic attenuation curve can be customized through software to fit the desired application.

The performance of a μPot is demonstrated through its excellent Signal-to-Noise Ratio, extremely low (THD + N), and high channel separation. Each μPot contains a mute function that disconnects the input signal from the output, providing a minimum attenuation of 96dB. Transitions between any attenuation settings are pop free.

The LM1972's 3-wire serial digital interface is TTL and CMOS compatible; receiving data that selects a channel and the desired attenuation level. The Data-Out pin of the LM1972 allows multiple μPots to be daisy-chained together, reducing the number of enable and data lines to be routed for a given application.

Key Specifications

- Total Harmonic Distortion + Noise 0.003% (max)
- Frequency response 100 kHz (−3dB) (min)
- Attenuation range (excluding mute) 78dB (typ)
- Differential attenuation ±0.25dB (max)
- Signal-to-noise ratio (ref. 4 Vrms) 110dB (min)
- Channel separation 100dB (min)

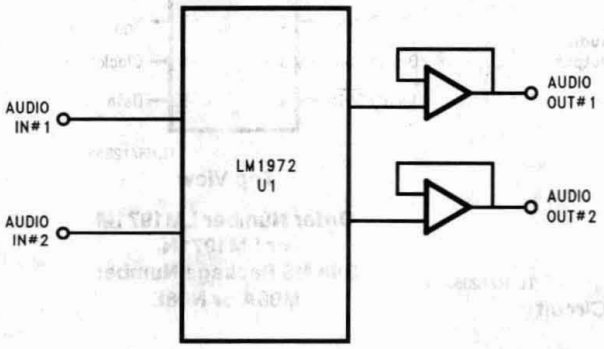
Features

- 3-wire serial interface
- Daisy-chain capability
- 104dB mute attenuation
- Pop and click free attenuation changes

Applications

- Automated studio mixing consoles
- Music reproduction systems
- Sound reinforcement systems
- Electronic music (MIDI)
- Personal computer audio control

Typical Application

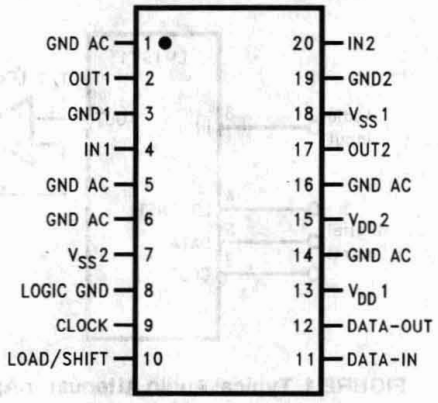


TL/H/11978–1

FIGURE 1. Typical Audio Attenuator Application Circuit

Connection Diagram

Dual-In-Line Plastic or Surface Mount Package



TL/H/11978–2

Top View

Order Number LM1972M or LM1972N
See NS Package Number M20B or N20A

Absolute Maximum Ratings (Notes 1, 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage ($V_{DD}-V_{SS}$)	15V
Voltage at Any Pin	V_{SS} − 0.2V to V_{DD} + 0.2V
Power Dissipation (Note 3)	150 mW
ESD Susceptability (Note 4)	2000V
Junction Temperature	150°C
Soldering Information N Package (10 sec.)	+260°C
Storage Temperature	−65°C to +150°C

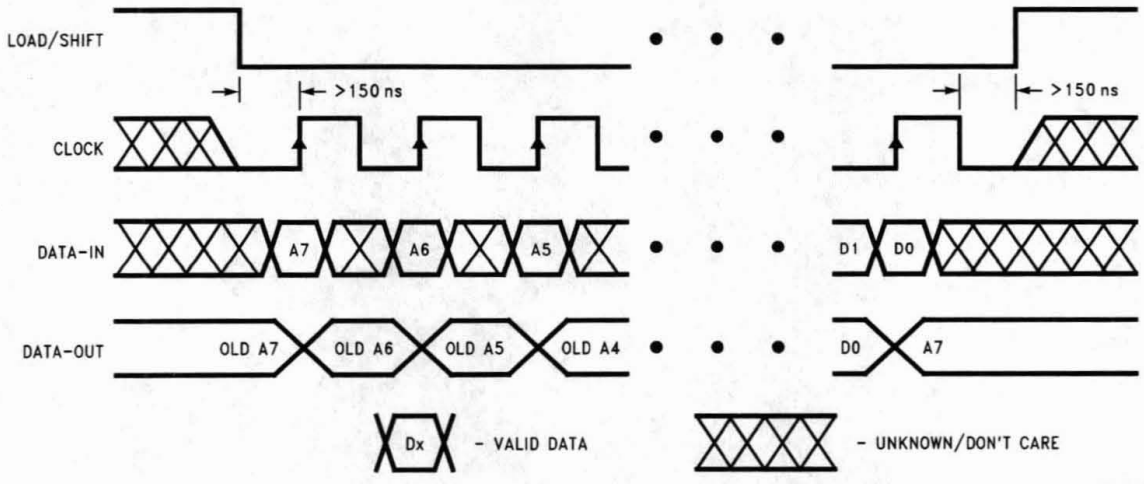
Operating Ratings (Notes 1, 2)

	T_{MIN}	T_A	T_{MAX}
Temperature Range $T_{MIN} \le T_A \le T_{MAX}$	0°C	$\le T_A$	$\le$ +70°C
Supply Voltage ($V_{DD} - V_{SS}$)			4.5V to 12V

Electrical Characteristics (Notes 1, 2)

The following specifications apply for all channels with V_{DD} = +6V, V_{SS} = −6V, V_{IN} = 5.5 Vpk, and f = 1 kHz, unless otherwise specified. Limits apply for T_A = 25°C. Digital inputs are TTL and CMOS compatible.

Symbol	Parameter	Conditions	LM1972 Typical (Note 5)	LM1972 Limit (Note 6)	Units (Limits)
I_S	Supply Current	Inputs are AC Grounded	2	4	mA (max)
THD+N	Total Harmonic Distortion plus Noise	V_{IN} = 0.5 Vpk @ 0dB Attenuation	0.0008	0.003	% (max)
XTalk	Crosstalk (Channel Separation)	0dB Attenuation for V_{IN} V_{CH} measured @ −78dB	110	100	dB (min)
SNR	Signal-to-Noise Ratio	Inputs are AC Grounded @ −12dB Attenuation A-Weighted	120	110	dB (min)
A_M	Mute Attenuation		104	96	dB (min)
	Attenuation Step Size Error	0dB to −47.5dB −48dB to −78dB		±0.05 ±0.25	dB (max) dB (max)
	Absolute Attenuation Error	Attenuation @ 0dB Attenuation @ −20dB Attenuation @ −40dB Attenuation @ −60dB Attenuation @ −78dB	0.03 19.8 39.5 59.3 76.3	0.5 19.0 39.0 57.5 74.5	dB (min) dB (min) dB (min) dB (min) dB (min)
	Channel-to-Channel Attenuation Tracking Error	Attenuation @ 0dB, −20dB, −40dB, −60dB Attenuation @ −78dB		±0.5 ±0.75	dB (max) dB (max)
I_{LEAK}	Analog Input Leakage Current	Inputs are AC Grounded	10.0	100	nA (max)



TL/H/11978–3

FIGURE 2. Timing Diagram

Electrical Characteristics (Notes 1, 2)

The following specifications apply for all channels with $V_{DD} = +6V$, $V_{SS} = -6V$, $V_{IN} = 5.5$ Vpk, and f = 1 kHz, unless otherwise specified. Limits apply for $T_A = 25°C$. Digital inputs are TTL and CMOS compatible. (Continued)

Symbol	Parameter	Conditions	LM1972		Units (Limits)
			Typical (Note 5)	Limit (Note 6)	
R_{IN}	AC Input Impedance	Pins 4, 20, $V_{IN} = 1.0$ Vpk, f = 1 kHz	40	20 60	kΩ (min) kΩ (max)
I_{IN}	Input Current	@ Pins 9, 10, 11 @ $0V < V_{IN} < 5V$	1.0	±100	nA (max)
f_{CLK}	Clock Frequency		3	2	MHz (max)
V_{IH}	High-Level Input Voltage	@ Pins 9, 10, 11		2.0	V (min)
V_{IL}	Low-Level Input Voltage	@ Pins 9, 10, 11		0.8	V (max)
	Data-Out Levels (Pin 12)	$V_{DD} = 6V$, $V_{SS} = 0V$		0.1 5.9	V (max) V (min)

Note 1: All voltages are measured with respect to GND pins (1, 3, 5, 6, 14, 16, 19), unless otherwise specified.

Note 2: *Absolute Maximum Ratings* indicate limits beyond which damage to the device may occur. *Operating Ratings* indicate conditions for which the device is functional, but do not guarantee specific performance limits. *Electrical Characteristics* state DC and AC electrical specifications under particular test conditions which guarantee specific performance limits. This assumes that the device is within the Operating Ratings. Specifications are not guaranteed for parameters where no limit is given, however, the typical value is a good indication of device performance.

Note 3: The maximum power dissipation must be derated at elevated temperatures and is dictated by T_{JMAX}, θ_{JA}, and the ambient temperature T_A. The maximum allowable power dissipation is $PD = (T_{JMAX} - T_A)/\theta_{JA}$ or the number given in the Absolute Maximum Ratings, whichever is lower. For the LM1972, $T_{JMAX} = +150°C$, and the typical junction-to-ambient thermal resistance, when board mounted, is 65°C/W.

Note 4: Human body model, 100 pF discharged through a 1.5 kΩ resistor.

Note 5: Typicals are measured at 25°C and represent the parametric norm.

Note 6: Limits are guaranteed to National's AOQL (Average Output Quality Level).

Pin Description

Signal Ground (3, 19): Each input has its own independent ground, GND1 and GND2.

Signal Input (4, 20): There are 2 independent signal inputs, IN1 and IN2.

Signal Output (2, 17): There are 2 independent signal outputs, OUT1 and OUT2.

Voltage Supply (13, 15): Positive voltage supply pins, V_{DD1} and V_{DD2}.

Voltage Supply (7, 18): Negative voltage supply pins, V_{SS1} and V_{SS2}. To be tied to ground in a single supply configuration.

AC Ground (1, 5, 6, 14, 16): These five pins are not physically connected to the die in any way (i.e., No bondwires). These pins must be AC grounded to prevent signal coupling between any of the pins nearby. Pin 14 should be connected to pins 13 and 15 for ease of wiring and the best isolation, as an example.

Logic Ground (8): Digital signal ground for the interface lines; CLOCK, LOAD/SHIFT, DATA-IN and DATA-OUT.

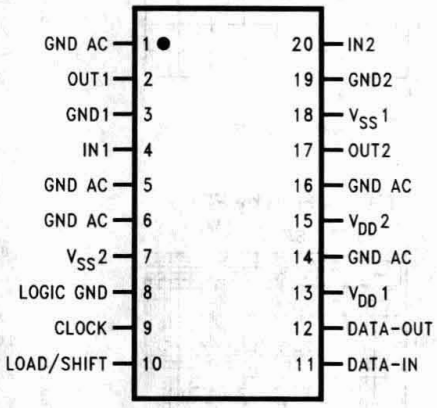
Clock (9): The clock input accepts a TTL or CMOS level signal. The clock input is used to load data into the internal shift register on the rising edge of the input clock waveform.

Load/Shift (10): The load/shift input accepts a TTL or CMOS level signal. This is the enable pin of the device, allowing data to be clocked in while this input is low (0V).

Data-In (11): The data-in input accepts a TTL or CMOS level signal. This pin is used to accept serial data from a microcontroller that will be latched and decoded to change a channel's attenuation level.

Data-Out (12): This pin is used in daisy-chain mode where more than one μPot is controlled via the same data line. As the data is clocked into the chain from the μC, the preceding data in the shift register is shifted out the DATA-OUT pin to the next μPot in the chain or to ground if it is the last μPot in the chain. The LOAD/SHIFT line goes high once all of the new data has been shifted into each of its respective registers.

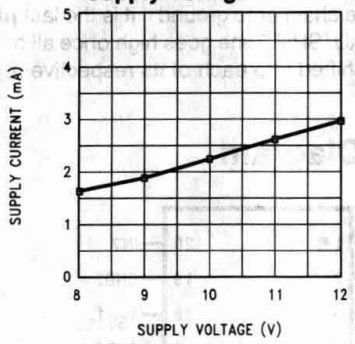
Connection Diagram



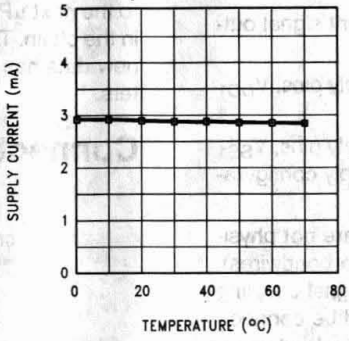
TL/H/11978–4

Typical Performance Characteristics

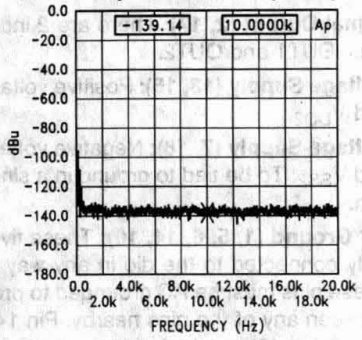
Supply Current vs Supply Voltage



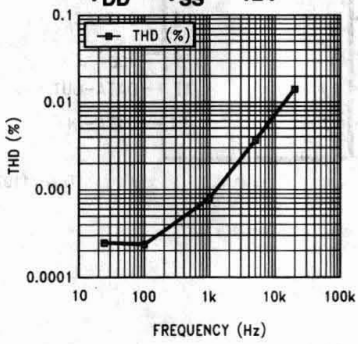
Supply Current vs Temperature



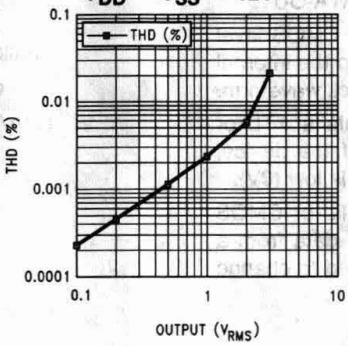
Noise Floor Spectrum by FFT Amplitude vs Frequency



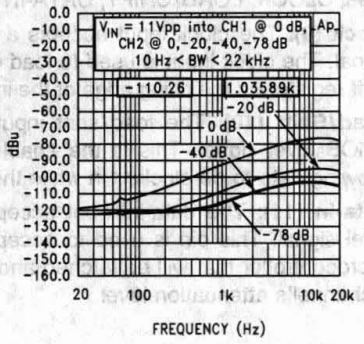
THD vs Freq by FFT $V_{DD} - V_{SS} = 12V$



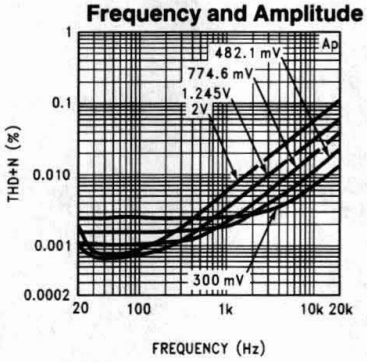
THD vs V_{OUT} at 1 KHz by FFT $V_{DD} - V_{SS} = 12V$



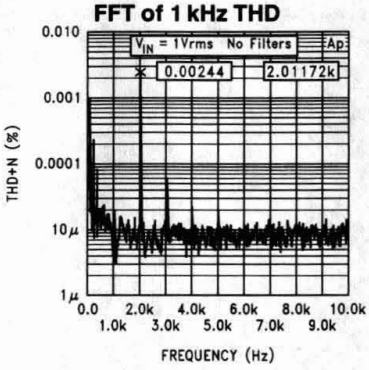
Crosstalk Test



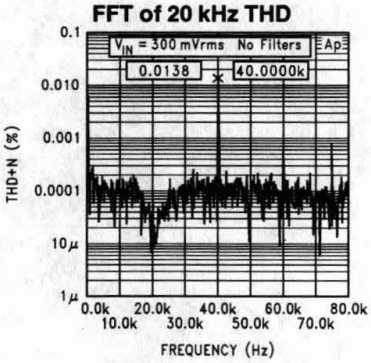
THD + N vs Frequency and Amplitude



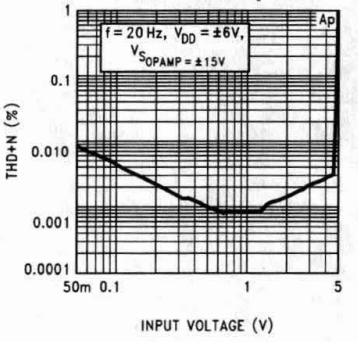
FFT of 1 kHz THD



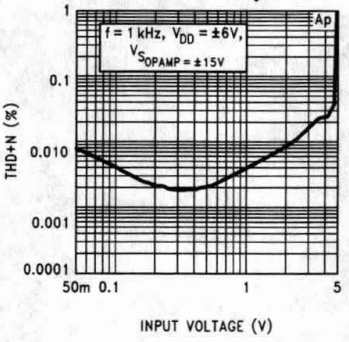
FFT of 20 kHz THD



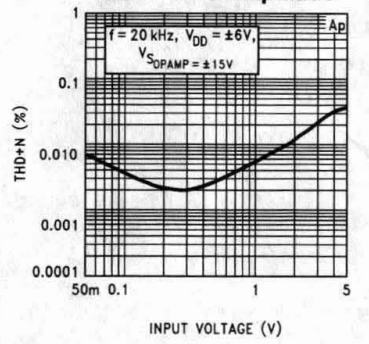
THD + N vs Amplitude



THD + N vs Amplitude



THD + N vs Amplitude



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Application Information

ATTENUATION STEP SCHEME

The fundamental attenuation step scheme for the LM1972 μPot is shown in *Figure 3*. This attenuation step scheme, however, can be changed through programming techniques to fit different application requirements. One such example would be a constant logarithmic attenuation scheme of 1dB steps for a panning function as shown in *Figure 4*. The only restriction to the customization of attenuation schemes are the given attenuation levels and their corresponding data bits shown in Table I. The device will change attenuation levels only when a channel address is recognized. When recognized, the attenuation level will be changed corresponding to the data bits shown in Table I. As shown in *Figure 6*, an LM1972 can be configured as a panning control which separates the mono signal into left and right channels. This circuit may utilize the fundamental attenuation scheme of the LM1972 or be programmed to provide a constant 1dB logarithmic attenuation scheme as shown in *Figure 4*.

LM1972 Channel Attenuation vs Digital Step Value

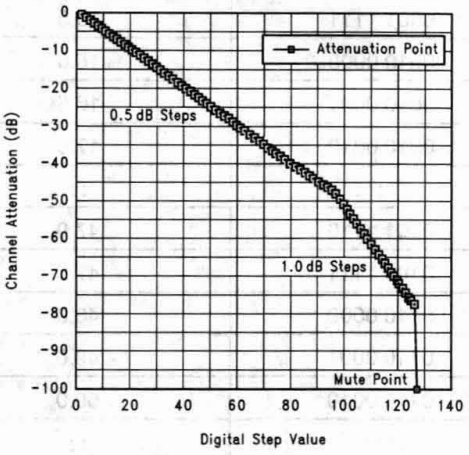

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FIGURE 3. LM1972 Attenuation Step Scheme

LM1972 Channel Attenuation vs Digital Step Value (Programmed 1.0dB Steps)

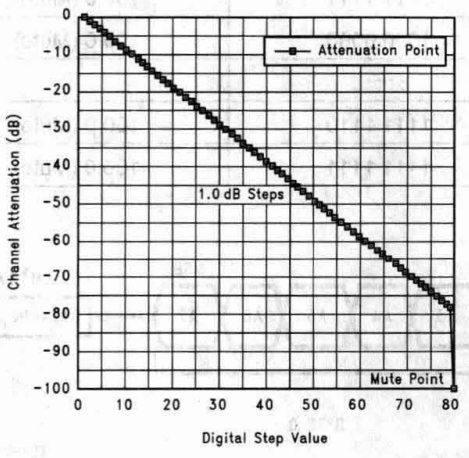

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FIGURE 4. LM1972 1.0dB Attenuation Step Scheme

LM1972 Channel Attenuation vs Digital Step Value (Programmed 2.0dB Steps)

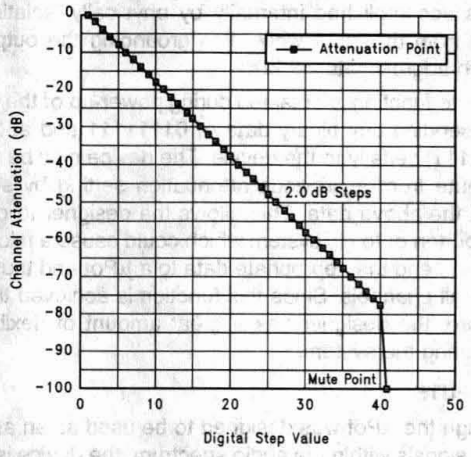

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FIGURE 5. LM1972 2.0dB Attenuation Step Scheme

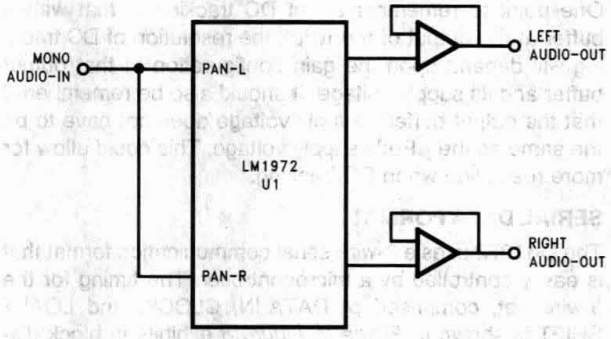

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FIGURE 6. Mono Panning Circuit

INPUT IMPEDANCE

The input impedance of a μPot is constant at a nominal 40 kΩ. To eliminate any unwanted DC components from propagating through the device it is common to use 1 μF input coupling caps. This is not necessary, however, if the dc offset from the previous stage is negligible. For higher performance systems, input coupling caps are preferred.

OUTPUT IMPEDANCE

The output of a μPot varies typically between 25 kΩ and 35 kΩ and changes nonlinearly with step changes. Since a μPot is made up of a resistor ladder network with a logarithmic attenuation, the output impedance is nonlinear. Due to this configuration, a μPot cannot be considered as a linear potentiometer, but can be considered only as a logarithmic attenuator.

It should be noted that the linearity of a μPot cannot be measured directly without a buffer because the input impedance of most measurement systems is not high enough to provide the required accuracy. Due to the low impedance of the measurement system, the output of the μPot would be loaded down and an incorrect reading will result. To prevent loading from occurring, a JFET input op amp should be used as the buffer/amplifier. The performance of a μPot is limited only by the performance of the external buffer/amplifier.

Application Information (Continued)

MUTE FUNCTION

One major feature of a μPot is its ability to mute the input signal to an attenuation level of 104dB as shown in *Figure 3.* This is accomplished internally by physically isolating the output from the input while also grounding the output pin through approximately 2 kΩ.

The mute function is obtained during power-up of the device or by sending any binary data of 01111111 and above (to 11111111) serially to the device. The device may be placed into mute from a previous attenuation setting by sending any of the above data. This allows the designer to place a mute button onto his system which could cause a microcontroller to send the appropriate data to a μPot and thus mute any or all channels. Since this function is achieved through software, the designer has a great amount of flexibility in configuring the system.

DC INPUTS

Although the μPot was designed to be used as an attenuator for signals within the audio spectrum, the device is capable of tracking an input DC voltage. The device will track DC voltages to a diode drop above each supply rail.

One point to remember about DC tracking is that with a buffer at the output of the μPot, the resolution of DC tracking will depend upon the gain configuration of that output buffer and its supply voltage. It should also be remembered that the output buffer's supply voltage does not have to be the same as the μPot's supply voltage. This could allow for more resolution when DC tracking.

SERIAL DATA FORMAT

The LM1972 uses a 3-wire serial communication format that is easily controlled by a microcontroller. The timing for the 3-wire set, comprised of DATA-IN, CLOCK, and LOAD/SHIFT is shown in *Figure 2. Figure 8* exhibits in block diagram form how the digital interface controls the tap switches which select the appropriate attenuation level. As depicted in *Figure 2,* the LOAD/SHIFT line is to go low at least 150 ns before the rising edge of the first clock pulse and is to remain low throughout the transmission of each set of 16 data bits. The serial data is comprised of 8 bits for channel selection and 8 bits for attenuation setting. For both address data and attenuation setting data, the MSB is sent first and the 8 bits of address data are to be sent before the 8 bits of attenuation data. Please refer to *Figure 7* to confirm the serial data format transfer process.

TABLE I. LM1972 Micropot Attenuator Register Set Description

MSB LSB	
Address Register (Byte 0)	
0000 0000	Channel 1
0000 0001	Channel 2
0000 0010	Channel 3
Data Register (Byte 1)	
Contents	**Attenuation Level dB**
0000 0000	0.0
0000 0001	0.5
0000 0010	1.0
0000 0011	1.5
:::::	::
0001 1110	15.0
0001 1111	15.5
0010 0000	16.0
0010 0001	16.5
0010 0010	17.0
:::::	::
0101 1110	47.0
0101 1111	47.5
0110 0000	48.0
0110 0001	49.0
0110 0010	50.0
:::::	::
0111 1100	76.0
0111 1101	77.0
0111 1110	78.0
0111 1111	100.0 (Mute)
1000 0000	100.0 (Mute)
:::::	::
1111 1110	100.0 (Mute)
1111 1111	100.0 (Mute)

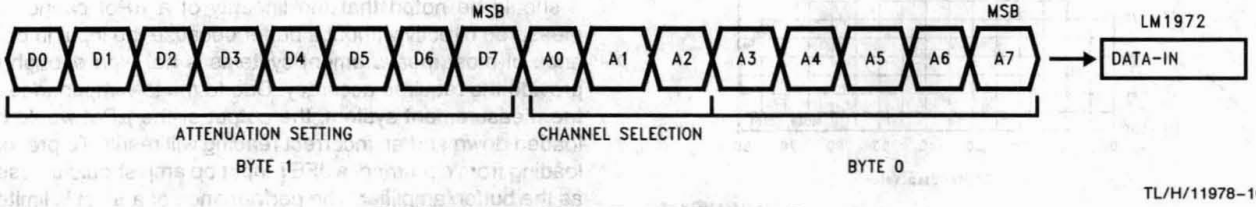

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FIGURE 7. Serial Data Format Transfer Process

Application Information (Continued)

μPot SYSTEM ARCHITECTURE

The μPot's digital interface is essentially a shift register, where serial data is shifted in, latched, and then decoded. As new data is shifted into the DATA-IN pin, the previously latched data is shifted out the DATA-OUT pin. Once the data is shifted in, the LOAD/SHIFT line goes high, latching in the new data. The data is then decoded and the appropriate switch is activated to set the desired attenuation level for the selected channel. This process is continued each and every time an attenuation change is made. Each channel is updated, only, when that channel is selected for an attenuator change or the system is powered down and then back up again. When the μPot is powered up, each channel is placed into the muted mode.

μPot LADDER ARCHITECTURE

Each channel of a μPot has its own independent resistor ladder network. As shown in *Figure 9,* the ladder consists of multiple R1/R2 elements which make up the attenuation scheme. Within each element there are tap switches that select the appropriate attenuation level corresponding to the data bits in Table I. It can be seen in *Figure 9* that the input impedance for the channel is a constant value regardless of which tap switch is selected, while the output impedance varies according to the tap switch selected.

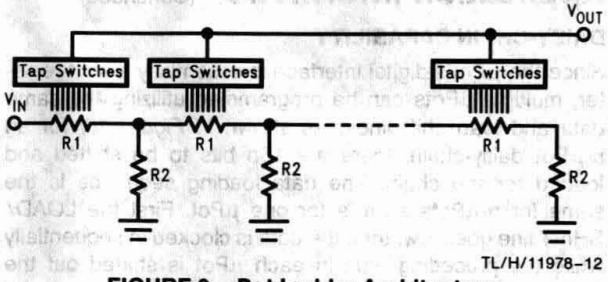

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FIGURE 9. μPot Ladder Architecture

DIGITAL LINE COMPATIBILITY

The μPot's digital interface section is compatible with either TTL or CMOS logic due to the shift register inputs acting upon a threshold voltage of 2 diode drops or approximately 1.4V.

DIGITAL DATA-OUT PIN

The DATA-OUT pin is available for daisy-chain system configurations where multiple μPots will be used. The use of the daisy-chain configuration allows the system designer to use only one DATA and one LOAD/SHIFT line per chain, thus simplifying PCB trace layouts.

In order to provide the highest level of channel separation and isolate any of the signal lines from digital noise, the DATA-OUT pin should be terminated through a 2 kΩ resistor if not used. The pin may be left floating, however, any signal noise on that line may couple to adjacent lines creating higher noise specs.

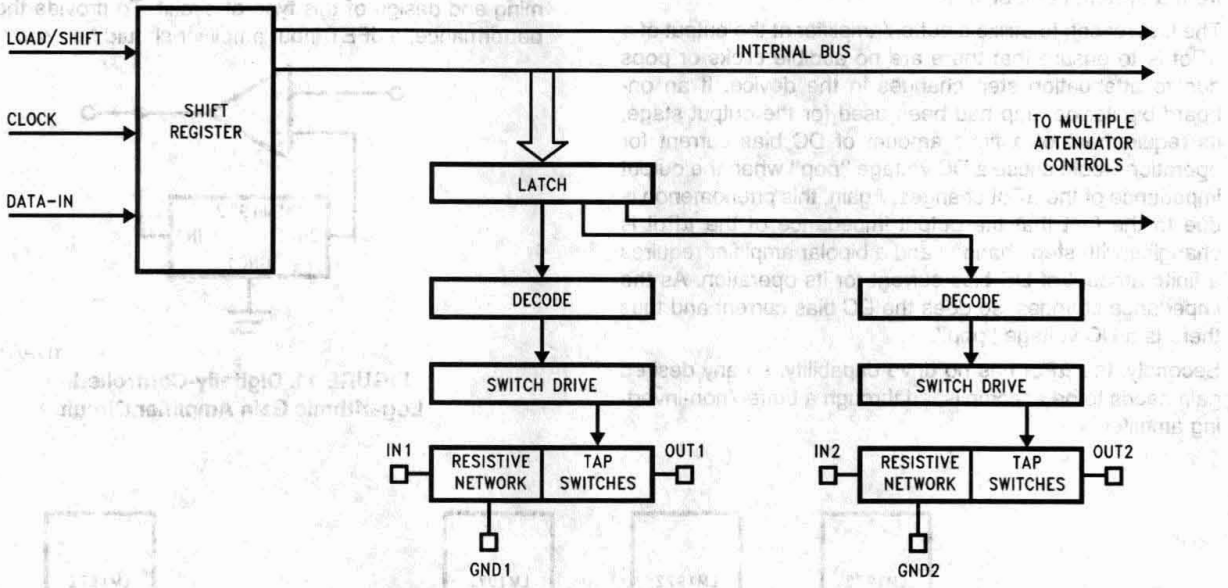

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FIGURE 8. μPot System Architecture

Application Information (Continued)

DAISY-CHAIN CAPABILITY

Since the μPot's digital interface is essentially a shift register, multiple μPots can be programmed utilizing the same data and load/shift lines. As shown in *Figure 10,* for an n-μPot daisy-chain, there are 16n bits to be shifted and loaded for the chain. The data loading sequence is the same for n-μPots as it is for one μPot. First the LOAD/SHIFT line goes low, then the data is clocked in sequentially while the preceding data in each μPot is shifted out the DATA-OUT pin to the next μPot in the chain or to ground if it is the last μPot in the chain. Then the LOAD/SHIFT line goes high; latching the data into each of their corresponding μPots. The data is then decoded according to the address (channel selection) and the appropriate tap switch controlling the attenuation level is selected.

CROSSTALK MEASUREMENTS

The crosstalk of a μPot as shown in the **Typical Performance Characteristics** section was obtained by placing a signal on one channel and measuring the level at the output of another channel of the same frequency. It is important to be sure that the signal level being measured is of the same frequency such that a true indication of crosstalk may be obtained. Also, to ensure an accurate measurement, the measured channel's input should be AC grounded through a 1 μF capacitor.

CLICKS AND POPS

So, why is that output buffer needed anyway? There are three answers to this question, all of which are important from a system point of view.

The first reason to utilize a buffer/amplifier at the output of a μPot is to ensure that there are no audible clicks or pops due to attenuation step changes in the device. If an on-board bipolar op amp had been used for the output stage, its requirement of a finite amount of DC bias current for operation would cause a DC voltage "pop" when the output impedance of the μPot changes. Again, this phenomenon is due to the fact that the output impedance of the μPot is changing with step changes and a bipolar amplifier requires a finite amount of DC bias current for its operation. As the impedance changes, so does the DC bias current and thus there is a DC voltage "pop".

Secondly, the μPot has no drive capability, so any desired gain needs to be accomplished through a buffer/non-inverting amplifer.

Third, the output of a μPot needs to see a high impedance to prevent loading and subsequent linearity errors from ocurring. A JFET input buffer provides a high input impedance to the output of the μPot so that this does not occur.

Clicks and pops can be avoided by using a JFET input buffer/amplifier such as an LF412ACN. The LF412 has a high input impedance and exhibits both a low noise floor and low THD+N throughout the audio spectrum which maintains signal integrity and linearity for the system. The performance of the system solution is entirely dependent upon the quality and performance of the JFET input buffer/amplifier.

LOGARITHMIC GAIN AMPUFIER

The μPot is capable of being used in the feedback loop of an amplifier, however, as stated previously, the output of the μPot needs to see a high impedance in order to maintain its high performance and linearity. Again, loading the output will change the values of attenuation for the device. As shown in *Figure 11,* a μPot used in the feedback loop creates a logarithmic gain amplifier. In this configuration the attenuation levels from Table I, now become gain levels with the largest possible gain value being 78dB. For most applications 78dB of gain will cause signal clipping to occur, however, because of the μPot's versatility the gain can be controlled through programming such that the clipping level of the system is never obtained. An important point to remember is that when in mute mode the input is disconnected from the output. In this configuration this will place the amplifier in its open loop gain state, thus resulting in severe comparator action. Care should be taken with the programming and design of this type of circuit. To provide the best performance, a JFET input amplifier should be used.

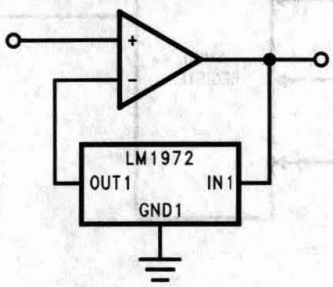

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FIGURE 11. Digitally-Controlled Logarithmic Gain Amplifier Circuit

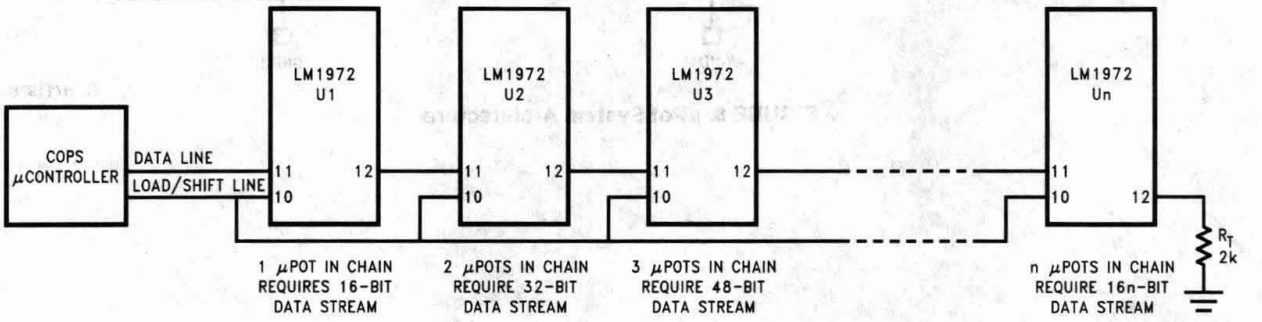

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FIGURE 10. n-μPot Daisy-Chained Circuit

National Semiconductor

LM1973
μPot™ 3-Channel 76dB Audio Attenuator with Mute

General Description

The LM1973 is a digitally controlled 3-channel 76dB audio attenuator fabricated on a CMOS process. Each channel has attenuation steps of 0.5dB from 0dB–15.5dB, 1.0dB steps from 16dB–47dB, and 2.0dB steps from 48dB–76dB, with a mute function attenuating 104dB. Its logarithmic attenuation curve can be customized through software to fit the desired application.

The performance of a μPot is demonstrated through its excellent Signal-to-Noise Ratio, extremely low (THD + N), and high channel separation. Each μPot contains a mute function that disconnects the input signal from the output, providing a minimum attenuation of 96dB. Transitions between any attenuation settings are pop free.

The LM1973's 3-wire serial digital interface is TTL and CMOS compatible; receiving data that selects a channel and the desired attenuation level. The Data-Out pin of the LM1973 allows multiple μPots to be daisy-chained together, reducing the number of enable and data lines to be routed for a given application.

Key Specifications

- Total Harmonic Distortion + Noise — 0.003% (max)
- Frequency response — 100 kHz (−3dB) (min)
- Attenuation range (excluding mute) — 76dB (typ)
- Differential attenuation — ±0.25dB (max)
- Signal-to-noise ratio (ref. 4 Vrms) — 110dB (min)
- Channel separation — 110dB (typ)

Features

- 3-wire serial interface
- Daisy-chain capability
- 104dB mute attenuation
- Pop and click free attenuation changes

Applications

- Automated studio mixing consoles
- Music reproduction systems
- Sound reinforcement systems
- Electronic music (MIDI)
- Personal computer audio control

Typical Application

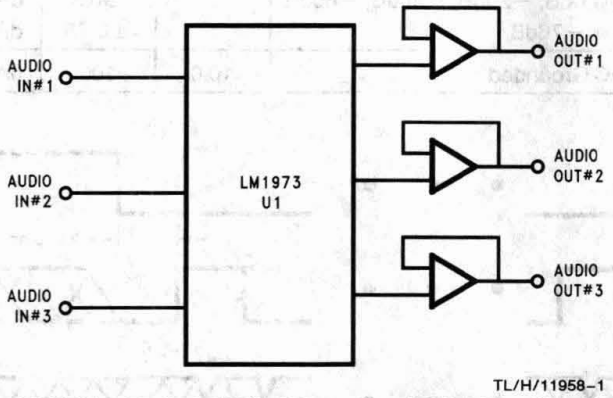

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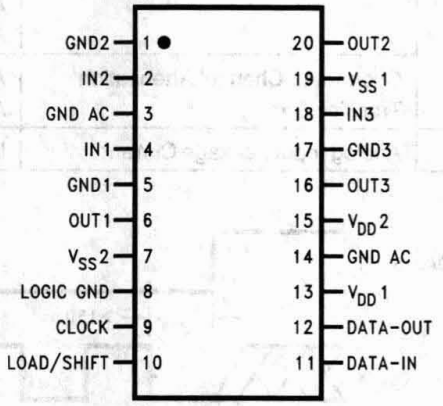
FIGURE 1. Typical Audio Attenuator Application Circuit

Connection Diagram

Dual-In-Line Plastic or Surface Mount Package



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Top View

Order Number LM1973M or LM1973N
See NS Package Number M20B or N20A

Absolute Maximum Ratings (Notes 1, 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage ($V_{DD}-V_{SS}$)	15V
Voltage at Any Pin	V_{SS} − 0.2V to V_{DD} + 0.2V
Power Dissipation (Note 3)	150 mW
ESD Susceptability (Note 4)	1800V
Junction Temperature	150°C
Soldering Information N Package (10 sec.)	+260°C
Storage Temperature	−65°C to +150°C

Operating Ratings (Notes 1, 2)

	T_{MIN}	T_A	T_{MAX}
Temperature Range $T_{MIN} \le T_A \le T_{MAX}$	0°C	$\le T_A$	$\le$ +70°C
Supply Voltage ($V_{DD} - V_{SS}$)	4.5V to 12V		

Electrical Characteristics (Notes 1, 2)

The following specifications apply for all channels with V_{DD} = +6V, V_{SS} = −6V, V_{IN} = 5.5 Vpk, and f = 1 kHz, unless otherwise specified. Limits apply for T_A = 25°C. Digital inputs are TTL and CMOS compatible.

Symbol	Parameter	Conditions	LM1973 Typical (Note 5)	LM1973 Limit (Note 6)	Units (Limits)
I_S	Supply Current	Inputs are AC Grounded	3	5	mA (max)
THD+N	Total Harmonic Distortion plus Noise	V_{IN} = 0.5 Vpk @ 0dB Attenuation	0.0008	0.003	% (max)
XTalk	Crosstalk (Channel Separation) (Note 7)	0dB Attenuation for V_{IN} V_{CH} measured @ −76dB	110		dB
SNR	Signal-to-Noise Ratio	Inputs are AC Grounded @ −12dB Attenuation A-Weighted	120	110	dB (min)
A_M	Mute Attenuation		104	96	dB (min)
	Attenuation Step Size Error	0dB to −16dB		±0.05	dB (max)
		−17dB to −48dB		±0.1	dB (max)
		−49dB to −76dB		±0.25	dB (max)
	Absolute Attenuation Error	Attenuation @ 0dB	0.01	0.5	dB (min)
		Attenuation @ −20dB	19.8	19.0	dB (min)
		Attenuation @ −40dB	39.5	38.5	dB (min)
		Attenuation @ −60dB	59.3	58.0	dB (min)
		Attenuation @ −76dB	74.5	73.0	dB (min)
	Channel-to-Channel Attenuation Tracking Error	Attenuation @ 0dB, −20dB, −40dB, −60dB		±0.5	dB (max)
		Attenuation @ −76dB		±0.75	dB (max)
I_{LEAK}	Analog Input Leakage Current	Inputs are AC Grounded	10.0	100	nA (max)

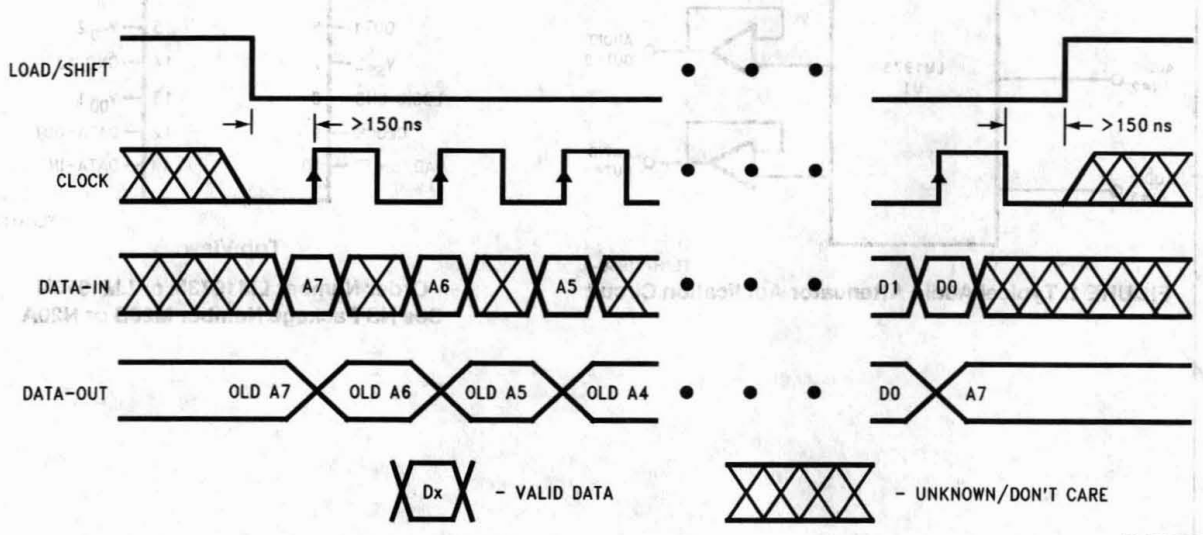

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FIGURE 2. Timing Diagram

Electrical Characteristics (Notes 1, 2)

The following specifications apply for all channels with $V_{DD} = +6V$, $V_{SS} = -6V$, $V_{IN} = 5.5$ Vpk, and f = 1 kHz, unless otherwise specified. Limits apply for $T_A = 25°C$. Digital inputs are TTL and CMOS compatible. (Continued)

Symbol	Parameter	Conditions	LM1973		Units (Limits)
			Typical (Note 5)	Limit (Note 6)	
R_{IN}	AC Input Impedance	Pins 2, 4, 18, $V_{IN} = 1.0$ Vpk, f = 1 kHz	40	20 60	kΩ (min) kΩ (max)
I_{IN}	Input Current	@ Pins 9, 10, 11 @ $0V < V_{IN} < 5V$	1.0	±100	nA (max)
f_{CLK}	Clock Frequency		3	2	MHz (max)
V_{IH}	High-Level Input Voltage	@ Pins 9, 10, 11		2.0	V (min)
V_{IL}	Low-Level Input Voltage	@ Pins 9, 10, 11		0.8	V (max)
	Data-Out Levels (Pin 12)	$V_{DD} = 6V$, $V_{SS} = 0V$		0.1 5.9	V (max) V (min)

Note 1: All voltages are measured with respect to GND (pins 1,3, 5, 14, 17), unless otherwise specified.

Note 2: *Absolute Maximum Ratings* indicate limits beyond which damage to the device may occur. *Operating Ratings* indicate conditions for which the device is functional, but do not guarantee specific performance limits. *Electrical Characteristics* state DC and AC electrical specifications under particular test conditions which guarantee specific performance limits. This assumes that the device is within the Operating Ratings. Specifications are not guaranteed for parameters where no limit is given, however, the typical value is a good indication of device performance.

Note 3: The maximum power dissipation must be derated at elevated temperatures and is dictated by T_{JMAX}, θ_{JA}, and the ambient temperature T_A. The maximum allowable power dissipation is $PD = (T_{JMAX} - T_A)/\theta_{JA}$ or the number given in the Absolute Maximum Ratings, whichever is lower. For the LM1973N, $T_{JMAX} = +150°C$, and the typical junction-to-ambient thermal resistance, when board mounted, is 65°C/W.

Note 4: Human body model, 100 pF discharged through a 1.5 kΩ resistor.

Note 5: Typicals are measured at 25°C and represent the parametric norm.

Note 6: Limits are guaranteed to National's AOQL (Average Output Quality Level).

Note 7: At the present time the Crosstalk measurement is specified as a typical only, which is due to a hardware limitation of the automated test equipment.

Pin Description

Signal Ground (1, 5, 17): Each input has its own independent ground, GND1, GND2, and GND3.

Signal Input (2, 4, 18): There are 3 independent signal inputs, IN1, IN2, and IN3.

Signal Output (6, 16, 20): There are 3 independent signal outputs, OUT1, OUT2, and OUT3.

Voltage Supply (13, 15): Positive voltage supply pins, V_{DD1} and V_{DD2}.

Voltage Supply (7, 19): Negative voltage supply pins, V_{SS1} and V_{SS2}. To be tied to ground in a single supply configuration.

AC Ground (3, 14): These two pins are not physically connected to the die in any way (i.e., No bondwires). These pins must be AC grounded to prevent signal coupling between any of the pins nearby. Pin 14 should be connected to pins 13 and 15 for ease of wiring and the best isolation.

Logic Ground (8): Digital signal ground for the interface lines; CLOCK, LOAD/SHIFT, DATA-IN and DATA-OUT.

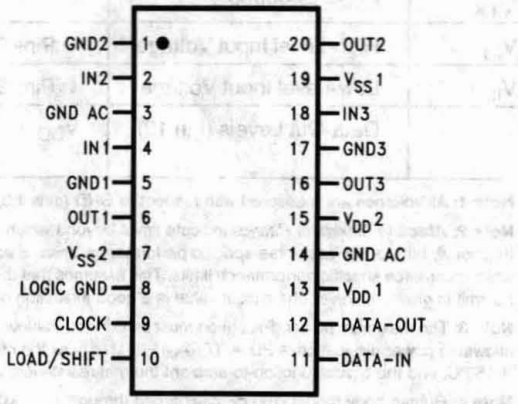
Clock (9): The clock input accepts a TTL or CMOS level signal. The clock input is used to load data into the internal shift register on the rising edge of the input clock waveform.

Load/Shift (10): The load/shift input accepts a TTL or CMOS level signal. This is the enable pin of the device, allowing data to be clocked in while this input is low (0V).

Data-In (11): The data-in input accepts a TTL or CMOS level signal. This pin is used to accept serial data from a microcontroller that will be latched and decoded to change a channel's attenuation level.

Data-Out (12): This pin is used in daisy-chain mode where more than one μPot is controlled via the same data line. As the data is clocked into the chain from the μC, the preceding data in the shift register is shifted out the DATA-OUT pin to the next μPot in the chain or to ground if it is the last μPot in the chain. The LOAD/SHIFT line goes high once all of the new data has been shifted into each of its respective registers.

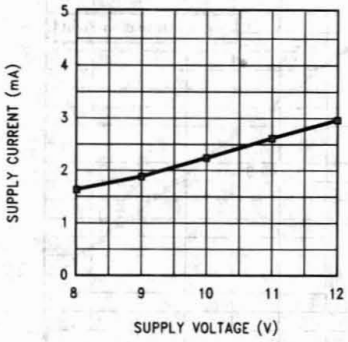
Connection Diagram



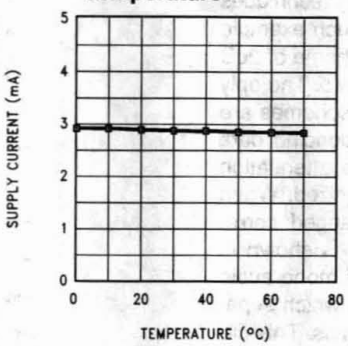
TL/H/11958–4

Typical Performance Characteristics

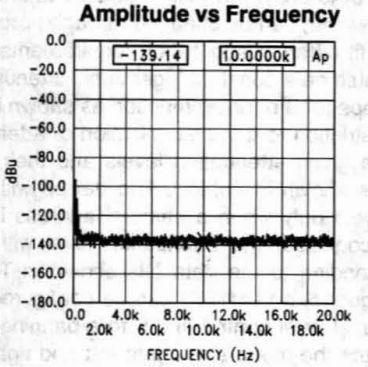
Supply Current vs Supply Voltage



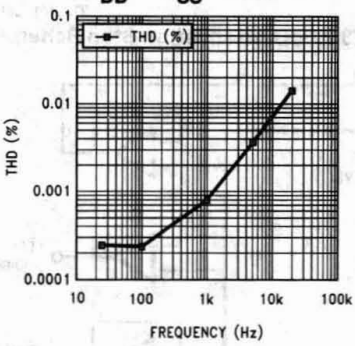
Supply Current vs Temperature



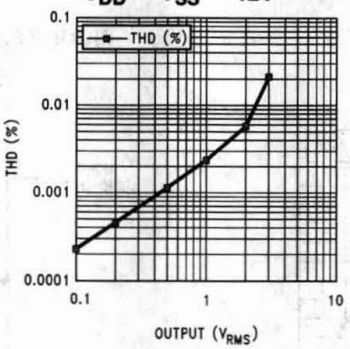
Noise Floor Spectrum by FFT Amplitude vs Frequency



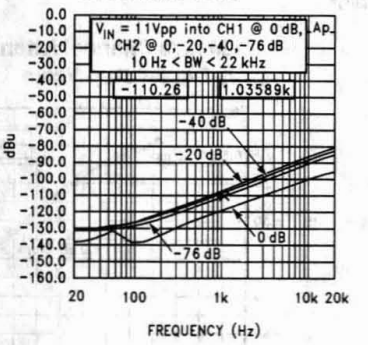
THD vs Freq by FFT $V_{DD} - V_{SS} = 12V$



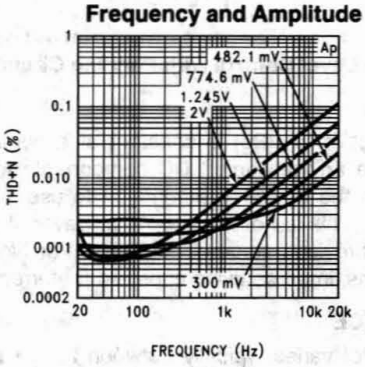
THD vs V_{OUT} at 1 kHz by FFT $V_{DD} - V_{SS} = 12V$



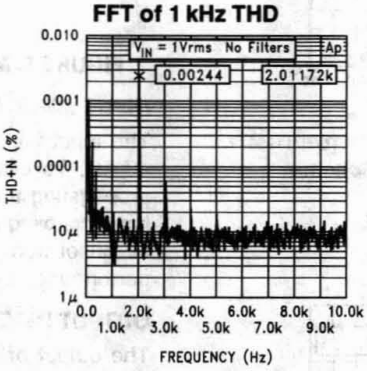
Crosstalk Test



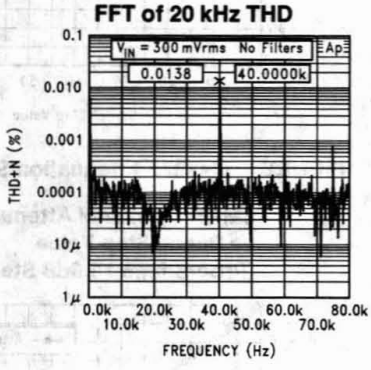
THD + N vs Frequency and Amplitude



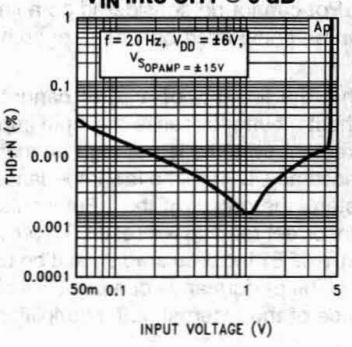
FFT of 1 kHz THD



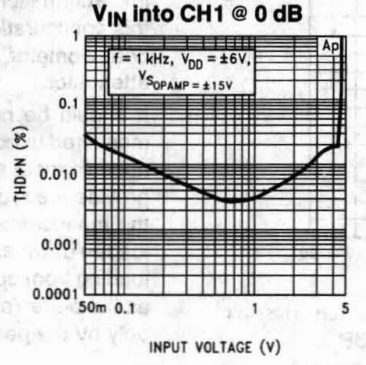
FFT of 20 kHz THD



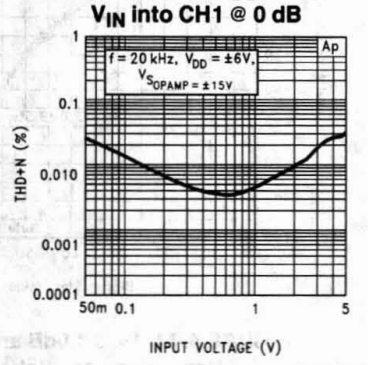
THD + N vs Amplitude $f = 20$ Hz, $V_{DD} = \pm 6V$ V_{IN} into CH1 @ 0 dB



THD + N vs Amplitude $f = 1$ kHz, $V_{DD} = \pm 6V$ V_{IN} into CH1 @ 0 dB



THD + N vs Amplitude $f = 20$ kHz, $V_{DD} = \pm 6V$ V_{IN} into CH1 @ 0 dB



TL/H/11958–6

Application Information

ATTENUATION STEP SCHEME

The fundamental attenuation step scheme for the LM1973 μPot is shown in *Figure 3.* This attenuation step scheme, however, can be changed through programming techniques to fit different application requirements. One such example would be a constant logarithmic attenuation scheme of 2dB steps for a panning function as shown in *Figure 5.* The only restriction to the customization of attenuation schemes are the given attenuation levels and their corresponding data bits shown in Table I. The device will change attenuation levels only when a channel address is recognized. When recognized, the attenuation level will be changed corresponding to the data bits shown in Table I. As shown in *Figure 6,* an LM1973 can be configured with a mono audio signal level control and with a panning control which separates the mono signal into left and right channels. This circuit may utilize the fundamental attenuation scheme of the LM1973 for the level control, but also possess a constant 2dB panning control for the left and right channels as stated earlier.

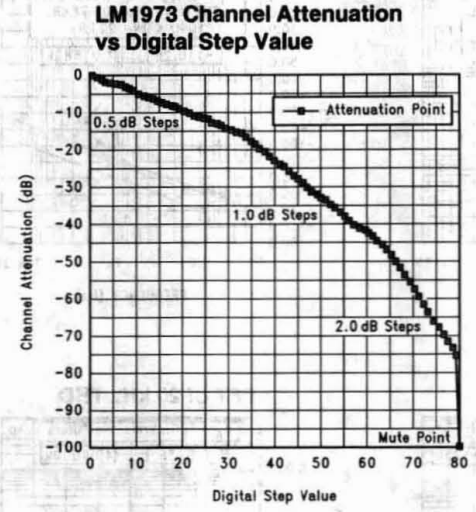


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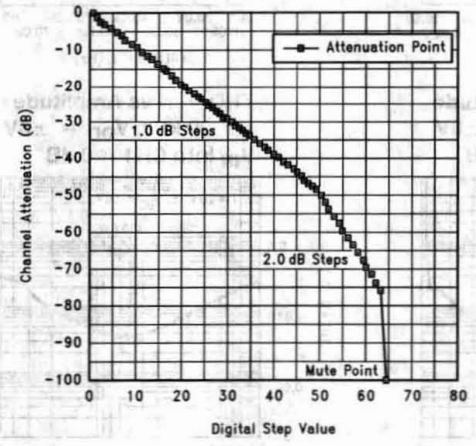
FIGURE 3. LM1973 Attenuation Step Scheme



TL/H/11958–14

FIGURE 4. LM1973 1.0dB and 2.0dB Attenuation Step Scheme

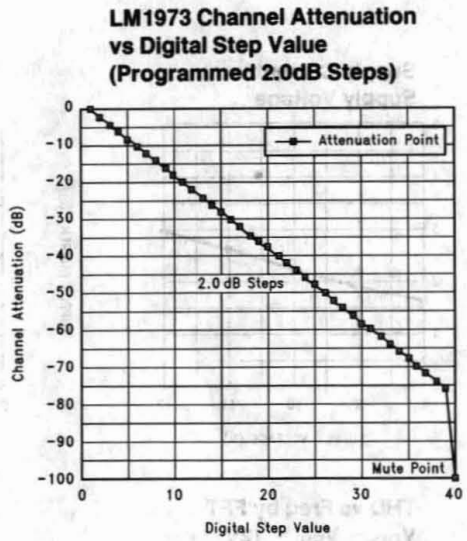


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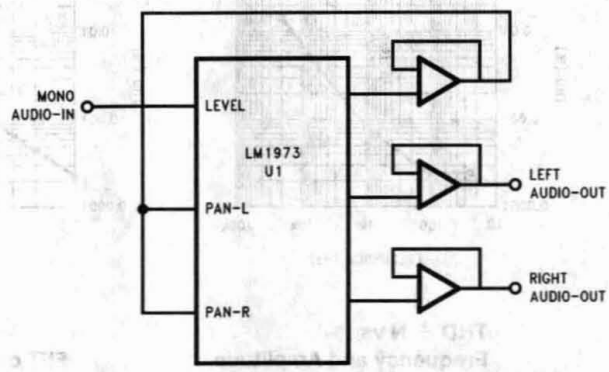
FIGURE 5. LM1973 2.0dB Attenuation Step Scheme



TL/H/11958–8

FIGURE 6. Mono Level Control with Panning Circuit

INPUT IMPEDANCE

The input impedance of a μPot is constant at a nominal 40 kΩ. To eliminate any unwanted DC components from propagating through the device it is common to use 1 μF input coupling caps. This is not necessary, however, if the dc offset from the previous stage is negligible. For higher performance systems, input coupling caps are preferred.

OUTPUT IMPEDANCE

The output of a μPot varies typically between 25 kΩ and 35 kΩ and changes nonlinearly with step changes. Since a μPot is made up of a resistor ladder network with a logarithmic attenuation, the output impedance is nonlinear. Due to this configuration, a μPot cannot be considered as a linear potentiometer, but can be considered only as a logarithmic attenuator.

It should be noted that the linearity of a μPot cannot be measured directly without a buffer because the input impedance of most measurement systems is not high enough to provide the required accuracy. Due to the low impedance of the measurement system, the output of the μPot would be loaded down and an incorrect reading will result. To prevent loading from occurring, a JFET input op amp should be used as the buffer/amplifier. The performance of a μPot is limited only by the performance of the external buffer/amplifier.

Application Information (Continued)

MUTE FUNCTION

One major feature of a μPot is its ability to mute the input signal to an attenuation level of 104dB as shown in *Figure 3.* This is accomplished internally by physically isolating the output from the input while also grounding the output pin through approximately 2 kΩ.

The mute function is obtained during power-up of the device or by sending any binary data of 01001111 and above (to 11111111) serially to the device. The device may be placed into mute from a previous attenuation setting by sending any of the above data. This allows the designer to place a mute button onto his system which could cause a microcontroller to send the appropriate data to a μPot and thus mute any or all channels. Since this function is achieved through software, the designer has a great amount of flexibility in configuring the system.

DC INPUTS

Although the μPot was designed to be used as an attenuator for signals within the audio spectrum, the device is capable of tracking an input DC voltage. The device will track DC voltages to a diode drop above each supply rail.

One point to remember about DC tracking is that with a buffer at the output of the μPot, the resolution of DC tracking will depend upon the gain configuration of that output buffer and its supply voltage. It should also be remembered that the output buffer's supply voltage does not have to be the same as the μPot's supply voltage. This could allow for more resolution when DC tracking.

SERIAL DATA FORMAT

The LM1973 uses a 3-wire serial communication format that is easily controlled by a microcontroller. The timing for the 3-wire set, comprised of DATA-IN, CLOCK, and LOAD/SHIFT is shown in *Figure 2. Figure 8* exhibits in block diagram form how the digital interface controls the tap switches which select the appropriate attenuation level. As depicted in *Figure 2,* the LOAD/SHIFT line is to go low at least 150 ns before the rising edge of the first clock pulse and is to remain low throughout the transmission of each set of 16 data bits. The serial data is comprised of 8 bits for channel selection and 8 bits for attenuation setting. For both address data and attenuation setting data, the MSB is sent first and the 8 bits of address data are to be sent before the 8 bits of attenuation data. Please refer to *Figure 7* to confirm the serial data format transfer process.

TABLE I. LM1973 Micropot Attenuator Register Set Description

MSB LSB	
Address Register (Byte 0)	
0000 0000	Channel 1
0000 0001	Channel 2
0000 0010	Channel 3
Data Register (Byte 1)	
Contents	**Attenuation Level dB**
0000 0000	0.0
0000 0001	0.5
0000 0010	1.0
0000 0011	1.5
:::::	::
0001 1110	15.0
0001 1111	15.5
0010 0000	16.0
0010 0001	17.0
0010 0010	18.0
:::::	::
0011 1110	46.0
0011 1111	47.0
0100 0000	48.0
0100 0001	50.0
0100 0010	52.0
:::::	::
0100 1100	72.0
0100 1101	74.0
0100 1110	76.0
0100 1111	100.0 (Mute)
0101 0000	100.0 (Mute)
:::::	::
1111 1110	100.0 (Mute)
1111 1111	100.0 (Mute)

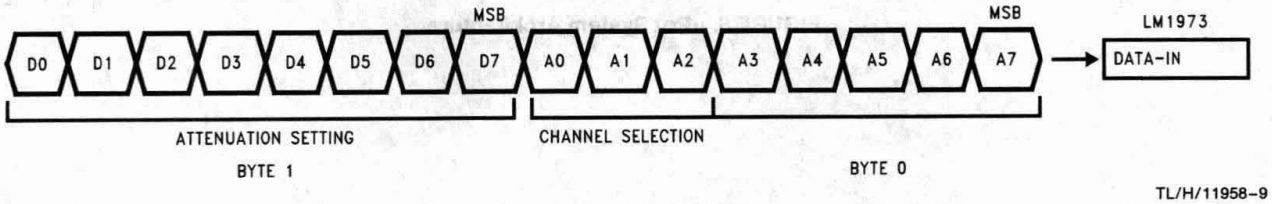


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FIGURE 7. Serial Data Format Transfer Process

Application Information (Continued)

μPot SYSTEM ARCHITECTURE

The μPot's digital interface is essentially a shift register, where serial data is shifted in, latched, and then decoded. As new data is shifted into the DATA-IN pin, the previously latched data is shifted out the DATA-OUT pin. Once the data is shifted in, the LOAD/SHIFT line goes high, latching in the new data. The data is then decoded and the appropriate switch is activated to set the desired attenuation level for the selected channel. This process is continued each and every time an attenuation change is made. Each channel is updated, only, when that channel is selected for an attenuator change or the system is powered down and then back up again. When the μPot is powered up, each channel is placed into the muted mode.

μPot LADDER ARCHITECTURE

Each channel of a μPot has its own independent resistor ladder network. As shown in *Figure 9,* the ladder consists of multiple R1/R2 elements which make up the attenuation scheme. Within each element there are tap switches that select the appropriate attenuation level corresponding to the data bits in Table I. It can be seen in *Figure 9* that the input impedance for the channel is a constant value regardless of which tap switch is selected, while the output impedance varies according to the tap switch selected.

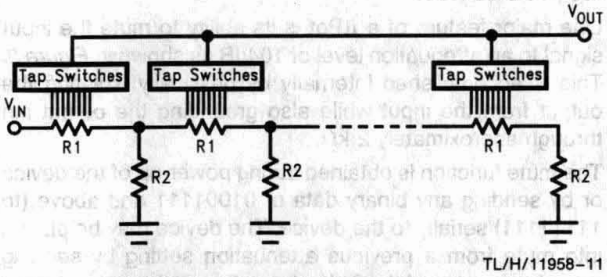

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FIGURE 9. μPot Ladder Architecture

DIGITAL LINE COMPATIBILITY

The μPot's digital interface section is compatible with either TTL or CMOS logic due to the shift register inputs acting upon a threshold voltage of 2 diode drops or approximately 1.4V.

DIGITAL DATA-OUT PIN

The DATA-OUT pin is available for daisy-chain system configurations where multiple μPots will be used. The use of the daisy-chain configuration allows the system designer to use only one DATA and one LOAD/SHIFT line per chain, thus simplifying PCB trace layouts.

In order to provide the highest level of channel separation and isolate any of the signal lines from digital noise, the DATA-OUT pin should be terminated through a 2 kΩ resistor if not used. The pin may be left floating, however, any signal noise on that line may couple to adjacent lines creating higher noise specs.

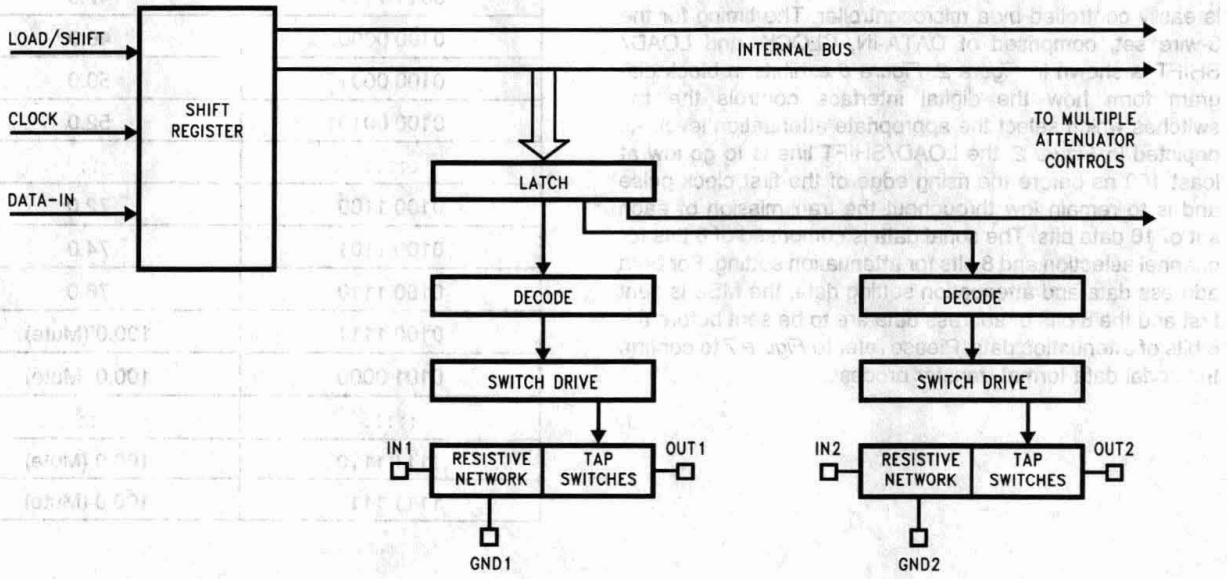

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FIGURE 8. μPot System Architecture

Application Information (Continued)

DAISY-CHAIN CAPABILITY

Since the μPot's digital interface is essentially a shift register, multiple μPots can be programmed utilizing the same data and load/shift lines. As shown in *Figure 10,* for an n-μPot daisy-chain, there are 16n bits to be shifted and loaded for the chain. The data loading sequence is the same for n-μPots as it is for one μPot. First the LOAD/SHIFT line goes low, then the data is clocked in sequentially while the preceding data in each μPot is shifted out the DATA-OUT pin to the next μPot in the chain or to ground if it is the last μPot in the chain. Then the LOAD/SHIFT line goes high; latching the data into each of their corresponding μPots. The data is then decoded according to the address (channel selection) and the appropriate tap switch controlling the attenuation level is selected.

CROSSTALK MEASUREMENTS

The crosstalk of a μPot as shown in the **Typical Performance Characteristics** section was obtained by placing a signal on one channel and measuring the level at the output of another channel of the same frequency. It is important to be sure that the signal level being measured is of the same frequency such that a true indication of crosstalk may be obtained. Also, to ensure an accurate measurement, the measured channel's input should be AC grounded through a 1 μF capacitor.

CLICKS AND POPS

So, why is that output buffer needed anyway? There are three answers to this question, all of which are important from a system point of view.

The first reason to utilize a buffer/amplifier at the output of a μPot is to ensure that there are no audible clicks or pops due to attenuation step changes in the device. If an on-board bipolar op amp had been used for the output stage, its requirement of a finite amount of DC bias current for operation would cause a DC voltage "pop" when the output impedance of the μPot changes. Again, this phenomenon is due to the fact that the output impedance of the μPot is changing with step changes and a bipolar amplifier requires a finite amount of DC bias current for its operation. As the impedance changes, so does the DC bias current and thus there is a DC voltage "pop".

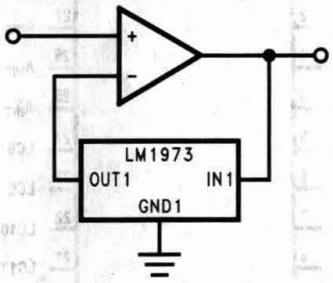
Secondly, the μPot has no drive capability, so any desired gain needs to be accomplished through a buffer/non-inverting amplifer.

Third, the output of a μPot needs to see a high impedance to prevent loading and subsequent linearity errors from ocurring. A JFET input buffer provides a high input impedance to the output of the μPot so that this does not occur.

Clicks and pops can be avoided by using a JFET input buffer/amplifier such as an LF412ACN. The LF412 has a high input impedance and exhibits both a low noise floor and low THD + N throughout the audio spectrum which maintains signal integrity and linearity for the system. The performance of the system solution is entirely dependent upon the quality and performance of the JFET input buffer/amplifier.

LOGARITHMIC GAIN AMPLIFIER

The μPot is capable of being used in the feedback loop of an amplifier, however, as stated previously, the output of the μPot needs to see a high impedance in order to maintain its high performance and linearity. Again, loading the output will change the values of attenuation for the device. As shown in *Figure 11,* a μPot used in the feedback loop creates a logarithmic gain amplifier. In this configuration the attenuation levels from Table I, now become gain levels with the largest possible gain value being 76dB. For most applications 76dB of gain will cause signal clipping to occur, however, because of the μPot's versatility the gain can be controlled through programming such that the clipping level of the system is never obtained. An important point to remember is that when in mute mode the input is disconnected from the output. In this configuration this will place the amplifier in its open loop gain state, thus resulting in severe comparator action. Care should be taken with the programming and design of this type of circuit. To provide the best performance, a JFET input amplifier should be used.



TL/H/11958–13

FIGURE 11. Digitally-Controlled Logarithmic Gain Amplifier Circuit

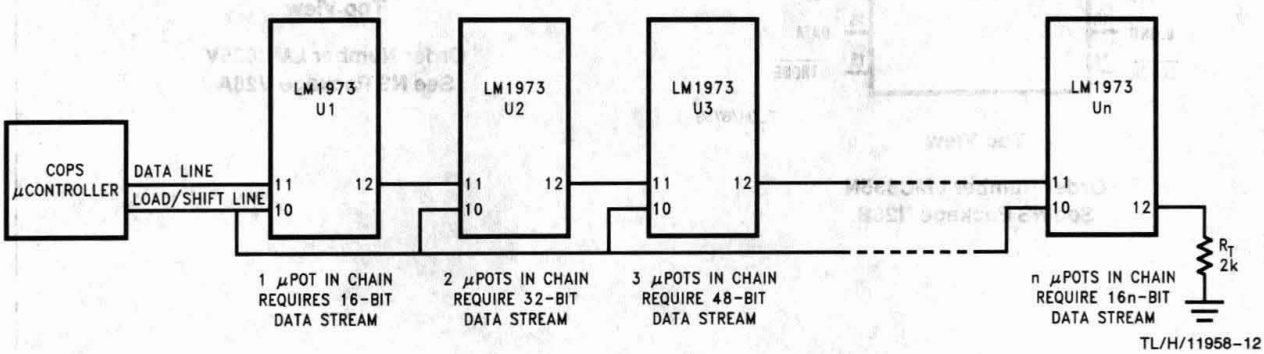


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FIGURE 10. n-μPot Daisy-Chained Circuit

National Semiconductor

LMC835 Digital Controlled Graphic Equalizer

General Description

The LMC835 is a monolithic, digitally-controlled graphic equalizer CMOS LSI for Hi-Fi audio. The LMC835 consists of a Logic section and a Signal Path section made of analog switches and thin-film silicon-chromium resistor networks. The LMC835 is used with external resonator circuits to make a stereo equalizer with seven bands, ±12 dB or ±6 dB gain range and 25 steps each. Only three digital inputs are needed to control the equalization. The LMC835 makes it easy to build a μP-controlled equalizer.

The signal path is designed for very low noise and distortion, resulting in very high performance, compatible with PCM audio.

Features

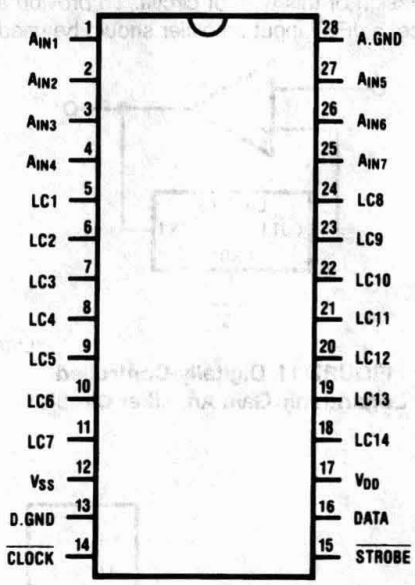
- No volume controls required
- Three-wire interface
- 14 bands, 25 steps each
- ±12 dB or ±6 dB gain ranges
- Low noise and distortion
- TTL, CMOS logic compatible

Applications

- Hi-Fi equalizer
- Receiver
- Car stereo
- Musical instrument
- Tape equalization
- Mixer
- Volume controller

Connection Diagrams

Dual-In-Line Package

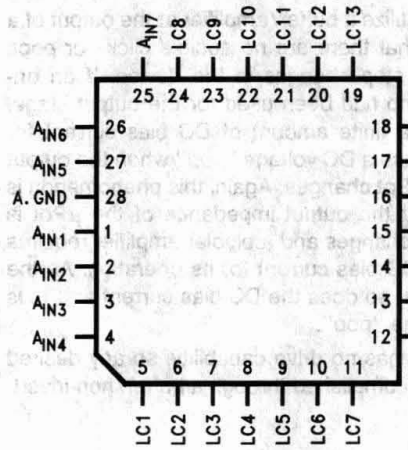


TL/H/6753–1

Top View

Order Number LMC835N
See NS Package N28B

Molded Chip Carrier Package

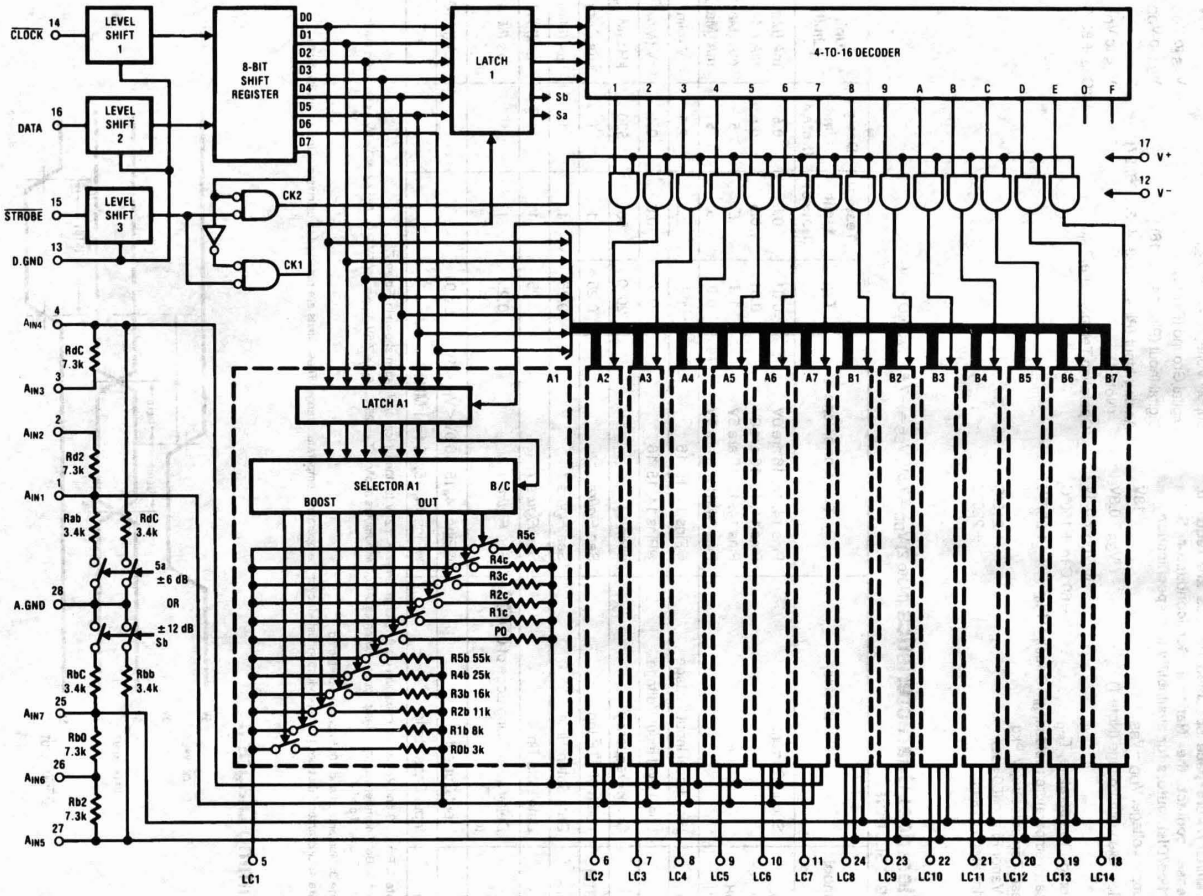


TL/H/6753–26

Top View

Order Number LMC835V
See NS Package V28A

Block Diagram



TL/H/6753–2

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage, $V_{DD}-V_{SS}$	18V
Allowable Input Voltage (Note 1)	$V_{SS}-0.3V$ to $V_{DD}+0.3V$
Storage Temperature, T_{stg}	$-60°C$ to $+150°C$
Lead Temperature (Soldering, 10 sec), N Pkg	$+260°C$
Lead Temperature, V Pkg	
Vapor Phase (60 sec)	$+215°C$
Infrared (15 sec)	$+220°C$

Operating Ratings

Supply Voltage, $V_{DD}-V_{SS}$	5V to 16V
Digital Ground (Pin 13)	V_{SS} to V_{DD}
Digital Input (Pins 14, 15, 16)	V_{SS} to V_{DD}
Analog Input (Pins 1, 2, 3, 4, 25, 26, 27) (Note 1)	V_{SS} to V_{DD}
Operating Temperature, T_{opr}	$-40°C$ to $+85°C$

Electrical Characteristics (Note 2) $V_{DD}=7.5V$, $V_{SS}=-7.5V$, A.GND = 0V

LOGIC SECTION

Symbol	Parameter	Test Conditions	Typ	Tested Limit (Note 3)	Design Limit (Note 4)	Unit (Limit)
I_{DDL}	Supply Current	Pins 14, 15, 16 are 0V	0.01	0.5	**0.5**	mA (Max)
I_{SSL}		Pins 14, 15, 16 are 0V	0.01	0.5	**0.5**	mA (Max)
I_{DDH}		Pins 14, 15, 16 are 5V	1.3	5	**5**	mA (Max)
I_{SSH}		Pins 14, 15, 16 are 5V	0.9	5	**5**	mA (Max)
V_{IH}	High-Level Input Voltage	@Pins 14, 15, 16	1.8	2.3	**2.5**	V (Min)
V_{IL}	Low-Level Input Voltage	@Pins 14, 15, 16	0.9	0.6	**0.4**	V (Max)
f_o	Clock Frequency	@Pin 14	2000	500	**500**	kHz (Max)
$t_{w(\overline{STB})}$	Width of $\overline{STB}$ Input	See *Figure 1*	0.25	1	**1**	μs (Min)
t_{setup}	Data Setup Time	See *Figure 1*	0.25	1	**1**	μs (Min)
t_{hold}	Data Hold Time	See *Figure 1*	0.25	1	**1**	μs (Min)
t_{cs}	Delay from Rising Edge of $\overline{CLOCK}$ to $\overline{STB}$	See *Figure 1*	0.25	1	**1**	μs (Min)
I_{IN}	Input Current	@Pins 14, 15, 16 $0V<V_{IN}<5V$	±0.01	±1		μA (Max)
C_{IN}	Input Capacitance	@Pins 14, 15, 16 f = 1 MHz	5			pF

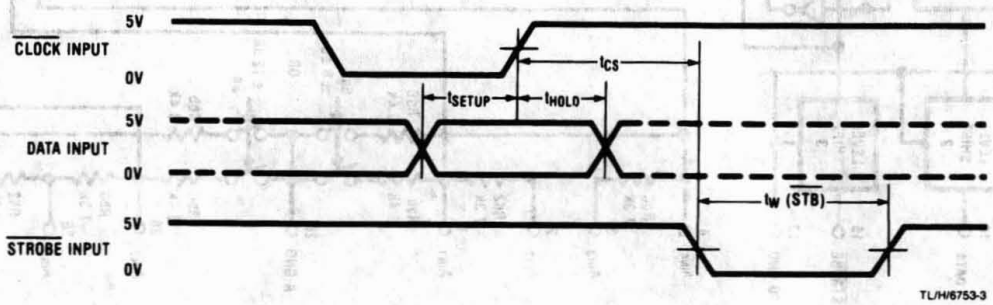
Note 1: Pins 2, 3 and 26 have a maximum input voltage range of ±22V for the typical application shown in *Figure 7*.

Note 2: Bold numbers apply at temperature extremes. All other numbers apply at $T_A=25°C$, $V_{DD}=7.5V$, $V_{SS}=-7.5V$, D.GND = A.GND = 0V as shown in the test circuit, *Figures 3* and *4*.

Note 3: Guaranteed and 100% production tested.

Note 4: Guaranteed (but not 100% production tested) over the operating temperature range. These limits are not used to calculate outgoing quality levels.

Timing Diagram



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Note: To change the gain of the presently selected band, it is not necessary to send DATA 1 (Band Selection) each time.

FIGURE 1

Electrical Characteristics (Note 2) $V_{DD} = 7.5V$, $V_{SS} = -7.5V$, D.GND = A.GND = 0V

SIGNAL PATH SECTION

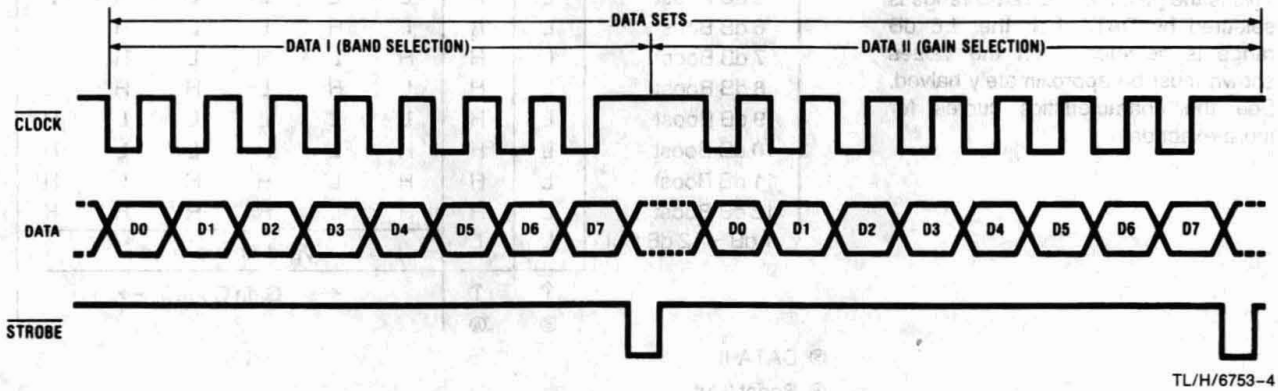
Symbol	Parameter	Test Conditions	Typ	Tested Limit (Note 3)	Design Limit (Note 4)	Unit (Limit)
E_A	Gain Error	$A_V = 0$ dB @ ± 12 dB Range	0.1	0.5	**0.5**	dB (Max)
		$A_V = 0$ dB @ ± 6 dB Range	0.1	1	**1**	dB (Max)
		$A_V = \pm 1$ dB @ ± dB Range (R_{5b} or R_{5c} is ON)	0.1	0.5	**0.6**	dB (Max)
		$A_V = \pm 2$ dB @ ± 12 dB Range (R_{4b} or R_{4c} is ON)	0.1	0.5	**0.6**	dB (Max)
		$A_V = \pm 3$ dB @ ± 12 dB Range (R_{3b} or R_{3c} is ON)	0.1	0.5	**0.6**	dB (Max)
		$A_V = \pm 4$ dB @ ± 12 dB Range (R_{2b} or R_{2c} is ON)	0.1	0.5	**0.7**	dB (Max)
		$A_V = \pm 5$ dB @ ± 12 dB Range (R_{1b} or R_{1c} is ON)	0.1	0.5	**0.7**	dB (Max)
		$A_V = \pm 9$ dB @ ± 12 dB Range (R_{0b} or R_{0c} is ON)	0.2	1	**1.3**	dB (Max)
THD	Total Harmonic Distortion	$A_V = 0$ dB @ ± 12 dB Range $V_{IN} = 4V_{rms}$, f = 1 kHz	0.0015			%
		$A_V = 12$ dB @ ± 12 dB Range				
		$V_{IN} = 1V_{rms}$, f = 1 kHz	0.01	0.1		% (Max)
		$V_{IN} = 1V_{rms}$, f = 20 kHz	0.1	0.5		% (Max)
		$A_V = -12$ dB @ ± 12 dB Range				
		$V_{IN} = 4V_{rms}$, f = 1 kHz	0.01	0.1		% (Max)
		$V_{IN} = 4V_{rms}$, f = 20 kHz	0.1	0.5		% (Max)
$V_{O\ Max}$	Maximum Output Voltage	$A_V = 0$ dB @ ± 12 dB Range THD < 1%, f = 1 kHz	5.5	5.1	**5**	V_{rms} (Min)
S/N	Signal to Noise Ratio	$A_V = 0$ dB @ ± 12 dB Range $V_{ref} = 1\ V_{rms}$	114			dB
		$A_V = 12$ dB @ ± 12 dB Range $V_{ref} = 1V_{rms}$	106			dB
		$A_V = -12$ dB @ ± 12 dB Range $V_{ref} = 1V_{rms}$	116			dB
I_{LEAK}	Leakage Current	$A_V = 0$ dB @ ± 12 dB Range (All internal switches are OFF)				
		Pin 2 + 3, Pin 26		500		nA (Max)
		Pin 5 ~ Pin 11, Pin 18 ~ Pin 24		50		nA (Max)

Note 2; Boldface numbers apply at temperature extremes. All other numbers apply at $T_A = 25°C$, $V_{DD} = 7.5V$, $V_{SS} = -7.5V$, D.GND = A.GND = 0V as shown in the test circuit, *Figures 3* and *4*.

Note 3: Guaranteed and 100% production tested.

Note 4: Guaranteed (but not 100% production tested) over the operating temperature range. These limits are not used to calculate outgoing quality levels.

Timing Diagrams



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Note: To change the gain of the presently selected band, it is not necessary to send DATA 1 (Band Selection) each time.

FIGURE 2

Truth Tables

DATA I (Band Selection)

D7	D6	D5	D4	D3	D2	D1	D0	
H	X	L	L	L	L	L	L	Ch A ± 12 dB Range, Ch B ± 12 dB Range, No Band Selection
H	X	L	L	L	L	L	H	Ch A ± 12 dB Range, Ch B ± 12 dB Range, Band 1
H	X	L	L	L	L	H	L	Ch A ± 12 dB Range, Ch B ± 12 dB Range, Band 2
H	X	L	L	L	L	H	H	Ch A ± 12 dB Range, Ch B ± 12 dB Range, Band 3
H	X	L	L	L	H	L	L	Ch A ± 12 dB Range, Ch B ± 12 dB Range, Band 4
H	X	L	L	L	H	L	H	Ch A ± 12 dB Range, Ch B ± 12 dB Range, Band 5
H	X	L	L	L	H	H	L	Ch A ± 12 dB Range, Ch B ± 12 dB Range, Band 6
H	X	L	L	L	H	H	H	Ch A ± 12 dB Range, Ch B ± 12 dB Range, Band 7
H	X	L	L	H	L	L	L	Ch A ± 12 dB Range, Ch B ± 12 dB Range, Band 8
H	X	L	L	H	L	L	H	Ch A ± 12 dB Range, Ch B ± 12 dB Range, Band 9
H	X	L	L	H	L	H	L	Ch A ± 12 dB Range, Ch B ± 12 dB Range, Band 10
H	X	L	L	H	L	H	H	Ch A ± 12 dB Range, Ch B ± 12 dB Range, Band 11
H	X	L	L	H	H	L	L	Ch A ± 12 dB Range, Ch B ± 12 dB Range, Band 12
H	X	L	L	H	H	L	H	Ch A ± 12 dB Range, Ch B ± 12 dB Range, Band 13
H	X	L	L	H	H	H	L	Ch A ± 12 dB Range, Ch B ± 12 dB Range, Band 14
H	X	L	L	H	H	H	H	Ch A ± 12 dB Range, Ch B ± 12 dB Range, No Band Selection
H	X	L	H	Valid Binary Input				Ch A ± 12 dB Range, Ch B ± 6 dB Range, Band 1 ~ 14
H	X	H	L	Valid Binary Input				Ch A ± 6 dB Range, Ch B ± 12 dB Range, Band 1 ~ 14
H	X	H	H	Valid Binary Input				Ch A ± 6 dB Range, Ch B ± 6 dB Range, Band 1 ~ 14
↑ ①	↑ ②	↑ ③	↑ ④	← Band Code →				

(Ch A: Band 1 ~ 7, Ch B: Band 8 ~ 14)

① DATA 1
② Don't Care
③ Ch A ±6 dB/±12 dB Range
④ Ch B ±6 dB/±12 dB Range

DATA II (Gain Selection)

D7	D6	D5	D4	D3	D2	D1	D0	
L	X	L	L	L	L	L	L	Flat
L	H	H	L	L	L	L	L	1 dB Boost
L	H	L	H	L	L	L	L	2 dB Boost
L	H	L	L	H	L	L	L	3 dB Boost
L	H	L	L	L	H	L	L	4 dB Boost
L	H	L	L	L	L	H	L	5 dB Boost
L	H	L	H	L	L	H	L	6 dB Boost
L	H	H	L	H	L	H	L	7 dB Boost
L	H	L	H	L	H	H	L	8 dB Boost
L	H	L	L	L	L	L	H	9 dB Boost
L	H	H	L	H	L	L	H	10 dB Boost
L	H	H	L	H	H	L	H	11 dB Boost
L	H	H	L	H	H	H	H	12 dB Boost
L	L	Valid Above Input						1 dB ~ 12 dB Cut
↑ ⑤	↑ ⑥	← Gain Code →						

This is the gain if the ±12 dB range is selected by DATA I. If the ±6 dB range is selected, then the values shown must be approximately halved. See the characteristics curves for more exact data.

⑤ DATA II
⑥ Boost/Cut

Test Circuits

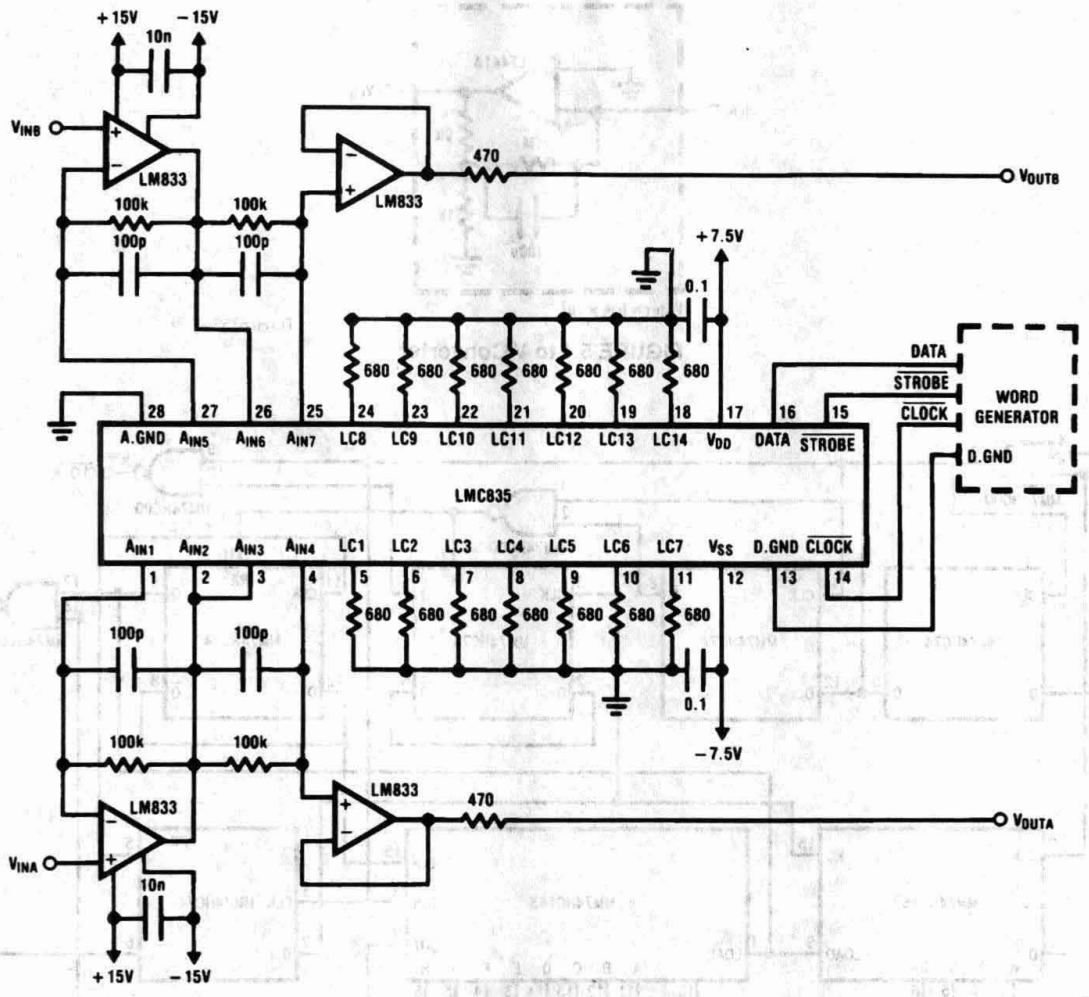

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FIGURE 3. Test Circuit for AC Measurement

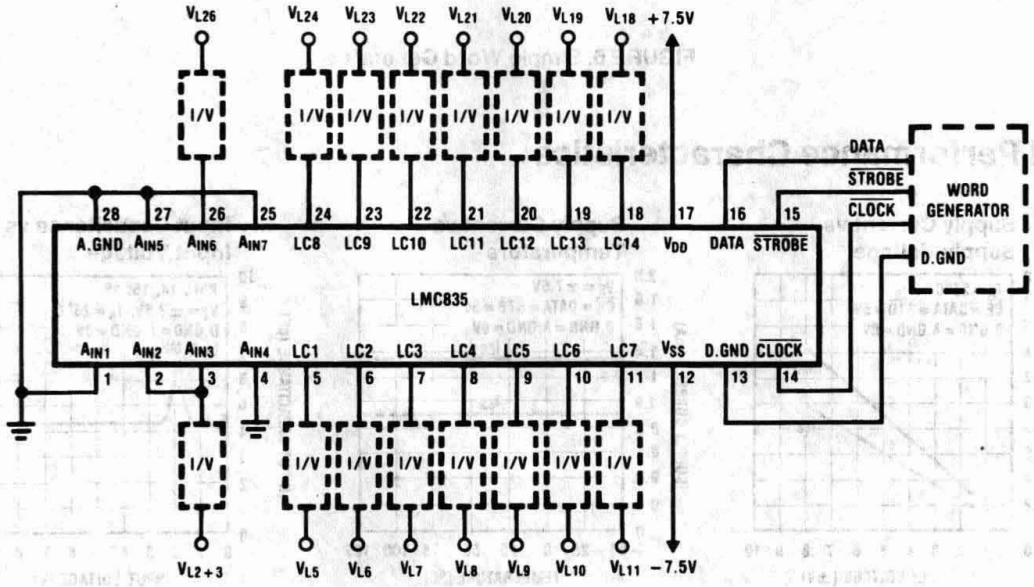
VL26
VL24 VL23 VL22 VL21 VL20 VL19 VL18 +7.5V
I/V
DATA
STROBE
CLOCK
WORD GENERATOR
D.GND
28 27 26 25 24 23 22 21 20 19 18 17 16 15
A.GND AIN5 AIN6 AIN7 LC8 LC9 LC10 LC11 LC12 LC13 LC14 VDD DATA STROBE
LMC835
AIN1 AIN2 AIN3 AIN4 LC1 LC2 LC3 LC4 LC5 LC6 LC7 VSS D.GND CLOCK
1 2 3 4 5 6 7 8 9 10 11 12 13 14
VL2+3
VL5 VL6 VL7 VL8 VL9 VL10 VL11 −7.5V

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FIGURE 4. Test Circuit for Leakage Current Measurement

Test Circuits (Continued)

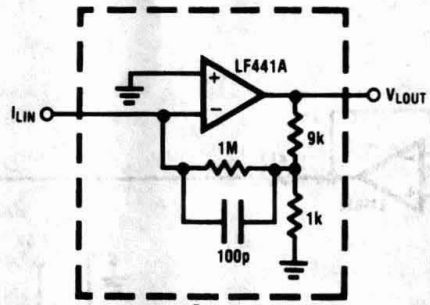

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FIGURE 5. I to V Converter

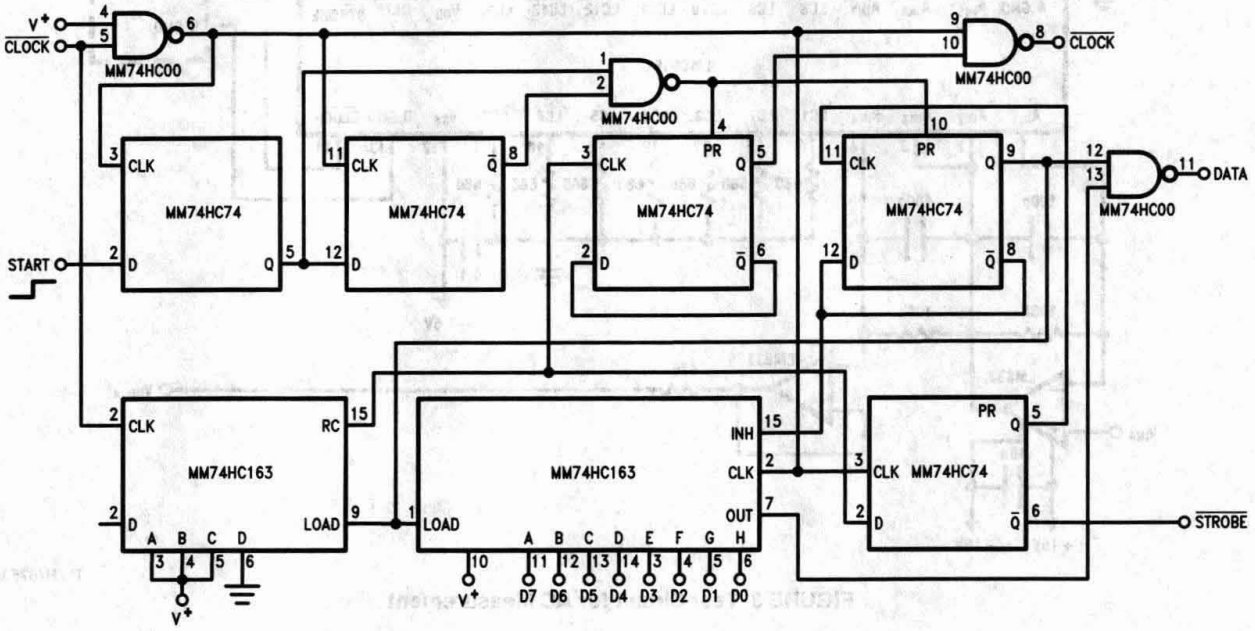

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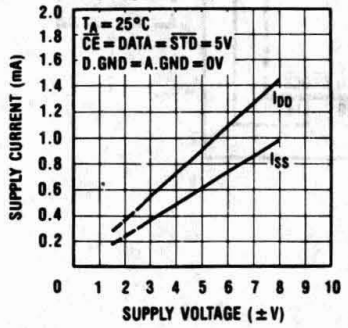
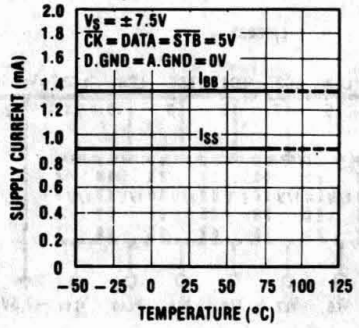
FIGURE 6. Simple Word Generator

Typical Performance Characteristics

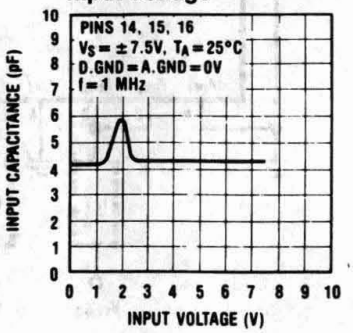
Supply Current vs Supply Voltage



Supply Current vs Temperature



Input Capacitance vs Input Voltage



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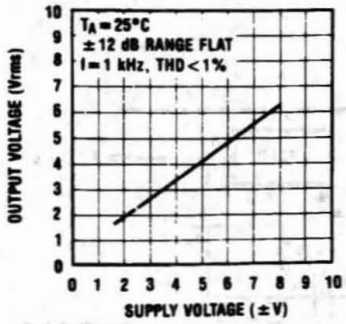
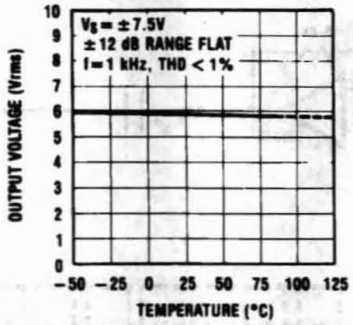
Typical Performance Characteristics (Continued)

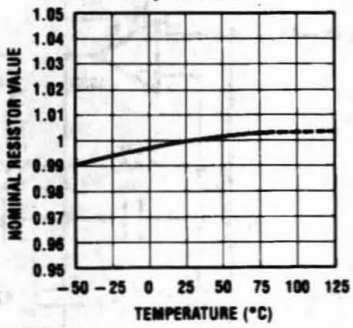
Maximum Output Voltage vs Supply Voltage



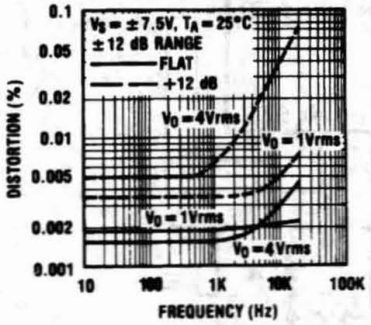
Maximum Output Voltage vs Temperature



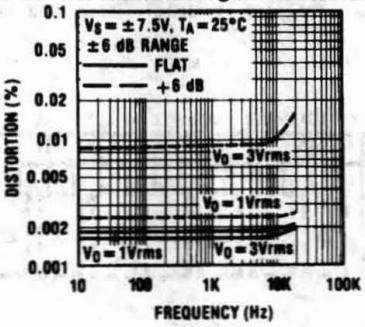
Nominal Resistor vs Temperature



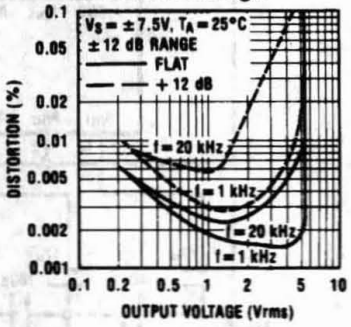
Distortion vs Frequency @ ± 12 dB Range



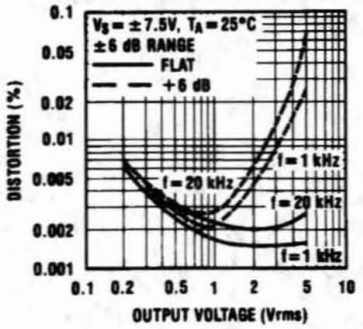
Distortion vs Frequency @ ±6 dB Range



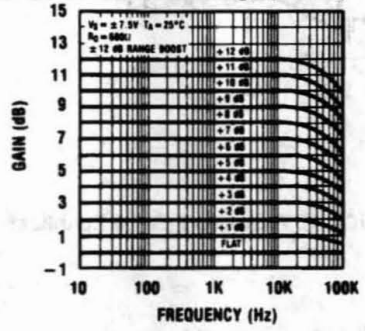
Distortion vs Output Voltage @ ± 12 dB Range



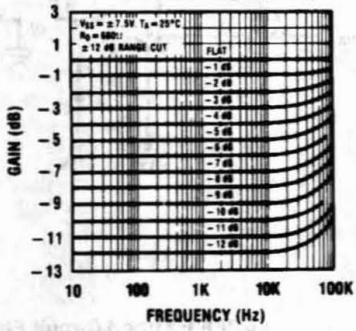
Distortion vs Output Voltage @ ±6 dB Range



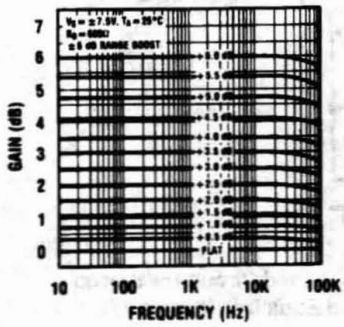
Gain vs Frequency @ ± 12 dB Range (Boost)



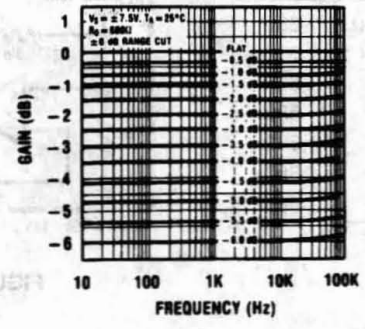
Gain vs Frequency @ ± 12 dB Range (Cut)



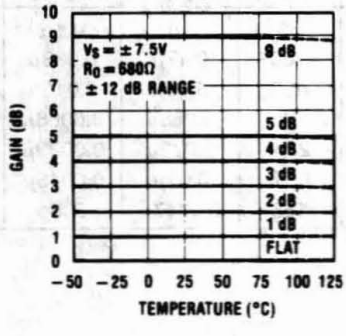
Gain vs Frequency @ ±6 dB Range (Boost)



Gain vs Frequency @ ±6 dB Range (Cut)



Gain vs Temperature



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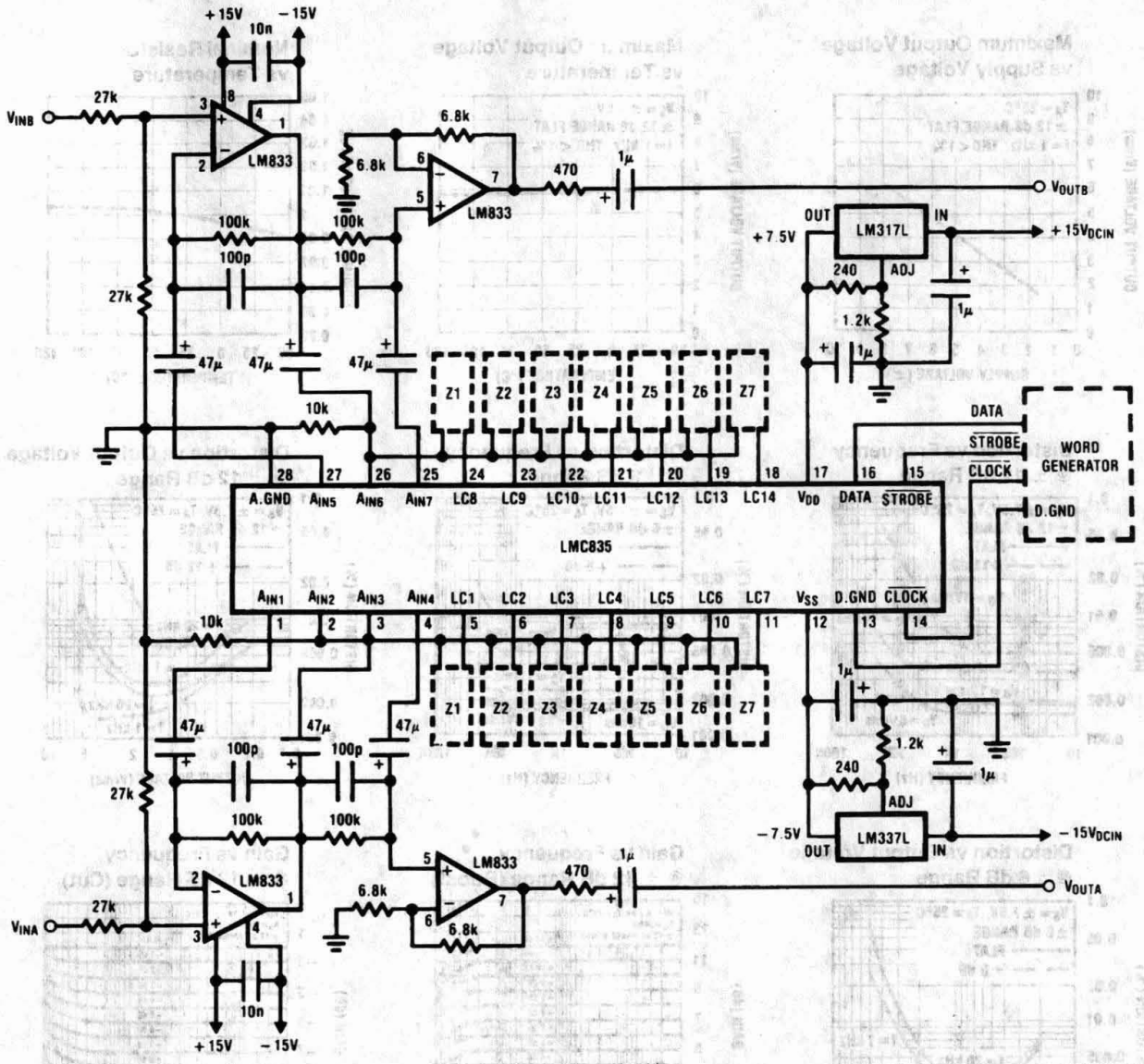
Typical Applications

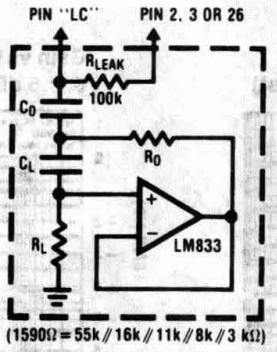


TL/H/6753–11

FIGURE 7. Stereo 7-Band Equalizer

TABLE I: Tuned Circuit Elements

$Q_0 = 3.5$, $Q_{12dB} = 1.05$					
Z1	f_o (Hz)	C_O (F)	C_L (F)	R_L (Ω)	R_O (Ω)
Z1	63	1μ	0.1μ	100k	680
Z2	160	0.47μ	0.033μ	100k	680
Z3	400	0.15μ	0.015μ	100k	680
Z4	1k	0.068μ	0.0068μ	82k	680
Z5	2.5k	0.022μ	0.0033μ	82k	680
Z6	6.3k	0.01μ	0.0015μ	62k	680
Z7	16k	0.0047μ	680p	47k	680



$$L_O = C_L R_L R_O$$

$$f_O = \frac{1}{2\pi\sqrt{L_O C_O}}$$

$$Q_O = \sqrt{\frac{L_O}{C_O R_O^2}}$$

$$Q_{12\,dB} = \frac{R_O Q_O}{R_O + 1590}$$

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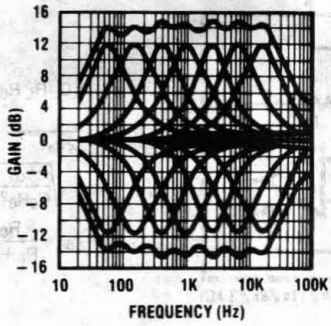
FIGURE 8. Tuned Circuit for Stereo 7-Band Equalizer (*Figure 7*)

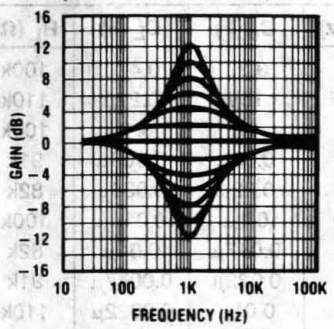
Typical Applications (Continued)

Performance Characteristics (Circuit of *Figure 7*)

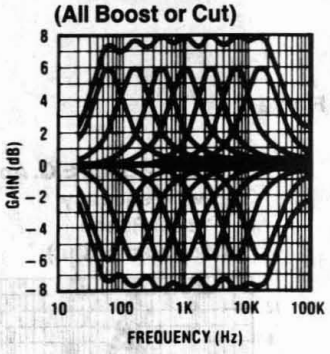
LMC835 Gain vs Frequency @ ± 12 dB Range (All Boost or Cut)



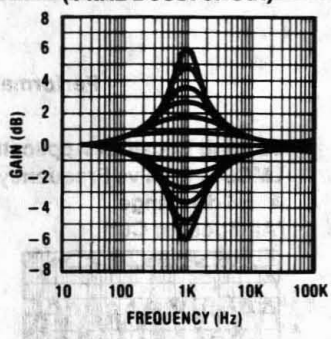
LMC835 Gain vs Frequency @ ± 12 dB Range (1 kHz Boost or Cut)



LMC835 Gain vs Frequency @ ±6 dB Range (All Boost or Cut)



LMC835 Gain vs Frequency @ ±6 dB Range (1 kHz Boost or Cut)



TL/H/6753–13

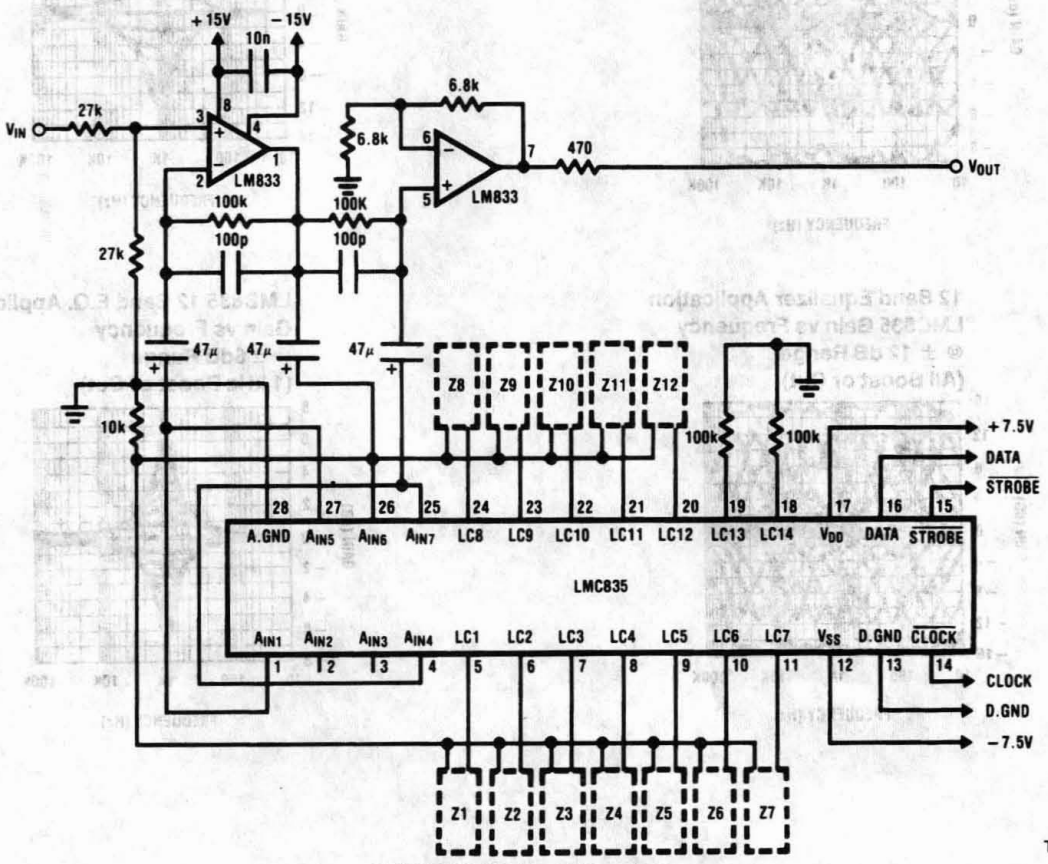


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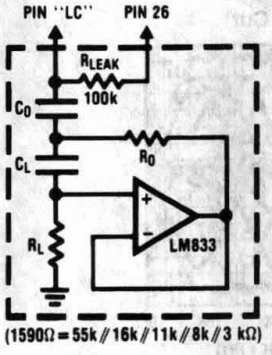
FIGURE 9. 12-Band Equalizer

Typical Applications (Continued)

TABLE II. Tuned Circuit Elements

$Q_0 = 4.7, Q_{12\,dB} = 1.4$					
	f_o (Hz)	C_o (F)	C_L (F)	R_L (Ω)	R_o (Ω)
Z1	16	3.3μ	0.47μ	100k	680
Z2	31.5	15μ	0.22μ	110k	680
Z3	63	1μ	0.1μ	100k	680
Z4	125	0.39μ	0.068μ	91k	680
Z5	250	0.22μ	0.033μ	82k	680
Z6	500	0.1μ	0.015μ	100k	680
Z7	1k	0.047μ	0.01μ	82k	680
Z8	2k	0.022μ	0.0047μ	91k	680
Z9	4k	0.01μ	0.0022μ	110k	680
Z10	8k	0.0068μ	0.001μ	82k	680
Z11	16k	0.0033μ	680p	62k	680
Z12	32k	0.0015μ	470p	68k	510



$$L_O = C_L R_L R_O$$

$$f_O = \frac{1}{2\pi\sqrt{L_O C_O}}$$

$$Q_O = \sqrt{\frac{L_O}{C_O R_O^2}}$$

$$Q_{12\,dB} = \frac{R_O Q_O}{R_O + 1590}$$

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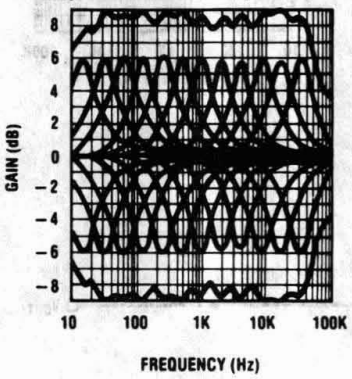
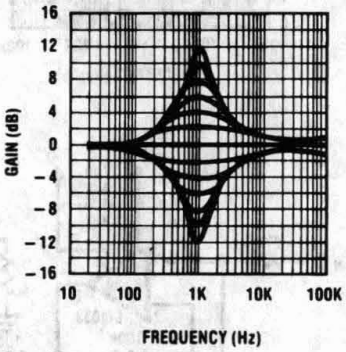
FIGURE 10. Tuned Circuit for 12-Band Equalizer (*Figure 9*)

Performance Characteristics (Circuit of Figure 9)

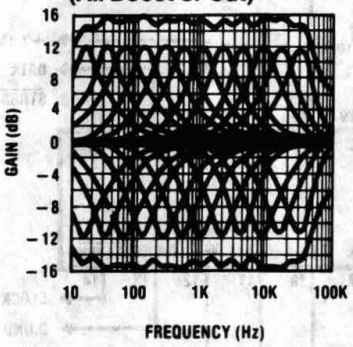
12 Band Equalizer Application
LMC835 Gain vs Frequency
@ ±6 dB Range
(All Boost or Cut)



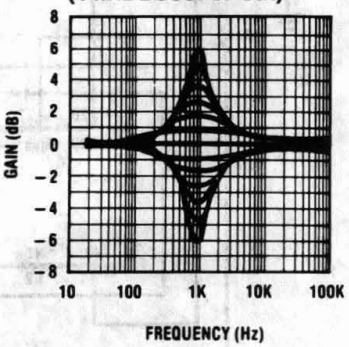
LMC835 12 Band E.Q. Application
Gain vs Frequency
@ ±12 dB Range
(1 kHz Boost or Cut)



12 Band Equalizer Application
LMC835 Gain vs Frequency
@ ± 12 dB Range
(All Boost or Cut)

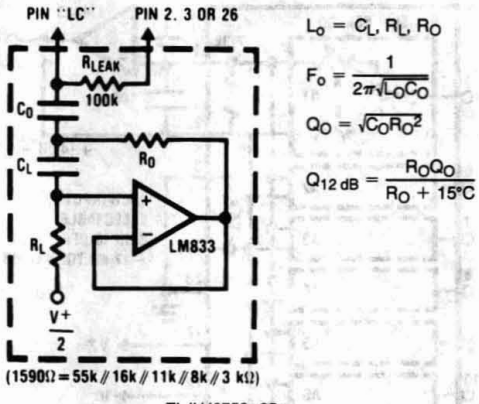


LMC835 12 Band E.Q. Application
Gain vs Frequency
@ ±6dB Range
(1 kHz Boost or Cut)

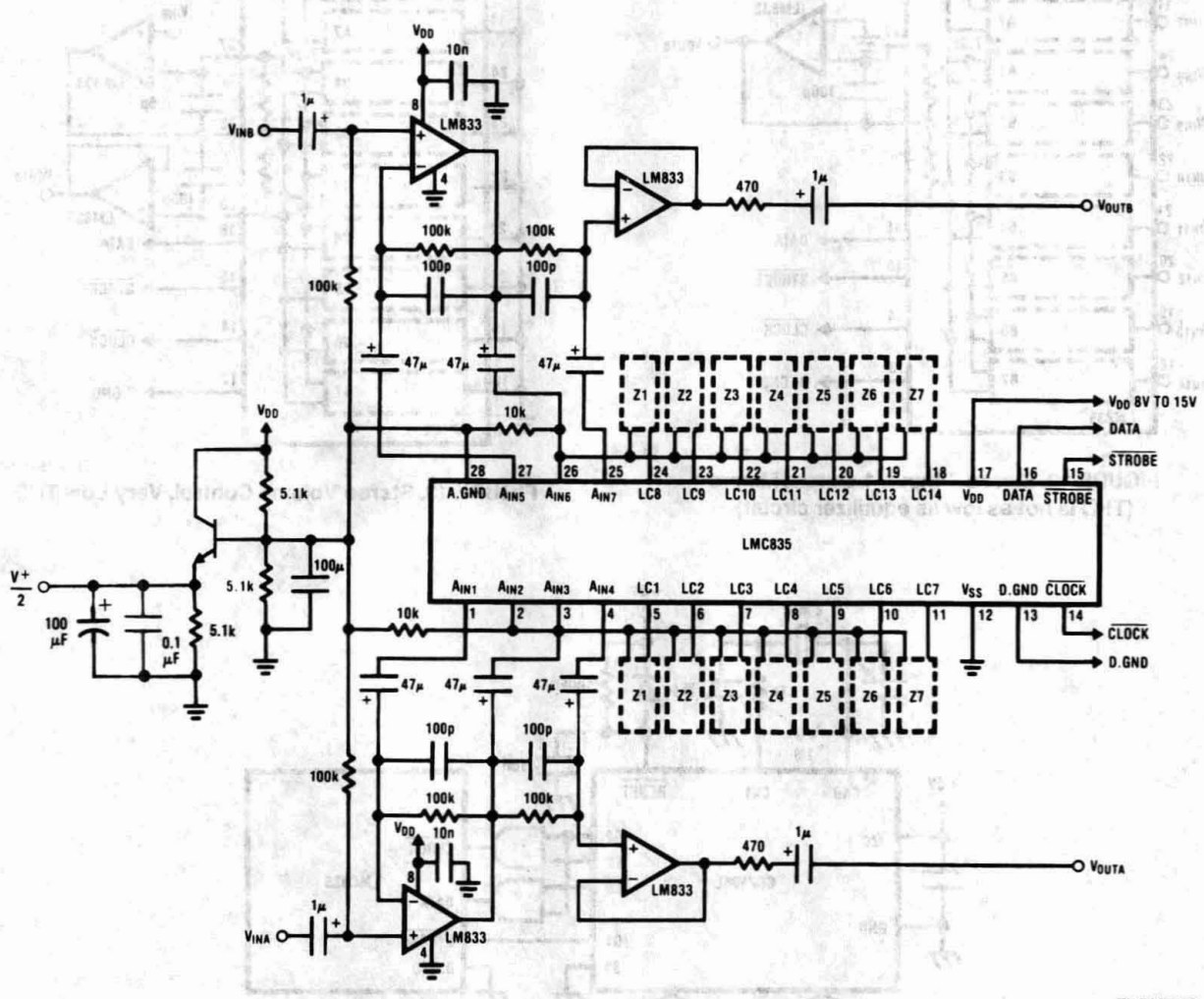


TL/H/6753–16

Typical Applications (Continued)



TL/H/6753–25



TL/H/6753–17

The $\frac{V+}{2}$ output is used to bias the gyrators

FIGURE 11. Single Supply Stereo Equalizer

Typical Applications (Continued)

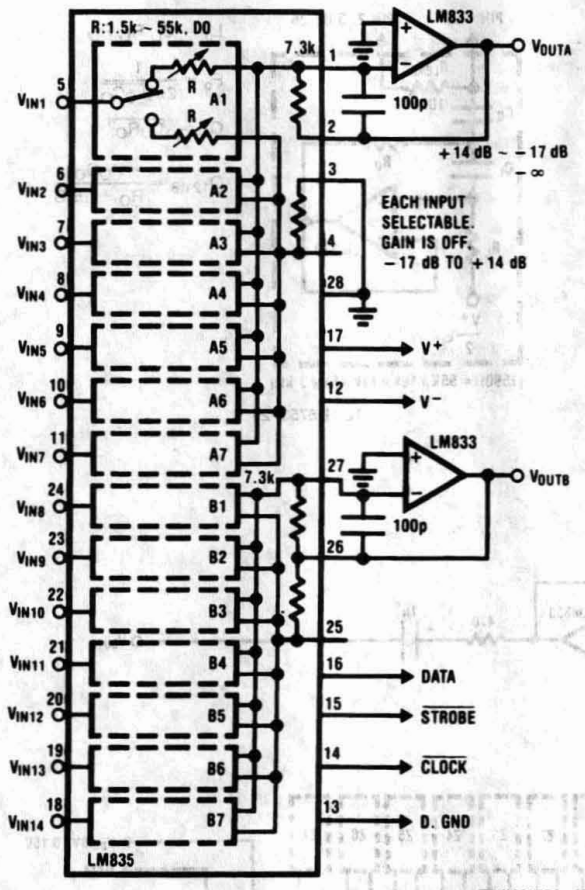


FIGURE 12. Stereo 7-Input/1-Output Mixers (THD is not as low as equalizer circuit)

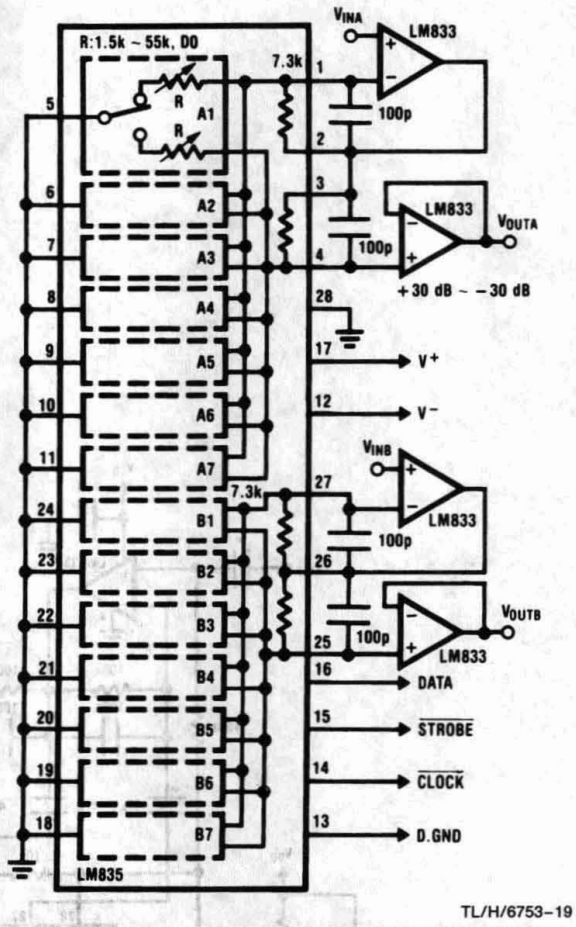


FIGURE 13. Stereo Volume Control, Very Low THD

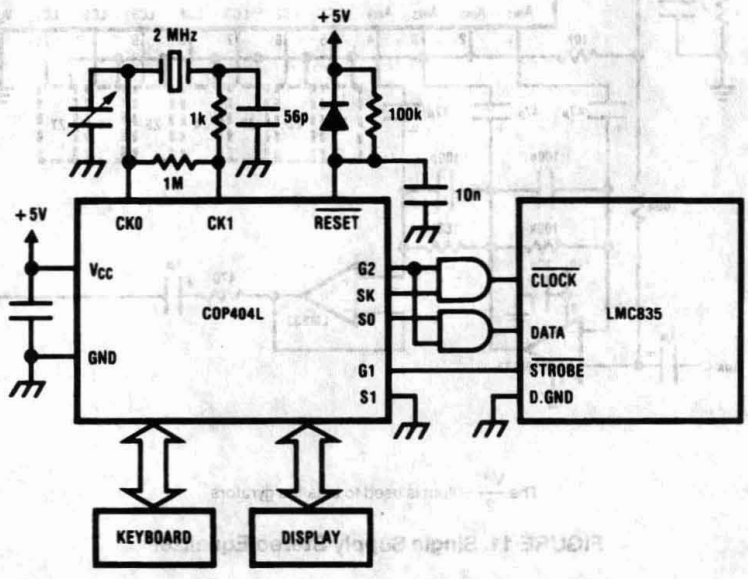


FIGURE 14. LMC835-COP404L CPU Interface

Typical Applications (Continued)

Sample Subroutine Program for *Figure 14*, LMC835-COP404L CPU Interface

```
HEX
CODE    LABEL      MNEMONICS          COMMENTS
3F      LMC835:    LBI      3F        ;POINT TO RAMADDRESS 3F
05      SEND       LD                 ;RAMDATA TO A
22                 SC                 ; SET CARRY
335F               OGI                ;SET PORT G= 1111, OPEN THE AND GATES
4F                 XAS                ;SWAP A AND SIO, CLOCK START
05                 LD                 ;RAMDATA TO A, MAKE SURE A = DATA
07                 XDS                ;SWAP A AND RAMDATA, RAMADDRESS=RAMADDRESS-1
05                 LD                 ;RAMDATA TO A
4F                 XAS                ;SWAP A AND SIO
05                 LD                 ;RAMDATA TO A, MAKE SURE A=NEWDATA
07                 XDS                ;SWAP A AND RAMDATA, RAMADDRESS=RAMADDRESS-1
32                 RC                 ;RESET CARRY
4F                 XAS                ;SWAP A AND SIO, CLOCK STOP
335D               OGJ      13        ;SET PORT G=1101, MAKE STROBE LOW
335B               OGI      11        ;SET PORT G=1011, MAKE STROBE HIGH, CLOSE THE
                                                                        GATES
4E                 CBA                ;BD TO A
43                 AISC     3         ;RAMADDRESS<3C THEN RETURN
48                 RET
80                 JP       SEND
```

RAM ADDRESS	DATA	COMMENTS
3C	DATA	;GAIN DATA D4–D7
3D	DATA	;GAIN DATA D0–D3
3E	DATA	;BAND DATA D4–D7
3F	DATA	;BAND DATA D0–D3

Application Hints

SWITCHING NOISE

The LMC835 uses CMOS analog switches that have small leakages (less than 50 nA). When a band is selected for flat gain, all the switches in that band are open and the resonator circuit is not connected to the LMC835 resistor network. It is only in the flat mode that the small leakage currents can cause problems. The input to the resonator circuit is usually a capacitor and the leakage currents will slowly charge up this capacitor to a large voltage if there is no resistive path to limit it. When the band is set to any value other than flat, the charge on the capacitor will be discharged by the resistor network and there will be a transient at the output. To limit the size of this transient, R_{LEAK} is necessary.

HOW TO AVOID SWITCHING NOISE DUE TO LEAKAGE CURRENT (Refer to *Figures 7* and *8*)

To avoid switching noise due to leakage currents when changing the gain, it is recommended to put R_{LEAK} = 100 kΩ between Pin 3 and Pin 5—11 each, Pin 26 and Pin 12—24 each. The resistor limits the voltage that the capacitor can charge to, with minimal effects on the equalization. The frequency response change due to R_{LEAK} are shown in *Figure 15*. The gain error is only 0.2 dB and Q error is only 5% at 12 dB boost or cut.

SIMPLE WORD GENERATOR *(Figure 6)*

Circuit operation revolves around an MM74HC165 parallel-in/serial-out shift register. Data bits D0 through D7 are applied to the parallel of the MM74HC165 from 8 toggle switches. The bits are shifted out to the DATA input of the LMC835 in sync with the clock. When all data bits have been loaded, CLOCK is inhibited and a STROBE pulse is generated: this sequence is initiated by a START pulse.

LMC835-COP404L CPU INTERFACE (Refer to *Figure 14*)

The diagram shows AND gates between the COP and the LMC835. These permit G2 to inhibit the CLOCK and DATA lines (SK and SO) during a STROBE (G1) pulse. This function may also be implemented in software. As shown in *Figure 2*, the data groups are shifted in D0 first. Data is loaded on positive clock edges.

POWER SUPPLIES

These applications show LM317/337 regulators for the ±7.5V supplies for the LMC835. Since the latter draws only 5 mA max., 1k series dropping resistors from the ±15V op amp supply and a pair of 7.5V zeners and bypass caps will also suffice.

Application Hints (Continued)

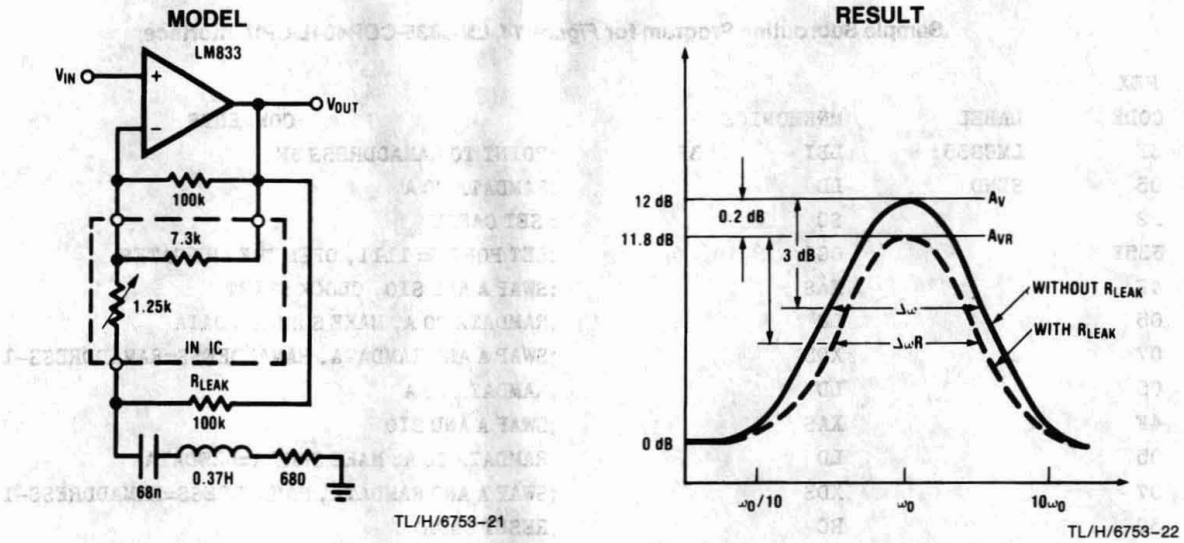


FIGURE 15. Effect of R_{LEAK}

REDUCING EXTERNAL COMPONENTS

The typical application shown in *Figure 7* is switching noise free. The DC-coupled circuit in *Figure 16* is also switching noise free, except at 12 dB/6 dB switch turn ON/OFF. This switching noise is caused by the I_{bias} and V_{offset} of the op amps. Selecting a low I_{bias} and V_{offset} op amp can minimize the switching noise due to the 12 dB/6 dB switch. The DC-coupled application can also eliminate the $R_F = 100k$ resistors with only a 0.5 dB gain error at 12 dB boost or cut.

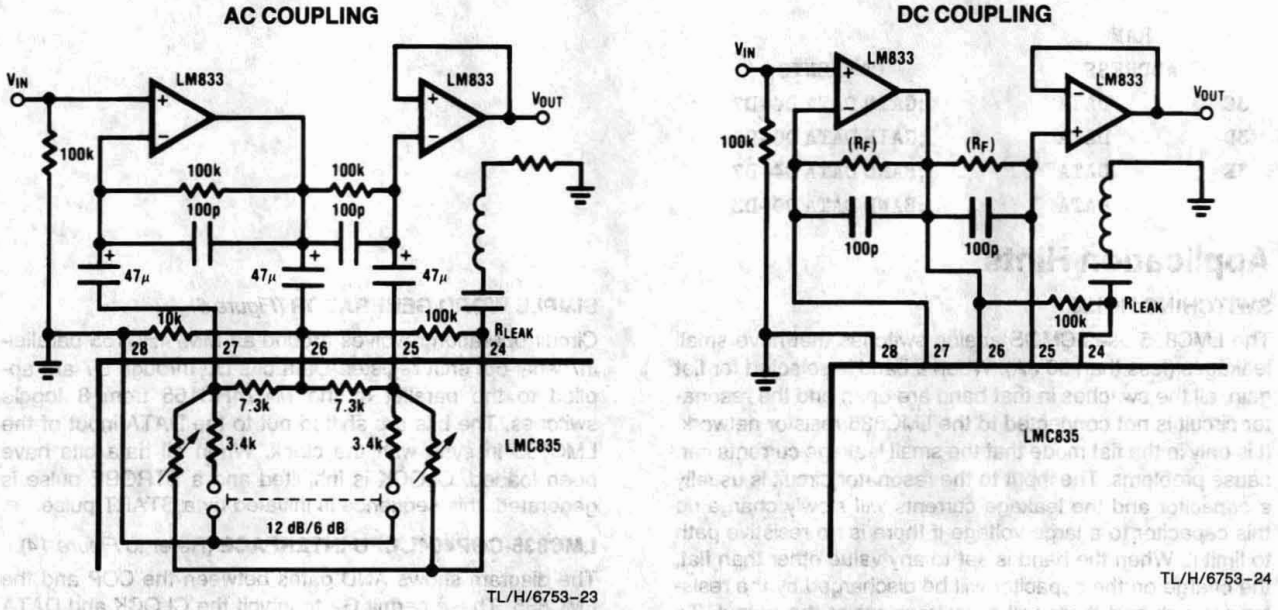


FIGURE 16. Reducing External Components

National Semiconductor

LMC1982
Digitally-Controlled Stereo Tone and Volume Circuit with Two Selectable Stereo Inputs

General Description

The LMC1982 is a monolithic integrated circuit that provides volume, balance, tone (bass and treble), enhanced stereo, and loudness controls and selection between two pairs of stereo inputs. These functions are digitally controlled through a three-wire communication interface. There are two digital inputs for easy interface to other audio peripherals such as stereo decoders. The LMC1982 is designed for line level input signals (300 mV–2V) and has a maximum gain of −0.5 dB. Volume is set at minimum and tone controls are flat when supply voltage is first applied.

Low noise and distortion result from using analog switches and poly-silicon resistor networks in the signal path.

Additional tone control can be achieved using the LMC835 stereo 7-band graphic equalizer connected to the LMC1982's SELECT OUT/SELECT IN external processor loop.

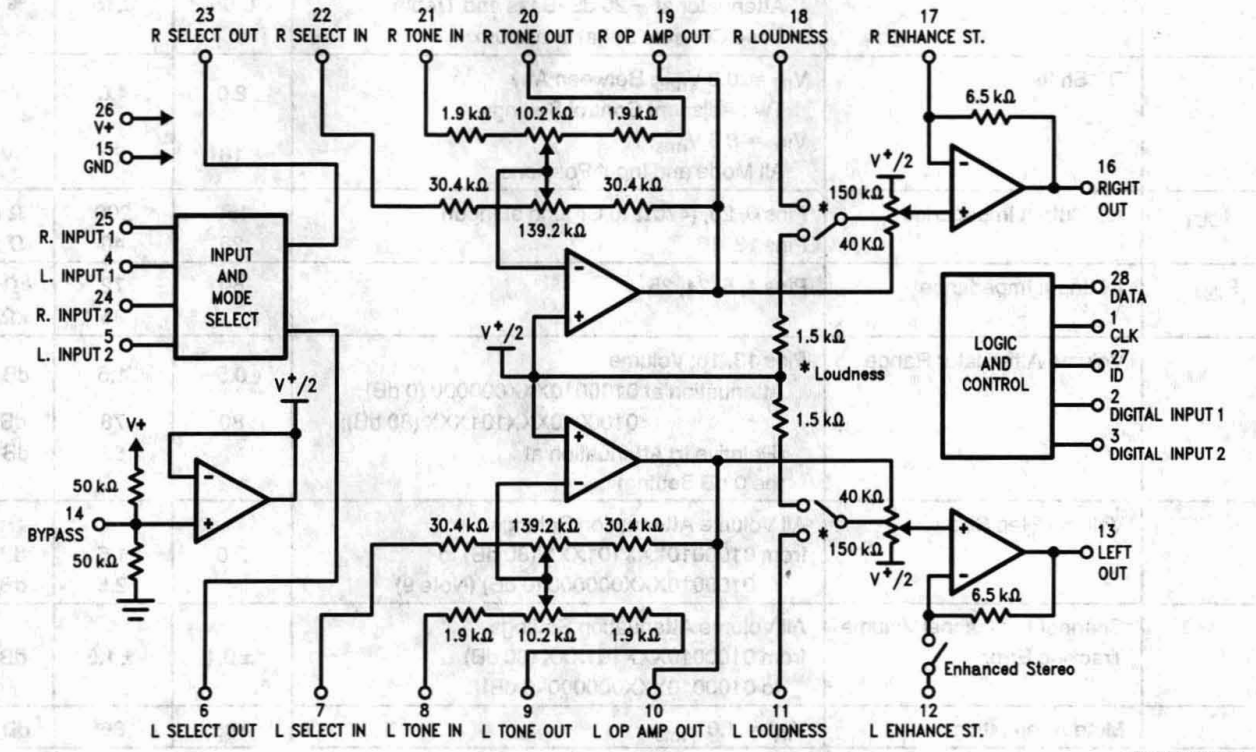
Features

- Low noise and distortion
- Two pairs of stereo inputs
- Enhanced stereo function
- Loudness compensation
- 40 position 2 dB/step volume attenuator plus mute
- Independent left and right volume controls
- Low noise-suitable for use with DNR® and Dolby® noise reduction
- External processor loop
- Signal handling suitable for compact discs
- Pop-free switching
- Serially programmable: INTERMETAL bus (IM) interface
- 6V to 12V single supply operation
- 28 Pin DIP or PLCC package

Applications

- Stereo television
- Music reproduction systems
- Sound reinforcement systems
- Electronic music (MIDI)
- Personal computer audio control

Block and Connection Diagrams



TL/H/11028–1

Absolute Maximum Ratings (Notes 1 and 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage ($V^+ - GND$)	15V
Voltage at any Pin	GND − 0.2V to V^+ + 0.2V
Input Current at any Pin (Note 3)	5 mA
Package Input Current (Note 3)	20 mA
Power Dissipation (Note 4)	500 mW
Junction Temperature	+125°C
Storage Temperature	−65°C to +150°C
Lead Temperature	
N Package, (Soldering, 10 Seconds)	+260°C
V Package, (Vapor Phase, 60 Seconds)	215°C
Infrared, (15 Seconds)	220°C
ESD Susceptability (Note 5)	2 kV

Operating Ratings (Notes 1 and 2)

Temperature Range	$T_{MIN} \le T_A \le T_{MAX}$
LMC1982CIN, LMC1982CIV	$-40°C \le T_A \le +85°C$
Supply Voltage ($V^+ - V^-$)	6V to 12V

Electrical Characteristics

The following specifications apply for $V^+ = 9V$, $f_{IN} = 1$ kHz, input signal (300 mV) applied to INPUT 1, volume = 0 dB, bass = 0 dB, treble = 0 dB, enhanced stereo is off, and loudness is off unless otherwise specified. All limits apply for $T_A = T_J = +25°C$.

Symbol	Parameter	Conditions	Typical (Note 6)	Limit (Note 7)	Unit (Limit)
I_S	Supply Current		15	25	mA (max)
V_{IN}	Input Voltage	Clipping Level (1,.0% THD), Select Out (Pins 6, 23)	2.3	2.0	V_{rms} (min)
THD	Total Harmonic Distortion	Left and Right channels; Output Pins 13, 16			
		V_{IN} = 0.3 V_{rms}; f_{IN} = 100 Hz, 1 kHz, 10 kHz	0.008	0.1	% (max)
		V_{IN} = 2.0 V_{rms}; f_{IN} = 100 Hz, 1 kHz	0.4	1.0	% (max)
		V_{IN} = 2.0 V_{rms}; f_{IN} = 10 kHz	0.5	1.0	% (max)
		V_{IN} = 0.5 V_{rms}; Bass and Treble Tone Controls Set at Maximum	0.07	0.5	% (max)
		V_{IN} = 0.3 V_{rms}; Volume Attenuator at −20 dB, Bass and Treble Tone Controls Set at Maximum	0.06	0.15	% (max)
	DC Shifts	V_{IN} = 0.3 V_{rms}; Between Any Two Adjacent Control Settings	2.0	4.0	mV (max)
		V_{IN} = 0.3 V_{rms}; All Mode and Input Positions	18	20	mV (max)
R_{OUT}	AC Output Impedance	Pins 6, 23, (470Ω to Ground at Input)	150	200	Ω (max)
		Pins 13, 16	26	40	Ω (max)
R_{IN}	AC Input Impedance	Pins 4, 5, 24, 25	50	72	kΩ (max)
				35	kΩ (min)
	Volume Attenuator Range	Pins 13, 16; Volume Attenuation at 0100010XXX000000 (0 dB)	0.5	1.5	dB (max)
		0100010XXX101XXX (80 dB); (Relative to Attenuation at the 0 dB Setting)	80	78	dB (min)
				82	dB (max)
	Volume Step Size	All Volume Attenuation Settings from 0100010XXX101XXX (80 dB) to 0100010XXX000000 (0 dB) (Note 9)	2.0	1.5	dB (min)
				2.5	dB (min)
	Channel-to-Channel Volume Tracking Error	All Volume Attenuation Settings from 0100010XXX101XXX (80 dB) to 0100010XXX000000 (0 dB)	±0.1	±1.5	dB (min)
	Mute Attenuation	V_{IN} = 1.0 V_{rms}	105	86	dB (max)

Electrical Characteristics The following specifications apply for $V^+ = 9V$, $f_{IN} = 1$ kHz, input signal (300 mV) applied to INPUT 1, volume = 0 dB, bass = 0 dB, treble = 0 dB, enhanced stereo is off, and loudness is off unless otherwise specified. All limits apply for $T_A = T_J = +25°C$. (Continued)

Symbol	Parameter	Conditions	Typical (Note 6)	Limit (Note 7)	Unit (Limit)
	Bass Gain Range	f_{IN} = 100 Hz, Pins 13, 16	±12	±10.0 ±14.0	dB (min) dB (max)
	Bass Tracking Error	f_{IN} = 100 Hz, Pins 13, 16	±0.1	±1.5	dB (max)
	Bass Step Size	f_{IN} = 100 Hz, Pins 13, 16 (Relative to Previous Level)	2.0	1.5 2.5	dB (min) dB (max)
	Treble Gain Range	f_{IN} = 10 kHz, Pins 13, 16	±12	±10.0 ±14.0	dB (min) dB (max)
	Treble Tracking Error	f_{IN} = 10 kHz, Pins 13, 16	±0.1	±1.5	dB (max)
	Treble Step Size	f_{IN} = 10 kHz, Pins 13, 16 (Relative to Previous Level)	2.0	1.5 2.5	dB (min) dB (max)
	Enhanced Stereo Cross Coupling	(Note 10)	−4.4	−2.5 −6.9	dB (min) dB (max)
	Frequency Response	V_{IN} Applied to Input 1 and Input 2; f_{IN} = 20 Hz − 20 kHz (Relative to Signal Amplitude at 1 kHz)	±0.1	±1.0	dB (max)
	Loudness	Volume Attenuator = 40 dB, Loudness on (See *Figure 5*) Gain at 100 Hz (Referenced to Gain at 1 kHz) Gain at 10 kHz (Referenced to Gain at 1 kHz)	 11.5 6.5	 13.5 9.5 8.5 4.5	 dB (max) dB (min) dB (max) dB (min)
	Signal-to-Noise Ratio	V_{IN} = 1.0 V_{rms}, A Weighted, Measured at 1 kHz, R_S = 470Ω	95	90	dB (min)
	Channel Balance	All Volume Settings	0.2	1.0	dB (max)
	Channel Separation	Input Pins 4, 25: Output Pins 13, 16; V_{IN} = 1.0 V_{rms} (Note 8)	80	60	dB (min)
	Input-Input Isolation	470Ω to AC Ground on Unused Input	95	60	dB (min)
PSSR	Power Supply Rejection Ratio	V^+ = 9 V_{DC}; 200 mV_{rms}, 100 Hz Sinewave Applied to Pin 26	32	28	dB (min)
f_{CLK}	Clock Frequency		5.0	1.0	MHz (max)
$V_{IN(1)}$	Logic "1" Input Voltage	Pins 1, 27, 28 (IM Bus) Pins 2, 3	1.3 2.9	2.0 5.5	V (min) V (min)
$V_{IN(0)}$	Logic "0" Input Voltage	Pins 1, 27, 28 (IM Bus) Pins 2, 3	0.4 1.2	0.8 3.5	V (max) V (max)
$V_{OUT(1)}$	Logic "1" Output Voltage	Pin 28 (IM Bus)		2.0	V (min)
$V_{OUT(0)}$	Logic "0" Output Voltage	Pin 28 (IM Bus)	0.4	0.8	V (max)

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the deivce may occur. Operating Ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.

Note 2: All voltages are specified with respect to ground.

Note 3: When the input voltage (V_{IN}) at any pin exceeds the power supply voltages ($V_{IN} < V^-$ or $V_{IN} > V^+$) the absolute value of the current at that pin should be limited to 5 mA or less. The 20 mA package input current limits the number of pins that can exceed the power supply voltages with 5 mA current limit to four.

Note 4: The maximum power dissipation must be derated at elevated temperatures and is dictated by T_{JMAX}, θ_{JA}, and the ambient temperature T_A. The maximum allowable power dissipation is $P_D = (T_{JMAX} - T_A)/\theta_{JA}$ or the number given in the Absolute Maximum Ratings, whichever is lower. For the LMC1982CIN, T_{JMAX} = +125°C, and the typical junction-to-ambient thermal resistance, when board mounted, is 67°C/W.

Note 5: Human body model; 100 pF discharged through a 1.5 kΩ resistor.

Note 6: Typicals are at $T_J = +25°C$ and represent the most likely parametric norm.

Note 7: Limits are guaranteed to National's AOQL (Average Outgoing Quality Level).

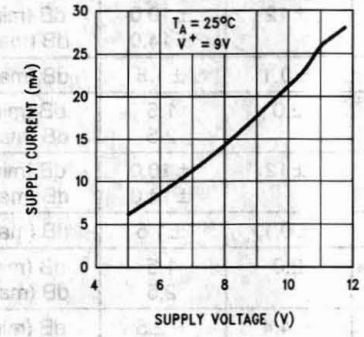
Note 8: The Input-Input Isolation is tested by driving one input and measuring the output when the undriven input are selected.

Note 9: The Volume Step Size is defined as the change in attenuation between any two adjacent volume attenuation settings. The nominal Volume Step Size is 2 dB.

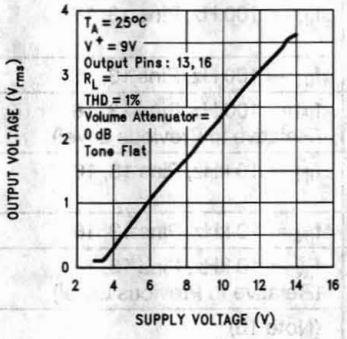
Note 10: Enhanced Stereo Cross Coupling is a measure of the ratio between the undriven right channel output signal and the driven left channel output signal. It is measured by driving the left inputs with a 300 mV_{rms} signal while the right inputs are grounded.

Typical Performance Characteristics

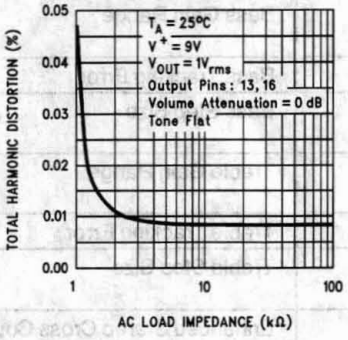
Supply Current vs Supply Voltage



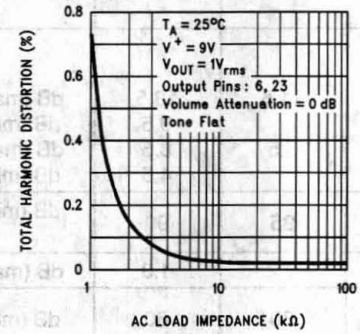
Output Voltage vs Supply Voltage



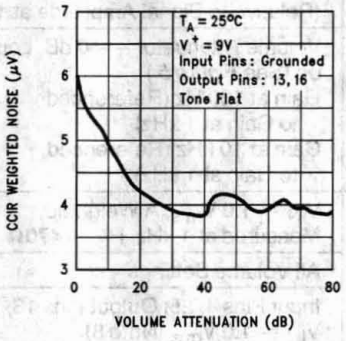
THD vs Load Impedance



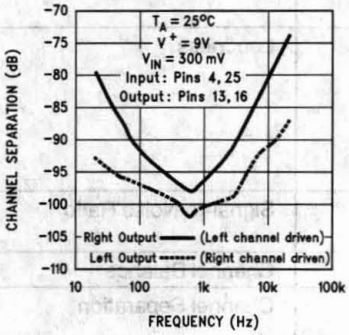
THD vs Load Impedance



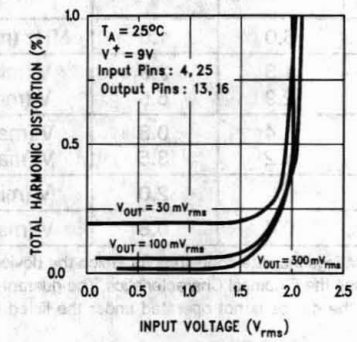
CCIR Output Noise vs Volume Setting



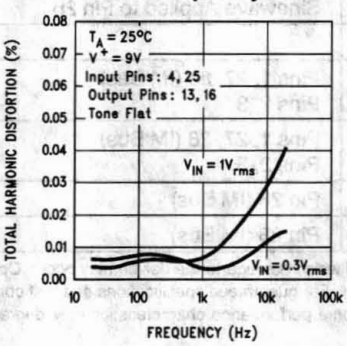
Channel Separation vs Frequency



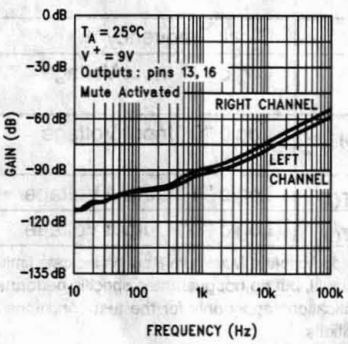
THD vs V_{IN} (V_{OUT} Constant)



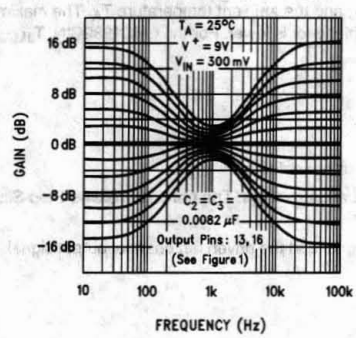
THD vs Frequency



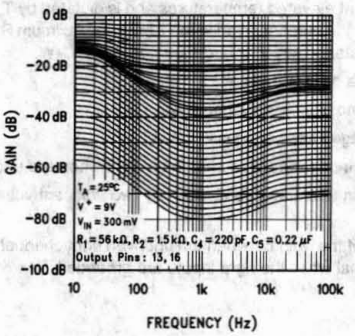
Mute Gain vs Frequency



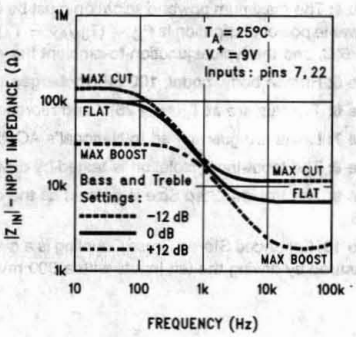
Tone Control Response with Equal Bass and Treble Control Settings



Loudness Response vs Frequency

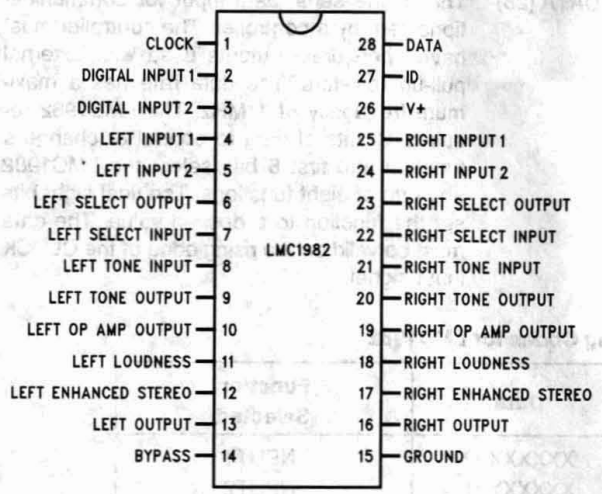


Select Input Impedance vs Frequency



TL/H/11028–3

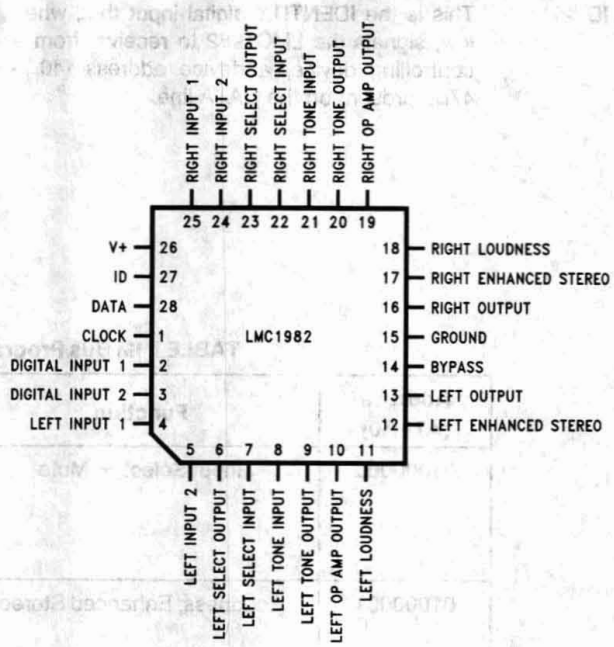
Connection Diagram



TL/H/11028–2

Top View

Order Number LMC1982CIN
See NS Package Number N28B



TL/H/11028–12

Top View

Order Number LMC1982CIV
See NS Package Number V28A

Pin Description

CLK (1) The INTERMETAL (IM) Bus clock is applied to the CLOCK pin. This input accepts a TTL or CMOS level signal. The input is used to clock the DATA signal. A data bit must be valid on the rising clock edge.

DIGITAL INPUT 1 & 2 (2, 3) Internally tied high to V^+ through a 30 kΩ pull-up resistor, these inputs allow a peripheral device to place any single-bit, active low digital information onto the IM Bus. It is then sent out to the controlling device through the DATA pin. Examples of such information could include indication of the presence of a Second Audio Program (SAP) or an FM stereo carrier.

INPUTS 1 & 2 (4, 25; 5, 24) These are the LMC1982's two stereo input pairs.

SELECT OUT (6, 23) The selected INPUT signal is available at this output. This feature allows external signal processors such as noise reduction or graphic equalizers to be used. This output can typically sink 1 mA. These pins should be capacitively coupled to pins 7 and 22, respectively, if no external processor is used.

SELECT IN (7, 22) These are the inputs that an external signal processor uses to return a signal to the LMC1982. These pins should be capacitively coupled to pins 6 and 23, respectively, if no external processor is used.

TONE IN (8, 21) These are the inputs to the tone control amplifier. See the Application Information section titled "Tone Control Response".

TONE OUT (9, 20) Tone control amplifier output. See the Application Information section titled "Tone Control Response".

OP AMP OUT (10, 19) These outputs are used with external tone control capacitors. Internally, this output is applied to the volume attenuators.

LOUDNESS (11, 18) The output signal on these pins is a voltage taken from the volume attenuator's −40 dB tap point. An external R–C network is connected to these pins.

ENHANCED STEREO (12, 17) An external R–C network is connected across these pins. This provides left-right channel cross-coupling and cancellation to create an enhanced stereo channel separation effect.

MAIN OUTPUT (13, 16) The output signal from these pins drives a stereo power amplifier. The output can typically sink 1 mA.

BYPASS (14) A 10 μF capacitor is connected between this pin and ground to provide an AC ground for the internal half-supply voltage reference.

GROUND (15) This pin is connected to analog ground.

V^+ (26) This is the power supply connection. The LMC1982 is operational with supply voltages from 6V to 12V. This pin should be bypassed to ground through a 1.0 μF capacitor.

Pin Description (Continued)

ID (27) This is the IDENTITY digital input that, when low, signals the LMC1982 to receive, from a controlling device, a device address (40_H–47_H), present on the DATA line.

DATA (28) This is the serial data input for communications sent by a controller. The controller must have open drain outputs used with external pull-up resistors. The data rate has a maximum frequency of 1 MHz. The LMC1982 requires 16 bits of data to control or change a function: the first 8 bits select the LMC1982 and one of eight functions. The final eight bits set the function to a desired value. The data must be valid on the rising edge of the CLOCK input signal.

TABLE I. IM Bus Programming Codes for LMC1982

Address (A7–A0)	Function	Data	Function Selected
01000000	Input Select + Mute	XXXXXX00	INPUT1
		XXXXXX01	INPUT2
		XXXXXX10	N/A
		XXXXXX11	MUTE
01000001	Loudness, Enhanced Stereo	XXXXXX00	Loudness OFF Enhanced Stereo OFF
		XXXXXX01	Loudness ON Enhanced Stereo OFF
		XXXXXX10	Loudness OFF Enhanced Stereo ON
		XXXXXX11	Loudness ON Enhanced Stereo ON
01000010	Bass	XXXX0000	−12 dB
		XXXX0011	−6 dB
		XXXX0110	FLAT
		XXXX1001	+6 dB
		XXXX11XX	+12 dB
01000011	Treble	XXXX0000	−12 dB
		XXXX0011	−6 dB
		XXXX0110	FLAT
		XXXX1001	+6 dB
		XXXX11XX	+12 dB
01000100	Left Volume	XX000000	0 dB
		XX010100	−40 dB
		XX101XXX	−80 dB
		XX11XXXX	−80 dB
01000101	Right Volume	XX000000	0 dB
		XX010100	−40 dB
		XX101XXX	−80 dB
		XX11XXXX	−80 dB
01000110	Mode Select	XXXXX100	Left Mono
		XXXXX101	Stereo
		XXXXX11X	Right Mono
01000111	Read Digital Input 1 or Digital Input 2 on IM Bus	XXXXXXD1D0	D0 = Digital Input 1 D1 = Digital Input 2

General Information

The LMC1982 is a CMOS/bipolar building block intended for high fidelity audio signal processing. It is designed for line level inputs signals (300 mV − 2V) and has a maximum gain of −0.5 dB. While the LMC1982 is manufactured with CMOS processing, NPN transistors are used to build low noise op amps. The combination of CMOS switches, bipolar op amps, and poly-silicon resistors make it possible to achieve an order of magnitude quality improvement over other bipolar circuits that use analog multipliers to accomplish gain adjustment. Internal circuits set the volume to minimum, tone controls to flat, the mute to on, and all other functions off when power is first applied. Individual left and right volume controls are software programmed to achieve the stereo balance function. *Figure 1* shows the connection diagram of a typical LMC1982 application.

The LMC1982 has internal decoding logic that allows a microprocessor (μP) or microcontroller (μC) to communicate directly to the audio control circuitry through an INTERMETAL (IM) Bus interface. This three-wire interface consists of a bi-directional DATA line, a Clock (CLK) input line, and an Identity (ID) line. Address and function selection data (8 bits) are serially shifted from the controller to the LMC1982. This is followed by 8 bits of function value data. Data present in the internal shift register is latched and the instruction is executed.

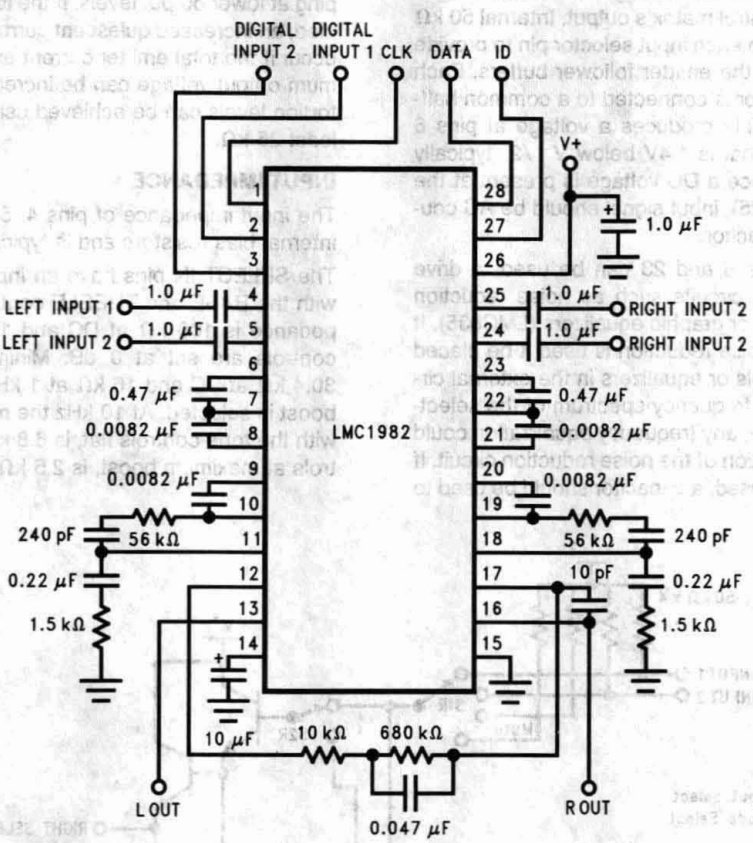


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FIGURE 1. Typical Application

Application Information

INPUT SELECTOR

The LMC1982's input selector and mode control are shown in *Figure 2*. The input selector selects one of two stereo signal sources or a mute function with typical attenuation of 100 dB. The selected signals are then sent to a mode control matrix. As shown in Table I, the matrix provides normal stereo or can direct either channel to both LEFT or RIGHT SELECT OUTPUTs. The third matrix mode is normal stereo. The control matrix output is buffered and appears on each channel's respective SELECT OUT pin (6, 23). Switching noise is kept to a minimum when mute is selected by using a 50 kΩ bias resistor.

Noise performance is optimized through the use of emitter followers in the mode control matrix's output. Internal 50 kΩ resistors are connected to each input selector pin to provide the proper bias point for the emitter follower buffers. Each internal 50 kΩ bias resistor is connected to a common half-supply ($V^+/2$) source. This produces a voltage at pins 6 and 23 (SELECT OUT) that is 1.4V below $V^+/2$ (typically 3.1V with $V^+ = 9V$). Since a DC voltage is present at the input pins (4, 5, 24, and 25), input signal should be AC coupled through a 1 μF capacitor.

The output signal at pins 6 and 23 can be used to drive exteral audio processing circuits such as noise reduction (LM1894–DNR or Dolby) or graphic equalizers (LMC835). It is important that if any noise reduction is used it be placed ahead of any tone controls or equalizers in the external circuit path to preserve the frequency spectrum of the selected input signal. Otherwise, any frequency equalization could prevent the proper operation of the noise reduction circuit. If no external processor is used, a capacitor should be used to couple the SELECT OUT signals directly to pins 7 and 22, respetively.

MINIMUM LOAD IMPEDANCE

The LMC1982 employs emitter-followers to buffer the selected stereo channels. The buffered signals are available at pins 6 and 23 (SELECT OUT). The SELECT OUT buffers operate with a typical bias current 1 mA.

The Electrical Specifications table lists a maximum input signal of 2.0 V_{rms} (2.5 V_{peak}) for 1% THD at the SELECT OUT pins. This distortion level is achieved when the minimum AC load impedance seen by the SELECT OUT pins is 2.5 kΩ (2.5V/1 mA). Using lower load impedances results in clipping at lower output levels. If the load impedance is DC-coupled, an increased quiescent current can flow. Latch-up may occur if the total emitter current exceeds 5 mA. Thus, maximum output voltage can be increased and much lower distortion levels can be achieved using load impedances of at least 25 kΩ.

INPUT IMPEDANCE

The input impedance of pins 4, 5, 24 and 25 is defined by internal bias resistors and is typically 50 kΩ.

The SELECT IN pins have an input impedance that varies with the BASE and TREBLE control settings. The input impedance is 100 kΩ at DC and 19 kΩ at 1 kHz when the controls are set at 0 dB. Minimum input impedance of 30.4 kΩ at DC and 16 kΩ at 1 kHz occurs when maximum boost is selected. At 10 kHz the minimum input impedance, with the tone controls flat, is 6.8 kΩ and, with the tone controls at maximum boost, is 2.5 kΩ.

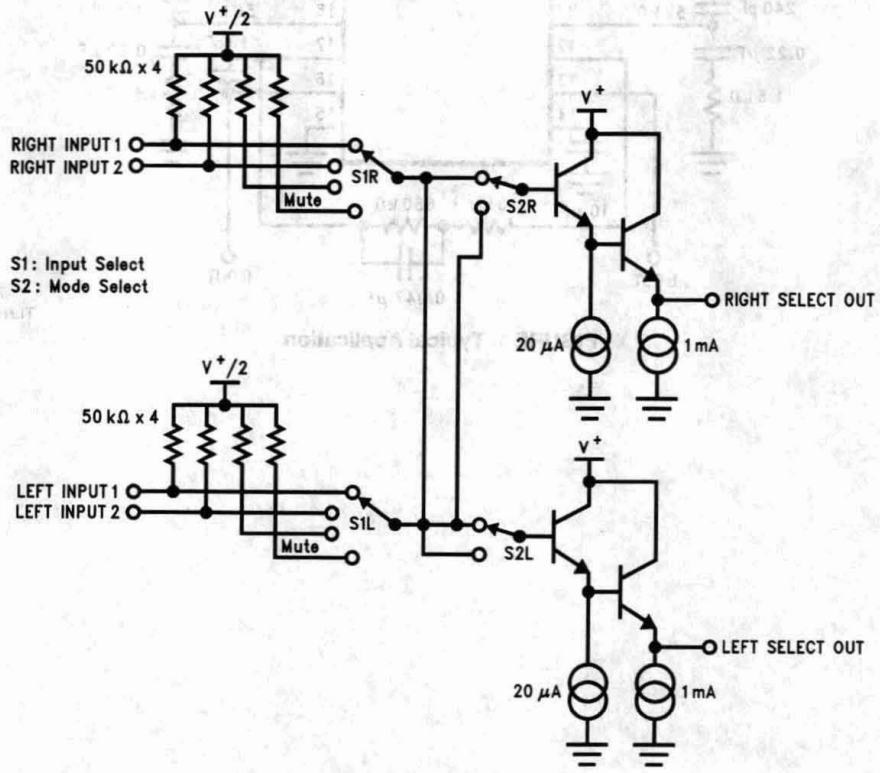

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FIGURE 2. Input and Mode Select Circuitry

Application Information (Continued)

EXTERNAL SIGNAL PROCESSING

The SELECT OUT pins (6 and 23) enable greater system design flexibility by providing a means to implement an external processing loop. This loop can be used for noise reduction circuits such as DNR (LM1894) or multi-band graphic equalizers (LMC835). If both are used, it is important to ensure that the noise reduction circuitry precede the equalization circuits. Failure to do so results in improper operation of the noise reduction circuits. The system shown in *Figure 3* utilizes the external loop to include DNR and a multi-band equalizer.

TONE CONTROL RESPONSE

Bass and treble tone controls are included in the LMC1982. The tone controls used just two external capacitors for each stereo channel. Each has a corner frequency determined by the value of C2 and C3 (see *Figure 4*) and internal resistors in the feedback loop of the internal tone amplifier. The maximum-boost or cut is determined by the data sent to the LMC1982 (see Table I).

The typical tone control response shown in Typical Performance Curves were generated with C2 = C3 = 0.0082 μF and show the response for each step. When modifying the tone control response it is important to note that the ratio of C3 and C2 sets the mid-frequency gain. Symmetrical tone response is achieved when C2 = C3. However, with C2 = 2(C3) and the tone controls set to "flat", the frequency response will be flat at 20 Hz and 20 kHz, and +6 dB at 1 kHz.

The frequency where a tone control begins to deviate from a flat response is referred to as the turn-over frequency. With C = C2 = C3, the LMC1982's treble turn-over frequency is nominally

$$f_{TT} = \frac{1}{2\pi C(14\ k\Omega)}$$

The bass turn-over frequency is nominally

$$f_{BT} = \frac{1}{2\pi C(30.4\ k\Omega)}$$

when maximum boost is chosen. The inflection points (the frequencies where the boost or cut is within 3 dB of the final value) are for treble and bass

$$f_{TI} = \frac{1}{2\pi C(1.9\ k\Omega)}$$

$$f_{BI} = \frac{1}{2\pi C(169.6\ k\Omega)}$$

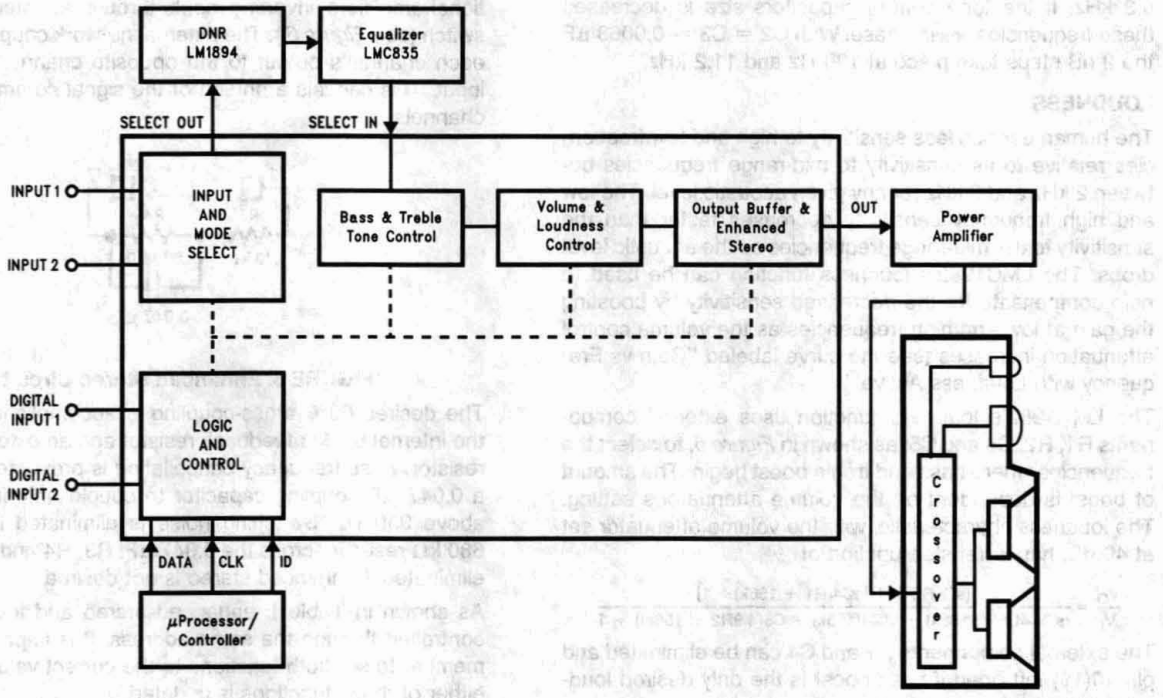

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FIGURE 3. System Block Diagram Utilizing the External Processing Loop (One Channel Shown)

Application Information (Continued)

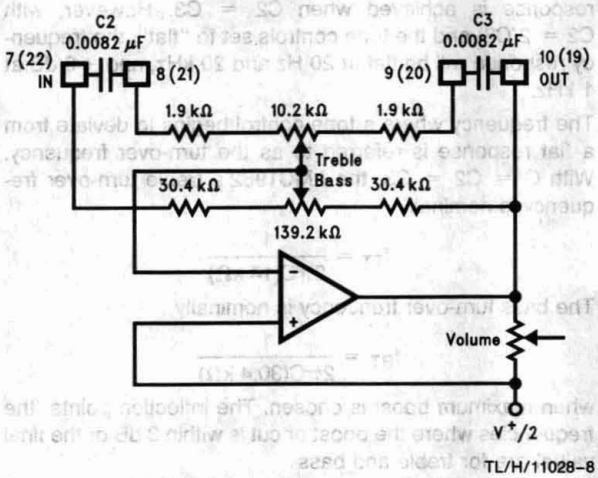

FIGURE 4. The Tone Control Amplifier

Increasing the values of C2 and C3 decreases the turnover and inflection frequencies: i.e., the Tone Control Response Curves shown in Typical Performance Curves will shift left when C2 and C3 are increased and shift right when C2 and C3 are decreased. With C2 = C3 = 0.0082 μF, 2 dB steps are achieved at 100 Hz and 10 kHz. Changing C2 and C3 to 0.01 μF shifts the 2 dB per step frequency to 72 Hz and 8.3 kHz. If the tone control capacitors size is decreased these frequencies will increase. With C2 = C3 = 0.0068 μF the 2 dB steps take place at 130 Hz and 11.2 kHz.

LOUDNESS

The human ear has less sensitivity to high and low frequencies relative to its sensitivity to mid-range frequencies between 2 kHz and 6 kHz for any given acoustic level. The low and high frequency sensitivity decreases faster than the sensitivity to the mid-range frequencies as the acoustic level drops. The LMC1982's loudness function can be used to help compensate for the decreased sensitivity by boosting the gain at low and high frequencies as the volume control attenuation increases (see the curve labeled "Gain vs Frequency with Loudness Active").

The LMC1982's loudness function uses external components R1, R2, C4 and C5, as shown in *Figure 5*, to select the frequencies where bass and treble boost begin. The amount of boost is dependent on the volume attenuator's setting. The loudness characteristic, with the volume attenuator set at 40 dB, has a transfer function of

$$\frac{V_O}{V_I} = \frac{(sC5R2 + 1)[sC4(R1 + 156k) + 1]}{(s^2)C4C5R2(163k) + s[C4(156k) + C5(4.9R2 + 156k)] + 1}$$

The external components R1 and C4 can be eliminated and pin 10(19) left open if bass boost is the only desired loudness characteristic.

As shown in Table I, loudness and enhanced stereo are controlled through the same address. It is important to remember to set both functions to the correct value any time either of these functions is updated.

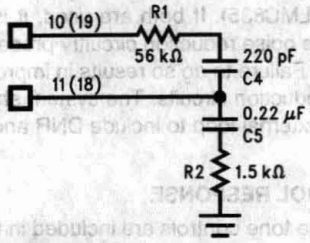

FIGURE 5. Loudness Control Circuit

ENHANCED STEREO

The LMC1982 has an enhanced stereo effect that can be achieved by cross-coupling reverse phase information between the left and right stereo channels. This feature can help improve the apparent stereo channel separation when, because of cabinet or equipment limitations, the left and right speakers are closer to each other than optimum.

Enhanced stereo is created by connecting an external frequency shaping RC network between the OUTPUT operational amplifiers' inverting inputs through an internal CMOS switch (see *Figure 6*). The external network couples 60% of each channel's output to the opposite channel's inverting input. This cancels a portion of the signal common to both channels.

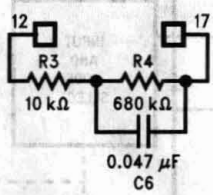

FIGURE 6. Enhanced Stereo Circuit

The desired 60% cross-coupling is accomplished through the internal 6.5 kΩ feedback resistor and an external 10 kΩ resistor. Bass frequency cancellation is prevented by using a 0.047 μF coupling capacitor to couple only frequencies above 330 Hz. Switching noise is eliminated by using a 680 kΩ resistor across the 0.047 μF. R3, R4 and C6 can be eliminated if enhanced stereo is not desired.

As shown in Table I, enhanced stereo and loudness are controlled through the same address. It is important to remember to set both functions to the correct value any time either of these functions is updated.

Application Information (Continued)

SERIAL DATA COMMUNICATION

The LMC1982 uses the INTERMETAL serial bus (IM Bus) standard. Serial data information is sent to the LMC1982 over a three wire IM Bus consisting of Clock (CLK), Data (DATA), and Identity (ID). The DATA line is bidirectional and the CLK and ID lines are unidirectional from the microprocessor or micontroller to the LMC1982. The LMC1982's bidirectional capability is accomplished by using an open drain output on the DATA line and an external 1 kΩ pull-up resistor.

The LMC1982 responds to address values from 01000000 (40_H) through 01000111 (47_H). The addresses select one of the eight available functions (see Table I). The IM Bus' lines have a logic high standby state when using TTL logic levels. As shown in *Figure 7*, data transmission is initiated by low levels on CLK and ID. Next, eight address bits are sent. This address information includes the code to select one of the LMC1982's desired functions. Each address bit is clocked in on the rising edge of CLK. The ID line is taken high after the eight bits of address data are received by the LMC1982. The controlling system continues toggling the CLK line eight more times. Data that determines the selected function's operating point is written into, or single bit information on DIGITAL INPUT 1 or DIGITAL INPUT 2 is read from, the LMC1982. Finally, the end of transmission is signalled by pulsing the ID line low for a minimum of 1 μs. The transmitted function data is latched and the function changes to its new setting.

Table I also details the serial data structure, range, and bit assignments that sets each function's operating point. The volume and tone controls' function control data binarily increments from zero to maximum as the function's operating point changes from 80 dB attenuation to 0 dB attenuation (volume) or −12 dB to +12 dB (tone controls). Note that not all data bits are needed by each function. The extra bits shown as "X"s ("don't cares") are position holders and have no affect on a respective function. They are necessary to properly position the data in the LMC1982's internal data shift register. Unexpected results may take place if these bits are not sent.

The LMC1982's internal data shift register can handle either a 16-bit word or two 8-bit serial data transmissions. It is the final 8 bits of data received before the ID line goes high that are used as the LMC1982 selection and function addresses. The final eight bits after the ID line returns high are used to change a function's operating point. CLK must be stopped when the final 8 data bits are received. The data stored in the internal data latch remains unchanged until the ID is pulsed, signifying the end of data transmission. When ID is pulsed, the new data in the data shift register is latched into the data latch and the selected function takes on a new operating point.

A complete description and more information concerning the IM Bus is given in the appendix of ITT's CCU2000 datasheet.

DIGITAL I/O

The LMC1982's two Digital Input pins, 2 and 3, provide single-bit communication between a peripheral device and the controller over the IM Bus. Each pin has an internal 30 kΩ pull-up resistor. Therefore, these pins should be connected to open collector/drain outputs. The type of information that could be received on these lines and retrieved by a controller include FM stereo pilot indication, power on/off, Secondary Audio Program (SAP), etc.

According to Table I, the logic state of DIGITAL INPUT 1 and DIGITAL INPUT 2 is latched and can be retrieved over the IM Bus using the read command (47_H). The single-bit information sent on the IM Bus is active low since these lines are internally pulled high.

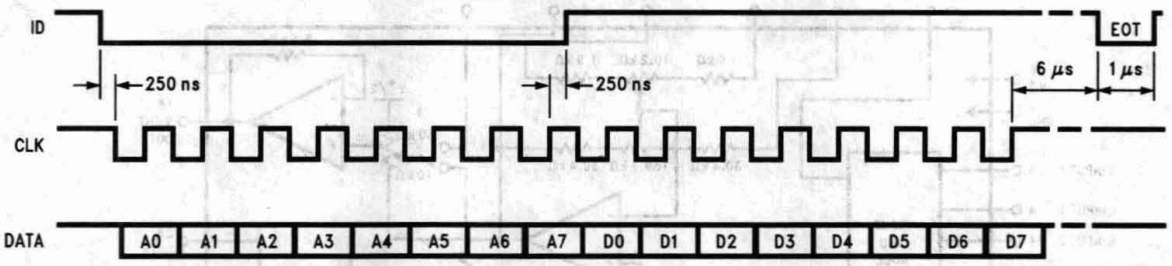

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FIGURE 7. LMC1982's INTERMETAL Serial Bus Timing

National Semiconductor

LMC1983
Digitally-Controlled Stereo Tone and Volume Circuit with Three Selectable Stereo Inputs

General Description

The LMC1983 is a monolithic integrated circuit that provides volume, balance, tone (bass and treble), loudness controls and selection between three pairs of stereo inputs. These functions are digitally controlled through a three-wire communication interface. There are two digital inputs for easy interface to other audio peripherals such as stereo decoders. The LMC1983 is designed for line level input signals (300 mV–2V) and has a maximum gain of −0.5 dB. Volume is set at minimum and tone controls are flat when supply voltage is first applied.

Low noise and distortion result from using analog switches and poly-silicon resistor networks in the signal path.

Additional tone control can be achieved using the LMC835 stereo 7-band graphic equalizer connected to the LMC1983's SELECT OUT/SELECT IN external processor loop.

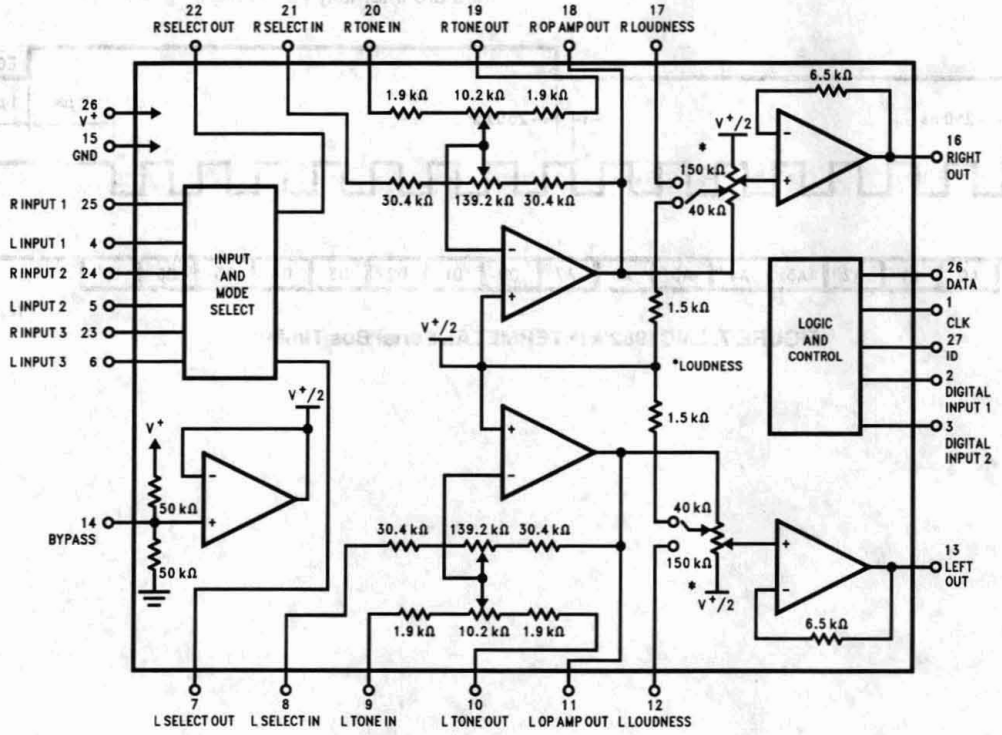
Features

- Low noise and distortion
- Three pairs of stereo inputs
- Loudness compensation
- 40 position 2 dB/step volume attenuator plus mute
- Independent left and right volume controls
- Low noise-suitable for use with DNR® and Dolby® noise reduction
- External processor loop
- Signal handling suitable for compact discs
- Pop-free switching
- Serially programmable: INTERMETAL bus (IM) interface
- 6V to 12V single supply operation
- 28 Pin DIP or PLCC Package

Applications

- Stereo television
- Music reproduction systems
- Sound reinforcement systems
- Electronic music (MIDI)
- Personal computer audio control

Block Diagram



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Absolute Maximum Ratings (Notes 1 and 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage ($V^+ - GND$)	15V
Voltage at any Pin	GND − 0.2V to V^+ + 0.2V
Input Current at any Pin (Note 3)	5 mA
Package Input Current (Note 3)	20 mA
Power Dissipation (Note 4)	500 mW
Junction Temperature	+125°C
Storage Temperature	−65°C to +150°C
Lead Temperature	
N Package, (Soldering, 10 Seconds)	+260°C
V Package, (Vapor Phase, 60 Seconds)	215°C
Infrared, (15 Seconds)	220°C
ESD Susceptability (Note 5)	2 kV

Operating Ratings (Notes 1 and 2)

Temperature Range	$T_{MIN} \le T_A \le T_{MAX}$
LMC1983CIN, LMC1983CIV	$-40°C \le T_A \le +85°C$
Supply Voltage ($V^+ - V^-$)	6V to 12V

Electrical Characteristics

The following specifications apply for $V^+ = 9V$, $f_{IN} = 1$ kHz, input signal (300 mV) applied to INPUT 1, volume = 0 dB, bass = 0 dB, treble = 0 dB, and loudness is off unless otherwise specified. All limits apply for $T_A = T_J = +25°C$.

Symbol	Parameter	Conditions	Typical (Note 6)	Limit (Note 7)	Unit (Limit)
I_S	Supply Current		15	25	mA (max)
V_{IN}	Input Voltage	Clipping Level (1.0% THD), Select Out (Pins 7, 22)	2.3	2.0	V_{rms} (min)
THD	Total Harmonic Distortion	Left and Right channels; Output Pins 13, 16			
		$V_{IN} = 0.3\ V_{rms}$; f_{IN} = 100 Hz, 1 kHz, 10 kHz	0.008	0.1	% (max)
		$V_{IN} = 2.0\ V_{rms}$; f_{IN} = 100 Hz, 1 kHz	0.4	1.0	% (max)
		$V_{IN} = 2.0\ V_{rms}$; f_{IN} = 10 kHz	0.5	1.0	% (max)
		$V_{IN} = 0.5\ V_{rms}$; Bass and Treble Tone Controls Set at Maximum	0.07	0.5	% (max)
		$V_{IN} = 0.3\ V_{rms}$; Volume Attenuator at −20 dB, Bass and Treble Tone Controls Set at Maximum	0.06	0.15	% (max)
	DC Shifts	$V_{IN} = 0.3\ V_{rms}$; between Any Two Adjacent Control Settings	2.0	4.0	mV (max)
		$V_{IN} = 0.3\ V_{rms}$; All Mode and Input Positions	18	20	mV (max)
R_{OUT}	AC Output Impedance	Pins 7, 22, (470Ω to Ground at Input)	150	200	Ω (max)
		Pins 13, 16	26	40	Ω (max)
R_{IN}	AC Input Impedance	Pins 4, 5, 23, 24, 25	50	72	kΩ (max)
				35	kΩ (min)
	Volume Attenuator Range	Pins 13, 16; Volume Attenuation at 0100010XXX000000 (0 dB)	0.5	1.5	dB (max)
		0100010XXX101XXX (80 dB);	80	78	dB (min)
		(Relative to Attenuation at the 0 dB Setting)		82	dB (max)
	Volume Step Size	All Volume Attenuation Settings from 0100010XXX101XXX (80 dB) to 0100010XXX000000 (0 dB) (Note 9)	2.0	1.5	dB (min)
				2.5	dB (min)
	Channel-to-Channel Tracking Error	All Volume Attenuation Settings from 0100010XXX100110 (76 dB) to 0100010XXX000000 (0 dB)	±0.1	±1.5	dB (min)
		from 0100010XXX101XXX (80 dB) to 0100010XXX100111 (78 dB)		±2.0	dB (min)
	Mute Attenuation	$V_{IN} = 1.0\ V_{rms}$	105	86	dB (max)

Electrical Characteristics

The following specifications apply for $V^+ = 9V$, $f_{IN} = 1$ kHz, input signal (300 mV) applied to INPUT 1, volume = 0 dB, bass = 0 dB, treble = 0 dB, and loudness is off unless otherwise specified. All limits apply for $T_A = T_J = +25°C$. (Continued)

Symbol	Parameter	Conditions	Typical (Note 6)	Limit (Note 7)	Unit (Limit)
	Bass Gain Range	f_{IN} = 100 Hz, Pins 13, 16	±12	±10.0 ±14.0	dB (min) dB (max)
	Bass Tracking Error	f_{IN} = 100 Hz, Pins 13, 16	±0.1	±1.5	dB (max)
	Bass Step Size	f_{IN} = 100 Hz, Pins 13, 16 (Relative to Previous Level)	2.0	1.5 2.5	dB (min) dB (max)
	Treble Gain Range	f_{IN} = 10 kHz, Pins 13, 16	±12	±10.0 ±14.0	dB (min) dB (max)
	Treble Tracking Error	f_{IN} = 10 kHz, Pins 13, 16	±0.1	±1.5	dB (max)
	Treble Step Size	f_{IN} = 10 kHz, Pins 13, 16 (Relative to Previous Level)	2.0	1.5 2.5	dB (min) dB (max)
	Frequency Response	V_{IN} Applied to Input 1 and Input 2; f_{IN} = 20 Hz − 20 kHz (Relative to Signal Amplitude at 1 kHz)	±0.1	±1.0	dB (max)
	Loudness	Volume Attenuator = 40 dB, Loudness on (See *Figure 5*) Gain at 100 Hz (Referenced to Gain at 1 kHz) Gain at 10 kHz (Referenced to Gain at 1 kHz)	 11.5 6.5	 13.5 9.5 8.5 4.5	 dB (max) dB (min) dB (max) dB (min)
	Signal-to-Noise Ratio	V_{IN} = 1.0 V_{rms}, A Weighted, Measured at 1 kHz, R_S = 470Ω	95	90	dB (min)
	Channel Balance	All Volume Settings	0.2	1.0	dB (max)
	Channel Separation	Input Pins 4, 25: Output Pins 13, 16; V_{IN} = 1.0 V_{rms} (Note 8)	80	60	dB (min)
	Input-Input Isolation	470Ω to AC Ground on Unused Input	95	60	dB (min)
PSSR	Power Supply Rejection Ratio	V^+ = 9 V_{DC}; 200 mV_{rms}, 100 Hz Sinewave Applied to Pin 26	32	28	dB (min)
f_{CLK}	Clock Frequency		5.0	1.0	MHz (max)
$V_{IN(1)}$	Logic "1" Input Voltage	Pins 1, 27, 28 (IM Bus) Pins 2, 3	1.3 2.9	2.0 5.5	V (min) V (min)
$V_{IN(0)}$	Logic "0" Input Voltage	Pins 1, 27, 28 (IM Bus) Pins 2, 3	0.4 1.2	0.8 3.5	V (max) V (max)
$V_{OUT(1)}$	Logic "1" Output Voltage	Pin 28 (IM Bus)		2.0	V (min)
$V_{OUT(0)}$	Logic "0" Output Voltage	Pin 28 (IM Bus)	0.4	0.8	V (max)

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the deivce may occur. Operating Ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.

Note 2: All voltages are specified with respect to ground.

Note 3: When the input voltage (V_{IN}) at any pin exceeds the power supply voltages ($V_{IN} < V^-$ or $V_{IN} > V^+$) the absolute value of the current at that pin should be limited to 5 mA or less. The 20 mA package input current limits the number of pins that can exceed the power supply voltages with 5 mA current limit to four.

Note 4: The maximum power dissipation must be derated at elevated temperatures and is dictated by T_{JMAX}, θ_{JA}, and the ambient temperature T_A. The maximum allowable power dissipation is $P_D = (T_{JMAX} - T_A)/\theta_{JA}$ or the number given in the Absolute Maximum Ratings, whichever is lower. For the LMC1983CIN, T_{JMAX} = +125°C, and the typical junction-to-ambient thermal resistance, when board mounted, is 67°C/W.

Note 5: Human body model; 100 pF discharged through a 1.5 kΩ resistor.

Note 6: Typicals are at $T_J = +25°C$ and represent the most likely parametric norm.

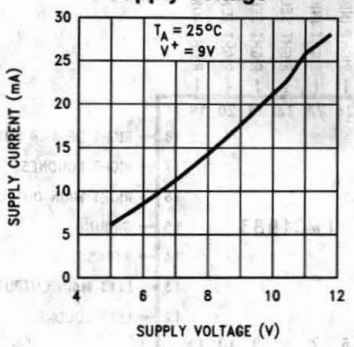
Note 7: Limits are guaranteed to National's AOQL (Average Outgoing Quality Level).

Note 8: The Input-Input Isolation is tested by driving one input and measuring the output when the undriven input are selected.

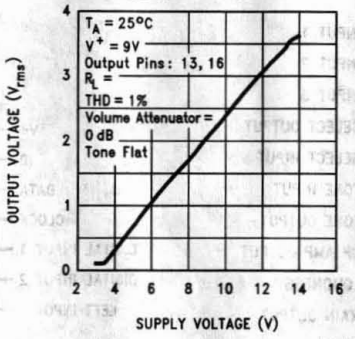
Note 9: The Volume Step Size is defined as the change in attenuation between any two adjacent volume attenuation settings. The nominal Volume Step Size is 2 dB.

Typical Performance Characteristics

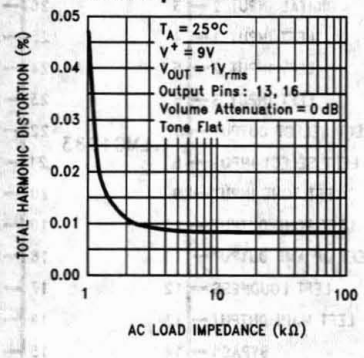
Supply Current vs Supply Voltage



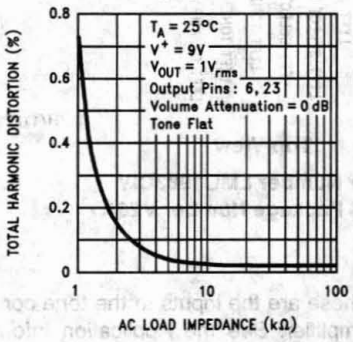
Output Voltage vs Supply Voltage



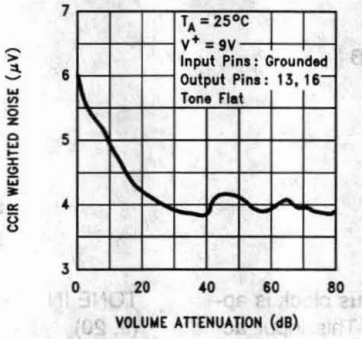
THD vs Load Impedance



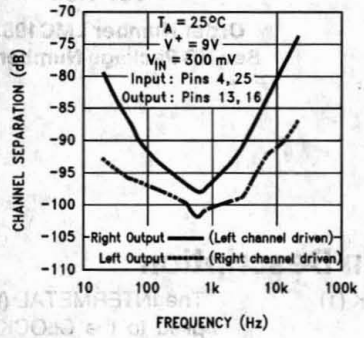
THD vs Load Impedance



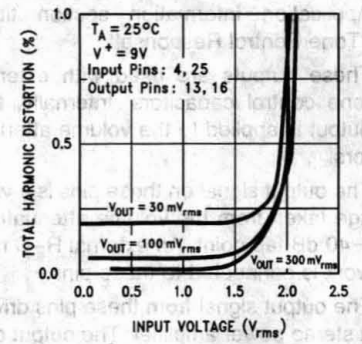
CCIR Output Noise vs Volume Setting



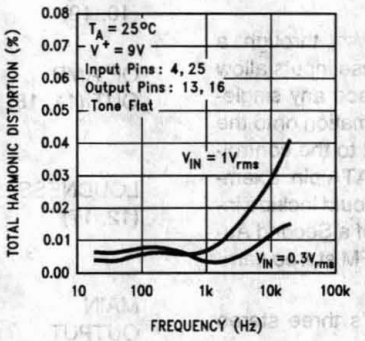
Channel Separation vs Frequency



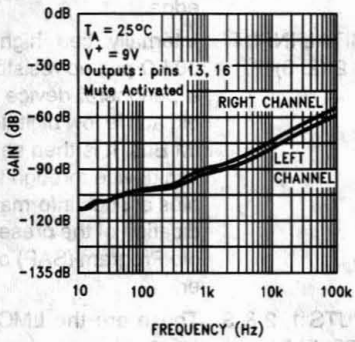
THD vs V_{IN} (V_{OUT} Constant)



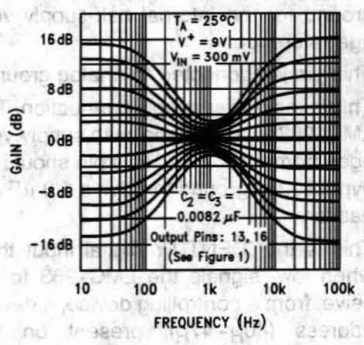
THD vs Frequency



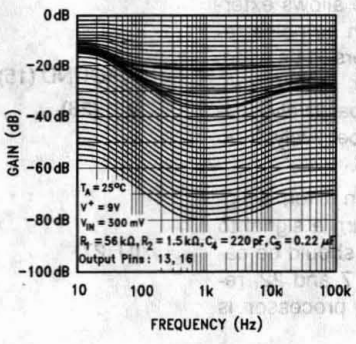
Mute Gain vs Frequency



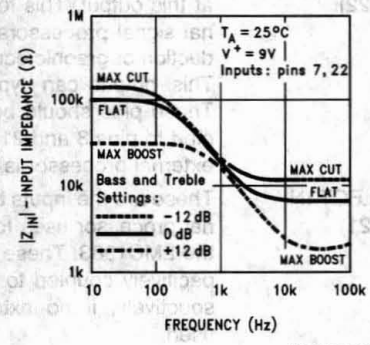
Tone Control Response with Equal Bass and Treble Control Settings



Loudness Response vs Frequency



Select Input Impedance vs Frequency



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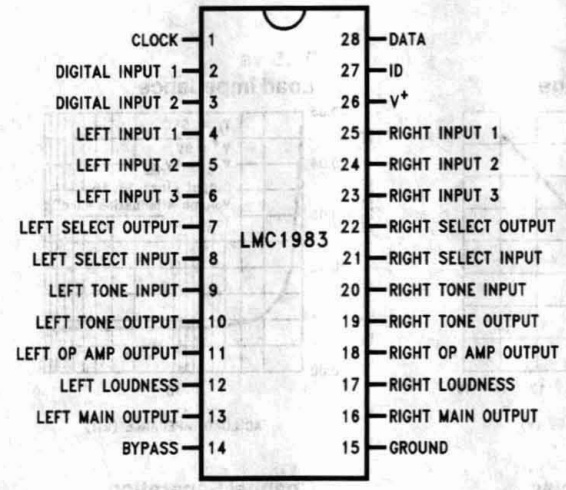
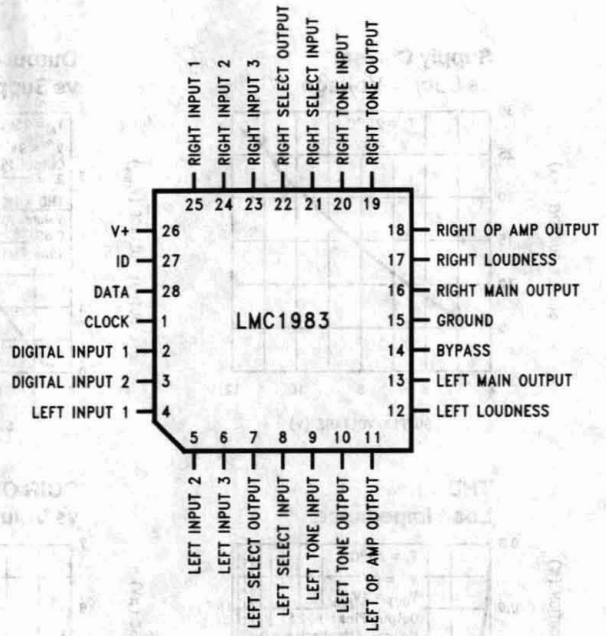
Connection Diagram



TL/H/11279–2

Top View

Order Number LMC1983CIN
See NS Package Number N28B



TL/H/11279–10

Top View

Order Number LMC1983CIV
See NS Package Number V28A

Pin Description

CLK (1)	The INTERMETAL (IM) Bus clock is applied to the CLOCK pin. This input accepts a TTL or CMOS level signal. The input is used to clock the DATA signal. A data bit must be valid on the rising clock edge.
DIGITAL INPUT 1 & 2 (2, 3)	Internally tied high to V^+ through a 30 kΩ pull-up resistor, these inputs allow a peripheral device to place any single-bit, active low digital information onto the IM Bus. It is then sent out to the controlling device through the DATA pin. Examples of such information could include indication of the presence of a Second Audio Program (SAP) or an FM stereo carrier.
INPUTS 1, 2 & 3 (4, 25; 5, 24; 6, 23)	These are the LMC1983's three stereo input pairs.
SELECT OUT (7, 22)	The selected INPUT signal is available at this output. This feature allows external signal processors such as noise reduction or graphic equalizers to be used. This output can typically sink 1 mA. These pins should be capacitively coupled to pins 8 and 21, respectively, if no external processor is used.
SELECT IN (8, 21)	These are the inputs that an external signal processor uses to return a signal to the LMC1983. These pins should be capacitively coupled to pins 7 and 22, respectively, if no external processor is used.
TONE IN (9, 20)	These are the inputs to the tone control amplifier. See the Application Information section titled "Tone Control Response".
TONE OUT (10, 19)	Tone control amplifier output. See the Application Information section titled "Tone Control Response".
OP AMP OUT (11, 18)	These outputs are used with external tone control capacitors. Internally, this output is applied to the volume attenuators.
LOUDNESS (12, 17)	The output signal on these pins is a voltage taken from the volume attenuator's −40 dB tap point. An external R–C network is connected to these pins.
MAIN OUTPUT (13, 16)	The output signal from these pins drives a stereo power amplifier. The output can typically sink 1 mA.
BYPASS (14)	A 10 μF capacitor is connected between this pin and ground to provide an AC ground for the internal half-supply voltage reference.
GROUND (15)	This pin is connected to analog ground.
V^+ (26)	This is the power supply connection. The LMC1983 is operational with supply voltages from 6V to 12V. This pin should be bypassed to ground through a 1.0 μF capacitor.
ID (27)	This is the IDENTITY digital input that, when low, signals the LMC1983 to receive, from a controlling device, a device address (40_H–47_H), present on the DATA line.

Pin Description (Continued)

DATA (28) This is the serial data input for communications sent by a controller. The controller must have open drain outputs used with external pull-up resistors. The data rate has a maximum frequency of 1 MHz. The LMC1983 requires 16 bits of data to control or change a function: the first 8 bits select the LMC1983 and one of eight functions. The final eight bits set the function to a desired value. The data must be valid on the rising edge of the CLOCK input signal.

General Information

The LMC1983 is a CMOS/bipolar building block intended for high fidelity audio signal processing. It is designed for line level inputs signals (300 mV − 2V) and has a maximum gain of −0.5 dB. While the LMC1983 is manufactured with CMOS processing, NPN transistors are used to build low noise op amps. The combination of CMOS switches, bipolar op amps, and poly-silicon resistors make it possible to achieve an order of magnitude quality improvement over other bipolar circuits that use analog multipliers to accomplish gain adjustment. Internal circuits set the volume to minimum, tone controls to flat, the mute to on, and all other functions off when power is first applied. Individual left and right volume controls are software programmed to achieve the stereo balance function. *Figure 1* shows the connection diagram of a typical LMC1983 application.

The LMC1983 has internal decoding logic that allows a microprocessor (μP) or microcontroller (μC) to communicate directly to the audio control circuitry through an INTERMETAL (IM) Bus interface. This three-wire interface consists of a bi-directional DATA line, a Clock (CLK) input line, and an Identity (ID) line. Address and function selection data (8 bits) are serially shifted from the controller to the LMC1983. This is followed by 8 bits of function value data. Data present in the internal shift register is latched and the instruction is executed.

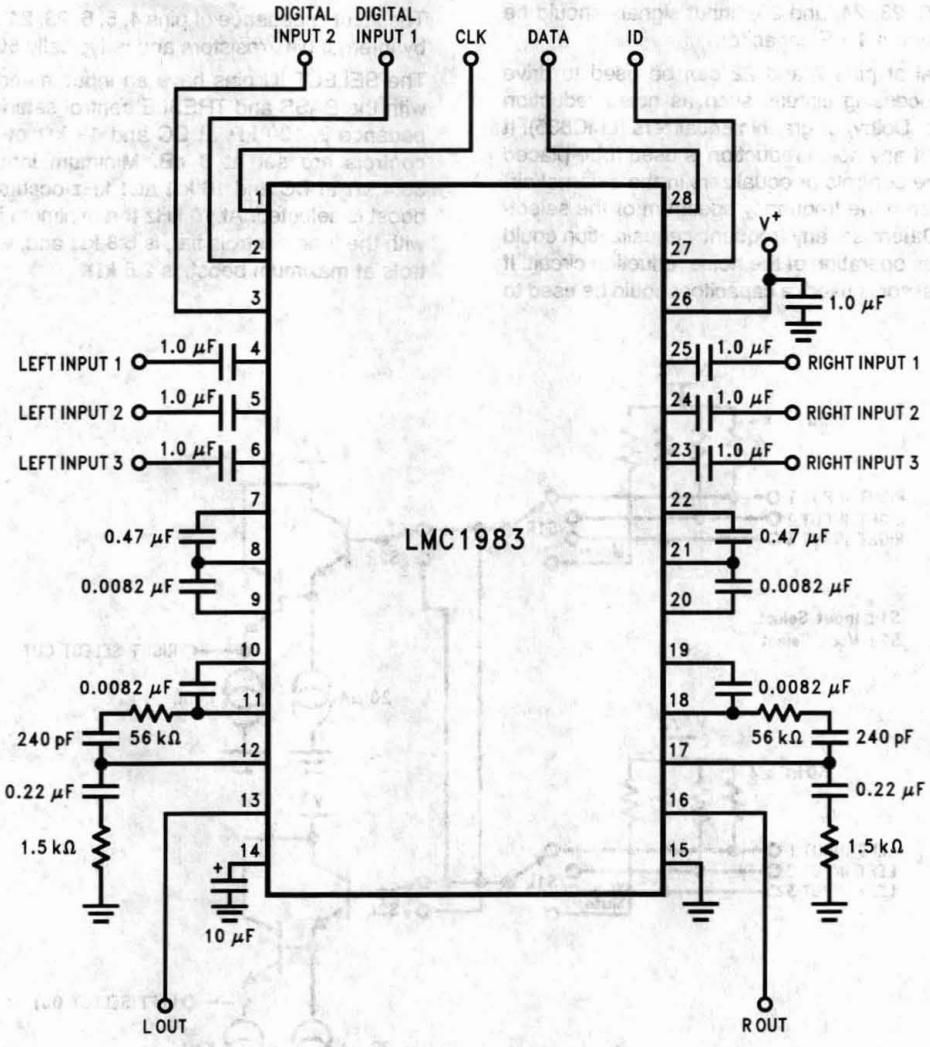


FIGURE 1. Typical Application

Application Information

INPUT SELECTOR

The LMC1983's input selector and mode control are shown in *Figure 2*. The input selector selects one of three stereo signal sources or a mute function with typical attenuation of 100 dB. The selected signals are then sent to a mode control matrix. As shown in Table I, the matrix provides normal stereo or can direct any given channel to both LEFT or RIGHT SELECT OUTPUTs. The third matrix mode is normal stereo. The control matrix output is buffered and appears on each channel's respective SELECT OUT pin (7, 22). Switching noise is kept to a minimum when mute is selected by using a 50 kΩ bias resistor.

Noise performance is optimized through the use of emitter followers in the mode control matrix's output. Internal 50 kΩ resistors are connected to each input selector pin to provide the proper bias point for the emitter follower buffers. Each internal 50 kΩ bias resistor is connected to a common half-supply ($V^+/2$) source. This produces a voltage at pins 7 and 22 (SELECT OUT) that is 1.4V below $V^+/2$ (typically 3.1V with $V^+ = 9V$). Since a DC voltage is present at the input pins (4, 5, 6, 23, 24, and 25), input signals should be AC coupled through a 1 μF capacitor.

The output signal at pins 7 and 22 can be used to drive exteral audio processing circuits such as noise reduction (LM1894–DNR or Dolby) or graphic equalizers (LMC835). It is important that if any noise reduction is used it be placed ahead of any tone controls or equalizers in the external circuit path to preserve the frequency spectrum of the selected input signal. Otherwise, any frequency equalization could prevent the proper operation of the noise reduction circuit. If no external processor is used, a capacitor should be used to couple the SELECT OUT signals directly to pins 8 and 21, respectively.

MINIMUM LOAD IMPEDANCE

The LMC1983 employs emitter-followers to buffer the selected stereo channels. The buffered signals are available at pins 7 and 22 (SELECT OUT). The SELECT OUT buffers operate with a typical bias current of 1 mA.

The Electrical Specifications table lists a maximum input signal of 2.0 V_{rms} (2.8 V_{peak}) for 1% THD at the SELECT OUT pins. This distortion level is achieved when the minimum AC load impedance seen by the SELECT OUT pins is 2.5 kΩ (2.5V/1 mA). Using lower load impedances results in clipping at lower output levels. If the load impedance is DC-coupled, an increased quiescent current can flow. Latch-up may occur if the total emitter current exceeds 5 mA. Thus, maximum output voltage can be increased and much lower distortion levels can be achieved using load impedances of at least 25 kΩ.

INPUT IMPEDANCE

The input impedance of pins 4, 5, 6, 23, 24 and 25 is defined by internal bias resistors and is typically 50 kΩ.

The SELECT IN pins have an input impedance that varies with the BASS and TREBLE control settings. The input impedance is 100 kΩ at DC and 19 kΩ at 1 kHz when the controls are set at 0 dB. Minimum input impedance of 30.4 kΩ at DC and 16 kΩ at 1 kHz occurs when maximum boost is selected. At 10 kHz the minimum input impedance, with the tone controls flat, is 6.8 kΩ and, with the tone controls at maximum boost, is 2.5 kΩ.

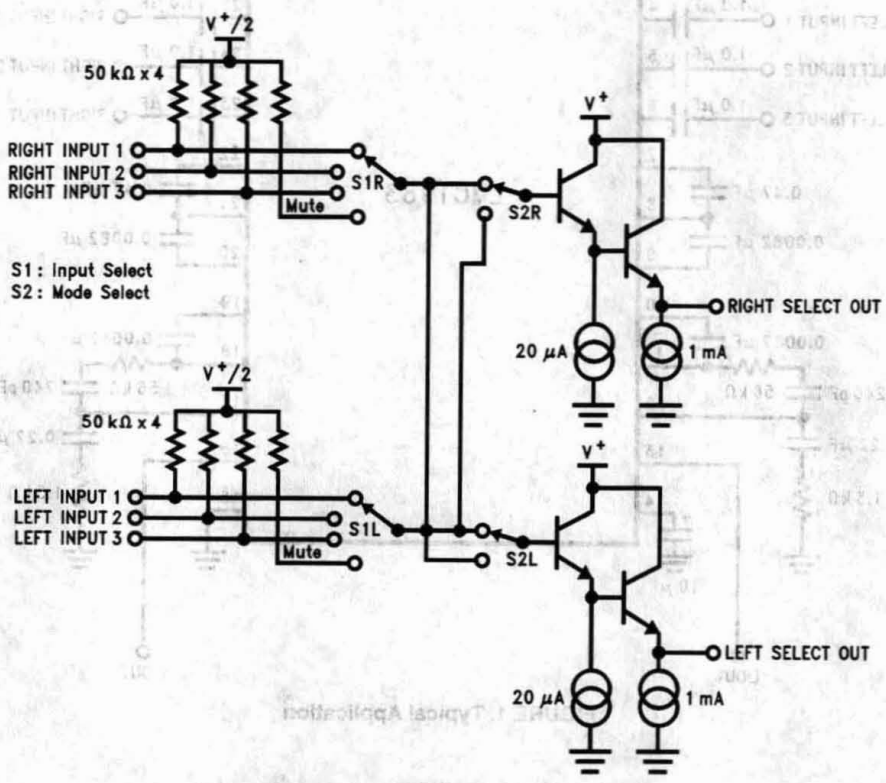


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FIGURE 2. Input and Mode Select Circuitry

Application Information (Continued)

TABLE I. IM Bus Programming Codes for LMC1983

Address (A7–A0)	Function	Data	Function Selected
01000000	Input Select + Mute	XXXXXX00	INPUT1
		XXXXXX01	INPUT2
		XXXXXX10	INPUT3
		XXXXXX11	MUTE
01000001	Loudness	XXXXXXX0	Loudness **OFF**
		XXXXXXX1	Loudness **ON**
01000010	Bass	XXXX0000	−12 dB
		XXXX0011	−6 dB
		XXXX0110	FLAT
		XXXX1001	+6 dB
		XXXX11XX	+12 dB
01000011	Treble	XXXX0000	−12 dB
		XXXX0011	−6 dB
		XXXX0110	FLAT
		XXXX1001	+6 dB
		XXXX11XX	+12 dB
01000100	Left Volume	XX000000	0 dB
		XX010100	−40 dB
		XX101XXX	−80 dB
		XX11XXXX	−80 dB
01000101	Right Volume	XX000000	0 dB
		XX010100	−40 dB
		XX101XXX	−80 dB
		XX11XXXX	−80 dB
01000110	Mode Select	XXXXX100	Left Mono
		XXXXX101	Stereo
		XXXXX11X	Right Mono
01000111	Read Digital Input 1 or Digital Input 2 on IM Bus	XXXXXXD1D0	D0 = Digital Input 1 D1 = Digital Input 2

Application Information (Continued)

EXTERNAL SIGNAL PROCESSING

The SELECT OUT pins (7 and 22) enable greater system design flexibility by providing a means to implement an external processing loop. This loop can be used for noise reduction circuits such as DNR (LM1894) or multi-band graphic equalizers (LMC835). If both are used, it is important to ensure that the noise reduction circuitry precede the equalization circuits. Failure to do so results in improper operation of the noise reduction circuits. The system shown in *Figure 3* utilizes the external loop to include DNR and a multi-band equalizer.

TONE CONTROL RESPONSE

Bass and treble tone controls are included in the LMC1983. The tone controls use just two external capacitors for each stereo channel. Each has a corner frequency determined by the value of C2 and C3 (see *Figure 4*) and internal resistors in the feedback loop of the internal tone amplifier. The maximum-boost or cut is determined by the data sent to the LMC1983 (see Table I).

The typical tone control response shown in Typical Performance Curves were generated with C2 = C3 = 0.0082 μF and show the response for each step. When modifying the tone control response it is important to note that the ratio of C3 and C2 sets the mid-frequency gain. Symmetrical tone response is achieved when C2 = C3. However, with C2 = 2(C3) and the tone controls set to "flat", the frequency response will be flat at 20 Hz and 20 kHz, and +6 dB at 1 kHz.

The frequency where a tone control begins to deviate from a flat response is referred to as the turn-over frequency. With C = C2 = C3, the LMC1983's treble turn-over frequency is nominally

$$f_{TT} = \frac{1}{2\pi C(14\ k\Omega)}$$

The bass turn-over frequency is nominally

$$f_{BT} = \frac{1}{2\pi C(30.4\ k\Omega)}$$

when maximum boost is chosen. The inflection points (the frequencies where the boost or cut is within 3 dB of the final value) are for treble and bass

$$f_{TI} = \frac{1}{2\pi C(1.9\ k\Omega)}$$

$$f_{BI} = \frac{1}{2\pi C(169.6\ k\Omega)}$$

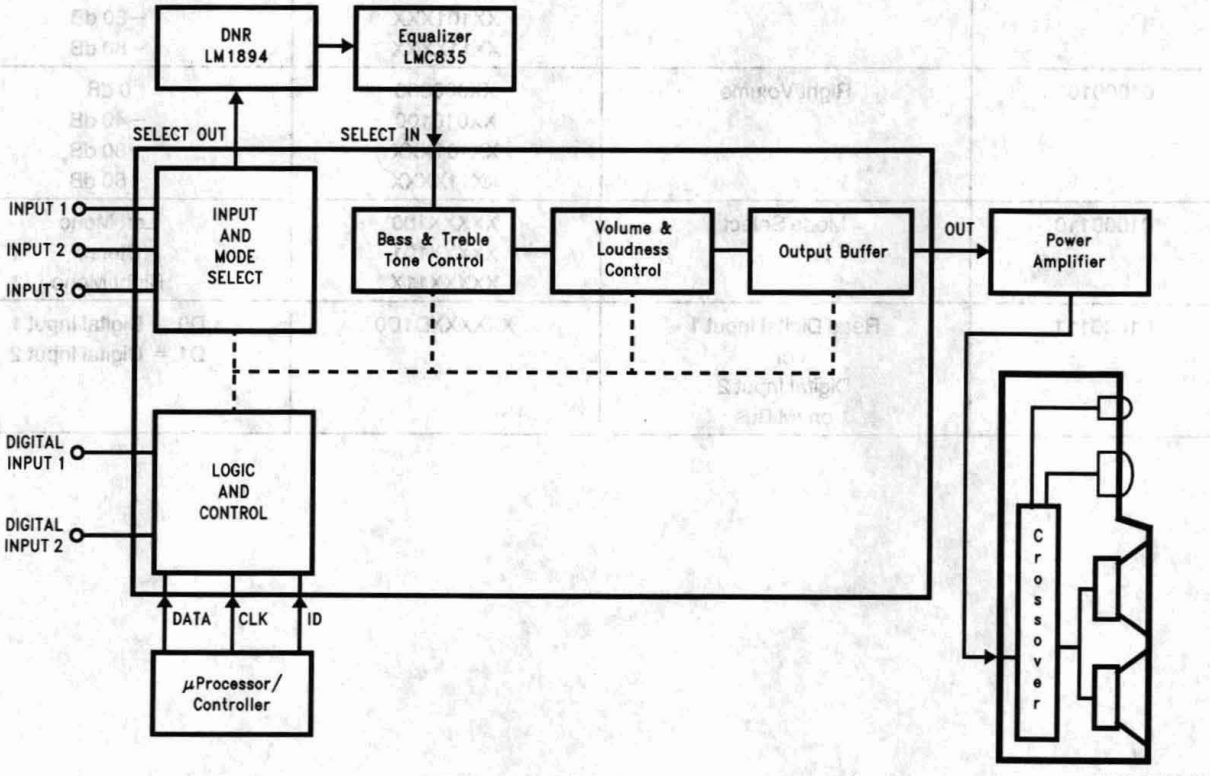

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FIGURE 3. System Block Diagram Utilizing the External Processing Loop (One Channel Shown)

Application Information (Continued)

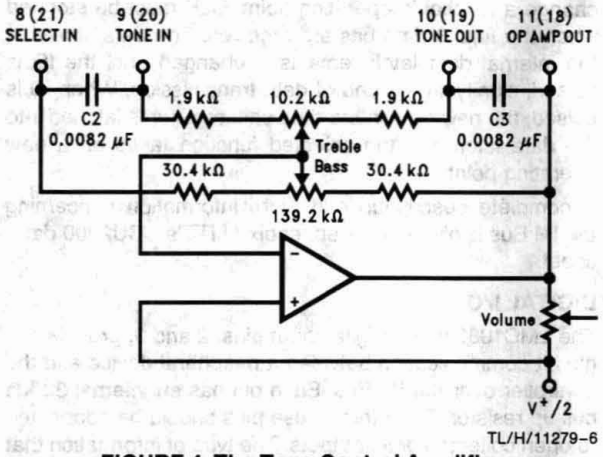

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FIGURE 4. The Tone Control Amplifier

Increasing the values of C2 and C3 decreases the turnover and inflection frequencies: i.e., the Tone Control Response Curves shown in Typical Performance Curves will shift left when C2 and C3 are increased and shift right when C2 and C3 are decreased. With C2 = C3 = 0.0082, 2 dB steps are achieved at 100 Hz and 10 kHz. Changing C2 and C3 to 0.01 μF shifts the 2 dB per step frequency to 72 Hz and 8.3 kHz. If the tone control capacitors' size is decreased these frequencies will increase. With C2 = C3 = 0.0068 μF the 2 dB steps take place at 130 Hz and 11.2 kHz.

LOUDNESS

The human ear has less sensitivity to high and low frequencies relative to its sensitivity to mid-range frequencies between 2 kHz and 6 kHz for any given acoustic level. The low and high frequency sensitivity decreases faster than the sensitivity to the mid-range frequencies as the acoustic level drops. The LMC1983's loudness function can be used to help compensate for the decreased sensitivity by boosting the gain at low and high frequencies as the volume control attenuation increases (see the curve labeled "Gain vs Frequency with Loudness Active").

The LMC1983's loudness function uses external components R1, R2, C4 and C5, as shown in *Figure 5*, to select the frequencies where bass and treble boost begin. The amount of boost is dependent on the volume attenuator's setting. The loudness characteristic, with the volume attenuator set at 40 dB, has a transfer function of

$$\frac{V_O}{V_I} = \frac{(sC5R2 + 1)[sC4(R1 + 156k) + 1]}{(s^2)C4C5R2(163k) + s[C4(156k) + C5(4.9R2 + 156k)] + 1}$$

The external components R1 and C4 can be eliminated and pin 11(18) left open if bass boost is the only desired loudness characteristic.

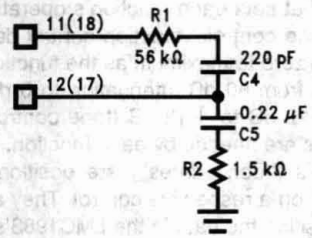

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FIGURE 5. Loudness Control Circuit

SERIAL DATA COMMUNICATION

The LMC1983 uses the INTERMETAL serial bus (IM Bus) standard. Serial data information is sent to the LMC1983 over a three wire IM Bus consisting of Clock (CLK), Data (DATA), and Identity (ID). The DATA line is bidirectional and the CLK and ID lines are unidirectional from the microprocessor or micontroller to the LMC1983. The LMC1983's bidirectional capability is accomplished by using an open drain output on the DATA line and an external 1 kΩ pull-up resistor.

The LMC1983 responds to address values from 01000000 (40_H) through 01000111 (47_H). The addresses select one of the eight available functions (see Table I). The IM Bus' lines have a logic high standby state when using TTL logic levels. As shown in *Figure 6*, data transmission is initiated by low levels on CLK and ID. Next, eight address bits are sent. This address information includes the code to select one of the LMC1983's desired functions. Each address bit is clocked in on the rising edge of CLK. The ID line is taken high after the eight bits of address data are received by the LMC1983.

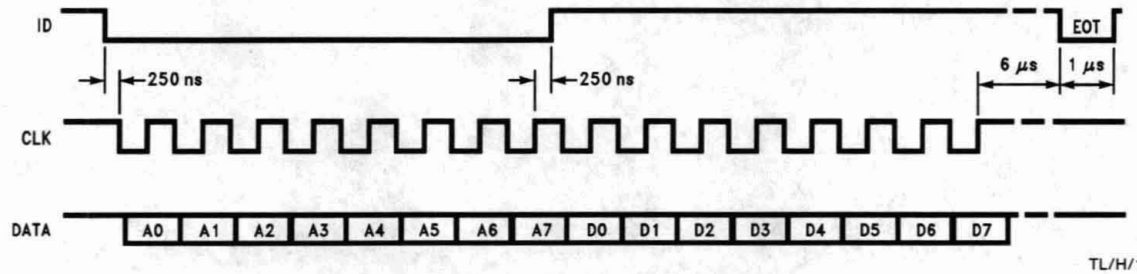

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FIGURE 6. LMC1983's INTERMETAL Serial Bus Timing

Application Information (Continued)

The controlling system continues toggling the CLK line eight more times. Data that determines the selected function's operating point is written into, or single bit information on DIGITAL INPUT 1 or DIGITAL INPUT 2 is read from, the LMC1983. Finally, the end of transmission is signaled by pulsing the ID line low for a minimum of 3 μs. The transmitted function data is latched and the function changes to its new setting.

Table I also details the serial data structure, range, and bit assignments that sets each function's operating point. The volume and tone controls' function control data binarily increments from zero to maximum as the function's operating point changes from 80 dB attenuation to 0 dB attenuation (volume) or −12 dB to +12 dB (tone controls). Note that not all data bits are needed by each function. The extra bits shown as "X"s ("don't cares") are position holders and have no affect on a respective control. They are necessary to properly position the data in the LMC1983's internal data shift register. Unexpected results may take place if these bits are not sent.

The LMC1983's internal data shift register can handle either a 16-bit word or two 8-bit serial data transmissions. It is the final 8 bits of data received before the ID line goes high that are used as the LMC1983 selection and function addresses. The final eight bits after the ID line returns high are used to change a function's operating point. CLK must be stopped when the final 8 data bits are received. The data stored in the internal data latch remains unchanged until the ID is pulsed, signifying the end of data transmission. When ID is pulsed, the new data in the data shift register is latched into the data latch and the selected function takes on a new operating point.

A complete description and more information concerning the IM Bus is given in the appendix of ITT's CCU2000 datasheet.

DIGITAL I/O

The LMC1983's two Digital Input pins, 2 and 3, provide single-bit communication between a peripheral device and the controller over the IM Bus. Each pin has an internal 30 kΩ pull-up resistor. Therefore, these pins should be connected to open collector/drain outputs. The type of information that could be received on these lines and retrieved by a controller include FM stereo pilot indication, power on/off, Secondary Audio Program (SAP), etc.

According to Table I, the logic state of DIGITAL INPUT 1 and DIGITAL INPUT 2 is latched and can be retrieved over the IM Bus using the read command (47_H). The single-bit information sent on the IM Bus is active low since these lines are internally pulled high.

National Semiconductor

LMC1992 Digitally-Controlled Stereo Tone and Volume Circuit with Four-Channel Input-Selector

General Description

The LMC1992 is a monolithic integrated circuit that provides four stereo inputs, bass and treble tone controls, and volume, balance, and front-rear fader controls. These functions are digitally controlled through a three-wire communication interface. All of the LMC1992s functions are achieved with only three external capacitors per channel. It is designed for line level input signals (300 mV − 2V) and has a maximum gain of 0 dB.

The internal design is optimized for external capacitors having values of 0.1 μF or less. This allows the use of chip capacitors for coupling and tone control functions.

Low noise and distortion result from using analog switches and thin-film silicon-chromium resistor networks in the signal path.

Volume and fader are at minimum and tone controls are flat when supply voltage is first applied.

Additional tone control can be achieved using the LMC835 stereo 7-band graphic equalizer connected to the LMC1992's select-out/select-in external processor loop.

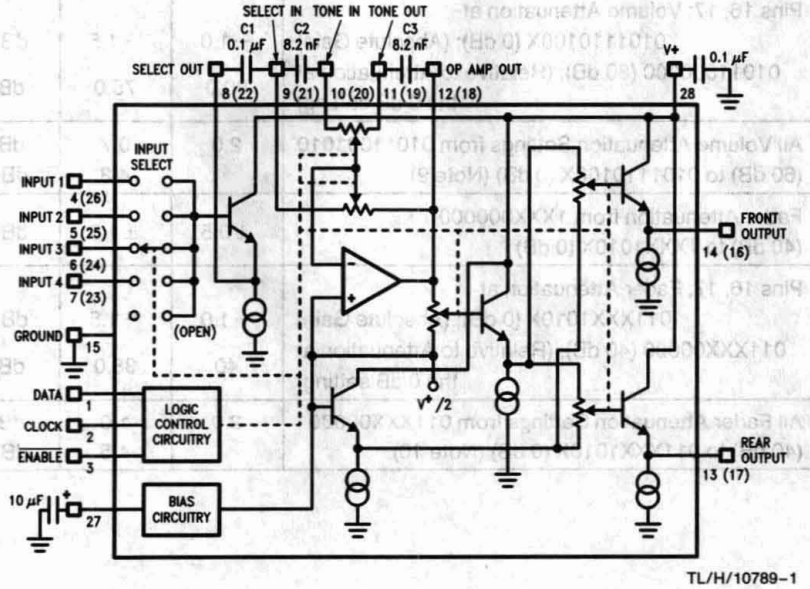
Features

- Low noise and distortion
- Four stereo inputs
- 40 volume levels including mute
- 20 fader levels
- All attenuators have a 2 dB of attenuation per step
- Front/back fade control
- External processor loop
- Only three external components per channel
- Serial programmable: standard MICROWIRE™ interface
- Single supply operation: 6V to 12V supply voltage
- Protection address (similar to DS8906)
- DC-coupled inputs
- Single supply operation

Applications

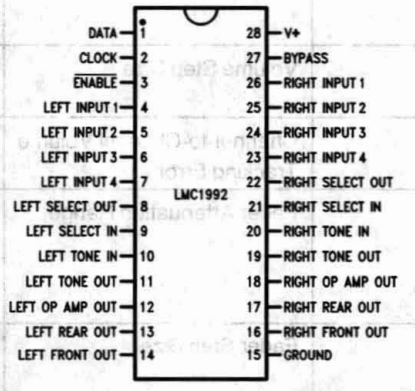
- Automotive audio systems
- Sound reinforcement systems
- Home entertainment—stereo television and music reproduction systems
- Electronic music (MIDI)

Block and Connection Diagrams



TL/H/10789–1

Left channel shown. Pin numbers in parentheses are for the right channel.



TL/H/10789–2

Order Number LMC1992CCN
See NS Package Number N28B

Absolute Maximum Ratings (Notes 1 and 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage ($V^+ - GND$)	15V
Voltage at Any Pin	GND − 0.2V to V^+ + 0.2V
Input Current at Any Pin (Note 3)	5 mA
Package Input Current (Note 3)	20 mA
Power Dissipation (Note 4)	500 mW
Junction Temperature	125°C
Storage Temperature	−65°C to +150°C
Lead Temperature	
N Package, Soldering, 10 sec.	+260°C
ESD Susceptibility (Note 5)	2000V
Pins 9, 10, 11, 19, 20, 21	850V

Operating Ratings (Notes 1 and 2)

Temperature Range	$T_{MIN} \le T_A \le T_{MAX}$
LMC1992CCN	$0°C \le T_A \le 70°C$
Supply Voltage Range ($V^+ - V^-$)	6V to 12V

Electrical Characteristics

The following specifications apply for $V^+ = 8V$, $f_{IN} = 1$ kHz, input signal applied to channel 1, volume = 0 dB, bass = 0 dB, treble = 0 dB, and faders = 0 dB unless otherwise specified. All limits $T_A = T_J = 25°C$.

Symbol	Parameter	Conditions	Typical (Note 6)	Limit (Note 7)	Units (Limit)
I_S	Supply Current			27.0	mA (max)
V_{IN}	Input Voltage	Clipping Level (1.0% THD), Select Out (Pins 8, 22)	2.3	2.0	V_{rms}(min)
V_{OUT}	Output Voltage	Clipping Level (1.0% THD), Outputs (Pins 13, 14, 16, 17)	1.2	0.65	V_{rms}(min)
THD	Total Harmonic Distortion	All Four Channels			
		Volume Attenuator at 0 dB, Input Level 0.3 V_{rms}	0.15	0.3	% (max)
		Volume Attenuator at −20 dB, Input Level 0.6 V_{rms}	0.03	0.1	% (max)
E_{nOUT}	Output Noise	All Four Channels CCIR/ARM Filter, $R_S = 0\Omega$	6.5	30.0	μV_{rms} (max)
E_{nOUT}	Output Noise	All Four Channels CCIR/ARM Filter, $R_S = 0\Omega$ Volume Attenuator = −80 dB	5.0	20.0	μV_{rms} (max)
R_{OUT}	DC Output Impedance	Pins 8, 22	100	150	Ω (max)
		Pins 13, 14, 16, 17	80	120	Ω (max)
R_{IN}	DC Input Impedance	Pins 4, 5, 6, 7, 23, 24, 25, 26	2		MΩ
	Volume Attenuator Range	Pins 16, 17; Volume Attenuation at 0101110100X (0 dB); (Absolute Gain)	−1.0	−1.5	dB (max)
		01011000000 (80 dB); (Relative to Attenuation at the 0 dB setting)	80.0	75.0	dB (min)
	Volume Step Size	All Volume Attenuation Settings from 01011001010 (60 dB) to 0101110100X (0 dB) (Note 9)	2.0	0.7 4.3	dB (min) dB (max)
	Channel-to-Channel Volume Tracking Error	Fader Attenuation from 1XXX000000 (40 dB) to 1XXX1010X (0 dB)	±0.5	±1.0	dB (max)
	Fader Attenuation Range	Pins 16, 17; Fader Attenuation at 011XXX1010X (0 dB); (Absolute Gain)	−1.0	−1.5	dB (max)
		011XXX00000 (40 dB); (Relative to Attenuation at the 0 dB setting)	40	38.0	dB (min)
	Fader Step Size	All Fader Attenuation Settings from 011XXX00000 (40 dB) to 011XXX1010X (0 dB) (Note 10)	2.0	1.0 4.5	dB (min) dB (max)

Electrical Characteristics The following specifications apply for $V^+ = 8V$, $f_{IN} = 1$ kHz, input signal applied to channel 1, volume = 0 dB, bass = 0 dB, treble = 0 dB, and faders = 0 dB unless otherwise specified. All limits $T_A = T_J = 25°C$. (Continued)

Symbol	Parameter	Conditions	Typical (Note 6)	Limit (Note 7)	Units (Limit)
	Bass Gain Range	f_{IN} = 100 Hz, Pins 14, 16	±12	±10.0	dB (min)
	Bass Tracking Error	f_{IN} = 100 Hz, Pins 14, 16	±0.1	±1.0	dB (max)
	Bass Step Size	f_{IN} = 100 Hz, Pins 14, 16 (Relative to Previous Level)	2.0	1.0 3.0	dB (min) dB (max)
	Treble Gain Range	f_{IN} = 10 kHz, Pins 14, 16	±12	±10.0	dB (min)
	Treble Tracking Error	f_{IN} = 10 kHz, Pins 14, 16	±0.1	±1.0	dB (max)
	Treble Step Size	f_{IN} = 10 kHz, Pins 14, 16 (Relative to Previous Level)	2.0	1.0 3.0	dB (min) dB (max)
	Frequency Response	−3 dB −0.3 dB (Relative to Signal Amplitude at 1 kHz)	450	 20	kHz kHz (min)
	Channel Separation	V_{IN} = 1.0 V_{rms}	97	70	dB (min)
	Input-Input Isolation	V_{IN} = 1.0 V_{rms} (Note 8)	90	70	dB (min)
PSRR	Power Supply Rejection Ratio	V^+ = 8 V_{DC}; 100 mV_{P-P}, 100 Hz Sinewave Applied to Pin 28	40	31	dB (min)
f_{CLK}	Clock Frequency		1.0	0.5	MHz (max)
$V_{IN(1)}$	Logic "1" Input Voltage		1.3	2.0	V (min)
$V_{IN(0)}$	Logic "0" Input Voltage		0.4	0.8	V (max)

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.

Note 2: All voltages are specified with respect to ground.

Note 3: When the input voltage (V_{IN}) at any pin exceeds the power supply voltages ($V_{IN} < V^-$ or $V_{IN} > V^+$) the absolute value of the current at that pin should be limited to 5 mA or less. The 20 mA package input current limits the number of pins that can exceed the power supply voltages with 5 mA current limit to four.

Note 4: The maximum power dissipation must be de-rated at elevated temperatures and is dictated by T_{JMAX}, ϕ_{JA}, and the ambient temperature T_A. The maximum allowable power dissipation is $PD = (T_{JMAX} - T_A)/\theta_{JA}$ or the number given in the Absolute Maximum Ratings, whichever is lower. For the LMC1992CCN, T_{JMAX} = 125°C, and the typical junction-to-ambient thermal resistance, when board mounted, is 67°C/W.

Note 5: Human body model; 100 pF discharged through a 1.5 kΩ resistor.

Note 6: Typicals are at T_J = 25°C and represent the most likely parametric norm.

Note 7: Limits are guaranteed to National's AOQL (Average Outgoing Quality Level).

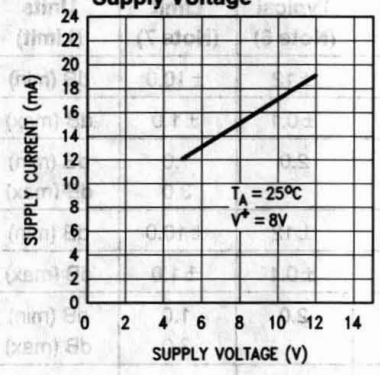
Note 8: The Input-Input Isolation is tested by driving one input and measuring the front outputs when the undriven inputs are selected.

Note 9: The Volume Step Size is defined as the change in attenuation between any two adjacent volume attenuation settings. The nominal Volume Step Size is 2 dB.

Note 10: The Fader Step Size is defined as the change in attenuation between any two adjacent fader attenuation settings. The nominal Volume Step Size is 2 dB.

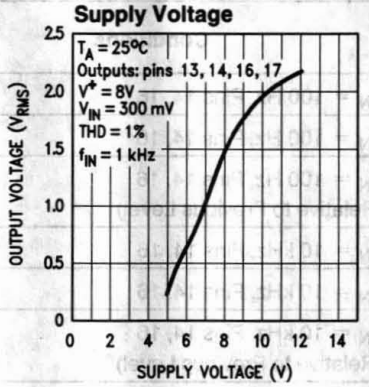
Typical Performance Characteristics

Quiescent Current vs Supply Voltage



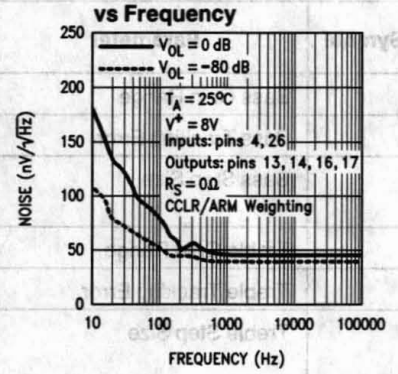
TL/H/10789-3

Maximum Output Swing vs Supply Voltage



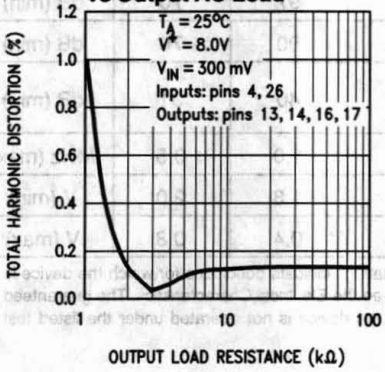
TL/H/10789-4

Output Noise Voltage vs Frequency



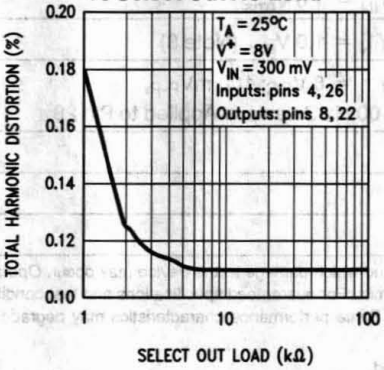
TL/H/10789-5

Total Harmonic Distortion vs Output AC Load



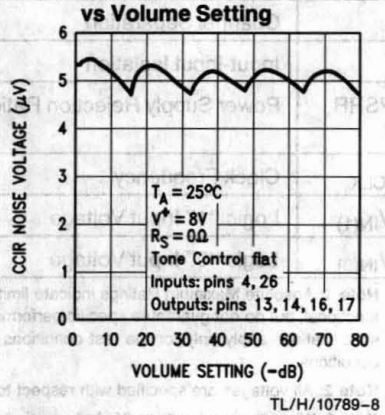
TL/H/10789-6

Total Harmonic Distortion vs Select Out AC Load



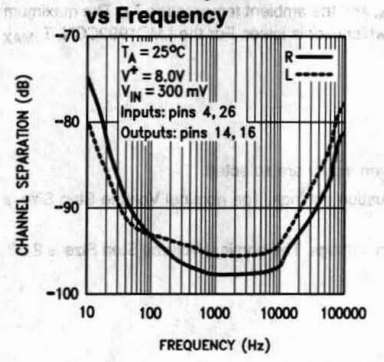
TL/H/10789-7

CCIR Output Noise Voltage vs Volume Setting



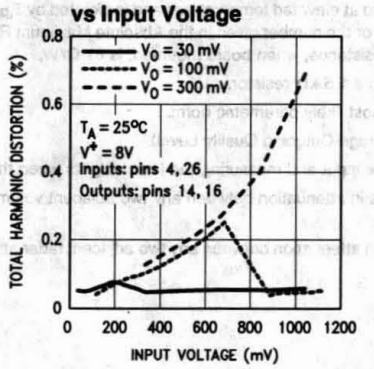
TL/H/10789-8

Channel Separation vs Frequency



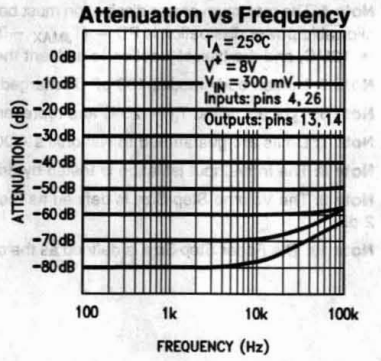
TL/H/10789-9

Total Harmonic Distortion vs Input Voltage



TL/H/10789-10

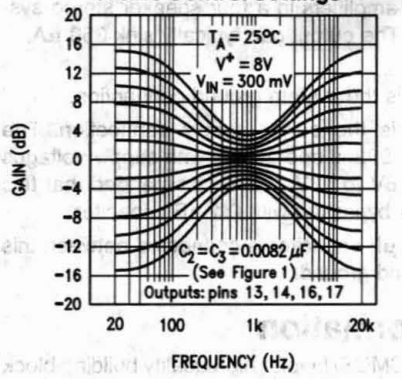
Attenuation vs Frequency



TL/H/10789-11

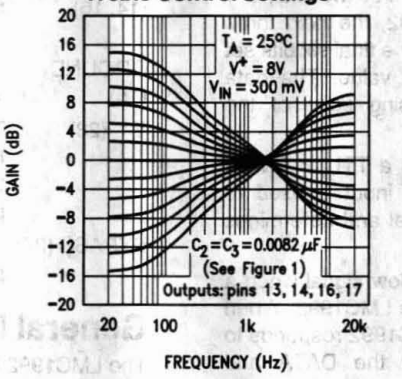
Typical Performance Characteristics (Continued)

Tone Control Response with Equal Bass and Treble Control Settings



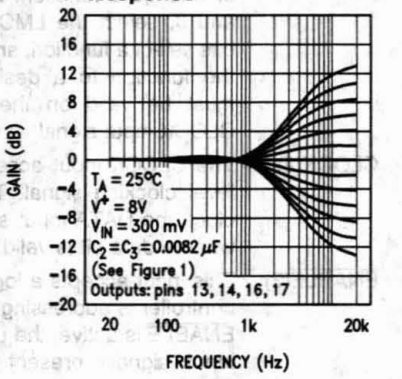
TL/H/10789–12

Tone Control Response with Reciprocal Bass and Treble Control Settings



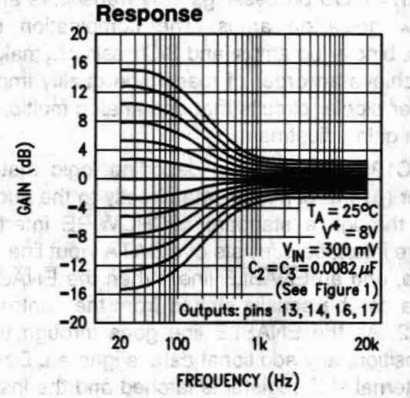
TL/H/10789–13

Treble Tone Control Response



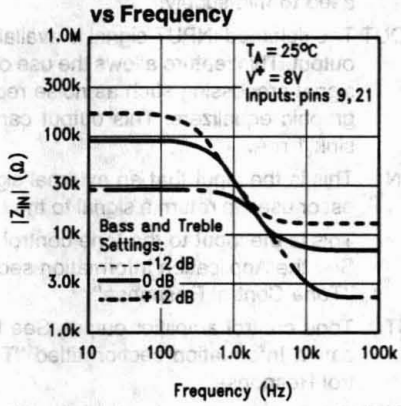
TL/H/10789–14

Bass Tone Control Response



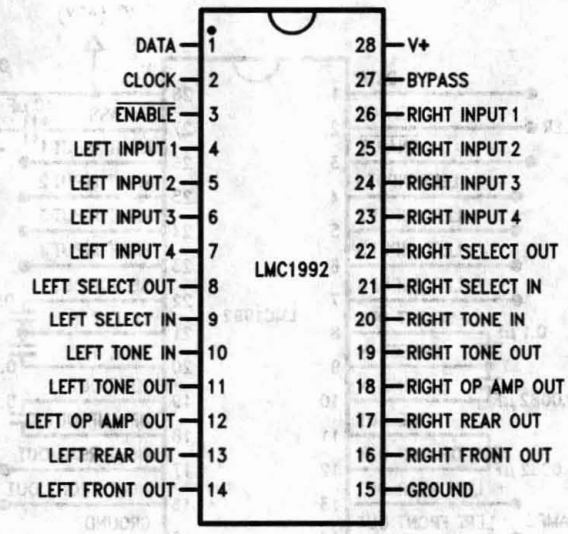
TL/H/10789–15

Select In Impedance vs Frequency



TL/H/10789–16

Connection Diagram



TL/H/10789–17

Pin Description

DATA(1) This is the serial data input for communications sent by a controller. The data rate has a maximum frequency of 500 kHz. The LMC1992 requires 11 bits of data to control or change a function: the first two bits, a 1 and 0, select the LMC1992, the next three bits select a function, and the final six bits set the function to a desired value. The data must be valid on the rising edge of the CLOCK input signal.

CLOCK(2) The CLOCK input accepts a TTL or CMOS level clocking signal. The input is used to clock the DATA input signal and determines when a data bit is valid.

$\overline{\text{ENABLE}}$(3) This input accepts a logic low signal when a controller is addressing the LMC1992. When $\overline{\text{ENABLE}}$ is active, the LMC1992 responds to input signals present on the DATA and CLOCK inputs.

INPUT 1–4 (4–7, 23–26) Four two-channel analog inputs are available on the LMC1992. These pins should be dc-biased to mid-supply.

SELECT OUT (8, 22) The selected INPUT signal is available at this output. This feature allows the use of external signal processing such as noise reduction or graphic equalizers. This output can typically sink 1 mA.

SELECT IN (9, 21) This is the input that an external signal processor uses to return a signal to the LMC1992.

TONE IN (10, 20) This is the input to the tone control amplifier. See the Application Information section titled "Tone Control Response".

TONE OUT (11, 19) Tone control amplifier output. See the Application Information section titled "Tone Control Response".

OP AMP OUT (12, 18) This output is used externally with the tone control capacitors. Internally, this output is applied to the volume attenuators.

REAR OUT (13, 17) This pin's output signal is intended for the rear amplifiers in a four speaker stereo system. The output can typically sink 350 μA.

FRONT OUT (14, 16) This pin's output signal is intended for the front amplifiers in a four speaker stereo system. The output can typically sink 350 μA.

GROUND (15) This is the system ground connection.

V^+ (28) This is the power supply connection. The LMC1992 is operational with supply voltages from 6V to 12V. It is recommended that this pin is bypassed with 0.1 μF capacitor.

BYPASS (27) A 10 μF capacitor is connected between this pin and ground.

General Information

The LMC1992 is a CMOS/bipolar high quality building block intended for high fidelity audio signal processing. It is designed for line level input signals (300 mV − 2V) and has a maximum gain of −1 dB. While the LMC1992 is manufactured with CMOS processing, NPN transistors are used to build low noise op amps. The combination of CMOS switches, bipolar op amps, and SiCr resistors make it possible to achieve an order of magnitude quality improvement over other bipolar circuits that use analog multipliers to accomplish gain adjustment.

The LMC1992 has internal decoding logic that allows a computer (μP) to communicate directly to the audio control circuitry through a standard MICROWIRE interface. This three-wire interface consists of a DATA input line, a CLOCK input line, and an $\overline{\text{ENABLE}}$ line. When the $\overline{\text{ENABLE}}$ line is low, data can be serially shifted from the controller to the LMC1992. As the $\overline{\text{ENABLE}}$ line goes through the low-to-high transition, any additional data is ignored. Data present in the internal shift register is latched and the instruction is executed.

Figure 1 shows the connection diagram of a typical LMC1992 application.

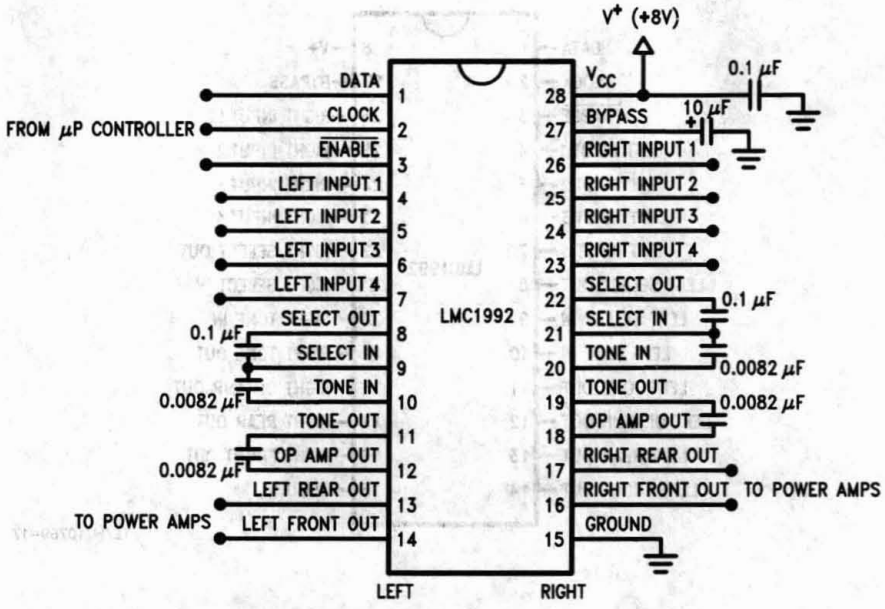


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FIGURE 1. Typical Connection Diagram

Applications Information

MINIMUM LOAD IMPEDANCE

The LMC1992 employs emitter-follower buffers at pins 8 and 22 (SELECT OUT), 13 and 14 (LEFT FRONT and REAR OUTPUTs), and 16 and 17 (RIGHT FRONT-and-REAR OUTPUTs) that buffer output signals. Typical bias current of 1 mA is used for the SELECT OUTPUT buffers and 350 μA for the LEFT-and-RIGHT, FRONT-and-REAR OUTPUT buffers.

The Electrical Specifications table lists a maximum input signal of 2.3 V_{rms} (3.25 V_{peak}) for 1% THD at the SELECT OUT pins. This distortion level is achieved when the minimum ac load impedance seen by the SELECT OUT pin is 3.25 kΩ (3.25V/1 mA). For the LEFT-and-RIGHT, FRONT-and-REAR OUTPUTs, the typical maximum output is 1.2 V_{rms} (1.55 V_{peak}). Therefore, the minimum load impedance is 4.43 kΩ (1.55 V/0.35 mA). Trying to use a lower impedance results in a clipped output signal. Therefore, *the chance of clipping can be greatly reduced and much lower distortion levels can be achieved by using load impedances that are an order of magnitude higher than shown here.*

For applications that require dc coupling and the INPUTs biased to $V^+/2$, the minimum load impedance will differ from that detailed in the above discussion. The emitter followers may be potentially operating at high currents because there is a dc voltage $V^+/2 - 0.7V$ at the SELECT OUT pins; dc resistance to ground will result in increased current flow. Latch-up may occur if the total emitter current exceeds 5 mA. This current is a combination of the emitter follower's 1 mA current source and 4 mA drawn by the external load. Therefore, to prevent this possibility, the minimum dc load impedance should be

$$\frac{V_{peak} + (V^+/2 - 0.7V)}{4\ mA} = 1638\Omega$$

$V_{peak} = 3.25V$

$V^+ = 8V$

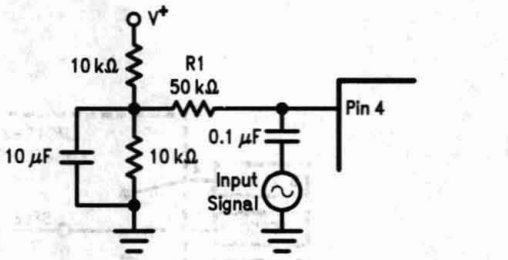
To allow for variations and part tolerances, 2.0 kΩ is a good choice for this minimum dc load impedance.

When dc coupling is used at the LEFT-and-RIGHT, FRONT-and-REAR OUTPUTs, the output emitter followers will be operating at a nominal dc voltage of $V^+/2 - 2(0.7V)$. Latch-up may occur if the total emitter current exceeds 1 mA. This current is a combination of the emitter follower's 0.35 mA current source and 0.65 mA drawn by the external load. Therefore, to prevent this possibility, the minimum dc load impedance should be

$$\frac{V_{peak} + (V^+/2 - 2(0.7V))}{0.65\ mA} = 9\ k\Omega$$

$V_{peak} = 3.25V$

$V^+ = 8V$



TL/H/10789–20

FIGURE 2. Input Bias Network

To allow for variations and part tolerances, 10 kΩ is a good choice for this minimum dc load impedance.

INPUT IMPEDANCE

For ac coupled input signals the input impedance value is determined by bias resistor R1, as shown in *Figure 2.* A directly coupled input signal will see an emitter follower's nominal input impedance of 2 MΩ.

The SELECT IN pins have an input impedance that varies with the BASS and TREBLE control settings. The input impedance is 96 kΩ at dc and 27 kΩ at 1 kHz when the controls are set at 0 dB. Minimum input impedance of 28 kΩ at dc and 24 kΩ at 1 kHz occurs when maximum boost is selected. At 10 kHz the minimum input impedance, with the tone controls flat, is 8 kΩ and, with the tone controls at maximum boost, is 3 kΩ.

STEREO SIGNAL INPUTS

When operating with a single supply voltage, the stereo signal inputs must be dc biased to one-half of the supply voltage, as shown in *Figure 2.* As an example, with a supply voltage of 8V, all signal sources should have a dc bias of 4V. The maximum input signal level of 6.5 V_{p-p} (for 1% THD) would then swing from 0.75V to 7.25V. Input-to-input crosstalk can be minimized by using a separate dc bias circuit for each stereo input pair.

EXTERNAL SIGNAL PROCESSING

The signal present at the selected input will be available at the SELECT OUT pins 8 (left) and 22 (right). The dc bias voltage at those pins will be one base-emitter voltage, approximately 0.7 V_{dc}, below the source because of the internal emitter follower. Therefore, if the selected input has a bias of 4.0 V_{dc} the dc component at pins 8 and 22 will be about 3.3 V_{dc}.

The LMC1992's SELECT OUT emitter followers allow additional signal sources using emitter follower outputs (such as multiple LMC1992s) to be "wired-ORed" together. When this feature is in use, the input channel of the LMC1992 not in use should be set to "open" input codes 01000XX0000 or 01000XX011X.

Applications Information (Continued)

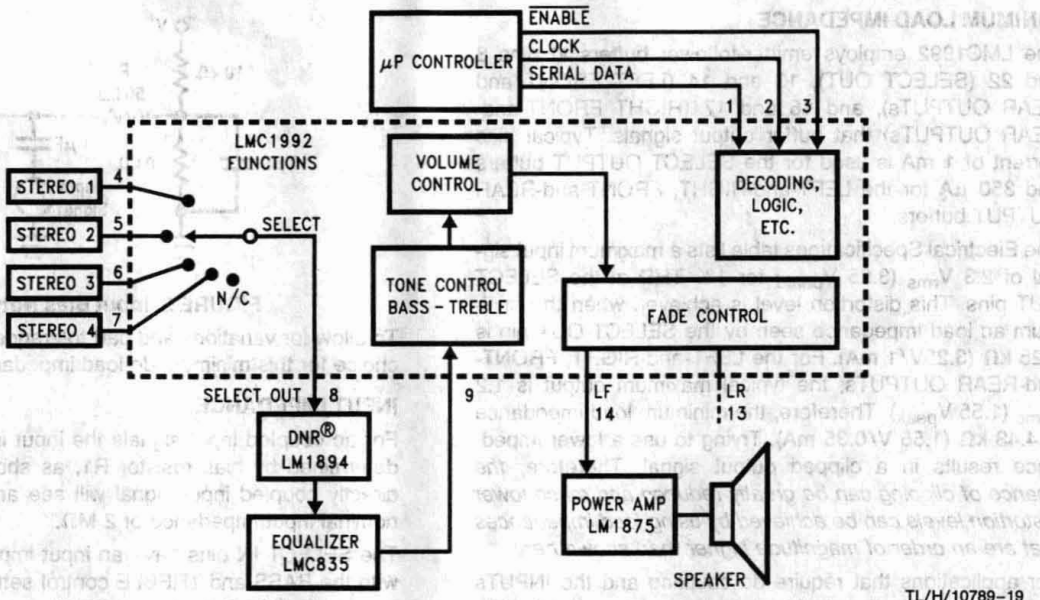


FIGURE 3. System Block Diagram Showing Inclusion of DNR® Noise Reduction (LM1894) and Equalizer (LMC835) (One Channel Only—LMC1992)

The SELECT OUT pins (8 and 22) enable greater system design flexibility by providing a means to implement an external processing loop. This loop can be used for noise reduction circuits such as DNR (LM1894) or mulit-band graphic equalizers (LMC835). It is important to ensure that if both are used, the noise reduction circuitry precede the equalization circuits. Failure to do so will result in improper operation of the noise reduction circuits. The system shown in *Figure 3* utilizes the external loop to include DNR and a multi-band equalizer.

AUDIO MUTE

A mute function with attenuation of 100 dB is possible with the volume control set to −80 dB and the INPUT select code set to 01000XX0000 (open circuit).

TONE CONTROL RESPONSE

Base and treble tone controls are included in the LMC1992. The tone controls use just two external capacitors for each stereo channel. Each has a corner frequency determined by the value of C2 and C3 *(Figure 4)* and internal resistors in the feedback loop of the internal tone amplifier. The maximum amplitude boost or cut is determined by the data sent to the LMC1992 (see Table I).

The typical tone control response shown in the Typical Performance Curves were generated with C2 = C3 = 0.0082 μF and show the response for each step. When modifying the tone control response it is important to note that the ratio of C3 and C2 sets the mid-frequency gain. Symmetrical tone response is achieved when C2 = C3. However, with C2 = 2(C3) and the tone controls set to "flat", the frequency response will be flat at 20 Hz and 20 kHz, and +6 dB at 1 kHz.

The frequency where a tone control begins to deviate from a flat response will be referred to as the turn-over frequency. With C = C2 = C3, the LMC1992's treble turn-over frequency is nominally

$$f_{TT} = \frac{1}{2\pi C(14.2\ k\Omega)}$$

The base turn-over frequency is nominally

$$f_{BT} = \frac{1}{2\pi C(27.7\ k\Omega)}$$

when maximum boost is chosen. The inflection points (the frequencies where the boost or cut is within 3 dB of the final value) are for treble and bass

$$f_{TI} = \frac{1}{2\pi C(2.3\ k\Omega)}$$

$$f_{BI} = \frac{1}{2\pi C(164.1\ k\Omega)}$$

Applications Information (Continued)

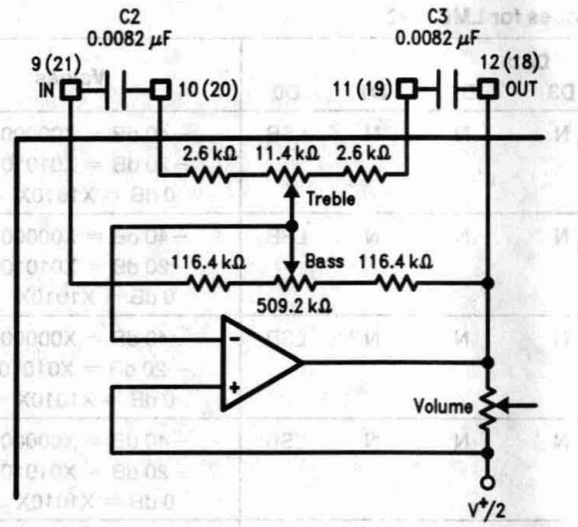


FIGURE 4. The Tone Control Amplifier

Increasing the values of C2 and C3 decreases the turnover and inflection frequencies: i.e., the Tone Control Response Curves shown in Typical Performance Curves will shift left when C2 and C3 are increased and shift right when C2 and C3 are decreased. With C2 = C3 = 0.0082, 2 dB steps are achieved at 100 Hz and 10 kHz. Changing C2 and C3 to 0.01 µF shifts the 2 dB per step frequency to 72 Hz and 8.3 kHz. If the tone control capacitors' size is decreased these frequencies will increase. With C2 = C3 = 0.0068 µF the 2 dB steps take place at 130 Hz and 11.2 kHz.

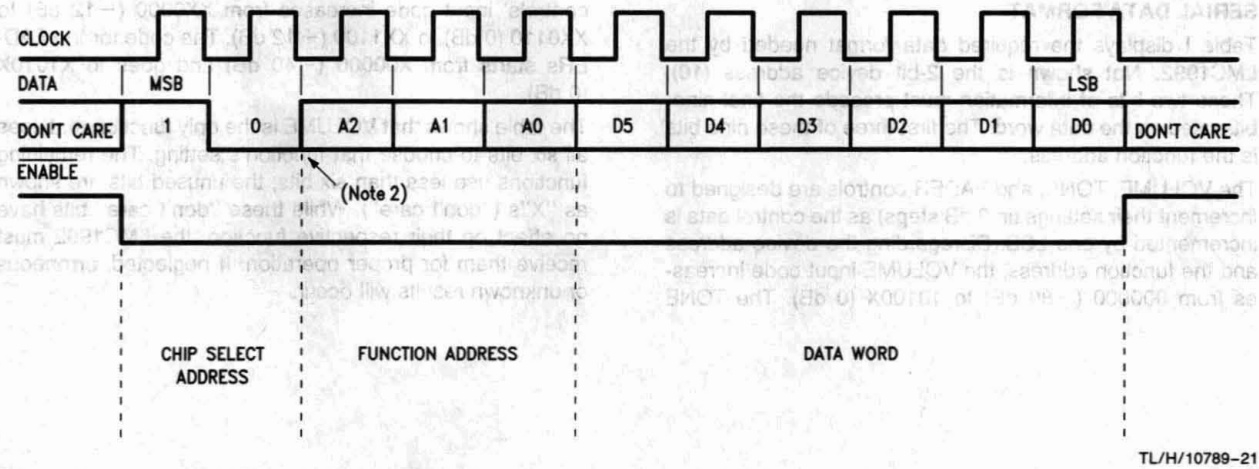
FADER FUNCTION

The four fader functions are all independently adjustable and therefore no balance control is needed. Emulating a balance control is accomplished through software by simultaneously changing a channel's front and rear faders by equal amounts. To satisfy normal balance requirements the faders have an attenuation range of 40 dB.

SERIAL COMMUNICATION INTERFACE

Figure 5 shows the LMC1992's timing diagram for its three wire MICROWIRE interface. A controller's data stream can be any length; once the correct device address is received by the LMC1992, any number of data bits can be sent; the last nine bits occurring before $\overline{\text{ENABLE}}$ goes high are used by the LMC1992. The first two bits in a valid data stream are decoded and used as device address bits. The LMC1992 uses a unique address of 1,0. The LMC1992 will not respond to information on the DATA line if any other address is used. This allows other MICROWIRE serially programmable devices to share the same three-wire communication bus. When $\overline{\text{ENABLE}}$ goes high, any further serial data is ignored and the contents of the shift register is transferred to the data latches. Only when information is received by the data latches do any function or setting changes take place. The first three of nine bits select one of the LMC1992s functions. The remaining six bits set the selected function to the desired value or position.

A data bit is accepted as valid and clocked into an internal shift register on each rising edge of the signal appearing at the LMC1992s CLOCK input pin. Proper data interpretation and operation is ensured when $\overline{\text{ENABLE}}$ makes its falling transition during the time when CLOCK is low. Erroneous operation will result if the $\overline{\text{ENABLE}}$ signal makes its falling transition at any other time.



Note 1: Negative transition on $\overline{\text{ENABLE}}$ clears previous address. Clock must be low during transition.

Note 2: Additional don't care states may be inserted here for ease of programming. (Optional.)

Note 3: Positive transition on $\overline{\text{ENABLE}}$ latches in new data if the LMC1992 has been addressed. Clock can either be high or low during transition.

FIGURE 5. Clocking Data into the Standard MICROWIRE Interface (Minimum Number of Bits in Data Stream)

Applications Information (Continued)

TABLE I. Programming Codes for LMC1992

Address			Function	Data						Values
A2	A1	A0		D5	D4	D3	D2	D1	D0	
1	1	1	Left Rear Fader	X	MSB	N	N	N	LSB	−40 dB = X00000 −20 dB = X01010 0 dB = X1010X
1	1	0	Right Rear Fader	X	MSB	N	N	N	LSB	−40 dB = X00000 −20 dB = X01010 0 dB = X1010X
1	0	1	Left Front Fader	X	MSB	N	N	N	LSB	−40 dB = X00000 − 20 dB = X01010 0 dB = X1010X
1	0	0	Right Front Fader	X	MSB	N	N	N	LSB	−40 dB = X00000 −20 dB = X01010 0 dB = X1010X
0	1	1	Volume	MSB	N	N	N	N	LSB	−80 dB = 000000 −40 dB = 010100 0 dB = 10100X
0	1	0	Treble	X	X	MSB	N	N	LSB	−12 dB = XX0000 FLAT = XX0110 +12 dB = XX1100
0	0	1	Bass	X	X	MSB	N	N	LSB	−12 dB = XX0000 FLAT = XX0110 +12 dB = XX1100
0	0	0	Input Select	X	X	0	MSB	N	LSB	OPEN = XX0000 INPUT1 = XX0001 INPUT2 = XX0010 INPUT3 = XX0011 INPUT4 = XX0100

Note 1: All attenuators 2 dB/step.

Note 2: Tone controls 2 dB/step @ 100 Hz and 10 kHz.

Note 3: Use of data that deviates from the values shown in the table may result in erroneous results.

SERIAL DATA FORMAT

Table I displays the required data format needed by the LMC1992. Not shown is the 2-bit device address (10). These two bits of information must precede the final nine-bits used as the data word. The first three of these nine bits is the function address.

The VOLUME, TONE, and FADER controls are designed to increment their settings (in 2 dB steps) as the control data is incremented by one LSB. Disregarding the device address and the function address, the VOLUME input code increases from 000000 (−80 dB) to 10100X (0 dB). The TONE controls' input code increases from XX0000 (−12 dB) to XX0110 (0 dB) to XX1100 (+12 dB). The code for the FADERs starts from X00000 (−40 dB) and goes to X1010X (0 dB).

The table shows that VOLUME is the only function that uses all six bits to choose that function's setting. The remaining functions use less than six bits; the unused bits are shown as "X"s ("don't care"). While these "don't care" bits have no effect on their respective function, the LMC1992 must receive them for proper operation. If neglected, erroneous or unknown results will occur.

Applications Information (Continued)

DATA TRANSFER EXAMPLE

The following routines, based on the flowchart shown in *Figure 6,* are examples of COPS™ microcontroller instruction code that can be used to control the LMC1992 (see National Semiconductor's COPS Microcontrollers Databook for more information). These routines arbitrarily select COPS register 0 for I/O purposes. When these routines are entered, it is assumed that chip select is high, SK (clock) is low, and SO (data) is low. These routines exit with chip select high and SK and SO low. Output port G0 is arbitrarily chosen to send the chip select signal to the LMC1992.

The 11 data bits needed to control the LMC1992 are assumed to be in the 4-bit registers, 13–15, with the 4 MSBs in register 13. With this configuration there is an extra bit for a data stream that is 12 bits long. As previously mentioned, there can be any number of extra bits between the device address and the function address.

DATA TRANSFER ROUTINE 1

This general purpose routine handles all the overhead except loading data into registers 13–15. It sends the data according to the conditions discussed above. The data will be lost at the conclusion of the routine. This routine consumes only 17 ROM memory locations.

```
OUT1:  LBI   0,13   ;POINT TO START OF DATA
                    ;WORD
       SC           ;SET C TO ENABLE SK CLOCK
       OGI   14     ;SELECT EXTERNAL DEVICE G0
                    ;= 0
       LEI   8      ;ENABLE SHIFT REGISTER
                    ;OUTPUT
SEND:  LD
       XAS          ;DATA TRANSMISSION LOOP
       XIS          ;TURN-ON CLOCK
       JP    SEND
       RC
       OGI   15     ;DE-SELECT EXTERNAL
                     DEVICE
       LEI   0      ;SET SO TO 0
       RET
```

DATA TRANSFER ROUTINE 2

This routine performs the same function as routine 1 while preserving the contents of the data registers. This routine takes only 21 ROM memory locations.

```
OUT1:  LBI   0,13   ;POINT TO START OF DATA
                    ;WORD
       SC           ;SET C TO ENABLE SK CLOCK
       OGI   14     ;SELECT EXTERNAL DEVICE
                    G0 ;=0
       LEI   8      ;ENABLE SHIFT REGISTER
                    ;OUTPUT
       JP    SEND2
SEND1: XAS
SEND2: LD           ;DATA TRANSMISSION LOOP
       XIS          ;TURN-ON CLOCK
       JP    SEND1
       XAS          ;SEND LAST DATA
       RC           ;WAIT 4 CYCLES - DATA
                    ;GOING OUT
       CLRA
       NOP
       XAS          ;TURN SK CLOCK OFF
       OGI   15     ;DE-SELECT DEVICE
       LEI   0      ;SET SO TO 0
       RET
```

Applications Information (Continued)

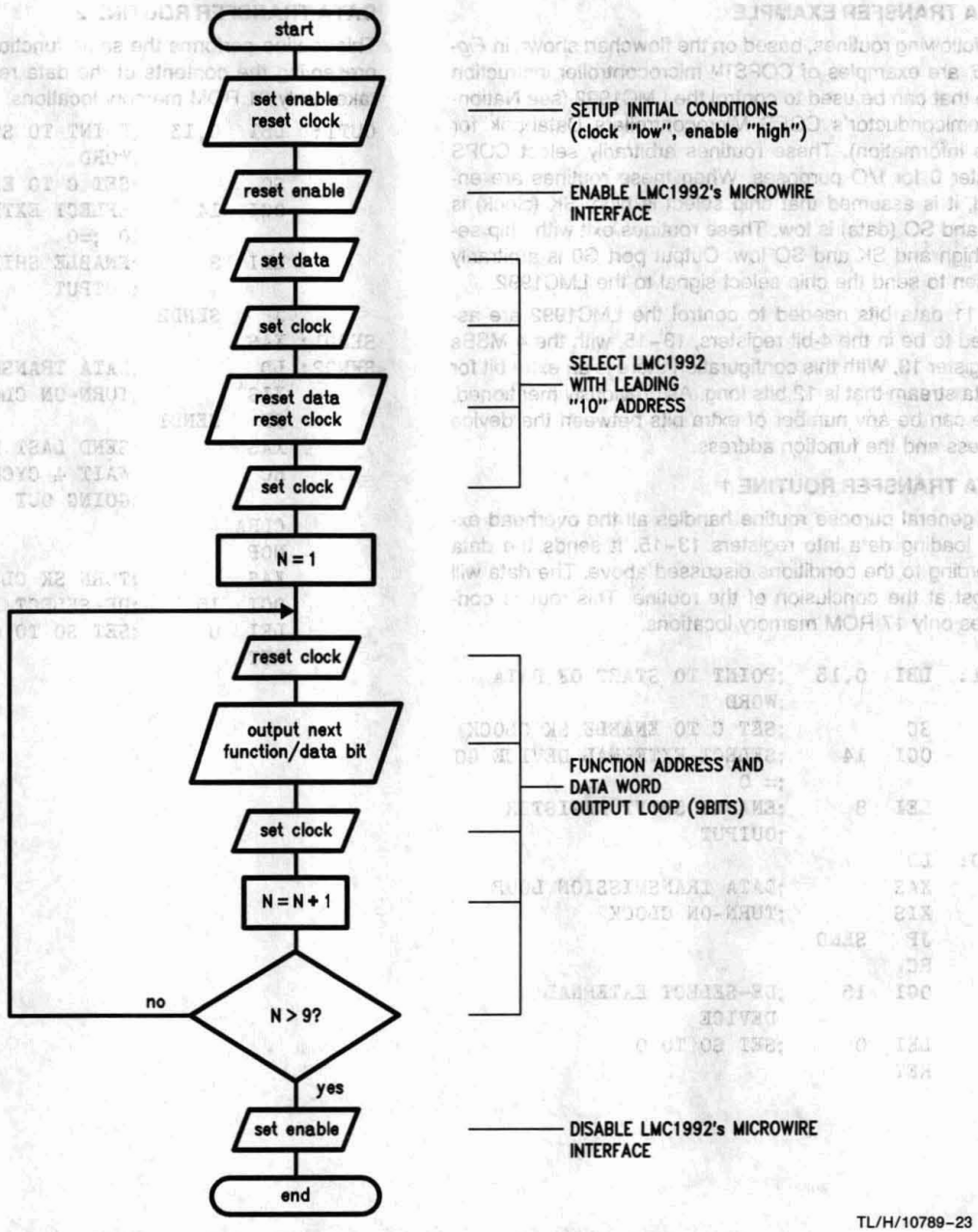


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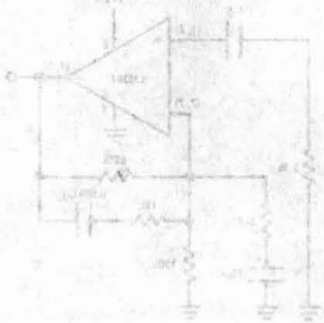
FIGURE 6. General Data Transmission Flowchart to Send Serial Data to the LMC1992's MICROWIRE Compatible Digital Inputs

National Semiconductor

Audio Op Amp Selection Guide

Part Number	Description Precision Op Amp	Input Referred Noise Voltage	THD	Slew Rate	GBW	PSRR	Supply Range	Single/ Dual/ Quad	Package (Pin Count)
LM833	Dual Audio Amplifier	4.5 nV/$\sqrt{Hz}$	0.002%	7V/μs	15 MHz	100 dB	±18V	Dual	SO(8), Dip(8)
LM837	Quad Audio Amplifier	4.5 nV/$\sqrt{Hz}$	0.0015%	10V/μs	25 MHz	100 dB	±18V	Quad	SO(14), Dip(14)
LF347	Wide Bandwidth JFET	20 nV/$\sqrt{Hz}$	0.02%	13V/μs	4 MHz	100 dB	±18V	Quad	Dip(14), SO(14)
LF351	Wide Bandwidth JFET	25 nV/$\sqrt{Hz}$	0.02%	13V/μs	4 MHz	100 dB	±18V	Single	SO(8), Dip(8)
LF353	Dual LF351	16 nV/$\sqrt{Hz}$	0.02%	13V/μs	4 MHz	100 dB	±18V	Dual	SO(14), Dip(14)
LF411	Low Offset, Low Drift JFET	25 nV/$\sqrt{Hz}$	0.02%	15V/μs	3 MHz	100 dB	±18V	Single	Dip(8)
LF412	Dual LF411	25 nV/$\sqrt{Hz}$	0.02%	15V/μs	3 MHz	100 dB	±18V	Dual	Dip(8)
LF444	Low Power JFET Quad	35 nV/$\sqrt{Hz}$	0.02%	1V/μs	1 MHz	100 dB	±18V	Quad	Dip(14), SO(14)
LM6142	High-Speed/Low Power Dual	16 nV/$\sqrt{Hz}$	0.03%	15V/μs	10 MHz	87 dB	+1.8V to 24V	Dual	Dip(8), SO(8)
LM6144	High-Speed/Low-Power Quad	16 nV/$\sqrt{Hz}$	0.03%	15V/μs	10 MHz	87 dB	+1.8V to 24V	Quad	Dip(14), SO(14)



National Semiconductor

LM387/LM387A Low Noise Dual Preamplifier

General Description

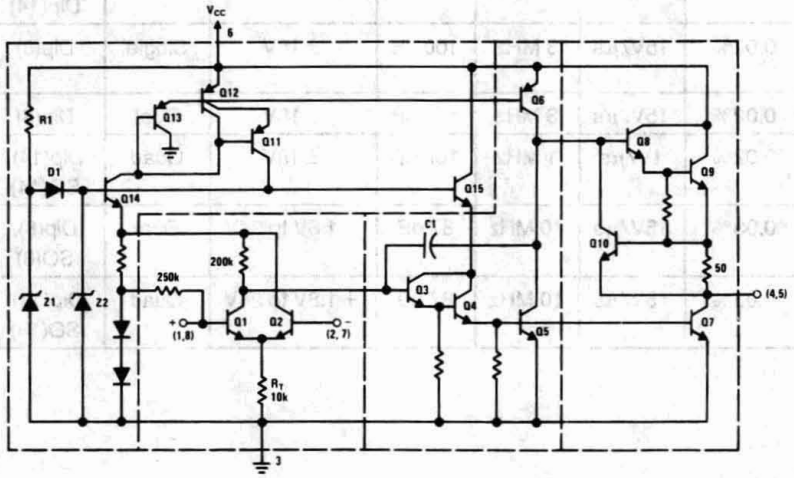
The LM387 is a dual preamplifier for the amplification of low level signals in applications requiring optimum noise performance. Each of the two amplifiers is completely independent, with an internal power supply decoupler-regulator, providing 110 dB supply rejection and 60 dB channel separation. Other outstanding features include high gain (104 dB), large output voltage swing (V_{CC} − 2V)p-p, and wide power bandwidth (75 kHz, 20 Vp-p). The LM387A is a selected version of the LM387 that has lower noise in a NAB tape circuit, and can operate on a larger supply voltage. The LM387 operates from a single supply across the wide range of 9V to 30V, the LM387A operates on a supply of 9V to 40V.

The amplifiers are internally compensated for gains greater than 10. The LN387, LM387A is available in an 8-lead dual-in-line package. The LM387, LM387A is biased like the LM381. See AN-64 and AN-104.

Features

- Low noise — 1.0 μV total input noise
- High gain — 104 dB open loop
- Single supply operation
- Wide supply range LM387 — 9 to 30V
  LM387A — 9 to 40V
- Power supply rejection — 110 dB
- Large output voltage swing (V_{CC} − 2V)p-p
- Wide bandwidth 15 MHz unity gain
- Power bandwidth 75 kHz, 20 Vp-p
- Internally compensated
- Short circuit protected
- Performance similar to LM381

Schematic and Connection Diagrams



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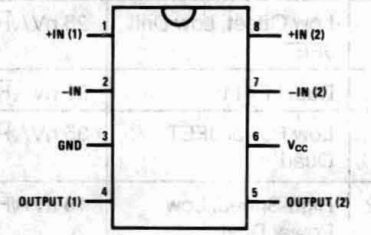
Dual-In-Line Package

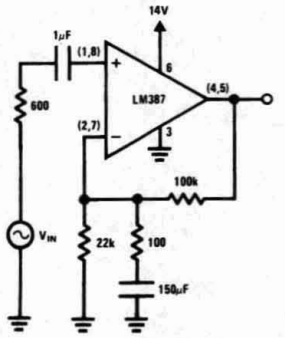


TL/H/7845–2

Top View

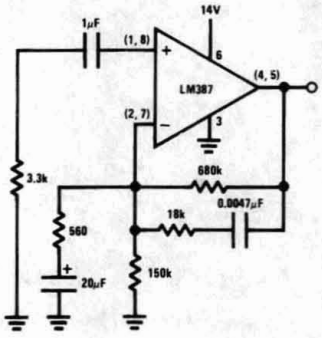
Order Number LM387N or LM387AN
See NS Package Number N08E

Typical Applications



TL/H/7845–3

FIGURE 1. Flat Gain Circuit (A_V = 1000)



TL/H/7845–4

FIGURE 2. NAB Tape Circuit

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage
- LM387 +30V
- LM387A +40V

Power Dissipation (Note 1)	1.5W
Operating Temperature Range	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec.)	260°C

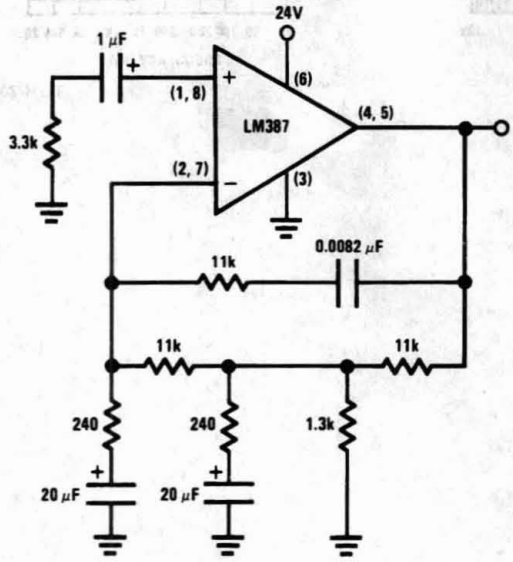
Electrical Characteristics $T_A = 25°C$, $V_{CC} = 14V$, unless otherwise stated

Parameter	Conditions	Min	Typ	Max	Units
Voltage Gain	Open Loop, f = 100 Hz		160,000		V/V
Supply Current	LM387, V_{CC} 9V–30V, $R_L = \infty$ LM387A, V_{CC} 9V–40V, $R_L = \infty$		10 10		mA mA
Input Resistance Positive Input Negative Input		50	 100 200		 kΩ kΩ
Input Current Negative Input			0.5	3.1	μA
Output Resistance	Open Loop		150		Ω
Output Current	Source Sink		8 2		mA mA
Output Voltage Swing	Peak-to-Peak		$V_{CC}-2$		V
Unity Gain Bandwidth			15		MHz
Large Signal Frequency Response	20 Vp-p ($V_{CC} > 24V$), THD ≤ 1%		75		kHz
Maximum Input Voltage	Linear Operation			300	mVrms
Supply Rejection Ratio Input Referred	f = 1 kHz		110		dB
Channel Separation	f = 1 kHz	40	60		dB
Total Harmonic Distortion	60 dB Gain, f = 1 kHz		0.1	0.5	%
Total Equivalent Input Noise (Flat Gain Cricuit)	10 Hz–10,000 Hz LM387 *Figure 1*		1.0	1.2	μVrms
Output Noise NAB Tape Playback Circuit Gain of 37 dB	Unweighted LM387A *Figure 2*		400	700	μVrms

Note 1: For operation in ambient temperatures above 25°C, the device must be derated based on a 150°C maximum junction temperature and a thermal resistance of 80°C/W junction to ambient.

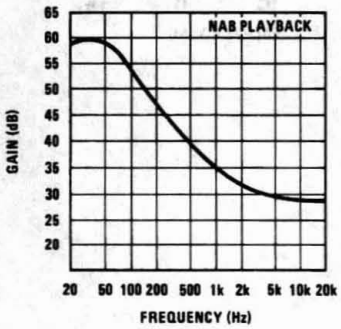
Typical Applications (Continued)

Two-Pole Fast Turn-ON NAB Tape Preamplifier



TL/H/7845–5

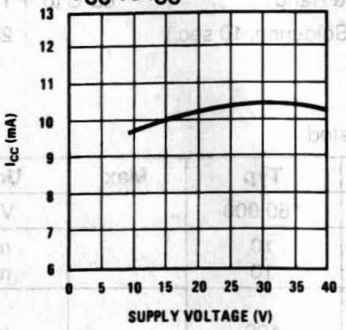
Frequency Response of NAB Circuit of Figure 2



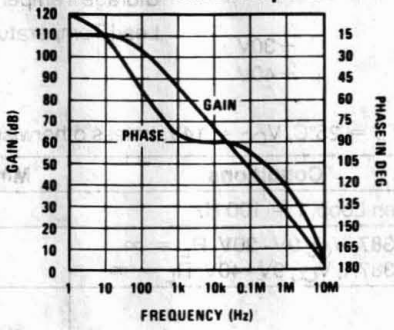
TL/H/7845–6

Typical Performance Characteristics

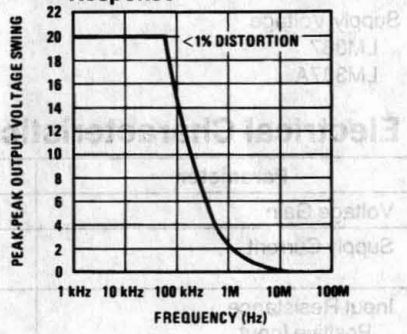
V_{CC} vs I_{CC}



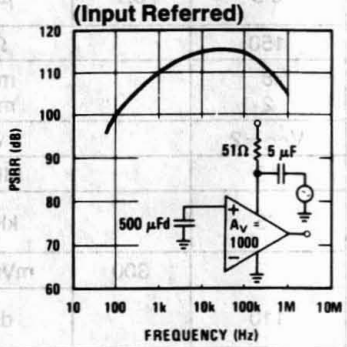
Gain and Phase Response



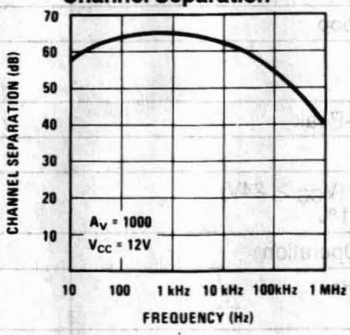
Large Signal Frequency Response



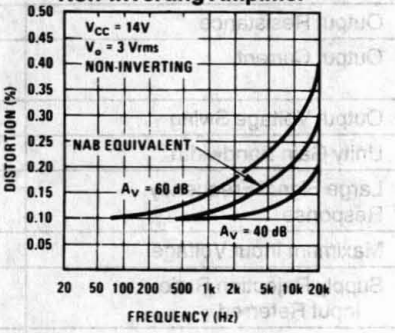
PSRR vs Frequency (Input Referred)



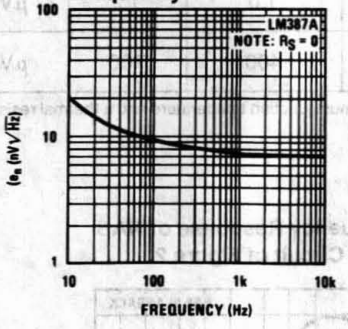
Channel Separation



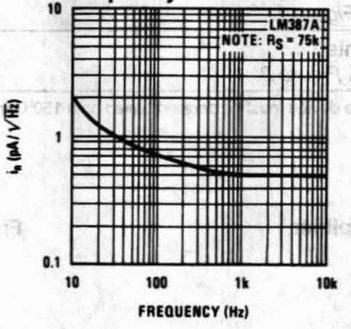
Distortion vs Frequency Non-Inverting Amplifier



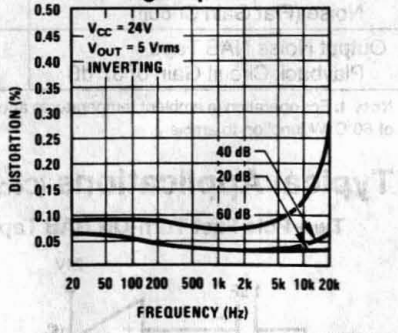
Noise Voltage vs Frequency



Noise Current vs Frequency



Distortion vs Frequency Inverting Amplifier



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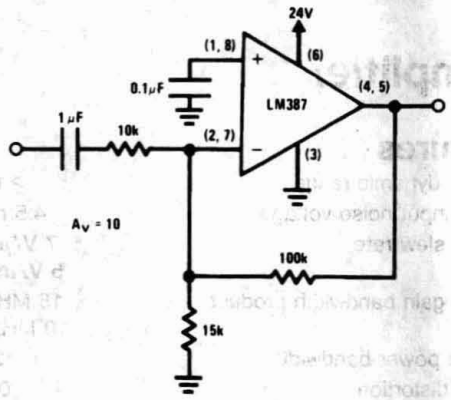
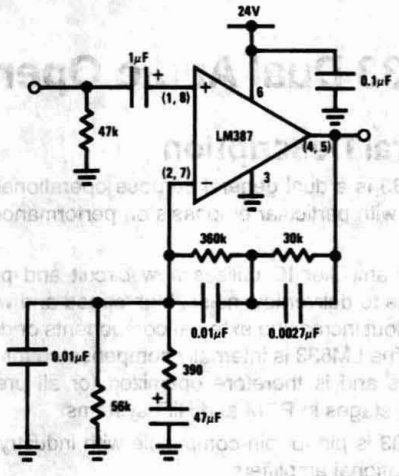
Typical Applications (Continued)

Inverting Amplifier Ultra-Low Distortion



TL/H/7845–8

Typical Magnetic Phono Preamplifier



TL/H/7845–9

National Semiconductor

LM833 Dual Audio Operational Amplifier

General Description

The LM833 is a dual general purpose operational amplifier designed with particular emphasis on performance in audio systems.

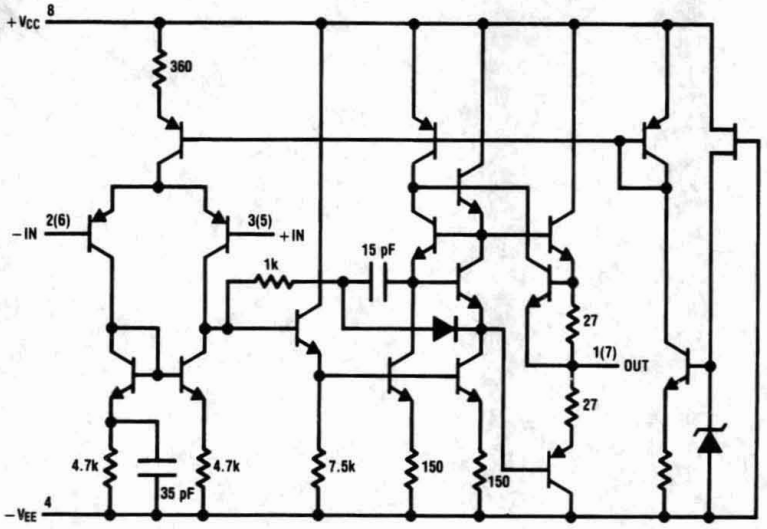
This dual amplifier IC utilizes new circuit and processing techniques to deliver low noise, high speed and wide bandwidth without increasing external components or decreasing stability. The LM833 is internally compensated for all closed loop gains and is therefore optimized for all preamp and high level stages in PCM and HiFi systems.

The LM833 is pin-for-pin compatible with industry standard dual operational amplifiers.

Features

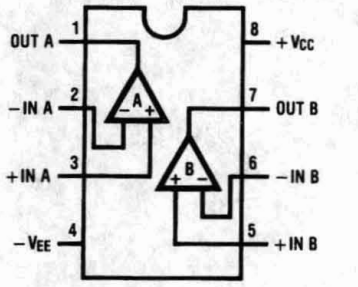
■ Wide dynamic range	>140 dB
■ Low input noise voltage	4.5 nV/√Hz
■ High slew rate	7 V/μs (typ) 5 V/μs (min)
■ High gain bandwidth product	15 MHz (typ) 10 MHz (min)
■ Wide power bandwidth	120 kHz
■ Low distortion	0.002%
■ Low offset voltage	0.3 mV
■ Large phase margin	60°

Schematic Diagram (1/2 LM833)



TL/H/5218–1

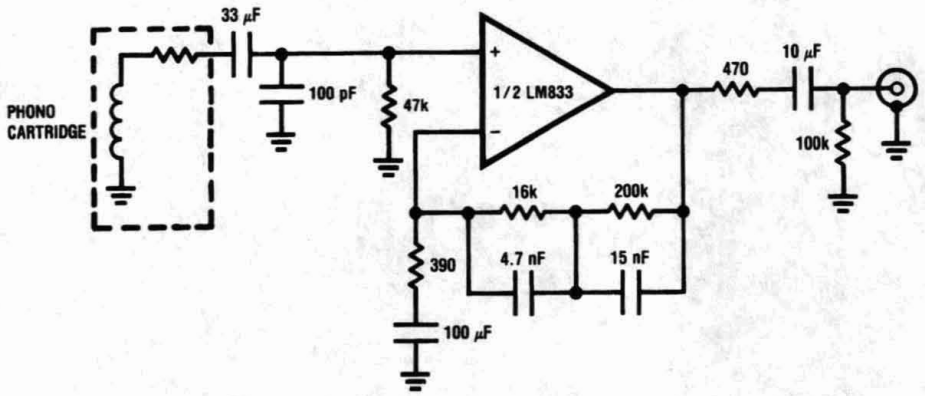
Connection Diagram



TL/H/5218–2

Order Number LM833M or LM833N
See NS Package Number M08A or N08E

Typical Application RIAA Preamp



TL/H/5218–3

A_v = 35 dB — f = 1 kHz
E_n = 0.33 μV — A Weighted
S/N = 90 dB — A Weighted, V_{IN} = 10 mV @ f = 1 kHz

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	$V_{CC}-V_{EE}$	36V
Differential Input Voltage (Note 1)	V_{ID}	±30V
Input Voltage Range (Note 1)	V_{IC}	±15V
Power Dissipation (Note 2)	P_D	500 mW
Operating Temperature Range	T_{OPR}	−40 ~ 85°C
Storage Temperature Range	T_{STG}	−60 ~ 150°C

Soldering Information

Dual-In-Line Package	
Soldering (10 seconds)	260°C
Small Outline Package	
Vapor Phase (60 seconds)	215°C
Infrared (15 seconds)	220°C

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.

ESD tolerance (Note 3) 1600V

DC Electrical Characteristics (T_A = 25°C, V_S = ±15V)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{OS}	Input Offset Voltage	R_S = 10Ω		0.3	5	mV
I_{OS}	Input Offset Current			10	200	nA
I_B	Input Bias Current			500	1000	nA
A_V	Voltage Gain	R_L = 2 kΩ, V_O = ±10V	90	110		dB
V_{OM}	Output Voltage Swing	R_L = 10 kΩ R_L = 2 kΩ	±12 ±10	±13.5 ±13.4		V V
V_{CM}	Input Common-Mode Range		±12	±14.0		V
CMRR	Common-Mode Rejection Ratio	V_{IN} = ±12V	80	100		dB
PSRR	Power Supply Rejection Ratio	V_S = 15~5V, −15~−5V	80	100		dB
I_Q	Supply Current	V_O = 0V, Both Amps		5	8	mA

AC Electrical Characteristics (T_A = 25°C, V_S = ±15V, R_L = 2 kΩ)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
SR	Slew Rate	R_L = 2 kΩ	5	7		V/μs
GBW	Gain Bandwidth Product	f = 100 kHz	10	15		MHz

Design Electrical Characteristics (T_A = 25°C, V_S = ±15V)

The following parameters are not tested or guaranteed.

Symbol	Parameter	Conditions	Typ	Units
$\Delta V_{OS}/\Delta T$	Average Temperature Coefficient of Input Offset Voltage		2	μV/°C
THD	Distortion	R_L = 2 kΩ, f = 20~20 kHz V_{OUT} = 3 Vrms, A_V = 1	0.002	%
e_n	Input Referred Noise Voltage	R_S = 100Ω, f = 1 kHz	4.5	nV/√Hz
i_n	Input Referred Noise Current	f = 1 kHz	0.7	pA/√Hz
PBW	Power Bandwidth	V_O = 27 V_{pp}, R_L = 2 kΩ, THD ≤ 1%	120	kHz
f_U	Unity Gain Frequency	Open Loop	9	MHz
ϕ_M	Phase Margin	Open Loop	60	deg
	Input Referred Cross Talk	f = 20~20 kHz	−120	dB

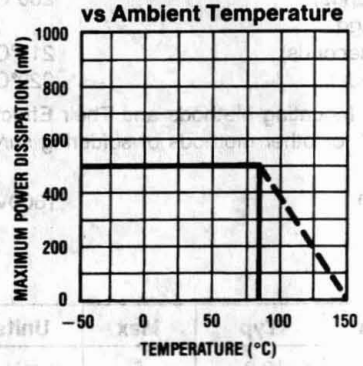
Note 1: If supply voltage is less than ±15V, it is equal to supply voltage.

Note 2: This is the permissible value at T_A ≤ 85°C.

Note 3: Human body model, 1.5 kΩ in series with 100 pF.

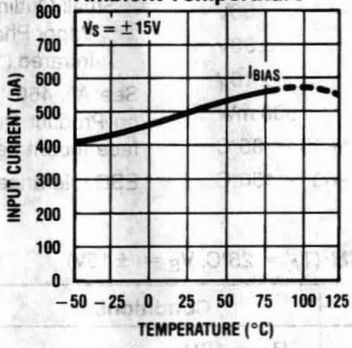
Typical Performance Characteristics

Maximum Power Dissipation vs Ambient Temperature



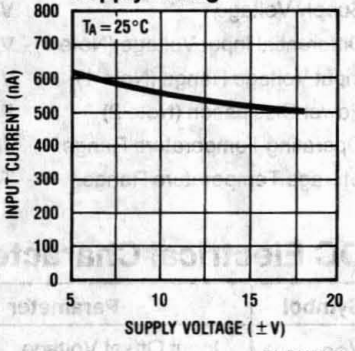
TL/H/5218–4

Input Bias Current vs Ambient Temperature



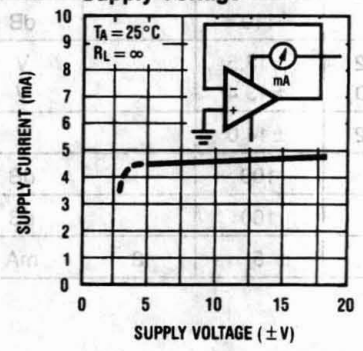
TL/H/5218–5

Input Bias Current vs Supply Voltage



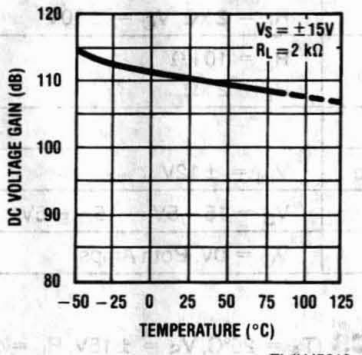
TL/H/5218–6

Supply Current vs Supply Voltage



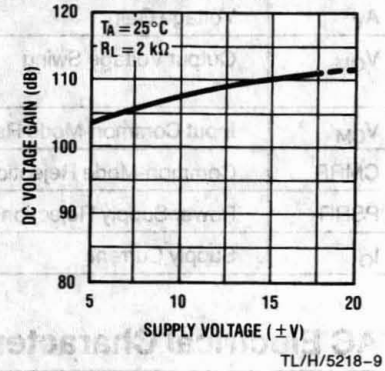
TL/H/5218–7

DC Voltage Gain vs Ambient Temperature



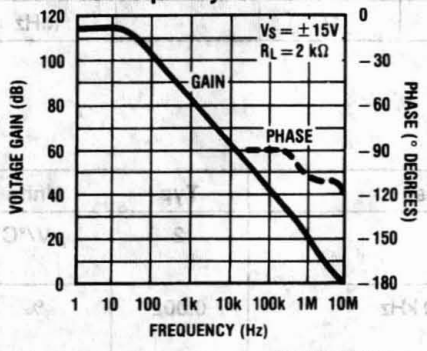
TL/H/5218–8

DC Voltage Gain vs Supply Voltage



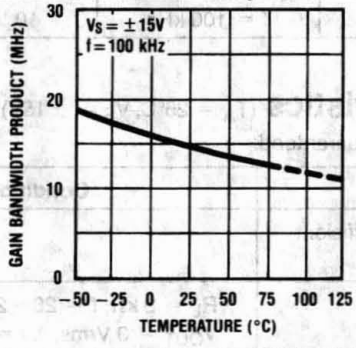
TL/H/5218–9

Voltage Gain & Phase vs Frequency



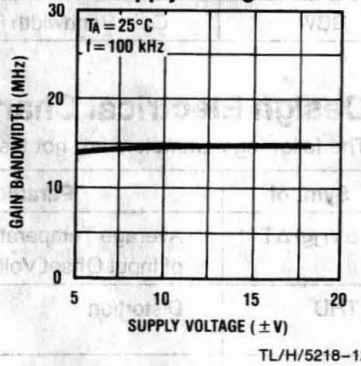
TL/H/5218–10

Gain Bandwidth Product vs Ambient Temperature



TL/H/5218–11

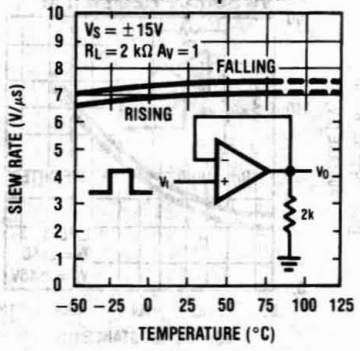
Gain Bandwidth vs Supply Voltage



TL/H/5218–12

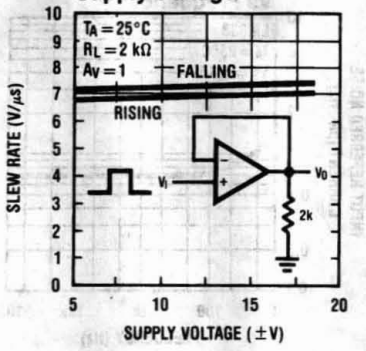
Typical Performance Characteristics (Continued)

Slew Rate vs Ambient Temperature



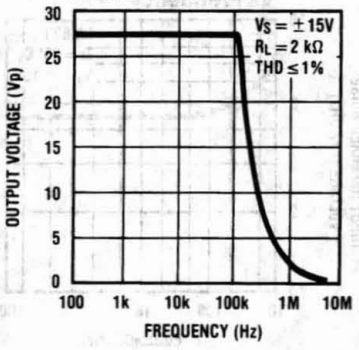
TL/H/5218–13

Slew Rate vs Supply Voltage



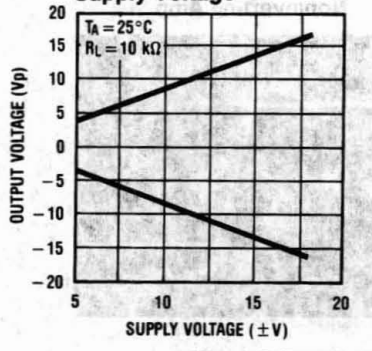
TL/H/5218–14

Power Bandwidth



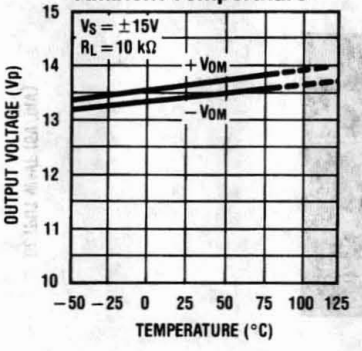
TL/H/5218–15

Maximum Output Voltage vs Supply Voltage



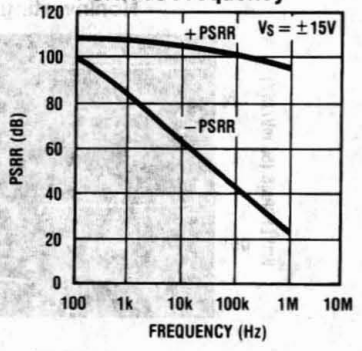
TL/H/5218–16

Maximum Output Voltage vs Ambient Temperature



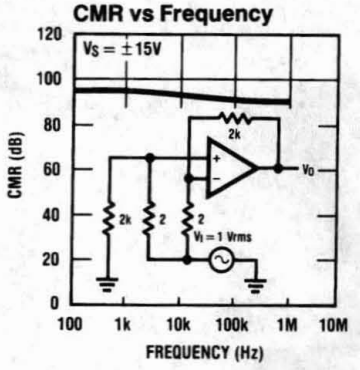
TL/H/5218–17

PSRR vs Frequency



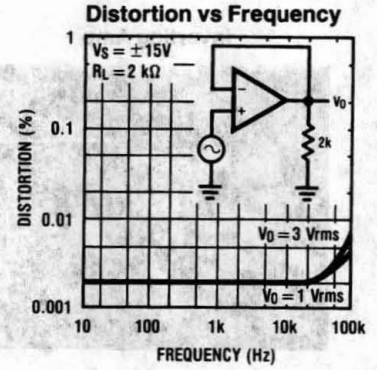
TL/H/5218–18

CMR vs Frequency



TL/H/5218–19

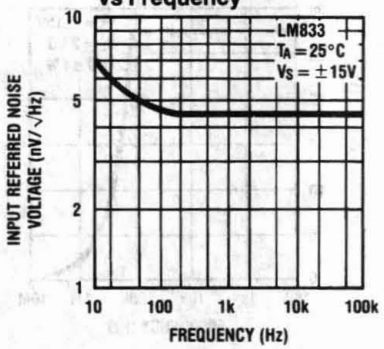
Distortion vs Frequency



TL/H/5218–20

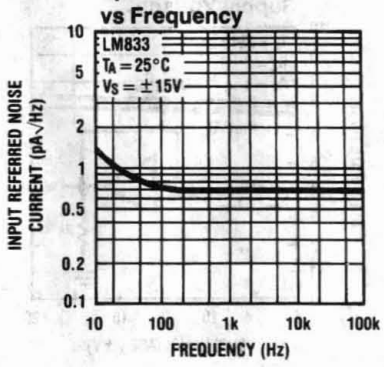
Typical Performance Characteristics (Continued)

Spot Noise Voltage vs Frequency



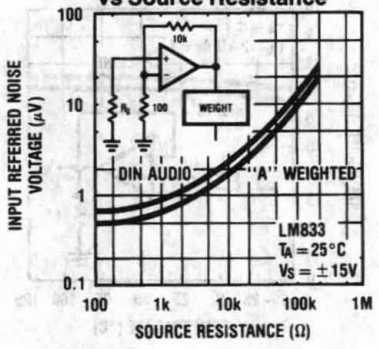
TL/H/5218–21

Spot Noise Current vs Frequency



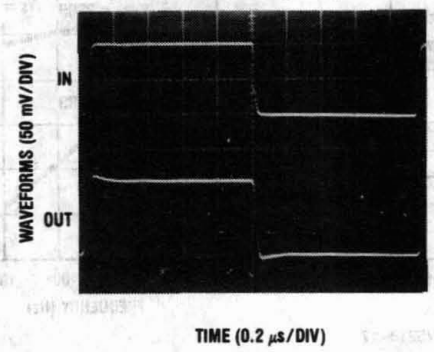
TL/H/5218–22

Input Referred Noise Voltage vs Source Resistance



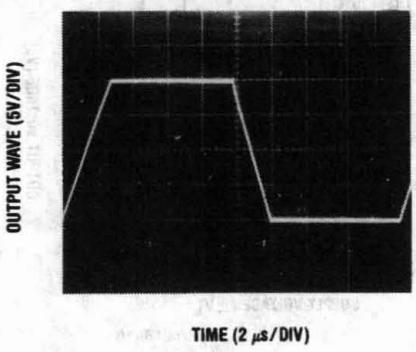
TL/H/5218–23

Noninverting Amp



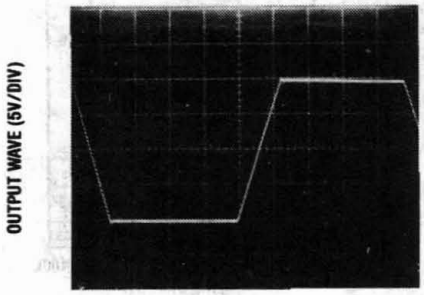
TL/H/5218–24

Noninverting Amp



TL/H/5218–25

Inverting Amp



TL/H/5218–26

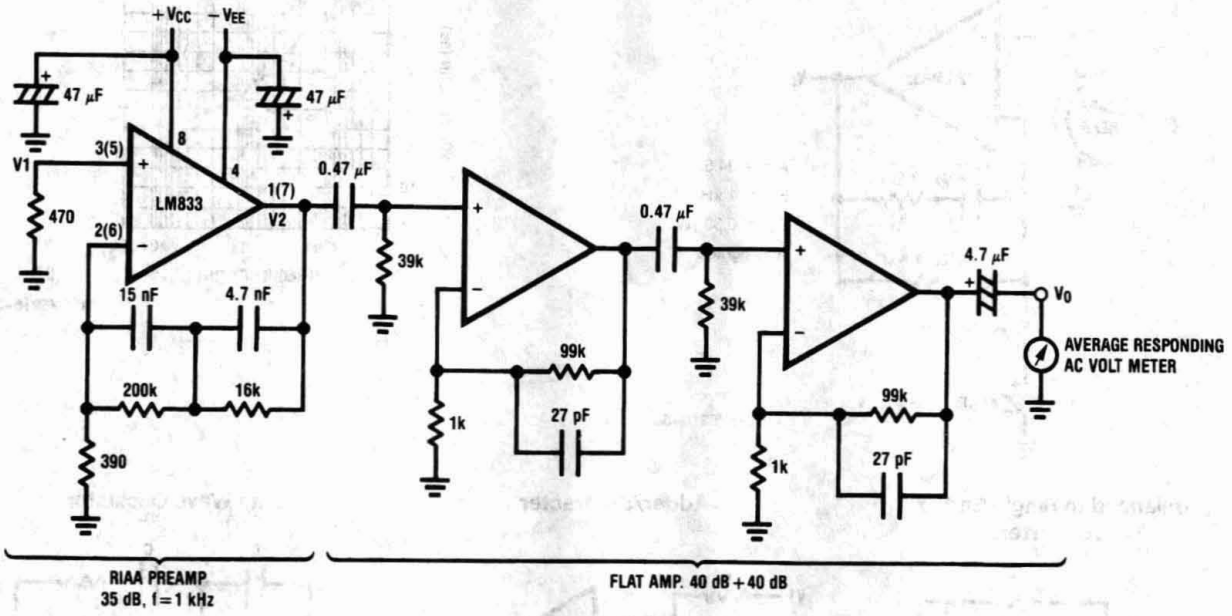
Application Hints

The LM833 is a high speed op amp with excellent phase margin and stability. Capacitive loads up to 50 pF will cause little change in the phase characteristics of the amplifiers and are therefore allowable.

Capacitive loads greater than 50 pF must be isolated from the output. The most straightforward way to do this is to put a resistor in series with the output. This resistor will also prevent excess power dissipation if the output is accidentally shorted.

Noise Measurement Circuit

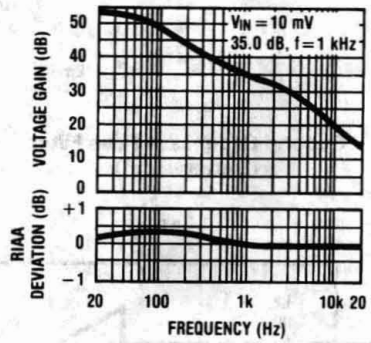
Complete shielding is required to prevent induced pick up from external sources. Always check with oscilloscope for power line noise.



TL/H/5218–27

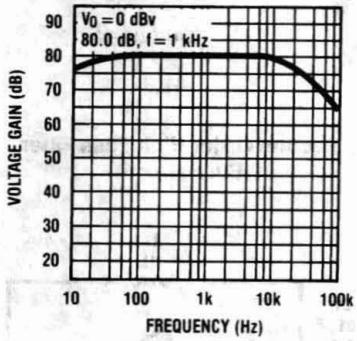
Total Gain: 115 dB @f = 1 kHz
Input Referred Noise Voltage: e_n = V0/560,000 (V)

RIAA Preamp Voltage Gain, RIAA Deviation vs Frequency



TL/H/5218–28

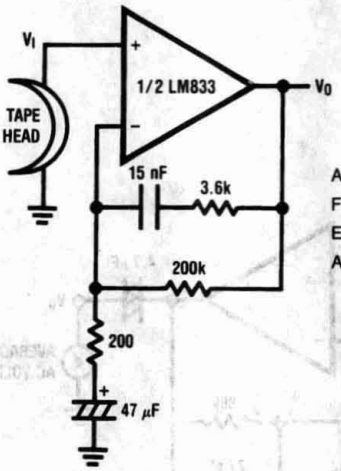
Flat Amp Voltage Gain vs Frequency



TL/H/5218–29

Typical Applications

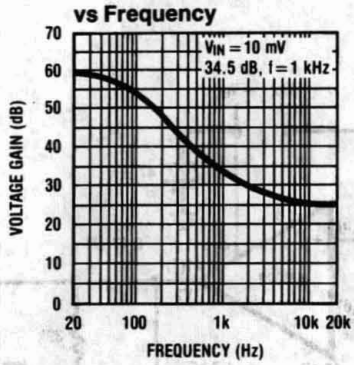
NAB Preamp



A_V = 34.5
F = 1 kHz
E_n = 0.38 μV
A Weighted

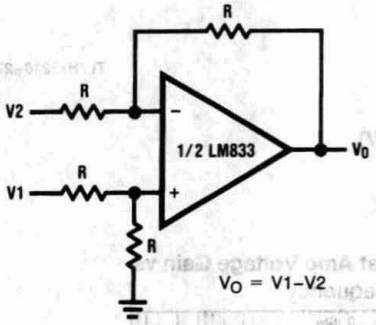
TL/H/5218–30

NAB Preamp Voltage Gain vs Frequency



TL/H/5218–31

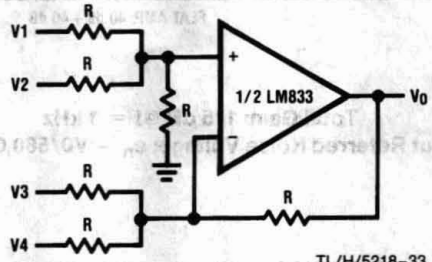
Balanced to Single Ended Converter



$V_O = V1 - V2$

TL/H/5218–32

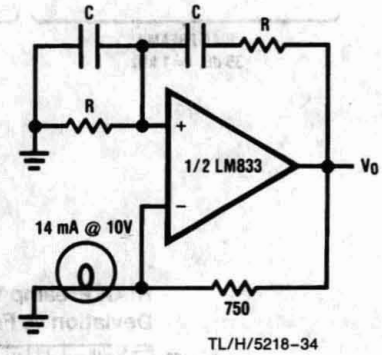
Adder/Subtracter



$V_O = V1 + V2 - V3 - V4$

TL/H/5218–33

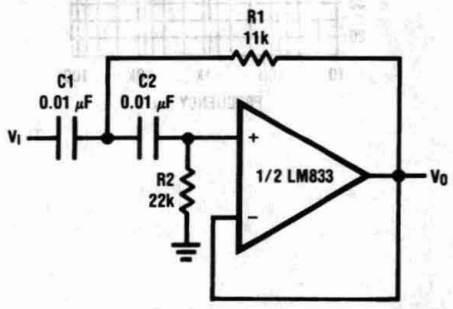
Sine Wave Oscillator



TL/H/5218–34

$$f_o = \frac{1}{2\pi RC}$$

Second Order High Pass Filter (Butterworth)



TL/H/5218–35

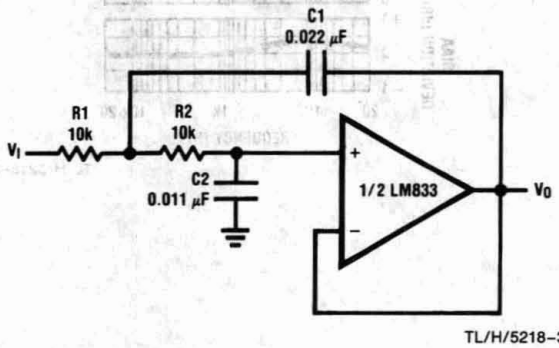
if C1 = C2 = C

$$R1 = \frac{\sqrt{2}}{2\omega_o C}$$

R2 = 2•R1

Illustration is f_0 = 1 kHz

Second Order Low Pass Filter (Butterworth)



TL/H/5218–36

if R1 = R2 = R

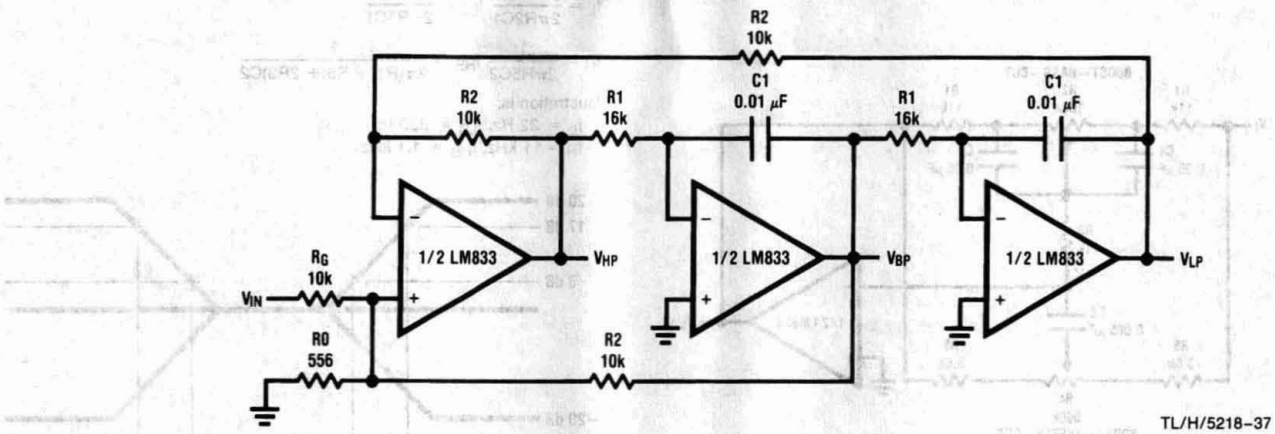
$$C1 = \frac{\sqrt{2}}{\omega_o R}$$

$$C2 = \frac{C1}{2}$$

Illustration is f_0 = 1 kHz

Typical Applications (Continued)

State Variable Filter

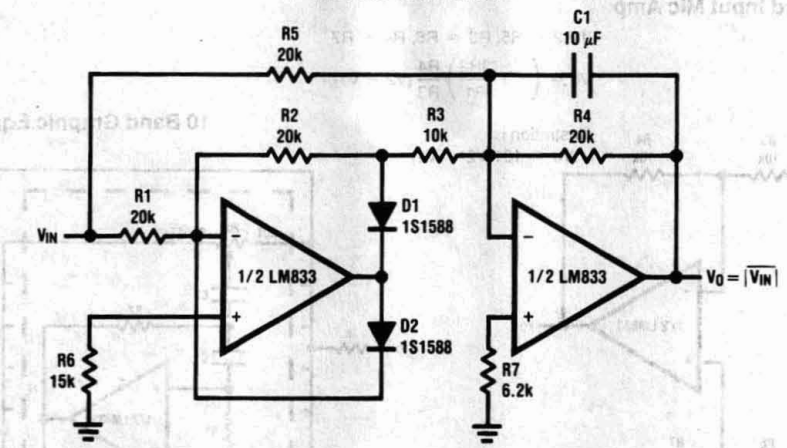


TL/H/5218–37

$$f_0 = \frac{1}{2\pi C1R1}, Q = \frac{1}{2}\left(1 + \frac{R2}{R0} + \frac{R2}{RG}\right), A_{BP} = QA_{LP} = QA_{LH} = \frac{R2}{RG}$$

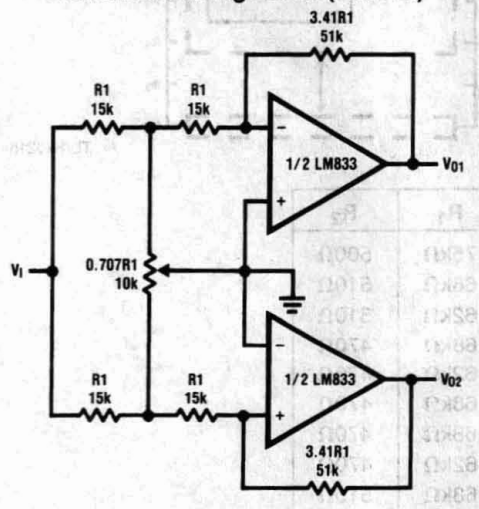
Illustration is f_0 = 1 kHz, Q = 10, A_{BP} = 1

AC/DC Converter



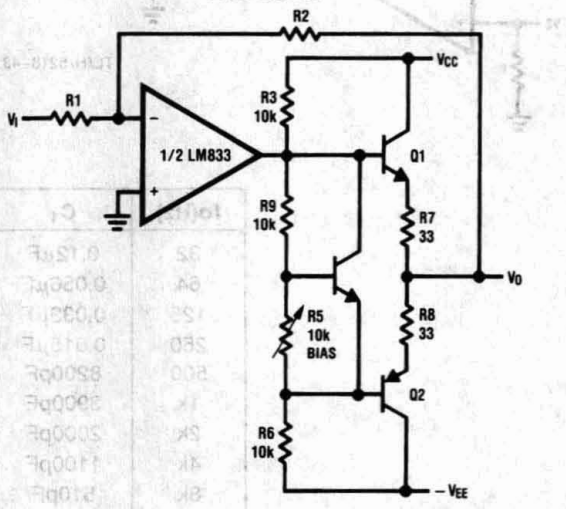
TL/H/5218–38

2 Channel Panning Circuit (Pan Pot)



TL/H/5218–39

Line Driver



TL/H/5218–40

Typical Application (Continued)

Tone Control

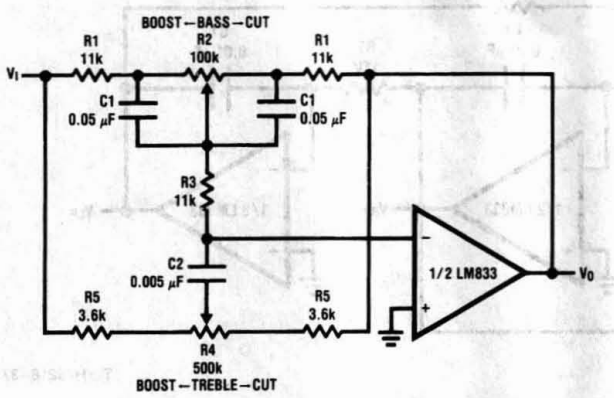
$$f_L = \frac{1}{2\pi R2C1},\ f_{LB} = \frac{1}{2\pi R1C1}$$

$$f_H = \frac{1}{2\pi R5C2},\ f_{HB} = \frac{1}{2\pi(R1 + R5 + 2R3)C2}$$

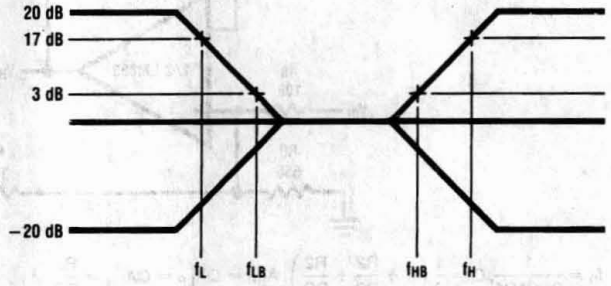
Illustration is:

f_L = 32 Hz, f_{LB} = 320 Hz

f_H = 11 kHz, f_{HB} = 1.1 kHz



TL/H/5218–41



TL/H/5218–42

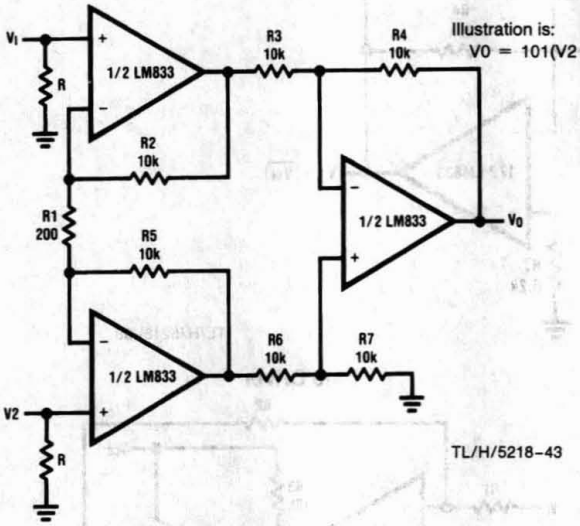
Balanced Input Mic Amp

If R2 = R5, R3 = R6, R4 = R7

$$V0 = \left(1 + \frac{2R2}{R1}\right)\frac{R4}{R3}(V2 - V1)$$

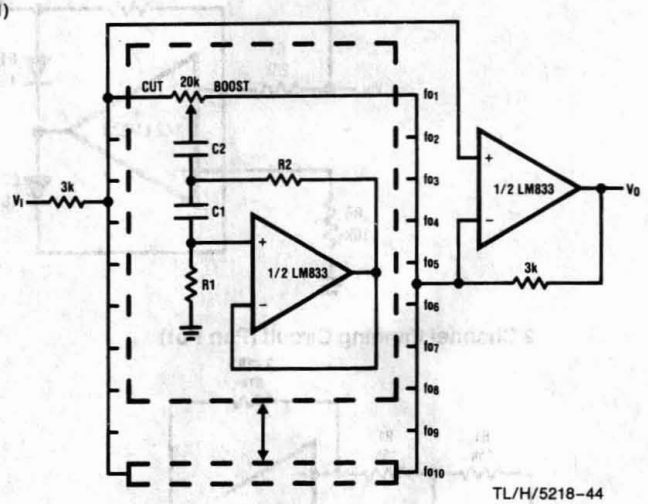
Illustration is:

V0 = 101(V2 − V1)



TL/H/5218–43

10 Band Graphic Equalizer



TL/H/5218–44

fo(Hz)	C_1	C_2	R_1	R_2
32	0.12μF	4.7μF	75kΩ	500Ω
64	0.056μF	3.3μF	68kΩ	510Ω
125	0.033μF	1.5μF	62kΩ	510Ω
250	0.015μF	0.82μF	68kΩ	470Ω
500	8200pF	0.39μF	62kΩ	470Ω
1k	3900pF	0.22μF	68kΩ	470Ω
2k	2000pF	0.1μF	68kΩ	470Ω
4k	1100pF	0.056μF	62kΩ	470Ω
8k	510pF	0.022μF	68kΩ	510Ω
16k	330pF	0.012μF	51kΩ	510Ω

At volume of change = ±12 dB

Q = 1.7

Reference: "AUDIO/RADIO HANDBOOK", National Semiconductor, 1980, Page 2–61

National Semiconductor

LM837 Low Noise Quad Operational Amplifier

General Description

The LM837 is a quad operational amplifier designed for low noise, high speed and wide bandwidth performance. It has a new type of output stage which can drive a 600Ω load, making it ideal for almost all digital audio, graphic equalizer, preamplifiers, and professional audio applications. Its high performance characteristics also make it suitable for instrumentation applications where low noise is the key consideration.

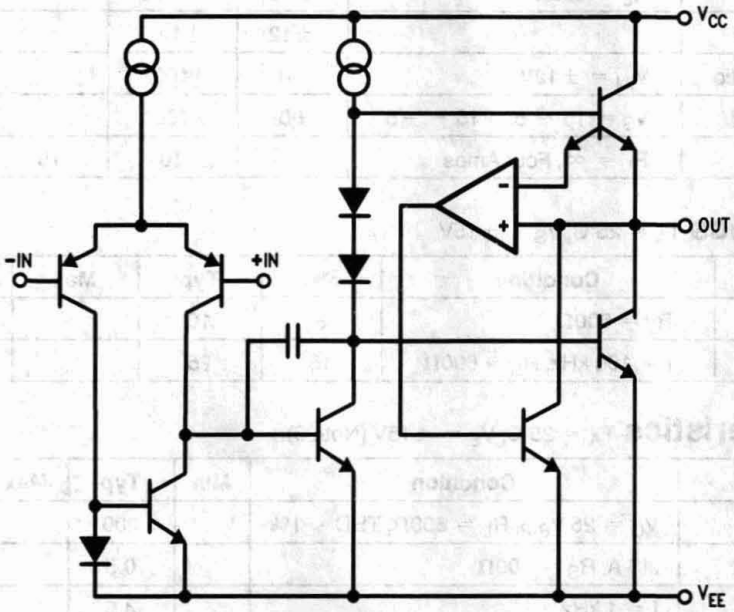
The LM837 is internally compensated for unity gain operation. It is pin compatible with most other standard quad op amps and can therefore be used to upgrade existing systems with little or no change.

Features

■ High slew rate	10 V/μs (typ) 8 V/μs (min)
■ Wide gain bandwidth product	25 MHz (typ) 15 MHz (min)
■ Power bandwidth	200 kHz (typ)
■ High output current	±40 mA
■ Excellent output drive performance	>600Ω
■ Low input noise voltage	4.5 nV/√Hz
■ Low total harmonic distortion	0.0015%
■ Low offset voltage	0.3 mV

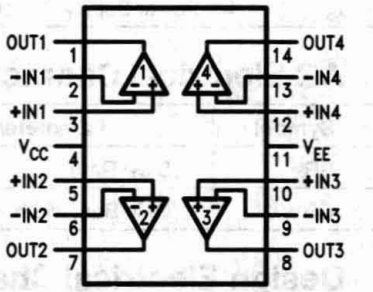
Schematic and Connection Diagrams

1/4 Quad



TL/H/9047–1

Dual-In-Line Package



TL/H/9047–2

Top View

Order Number LM837M or LM837N
See NS Package Number M14A or N14A

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	V_{CC}/V_{EE}	±18V
Differential Input Voltage (Note 1)	V_{ID}	±30V
Common Mode Input Voltage (Note 1)	V_{IC}	±15V
Power Dissipation (Note 2)	P_D	1.2W (N) 830 mW (M)
Operating Temperature Range	T_{OPR}	−40°C to +85°C
Storage Temperature Range	T_{STG}	−60°C to +150°C

Soldering Information

Dual-In-Line Package	
Soldering (10 seconds)	260°C
Small Outline Package	
Vapor Phase (60 seconds)	215°C
Infrared (15 seconds)	220°C

ESD rating is to be determined.

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.

DC Electrical Characteristics $T_A = 25°C, V_S = \pm 15V$

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{OS}	Input Offset Voltage	$R_S = 50\Omega$		0.3	5	mV
I_{OS}	Input Offset Current			10	200	nA
I_B	Input Bias Current			500	1000	nA
A_V	Large Signal Voltage Gain	$R_L = 2\,k\Omega, V_{OUT} = \pm 10V$	90	110		dB
V_{OM}	Output Voltage Swing	$R_L = 2\,k\Omega$	±12	±13.5		V
		$R_L = 600\Omega$	±10	±12.5		V
V_{CM}	Common Mode Input Voltage		±12	±14.0		V
CMRR	Common Mode Rejection Ratio	$V_{IN} = \pm 12V$	80	100		dB
PSRR	Power Supply Rejection Ratio	$V_S = 15 \sim 5, -15 \sim -5$	80	100		dB
I_S	Power Supply Current	$R_L = \infty$, Four Amps		10	15	mA

AC Electrical Characteristics $T_A = 25°C, V_S = \pm 15V$

Symbol	Parameter	Condition	Min	Typ	Max	Units
SR	Slew Rate	$R_L = 600\Omega$	8	10		V/μs
GBW	Gain Bandwidth Product	$f = 100\,kHz, R_L = 600\Omega$	15	25		MHz

Design Electrical Characteristics $T_A = 25°C, V_S = \pm 15V$ (Note 3)

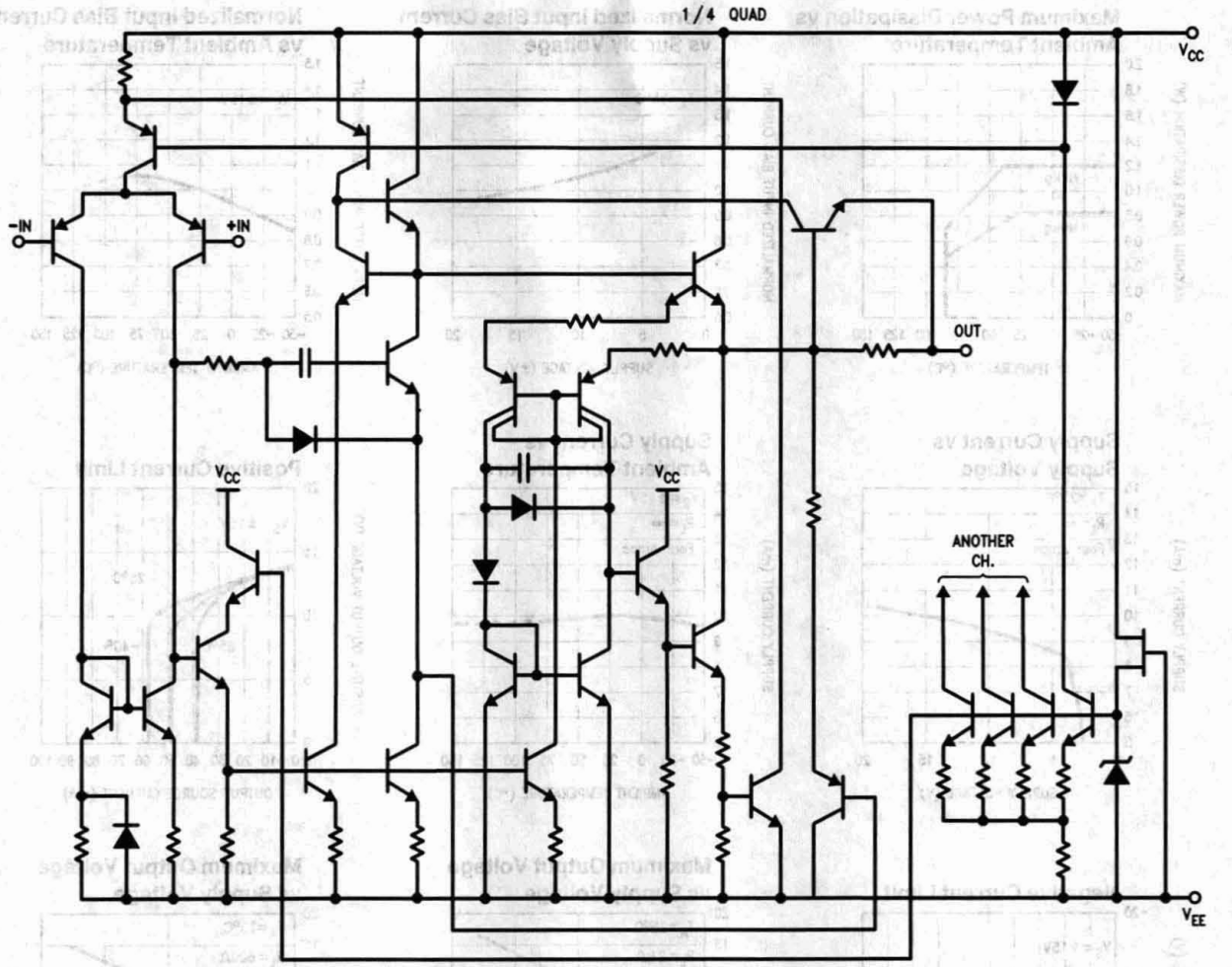
Symbol	Parameter	Condition	Min	Typ	Max	Units
PBW	Power Bandwidth	$V_O = 25\,V_{P-P}, R_L = 600\Omega$, THD < 1%		200		kHz
e_{n1}	Equivalent Input Noise Voltage	JIS A, $R_S = 100\Omega$		0.5		μV
e_{n2}	Equivalent Input Noise Voltage	f = 1 kHz		4.5		$nV/\sqrt{Hz}$
i_n	Equivalent Input Noise Current	f = 1 kHz		0.7		$pA/\sqrt{Hz}$
THD	Total Harmonic Distortion	$A_V = 1, V_{OUT} = 3$ Vrms, $f = 20 \sim 20\,kHz, R_L = 600\Omega$		0.0015		%
f_U	Zero Cross Frequency	Open Loop		12		MHz
ϕ_m	Phase Margin	Open Loop		45		deg
	Input-Referred Crosstalk	$f = 20 \sim 20\,kHz$		−120		dB
$\Delta V_{OS}/\Delta T$	Average TC of Input Offset Voltage			2		μV/°C

Note 1: Unless otherwise specified the absolute maximum input voltage is equal to the power supply voltage.

Note 2: For operation at ambient temperatures above 25°C, the device must be derated based on a 150°C maximum junction temperature and a thermal resistance, junction to ambient, as follows: LM837N, 90°C/W; LM837M, 150°C/W.

Note 3: The following parameters are not tested or guaranteed.

Detailed Schematic



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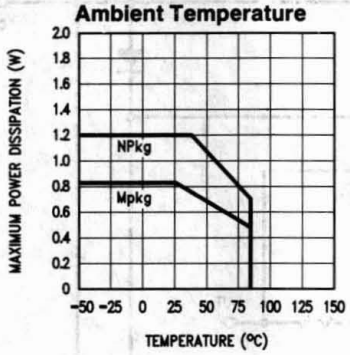
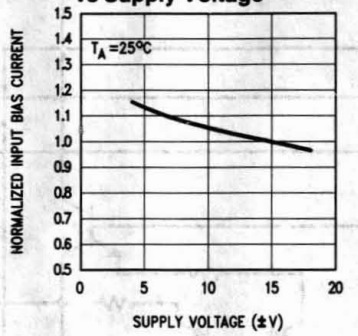
Typical Performance Characteristics

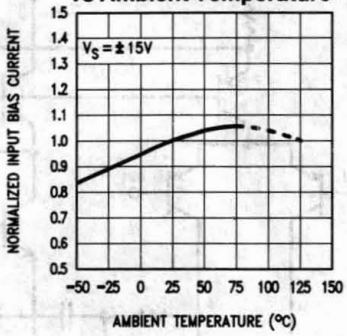
Maximum Power Dissipation vs Ambient Temperature



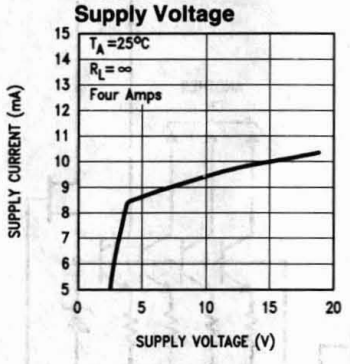
Normalized Input Bias Current vs Supply Voltage



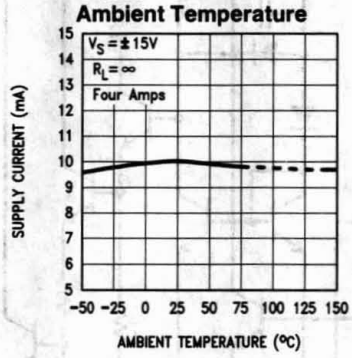
Normalized Input Bias Current vs Ambient Temperature



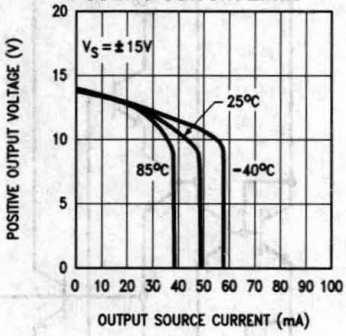
Supply Current vs Supply Voltage



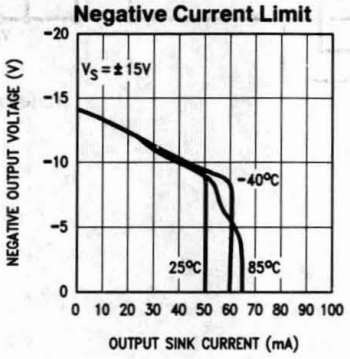
Supply Current vs Ambient Temperature



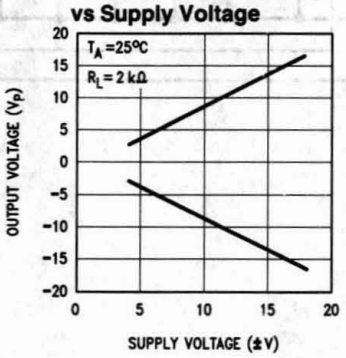
Positive Current Limit



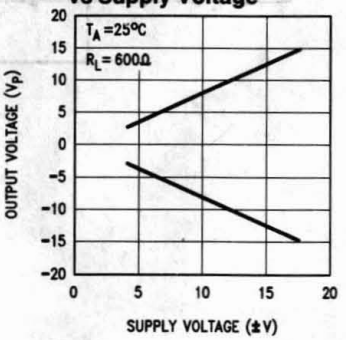
Negative Current Limit



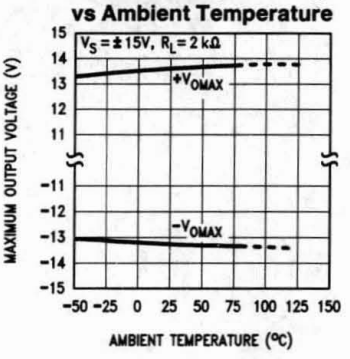
Maximum Output Voltage vs Supply Voltage



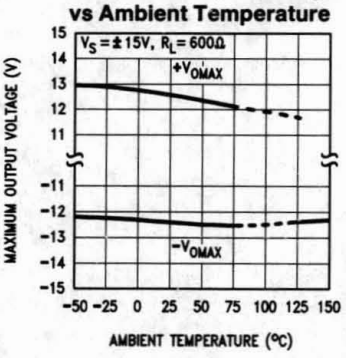
Maximum Output Voltage vs Supply Voltage



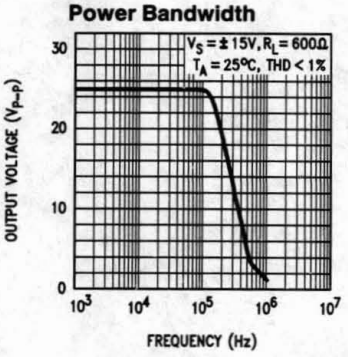
Maximum Output Voltage vs Ambient Temperature



Maximum Output Voltage vs Ambient Temperature



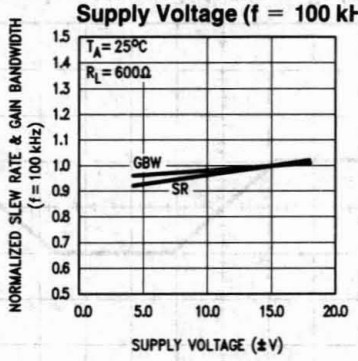
Power Bandwidth



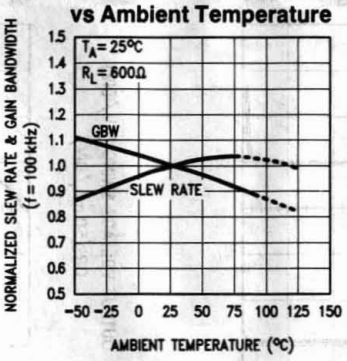
TL/H/9047–4

Typical Performance Characteristics (Continued)

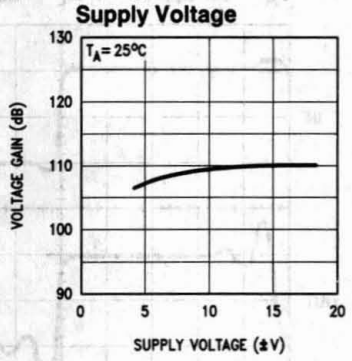
Normalized Slew Rate & Gain Bandwidth vs Supply Voltage (f = 100 kHz)



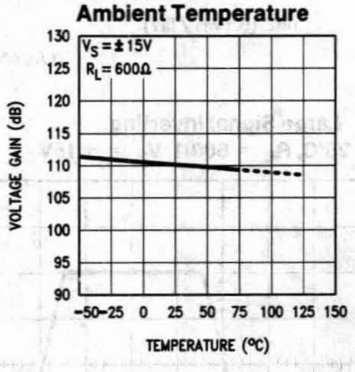
Normalized Slew Rate & Gain Bandwidth (f = 100 kHz) vs Ambient Temperature



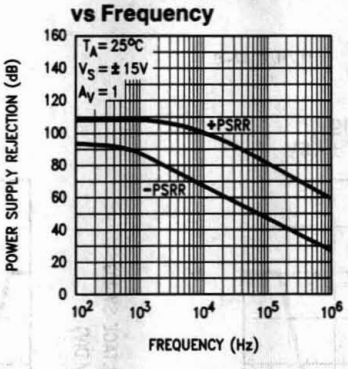
Voltage Gain vs Supply Voltage



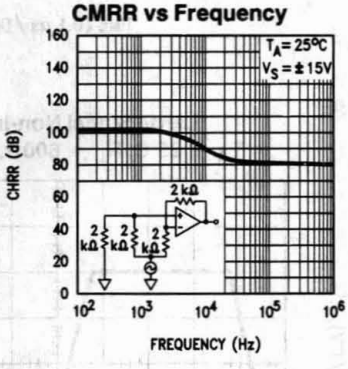
Voltage Gain vs Ambient Temperature



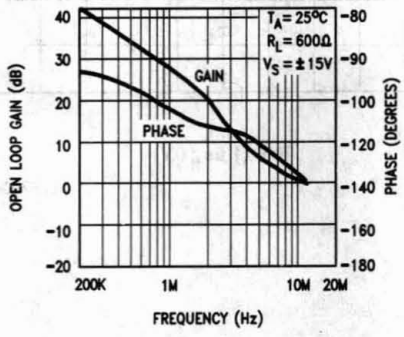
Power Supply Rejection vs Frequency



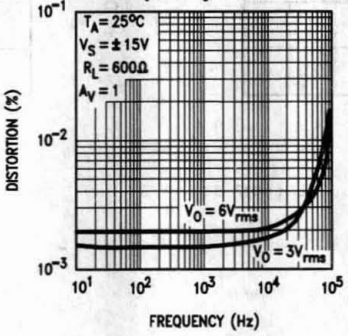
CMRR vs Frequency



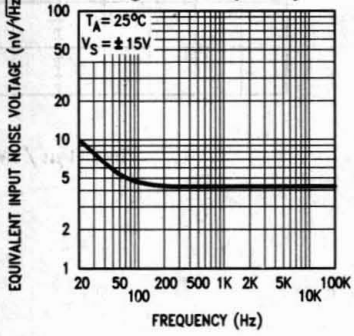
Open Loop Gain & Phase vs Frequency



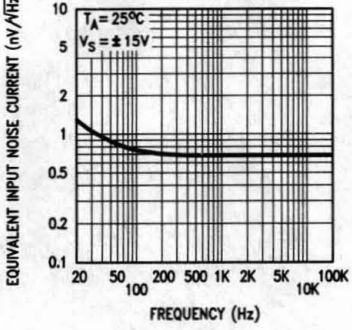
Total Harmonic Distortion vs Frequency



Equivalent Input Noise Voltage vs Frequency



Equivalent Input Noise Current vs Frequency

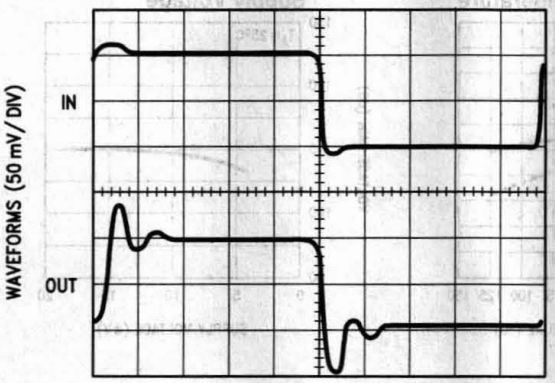


TL/H/9047–5

Typical Performance Characteristics (Continued)

Small Signal, Non-Inverting

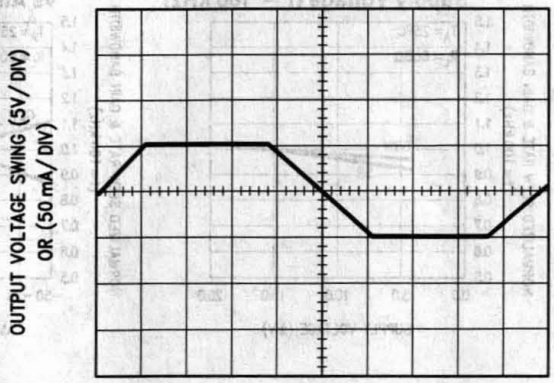
$T_A = 25°C$, $A_V = 1$, $R_L = 600\Omega$, $V_S = \pm 15V$



TL/H/9047–6

Current Limit

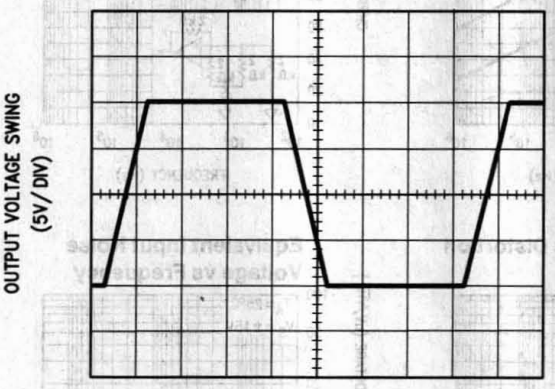
$T_A = 25°C$, $V_S = \pm 15V$, $R_L = 100\Omega$, $A_V = 1$



TL/H/9047–7

Large Signal Non-Inverting

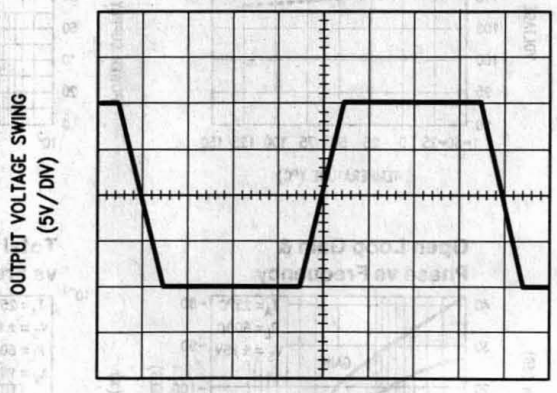
$T_A = 25°C$, $R_L = 600\Omega$, $V_S = \pm 15V$



TL/H/9047–8

Large Signal Inverting

$T_A = 25°C$, $R_L = 600\Omega$, $V_S = \pm 15V$



TL/H/9047–9

National Semiconductor

LM6142 Dual and LM6144 Quad High Speed/Low Power 17 MHz Rail-to-Rail Input-Output Operational Amplifiers

General Description

Using patent pending new circuit topologies, the LM6142/44 provides new levels of performance in applications where low voltage supplies or power limitations previously made compromise necessary. Operating on supplies of 1.8V to over 24V, the LM6142/44 is an excellent choice for battery operated systems, portable instrumentation and others.

The greater than rail-to-rail input voltage range eliminates concern over exceeding the common-mode voltage range. The rail-to-rail output swing provides the maximum possible dynamic range at the output. This is particularly important when operating on low supply voltages.

High gain-bandwidth with 650 μA/Amplifier supply current opens new battery powered applications where previous higher power consumption reduced battery life to unacceptable levels. The ability to drive large capacitive loads without oscillating functionally removes this common problem.

Features At V_S = 5V. Typ unless noted.

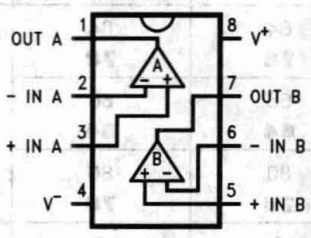
- Rail-to-rail input CMVR −0.25V to 5.25V
- Rail-to-rail output swing 0.005V to 4.995V
- Wide gain-bandwidth: 17 MHz at 50 kHz (typ)
- Slew rate:
  - Small signal, 5V/μs
  - Large signal, 30V/μs
- Low supply current 650 μA/Amplifier
- Wide supply range 1.8V to 24V
- CMRR 107 dB
- Gain 108 dB with R_L = 10k
- PSRR 87 dB

Applications

- Battery operated instrumentation
- Depth sounders/fish finders
- Barcode scanners
- Wireless communications
- Rail-to-rail in-out instrumentation amps

Connection Diagrams

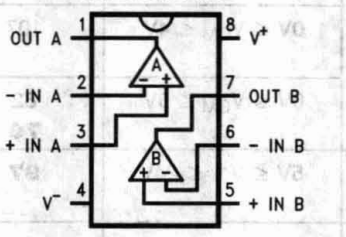
8-Pin CDIP



TL/H/12057–14

Top View

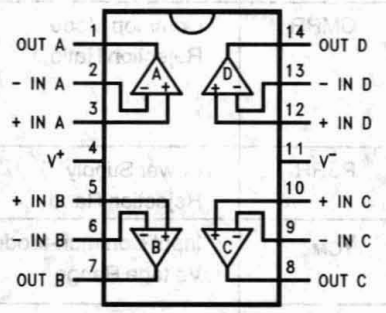
8-Pin DIP/SO



TL/H/12057–1

Top View

14-Pin DIP/SO



TL/H/12057–2

Top View

Ordering Information

Package	Temperature Range Industrial −40°C to +85°C	Temperature Range Military −55°C to +125°C	NSC Drawing
8-Pin Molded DIP	LM6142AIN, LM6142BIN		N08E
8-Pin Small Outline	LM6142AIM, LM6142BIM		M08A
14-Pin Molded DIP	LM6144AIN, LM6144BIN		N14A
14-Pin Small Outline	LM6144AIM, LM6144BIM		M14A
8-Pin CDIP		LM6142AMJ/883	D08C

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

ESD Tolerance (Note 2)	2500V
Differential Input Voltage	15V
Voltage at Input/Output Pin	$(V^+) + 0.3V, (V^-) - 0.3V$
Supply Voltage $(V^+ - V^-)$	35V
Current at Input Pin	±10 mA
Current at Output Pin (Note 3)	±25 mA
Current at Power Supply Pin	50 mA
Lead Temperature (soldering, 10 sec)	260°C
Storage Temp. Range	−65°C to +150°C
Junction Temperature (Note 4)	150°C

Operating Ratings (Note 1)

Supply Voltage	$1.8V \le V^+ \le 24V$
Junction Temperature Range	
LM6142, LM6144	$-40°C \le T_J \le +85°C$
Thermal Resistance (θ_{JA})	
N Package, 8-Pin Molded DIP	115°C/W
M Package, 8-Pin Surface Mount	193°C/W
N Package, 14-Pin Molded DIP	81°C/W
M Package, 14-Pin Surface Mount	126°C/W

5.0V DC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for $T_J = 25°C$, $V^+ = 5.0V$, $V^- = 0V$, $V_{CM} = V_O = V^+/2$ and $R_L > 1\ M\Omega$ to V+/2. **Boldface limits** apply at the temperature extremes.

Symbol	Parameter	Conditions	Typ (Note 5)	LM6144AI LM6142AI Limit (Note 6)	LM6144BI LM6142BI Limit (Note 6)	Units
V_{OS}	Input Offset Voltage		0.3	1.0 **2.2**	2.5 **3.3**	mV max
TCV_{OS}	Input Offset Voltage Average Drift		**3**			µV/°C
I_B	Input Bias Current		170	250	300	nA max
		$0V \le V_{CM} \le 5V$	180	280 **526**	**526**	nA max
I_{OS}	Input Offset Current		3	30 **80**	30 **80**	nA max
R_{IN}	Input Resistance, C_M		126			MΩ
CMRR	Common Mode Rejection Ratio	$0V \le V_{CM} \le 4V$	107	84 **78**	84 **78**	dB min
		$0V \le V_{CM} \le 5V$	82 **79**	66 **64**	66 **64**	dB min
PSRR	Power Supply Rejection Ratio	$5V \le V^+ \le 24V$	**87**	80 **78**	80 **78**	dB min
V_{CM}	Input Common-Mode Voltage Range		−0.25	**0**	**0**	V
			5.25	**5.0**	**5.0**	V
A_V	Large Signal Voltage Gain	$R_L = 10k$	270 **70**	100 **33**	80 **25**	V/mV min
V_O	Output Swing	$R_L = 100k$	0.005	0.01 **0.013**	0.01 **0.013**	V max
			4.995	4.98 **4.93**	4.98 **4.93**	V min
		$R_L = 10k$	0.02			V max
			4.97			V min
		$R_L = 2k$	0.06	0.1 **0.133**	0.1 **0.133**	V max
			4.90	4.86 **4.80**	4.86 **4.80**	V min

5.0V DC Electrical Characteristics

Unless Otherwise Specified, All Limits Guaranteed for T_J = 25°C, V^+ = 5.0V, V^- = 0V, V_{CM} = V_O = $V^+/2$ and R_L > 1 MΩ to $V^+/2$. **Boldface limits** apply at the temperature extremes. (Continued)

Symbol	Parameter	Conditions	Typ (Note 5)	LM6144AI LM6142AI Limit (Note 6)	LM6144BI LM6142BI Limit (Note 6)	Units
I_{SC}	Output Short Circuit Current LM6142	Sourcing	13	10 **4.9**	8 **4**	mA min
				35	**35**	mA max
		Sinking	24	10 **5.3**	10 **5.3**	mA min
				35	**35**	mA max
I_{SC}	Output Short Circuit Current LM6144	Sourcing	8	6 **3**	6 **3**	mA min
				35	**35**	mA max
		Sinking	22	8 **4**	8 **4**	mA min
				35	**35**	mA max
I_S	Supply Current	Per Amplifier	650	800 **880**	800 **880**	μA max

5.0V AC Electrical Characteristics

Unless Otherwise Specified, All Limits Guaranteed for T_J = 25°C, V^+ = 5.0V, V^- = 0V, V_{CM} = V_O = $V^+/2$ and R_L > 1 MΩ to $V_S/2$. **Boldface limits** apply at the temperature extremes.

Symbol	Parameter	Conditions	Typ (Note 5)	LM6144AI LM6142AI Limit (Note 6)	LM6144BI LM6142BI Limit (Note 6)	Units
SR	Slew Rate	8 V_{p-p} @ V_{CC} 12V R_S > 1 kΩ	25	15 **13**	13 **11**	V/μs min
GBW	Gain-Bandwidth Product	f = 50 kHz	17	10 **6**	10 **6**	MHz min
ϕ_m	Phase Margin		38			Deg
	Amp-to-Amp Isolation		130			dB
e_n	Input-Referred Voltage Noise	f = 1 kHz	16			$\frac{nV}{\sqrt{Hz}}$
i_n	Input-Referred Current Noise	f = 1 kHz	0.22			$\frac{pA}{\sqrt{Hz}}$
T.H.D.	Total Harmonic Distortion	f = 10 kHz, R_L = 10 kΩ,	0.003			%

2.7V DC Electrical Characteristics

Unless Otherwise Specified, All Limits Guaranteed for T_J = 25°C, V^+ = 2.7V, V^- = 0V, V_{CM} = V_O = $V^+/2$ and R_L > 1 MΩ to $V^+/2$. **Boldface** limits apply at the temperature extreme

Symbol	Parameter	Conditions	Typ (Note 5)	LM6144AI LM6142AI Limit (Note 6)	LM6144BI LM6142BI Limit (Note 6)	Units
V_{OS}	Input Offset Voltage		0.4	1.8 **4.3**	2.5 **4.3**	mV max
I_B	Input Bias Current		150	250 **526**	300 **526**	nA max
I_{OS}	Input Offset Current		4	30 **80**	30 **80**	nA max
R_{IN}	Input Resistance		128			MΩ
CMRR	Common Mode Rejection Ratio	0V ≤ V_{CM} ≤ 1.8V	90			dB min
		0V ≤ V_{CM} ≤ 2.7V	76			
PSRR	Power Supply Rejection Ratio	3V ≤ V^+ ≤ 5V	79			
V_{CM}	Input Common-Mode Voltage Range		−0.25	0	0	V min
			2.95	2.7	2.7	V max
A_V	Large Signal Voltage Gain	R_L = 10k	55			V/mV min
V_O	Output Swing	R_L = 10 kΩ	0.019	0.08 **0.112**	0.08 **0.112**	V max
			2.67	2.66 **2.25**	2.66 **2.25**	V min
I_S	Supply Current	Per Amplifier	510	800 **880**	800 **880**	μA max

2.7V AC Electrical Characteristics

Unless Otherwise Specified, All Limits Guaranteed for T_J = 25°C, V^+ = 2.7V, V^- = 0V, V_{CM} = V_O = $V^+/2$ and R_L > 1 MΩ to $V^+/2$. **Boldface** limits apply at the temperature extreme

Symbol	Parameter	Conditions	Typ (Note 5)	LM6144AI LM6142AI Limit (Note 6)	LM6144BI LM6142BI Limit (Note 6)	Units
GBW	Gain-Bandwidth Product	f = 50 kHz	9			MHz
ϕ_m	Phase Margin		36			Deg
G_m	Gain Margin		6			dB

24V Electrical Characteristics

Unless Otherwise Specified, All Limits Guaranteed for T_J = 25°C, V^+ = 24V, V^- = 0V, V_{CM} = V_O = $V^+/2$ and R_L > 1 MΩ to $V_S/2$. **Boldface** limits apply at the temperature extreme

Symbol	Parameter	Conditions	Typ (Note 5)	LM6144AI LM6142AI Limit (Note 6)	LM6144BI LM6142BI Limit (Note 6)	Units
V_{OS}	Input Offset Voltage		1.3	2 **4.8**	3.8 **4.8**	mV max
I_B	Input Bias Current		174			nA max
I_{OS}	Input Offset Current		5			nA max
R_{IN}	Input Resistance		288			MΩ
CMRR	Common Mode Rejection Ratio	0V ≤ V_{CM} ≤ 23V	114			dB min
		0V ≤ V_{CM} ≤ 24V	100			
PSRR	Power Supply Rejection Ratio	0V ≤ V_{CM} ≤ 24V	87			
V_{CM}	Input Common-Mode Voltage Range		−0.25	0	0	V min
			24.25	24	24	V max
A_V	Large Signal Voltage Gain	R_L = 10k	500			V/mV min
V_O	Output Swing	R_L = 10 kΩ	0.07	0.15 **0.185**	0.15 **0.185**	V max
			23.85	23.81 **23.62**	23.81 **23.62**	V min
I_S	Supply Current	Per Amplifier	750	1100 **1150**	1100 **1150**	μA max
GBW	Gain-Bandwidth Product	f = 50 kHz	18			MHz

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not guaranteed. For guaranteed specifications and the test conditions, see the Electrical Charactenstics.

Note 2: Human body model, 1.5 kΩ in series with 100 pF.

Note 3: Applies to both single-supply and split-supply operation. Continuous short circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 150°C.

Note 4: The maximum power dissipation is a function of $T_{J(max)}$, θ_{JA}, and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(max)} - T_A)/\theta_{JA}$. All numbers apply for packages soldered directly into a PC board.

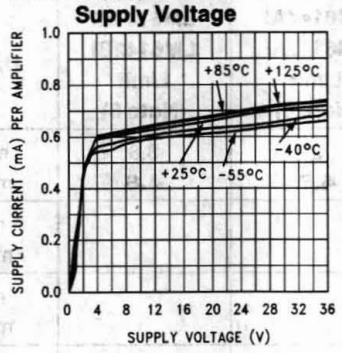
Note 5: Typical values represent the most likely parametric norm.

Note 6: All limits are guaranteed by testing or statistical analysis.

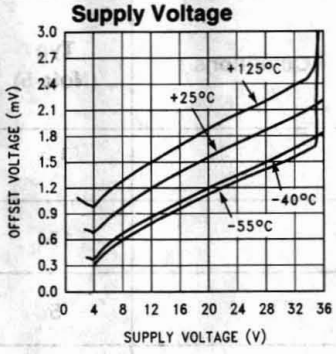
Note 7: For guaranteed military specifications see military datasheet MNLM6142AM-X.

Typical Performance Characteristics $T_A = 25°C$, $R_L = 10\ k\Omega$ Unless Otherwise Specified

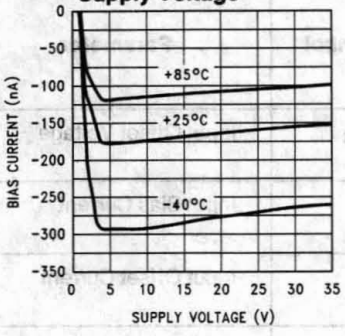
Supply Current vs Supply Voltage



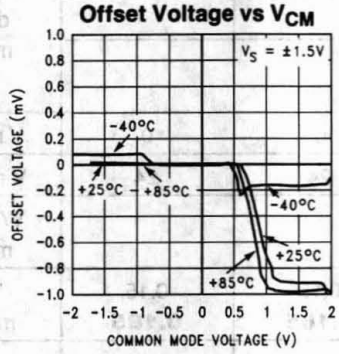
Offset Voltage vs Supply Voltage



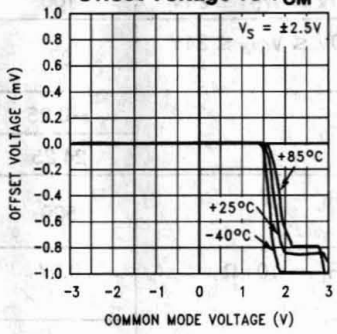
Bias Current vs Supply Voltage



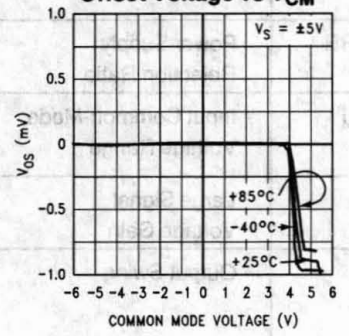
Offset Voltage vs V_{CM}



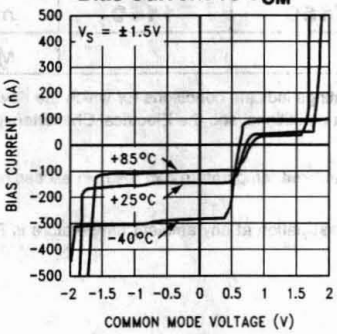
Offset Voltage vs V_{CM}



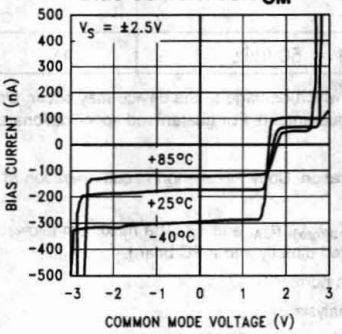
Offset Voltage vs V_{CM}



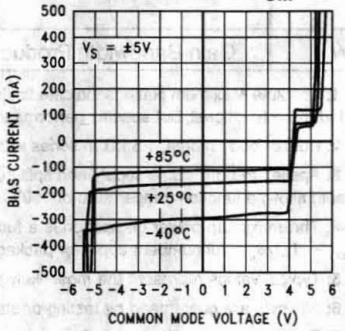
Bias Current vs V_{CM}



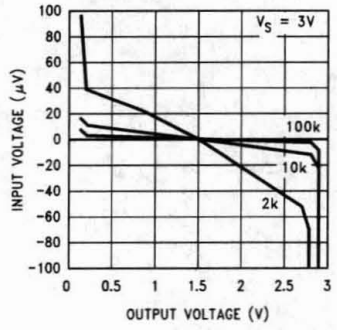
Bias Current vs V_{CM}



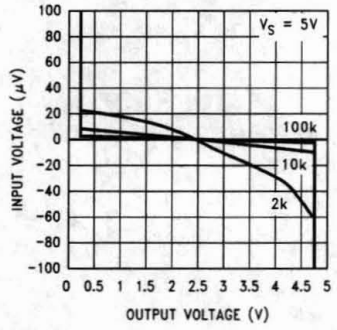
Bias Current vs V_{CM}



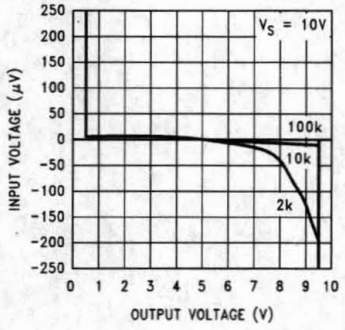
Open-Loop Transfer Function



Open-Loop Transfer Function



Open-Loop Transfer Function

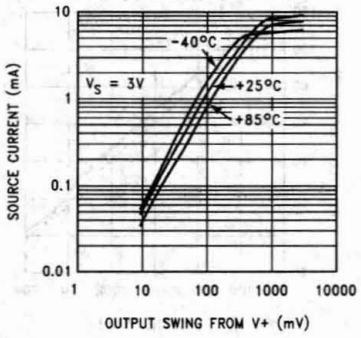


TL/H/12057–3

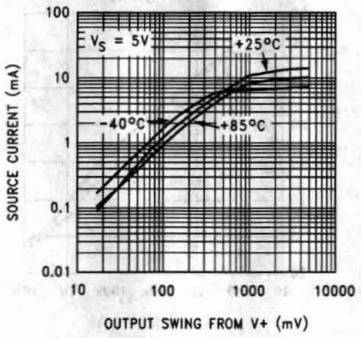
Typical Performance Characteristics

T_A = 25°C, R_L = 10 kΩ Unless Otherwise Specified (Continued)

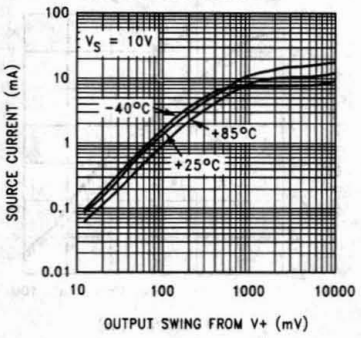
Output Voltage vs Source Current



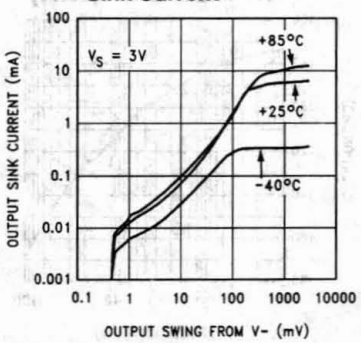
Output Voltage vs Source Current



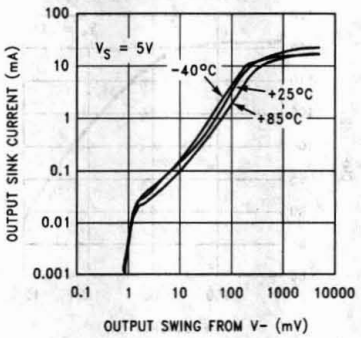
Output Voltage vs Source Current



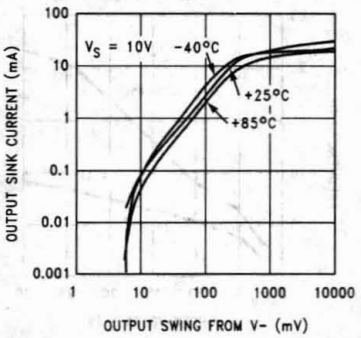
Output Voltage vs Sink Current



Output Voltage vs Sink Current



Output Voltage vs Sink Current



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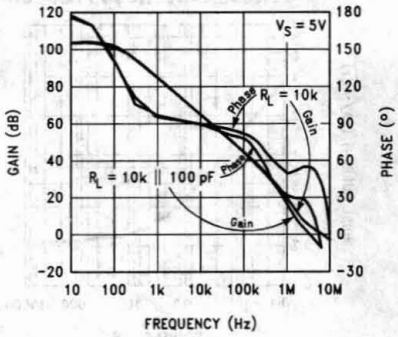
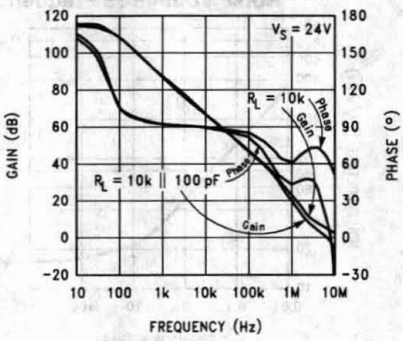
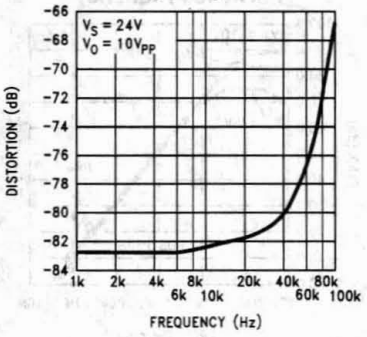
Gain and Phase vs Load



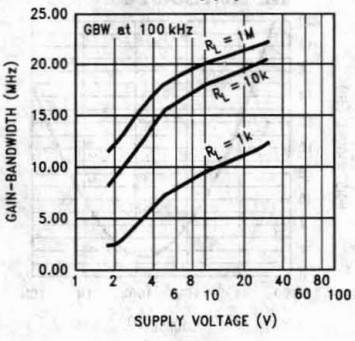
Gain and Phase vs Load



Distortion + Noise vs Frequency



GBW vs Supply

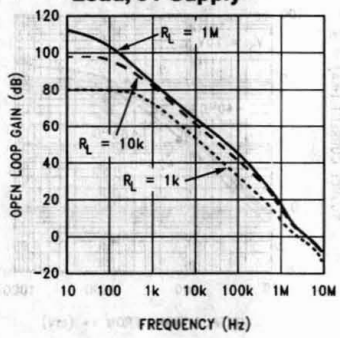


TL/H/12057–11

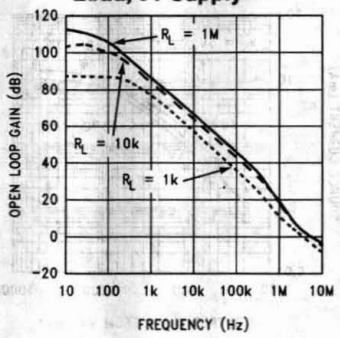
Typical Performance Characteristics

T_A = 25°C, R_L = 10 kΩ Unless Otherwise Specified (Continued)

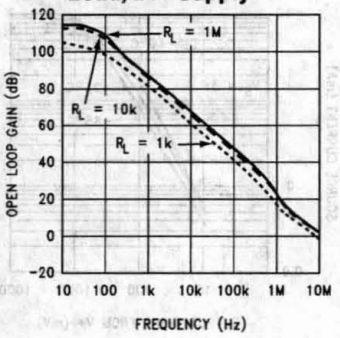
Open Loop Gain vs Load, 3V Supply



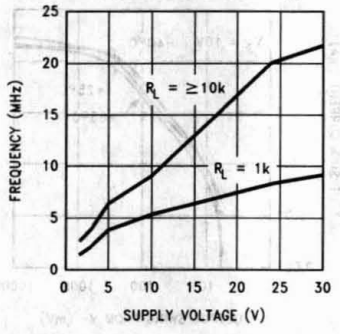
Open Loop Gain vs Load, 5V Supply



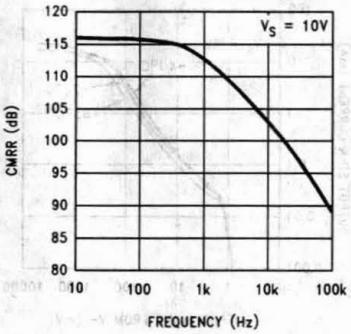
Open Loop Gain vs Load, 24V Supply



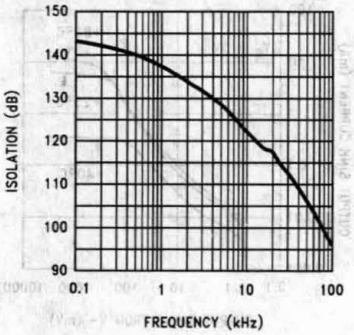
Unity Gain Freq vs V_S



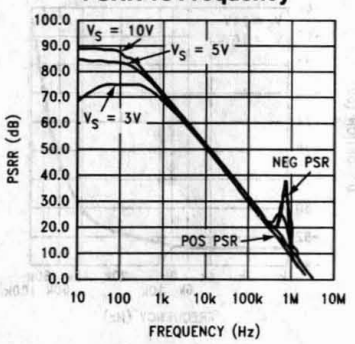
CMRR vs Frequency



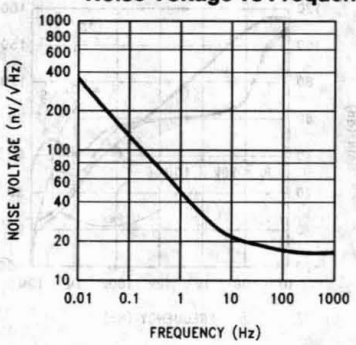
Crosstalk vs Frequency



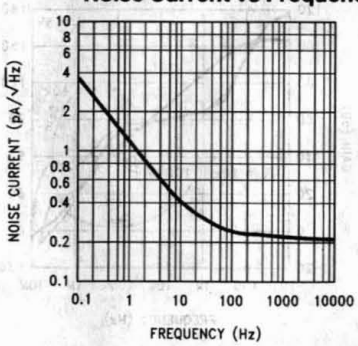
PSRR vs Frequency



Noise Voltage vs Frequency



Noise Current vs Frequency



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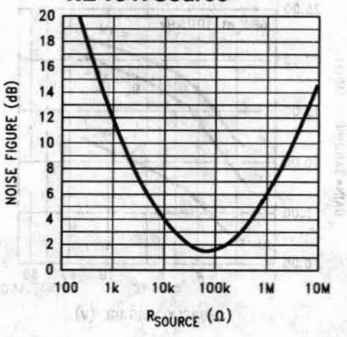
NE vs R Source



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LM6142/44 Application Ideas

The LM6142 brings a new level of ease of use to opamp system design.

With greater than rail-to-rail input voltage range concern over exceeding the common-mode voltage range is eliminated.

Rail-to-rail output swing provides the maximum possible dynamic range at the output. This is particularly important when operating on low supply voltages.

The high gain-bandwidth with low supply current opens new battery powered applications, where high power consumption, previously reduced battery life to unacceptable levels.

To take advantage of these features, some ideas should be kept in mind.

ENHANCED SLEW RATE

Unlike most bipolar opamps, the unique phase reversal prevention/speed-up circuit in the input stage causes the slew rate to be very much a function of the input signal amplitude.

Figure 1 shows how excess input signal, is routed around the input collector-base junctions, directly to the current mirrors.

The LM6142/44 input stage converts the input voltage change to a current change. This current change drives the current mirrors through the collectors of Q1–Q2, Q3–Q4 when the input levels are normal.

If the input signal exceeds the slew rate of the input stage, the differential input voltage rises above two diode drops. This excess signal bypasses the normal input transistors, (Q1–Q4), and is routed in correct phase through the two additional transistors, (Q5, Q6), directly into the current mirrors.

This rerouting of excess signal allows the slew-rate to increase by a factor of 10 to 1 or more. (See *Figure 2*.)

As the overdrive increases, the opamp reacts better than a conventional opamp. Large fast pulses will raise the slew-rate to around 30V to 60V/μs.

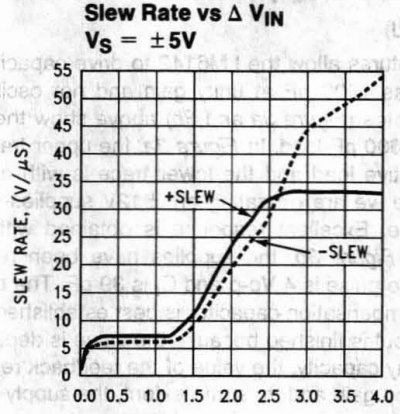
Slew Rate vs Δ V_{IN}
V_S = ±5V
SLEW RATE, (V/μS)
+SLEW
-SLEW
DIFFERENTIAL INPUT VOLTAGE, (V)
0.0 0.5 1.0 1.5 2.0 2.5 3.0 3.5 4.0
0 5 10 15 20 25 30 35 40 45 50 55

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FIGURE 2

This effect is most noticeable at higher supply voltages and lower gains where incoming signals are likely to be large.

This new input circuit also eliminates the phase reversal seen in many opamps when they are overdriven.

This speed-up action adds stability to the system when driving large capacitive loads.

DRIVING CAPACITIVE LOADS

Capacitive loads decrease the phase margin of all opamps. This is caused by the output resistance of the amplifier and the load capacitance forming an R-C phase lag network. This can lead to overshoot, ringing and oscillation. Slew rate limiting can also cause additional lag. Most opamps with a fixed maximum slew-rate will lag further and further behind when driving capacitive loads even though the differential input voltage raises. With the LM6142, the lag causes the slew rate to raise. The increased slew-rate keeps the output following the input much better. This effectively reduces phase lag. After the output has caught up with the input, the differential input voltage drops down and the amplifier settles rapidly.

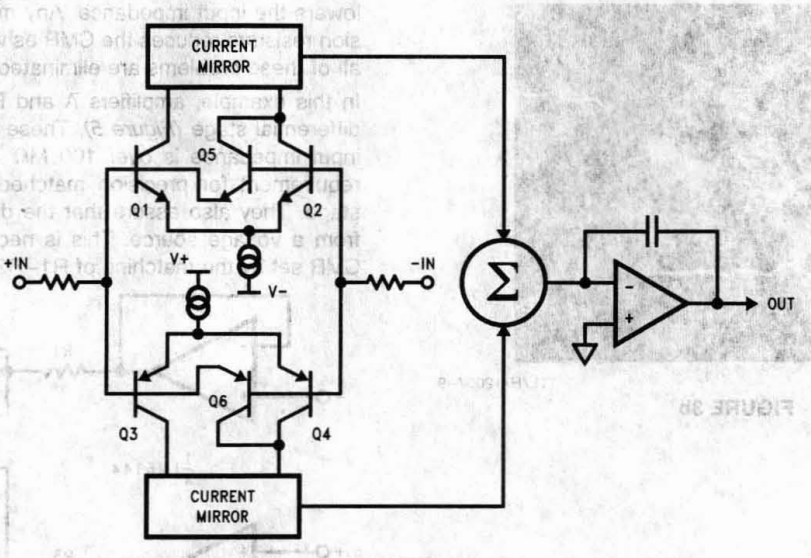

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FIGURE 1

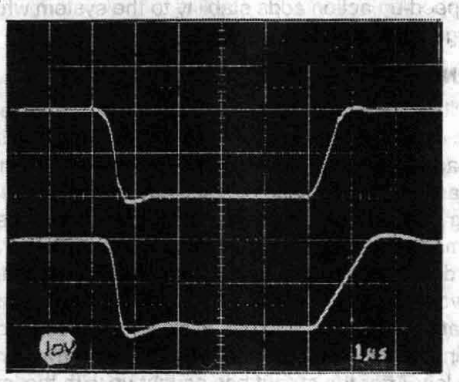
LM6142/44 Application Ideas

(Continued)

These features allow the LM6142 to drive capacitive loads as large as 1000 pF at unity gain and not oscillate. The scope photos (*Figure 3a* and *3b*) above show the LM6142 driving a l000 pF load. In *Figure 3a*, the upper trace is with no capacitive load and the lower trace is with a 1000 pF load. Here we are operating on ±12V supplies with a 20 Vp-p pulse. Excellent response is obtained with a C_f of l0 pF. In *Figure 3b*, the supplies have been reduced to ±2.5V, the pulse is 4 Vp-p and C_f is 39 pF. The best value for the compensation capacitor is best established after the board layout is finished because the value is dependent on board stray capacity, the value of the feedback resistor, the closed loop gain and, to some extent, the supply voltage.

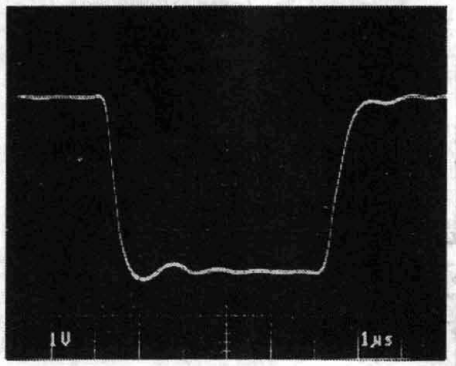
Another effect that is common to all opamps is the phase shift caused by the feedback resistor and the input capacitance. This phase shift also reduces phase margin. This effect is taken care of at the same time as the effect of the capacitive load when the capacitor is placed across the feedback resistor.

The circuit shown in *Figure 4* was used for these scope photos.



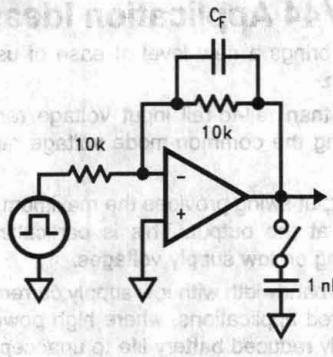
TL/H/12057–8

FIGURE 3a



TL/H/12057–9

FIGURE 3b



TL/H/12057–10

FIGURE 4

Typical Applications

FISH FINDER/ DEPTH SOUNDER.

The LM6142/44 is an excellent choice for battery operated fish finders. The low supply current, high gain-bandwidth and full rail to rail output swing of the LM6142 provides an ideal combination for use in this and similar applications.

ANALOG TO DIGITAL CONVERTER BUFFER

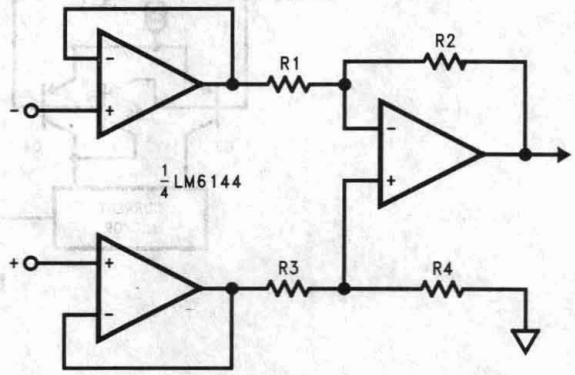
The high capacitive load driving ability, rail-to-rail input and output range with the excellent CMR of 82 dB, make the LM6142/44 a good choice for buffering the inputs of A to D converters.

3 OPAMP INSTRUMENTATION AMP WITH RAIL-TO-RAIL INPUT AND OUTPUT

Using the LM6144, a 3 opamp instrumentation amplifier with rail-to-rail inputs and rail to rail output can be made. These features make these instrumentation amplifiers ideal for single supply systems.

Some manufacturers use a precision voltage divider array of 5 resistors to divide the common-mode voltage to get an input range of rail-to-rail or greater. The problem with this method is that it also divides the signal, so to even get unity gain, the amplifier must be run at high closed loop gains. This raises the noise and drift by the internal gain factor and lowers the input impedance. Any mismatch in these precision resistors reduces the CMR as well. Using the LM6144, all of these problems are eliminated.

In this example, amplifiers A and B act as buffers to the differential stage *(Figure 5).* These buffers assure that the input impedance is over 100 MΩ and they eliminate the requirement for precision matched resistors in the input stage. They also assure that the difference amp is driven from a voltage source. This is necessary to maintain the CMR set by the matching of R1–R2 with R3–R4.



TL/H/12057–13

FIGURE 5

The gain is set by the ratio of R2/R1 and R3 should equal R1 and R4 equal R2. Making R4 slightly smaller than R2 and adding a trim pot equal to twice the difference between R2 and R4 will allow the CMR to be adjusted for optimum.

With both rail to rail input and output ranges, the inputs and outputs are only limited by the supply voltages. Remember that even with rail-to-rail output, the output can not swing past the supplies so the combined common mode voltage plus the signal should not be greater than the supplies or limiting will occur.

SPICE MACROMODEL

A SPICE macromodel of this and many other National Semiconductor opamps is available at no charge from the NSC Customer Response Group at 800-272-9959.

National Semiconductor

Audio Noise Reduction Selection Guide

Part Number	NR Type	NR Effect	Encoding Required	Single/ Dual	Decode S/N	Supply Range	Package (Pin Count)
LM1131	Dolby®	10 dB	Yes	Dual	90 dB	5V to 20V	Dip(18)
LM1894	DNR®	12 dB	No	Dual	76 dB	4.5V to 18V	Dip(14), SO(14)

National Semiconductor

LM1131A/LM1131B/LM1131C
Dual Dolby® B-Type Noise Reduction Processor

General Description

The LM1131 is a monolithic integrated circuit specifically designed to realize the Dolby B-Type noise reduction system.

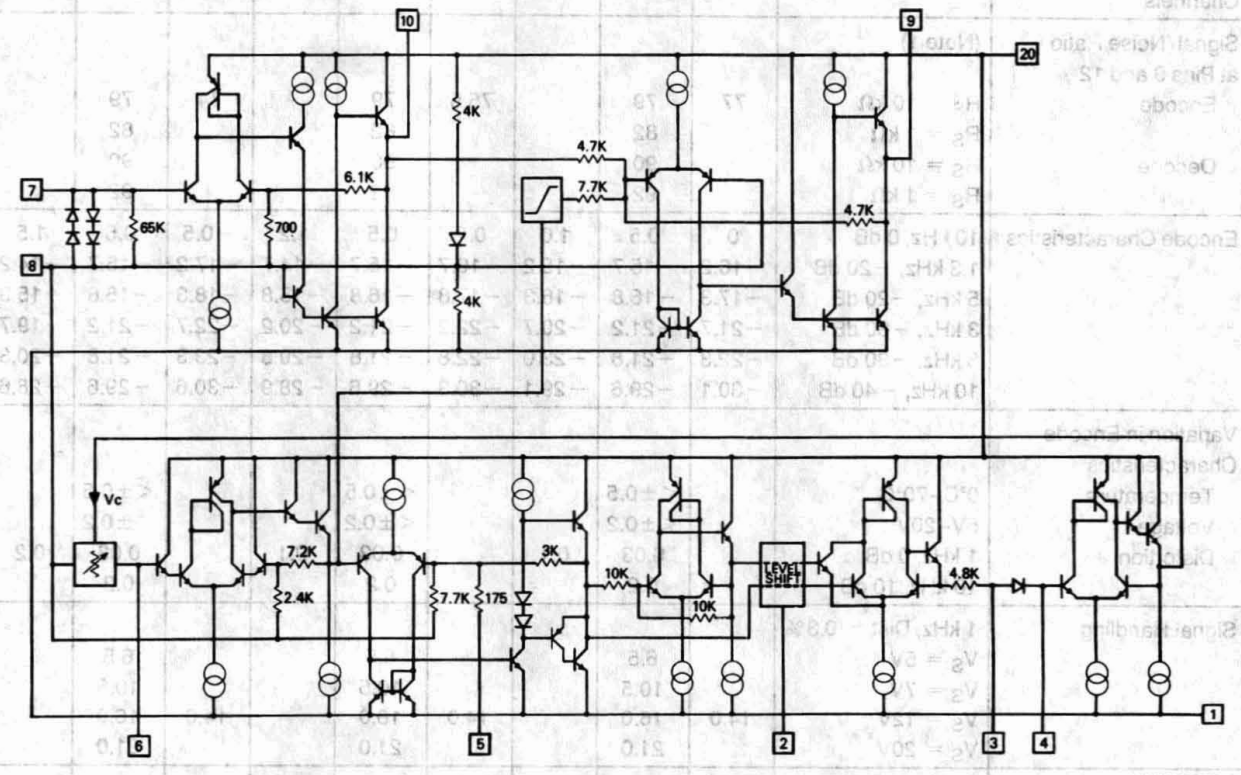
The circuit includes two completely separate noise reduction processors and will operate in both encode and decode modes. It is ideal for stereo applications in compact equipment or for mono applications in 3-head equipment where two processors with very closely matched internal gains are required.

Features

- Stereo Dolby noise reduction with one IC
- Wide supply voltage range, 5V–20V
- Very high signal/noise ratio, 79 dB encode, 90 dB decode (CCIR/ARM)
- Very close gain matching for 3-head recorders
- Close matching to standard Dolby characteristics
- Very low temperature drift of Dolby characteristics
- High signal handling capability, $> +20$ dB ($V_S = 20V$)
- Full-wave rectifier in both channels
- Operates with both single and split supply voltages
- Excellent transient response characteristics
- Minimal input switch-on transients
- Reduced number of external components per channel
- Improved input protection

Available to licensees of Dolby Laboratories Licensing Corporation, San Francisco, from whom licensing and application information must be obtained.

Schematic Diagram (1 channel shown only)



TL/H/6858–1

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	24V
Operating Temperature Range	−20°C to +70°C
Storage Temperature Range	−65°C to +150°C

Soldering Information

Dual-In-Line Package	
Soldering (10 seconds)	260°C
Small Outline Package	
Vapor Phase (60 seconds)	215°C
Infrared (15 seconds)	220°C

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.

Electrical Characteristics

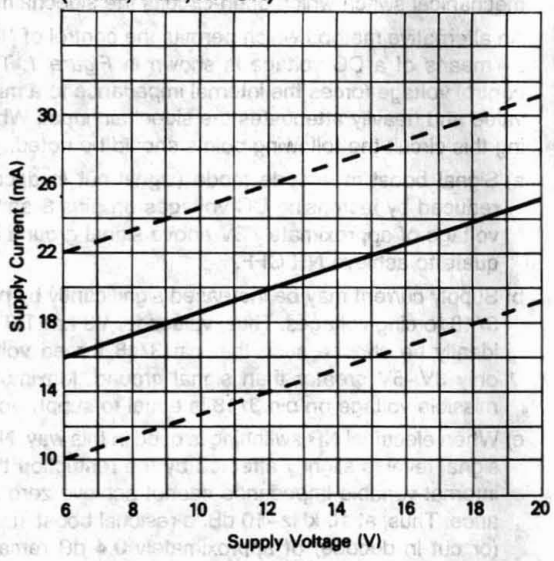
V_S = 12V, T_A = 25°C unless otherwise specified. 0 dB refers to Dolby level and is 580 mV, measured at TP1 and TP2.

Parameter	Conditions	LM1131A			LM1131B			LM1131C			Units
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Supply Voltage Range		5		20	5		20	5		20	V
Supply Current			20			20		20			mA
Voltage Gain											
(Pins 7-10 and 14-11)	1 kHz Decode	19.2	19.7	20.2	18.7	19.7	20.7	18.2	19.7	21.2	dB
(Pins 10-9 and 11-12)	1 kHz Decode	−0.5	0	0.5	−0.5	0	0.5	−1.0	0	1.0	dB
Difference in Voltage	1 kHz Noise	−0.2	0	0.2	−0.5	0	0.5	−1.0	0	1.0	dB
Gain between Channels	Reduction OFF										
Crosstalk between Channels	1 kHz, 0 dB	−60	−90		−60	−90		−60	−90		dB
Signal/Noise Ratio at Pins 9 and 12	(Note 1)										
Encode	R_S = 10 kΩ	77	79		75.5	79		74	79		dB
	R_S = 1 kΩ		82			82			82		dB
Decode	R_S = 10 kΩ		90			90			90		dB
	R_S = 1 kΩ		92			92			92		dB
Encode Characteristics	10 kHz, 0 dB	0	0.5	1.0	0.2	0.5	1.2	−0.5	0.5	1.5	dB
	1.3 kHz, −20 dB	−16.2	−15.7	−15.2	−16.7	−15.7	−14.7	−17.2	−15.7	−14.2	dB
	5 kHz, −20 dB	−17.3	−16.8	−16.3	−17.8	−16.8	−15.8	−18.3	−16.8	−15.3	dB
	3 kHz, −30 dB	−21.7	−21.2	−20.7	−22.2	−21.2	−20.2	−22.7	−21.2	−19.7	dB
	5 kHz, −30 dB	−22.3	−21.8	−23.0	−22.8	−21.8	−20.8	−23.3	−21.8	−20.3	dB
	10 kHz, −40 dB	−30.1	−29.6	−29.1	−30.3	−29.6	−28.9	−30.6	−29.6	−28.6	dB
Variation in Encode Characteristics											
Temperature	0°C–70°C		< ±0.5			< ±0.5			< ±0.5		dB
Voltage	5V–20V		< ±0.2			< ±0.2			< ±0.2		dB
Distortion	1 kHz, 0 dB		0.03	0.1		0.03	0.1		0.03	0.2	%
	10 kHz, 10 dB		0.2			0.2			0.2		%
Signal Handling	1 kHz, Dist = 0.3%										
	V_S = 5V		6.5			6.5			6.5		dB
	V_S = 7V		10.5			10.5			10.5		dB
	V_S = 12V	14.0	16.0		14.0	16.0		14.0	16.0		dB
	V_S = 20V		21.0			21.0			21.0		dB
Input Resistance	Pins 7 and 14	45	65	80	45	65	80	45	65	80	kΩ
Output Resistance	Pins 9 and 12		30	55		30	55		30	55	Ω
	Pins 10 and 11		30	55		30	55		30	55	Ω

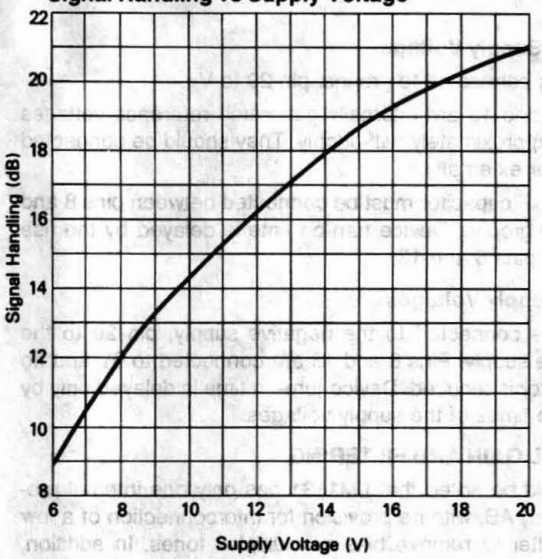
Note 1: Gaussian noise, measured over a period of 50 ms per channel, with a CCIR filter referenced to 2 kHz and an average-responding meter.

Typical Performance Characteristics

Supply Current vs Supply Voltage (1 kHz, 0 dB; NR ON)



Signal Handling vs Supply Voltage



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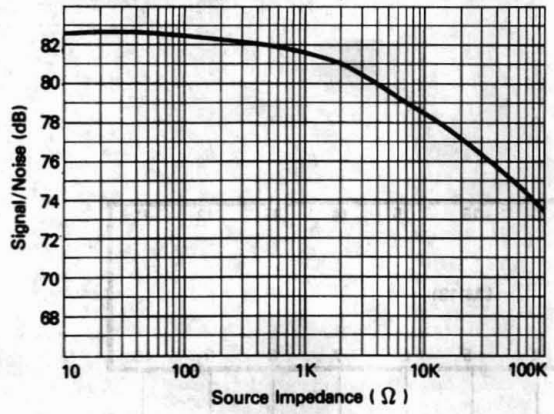
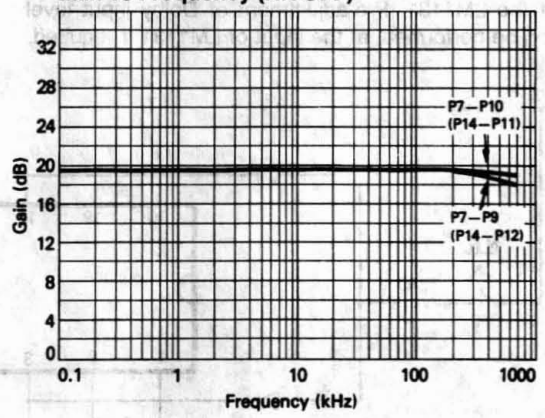
Signal to Noise Ratio vs Source Impedance Encode Mode (CCIR/ARM)

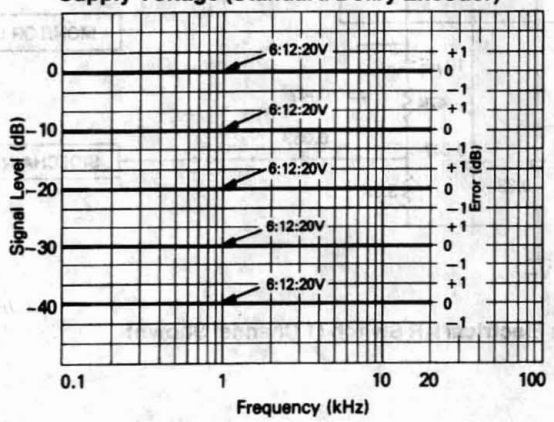


Gain vs Frequency (NR OFF)

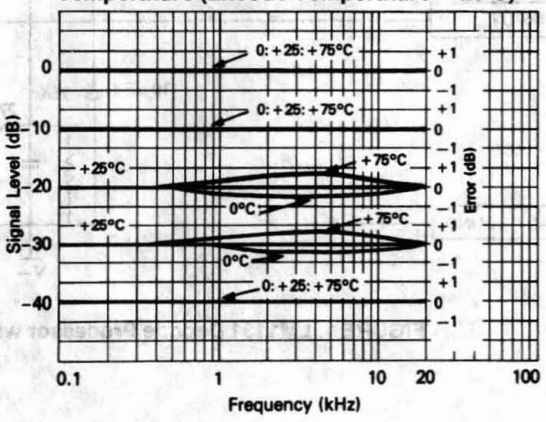


TL/H/6858–3

Back to Back Response Error vs Frequency and Supply Voltage (Standard Dolby Encoder)



Back to Back Response Error vs Frequency and Temperature (Encode Temperature + 25°C)



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Application Notes

SUPPLY VOLTAGE

LM1131 may operate with either single or split supply voltages.

Single Supply Voltage

Pin 1 is connected to ground, pin 20 to V_S.

Pins 8 and 13 are internally generated reference voltages set to approximately half-supply. They should be connected together externally.

A 220 μF capacitor must be connected between pins 8 and 13 and ground. Device turn-on time is delayed by the rise time of pins 8 and 13.

Split Supply Voltages

Pin 1 is connected to the negative supply, pin 20 to the positive supply. Pins 8 and 13 are connected to 0V and no capacitor is required. Device turn-on time is delayed only by the rise times of the supply voltages.

SIGNAL GAIN AND FILTERING

It should be noted that LM1131 has only one internal preamplifier, AB, with no provision for interconnection of a low pass filter to remove bias or multiplex tones. In addition, main chain gain has been reduced by 6 dB in comparison with LM1112/LM1011.

If a low pass filter is required it should be connected at the input of the LM1131. Pre-adjustment of Dolby input level may then be performed, at the input of LM1131 if required.

NOISE REDUCTION SWITCH

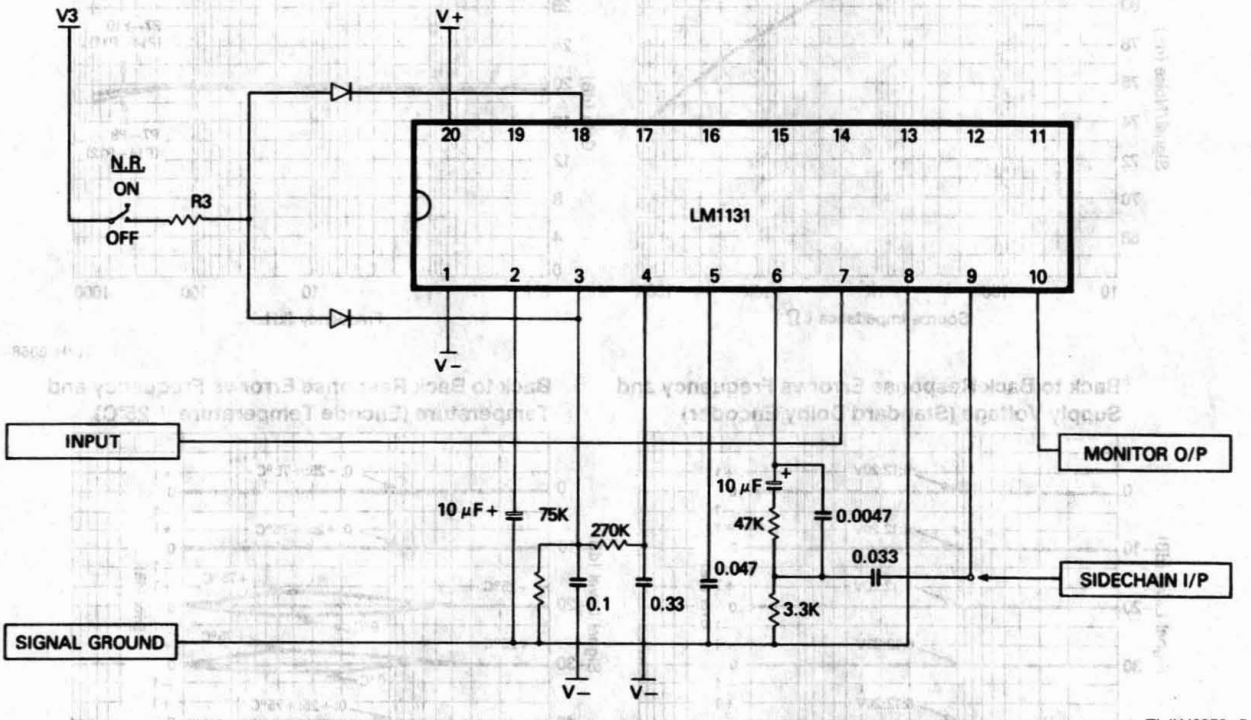
Noise reduction OFF is normally effected by means of a mechanical switch which open-circuits the sidechain input.

An alternative method which permits the control of NR OFF by means of a DC voltage is shown in *Figure 1*. The DC control voltage forces the internal impedance to a minimum value and heavily attenuates the sidechain input. When using this circuit the following points should be noted:

a) Signal boost in encode mode (signal cut in decode) is reduced by increasing DC voltages on pins 3 and 18. A voltage of approximately 3V above signal ground is adequate to achieve NR OFF.

b) Supply current may be increased significantly by high pin 3/18 forcing voltages. Thus, values for V3 and R3 should ideally be chosen such that pin 3/18 forced voltage is only 3V–5V greater than signal ground. Maximum permissible voltage on pin 3/18 is equal to supply voltage.

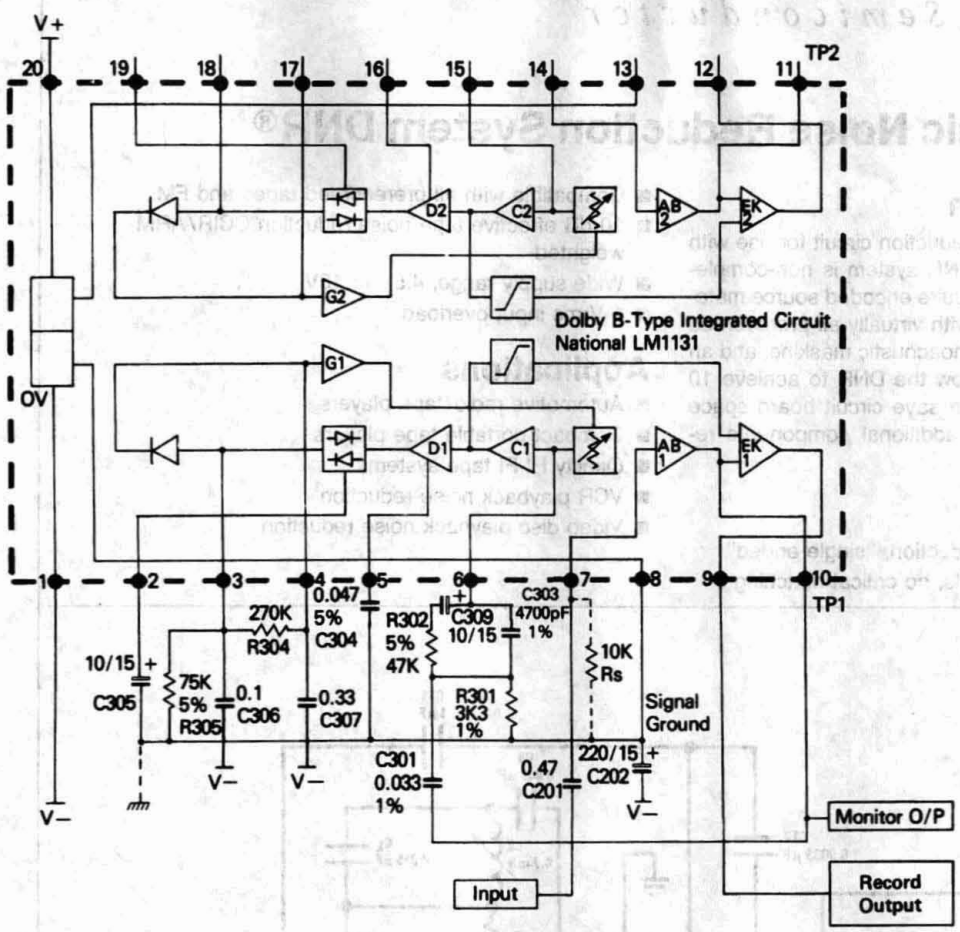
c) When electrical NR switching is used in this way, NR OFF signal level is slightly affected by the restriction that the internal variable impedance cannot achieve zero impedance. Thus, at 10 kHz–10 dB, a residual boost in encode (or cut in decode) of approximately 0.4 dB remains. At low frequencies this value reduces to insignificant levels. This is not the case for mechanical NR switching.



TL/H/6858–5

FIGURE 1. LM1131 Decode Processor with Electrical NR Switch (1 Channel Shown)

Test Circuit Encode Mode (components shown for channel 1 only)



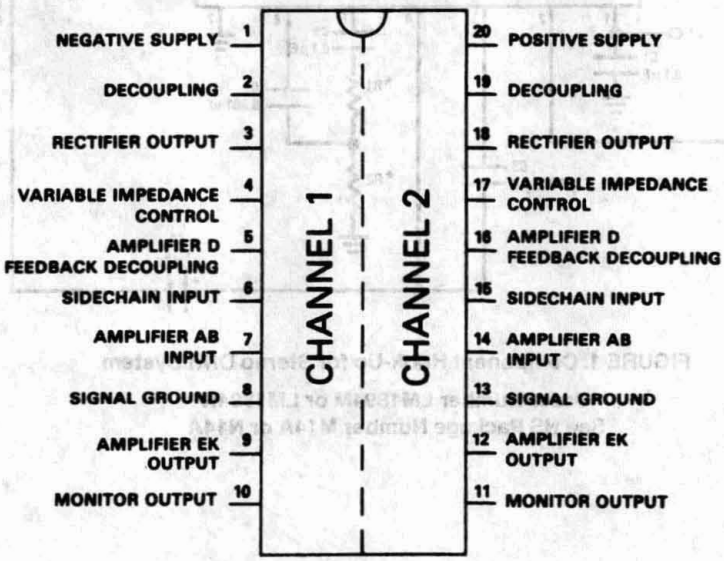
Note 1: Where not otherwise specified component tolerances are ±10%

Note 2: For LM1131AN use 2% components for C304, R303, R305. (5% components may cause errors up to ± 0.3 dB).

TL/H/6858–6

Connection Diagram

Dual-In-Line and Small Outline Packages



TL/H/6858–7

Order Number LM1131AN, LM1131BN, LM1131CM or LM1131CN
See NS Package Number M20B or N20A

National Semiconductor

LM1894 Dynamic Noise Reduction System DNR®

General Description

The LM1894 is a stereo noise reduction circuit for use with audio playback systems. The DNR system is non-complementary, meaning it does not require encoded source material. The system is compatible with virtually all prerecorded tapes and FM broadcasts. Psychoacoustic masking, and an adaptive bandwidth scheme allow the DNR to achieve 10 dB of noise reduction. DNR can save circuit board space and cost because of the few additional components required.

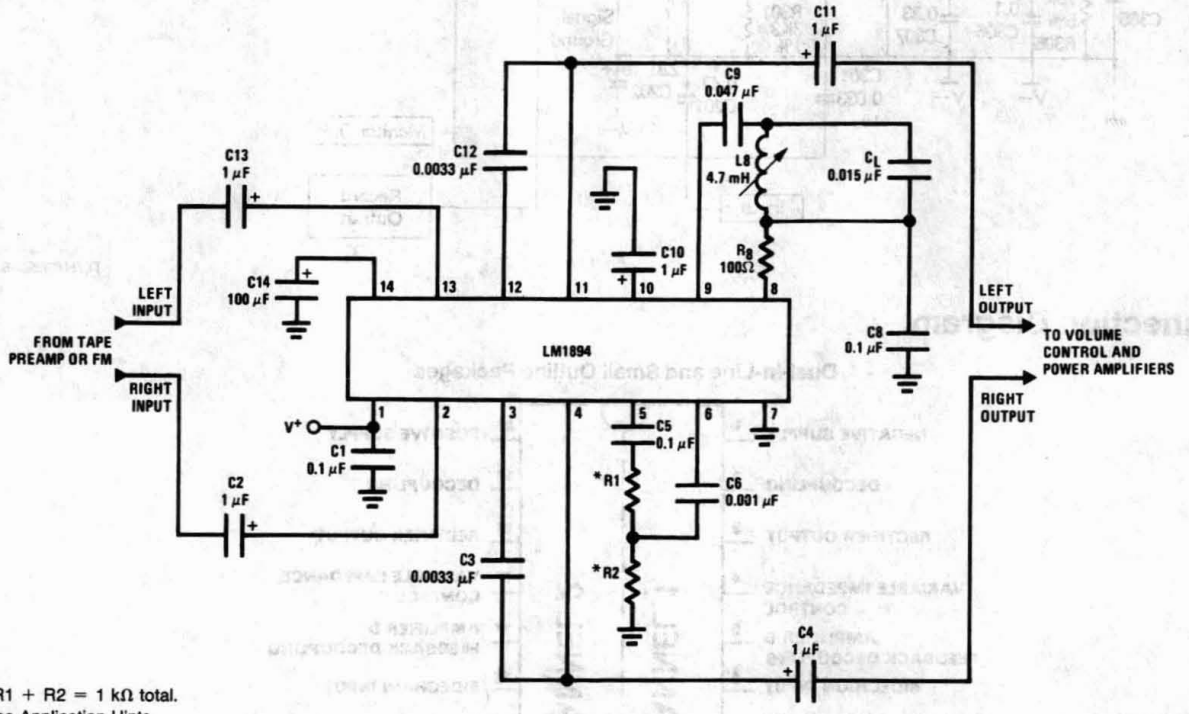
Features

- Non-complementary noise reduction, "single ended"
- Low cost external components, no critical matching
- Compatible with all prerecorded tapes and FM
- 10 dB effective tape noise reduction CCIR/ARM weighted
- Wide supply range, 4.5V to 18V
- 1 Vrms input overload

Applications

- Automotive radio/tape players
- Compact portable tape players
- Quality HI-FI tape systems
- VCR playback noise reduction
- Video disc playback noise reduction

Typical Application



*R1 + R2 = 1 kΩ total.
See Application Hints.

TL/H/7918–1

FIGURE 1. Component Hook-Up for Stereo DNR System

Order Number LM1894M or LM1894N
See NS Package Number M14A or N14A

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	20V
Input Voltage Range, V_{pk}	$V_S/2$
Operating Temperature (Note 1)	0°C to +70°C
Storage Temperature	−65°C to +150°C

Soldering Information

Dual-In-Line Package	
Soldering (10 seconds)	260°C
Small Outline Package	
Vapor Phase (60 seconds)	215°C
Infrared (15 seconds)	220°C

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.

Electrical Characteristics

V_S = 8V, T_A = 25°C, V_{IN} = 300 mV at 1 kHz, circuit shown in *Figure 1* unless otherwise specified

Parameter	Conditions	Min	Typ	Max	Units
Operating Supply Range		4.5	8	18	V
Supply Current	V_S = 8V		17	30	mA
MAIN SIGNAL PATH					
Voltage Gain	DC Ground Pin 9, Note 2	−0.9	−1	−1.1	V/V
DC Output Voltage		3.7	4.0	4.3	V
Channel Balance	DC Ground Pin 9	−1.0		1.0	dB
Minimum Balance	AC Ground Pin 9 with 0.1 μF Capacitor, Note 2	675	965	1400	Hz
Maximum Bandwidth	DC Ground Pin 9, Note 2	27	34	46	kHz
Effective Noise Reduction	CCIR/ARM Weighted, Note 3		−10	−14	dB
Total Harmonic Distortion	DC Ground Pin 9		0.05	0.1	%
Input Headroom	Maximum V_{IN} for 3% THD AC Ground Pin 9		1.0		Vrms
Output Headroom	Maximum V_{OUT} for 3% THD DC Ground Pin 9		V_S − 1.5		Vp-p
Signal to Noise	BW = 20 Hz–20 kHz, re 300 mV				
	AC Ground Pin 9		79		dB
	DC Ground Pin 9		77		dB
	CCIR/ARM Weighted re 300 mV Note 4				
	AC Ground Pin 9	82	88		dB
	DC Ground Pin 9	70	76		dB
	CCIR Peak, re 300 mV, Note 5				
	AC Ground Pin 9		77		dB
	DC Ground Pin 9		64		dB
Input Impedance	Pin 2 and Pin 13	14	20	26	kΩ
Channel Separation	DC Ground Pin 9	−50	−70		dB
Power Supply Rejection	C14 = 100 μF, V_{RIPPLE} = 500 mVrms, f = 1 kHz	−40	−56		dB
Output DC Shift	Reference DVM to Pin 14 and Measuree Output DC Shift from Minimum to Maximum Bandwidth, Note 6.		4.0	20	mV

Electrical Characteristics

V_S = 8V, T_A = 25°C, V_{IN} = 300 mV at 1 kHz, circuit shown in *Figure 1* unless otherwise specified (Continued)

Parameter	Conditions	Min	Typ	Max	Units
CONTROL SIGNAL PATH					
Summing Amplifier Voltage Gain	Both Channels Driven	0.9	1	1.1	V/V
Gain Amplifier Input Impedance	Pin 6	24	30	39	kΩ
Voltage Gain	Pin 6 to Pin 8	21.5	24	26.5	V/V
Peak Detector Input Impedance	Pin 9	560	700	840	Ω
Voltage Gain	Pin 9 to Pin 10	30	33	36	V/V
Attack Time	Measured to 90% of Final Value with 10 kHz Tone Burst	300	500	700	μs
Decay Time	Measured to 90% of Final Value with 10 kHz Tone Burst	45	60	75	ms
DC Voltage Range	Minimum Bandwidth to Maximum Bandwidth	1.1		3.8	V

Note 1: For operation in ambient temperature above 25°C, the device must be derated based on a 150°C maximum junction temperature and a thermal resistance of 1) 80°C/W junction to ambient for the dual-in-line package, and 2) 105°C/W junction to ambient for the small outline package.

Note 2: To force the DNR system into maximum bandwidth, DC ground the input to the peak detector, pin 9. A negative temperature coefficient of −0.5%/°C on the bandwidth, reduces the maximum bandwidth at increased ambient temperature or higher package dissipation. AC ground pin 9 or pin 6 to select minimum bandwidth. To change minimum and maximum bandwidth, see Appliction Hints.

Note 3: The maximum noise reduction CCIR/ARM weighted is about 14 dB. This is accomplished by changing the bandwidth from maximum to minimum. In actual operation, minimum bandwidth is not selected, a nominal minimum bandwidth of about 2 kHz gives −10 dB of noise reduction. See Application Hints.

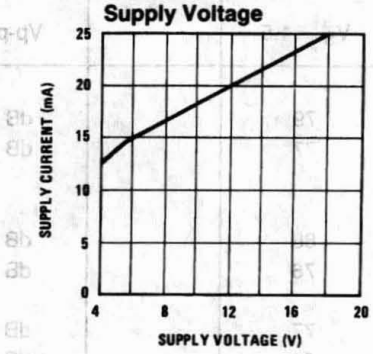
Note 4: The CCIR/ARM weighted noise is measured with a 40 dB gain amplifier between the DNR system and the CCIR weighting filter; it is then input referred.

Note 5: Measured using the Rhode-Schwartz psophometer.

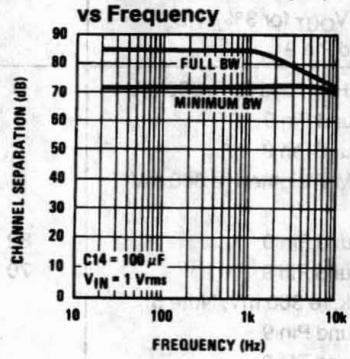
Note 6: Pin 10 is DC forced half way between the maximum bandwidth DC level and minimum bandwidth DC level. An AC 1 kHz signal is then applied to pin 10. Its peak-to-peak amplitude is V_{DC} (max BW) − V_{DC} (min BW).

Typical Performance Characteristics

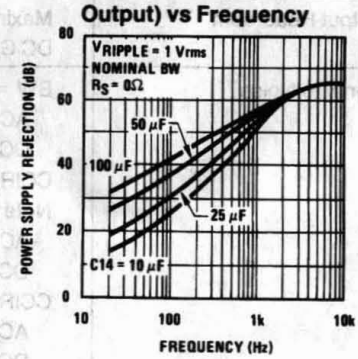
Supply Current vs Supply Voltage



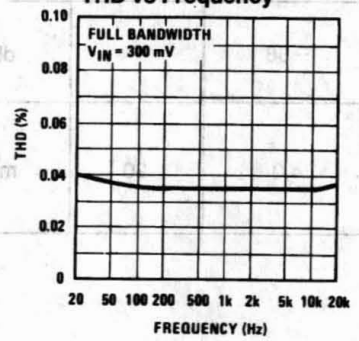
Channel Separation (Referred to the Output) vs Frequency



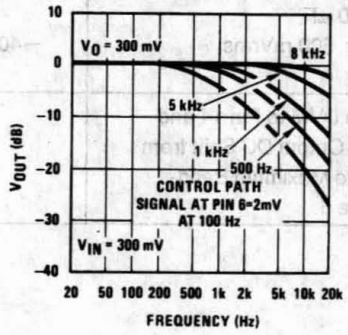
Power Supply Rejection Ratio (Referred to the Output) vs Frequency



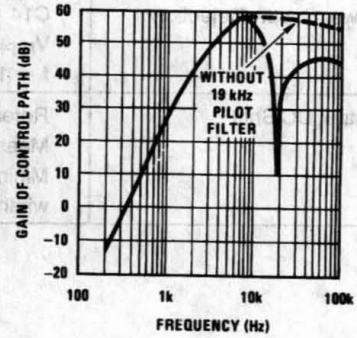
THD vs Frequency



−3 dB Bandwidth vs Frequency and Control Signal



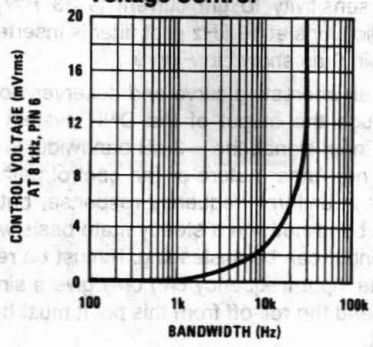
Gain of Control Path vs Frequency (with 10 kHz FM Pilot Filter)



TL/H/7918–2

Typical Performance Characteristics (Continued)

Main Signal Path Bandwidth vs Voltage Control



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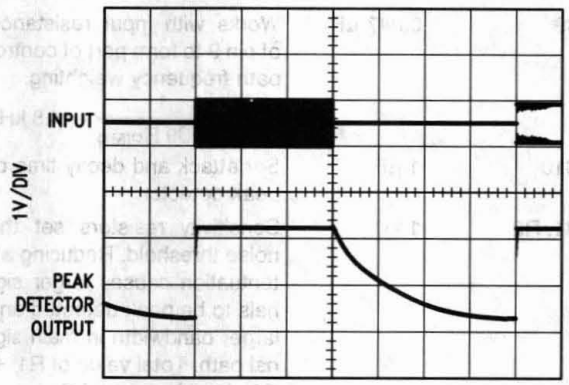
Peak Detector Response



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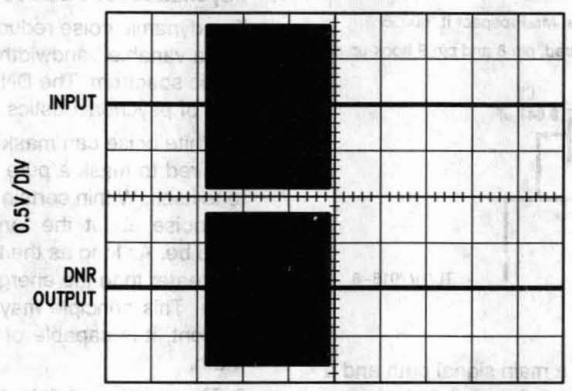
Output Response



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External Component Guide *(Figure 1)*

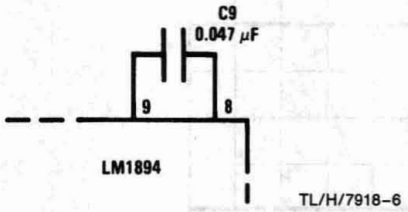
Component	Value	Purpose
C1	0.1 μF–100 μF	May be part of power supply, or may be added to suppress power supply oscillation.
C2, C13	1 μF	Blocks DC, pin 2 and pin 13 are at DC potential of $V_S/2$. C2, C13 form a low frequency pole with 20k R_{IN}. $f_L = \frac{1}{2\pi\ C2\ R_{IN}}$
C14	25 μF–100 μF	Improves power supply rejection.
C3, C12	0.0033 μF	Forms integrator with internal gm block and op amp. Sets bandwidth conversion gain of 33 Hz/μA of gm current.
C4, C11	1 μF	Output coupling capacitor. Output is at DC potential of $V_S/2$.
C5	0.1 μF	Works with R1 and R2 to attenuate low frequency transients which could disturb control path operation. $f_5 = \frac{1}{2\pi\ C5\ (R1 + R2)} = 1.6\ kHz$
C6	0.001 μF	Works with input resistance of pin 6 to form part of control path frequency weighting. $f_6 = \frac{1}{2\pi\ C6\ R1_{PIN\ 6}} = 5.3\ kHz$
C8	0.1 μF	Combined with L8 and C_L forms 19 kHz filter for FM pilot. This is only required in FM applications (Note 1).

External Component Guide (Figure 1)
(Continued)

Component	Value	Purpose
L8, C_L	4.7 mH, 0.015 μF	Forms 19 kHz filter for FM pilot. L8 is Toko coil CAN-1A185HM* (Note 1).
C9	0.047 μF	Works with input resistance of pin 9 to form part of control path frequency weighting. $f_9 = \frac{1}{2\pi\ C9\ R_{PIN\ 9}} = 4.8$ kHz
C10	1 μF	Set attack and decay time of peak detector.
R1, R2	1 kΩ	Sensitivity resistors set the noise threshold. Reducing attentuation causes larger signals to be peak detected and larger bandwidth in main signal path. Total value of R1 + R2 should equal 1 kΩ.
R8	100Ω	Forms RC roll-off with C8. This is only required in FM applications.

* Toko America Inc., 1250 Feehanville Drive, Mt. Prospect IL 60056

Note 1: When FM applications are not required, pin 8 and pin 9 hook-up as follows:



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Circuit Operation

The LM1894 has two signal paths, a main signal path and a bandwidth control path. The main path is an audio low pass filter comprised of a gm block with a variable current, and an op amp configured as an integrator. As seen in *Figure 2*, DC feedback constrains the low frequency gain to $A_V = -1$. Above the cutoff frequency of the filter, the output decreases at −6 dB/oct due to the action of the 0.0033 μF capacitor.

The purpose of the control paths is to generate a bandwidth control signal which replicates the ear's sensitivity to noise in the presence of a tone. A single control path is used for both channels to keep the stereo image from wandering. This is done by adding the right and left channels together in the summing amplifier of *Figure 2*. The R1, R2 resistor divider adjusts the incoming noise level to open slightly the bandwidth of the low pass filter. Control path gain is about 60 dB and is set by the gain amplifier and peak detector gain. This large gain is needed to ensure the low pass filter bandwidth can be opened by very low noise floors. The capacitors between the summing amplifier output and the peak detector input determine the frequency weighting as shown in the typical performance curves. The 1 μF capacitor at pin 10, in conjunction with internal resistors, sets the attack and decay times. The voltage is converted into a proportional current which is fed into the gm blocks. The bandwidth sensitivity to gm current is 33 Hz/μA. In FM stereo applications at 19 kHz pilot filter is inserted between pin 8 and pin 9 as shown in *Figure 1*.

Figure 3 is an interesting curve and deserves some discussion. Although the output of the DNR system is a linear function of input signal, the −3 dB bandwidth is not. This is due to the non-linear nature of the control path. The DNR system has a uniform frequency response, but looking at the −3 dB bandwidth on a steady state basis with a single frequency input can be misleading. It must be remembered that a single input frequency can only give a single −3 dB bandwidth and the roll-off from this point must be a smooth −6 dB/oct.

A more accurate evaluation of the frequency response can be seen in *Figure 4*. In this case the main signal path is frequency swept, while the control path has a constant frequency applied. It can be seen that different control path frequencies each give a distinctive gain roll-off.

Psychoacoustic Basics

The dynamic noise reduction system is a low pass filter that has a variable bandwidth of 1 kHz to 30 kHz, dependent on music spectrum. The DNR system operates on three principles of psychoacoustics.

1. White noise can mask pure tones. The total noise energy required to mask a pure tone must equal the energy of the tone itself. Within certain limits, the wider the band of masking noise about the tone, the lower the noise amplitude need be. As long as the total energy of the noise is equal to or greater than the energy of the tone, the tone will be inaudible. This principle may be turned around; when music is present, it is capable of masking noise in the same bandwidth.

2. The ear cannot detect distortion for less than 1 ms. On a transient basis, if distortion occurs in less than 1 ms, the ear acts as an integrator and is unable to detect it. Because of this, signals of sufficient energy to mask noise open bandwidth to 90% of the maximum value in less than 1 ms. Reducing the bandwidth to within 10% of its minimum value is done in about 60 ms: long enough to allow the ambience of the music to pass through, but not so long as to allow the noise floor to become audible.

3. Reducing the audio bandwidth reduces the audibility of noise. Audibility of noise is dependent on noise spectrum, or how the noise energy is distributed with frequency. Depending on the tape and the recorder equalization, tape noise spectrum may be slightly rolled off with frequency on a per octave basis. The ear sensitivity on the other hand greatly increases between 2 kHz and 10 kHz. Noise in this region is extremely audible. The DNR system low pass filters this noise. Low frequency music will not appreciably open the DNR bandwidth, thus 2 kHz to 20 kHz noise is not heard.

Block Diagram

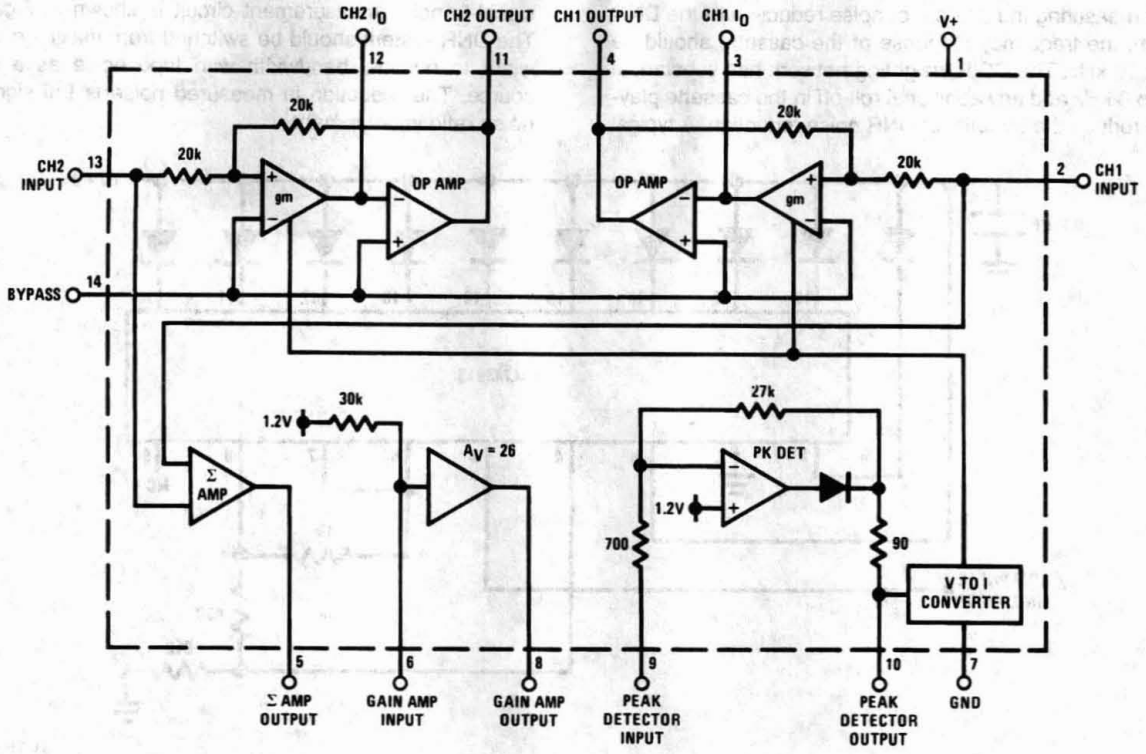

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FIGURE 2

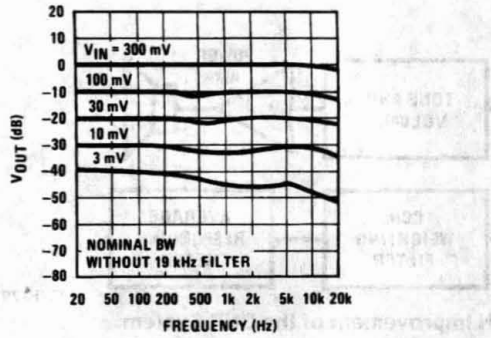

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FIGURE 3. Output vs Frequency

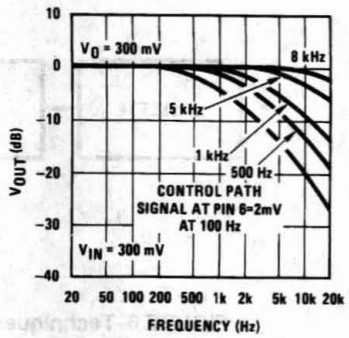

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FIGURE 4. −3 dB Bandwidth vs Frequency and Control Signal

Application Hints

The DNR system should always be placed before tone and volume controls as shown in *Figure 1*. This is because any adjustment of these controls would alter the noise floor seen by the DNR control path. The sensitivity resistors R1 and R2 may need to be switched with the input selector, depending on the noise floors of different sources, i.e., tape, FM, phono. To determine the value of R1 and R2 in a tape system for instance; apply tape noise (no program material) and adjust the ratio of R1 and R2 to open slightly the bandwidth of the main signal path. This can easily be done by viewing the capacitor voltage of pin 10 with an oscilloscope, or by using the circuit of *Figure 5*. This circuit gives an LED display of the voltage on the peak detector capacitor. Adjust the values of R1 and R2 (their sum is always 1 kΩ) to light the LEDs of pin 1 and pin 18. The LED bar graph does not indicate signal level, but rather instantaneous bandwidth of the two filters; it should not be used as a signal-level indicator. For greater flexibility in setting the bandwidth sensitivity, R1 and R2 could be replaced by a 1 kΩ potentiometer.

To change the minimum and maximum value of bandwidth, the integrating capacitors, C3 and C12, can be scaled up or down. Since the bandwidth is inversely proportional to the capacitance, changing this 0.0039 μF capacitor to 0.0033 μF will change the typical bandwidth from 965 Hz–34 kHz to 1.1 kHz–40 kHz. With C3 and C12 set at 0.0033 μF, the maximum bandwidth is typically 34 kHz. A double pole double throw switch can be used to completely bypass DNR.

The capacitor on pin 10 in conjunction with internal resistors sets the attack and decay times. The attack time can be altered by changing the size of C10. Decay times can be decreased by paralleling a resistor with C10, and increased by increasing the value of C10.

Application Hints (Continued)

When measuring the amount of noise reduction of the DNR system, the frequency response of the cassette should be flat to 10 kHz. The CCIR weighting network has substantial gain to 8 kHz and any additional roll-off in the cassette player will reduce the benefits of DNR noise reduction. A typical signal-to-noise measurement circuit is shown in *Figure 6*. The DNR system should be switched from maximum bandwidth to nominal bandwidth with tape noise as a signal source. The reduction in measured noise is the signal-to-noise ratio improvement.

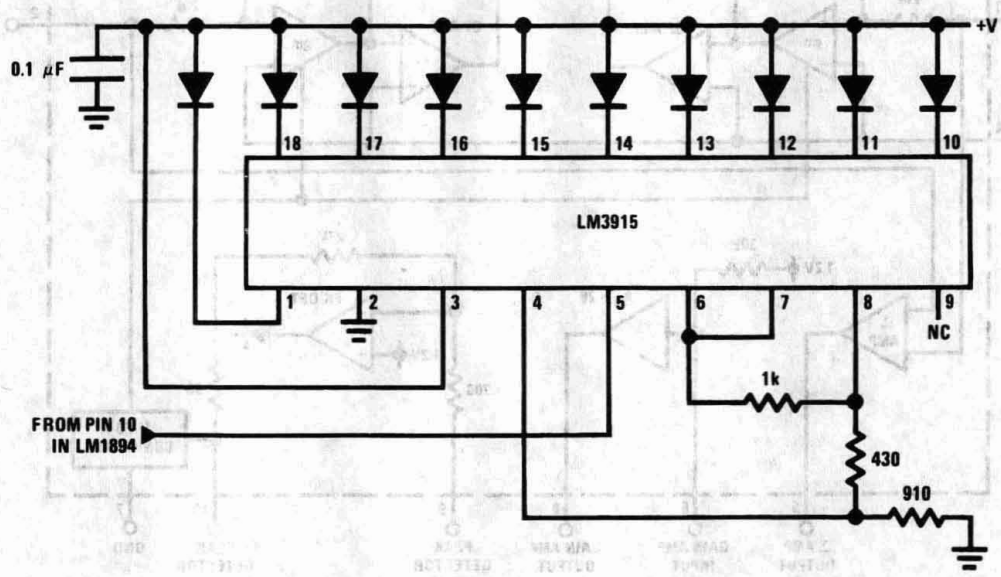

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FIGURE 5. Bar Graph Display of Peak Detector Voltage

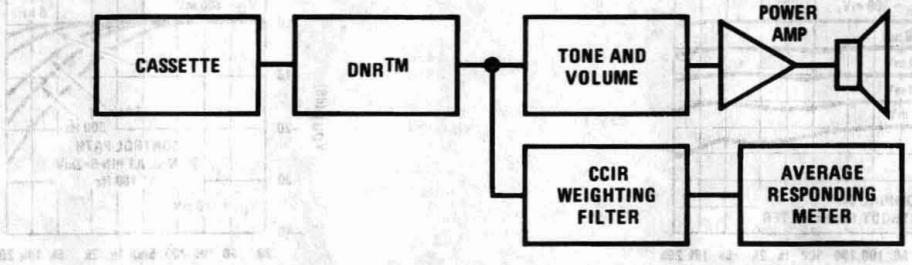

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FIGURE 6. Technique for Measuring S/N Improvement of the DNR System

Application Hints (Continued)

FOR FURTHER READING

Tape Noise Levels

1. "A Wide Range Dynamic Noise Reduction System", Blackmer, *'dB' Magazine,* August-September 1972, Volume 6, #8.

2. "Dolby B-Type Noise Reduction System", Berkowitz and Gundry, *Sert Journal,* May-June 1974, Volume 8.

3. "Cassette vs Elcaset vs Open Reel", Toole, *Audioscene Canada,* April 1978.

4. "CCIR/ARM: A Practical Noise Measurement Method", Dolby, Robinson, Gundry, *JAES,* 1978.

Noise Masking

1. "Masking and Discrimination", Bos and De Boer, *JAES,* Volume 39, #4, 1966.

2. "The Masking of Pure Tones and Speech by White Noise", Hawkins and Stevens, *JAES,* Volume 22, #1, 1950.

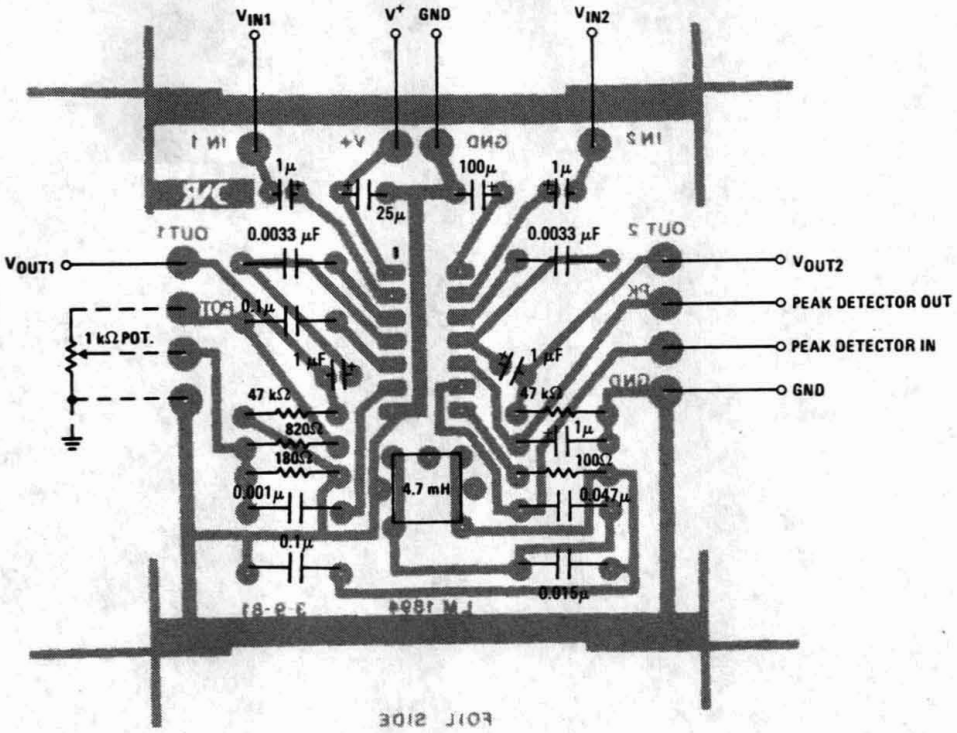
3. "Sound System Engineering", Davis Howard W. Sams and Co.

4. "High Quality Sound Reproduction", Moir, Chapman Hall, 1960.

5. "Speech and Hearing in Communication", Fletcher, Van Nostrand, 1953.

Printed Circuit Layout

DNR Component Diagram



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Section 2
Video Circuits

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LM6181 100 mA, 100 MHz Current Feedback Amplifier 2-277
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National Semiconductor

Video Circuits Selection Guide

Video Preamplifiers

Device	Pixel Clock Rate (MHz)	Typical t_r/t_f (ns)	Bandwidth (MHz)	Gain (V/V)	Supply Voltage (V)	Package	Comments
LM1202	460	1.5/1.5	230	20.0	12	20-Pin DIP	• Single Amplifier • 0V to 4V DC control on all functions • Contrast control tracking for RGB applications
LM1212	460	1.5/1.5	230	20	12	20-Pin DIP	• Single Amplifier System with OSD Blanking • 0V to 4V DC control on all functions • Contrast control tracking for RGB applications
LM1204	300	2.0/2.3	150	6.5	12	44-Pin PLCC	• Triple Amplifier System • Output stage Blanking with adjustable Blanking level • 0V to 4V DC control on all functions
LM1203A	300	2.5/3.4	150	6.5	12	28-Pin DIP	• Triple Amplifier System • 0V to 12V DC brightness and contrast control
LM1205	260	2.6/3.6	130	7.0	12	28-Pin DIP	• Triple Amplifier System with blanking • 0V to 4V DC control on all functions • Spot killer
LM1208	260	2.8/3.4	130	7.0	12	28-Pin DIP	• Triple Amplifier System with blanking • 0V to 4V DC control on all functions • Spot killer • Full Range Drive Control (40 dB)
LM1201	220	2.5/3.0	110	8.0	12	16-Pin DIP	• Single Amplifier • 0V to 12V DC brightness and contrast control
LM1209	200	3.2/3.6	100	7.0	12	28-Pin DIP	• Triple Amplifier System with blanking • 0V to 4V DC control on all functions • Spot killer • Full Range Drive Control (40 dB)
LM1203B	200	3.3/3.7	100	6.5	12	28-Pin DIP	• Triple Amplifier System • 0V to 12V DC brightness and contrast control
LM1207	170	4.3/4.3	85	7.0	12	28-Pin DIP	• Triple Amplifier System with blanking • 0V to 4V DC control on all functions • Spot killer
LM1281	170	4.3/4.3	85	7.0	12	28-Pin DIP	• Triple Amplifier and OSD System • Output stage Blanking • 0V to 4V DC control on all functions • Spot killer
LM1203	140	5/7	70	6.0	12	28-Pin DIP	• Triple Amplifier System • 0V to 12V DC brightness and contrast control

CRT Drivers

Device	Pixel Clock Rate (MHz)	Typical t_r/t_f (ns)	Bandwidth (MHz)	Gain (V/V)	Supply Voltage (V)	Package	Comments
LM2427	160	3.5	80	−13	80	12-Pin In-Line Plastic	• Triple channel CRT driver • 50 V_{PP} output swing • Closed loop design
LM2419	130	5	65	−15	80/12	11-Pin TO-220	• Triple channel CRT driver • 50 V_{PP} output swing • Open loop design
LM2416	100	8	50	−13	80/12	11-Pin TO-220	• Triple channel CRT driver • 50 V_{PP} output swing • Open loop design
LM2418	60	12	30	−19	90/12	11-Pin TO-220	• Triple channel CRT driver • 50 V_{PP} output swing • Open loop design

Video Channel Recommendations

Video Preamplifier	+	CRT Driver	Typical Calculated Video Channel t_r/t_f (ns)
LM1204		LM2427	6*
LM1205		LM2427	6.5*
LM1203A		LM2427	6.5*
LM1281		LM2427	7*
LM1281		LM2419	7
LM1205		LM2419	7
LM1203B		LM2419	7.5
LM1207		LM2416	10
LM1203		LM2418	15

*Estimated t_r/t_f includes affects of compensation networks

Video Special Functions

Device	Function	Supply Voltage	Package	Comments
LM1291	Horizontal Time Base	12V	28-Pin DIP	• Video PLL systems for Continuous Sync Monitors (15 kHz–135 kHz) • Includes Sync Separator and clamp pulse generator • Video mute signal indicates change in H input frequency
LM1295	Geometric Correction	12V	24-Pin Narrow DIP	• All correction terms are DC controlled (0V to 4V range) • Vertical dynamic focus control signal • Ramp generation for vertical deflection
LM1391	Horizontal PLL	Over 10V	8-Pin DIP	• Built-in 8.6V regulator • Linear balanced phase detector • DC controlled output duty cycle
LM1823	Video IF Amp & PLL Det.	12V	28-Pin DIP	• True synchronous video detector using PLL • 9 MHz video bandwidth • Excellent small-signal detector linearity
LM1881	Sync Separator	5V–12V	8-Pin DIP 8-Pin SO	• Generates composite sync, vertical sync, back porch clamp pulse, and Odd/Even field
LM1882	Sync Generator	5V	20-Pin DIP 20-Pin PLCC	• 130 MHz maximum clock frequency • Control via register programming with NTSC default values • Interlaced and Non-Interlaced Formats
LM2889	TV Video Modulator	12V	14-Pin DIP	• Low distortion FM sound modulator • Excellent oscillator stability • DC channel switching

National Semiconductor

Video Definition of Terms

Active Video Signal: That portion of the video signal which is above the blanking level and contains the picture information.

Arc Protection: Circuitry in the electronic systems connected to the CRT, to prevent them from being damaged by high voltage arcs within the CRT.

Arcover: An internal arc between electrodes in the CRT, which can apply high voltages to the CRT terminals.

Aspect Ratio: The ratio of picture width to picture height. For the NTSC system this is 4:3.

Back Porch: The section of the composite video signal between the trailing edge of the horizontal sync pulse and the end of the blanking pulse period (when picture information begins).

Bandwidth: The frequency at which the sine wave response of an amplifier has dropped 3 dB below the amplitude at a lower reference frequency. The reference frequency needs to be specified where the frequency response of the amplifier is very flat. The bandwidth frequency should be at least 10 times the reference frequency. The output level of the amplifier must be specified for the bandwidth specification.

Black Level: The DC voltage level in the picture signal which corresponds to beam cut-off on the display tube.

Blacker-than-Black: The amplitude region in the video signal that extends below the reference black level. The blacker-than-black is usually used for blanking.

Blanking: A portion of the video signal whose instantaneous amplitude makes the vertical and horizontal scan retrace not visible on the display tube.

Blanking Period: The period in the video signal where the level is reduced to the blanking level, below which the display electron beam is cut-off. This allows non-visible retrace of the beam from the right side of the display to the left side at the end of each scan line (horizontal blanking) and non-visible return of the electron beam from the bottom of the display to the top.

Blooming: Defocussing of the picture in regions where the brightness is too high.

Clamping: A process that established a fixed DC voltage level for the picture signal. This is important for maintaining the correct picture black level.

Composite Video Signal: A video signal that also contains the sync information. For an RGB color system the sync information is normally in the green video. Other RGB color systems may have the sync information in all three video signals. Many systems use separate syncs (no sync signal on any of the video signals). These systems would have no composite video signal.

Continuous Sync: A circuit or monitor that has the capability to lock on a range of different horizontal and vertical frequencies. The wide variety of different video standards makes a continuous sync monitor very desirable to prevent early obsolescence.

Contrast: The range of dark and light values in a picture.

Cross-talk: An undesired signal interfering with a desired signal.

CRT: Cathode Ray Tube (display tube)

CRT Driver: An amplifier which increases the 4 to 7V signal output from a preamplifier up to 50 volts, for driving the cathode of a CRT.

EMI: Electromagnetic Interference. Signals radiated or conducted from an electronic system which can interfere with the operation of another electronic system.

Equalizing Pulses: Pulses of one half the width of the horizontal sync pulses. They are used to help the vertical sync system of the monitor accommodate the half line difference in the number of scan lines on successive fields in an interlaced standard.

Field: One half of a complete picture interval in an interlaced standard. A field will contain either all the odd numbered scanning lines or all the even numbered scanning lines in the picture. For a non-interlaced standard the field and frame are the same and is the complete picture interval.

Fly-back: See Horizontal Retrace.

Frame: A complete picture. For an interlaced standard, a frame consists of two interlocking fields.

Front Porch: The section of the composite video signal between the end of the picture information on a horizontal line (start of blanking) and the start of the horizontal synchronization pulse.

Gain: An amplifier output voltage divided by input voltage. A negative value of gain means the amplifier is an inverting amplifier.

Horizontal Blanking: The blanking signal at the end of each horizontal line that prevents the retrace of the display tube electron beam from being visible.

Horizontal Retrace: The rapid return of the scanning electron beam from the right side of the raster to the left side.

Horizontal Scan Rate: The frequency at which the electron beam in a monitor is being deflected horizontally.

Interlace: A scanning process in which each adjacent line belongs to the alternate field. Note: most video standards for monitors do not use interlace.

Large Signal Bandwidth: The bandwidth of an amplifier where the output is specified near or at its largest expected output swing. For CRT drivers the specified output is typically between 40 V_{PP} and 50 V_{PP}. For video preamps the specified level is typically 4 V_{PP}.

Multi Sync: A circuit or monitor that has the capability to lock on a discrete number of preselected different video standards.

Noise: In a video picture, 'noise' refers to random interference producing a salt and pepper pattern over the picture.

Overshoot: An (excessive) response to a unidirectional signal change. Overshoot is often used deliberately to enhance the appearance of the displayed picture.

Pairing: A partial or complete failure of interlace in which scan lines of alternate fields fall in pairs, one on top of the other.

Pixel: Contraction of the words picture element. A picture displayed on a monitor is divided into very small segments, called pixels.

Pixel Clock Rate: The rate at which pixels of the incoming video are occurring.

Preamplifier: An amplifier which increases the nominal 0.7V video signal to the 4 to 7V level, as part of a video amplifier. Usually contains other functions, such as brightness, contrast and clamping.

Raster: The area on the face of the display tube that is scanned by the electron beam. This is not always entirely visible since monitors sometimes employ overscan so that the edges of the raster are hidden by the faceplate.

Resolution (Horizontal): The amount of resolvable detail in the horizontal direction of the picture. This depends on the high frequency and phase response of the monitor.

Resolution (Vertical): The amount of resolvable detail in the vertical direction of the picture. This depends primarily on the number of scan lines that are used and secondarily on the size (shape) of the electron scanning beam.

RGB Video Abbreviation for Red, Green, and Blue video. This means that there are three separate signals going to the monitor for video, each signal represents one of the three colors. Monitors used with various computers today all use RGB video.

Smear: A picture condition where the displayed video levels have an error with respect to what should be displayed. This condition is normally due to thermal shifts in the CRT driver due to a major change in the picture. As an example, if a black box is displayed in the center of the screen with a white background, the white background after the box may be either more white than the background, or slightly darker than the white background. This shift in the white level in the horizontal direction after the black box is called smear.

Spark Gap: A component connected between CRT pins (cathodes, G1, G2) and ground, to limit the arcover voltages appearing on the CRT pins.

Sync: Abbreviation for synchronizing or synchronization.

Sync Level: The level of the synchronizing pulse tips.

t_R/t_F: Rise time/fall time. During a video signal transition from one level to another, the time required to go between the 10% and 90% points of the transition.

Vertical Blanking: The blanking signal at the end of each field.

Vertical Frequency: The rate at which a complete field is scanned.

Vertical Retrace: The return of the electron beam from the bottom of the display to the top after a complete field has been scanned.

Vertical Scan Rate: The frequency at which the electron beam in a monitor is being deflected vertically.

Video: The visible portion of the video signal representing the picture. Also referred to as active video.

National Semiconductor

LM1201 Video Amplifier System

General Description

The LM1201 is a wideband video amplifier system intended for high resolution monochrome or RGB monitor applications. In addition to the wideband video amplifier the LM1201 contains a gated differential input black level clamp comparator for brightness control and an attenuator circuit for contrast control. The LM1201 also contains a voltage reference for the video input. For medium resolution RGB color monitor applications also see the LM1203 Video Amplifier System data sheet.

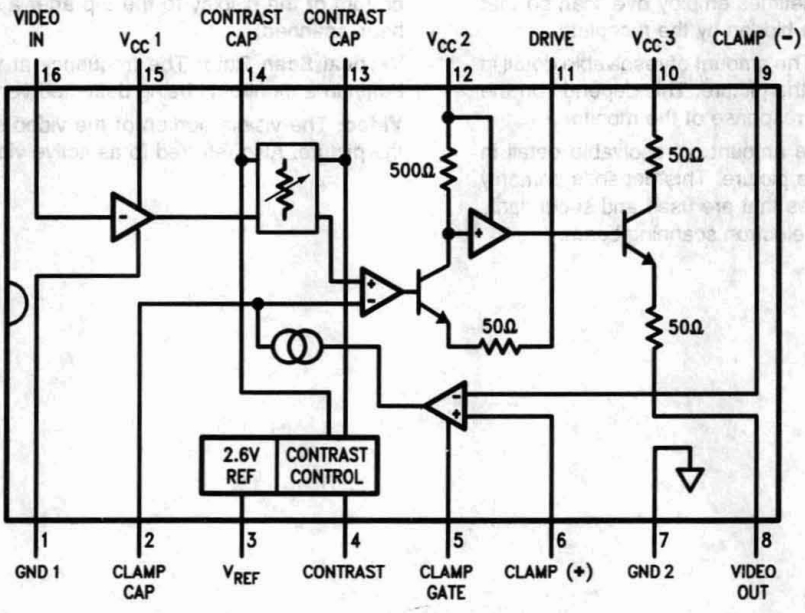
Features

- Wideband video amplifier (200 MHz @ −3 dB)
- Attenuator circuit for contrast control (>40 dB range)
- Externally gated comparator for brightness control
- Provisions for external gain set and peaking of video amplifier
- Video input voltage reference
- Low impedance output driver

Typical Applications

- CRT video amplifiers
- Video switches
- High frequency video preamplifiers
- Wideband gain controls
- PC monitors
- Workstations
- Facsimile machines
- Printers

Block and Connection Diagram



TL/H/10006–1

FIGURE 1

Order Number LM1201M or LM1201N
See NS Package Number M16A or N16E

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage V_{CC} Pins 10, 12, 15 to Ground Pins, 1, 7	13.5V
Voltage at Any Input Pin (V_{IN})	$V_{CC} \geq V_{IN} \geq$ GND
Video Output Current (I_8)	28 mA
Package Power Dissipation at T_A = 25°C (Above 25°C derate based on (θ_{JA} and T_J)	1.56W
Package Thermal Resistance (θ_{JA}) N16E	80°C/W
Package Thermal Resistance (θ_{JA}) M16A	100°C/W
Junction Temperature (T_J)	150°C
Storage Temperature Range (T_{STG})	−65°C to +150°C
Lead Temperature (Soldering, 10 sec.)	265°C
ESD Susceptibility	2 kV
Human body model: 100 pF discharged through a 1.5 kΩ resistor	

Operating Ratings (Note 4)

Temperature Range	0°C to +70°C
Supply Voltage (V_{CC})	$10.8V \leq V_{CC} \leq 13.2V$

Electrical Characteristics See Test Circuit (Figure 2), T_A = 25°C; $V_{CC1} = V_{CC2} = V_{CC3}$ = 12V

DC Static Tests S9 Open; V4 = 6V; V5 = 0V; V6 = 2.0V unless otherwise stated

Symbol	Parameter	Conditions	Typical	Tested Limit (Note 1)	Design Limit (Note 2)	Units (Limits)
I_S	Supply Current	V_{CC} Pins 12, 15 Only	45	57		mA(max)
V_3	Video Input Reference Voltage		2.65	2.4		V(min)
				2.95		V(max)
I_{16}	Video Input Bias Current	$(V_3-V_{16})/10$ kΩ	5.0	20		μA(max)
V_{5L}	Clamp Gate Low Input Voltage	Clamp Comparator On	1.2	0.8		V(min)
V_{5H}	Clamp Gate High Input Voltage	Clamp Comparator Off	1.6	2.0		V(max)
I_{5L}	Clamp Gate Low Input Current	V_5 = 0V	−0.5	−5.0		μA(max)
I_{5H}	Clamp Gate High Input Current	V_5 = 12V	0.005	1		μA(max)
I_{2+}	Clamp Cap Charge Current	V_2 = 0V	1	0.55		mA(min)
I_{2-}	Clamp Cap Discharge Current	V_2 = 5V	−1	−0.55		mA(min)
V_{8L}	Video Output Low Voltage	V_2 = 0V	0.5	0.9		V(max)
V_{8H}	Video Output High Voltage	V_2 = 5V	8.5	8.0		V(min)
V_{OS}	Comparator Input Offset Voltage	V_6-V_9	±0.5	±25		mV(max)

AC Dynamic Tests S9 Closed, V_5 = 0V, V_6 = 4V

Symbol	Parameter	Conditions	Typ	Tested Limit (Note 1)	Design Limit (Note 2)	Units (Limits)
Av max	Video Amplifier Gain	V_4 = 12V	8	5.5		V/V(min)
ΔAv 5V	Attenuation @ 5V	Ref: Av max, V_4 = 5V	−10			dB
ΔAv 2V	Attenuation @ 2V	Ref: Av max, V_4 = 2V	−45			dB
THD	Video Amplifier Distortion	V_4 = 5V, V_O = 1 V_{p-p}	0.3			%
f (−3dB)	Video Amplifier Bandwidth (Note 3)	V_4 = 12V, V_O = 100 mV_{rms}	200		170	MHz(min)
t_r	Output Rise Time (Note 3)	V_O = 4 V_{p-p}	2.5			ns
t_f	Output Fall Time (Note 3)	V_O = 4 V_{p-p}	3			ns

Note 1: These parameters are guaranteed and 100% production tested.

Note 2: Design limits are guaranteed (but not 100% production tested). These limits are not used to calculate outgoing quality levels.

Note 3: When measuring video amplifier bandwidth or pulse rise and fall times, a double sided full ground plane printed circuit board without socket is recommended.

Note 4: Operating Ratings indicate conditions of which the device is functional, but does not guarantee specific performance limits. For guaranteed specifications and test conditions, see Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.

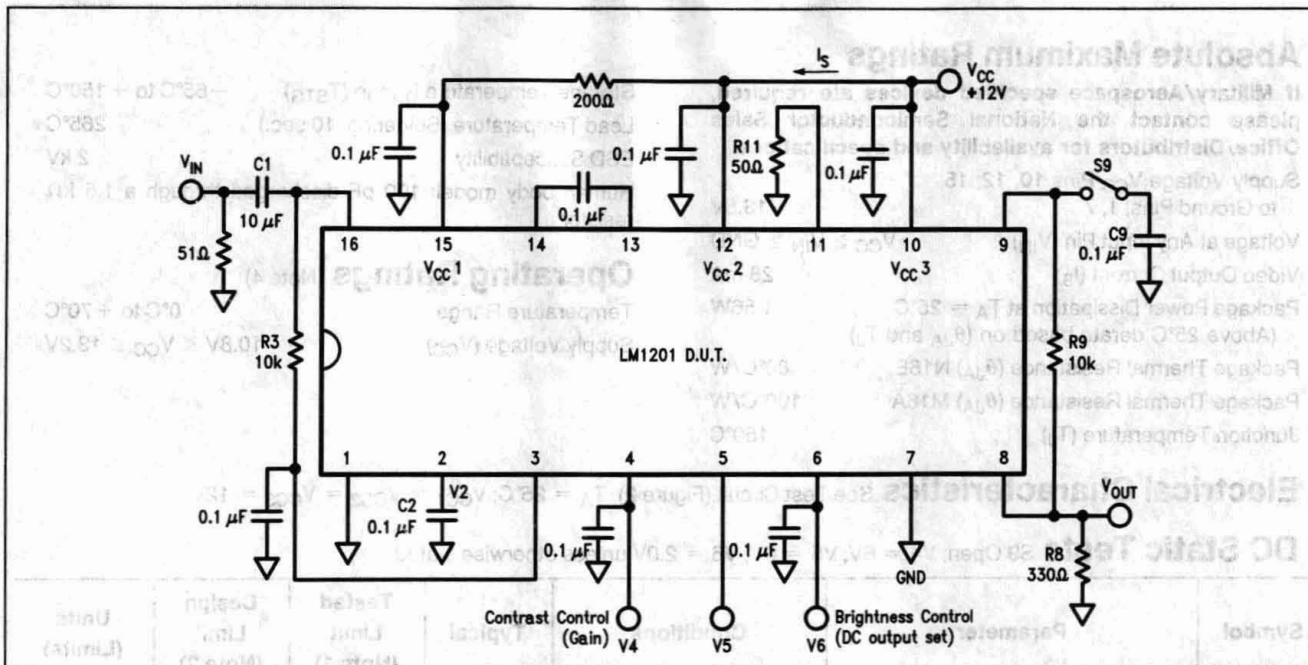


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FIGURE 2. LM1201 AC/DC Test Circuit

Note: When $V_5 \leq 0.8V$ and S9 is closed, DC feedback around the Video Amplifier is provided by the clamp comparator. Under these conditions sine wave or 50% duty cycle square waves can be used for test purposes. The low frequency dominant pole is determined by C2 at Pin 2. Capacitor C9 at pin 9 prevents overloading the clamp comparator inverting input. See applications section for additional information.

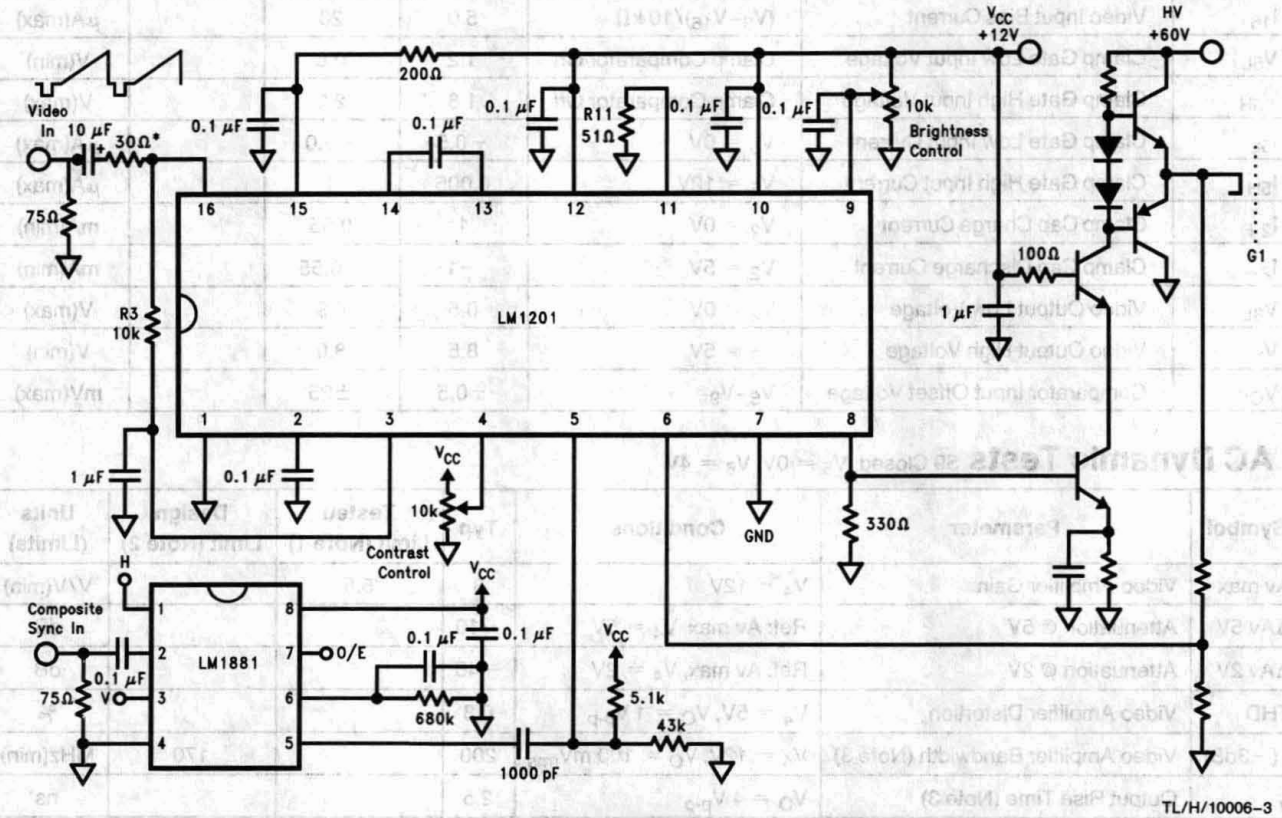

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FIGURE 3. Typical Application of the LM1201

* 30Ω resistor is added to the input pin for protection against current surges coming from the 10 μF input capacitor. By increasing this resistor to well over 100Ω the rise and fall times of the LM1201 can be increased for EMI considerations.

APPLICATIONS INFORMATION

Figure 4 shows the block diagram of a typical analog monochrome monitor. The monitor is used with CAD/CAM work stations, PCs, arcade games and in a wide range of other applications that benefit from the use of high resolution display terminals. Monitor characteristics may differ in such ways as sweep rates, screen size, or in video amplifier speed but will still be generally configured as shown in *Figure 4*. Separate horizontal and vertical sync signals may be required or they may be contained as a composite signal in the video input signal. The video input signal is usually supplied by coaxial cable which is terminated in 75Ω at the monitor input and internally AC coupled to the video amplifier. The input signal is approximately 1V peak-to-peak in amplitude and at the input of the high voltage video section, approximately 6V peak-to-peak. At the cathode of the CRT the video signals can be as high as 60V peak to peak. The block in *Figure 4* labeled "Video Amplification with DC Controlled Gain/Black Level" contains the function of the LM1201 video amplifier system.

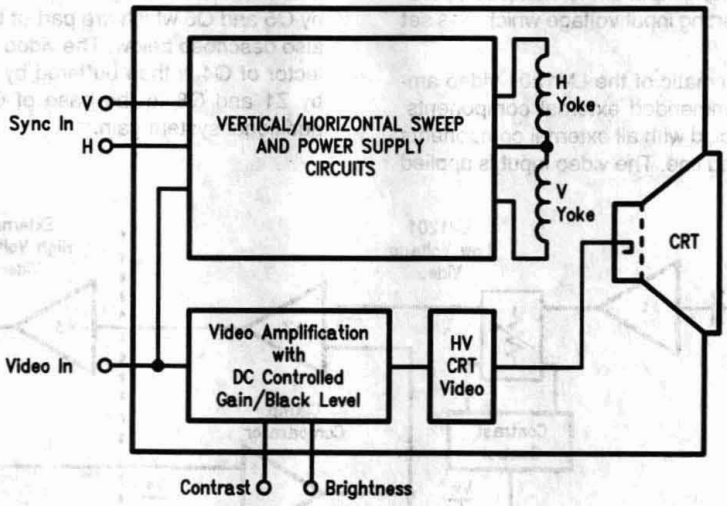

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FIGURE 4. Typical Monochrome Monitor Block Diagram

Circuit Description

Figure 5 is a block diagram of the LM1201 along with the contrast and brightness controls. The contrast control is a DC operated attenuator which varies the AC gain of the amplifier without introducing any signal distortions or DC output shift. The brightness control function requires a "sample and hold" circuit (black level clamp) which holds the DC bias of the video amplifier and CRT cathodes constant during the black level reference portion of the video waveform. The clamp comparator, when gated on during this reference period, will charge or discharge the clamp capacitor until the non-inverting input of the clamp comparator matches that of the inverting input voltage which was set by the brightness control.

Figure 6 is a simplified schematic of the LM1201 video amplifier along with the recommended external components. The IC pin numbers are circled with all external components shown outside of the dashed line. The video input is applied to pin 16 via the 10 μF coupling capacitor. DC bias to the video input is through the 10 kΩ resistor which is connected to the 2.6V reference at pin 3. The low frequency roll-off of the amplifier is set by these two components. Transistor Q1 buffers the video signal to the base of Q2. The Q2 collector current is then directed to the V_{CC1} supply through Q3 or to V_{CC2} through Q4 and the 500Ω load resistor depending upon the differential DC voltage at the bases of Q3 and Q4. The Q3 and Q4 differential base voltage is determined by the contrast control circuit which is described below. The black level DC voltage at the collector of Q4 is maintained by Q5 and Q6 which are part of the black level clamp circuit also described below. The video signal appearing at the collector of Q4 is then buffered by Q7 and level shifted down by Z1 and Q8 to the base of Q9 which will then provide additional system gain.

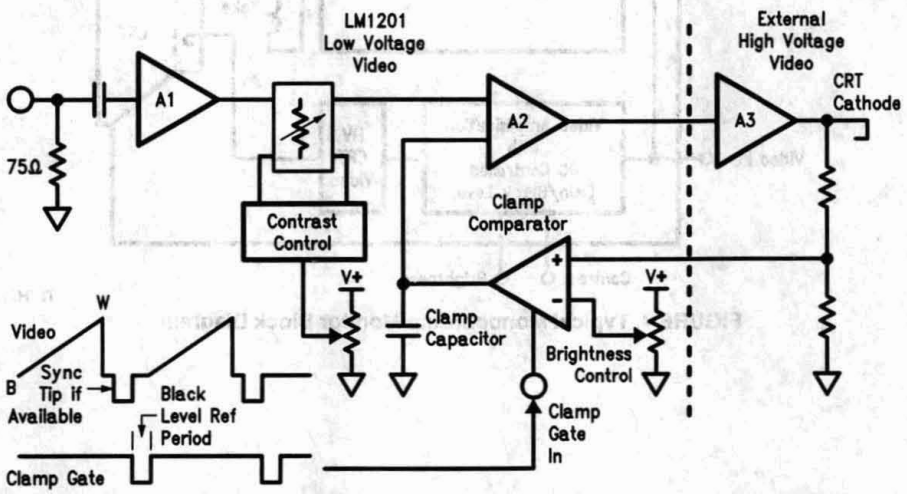

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FIGURE 5. Block Diagram of LM201 Video Amplifier with Contrast and Black Level Control

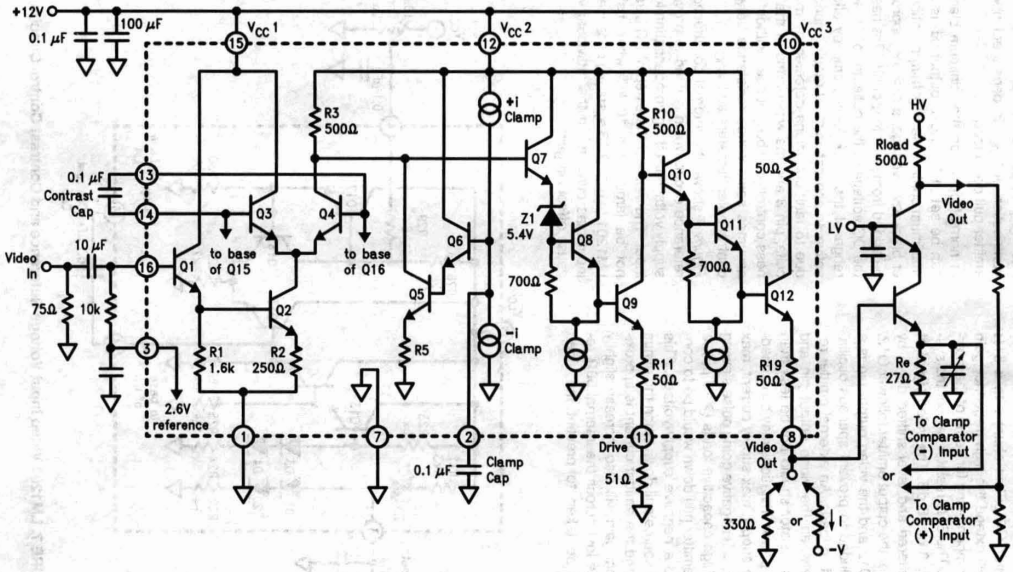

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FIGURE 6. Simplified LM1201 Video Amplifier Section with Recommended External Components

Circuit Description (Continued)

The "Drive" pin will allow the user to set the maximum gain of the amplifier based on the range of input video signal levels and the CRT stage gain if it is fixed or limited. When using three LM1201 devices for high resolution RGB applications, the "Drive" pin allows the user to trim the gain of each channel to correct for differences in the three CRT cathodes. A small capacitor (12 pF) in shunt with a 51Ω drive resistor at this pin will extend the high frequency gain of the video amplifier by compensating for some of the internal high frequency roll off. The 51Ω resistor will set the system gain to approximately 8 or 18 dB. The video signal at the collector of Q9 is buffered and level shifted down by Q10 and Q11 to the base of the output emitter follower Q12. Between the emitter of Q12 and the video output pin is a 50Ω resistor which is included to prevent spurious oscillations when driving capacitive loads. An external emitter resistor must be added between the video output pin and ground. The value of this resistor should not be less than 330Ω, otherwise package power limitations may be exceeded when worst case (high supply, max supply current, max temp) calculations are made. If negative going pulse slewing is a problem because of high capacitive loads (>10 pF), a more efficient method of emitter pull down would be to connect a suitable resistor to a negative supply voltage. This has the effect of a current source pull down when the minus supply voltage is −12V, and the emitter current is approximately 10 mA. The system gain will also increase slightly because less signal will be lost across the internal 50Ω resistor. Precautions must be taken to prevent the video output pin from going below ground since IC substrate currents may cause erratic operation. The collector current from the video output transistor is returned to the power supply at V_{CC3}, pin 10. When making power dissipation calculations note that the datasheet specifies only the V_{CC1} and V_{CC2} supply currents at 12V. The IC power dissipation contribution of V_{CC3} is dependent upon the video output emitter pull down load.

In normal operation the minimum black level voltage that can be set at the video output pin is approximately 2V at maximum contrast setting. In applications that require a lower black level voltage, a resistor (approximately 16 kΩ) can be added from pin 3 to ground. This has the effect of raising the DC voltage at the collector of Q4 which will extend the range of the black level clamp by allowing Q5 to remain active. In applications that require video amplifier shutdown due to fault conditions detected by monitor protection circuits, pin 3 and the wiper arms of the contrast and brightness controls can be grounded without harming the IC. This assumes some series resistance between the top of the control potentiometers and V_{CC}.

Figure 7 shows the internal construction of the pin 3 2.6V reference circuit which is used to provide temperature and supply voltage tracking compensation for the video amplifier input. The value of the external DC biasing resistors should not be larger than 10 kΩ when using more than one LM1201 (e.g. in RGB systems) because minor differences in input bias currents on the individual video amplifiers may cause offsets in gain.

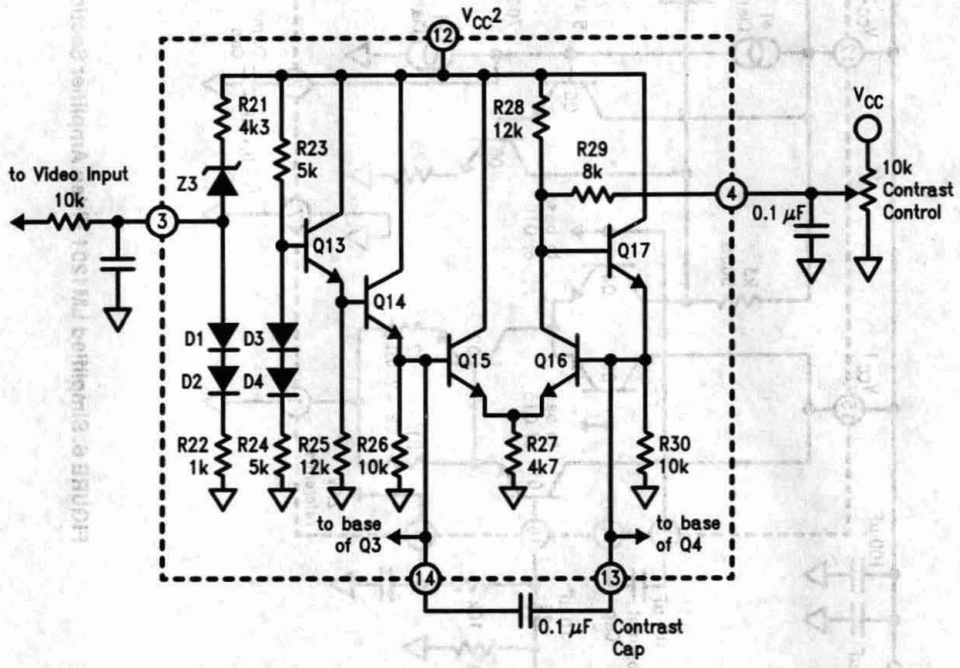

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FIGURE 7. LM1201 Video Input Voltage Reference and Contrast Control Circuits

Circuit Description (Continued)

Figure 7 also shows how the contrast control circuit is configured. Resistors R23, R24, diodes D3, D4, and transistor Q13 are used to establish a low impedance zero TC half supply voltage reference at the base of Q14. The differential amplifier formed by Q15, Q16 and feedback transistor Q17 along with resistors R27, R28 establish a differential base voltage for Q3 and Q4 in *Figure 6*. When externally adding or subtracting current from the collector of Q16, a new differential voltage is generated that reflects the change in the ratio of currents in Q15 and Q16. To provide voltage control of the Q16 current, resistor R29 is added between the Q16 collector and pin 4. A capacitor should be added from pin 4 to ground to prevent noise from the contrast control pot from entering the IC.

Figure 8 is a simplified schematic of the clamp gate and clamp comparator section of the LM1201. The clamp gate circuit consists of a PNP input buffer transistor (Q18), a PNP emitter coupled pair referenced on one side to 2.1V (Q19, Q20) and an output switch (Q21). When the clamp gate input at pin 5 is high (>1.5V), the Q21 switch is on and shunts the I1 1mA current to ground. When pin 5 is low (<1.3V), the Q21 switch is off and the I1 1mA current source is mirrored or "turned around" by reference diode D5 and Q26 to provide a 1mA current source for the clamp comparator. The inputs to the comparator are similar to the clamp gate input except that an NPN emitter coupled pair is used to control the current which will charge or discharge the clamp capacitor at pin 2. PNP transistors are used at the inputs because they offer a number of advantages over NPNs. PNPs will operate with base voltages at or near ground and will usually have a greater reverse emitter-base breakdown voltage (BVebo). Because the differential input voltage to the clamp comparator during the video scan period could be greater than the BVebo of NPN transistors, resistor R34 with a value one half that of R33 or R35 is connected between the bases of Q23 and Q27. This resistor will limit the maximum differential input to Q24, Q25 to approximately 350 mV. The clamp comparator common mode range extends from ground to approximately 9V and the maximum differential input voltage is V_{CC} and ground.

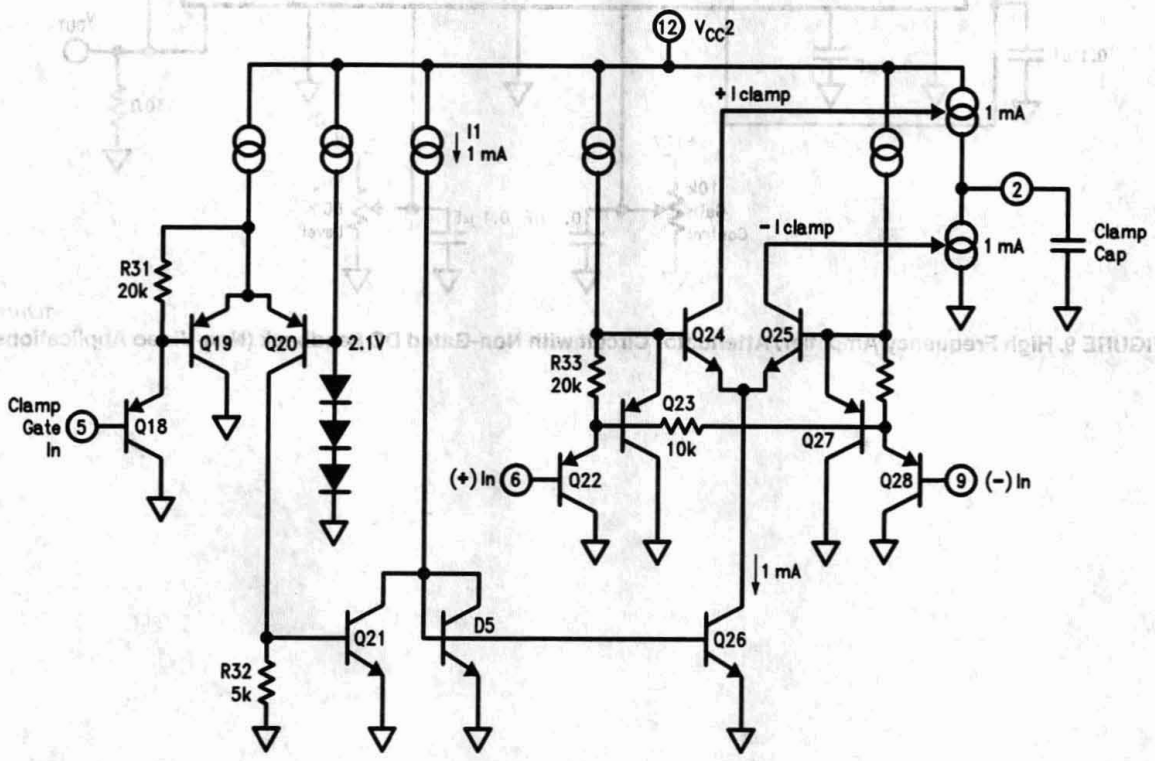

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FIGURE 8. Simplified Schematic of LM1201 Clamp Gate and Clamp Comparator Circuits

Applications Information

Figure 9 shows the configuration of a high frequency amplifier with non-gated DC feedback. Pin 5 is tied low to turn on the clamp comparator (feedback amplifier). The inverting input (pin 9) is connected to the amplifier output from a low pass filter. Additional low frequency filtering is provided by the clamp capacitor. The Drive pin is grounded to allow for the widest range of output signals. Maximum output swing is achieved when the DC output is set to approximately 4.5V.

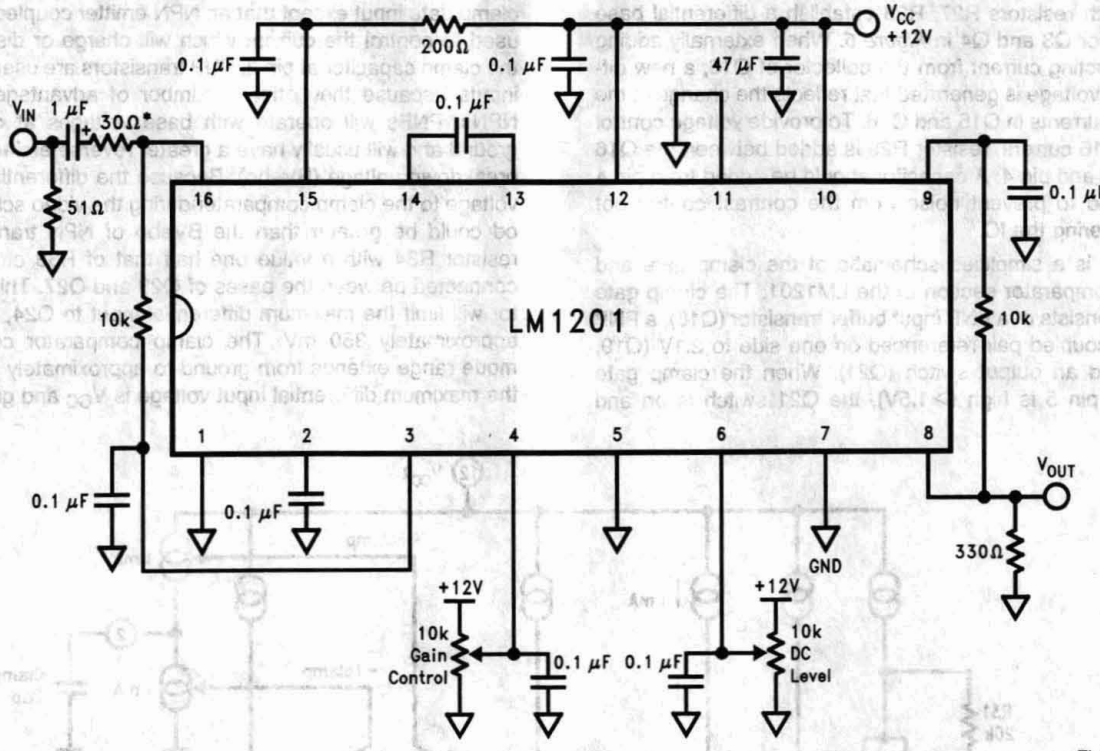

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FIGURE 9. High Frequency Amplifier/Attenuator Circuit with Non-Gated DC Feedback (Non-Video Applications)

Applications Information (Continued)

Figure 10 shows the LM1201 set up as a video amplifier with biphase outputs. Because the collector of output transistor Q12 is the only internal connection to V_{CC3}, a 75Ω termination to the power supply voltage allows one to obtain inverted video at pin 10. Black level on the non-inverted video output (pin 8) is set to 1.5V by the voltage divider on pin 6.

Figure 11 shows how a high frequency video switch may be designed using multiple LM1201 devices. All outputs can be OR'ed together assuming no more than one channel is selected at any given time. Channel selection is accomplished by keeping the appropriate SELECT SWITCH open. Closing the SELECT SWITCH on a given channel disables that channel's output (pin 8) leaving it in a high impedance state. A single pair of contrast and brightness potentiometers control the selected channel's gain and output DC level.

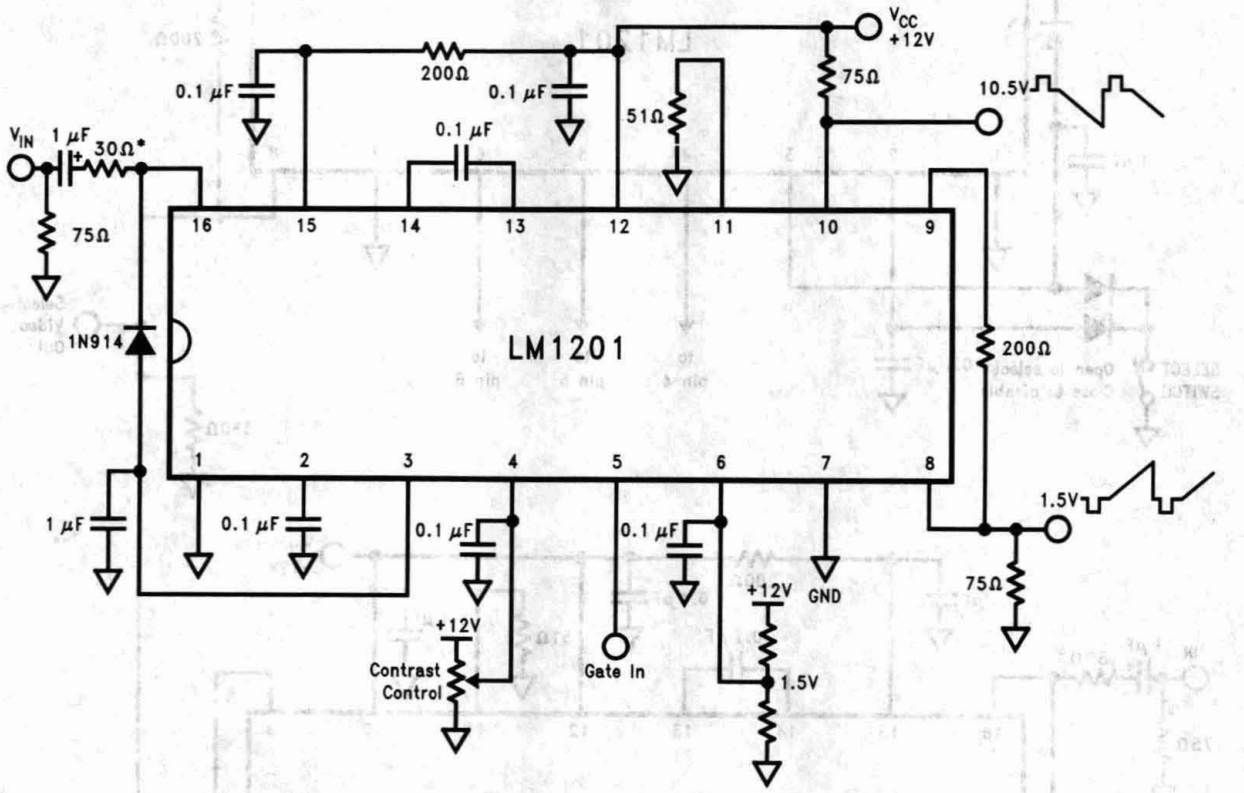

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FIGURE 10. Preclamped Video Amplifier with Biphase Outputs

Applications Information (Continued)

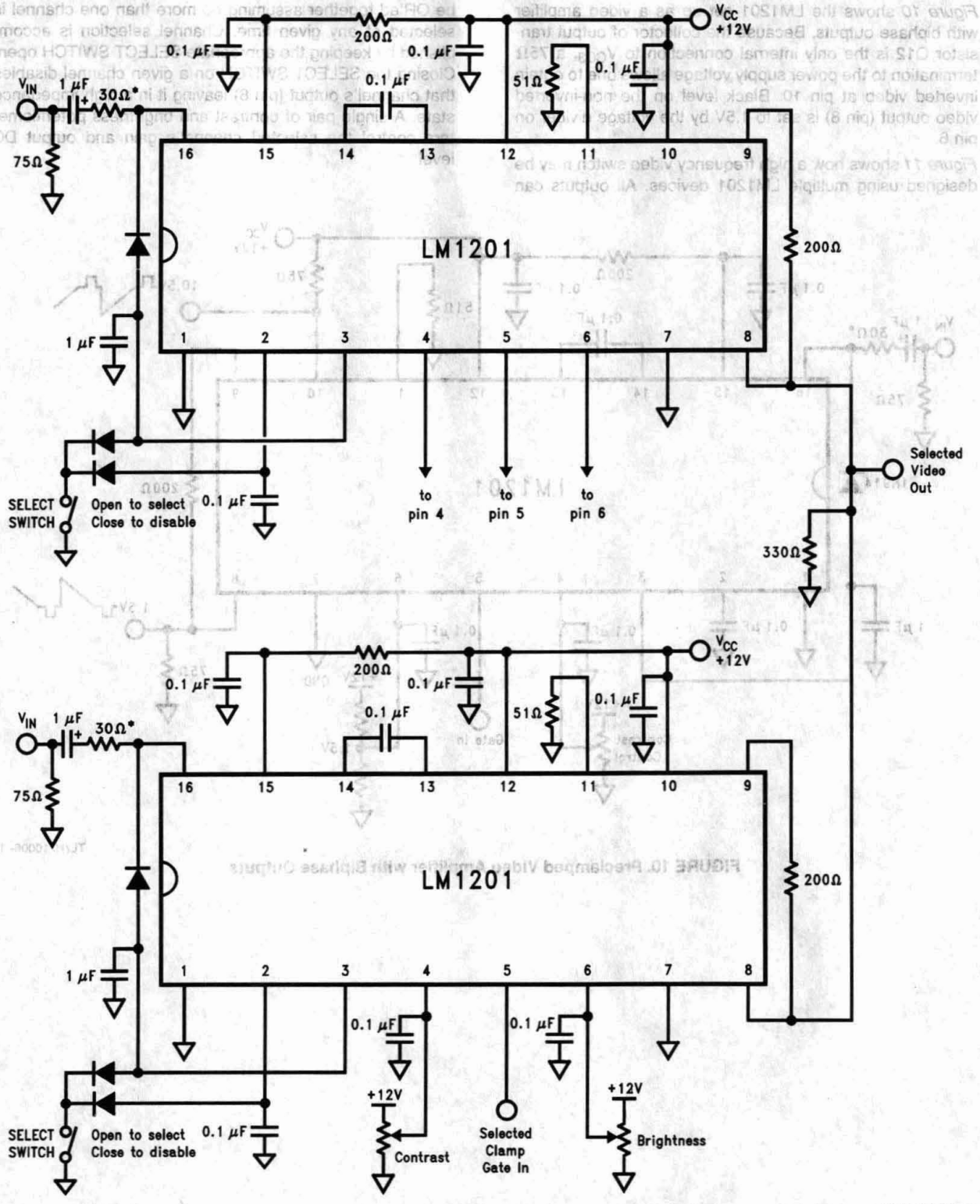

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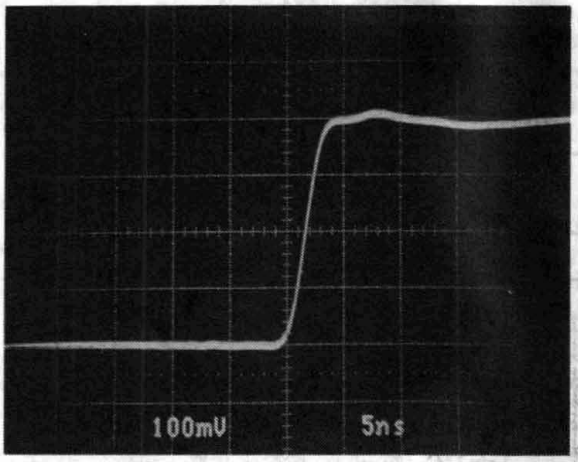
FIGURE 11. High Frequency Video Switch with Common Contrast and Brightness Controls

Rise Time No Socket



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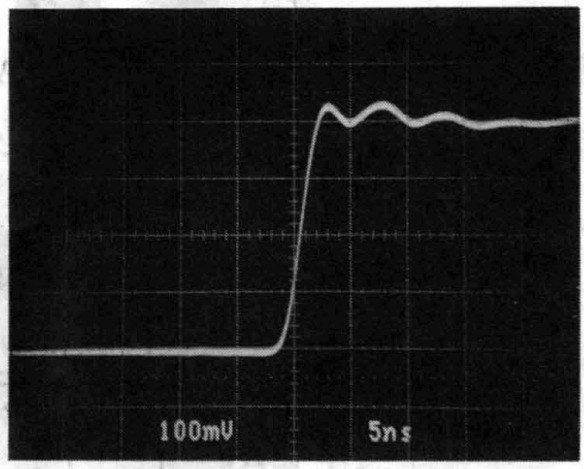
Rise Time In Socket



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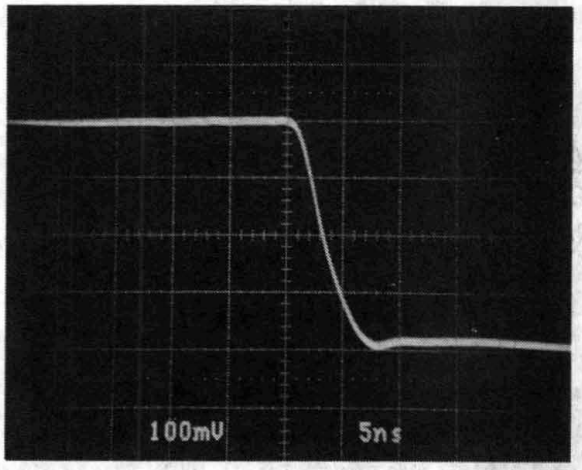
Fall Time No Socket



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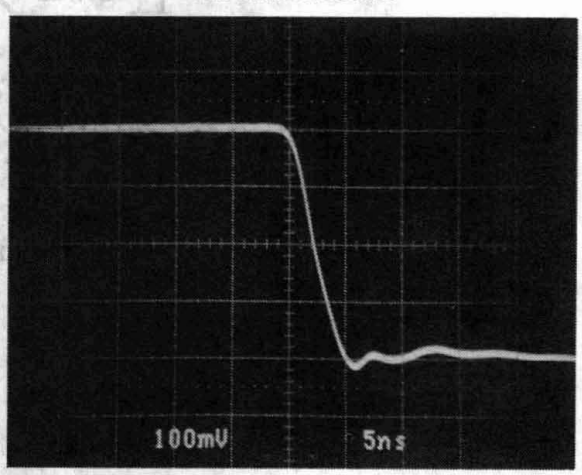
Fall Time In Socket



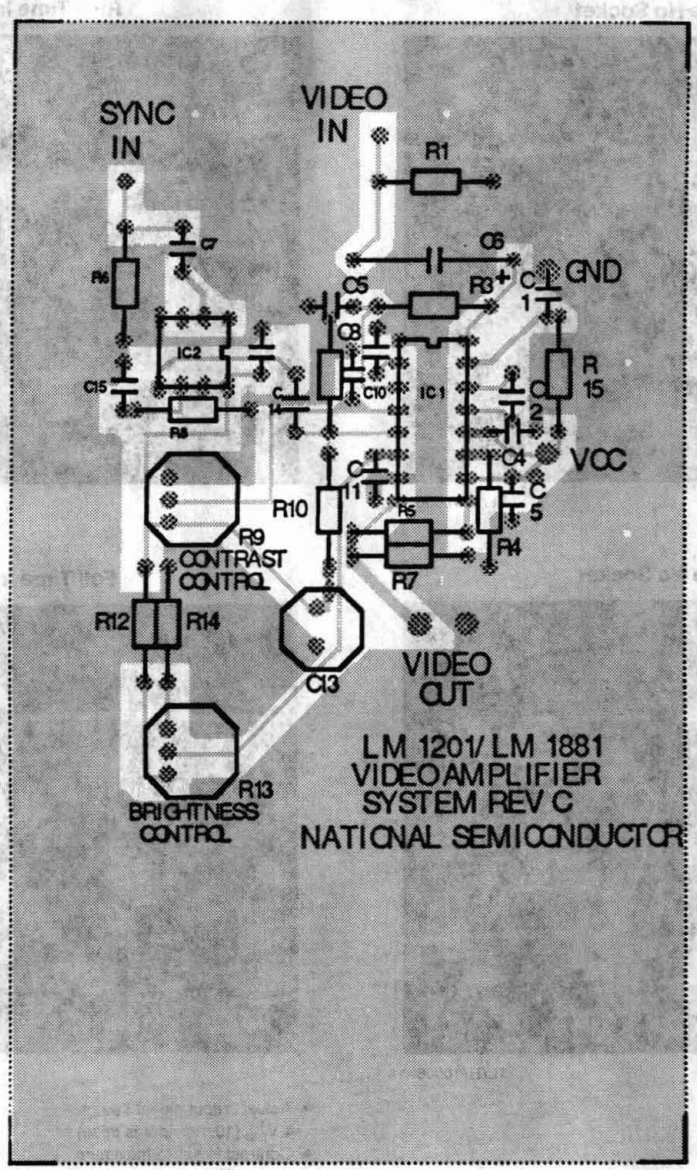
TL/H/10006–15

HP8082 pulse generator
HP10241A 10:1 voltage divider
HP1120A 500 MHz FET probe
Tektronix 2465A 350 MHz scope

Scale for All Photos—Vert: 1V/Div
Horiz: 5 ns/Div

- Actual output signal swings 4 V_{p-p} (10:1 divider is used)
- Contrast is set to maximum
- V_{IN} = 500 mV_{p-p}
- R_{DRIVE} = 50Ω
- Vertical scale is actually 1V/div and not 100 mV/div due to 10:1 attenuator used.
- Outputs are centered at 4V DC.

2



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Note: The p.c.b. layout shown above is suitable for evaluating the performance of the LM1201. Although it is similar to the typical application circuit of Figure 3, there is no c.r.t. driver stage. Instead, a feedback resistor is connected between Pins 8 and 9 and the brightness control is connected to Pin 6. Again, for best results, a socket should not be used for the LM1201.

COMPONENT VALUES:

R1	75Ω, 5%, 1/4 watt, carbon composition	C1	0.1 μF, ceramic
R3	10 kΩ, 5%, 1/4 watt, carbon composition	C2	0.1 μF, ceramic
R4	50Ω, 5%, 1/4 watt, carbon composition	C4	0.1 μF, ceramic
R5	200Ω, 5%, 1/4 watt, carbon composition	C5	0.1 μF, ceramic
R6	75Ω, 5%, 1/4 watt, carbon composition	C6	10 μF/6V, electrolytic
R7	330Ω, 5%, 1/4 watt, carbon composition	C7	0.1 μF, ceramic
R8	680 kΩ, 5%, 1/4 watt, carbon composition	C8	0.1 μF, ceramic
R9	10 kΩ, trim pot, helitrim model 91	C9	0.1 μF, ceramic
R10	5.1 kΩ, 5%, 1/4 watt, carbon composition	C10	0.1 μF, ceramic
R11	43 kΩ, 5%, 1/4 watt, carbon composition	C11	0.1 μF, ceramic
R12	12 kΩ, 5%, 1/4 watt, carbon composition	C12	0.1 μF, ceramic
R13	10 kΩ, trim pot, helitrim model 91	C13	100 μF/15V, electrolytic
R14	2 kΩ, 5%, 1/4 watt, carbon composition	C14	0.001 μF, mica
R15	200Ω, 5%, 1/4 watt, carbon composition	C15	0.1 μF, ceramic
IC1	LM1201		
IC2	LM1881		

National Semiconductor

LM1202 230 MHz Video Amplifier System

General Description

The LM1202 is a very high frequency video amplifier system intended for use in high resolution monochrome or RGB color monitor applications. In addition to the wideband video amplifier the LM1202 contains a gated differential input black level clamp comparator for brightness control, a DC controlled attenuator for contrast control and a DC controlled sub contrast attenuator for drive control. The DC control for the contrast attenuator is pinned out separately to provide a more accurate control system for RGB color monitor applications. All DC controls offer a high input impedance and operate over a 0V to 4V range for easy interface to bus controlled alignment systems. The LM1202 operates from a nominal 12V supply but can be operated with supply voltages down to 8V for applications that require reduced IC package power dissipation characteristics.

Features

- Wideband video amplifier (f_{-3dB} = 230 MHz at V_O = 4 V_{PP})
- t_r, t_f = 1.5 ns at V_O = 4 V_{PP}
- Externally gated comparator for brightness control
- 0V to 4V high input impedance DC contrast control (>40 dB range)
- 0V to 4V high input impedance DC drive control (±3 dB range)
- Easy to parallel three LM1202s for optimum color tracking in RGB systems
- Output stage clamps to 0.65V and provides up to 9V output voltage swing
- Output stage directly drives most hybrid or discrete CRT amplifier stages

Applications

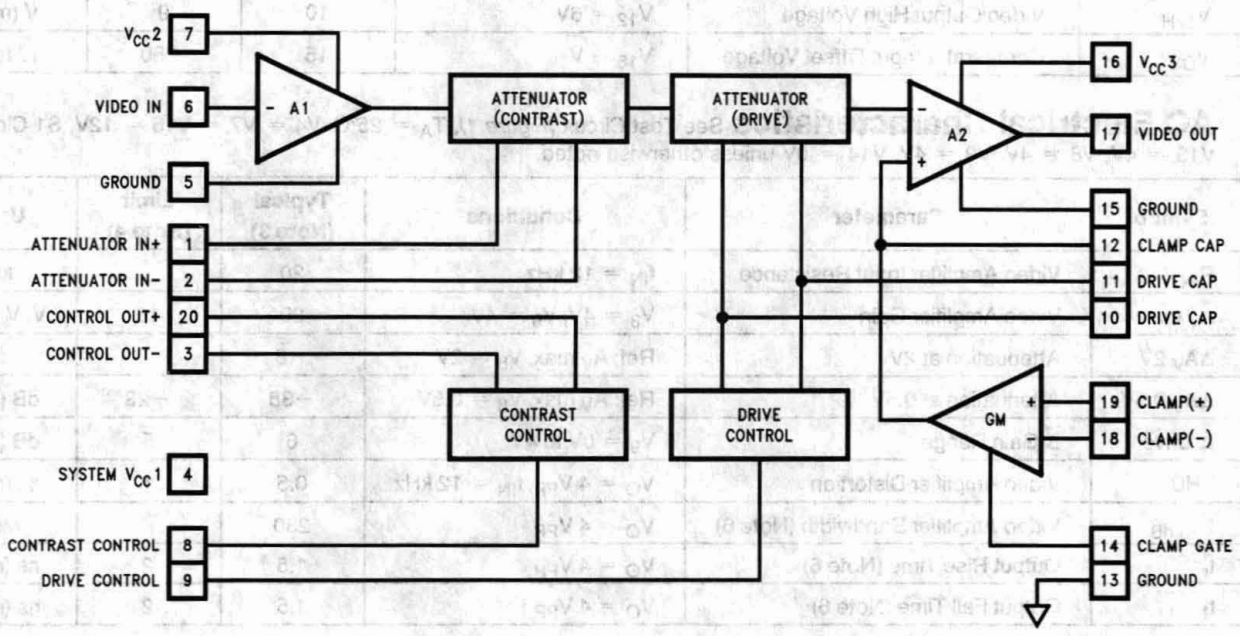
High resolution CRT monitors

Video switches

Video AGC amplifier

Wideband amplifier with gain and DC offset control

Block and Connection Diagram



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Order Number LM1202N or LM1202M
See NS Package Number N20A or M20B

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage V_{CC} Pins 4, 7, 16 to Ground Pins 5, 13, 15 — 13.5V

Voltage at Any Input Pin (V_{IN}) — $V_{CC} \geq V_{IN} \geq$ GND

Video Output Current (I_{17}) — 28 mA

Package Power Dissipation at $T_A = 25°C$ (Above 25°C Derate Based θ_{JA} and T_J) — 1.56W

Package Thermal Resistance (θ_{JA})
- N20A — 68°C/W
- M20B — 90°C/W

Junction Temperature (T_J) — 150°C

Storage Temperature Range (T_{stg}) — −65°C to +150°C

Lead Temperature
- N Package (Soldering, 10 sec.) — 265°C

ESD Susceptibility
- Human Body Model: 100 pF Discharged through a 1.5k Resistor — 1.5 kV

Operating Ratings (Note 2)

Temperature Range — −20°C to +80°C

Supply Voltage (V_{CC}) — $8V \leq V_{CC} \leq 13.2V$

DC Electrical Characteristics

See Test Circuit *(Figure 1)*, $T_A = 25°C$, V4 = V7 = V16 = 12V, S1 Open, V19 = 4V, V8 = 4V, V9 = 4V, V14 = 0V unless otherwise noted.

Symbol	Parameter	Conditions	Typical (Note 3)	Limit (Note 4)	Units
I_S 4, 7, 16	Total Supply Current	$R_{Load} = \infty$ (Note 5)	48	60	mA (max)
V_6	Video Input Bias Voltage		2.4	2	V (min)
V_{14L}	Clamp Gate Low Input Voltage	Clamp Comparator On		0.8	V (max)
V_{14H}	Clamp Gate High Input Voltage	Clamp Comparator Off		2	V (min)
I_{14L}	Clamp Gate Low Input Current	$V_{14} = 0V$	−0.5		μA
I_{14H}	Clamp Gate High Input Current	$V_{14} = 12V$	0.005		μA
I_{12+}	Clamp Cap Charge Current	$V_{12} = 0V$	800	500	μA (min)
I_{12-}	Clamp Cap Discharge Current	$V_{12} = 5V$	−800	−500	μA (min)
V_{17L}	Video Output Low Voltage	$V_{12} = 0V$	0.2	0.65	V (max)
V_{17H}	Video Output High Voltage	$V_{12} = 6V$	10	9	V (min)
V_{OS}	Comparator Input Offset Voltage	$V_{18} - V_{19}$	15	±50	mV (max)

AC Electrical Characteristics

See Test Circuit *(Figure 1)*, $T_A = 25°C$, V4 = V7 = V16 = 12V, S1 Closed, V19 = 4V, V8 = 4V, V9 = 4V, V14 = 0V unless otherwise noted.

Symbol	Parameter	Conditions	Typical (Note 3)	Limit (Note 4)	Units
R_{IN}	Video Amplifier Input Resistance	$f_{IN} = 12$ kHz	20		kΩ
A_V max	Video Amplifier Gain	$V_8 = 4V$, $V_9 = 4V$	20	16	V/V (min)
ΔA_V 2V	Attenuation at 2V	Ref: A_V max, $V_8 = 2V$	−6		dB
ΔA_V 0.5V	Attenuation at 0.5V	Ref: A_V max, $V_8 = 0.5V$	−38	−23	dB (min)
Δ Drive	Δ Gain Range	$V_9 = 0V$ to 4V	6	5	dB (min)
THD	Video Amplifier Distortion	$V_O = 4\ V_{PP}$, $f_{IN} = 12$ kHz	0.5	1	% (max)
$f_{-3\ dB}$	Video Amplifier Bandwidth (Note 6)	$V_O = 4\ V_{PP}$	230		MHz
t_r	Output Rise Time (Note 6)	$V_O = 4\ V_{PP}$	1.5	2	ns (max)
t_f	Output Fall Time (Note 6)	$V_O = 4\ V_{PP}$	1.5	2	ns (max)

Electrical Characteristics (Continued)

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur.

Note 2: Operating Ratings indicate conditions for which the device is functional but do not guarantee specific performance limits. For guaranteed specifications and test conditions see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.

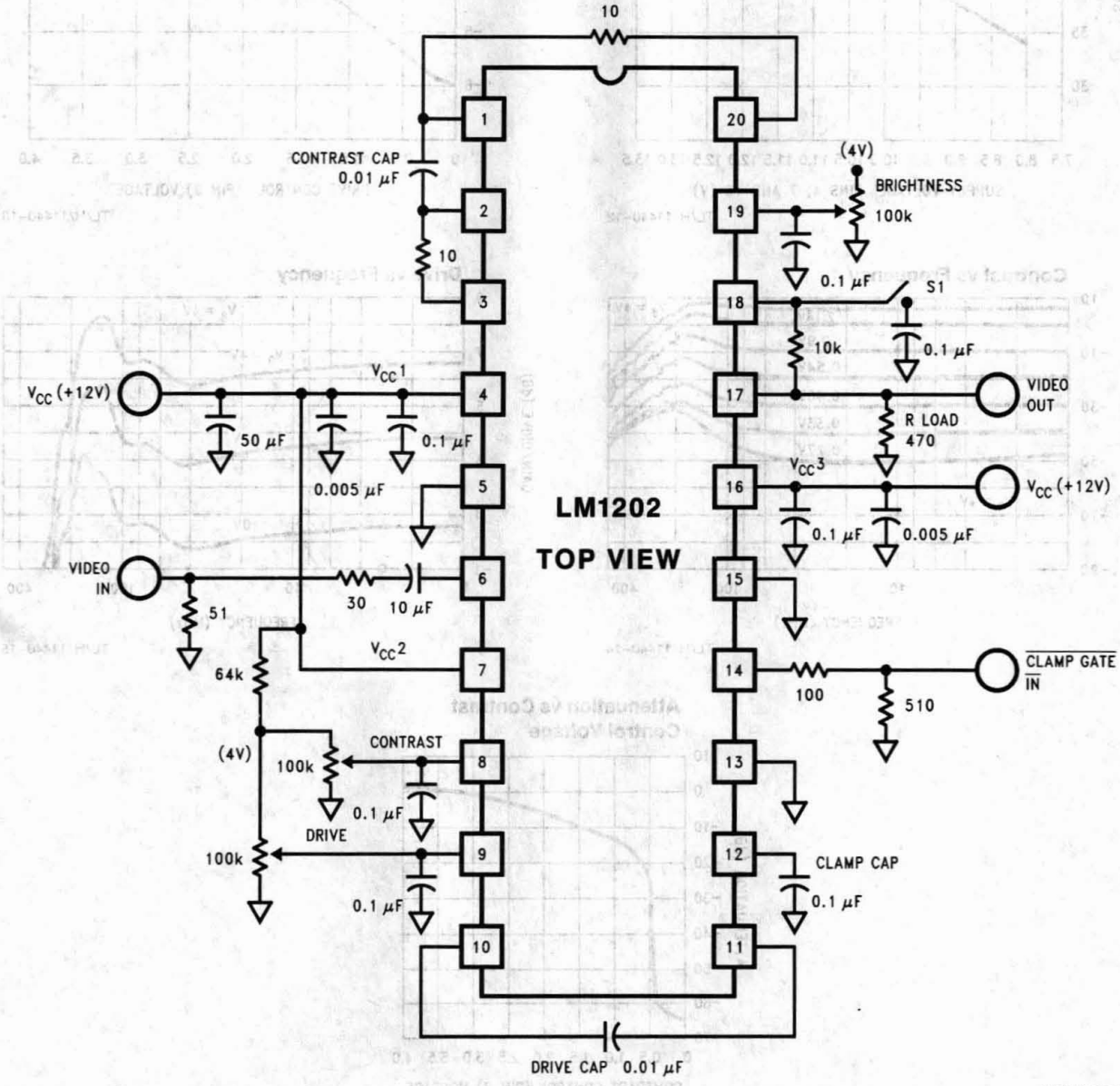
Note 3: Typical specifications are specified at +25°C and represent the most likely parametric norm.

Note 4: Tested limits are guaranteed to National's AOQL (Average Outgoing Quality Level).

Note 5: The supply current specified is the quiescent current for V_{CC1}, V_{CC2} and V_{CC3} with $R_{Load} = \infty$, see *Figure 1's* test circuit. The total supply current also depends on the output load, R_{Load}. The increase in device power dissipation due to R_{Load} must be taken into account when operating the device at the maximum ambient temperature.

Note 6: When measuring video amplifier bandwidth or pulse rise and fall times, a double sided full ground plane printed circuit board is recommended. The measured rise and fall times are effective rise and fall times, taking into account the rise and fall times of the generator and the oscilloscope.

Test Circuit

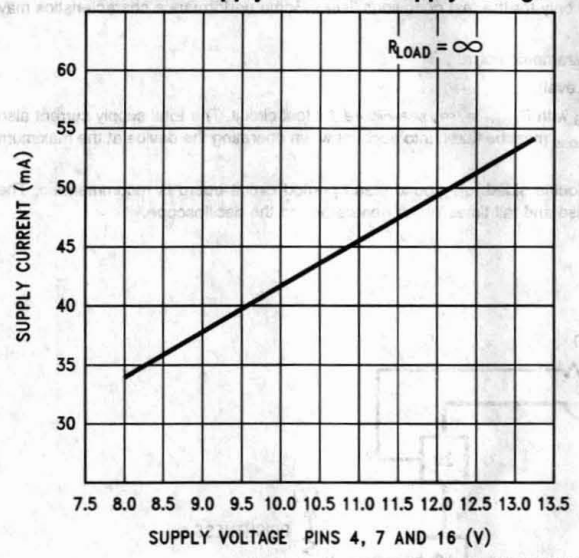


TL/H/11440–2

FIGURE 1. LM1202 Test Circuit

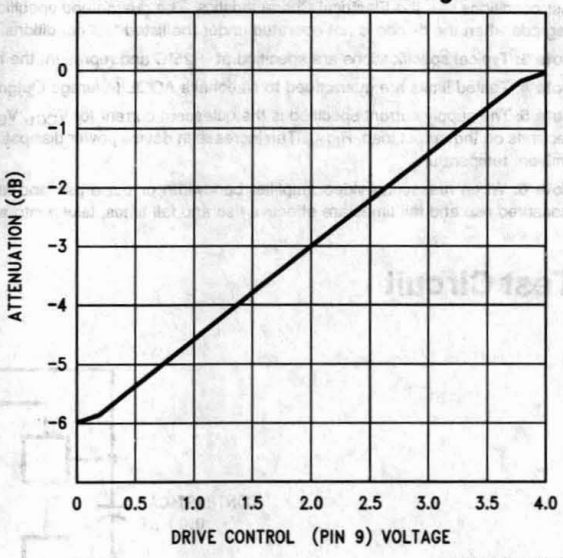
Typical Performance Characteristics (V_{CC} = 12V, T_A = 25°C unless otherwise specified)

Quiescent Supply Current vs Supply Voltage



TL/H/11440–12

Attenuation vs Drive Control Voltage



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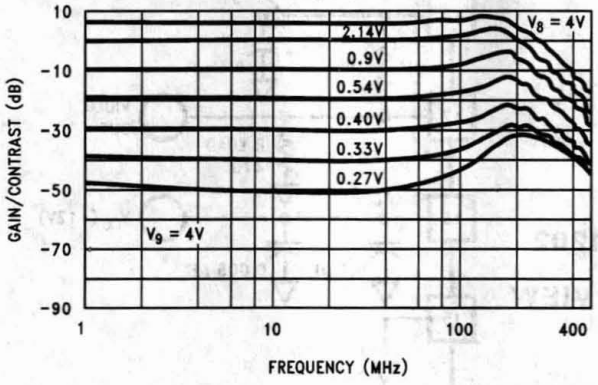
Contrast vs Frequency



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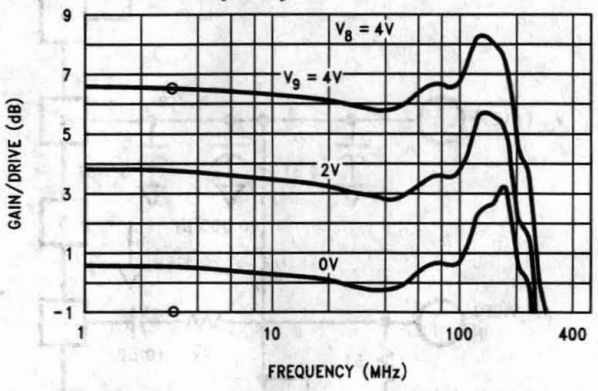
Drive vs Frequency



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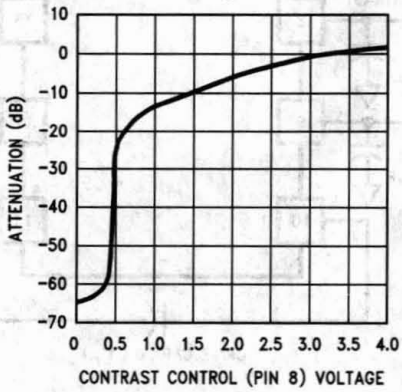
Attenuation vs Contrast Control Voltage



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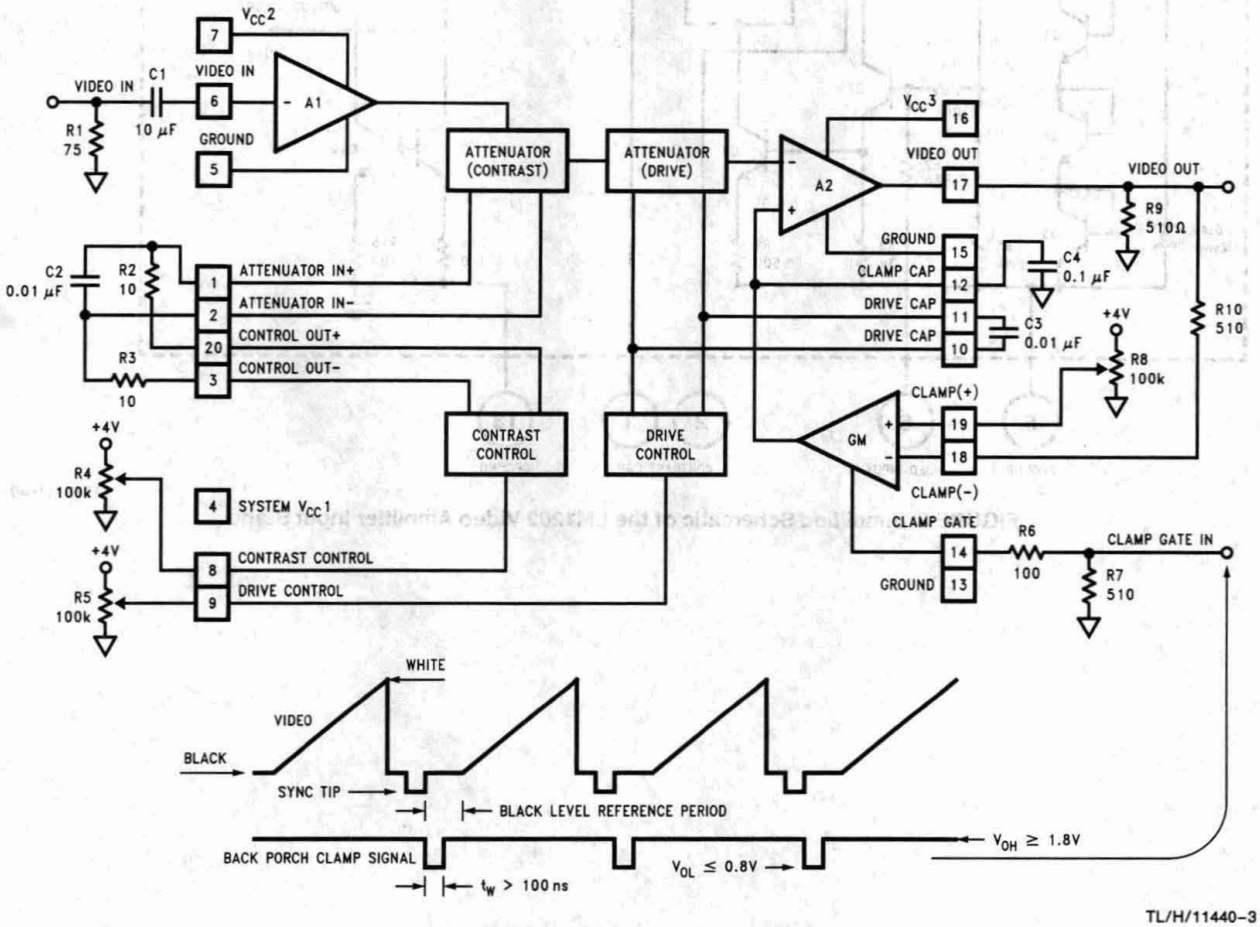
Circuit Description

Figure 2 shows a block diagram of the LM1202 video amplifier along with contrast and brightness (black level) control. Contrast control is a DC-operated attenuator which varies the AC gain of the amplifier. Signal attenuation (contrast) is achieved by varying the base drive to a differential pair and thereby unbalancing the current through the differential pair. As shown in *Figure 2*, pin 20 provides a 5.3V bias voltage for the positive input of the attenuator (pin 1). Pin 3 provides a control voltage for the negative input (pin 2) of the attenuator. The voltage at pin 3 varies as the voltage at the contrast control input (pin 8) varies thus providing signal attenuation. The gain is maximum (0 dB attenuation) if the voltage at pin 8 is 4V and is minimum (maximum attenuation) if the voltage at pin 8 is 0V. The 0V to 4V DC-operated drive control at pin 9 provides a 6 dB gain adjustment range. This feature is necessary for RGB applications where independent gain adjustment of each channel is required.

The brightness or black level clamping requires a "sample and hold" circuit which holds the DC bias of the video amplifier constant during the black level reference portion of the video waveform. Black level clamping, often referred to as DC restoration, is accomplished by applying a back porch clamp signal to the clamp gate input pin (pin 14). The clamp comparator is enabled when the clamp signal goes low during the black level reference period (see *Figure 2*). When the clamp comparator is enabled, the clamp capacitor connected to pin 12 is either charged or discharged until the voltage at the minus input of the comparator matches the voltage set at the plus input of the comparator. During the video portion of the signal, the clamp comparator is disabled and the clamp capacitor holds the proper DC bias. In a DC coupled cathode drive application, picture brightness function can be achieved by varying the voltage at the comparator's plus input. Note that the back porch clamp pulse width (t_W in *Figure 2*) must be greater than 100 ns for proper operation.

VIDEO AMPLIFIER SECTION (Input Stage)

A simplified schematic of LM1202's video amplifier input stage is shown in *Figure 3*. The 5.4V zener diode, Q1, Q6 and R2 bias the base of Q7 at 2.6V. The AC coupled video signal applied to pin 6 is referenced to the 2.6V bias voltage. Transistor Q7 buffers the video signal, V_{IN}, and Q8 converts the voltage to current. The AC collector current through Q8 is $I_{C8} = V_{IN}/R9$. Under maximum gain condition, transistors Q9 and Q11 are off and all of I_{C8} flows through the load resistors R10 and R11. The maximum signal gain at the base of Q13 is, $A_{V1} = -(R10 + R11)/R9 = -2$. Signal attenuation is achieved by varying the base drive to the differential pairs Q9, Q10 and Q11, Q12 thereby unbalancing the collector currents through the transistor pairs. Base of Q10 is biased at 5.3V by externally connecting pin 1 to pin 20 through a 100Ω resistor. Pin 2 is connected to pin 3 through a 100Ω resistor. Adjusting the contrast voltage at



TL/H/11440–3

FIGURE 2. Block Diagram of the LM1202 Video Amplifier with Contrast and Brightness (Black Level) Control

Circuit Description (Continued)

pin 8 produces a control voltage at pin 3 which drives the base of Q9. By varying the voltage at the base of Q9, Q8's collector current (I_{C8}) is diverted away from the load resistors R10 and R11, thereby providing signal attenuation. Maximum attenuation is achieved when all of I_{C8} flows through Q9 and no current flows through the load resistors.

The differential pair Q11 and Q12 provide drive control. Q12's base is internally biased at 7.3V. Adjusting the voltage at the drive control input (pin 9) produces a control voltage at the base of Q11. With Q9 off and Q12 off, all of I_{C8} flows through R10, thus providing a gain of $A_{V1} = -(R10/R9) \times V_{IN} = -1$. Drive control thus provides a 6 dB attenuation range.

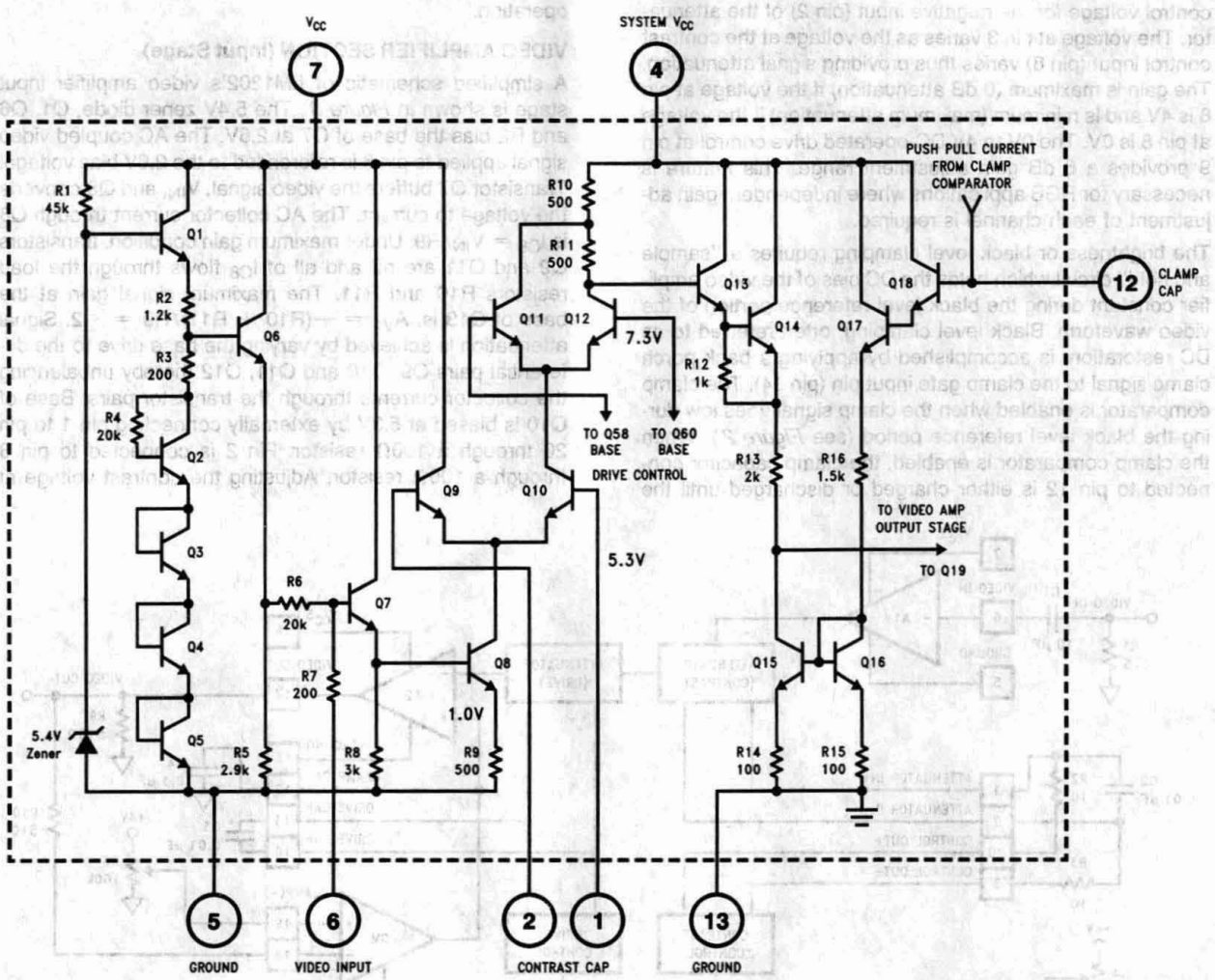


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FIGURE 3. Simplified Schematic of the LM1202 Video Amplifier Input Stage

Circuit Description (Continued)

VIDEO AMPLIFIER SECTION (Output Stage)

A simplified schematic of LM1202's video amplifier output stage is shown in *Figure 4*. The output stage is the second gain stage. Ideally the gain of the second gain stage would be $A_{V2} = -R21/R18 = -16$. Because of the output stage's low open loop gain, the gain is approximately $A_{V2} = -10$. Thus the maximum gain of the video amplifier is $A_V = A_{V1} \times A_{V2} = 20$. Transistors Q23 and Q24 provide a push-pull drive to the load. The output voltage can swing from 0.2V to 10V.

CONTRAST CONTROL SECTION

A simplified schematic of LM1202's contrast control section is shown in *Figure 5*. A 0V to 4V DC voltage is applied at the contrast input (pin 8). Transistors Q29, Q30 and Q34 buffer and level shift the contrast voltage to the base of Q36. The voltage at the emitter of Q36 equals the contrast voltage (V_{cont}) and the current through Q36's collector is given by $I_{C36} = V_{cont}/R28$.

Transistor Q36's collector current is used to unbalance the current through the differential pair comprised of Q38 and Q40. Q40's base is internally biased at 5.3V and made available at pin 20. Pin 20 is externally connected to pin 1 through a 100Ω resistor (see *Figures 2* and *3*). The base of Q38 (pin 3) is externally connected to pin 2 through a 100Ω resistor (see *Figures 2* and *3*). With $V_{cont} = 2V$, the differential pair (Q38, Q40) is balanced and the voltage at pins 1 and 2 is 5.3V. Under this condition, Q8's collector current is equally split between Q9 and Q10 (see *Figure 3*) and the amplifier's gain is half the maximum gain. If contrast voltage at pin 8 is greater than 2V then Q36's collector current increases, thus pulling Q38's collector node lower and consequently moving Q38's base below 5.3V. With pin 2 at a lower voltage than pin 1, current through Q10 (see *Figure 3*) increases and the amplifier's gain increases. With $V_{cont} = 4V$, the amplifier's gain is maximum.

If the contrast voltage at pin 8 is less than 2V then Q36's collector current decreases and Q38's base is pulled above 5.3V. With pin 2 voltage greater than pin 1 voltage, less current flows through Q10 (see *Figure 3*), consequently the amplifier's gain decreases. With $V_{cont} = 0V$, the amplifier's gain is minimum (i.e., maximum attenuation).

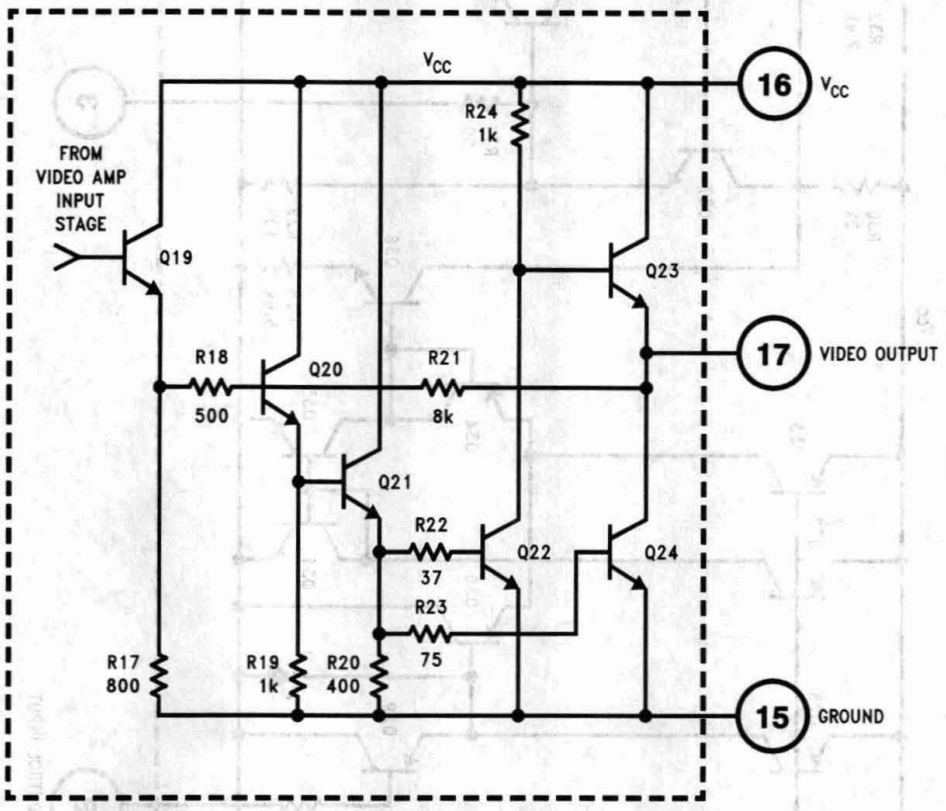

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FIGURE 4. Simplified Schematic of LM1202 Video Amplifier Output Stage

Circuit Description (Continued)

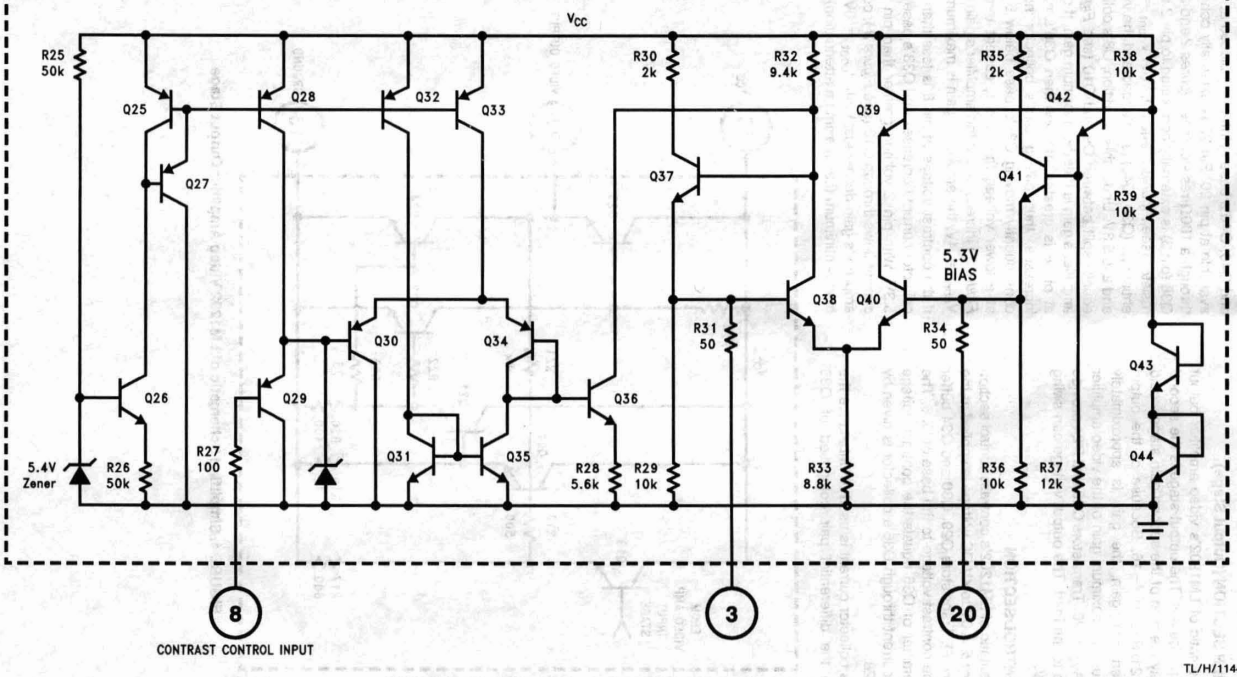

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FIGURE 5. Simplified Schematic of LM1202 Contrast Control

Circuit Description (Continued)

DRIVE CONTROL SECTION

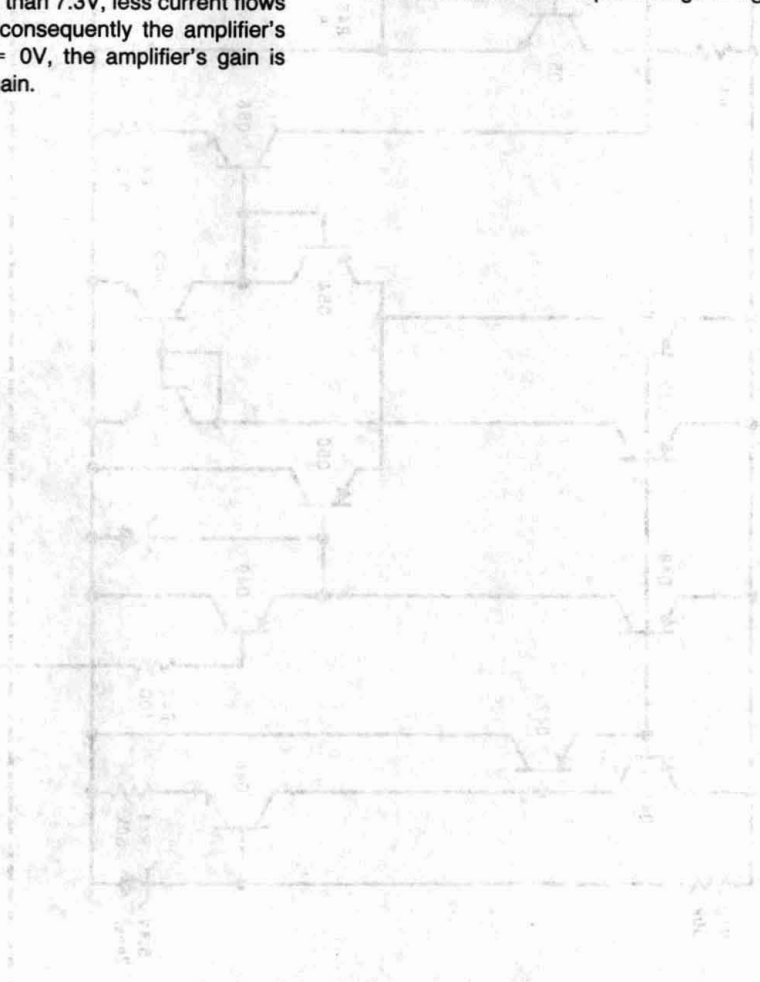
A simplified schematic of the LM1202's drive control section is shown in *Figure 6*. A 0V to 4V DC voltage is applied at the drive control input (pin 9). Transistors Q49, Q50 and Q54 buffer and level shift the contrast voltage to the base of Q56. The voltage at the emitter of Q56 equals the drive voltage, V_{drive} and the current through Q56's collector is given by $I_{C56} = V_{drive}/R43$.

Transistor Q56's collector current is used to unbalance the current through the differential pair comprised of Q58 and Q60. Q60's base is internally biased at 7.3V and connected to the base of Q12 (see *Figure 3*). Q58's base is internally connected to the base of Q11 (see *Figure 3*). With V_{cont} = 2V, the differential pair (Q58, Q60) is balanced and the voltage at the bases of Q11 and Q12 is 7.3V. Under this condition, Q10's collector current is equally split between Q11 and Q12 (see *Figure 3*). If the drive voltage at pin 9 is greater than 2V then Q56's collector current increases, thus pulling Q58's collector node lower and consequently moving Q58's base below 7.3V. With base of Q11 below 7.3V, current through Q12 (see *Figure 3*) increases and the amplifier's gain increases. With V_{drive} = 4V, the amplifier's gain is maximum under maximum contrast condition (i.e., V_{cont} = 4V).

If the drive voltage at pin 8 is less than 2V then Q56's collector current decreases and Q58's base is pulled above 7.3V. With base of Q11 greater than 7.3V, less current flows through Q12 (see *Figure 3*), consequently the amplifier's gain decreases. With V_{drive} = 0V, the amplifier's gain is 6 dB less than the maximum gain.

CLAMP GATE AND CLAMP COMPARATOR SECTION

Figures 7 and *8* show simplified schematics of the clamp gate and clamp comparator circuits. The clamp gate circuit *(Figure 7)* consists of a PNP input buffer transistor (Q82), a PNP emitter coupled pair (Q85 and Q86) referenced on one side to 2.1V and an output switch transistor Q89. When the clamp gate input at pin 14 is high (> 1.5V) the Q89 switch is on and shunts the 200 μA current from current source Q90 to ground. When pin 14 is low (< 1.3V) the Q89 switch is off and the 200 μA current is mirrored by the current mirror comprised of Q91 and Q75 (see *Figure 8*). Consequently the clamp comparator comprised of the differential pair Q74 and Q77 is enabled. The input of the clamp comparator is similar to the clamp gate except that an NPN emitter coupled pair is used to control the current that will charge or discharge the clamp capacitor externally connected from pin 12 to ground. PNP transistors are used at the inputs because they offer a number of advantages over NPNs. PNPs will operate with base voltages at or near ground and will usually have a greater emitter base breakdown voltage (BVebo). Because the differential input voltage to the clamp comparator during the video scan period could be greater than the BVebo of NPN transistors, a resistor (R63) with a value one half that of R60 or R68 is connected between the bases of Q71 and Q79. The clamp comparator's common mode range is from ground to approximately 9V and the maximum differential input voltage is V_{CC}.



Circuit Description (Continued)

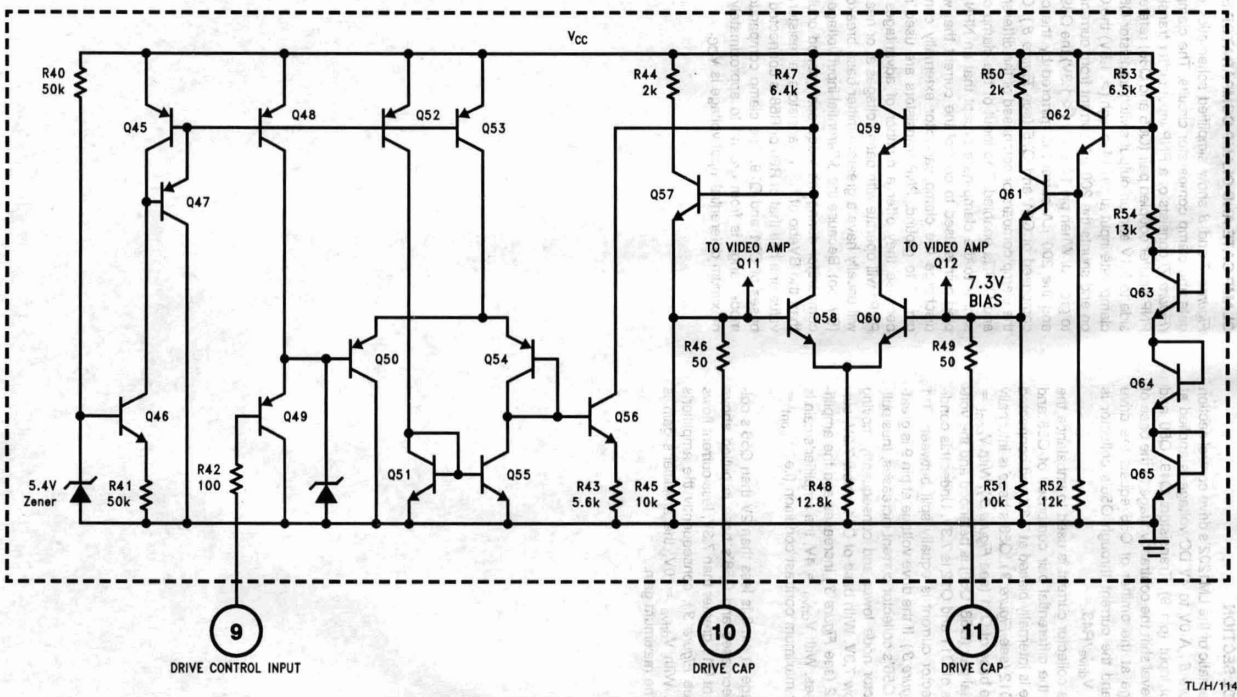


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FIGURE 6. Simplified Schematic of the LM1202 Drive Control

Circuit Description (Continued)

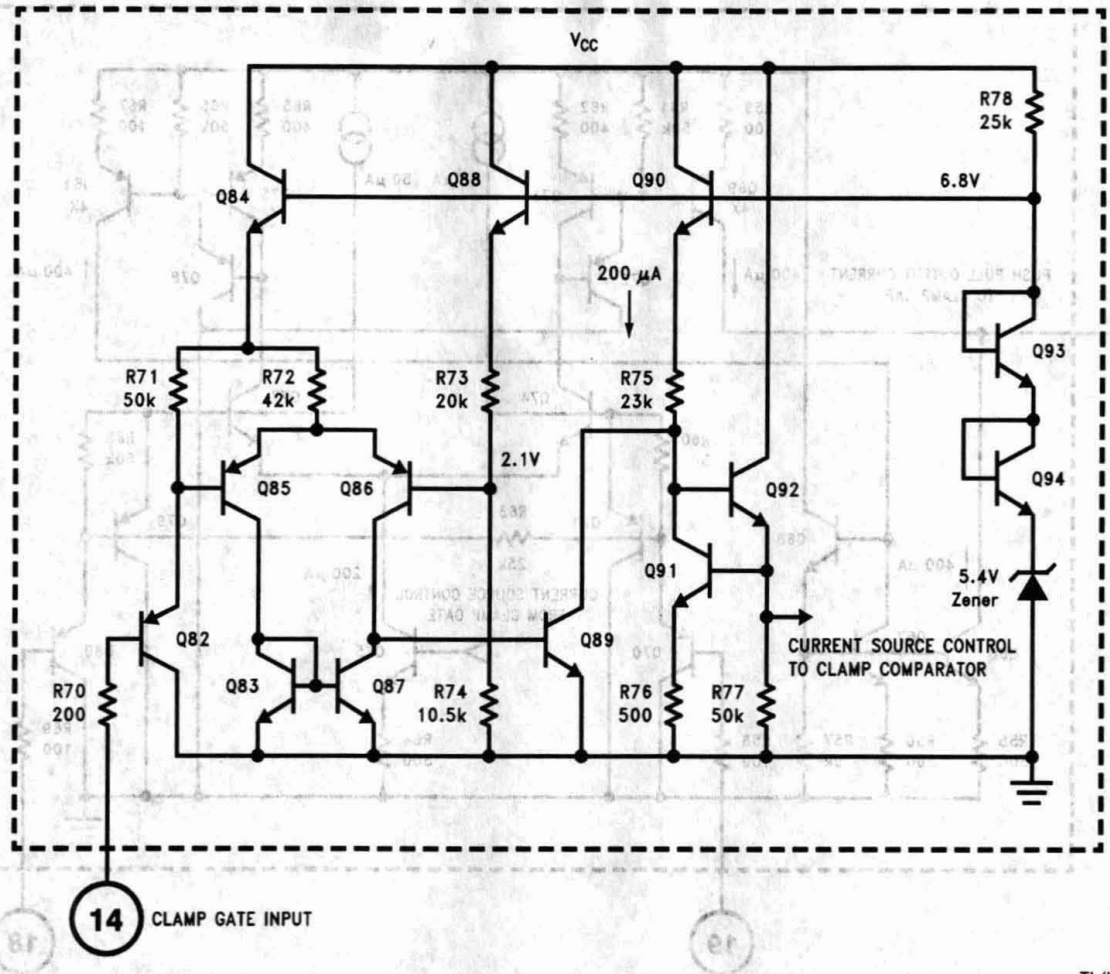

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FIGURE 7. Simplified Schematic of the LM1202 Clamp Gate Circuit

Circuit Description (Continued)

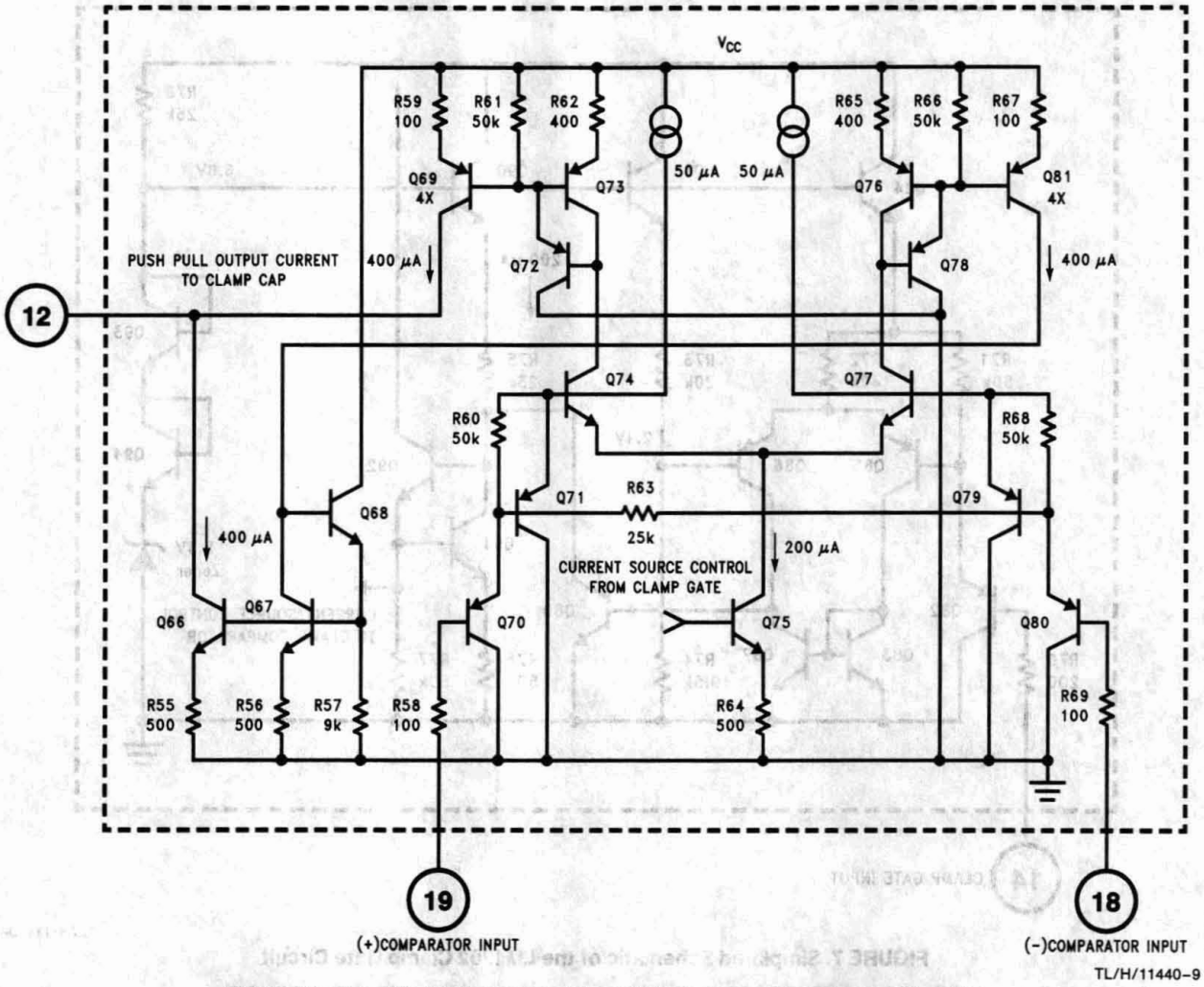

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FIGURE 8. Simplified Schematic of the LM1202 Clamp Comparator Circuit

Applications of the LM1202

SINGLE VIDEO CHANNEL

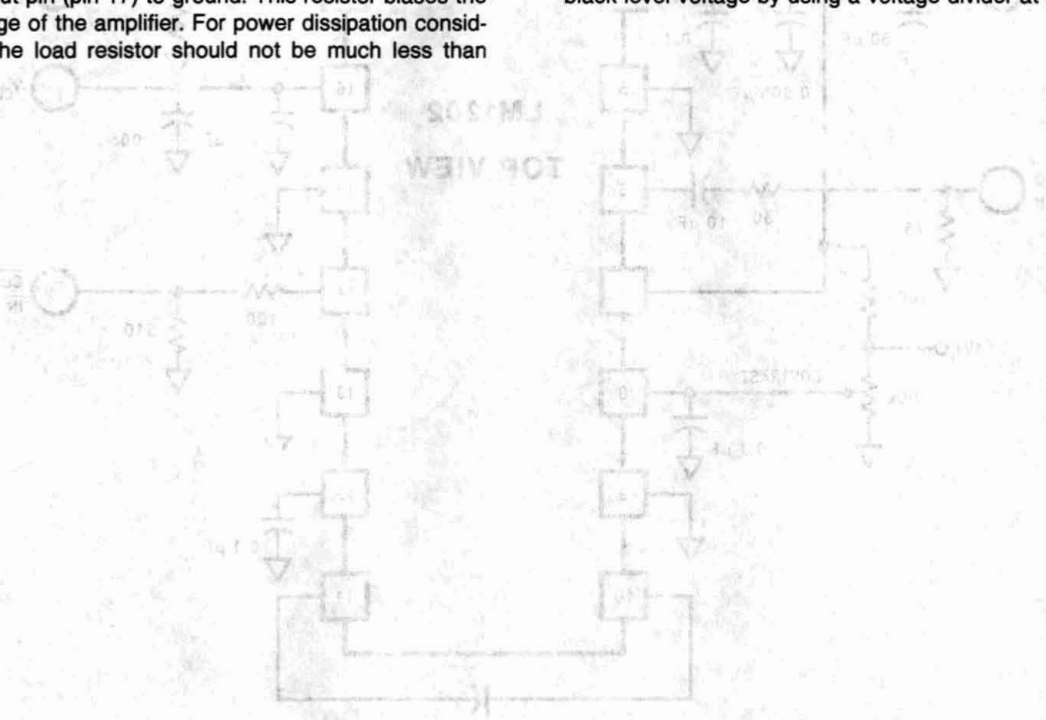
A typical application for a single video channel is shown in *Figure 9*. The video signal is AC coupled to pin 6. The LM1202 internally biases the video signal to 2.6 V_{DC}. Contrast control is achieved by applying a 0V to 4V DC voltage at pin 8. The amplifier's gain is minimum (i.e., maximum signal attenuation) if pin 8 is at 0V and is maximum if pin 8 is at 4V. With pin 9 (drive control) at 0V, the amplifier has a maximum gain of 10.

For DC restoration, a clamp signal must be applied to the clamp gate input (pin 14). The clamp signal should be logic low (less than 0.8V) only during the back porch (black level reference period) interval (see *Figure 2*). The clamp gate input is TTL compatible. Brightness control is provided by applying a 0V to 4V DC voltage at pin 19. For example, if pin 19 is biased at 1V then the video signal's black level will be clamped at 1V. A 510Ω load resistor is connected from the video output pin (pin 17) to ground. This resistor biases the output stage of the amplifier. For power dissipation considerations, the load resistor should not be much less than 510Ω.

RGB VIDEO PREAMPLIFIER

Figure 10 shows an RGB video preamplifier circuit using three LM1202s. Note that pins 1 and 2 of IC1 are connected to pins 1 and 2 of IC2 and IC3 respectively. This allows IC1 to provide a master contrast control and optimum contrast tracking. Adjusting the contrast voltage at pin 8 of IC1 will vary the gain of all three video channels. Drive control input (pin 9) of each LM1202 allows individual gain adjustment for achieving white balance.

The black level of each video channel can be individually adjusted to the desired voltage by adjusting the voltage at pin 19. In a DC-coupled cathode drive application, adjusting the voltage at pin 19 of each IC will provide cutoff adjustment. In an AC-coupled cathode drive application, the video signal is AC coupled and DC restored at the cathode. In such an application, the video signal's black level may be clamped to the desired level by simply biasing pin 19 to the black level voltage by using a voltage divider at pin 19.



Applications of the LM1202 (Continued)

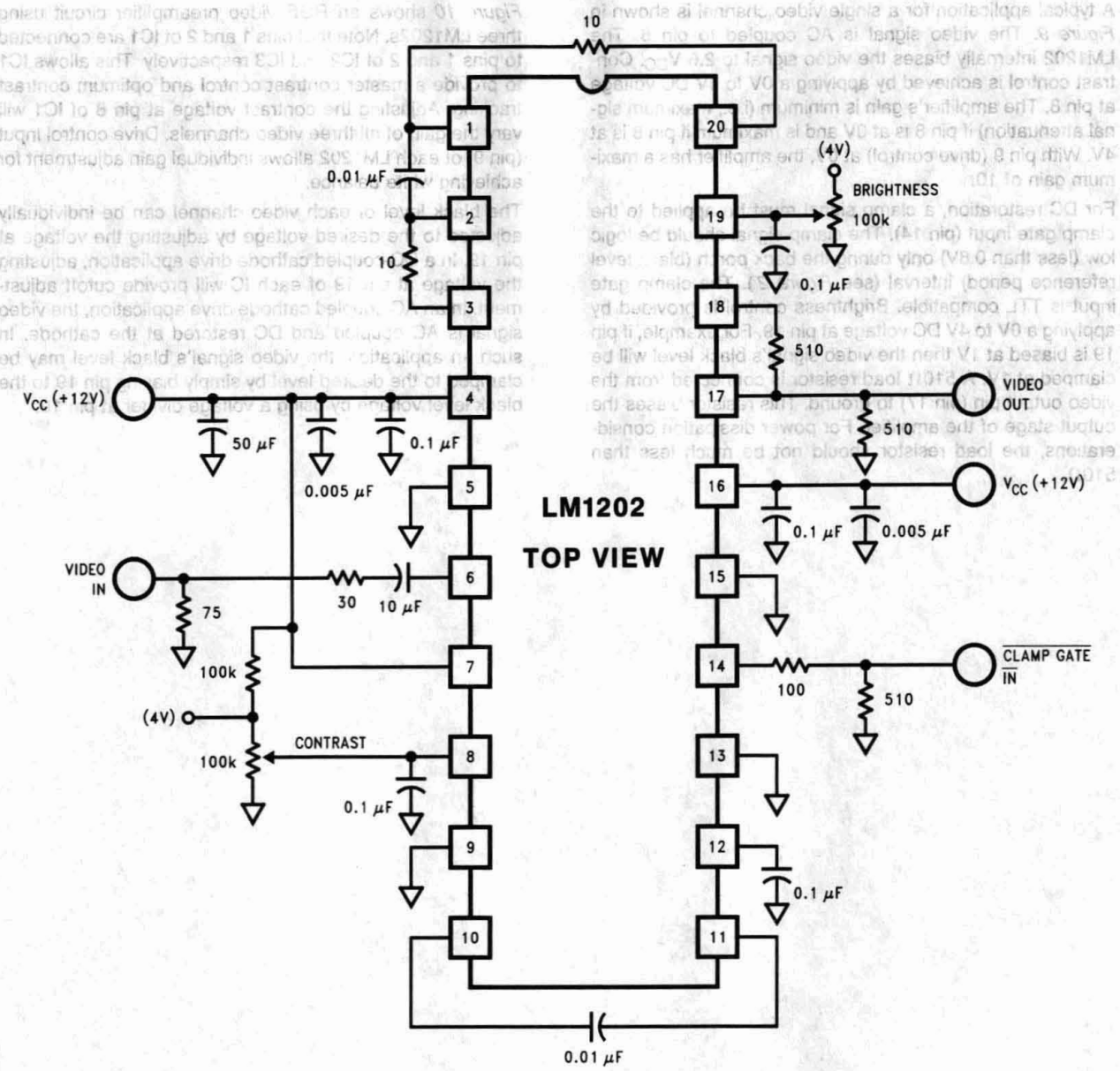


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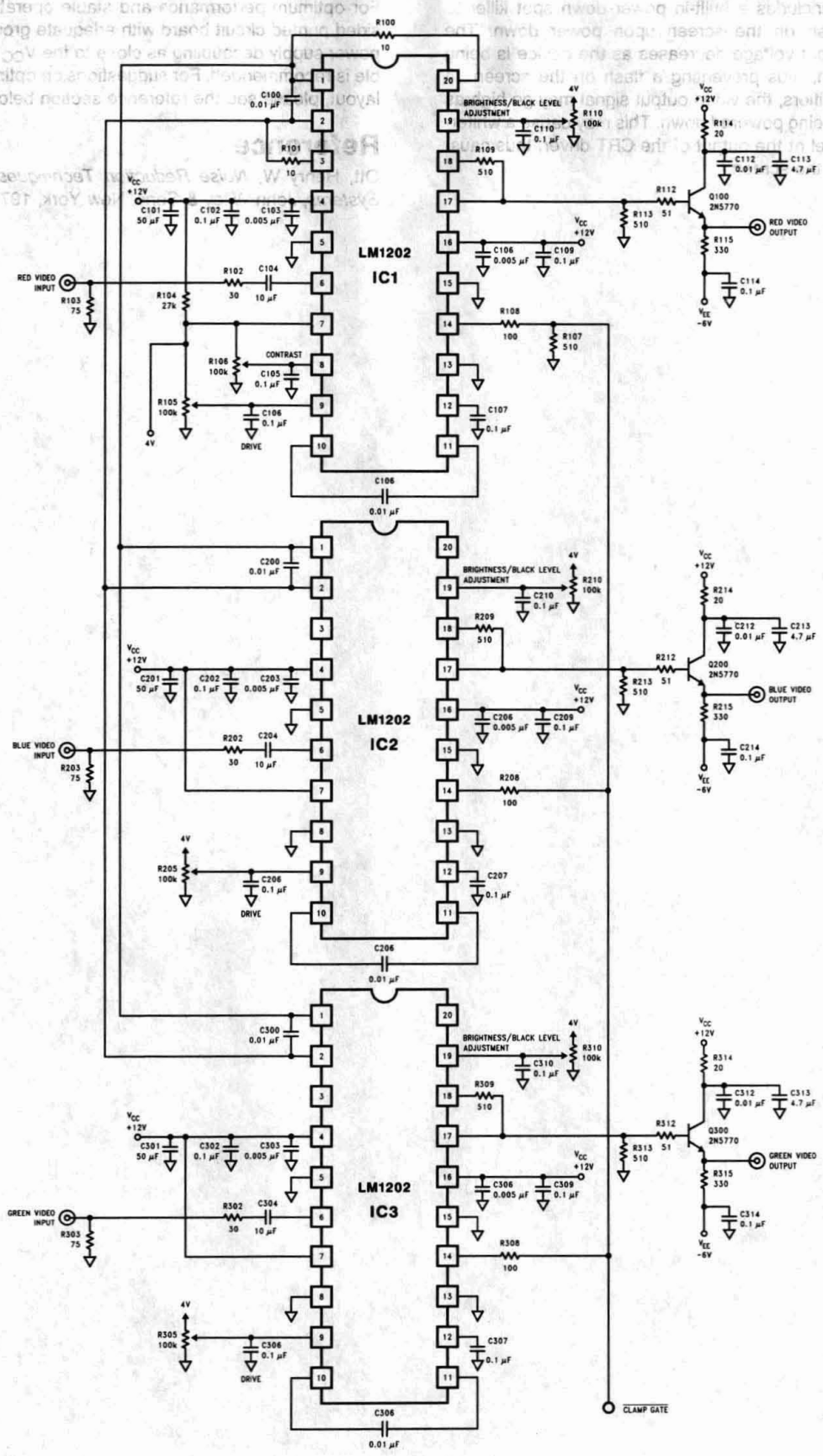
FIGURE 9. Typical LM1202 Application (Single Video Channel)

Applications of the LM1202 (Continued)



TL/H/11440–11

FIGURE 10. Typical RGB Application with Contrast, Drive and Black Level (Cutoff) Control

Power Down Characteristics

The LM1202 includes a built-in power down spot killer to prevent a flash on the screen upon power down. The LM1202's output voltage decreases as the device is being powered down, thus preventing a flash on the screen. In some preamplifiers, the video output signal may go high as the device is being powered down. This may cause a whiter-than-white level at the output of the CRT driver, thus causing a flash on the screen.

PC Board Layout Considerations

For optimum performance and stable operation, a double-sided printed circuit board with adequate ground plane and power supply decoupling as close to the V_{CC} pins as possible is recommended. For suggestions on optimum PC board layout, please see the reference section below.

Reference

Ott, Henry W, *Noise Reduction Techniques in Electronic Systems*, John Wiley & Sons, New York, 1976.

National Semiconductor

LM1203 RGB Video Amplifier System

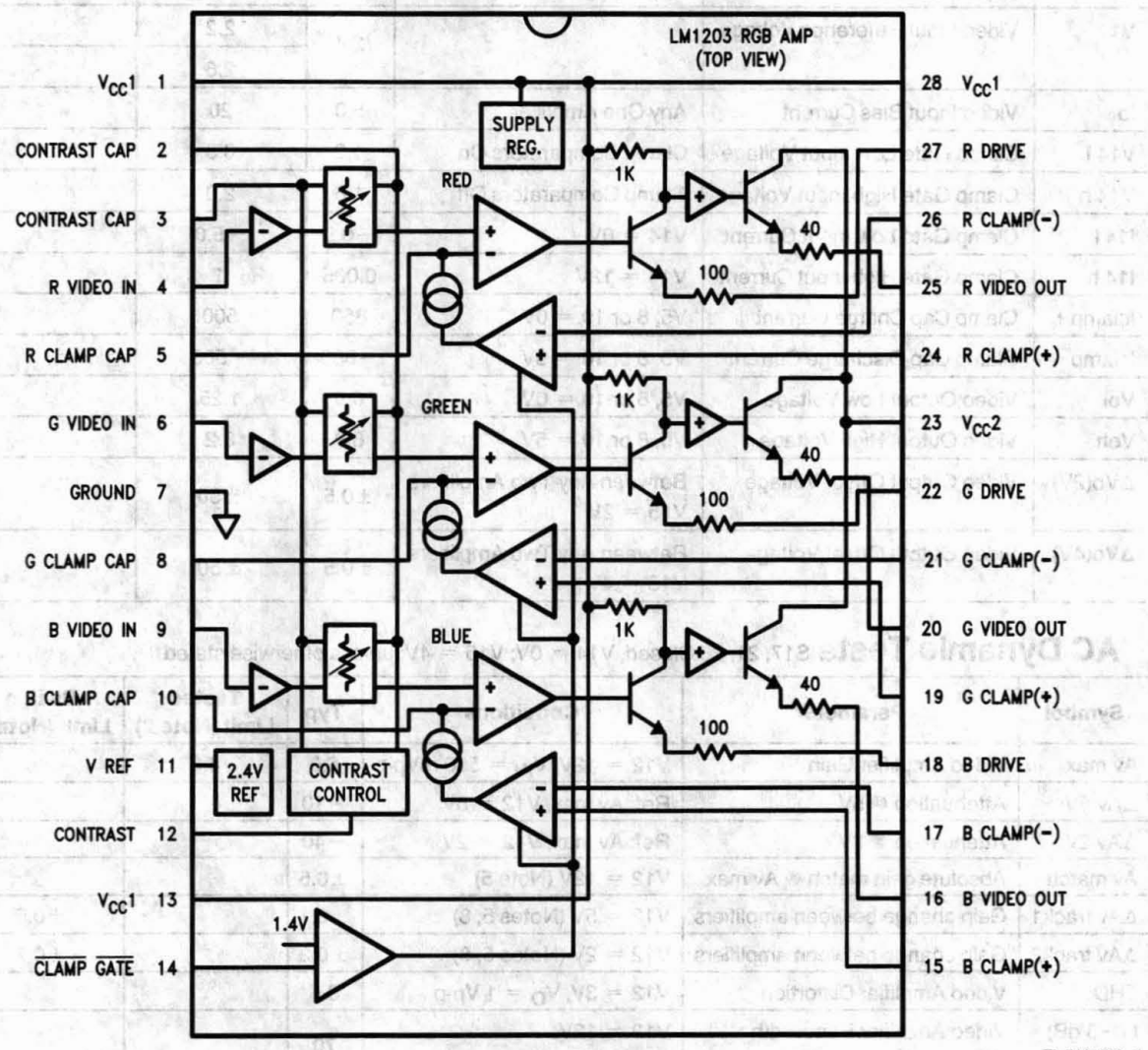
General Description

The LM1203 is a wideband video amplifier system intended for high resolution RGB color monitor applications. In addition to three matched video amplifiers, the LM1203 contains three gated differential input black level clamp comparators for brightness control and three matched attenuator circuits for contrast control. Each video amplifier contains a gain set or "Drive" node for setting maximum system gain (Av = 4 to 10) as well as providing trim capability. The LM1203 also contains a voltage reference for the video inputs. For high resolution monochrome monitor applications see the LM1201 Video Amplifier System datasheet.

Features

- Three wideband video amplifiers (70 MHz @ −3dB)
- Inherently matched (±0.1 dB or 1.2%) attenuators for contrast control
- Three externally gated comparators for brightness control
- Provisions for independent gain control (Drive) of each video amplifier
- Video input voltage reference
- Low impedance output driver

Block and Connection Diagram



TL/H/9178–1

FIGURE 1
Order Number LM1203N
See NS Package Number N28B

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage, V_{CC} Pins 1, 13, 23, 28 (Note 1) 13.5V

Voltage at Any Input Pin, V_{IN} $V_{CC} \geq V_{IN} \geq$ GND

Video Output Current, I16, 20 or 25 28 mA

Power Dissipation, P_D 2.5W

(Above 25°C) Derate Based on θ_{JA} and T_J

Thermal Resistance, θ_{JA} 50°C/W

Junction Temperature, T_J 150°C

Storage Temperature Range, T_{STG} −65°C to +150°C

Lead Temperature, (Soldering, 10 sec.) 265°C

ESD susceptibility 1 kV

Human body model: 100 pF discharged through a 1.5 kΩ resistor

Operating Ratings (Note 9)

Temperature Range 0°C to 70°C

Supply Voltage (V_{CC}) $10.8V \leq V_{CC} \leq 13.2V$

Electrical Characteristics See Test Circuit *(Figure 2)*, T_A = 25°C; $V_{CC1} = V_{CC2}$ = 12V

DC Static Tests S17, 21, 26 Open; V12 = 6V; V14 = 0V; V15 = 2.0V unless otherwise stated

Label	Parameter	Conditions	Typ	Tested Limit (Note 2)	Design Limit (Note 3)	Units (Limits)
Is	Supply Current	V_{CC} 1 only	73	90.0		mA(max)
V11	Video Input Reference Voltage		2.4	2.2		V(min)
				2.6		V(max)
Ib	Video Input Bias Current	Any One Amplifier	5.0	20		μA(max)
V14 l	Clamp Gate Low Input Voltage	Clamp Comparators On	1.2	0.8		V(max)
V14 h	Clamp Gate High Input Voltage	Clamp Comparators Off	1.6	2.0		V(min)
I14 l	Clamp Gate Low Input Current	V14 = 0V	−0.5	−5.0		μA(max)
I14 h	Clamp Gate High Input Current	V14 = 12V	0.005	1		μA(max)
Iclamp+	Clamp Cap Charge Current	V5, 8 or 10 = 0V	850	500		μA(min)
Iclamp−	Clamp Cap Discharge Current	V5, 8 or 10 = 5V	−850	−500		μA(min)
Vol	Video Output Low Voltage	V5, 8 or 10 = 0V	0.9	1.25		V(max)
Voh	Video Output High Voltage	V5, 8 or 10 = 5V	8.9	8.2		V(min)
ΔVo(2V)	Video Output Offset Voltage	Between Any Two Amplifiers V15 = 2V	±0.5	±50		mV(max)
ΔVo(4V)	Video Output Offset Voltage	Between Any Two Amplifiers V15 = 4V	±0.5	±50		mV(max)

AC Dynamic Tests S17, 21, 26 Closed; V14 = 0V; V15 = 4V; unless otherwise stated

Symbol	Parameter	Conditions	Typ	Tested Limit (Note 2)	Design Limit (Note 3)	Units (Limits)
Av max	Video Amplifier Gain	V12 = 12V, V_{IN} = 560 mVp-p	6.0	4.5		V/V(min)
ΔAv 5V	Attenuation @ 5V	Ref: Av max, V12 = 5V	−10			dB
ΔAv 2V	Attenuation @ 2V	Ref: Av max, V12 = 2V	−40			dB
Av match	Absolute gain match @ Av max	V12 = 12V (Note 5)	±0.5			dB
ΔAv track1	Gain change between amplifiers	V12 = 5V (Notes 5, 8)	±0.1		±0.5	dB(max)
ΔAv track2	Gain change between amplifiers	V12 = 2V (Notes 5, 8)	±0.3		±0.7	dB(max)
THD	Video Amplifier Distortion	V12 = 3V, V_O = 1 Vp-p	0.5			%
f (−3 dB)	Video Amplifier Bandwidth (Notes 4, 6)	V12 = 12V, V_O = 100 mV_{rms}	70			MHz
t_r	Output Rise Time (Note 4)	V_O = 4 Vp-p	5			ns
t_f	Output Fall Time (Note 4)	V_O = 4 Vp-p	7			ns

AC Dynamic Tests S17, 21, 26 Closed; V14 = 0V; V15 = 4V; unless otherwise stated (Continued)

Symbol	Parameter	Conditions	Typ	Tested Limit (Note 2)	Design Limit (Note 3)	Units
Vsep 10 kHz	Video Amplifier 10 kHz Isolation	V12 = 12V (Note 7)	−65			dB
Vsep 10 MHz	Video Amplifier 10 MHz Isolation	V12 = 12V (Notes 4, 7)	−46			dB

Note 1: V_{CC} supply pins 1, 13, 23, 28 must be externally wired together to prevent internal damage during V_{CC} power on/off cycles.

Note 2: These parameters are guaranteed and 100% production tested.

Note 3: Design limits are guaranteed (but not 100% production tested). These limits are not used to calculate outgoing quality levels.

Note 4: When measuring video amplifier bandwidth or pulse rise and fall times, a double sided full ground plane printed circuit board without socket is recommended. Video Amplifier 10 MHz isolation test also requires this printed circuit board.

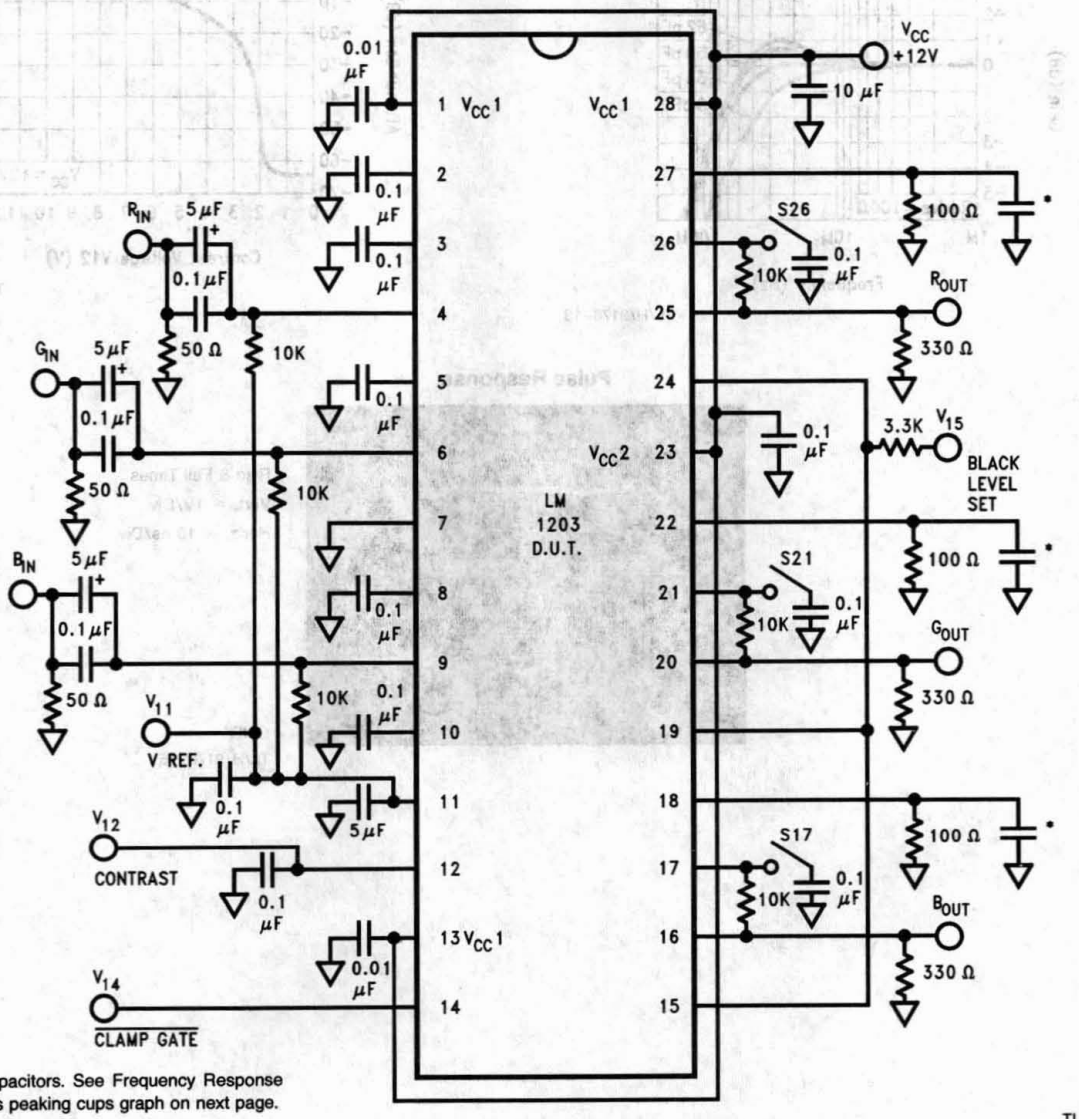
Note 5: Measure gain difference between any two amplifiers. V_{IN} = 1 Vp-p.

Note 6: Adjust input frequency from 10 kHz (Av_{max} ref level) to the −3 dB corner frequency (f −3 dB).

Note 7: Measure output levels of the other two undriven amplifiers relative to driven amplifier to determine channel separation. Terminate the undriven amplifier inputs to simulate generator loading. Repeat test at f_{IN} = 10 MHz for Vsep = 10 MHz.

Note 8: ΔAv track is a measure of the ability of any two amplifiers to track each other and quantifies the matching of the three attenuators. It is the difference in gain change between any two amplifiers with the Contrast Voltage V12 at either 5V or 2V measured relative to an Av max condition V12 = 12V. For example, at Av max the three amplifiers gains might be 17.4 dB, 16.9 dB, and 16.4 dB and change to 7.3 dB, 6.9 dB, and 6.5 dB respectively for V12 = 5V. This yields the measured typical ±0.1 dB channel tracking.

Note 9: Operating Ratings indicate conditions for which the device is functional. See Electrical Specifications for guaranteed performance limits.



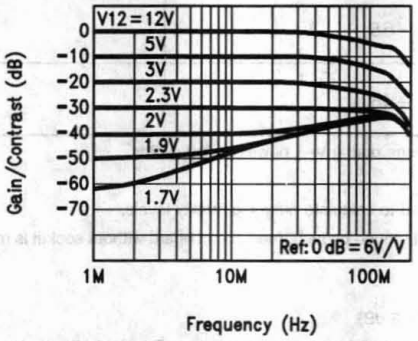
*Peaking capacitors. See Frequency Response using various peaking cups graph on next page.

TL/H/9178–2

FIGURE 2. LM1203 Test Circuit

Typical Performance Characteristics

Contrast vs Frequency



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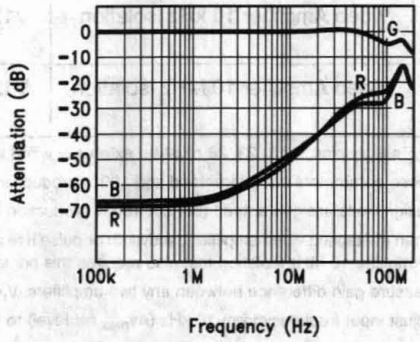
Crosstalk vs Frequency



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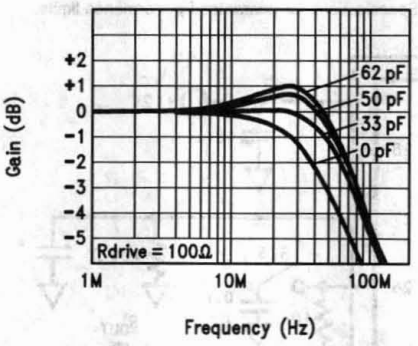
Frequency Response Using Various Peaking Caps



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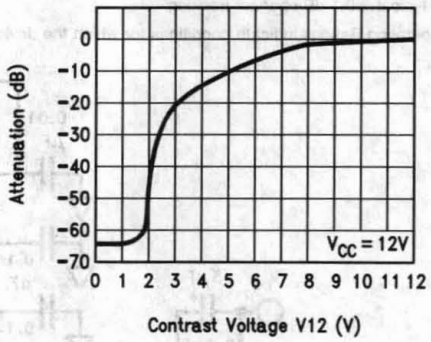
Attenuation vs Contrast Voltage



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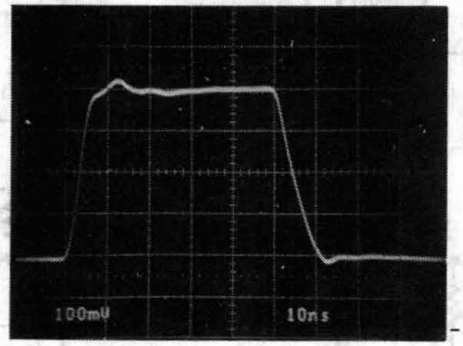
Pulse Response



Rise & Fall Times
Vert. = 1V/Div.
Horiz. = 10 ns/Div.

– – GND

TL/H/9178–15

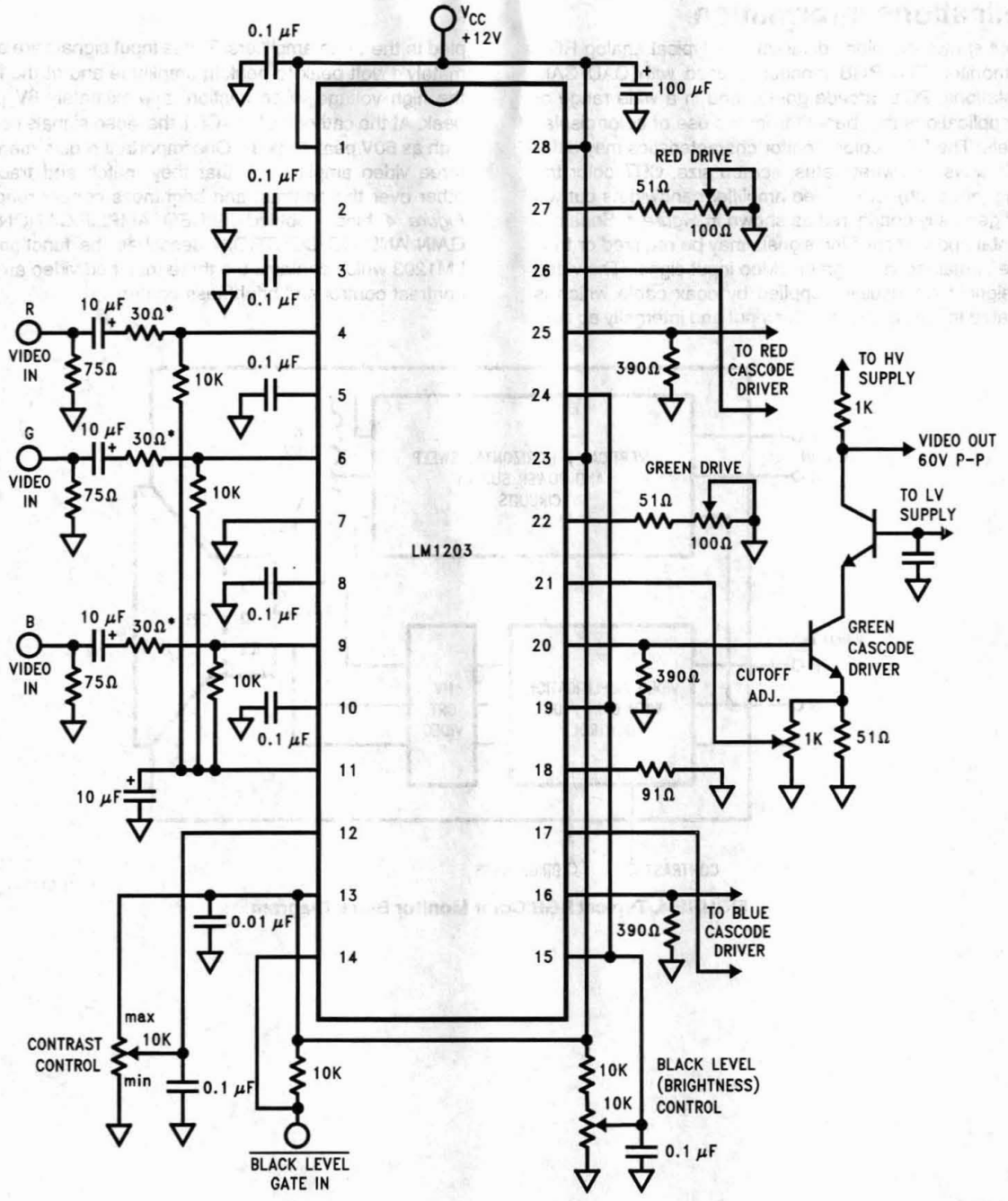


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FIGURE 3. LM1203 Typical Application

* 30Ω resistors are added to the input pins for protection against current surges coming through the 10 μF input capacitors. By increasing these resistors to well over 100Ω the rise and fall times of the LM1203 can be increased for EMI considerations.

2

Applications Information

Figure 4 shows the block diagram of a typical analog RGB color monitor. The RGB monitor is used with CAD/CAM work stations, PC's, arcade games and in a wide range of other applications that benefit from the use of color display terminals. The RGB color monitor characteristics may differ in such ways as sweep rates, screen size, CRT color trio spacing (dot pitch), or in video amplifier bandwidths but will still be generally configured as shown in *Figure 4*. Separate horizontal and vertical sync signals may be required or they may be contained in the green video input signal. The video input signals are usually supplied by coax cable which is terminated in 75Ω at the monitor input and internally ac coupled to the video amplifiers. These input signals are approximately 1 volt peak to peak in amplitude and at the input of the high voltage video section, approximately 6V peak to peak. At the cathode of the CRT the video signals can be as high as 60V peak to peak. One important requirement of the three video amplifiers is that they match and track each other over the contrast and brightness control range. The *Figure 4* block labeled "VIDEO AMPLIFICATION WITH GAIN AND DC CONTROL" describes the function of the LM1203 which contains the three matched video amplifiers, contrast control and brightness control.

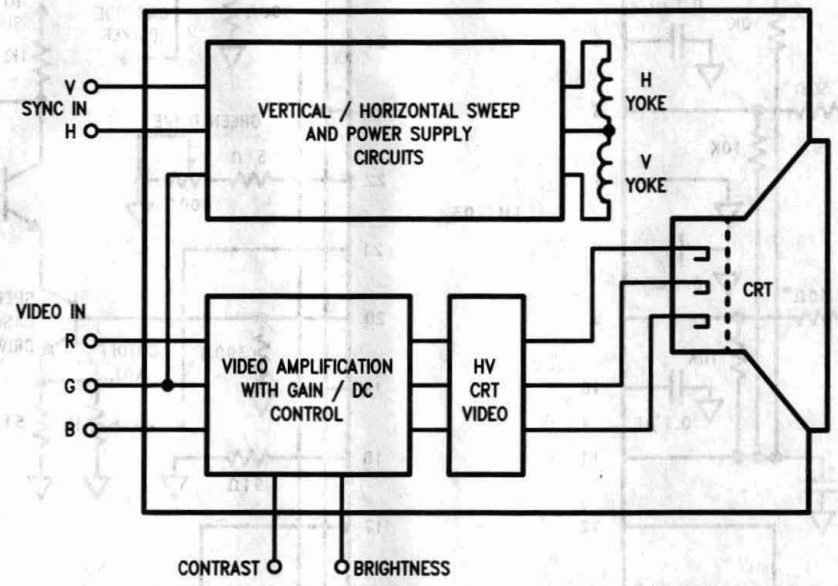

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FIGURE 4. Typical RGB Color Monitor Block Diagram

Circuit Description

Figure 5 is a block diagram of one of the video amplifiers along with the contrast and brightness controls. The contrast control is a dc-operated attenuator which varies the ac gain of all three amplifiers simultaneously while not introducing any signal distortions or tracking errors. The brightness control function requires a "sample and hold" circuit (black level clamp) which holds the dc bias of the video amplifiers and CRT cathodes constant during the black level reference portion of the video waveform. The clamp comparator, when gated on during this reference period, will charge or discharge the clamp capacitor until the plus input of the clamp comparator matches that of the minus input voltage which was set by the brightness control.

Figure 6 is a simplified schematic of one of the three video amplifiers along with the recommended external components. The IC pin numbers are circled with all external components shown outside of the dashed line. The video input is applied to pin 6 via the 10 μF coupling capacitor. DC bias to the video input is through the 10 kΩ resistor which is connected to the 2.4V reference at pin 11. The low frequency roll-off of the amplifier is set by these two components. Transistor Q1 buffers the video signal to the base of Q2. The Q2 collector current is then directed to the V_{CC} 1 supply directly or through the 1k load resistor depending upon the differential DC voltage at the bases of Q3 and Q4. The Q3 and Q4 differential base voltage is determined by the contrast control circuit which is described below. RF decoupling capacitors are required at pins 2 and 3 to insure high frequency isolation between the three video amplifiers which share these common connections. The black level dc voltage at the collector of Q4 is maintained by Q5 and Q6 which are part of the black level clamp circuit also described below. The video signal appearing at the collector of Q4 is then buffered by Q7 and level shifted down by Z1 and Q8 to the base of Q9 which will then provide additional system gain.

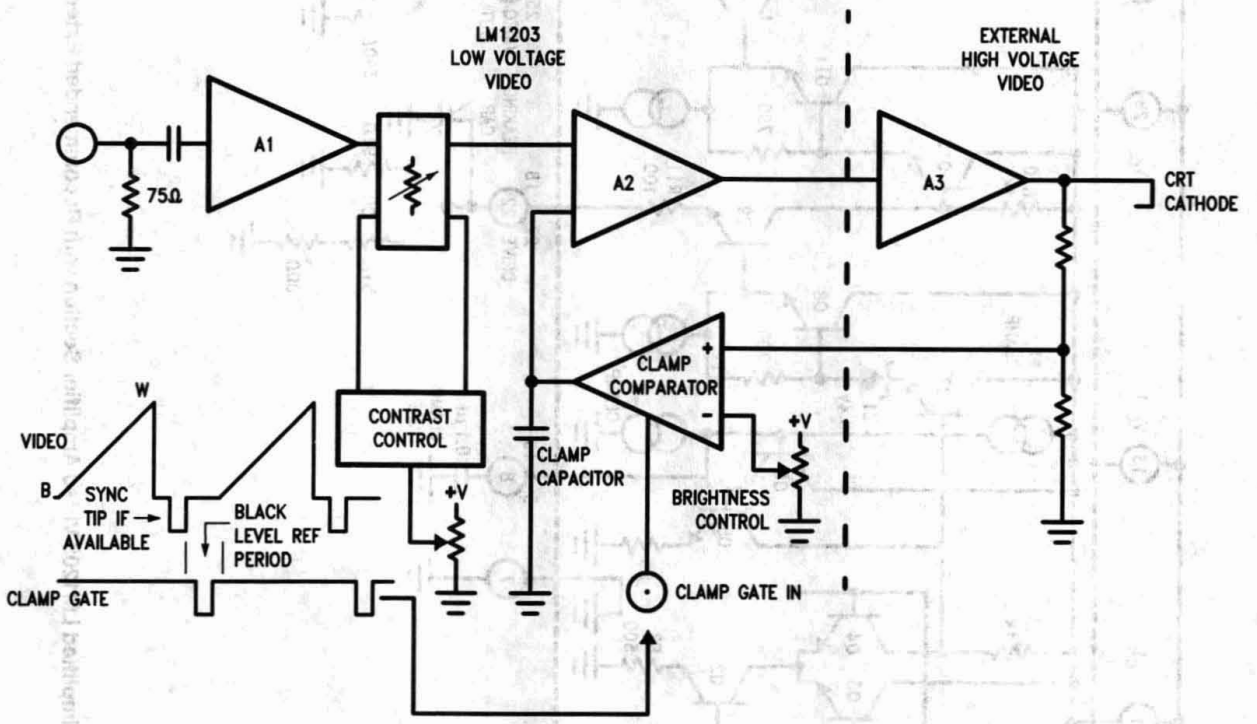

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FIGURE 5. Block Diagram of LM1203 Video Amplifier with Contrast and Black Level Control

Circuit Description (Continued)

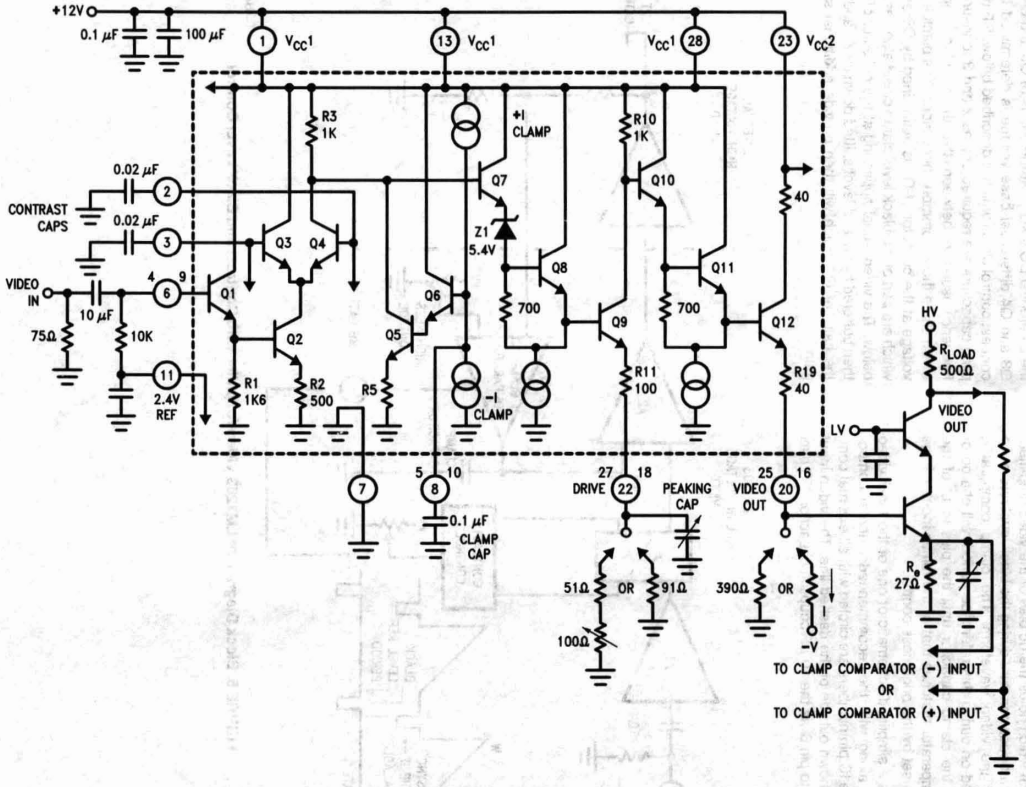

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FIGURE 6. Simplified LM1203 Video Amplifier Section with Recommended External Components

Circuit Description (Continued)

The "Drive" pin will allow the user to trim the Q9 gain of each amplifier to correct for differences in the CRT and high voltage cathode driver gain stages. A small capacitor (33 pF) at this pin will extend the high frequency gain of the video amplifier by compensating for some of the internal high frequency roll off. To use this capacitor and still provide variable gain adjustment, the 51Ω and series 100Ω pot should be used with the red and green drive pins. The 91Ω resistor used with the blue drive pin will set the system gain to approximately 6.2 and allow adjustment of the red and green gains to 6.2 plus or minus 25%. The video signal at the collector of Q9 is buffered and level shifted down by Q10 and Q11 to the base of the output emitter follower Q12. Between the emitter of Q12 and the video output pin is a 40Ω resistor which was included to prevent spurious oscillations when driving capacitive loads. An external emitter resistor must be added between the video output pin and ground. The value of this resistor should not be less than 390Ω or package power limitations may be exceeded when worst case (high supply, max supply current, max temp) calculations are made. If negative going pulse slewing is a problem because of high capacitive loads (>10 pF), a more efficient method of emitter pull down would be to connect a suitable resistor to a negative supply voltage. This has the effect of a current source pull down when the minus supply voltage is −12V and the emitter current is approximately 10 mA. The system gain will also increase slightly because less signal will be lost across the internal 40Ω resistor. Precautions must be taken to prevent the video output pin from going below ground because IC substrate currents may cause erratic operation. The collector currents from the video output transistors are returned to the power supply at V_{CC} 2 pin 23. When making power dissipation calculations note that the data sheet specifies only the V_{CC} 1 supply current at 12V. The IC power dissipation contribution of V_{CC} 2 is dependent upon the video output emitter pull down load.

In applications that require video amplifier shut down because of fault conditions detected by monitor protection circuits, pin 11 and the wiper arms of the contrast and brightness controls can be grounded without harming the IC. This assumes some series resistance between the top of the control pots and V_{CC}.

Figure 7 shows the internal construction of the pin 11 2.4V reference circuit which is used to provide temperature and supply voltage tracking compensation for the video amplifier inputs. The value of the external DC biasing resistors should not be larger than 10 kΩ because minor differences in input bias currents to the individual video amplifiers may cause offsets in gain.

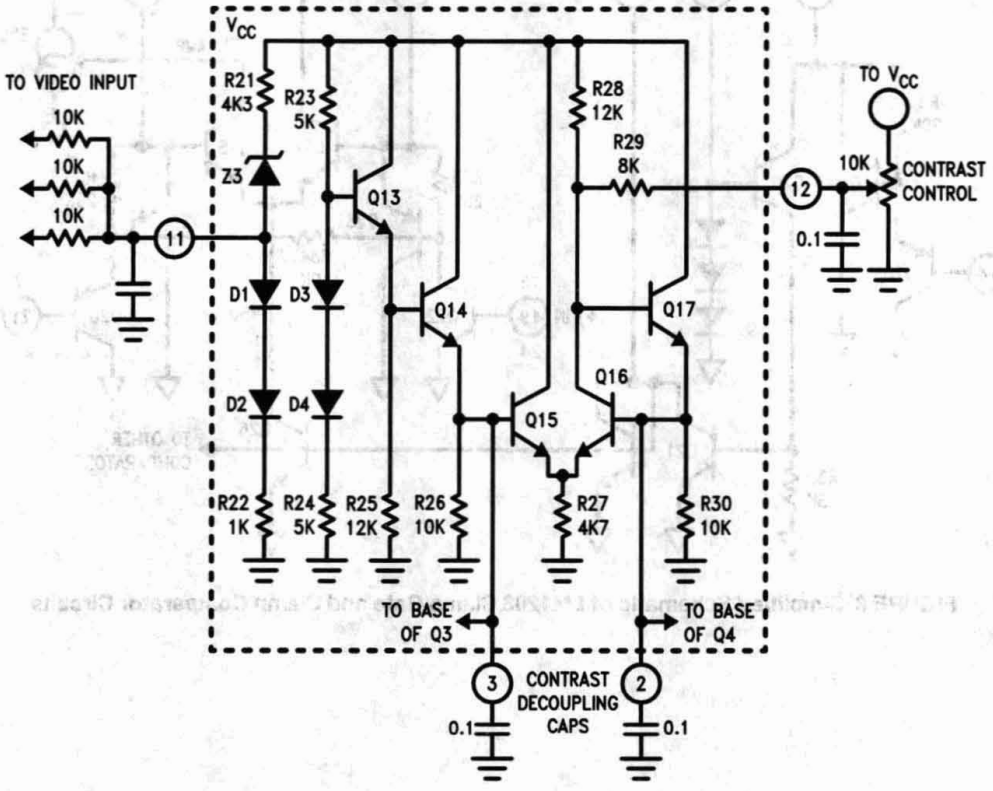

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FIGURE 7. LM1203 Video Input Voltage Reference and Contrast Control Circuits

Circuit Description (Continued)

Figure 7 also shows how the contrast control circuit is configured. Resistors R23, 24, diodes D3, 4 and transistor Q13 are used to establish a low impedance zero TC half supply voltage reference at the base of Q14. The differential amplifier formed by Q15, 16 and feedback transistor Q17 along with resistors R27, 28 establish a diferential base voltage for Q3 and Q4 in *Figure 6*. When externally adding or subtracting current from the collector of Q16, a new differential voltage is generated that reflects the change in the ratio of currents in Q15 and Q16. To provide voltage control of the Q16 current, resistor R29 is added between the Q16 collector and pin 12. A capacitor should be added from pin 12 to ground to prevent noise from the contrast control pot from entering the IC.

Figure 8 is a simplified schematic of the clamp gate and clamp comparator sections of the LM1203. The clamp gate circuit consists of a PNP input buffer transistor (Q18), a PNP emitter coupled pair referenced on one side to 2.1V (Q19, 20) and an output switch (Q21). When the clamp gate input at pin 14 is high (>1.5V) the Q21 switch is on and shunts the I1 850 μA current to ground. When pin 14 is low (<1.3V) the Q21 switch is off and the I1 850 μA current source is mirrored or "turned around" by reference diode D5 and Q26 to provide a 850 μA current source for the clamp comparator(s). The inputs to the comparator are similar to the clamp gate input except that an NPN emitter coupled pair is used to control the current which will charge or discharge the clamp capacitors at pins 5, 8, or 10. PNP transistors are used at the inputs because they offer a number of advantages over NPNs. PNPs will operate with base voltages at or near ground and will usually have a greater reverse emitter base breakdown voltage (BVebo). Because the differential input voltage to the clamp comparator during the video scan period could be greater than the BVebo of NPN transistors a resistor (R34) with a value one half that of R33 or R35 is connected between the bases of Q23 and Q27. This resistor will limit the maximum differential input to Q24, 25 to approximately 350 mV. The clamp comparator common mode range is from ground to approximately 9V and the maximum differential input voltage is V_{CC} and ground.

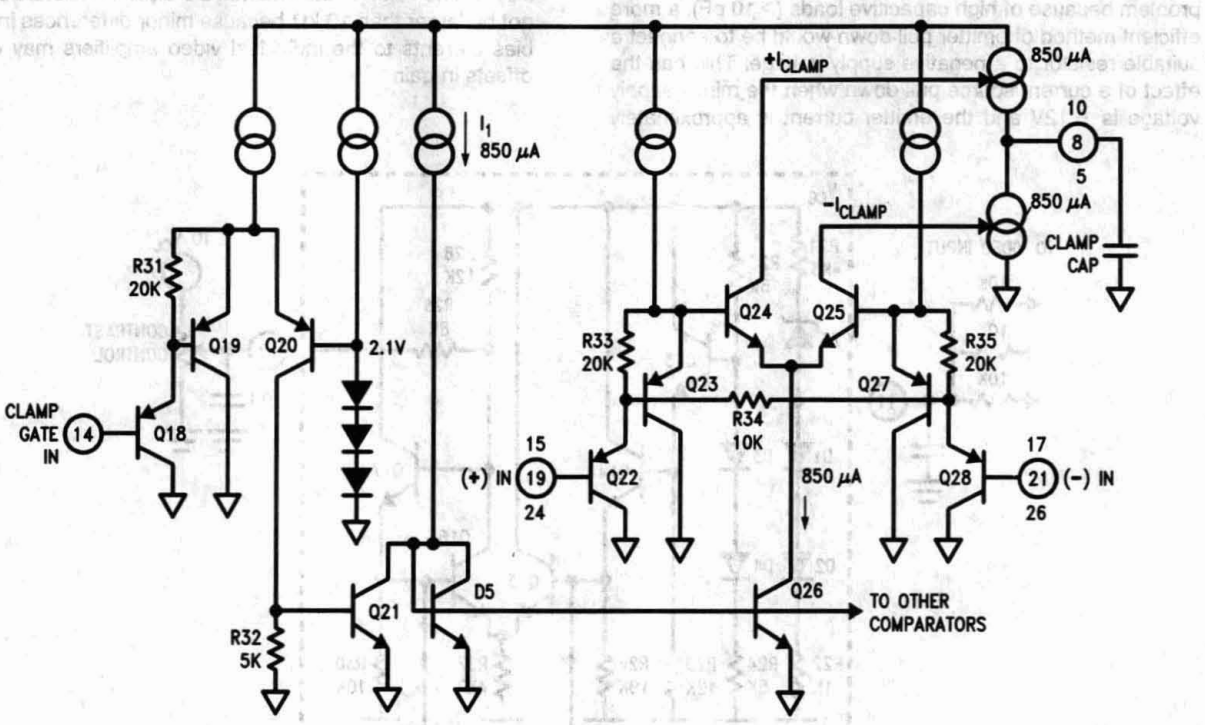

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FIGURE 8. Simplified Schematic of LM1203 Clamp Gate and Clamp Comparator Circuits

Additional Applications of the LM1203

Figure 9 shows how the LM1203 can be set up as a video buffer which could be used in low cost video switcher applications. Pin 14 is tied high to turn off the clamp comparators. The comparator input pins should be grounded as shown. Sync tip (black level if sync is not included) clamping is provided by diodes at the amplifier inputs. Note that the clamp cap pins are tied to the Pin 11 2.4V reference. This was done, along with the choice of 200Ω for the drive pin resistor, to establish an optimum DC output voltage. The contrast control (Pin 12) will provide the necessary gain or attenuation required for channel balancing. Changing the contrast control setting will cause minor DC shifts at the amplifier output which will not be objectionable as the output is AC coupled to the load. The dual NPN/PNP emitter follower will provide a low impedance output drive to the AC coupled 75Ω output impedance setting resistor. The dual 500 μF capacitors will set the low frequency response to approximately 4 Hz.

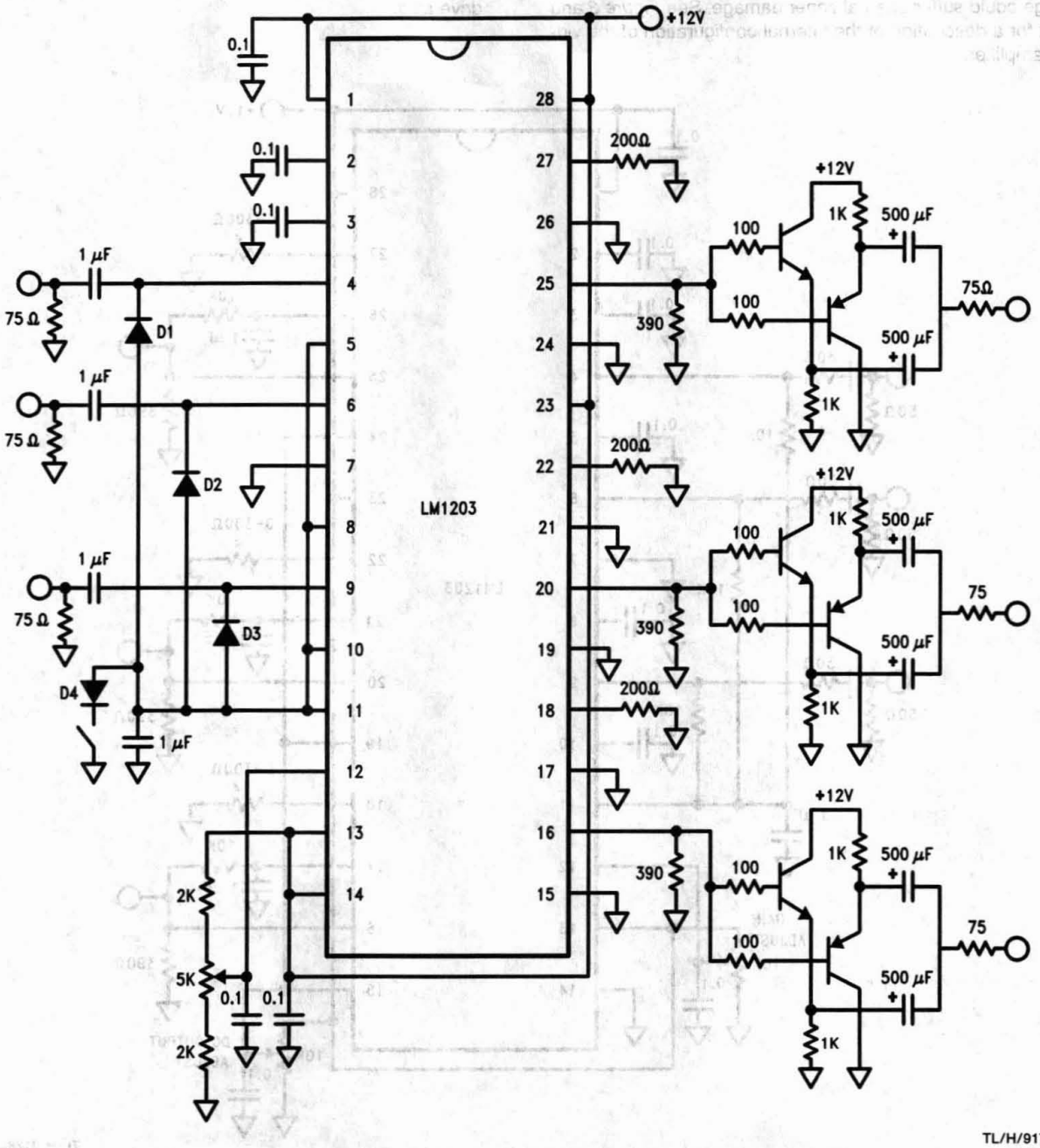

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FIGURE 9. RGB Video Buffer with Diode Sync Tip Clamps and 75Ω Cable Driver

Additional Applications of the LM1203 (Continued)

When diode D4 at Pin 11 is switched to ground the input video signals will be DC shifted down and clamped at a voltage near ground (approximately 250 mV). This will disable the video amplifiers and force the output DC level low. The DC outputs from other similarly configured LM1203s could overide this lower DC level and provide the output signals to the 75Ω cable drivers. In this case any additional LM1203s would share the same 390Ω output resistor. The maximum DC plus peak white output voltage should not be allowed to exceed 7V because the "off" amplifier output stage could suffer internal zener damage. See *Figure 3* and text for a description of the internal configuration of the video amplifier.

Figure 10 shows the configuration for a three channel high frequency amplifier with non gated DC feedback. Pin 14 is tied low to turn on the clamp comparators (feedback amplifiers). The inverting inputs (Pins 17, 21, 26) are connected to the amplifier outputs from a low pass filter. Additional low frequency filtering is provided by the clamp caps. The drive resistors can be made variable or fixed at values between 0 and 300Ω. Maximum output swings are achieved when the DC output is set to approximately 4V. The high frequency response will be dependent upon external peaking at the drive pins.

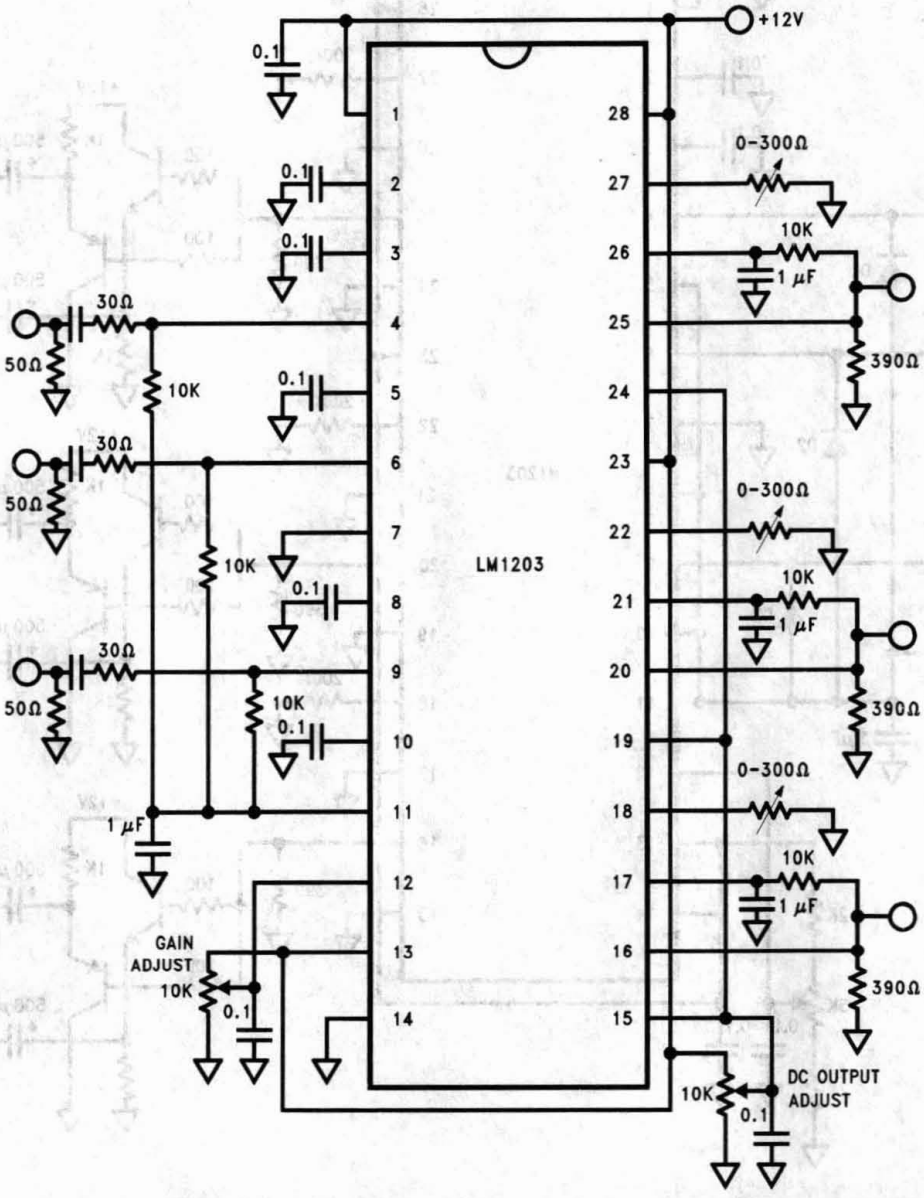

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FIGURE 10. Three Channel High Frequency Amplifier with Non-gated DC Feedback (Non-video Applications)

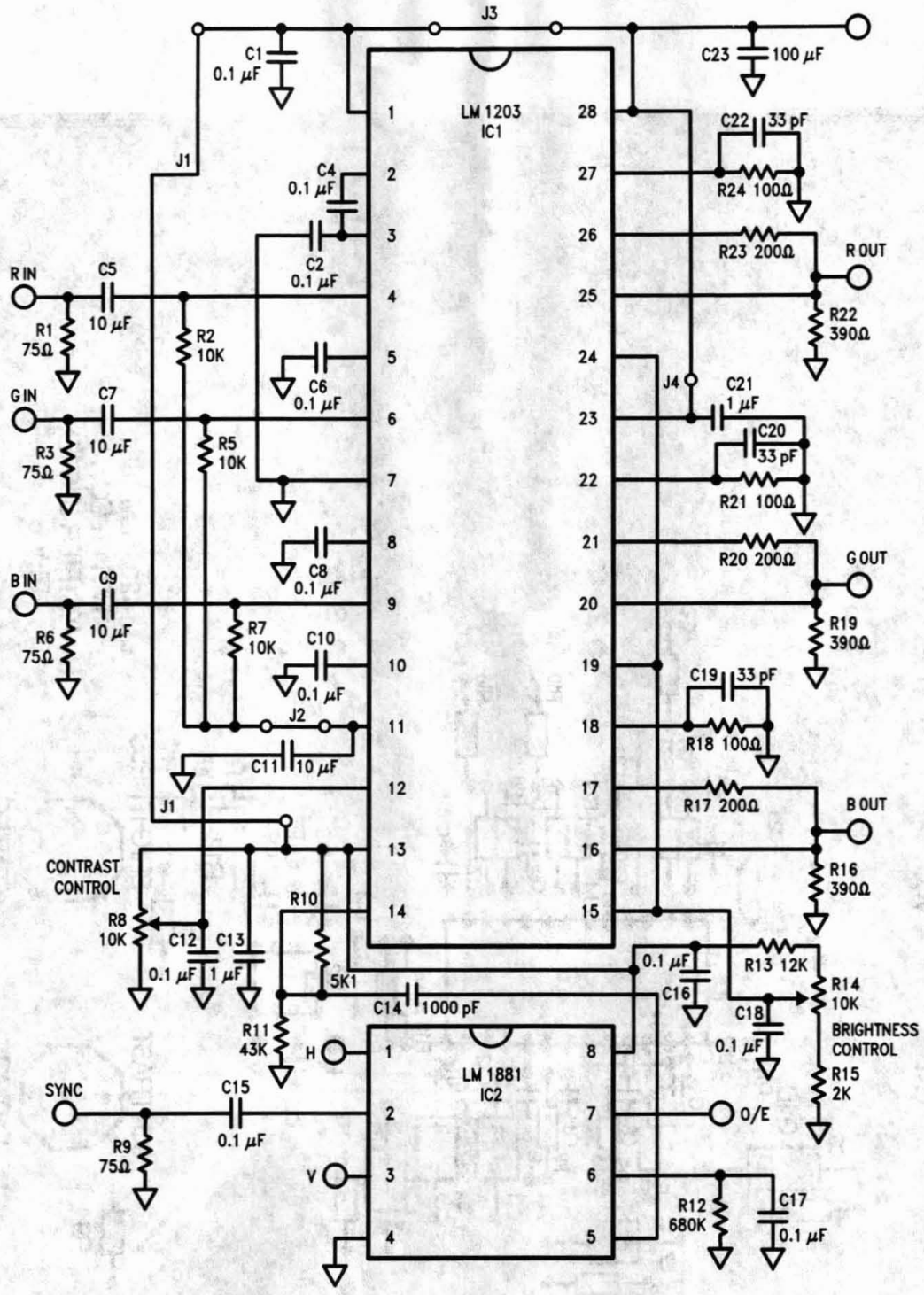

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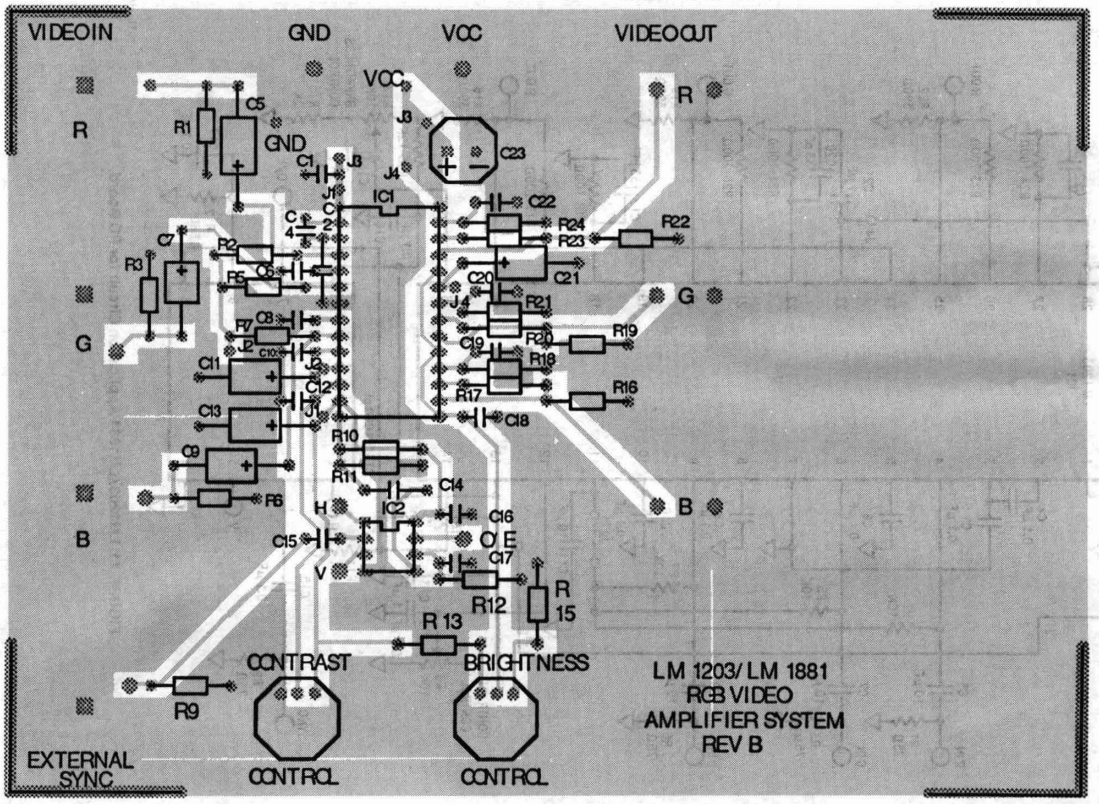
FIGURE 11. LM1203/LM1881 Application Circuit for PC Board

PC Board with Components



TL/H/9178–17

National Semiconductor

LM1203A
150 MHz RGB Video Amplifier System

General Description

The LM1203A is an improved version of the popular LM1203 wideband video amplifier system. The device is intended for high resolution RGB CRT monitors. In addition to three matched video amplifiers, the LM1203A contains three gated differential input black level clamp comparators for brightness control and three matched attenuator circuits for contrast control. Each video amplifier contains a gain set or "Drive" node for setting maximum system gain or providing gain trim capability for white balance. The LM1203A also contains a voltage reference for the video inputs. The LM1203A is pin and function compatible with the LM1203.

Features

- Three wideband video amplifiers 150 MHz @ −3 dB
- Matched (±0.1 dB or 1.2%) attenuators for contrast control
- Three externally gated comparators for brightness control
- Provisions for individual gain control (Drive) of each video amplifier
- Video input voltage reference
- Low impedance output driver

Improvements over LM1203

- 150 MHz vs 70 MHz bandwidth
- V_{OUT} low: 0.15V vs 0.9V
- t_r, t_f: 4 ns vs 7 ns
- Built in power down spot killer

Applications

- High resolution RGB CRT monitors
- Video AGC amplifiers
- Wideband amplifiers with gain and DC offset controls

Block and Connection Diagrams

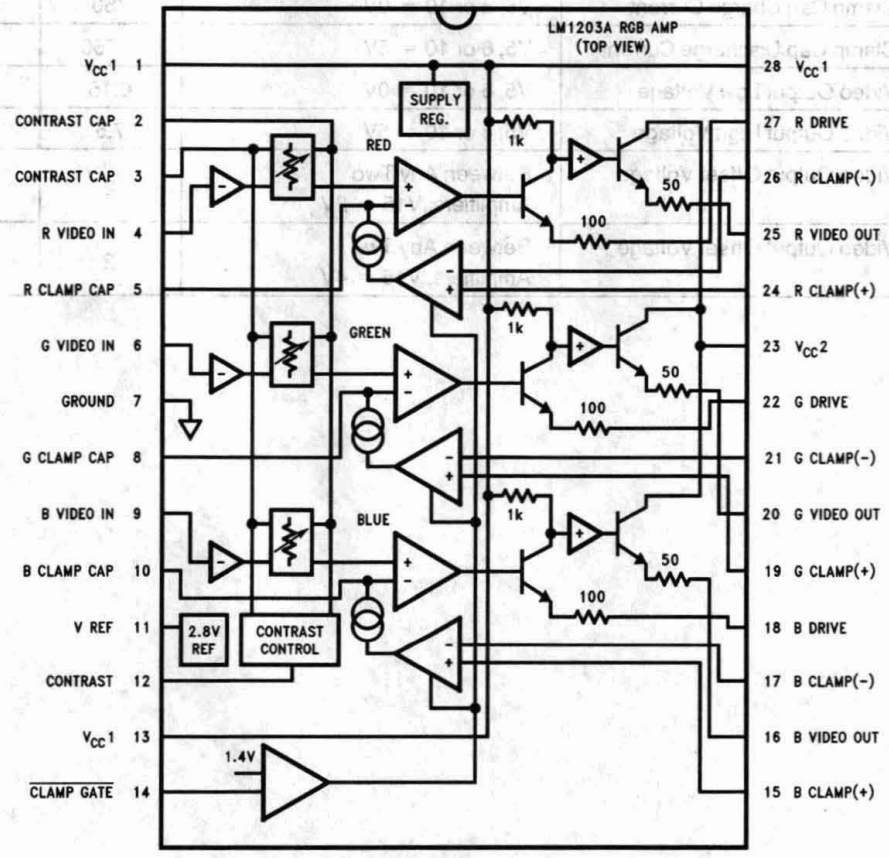


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FIGURE 1

Order Number LM1203AN
See NS Package Number N28B

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

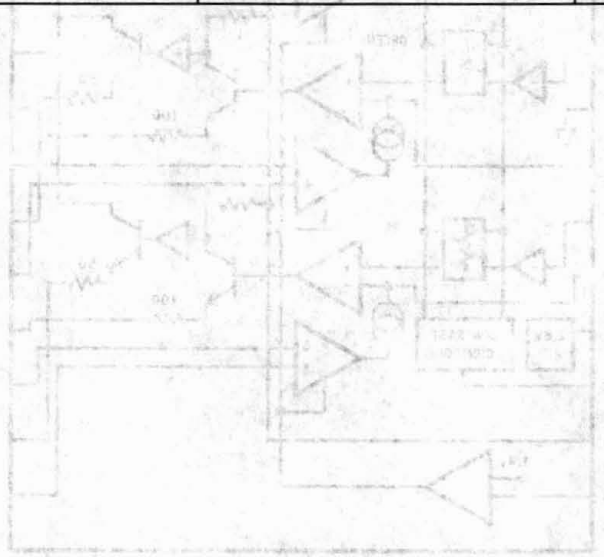
Supply Voltage (V_{CC}) Pins 1, 13, 23, 28 (Note 3)	13.5V
Peak Video Output Source Current (Any One Amp) Pins 16, 20 or 25	28 mA
Voltage at Any Input Pin (V_{IN})	$V_{CC} \geq V_{IN} \geq$ GND
Power Dissipation, (P_D) (Above 25°C derate based on θ_{JA} and T_J)	2.5W
Thermal Resistance (θ_{JA})	50°C/W
Junction Temperature (T_J)	150°C
ESD Susceptibility (Note 4)	2 kV
Storage Temperature	−65°C to 150°C
Lead Temperature (Soldering, 10 sec.)	265°C

Operating Ratings (Note 2)

Temperature Range	−20°C to +80°C
Supply Voltage (V_{CC})	$10.8V \leq V_{CC} \leq 13.2V$

DC Electrical Characteristics See Test Circuit *(Figure 2)*, T_A = 25°C; $V_{CC1} = V_{CC2}$ = 12V. S17, 21, 26 Open; V12 = 6V; V14 = 0V; V15 = 2.0V unless otherwise stated.

Symbol	Parameter	Conditions	Typical (Note 5)	Limit (Note 6)	Units
I_S	Supply Current	$V_{CC1} + V_{CC2}$, $R_L = \infty$ (Note 7)	70	95	mA (max)
V11	Video Input Reference Voltage		2.8	2.5	V (min)
				3.1	V (max)
I_B	Video Input Bias Current	Any One Amplifier	7	20	μA (max)
V_{14L}	Clamp Gate Low Input Voltage	Clamp Comparators On	1.2	0.8	V (max)
V_{14H}	Clamp Gate High Input Voltage	Clamp Comparators Off	1.6	2.0	V (min)
I_{14L}	Clamp Gate Low Input Current	V14 = 0V	−1	−5.0	μA (max)
I_{14H}	Clamp Gate High Input Current	V14 = 12V	0.07	0.2	μA (max)
I_{CLAMP+}	Clamp Cap Charge Current	V5, 8 or 10 = 0V	750	500	μA (min)
I_{CLAMP-}	Clamp Cap Discharge Current	V5, 8 or 10 = 5V	−750	−500	μA (min)
V_{OL}	Video Output Low Voltage	V5, 8 or 10 = 0V	0.15	0.5	V (max)
V_{OH}	Video Output High Voltage	V5, 8 or 10 = 5V	7.5	7	V (min)
$\Delta V_{O(2V)}$	Video Output Offset Voltage	Between Any Two Amplifiers, V15 = 2V	2	±25	mV (max)
$\Delta V_{O(4V)}$	Video Output Offset Voltage	Between Any Two Amplifiers, V15 = 4V	2	±25	mV (max)



AC Electrical Characteristics

See Test Circuit *(Figure 2)*, T_A = 25°C; V_{CC1} = V_{CC2} = 12V. S17, 21, 26 Closed; V14 = 0V; V15 = 4V unless otherwise stated.

Symbol	Parameter	Conditions	Typical (Note 5)	Limit (Note 6)	Units
$A_{V\ max}$	Video Amplifier Gain	V12 = 12V, V_{IN} = 560 mV_{PP}	6.5	4.5	V/V (min)
$\Delta A_{V\ 5V}$	Attenuation @ 5V	Ref: A_V max, V12 = 5V	−8		dB
$\Delta A_{V\ 2V}$	Attenuation @ 2V	Ref: A_V max, V12 = 2V	−30		dB
$A_{V\ match}$	Absolute Gain Match @ A_V max	V12 = 12V (Note 8)	±0.3		dB
$\Delta A_{V\ track\ 1}$	Gain Change Between Amplifiers	V12 = 5V (Notes 8, 9)	±0.1		dB
$\Delta A_{V\ track\ 2}$	Gain Change Between Amplifiers	V12 = 5V (Notes 8, 9)	±0.3		dB
THD	Video Amplifier Distortion	V12 = 3V, V_O = 1 V_{PP}	1		%
f (−3 dB)	Video Amplifier Bandwidth (Notes 10, 11)	V12 = 12V, V_O = 4 V_{PP} (No External Peaking Capacitor)	100		MHz
f (−3 dB)	Video Amplifier Bandwidth (Notes 10, 11)	V12 = 12V, V_O = 4 V_{PP} With 18 pF Peaking Cap from Pins 18, 22 and 27 to GND	150		MHz
t_r	Output Rise Time (Note 10)	V_O = 4 V_{PP} (No External Peaking Capacitor)	3		ns
t_f	Output Fall Time (Note 10)	V_O = 4 V_{PP} (No External Peaking Capacitor)	4		ns
$V_{sep\ 10\ kHz}$	Video Amplifier 10 kHz Isolation	V12 = 12V (Note 12)	−70		dB
$V_{sep\ 10\ MHz}$	Video Amplifier 10 MHz Isolation	V12 = 12V (Notes 10, 12)	−50		dB

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur.

Note 2: Operating Ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.

Note 3: V_{CC} supply pins 1, 13, 23, 28 must be externally wired together to prevent internal damage during V_{CC} power on/off cycles.

Note 4: Human body model, 100 pF discharged through a 1.5 kΩ resistor.

Note 5: Typical specifications are specified at +25°C and represent the most likely parametric norm.

Note 6: Tested limits are guaranteed to National's AOQL (Average Outgoing Quality Level).

Note 7: The supply current specified is the quiescent current for V_{CC1} and V_{CC2} with R_L = ∞, see *Figure 2's* test circuit. The supply current for V_{CC2} (pin 23) also depends on the output load. With video output at 2V DC, the additional current through V_{CC2} is 18 mA for *Figure 2's* test circuit.

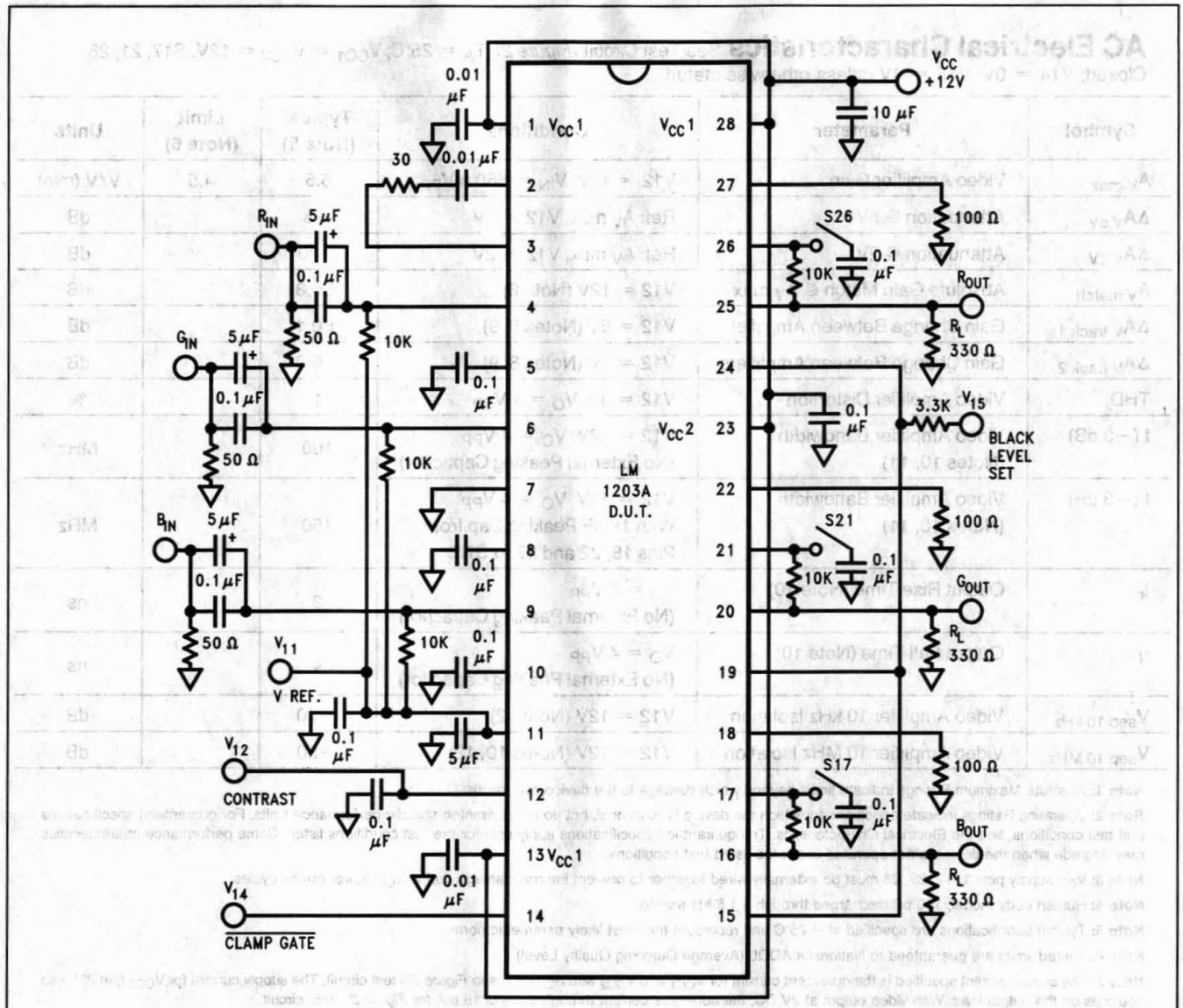
Note 8: Measure gain difference between any two amplifiers. V_{IN} = 1 V_{PP}.

Note 9: $\Delta A_{V\ track}$ is a measure of the ability of any two amplifiers to track each other and quantifies the matching of the three attenuators. It is the difference in gain change between any two amplifiers with the contrast voltage (V12) at either 5V or 2V measured relative to an A_V max condition, V12 = 12V. For example, at A_V max the three amplifiers' gains might be 17.4 dB, 16.9 dB and 16.4 dB and change to 7.3 dB, 6.9 dB, and 6.5 dB respectively for V12 = 5V. This yields the measured typical ±0.1 dB channel tracking.

Note 10: When measuring video amplifier bandwidth or pulse rise and fall times, a double sided full ground plane printed circuit board without socket is recommended. Video amplifier 10 MHz isolation test also requires this printed circuit board.

Note 11: Adjust input frequency from 10 kHz (A_V max reference level) to the −3 dB corner frequency ($f_{-3\ dB}$).

Note 12: Measure output levels of the other two undriven amplifiers relative to the driven amplifier to determine channel separation. Terminate the undriven amplifier inputs to simulate generator loading. Repeat test at f_{IN} = 10 MHz for V_{sep} = 10 MHz.

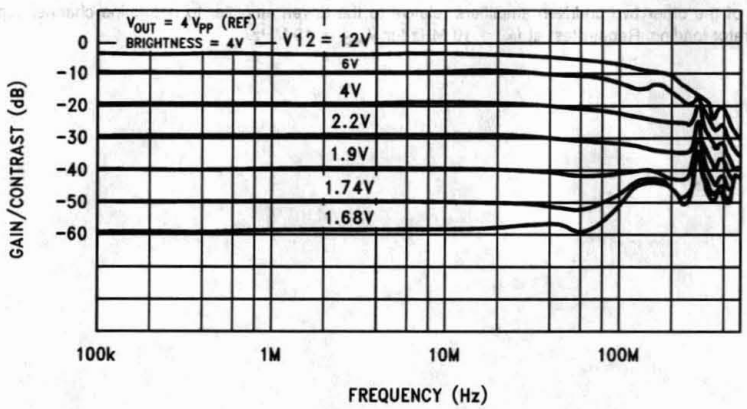


TL/H/11441–2

FIGURE 2. LM1203A Test Circuit

Typical Performance Characteristics V_{CC} = 12V, T_A = 25°C unless otherwise specified

Contrast vs Frequency



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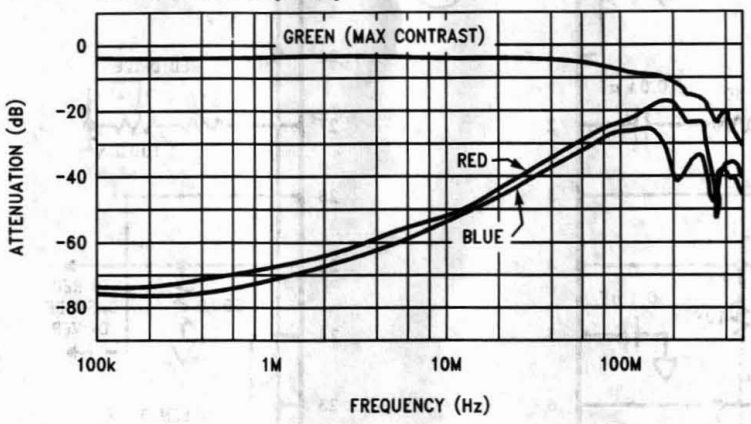
Typical Performance Characteristics V_{CC} = 12V, T_A = 25°C unless otherwise specified (Continued)

Crosstalk vs Frequency



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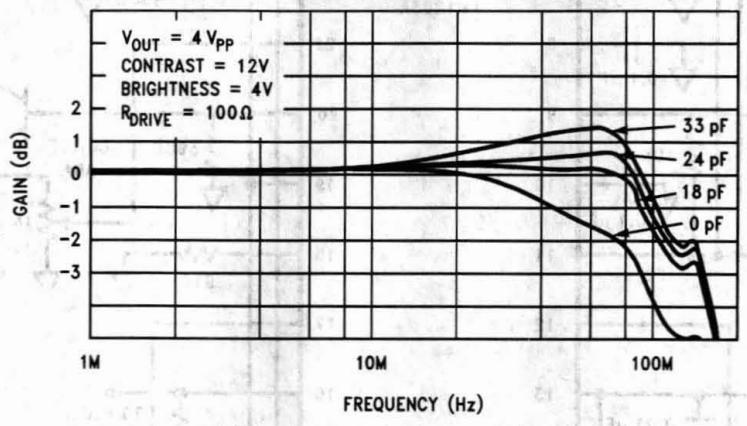
Frequency Response Using Various Peaking Caps



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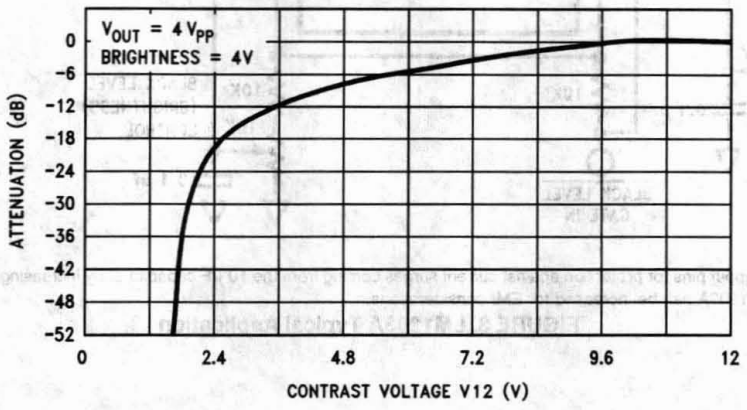
Attenuation vs Contrast Voltage



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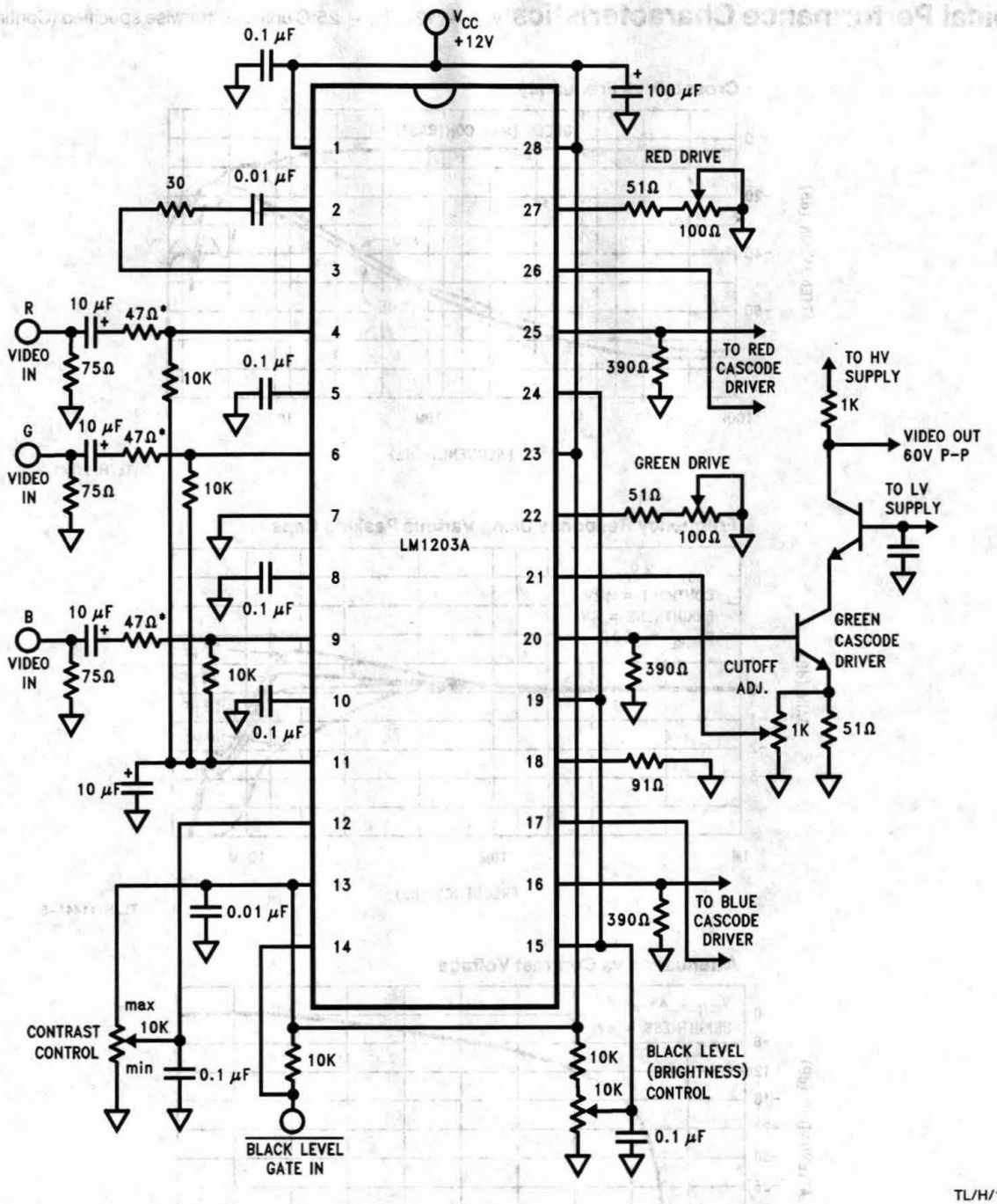

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*47Ω resistors are added to the input pins for protection against current surges coming from the 10 μF capacitors. By increasing these resistors to well over 100Ω the rise and fall times of the LM1203A can be increased for EMI considerations.

FIGURE 3. LM1203A Typical Application

Applications Information

Figure 4 shows the block diagram of a typical analog RGB color monitor. The RGB monitor is used with CAD/CAM work stations, PC's, arcade games and in a wide range of other applications that benefit from the use of color display terminals. The RGB color monitor characteristics may differ in such ways as sweep rates, screen size, CRT color trio spacing (dot pitch), or in video amplifier bandwidths but will still be generally configured as shown in *Figure 4*. Separate horizontal and vertical sync signals may be required or they may be contained in the green video input signal. The video input signals are usually supplied by coax cable which is terminated in 75Ω at the monitor input and internally AC coupled to the video amplifiers. These input signals are approximately 1V peak to peak in amplitude and at the input of the high voltage video section, approximately 6V peak to peak. At the cathode of the CRT the video signals can be as high as 60V peak to peak. One important requirement of the three video amplifiers is that they match and track each other over the contrast and brightness control range. The *Figure 4* block labeled "VIDEO AMPLIFICATION WITH GAIN AND DC CONTROL" describes the function of the LM1203A which contains the three matched video amplifiers, contrast control and brightness control.

Circuit Description

Figure 5 is a block diagram of one of the video amplifiers along with the contrast and brightness controls. The contrast control is a DC-operated attenuator which varies the AC gain of all three amplifiers simultaneously while not introducing any signal distortions or tracking errors. The brightness control function requires a "sample and hold" circuit (black level clamp) which holds the DC bias of the video amplifiers and CRT cathodes constant during the black level reference portion of the video waveform. The clamp comparator, when gated on during this reference period, will charge or discharge the clamp capacitor until the plus input of the clamp comparator matches that of the minus input voltage which was set by the brightness control.

VIDEO AMPLIFIER SECTION

Figure 6 is a simplified schematic of one of the three video amplifiers along with the recommended external components. The IC pin numbers are circled and all external components are shown outside the dashed line. The video input is applied to pin 6 via a 10 μF coupling capacitor. DC bias for the video input is through the 10k resistor connected to the 2.8V reference at pin 11. The low frequency roll-off of the amplifier is set by these two components. Transistor Q1 buffers the video signal to the base of Q2. Q2's collector current is then directed to the V_{CC1} supply directly or through the 2k load resistor depending upon the differential DC voltage at the bases of Q3 and Q4. This differential DC voltage is generated by the contrast control circuit which is described in the following sections. A 0.01 μF decoupling capacitor in series with a 30Ω resistor is required between pins 2 and 3 to ensure high frequency isolation between the three video amplifiers which share these common connections. The video signal is buffered by Q5 and Q6 and DC level shifted by the voltage drop across R5. The magnitude of the current through R5 is determined by the voltage at pin 8. The voltage at pin 8 is set by the clamp comparator output current which charges or discharges the clamp hold capacitor during the black level period of the video waveform. Transistors Q9 and Q10 are Darlington connected to ensure a minimum discharge of the clamp hold capacitor during the time that the clamp capacitor is gated off. Q7, Q8 and R6 form a current mirror which sets a voltage at the base of Q11. Q11 buffers the video signal to the base of Q12 which provides additional signal gain. The "Drive" pin allows the user to trim the Q12 gain of each amplifier to correct for gain differences in the CRT and high voltage cathode driver gain stages. A small capacitor (several pico-Farads) from the "Drive" pin to ground will cause high frequency peaking and slightly improve the amplifier's bandwidth.

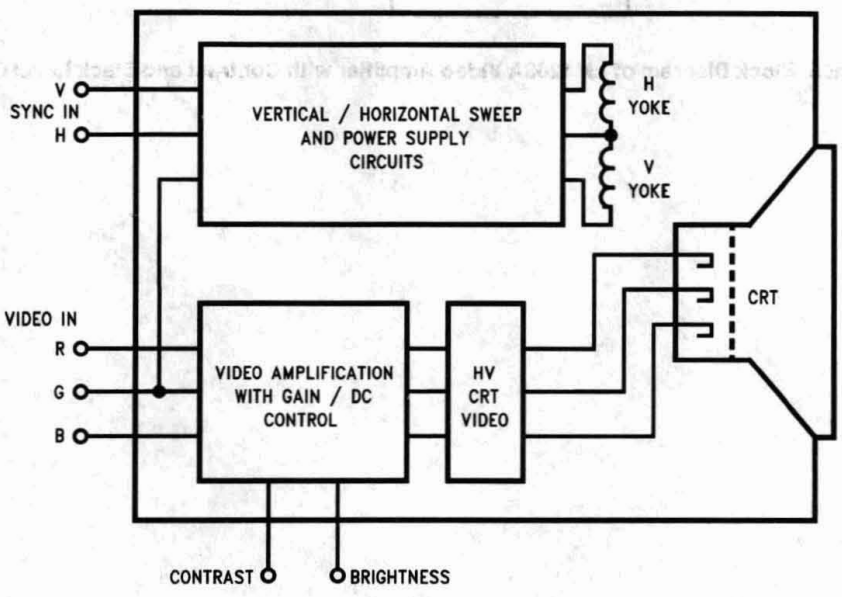

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FIGURE 4. Typical RGB Color Monitor Block Diagram

Circuit Description (Continued)

For individual gain adjustment of each video channel, a 51Ω resistor in series with a 100Ω potentiometer should be used with the red and green channel drive pins. A 91Ω resistor used with the blue channel drive pin sets the blue channel amplifier gain at approximately 6.2. The 100Ω potentiometer at the red and green channel drive pins allow a gain of 6.2 with ±25% gain adjustment. The video signal at the collector of Q12 is buffered and level shifted down by Q13, Q14 and Q15 to the base of the output emitter follower Q16. A 50Ω decoupling resistor is included in series with the emitter of Q16 and the video output pin so as to prevent oscillations when driving capacitive loads. An external resistor should be connected between the video output pin and ground. The value of this resistor should not be less than 390Ω or else package power limitations may be exceeded under worst case conditions (high supply voltage, maximum current, maximum temperature). The collector current from the video output transistor of each video channel is returned to the power supply at V_{CC2}, pin 23. When making power dissipation calculations note that the data sheet specifies only the V_{CC1} and V_{CC2} supply current at 12V supply voltage with no pull down resistor at the output (i.e., $R_L = \infty$, see test circuit *Figure 2*). The IC power dissipation due to V_{CC2} is dependant upon the external video output pull down resistor.

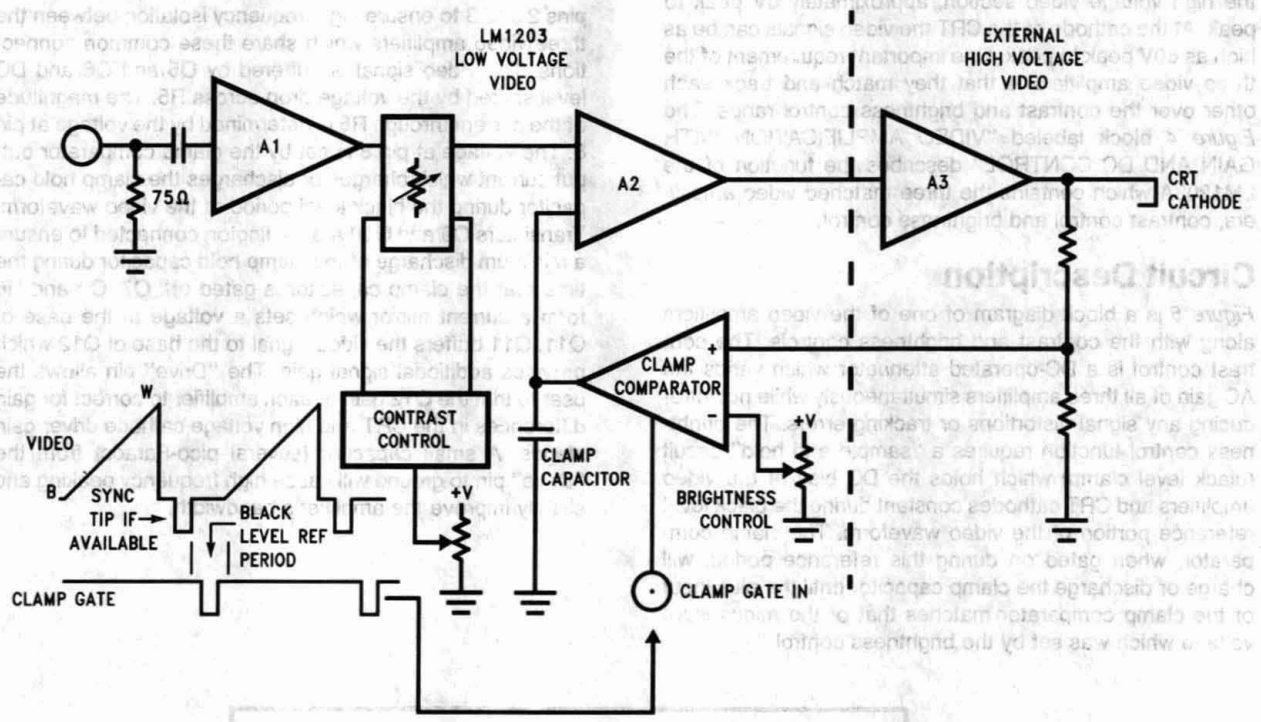

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FIGURE 5. Block Diagram of LM1203A Video Amplifier with Contrast and Black Level Control

Circuit Description (Continued)

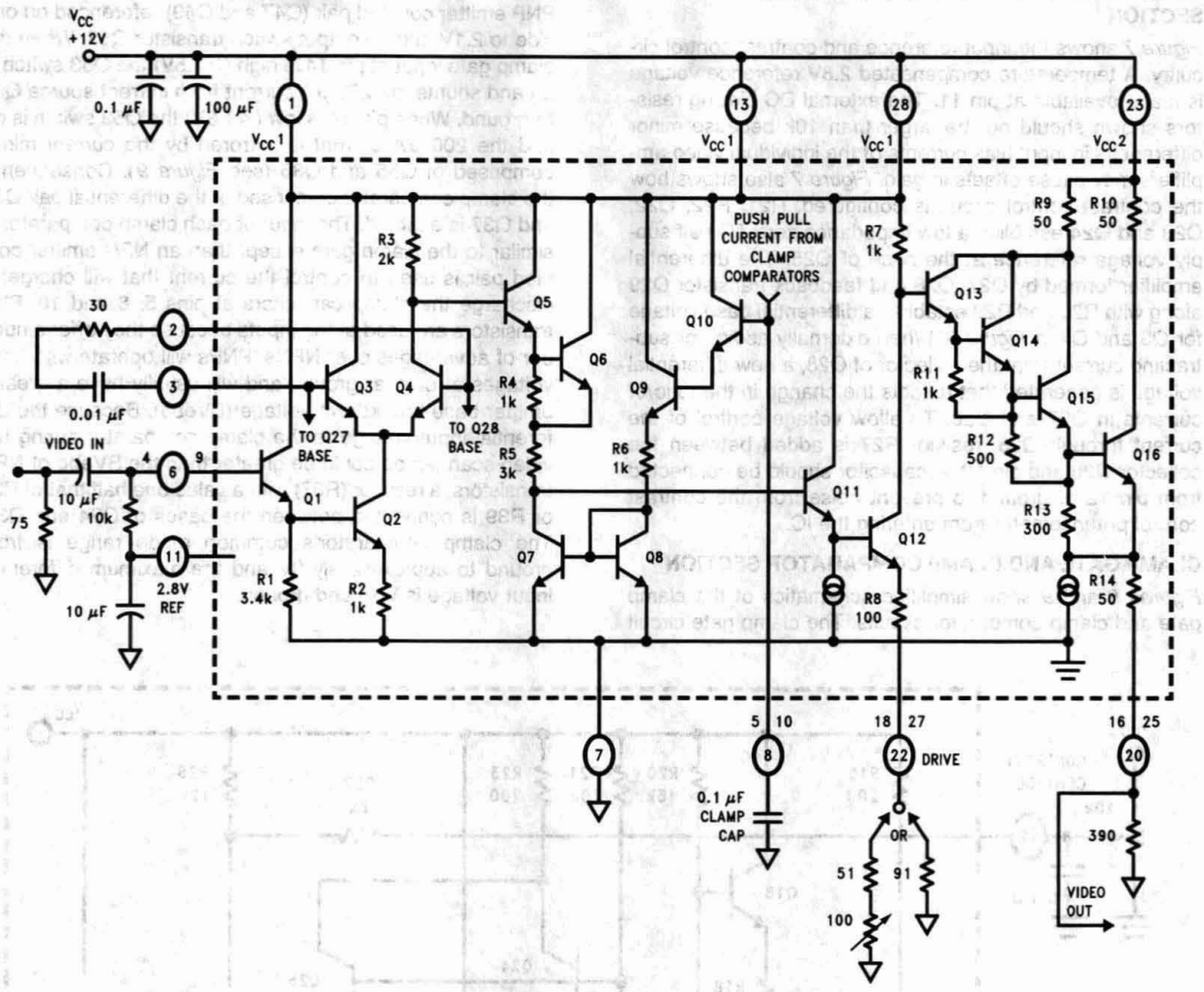

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FIGURE 6. Simplified Schematic of LM1203A Video Amplifier Section with Recommended External Components

Circuit Description (Continued)

INPUT REFERENCE AND CONTRAST CONTROL SECTION

Figure 7 shows the input reference and contrast control circuitry. A temperature compensated 2.8V reference voltage is made available at pin 11. The external DC biasing resistors shown should not be larger than 10k because minor differences in input bias currents of the individual video amplifiers may cause offsets in gain. *Figure 7* also shows how the contrast control circuit is configured. R21, R22, Q22, Q23 and Q24 establish a low impedance zero TC half supply voltage reference at the base of Q25. The differential amplifier formed by Q27, Q28 and feedback transistor Q29 along with R28 and R29 establish a differential base voltage for Q3 and Q4 in *Figure 6*. When externally adding or subtracting current from the collector of Q28, a new differential voltage is generated that reflects the change in the ratio of currents in Q27 and Q28. To allow voltage control of the current through Q28, resistor R27 is added between the collector Q28 and pin 12. A capacitor should be connected from pin 12 to ground to prevent noise from the contrast control potentiometer from entering the IC.

CLAMP GATE AND CLAMP COMPARATOR SECTION

Figures 8 and *9* show simplified schematics of the clamp gate and clamp comparator circuits. The clamp gate circuit *(Figure 8)* consists of a PNP input buffer transistor (Q46), a PNP emitter coupled pair (Q47 and Q49) referenced on one side to 2.1V and an output switch transistor Q53. When the clamp gate input at pin 14 is high (>1.5V) the Q53 switch is on and shunts the 200 μA current from current source Q54 to ground. When pin 14 is low (<1.3V) the Q53 switch is off and the 200 μA current is mirrored by the current mirror comprised of Q55 and Q36 (see *Figure 9*). Consequently the clamp comparator comprised of the differential pair Q35 and Q37 is enabled. The input of each clamp comparator is similar to the clamp gate except than an NPN emitter coupled pair is used to control the current that will charge or discharge the clamp capacitors at pins 5, 8 and 10. PNP transistors are used at the inputs because they offer a number of advantages over NPNs. PNPs will operate with base voltages at or near ground and will usually have a greater emitter base breakdown voltage (BVebo). Because the differential input voltage to the clamp comparator during the video scan period could be greater than the BVebo of NPN transistors, a resistor (R37) with a value one half that of R36 or R39 is connected between the bases of Q34 and Q38. The clamp comparator's common mode range is from ground to approximately 9V and the maximum differential input voltage is V_{CC} and ground.

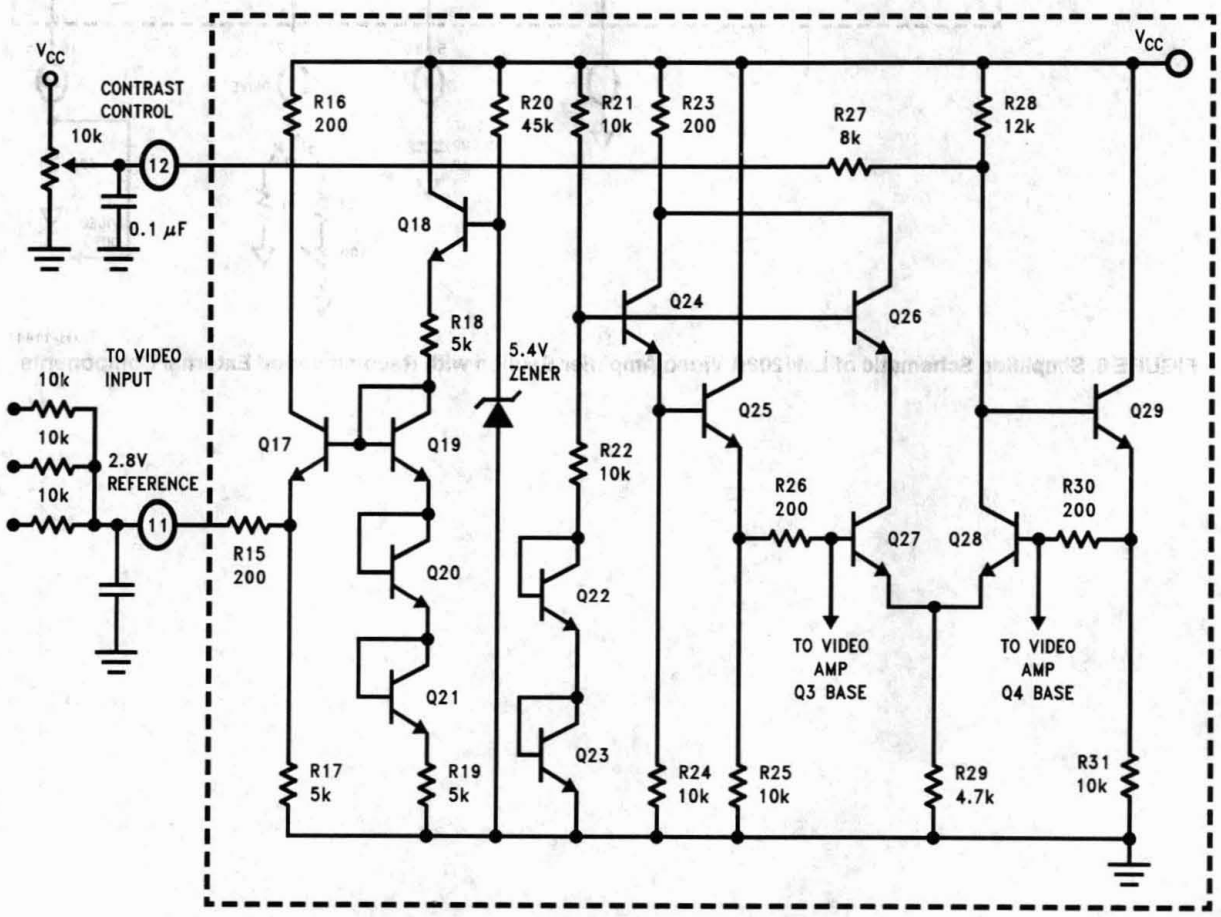

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FIGURE 7. Simplified Schematic of LM1203A Video Input Reference and Contrast Control Circuits

Circuit Description (Continued)

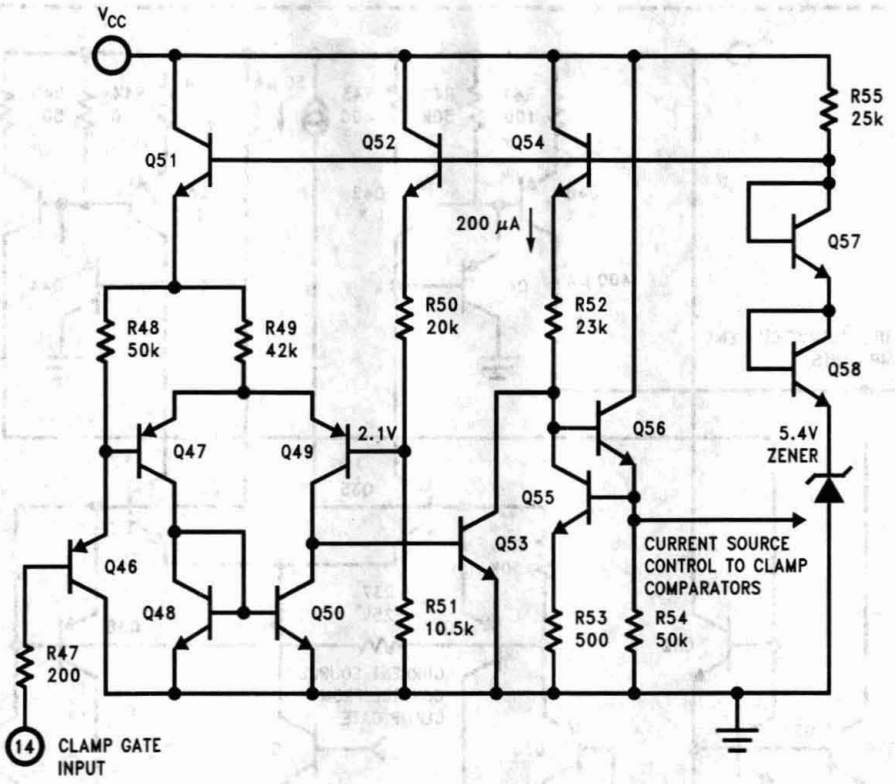

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FIGURE 8. Simplified Schematic of LM1203A Clamp Gate Circuit

Circuit Description (Continued)

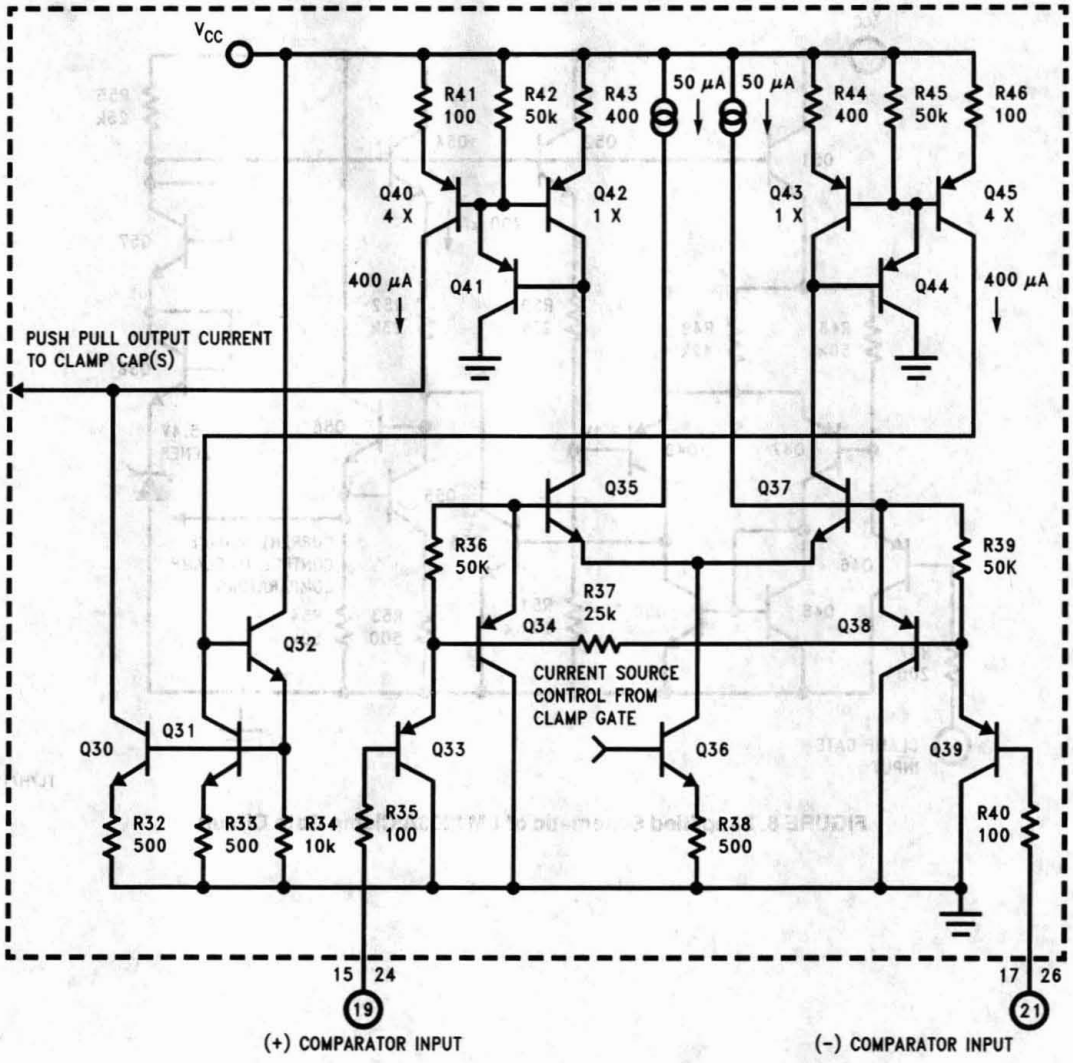

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FIGURE 9. Simplified Schematic of LM1203A Clamp Comparator Circuits

Additional Applications of the LM1203A

Figure 10 shows the configuration for a three channel high frequency amplifier with non gated DC feedback. Pin 14 is tied low to turn on the clamp comparators (feedback amplifiers). The inverting inputs (Pins 17, 21, 26) are connected to the amplifier outputs from a low pass filter. Additional low frequency filtering is provided by the clamp caps. The drive resistors can be made variable or fixed at values between 0Ω and 300Ω. Maximum output swings are achieved when the DC output is set to approximately 4V. The high frequency response will be dependent upon external peaking at the drive pins.

Figure 11 shows a complete RGB video preamplifier circuit using the LM1203A. A quad Exclusive-OR gate (MM74HC86) is used to generate the back porch clamp signal from the composite sync input signal. The composite H Sync input signal may have either polarity. The back porch clamp signal applied to LM1203A's pin 14 allows clamping the video output signals to the black reference level, thereby providing DC restoration. The back porch clamp pulse width is determined by the time constant due to the product of R11 and C15. For fast horizontal scan rates, the back porch clamp pulse width can be made narrower by decreasing the value of R11 or C15 or both. Note that an MM74C86 Exclusive-OR gate may also be used, however, the pin out is different than that of the MM74HC86.

For optimum performance and maximum bandwidth, high speed buffer transistors (Q1, Q2 and Q3 in *Figure 11*) are recommended. The 2N5770 NPN transistors maintain high speed at high currents when driving the inputs of high voltage CRT drivers.

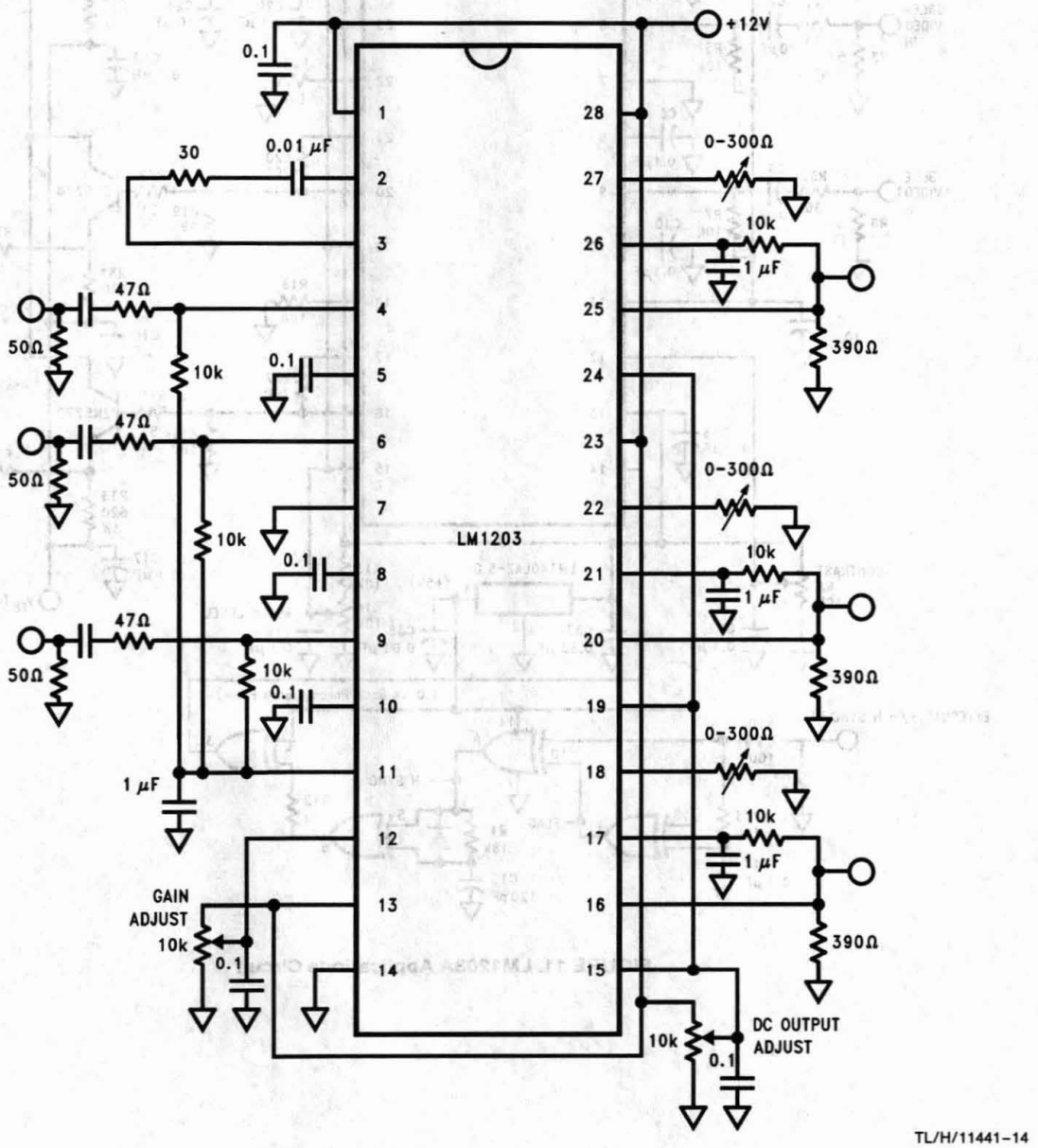

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FIGURE 10. Three Channel High Frequency Amplifier with Non-gated DC Feedback (Non-video Application)

Additional Applications of the LM1203A (Continued)

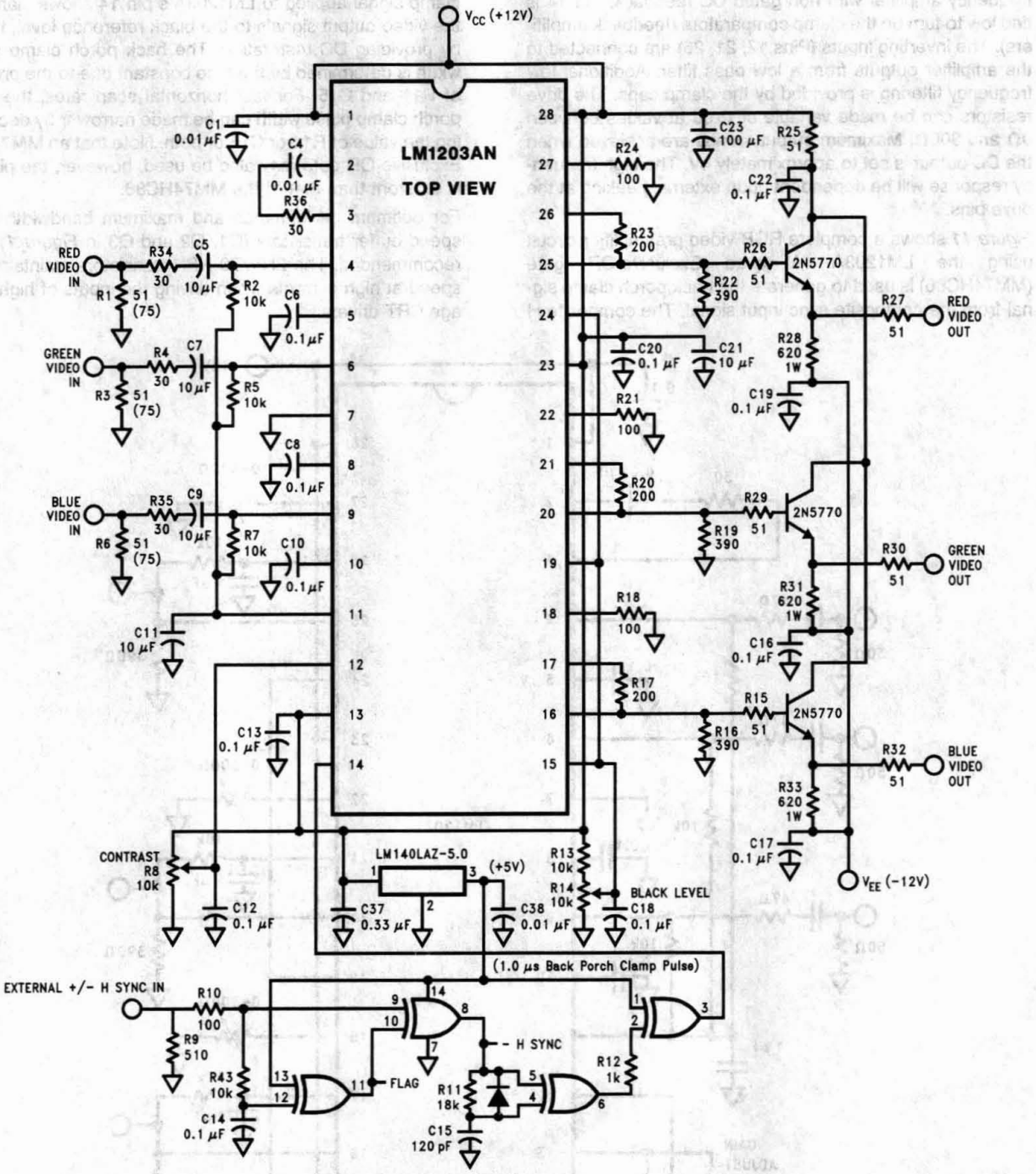

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FIGURE 11. LM1203A Applications Circuit

LM1203A vs LM1203

LM1203A is an improved version of the LM1203 RGB video amplifier system and is pin and function compatible with the LM1203. LM1203A's output voltage can swing as low as 0.15V as opposed to 0.9V for the LM1203. This eliminates the need for a level shift stage between the preamplifier and the CRT driver in most applications.

The LM1203A also offers faster rise and fall times of 4 ns vs 7 ns for the LM1203 and 100 MHz bandwidth vs 70 MHz for LM1203. With a peaking capacitor across the drive resistor, LM1203A's bandwidth can be extended to 150 MHz. Because of LM1203A's wide bandwidth, the device may oscillate if plugged directly into an existing LM1203 board. For optimum performance and stable operation, a double sided printed circuit board with adequate ground plane and power supply decoupling as close to the V_{CC} pins as possible is recommended. *Figure 12* shows the layout of the PC board for *Figure 11's* circuit. For suggestions on optimum PC board layout, please see the reference section below.

The LM1203A also includes a built-in power down spot killer to prevent a flash on the screen upon power down. In some preamplifiers, the video output signal may go high as the device is being powered down. This may cause a whiter than white level at the output of the CRT driver, thus causing a flash on the screen.

REFERENCE

Ott, Henry W. *Noise Reduction Techniques in Electronic Systems,* John Wiley & Sons, New York, 1976.

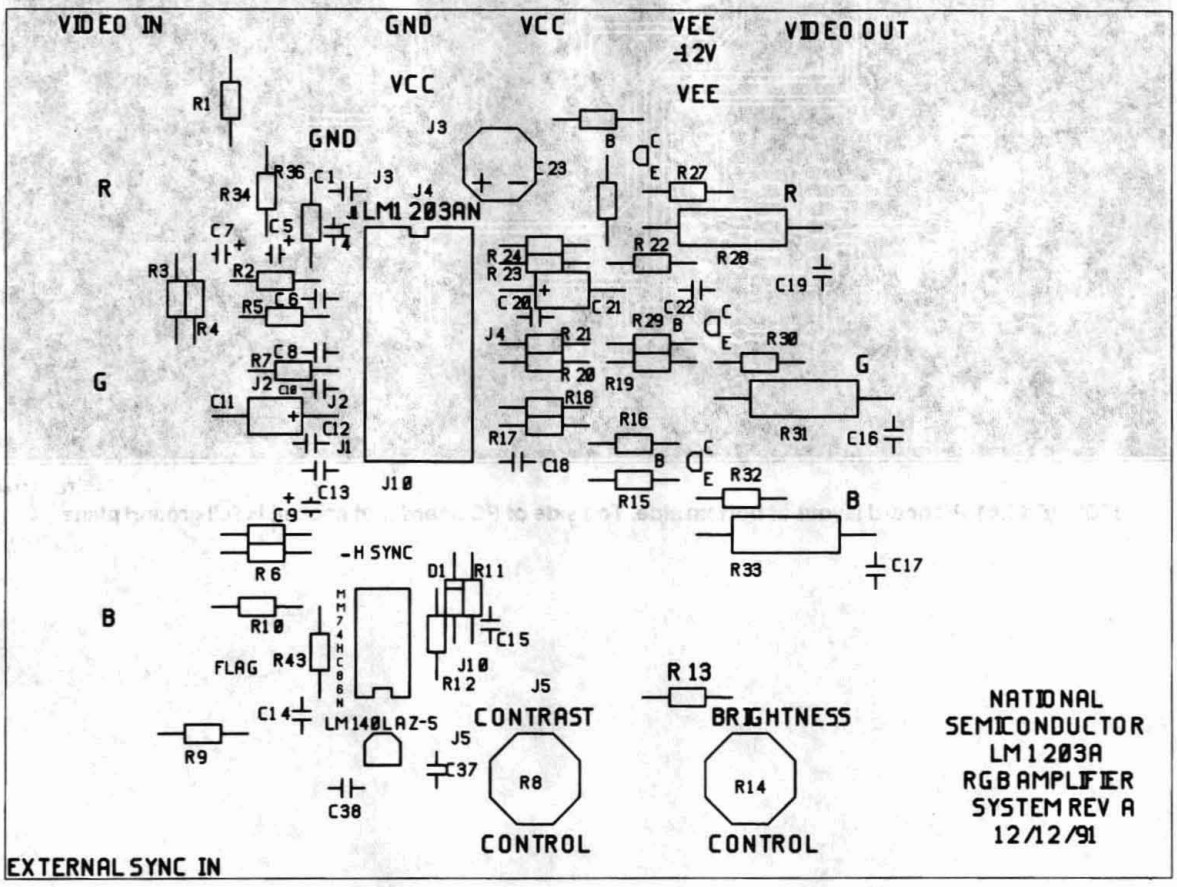

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FIGURE 12(a). PC Board Silk Screen

Additional Applications of the LM1203A (Continued)

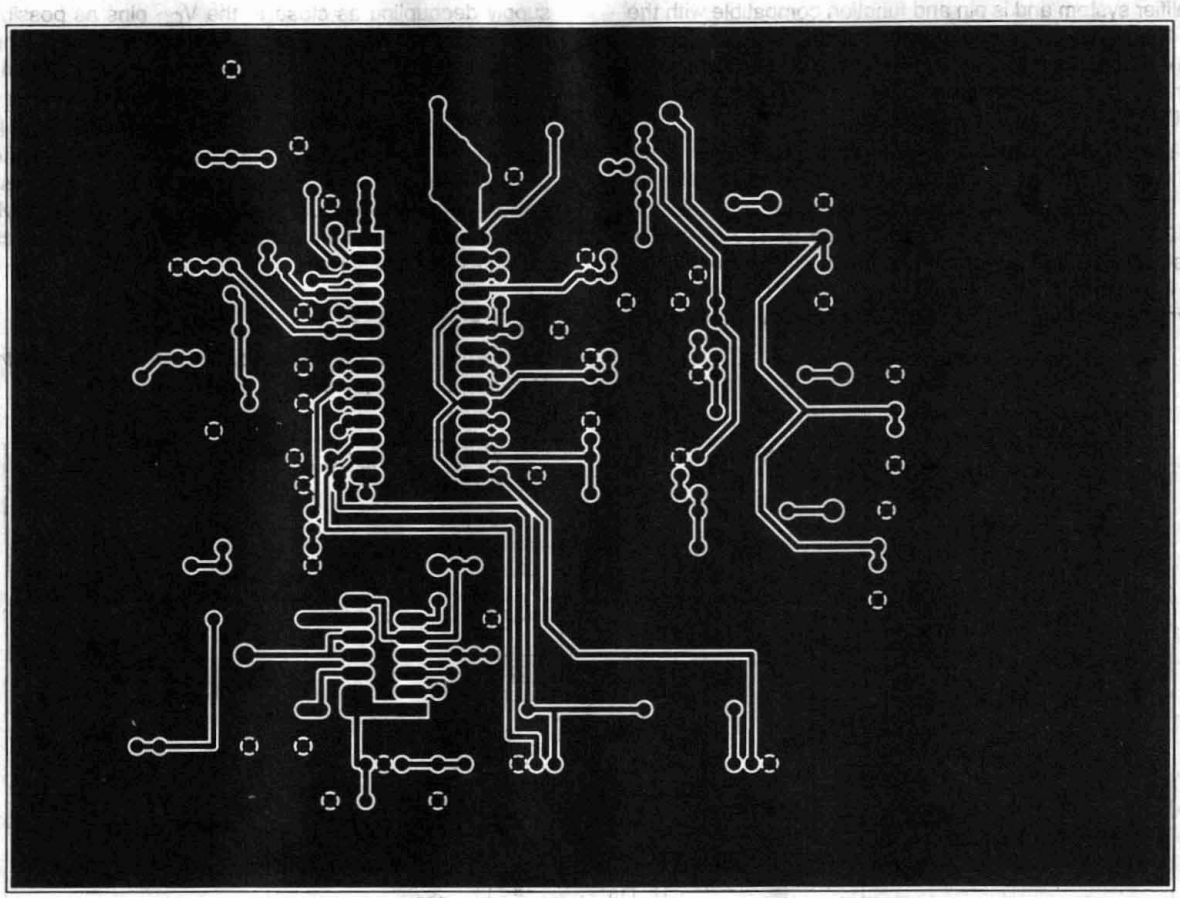

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FIGURE 12(b). PC board layout of bottom side. Top side of PC board (not shown) is full ground plane.

National Semiconductor

LM1203B
100 MHz RGB Video Amplifier System

General Description

The LM1203B is an improved version of the popular LM1203 wideband video amplifier system. The device is intended for high resolution RGB CRT monitors. In addition to three matched video amplifiers, the LM1203B contains three gated differential input black level clamp comparators for brightness control and three matched attenuator circuits for contrast control. Each video amplifier contains a gain set or "Drive" node for setting maximum system gain or providing gain trim capability for white balance. The LM1203B also contains a voltage reference for the video inputs. The LM1203B is pin and function compatible with the LM1203.

Features

- Three wideband video amplifiers (100 MHz @ −3 dB)
- Matched (±0.1 dB or 1.2%) attenuators for contrast control
- Three externally gated comparators for brightness control
- Provisions for individual gain control (Drive) of each video amplifier
- Video input voltage reference
- Low impedance output driver
- Stable on a single sided board

Applications

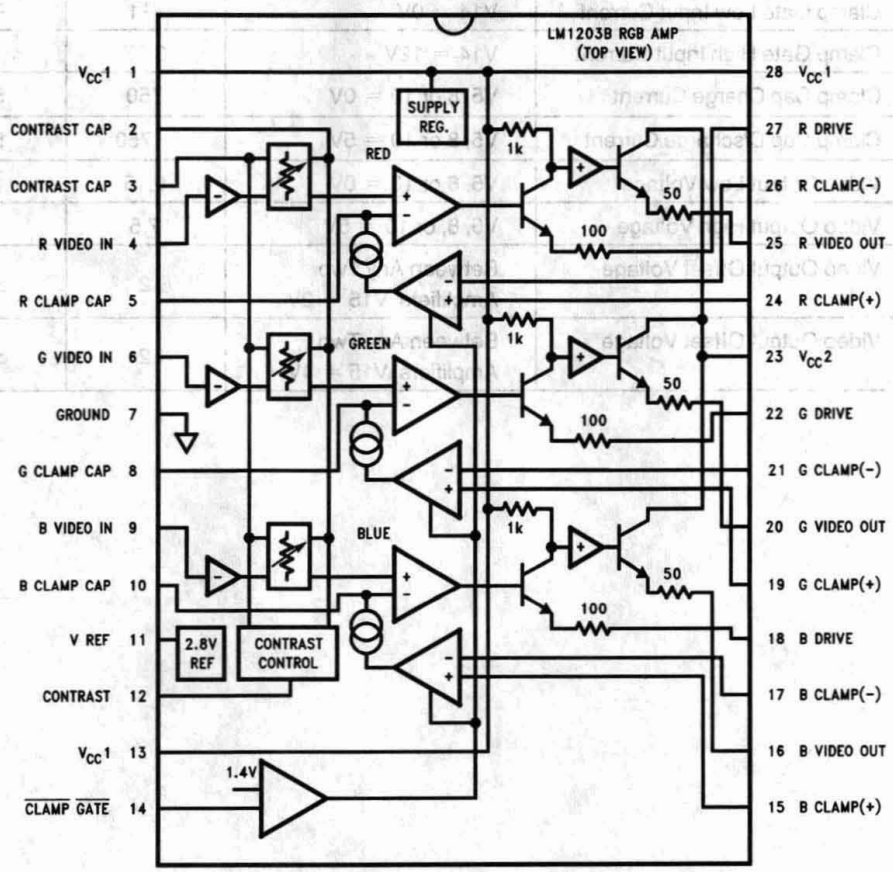
- High resolution RGB CRT monitors
- Video AGC amplifiers
- Wideband amplifiers with gain and DC offset controls

Improvements over LM1203

- 100 MHz vs 70 MHz bandwidth
- V_{OUT} low: 0.15V vs 0.9V
- t_r, t_f: 3.7 ns vs 5 ns
- Built in power down spot killer

Block and Connection Diagrams

28-Lead Molded DIP



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Order Number LM1203BN
See NS Package Number N28B

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC}) Pins 1, 13, 23, 28 (Note 3)	13.5V
Peak Video Output Source Current (Any 1A) Pins 15, 20, or 25	28 mA
Voltage at Any Input Pin (V_{IN})	$V_{CC} \geq V_{IN} \geq GND$
Power Dissipation (P_D) (Above 25°C Derate Based on θ_{JA} and T_J)	2.5W
Thermal Resistance (θ_{JA})	50°C/W
Junction Temperature (T_J)	150°C
ESD Susceptibility (Note 4)	2.0 kV
Storage Temperature	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	265°C

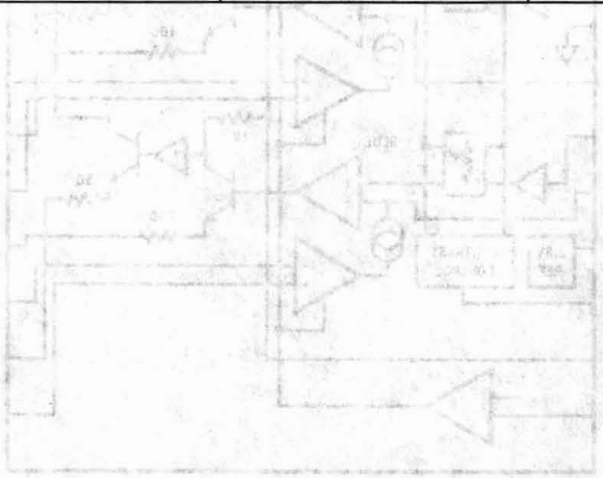
Operating Ratings (Note 2)

Temperature Range	−20°C to +80°C
Supply Voltage (V_{CC})	$10.8V \leq V_{CC} \leq 13.2V$

DC Electrical Characteristics

See Test Circuit *(Figure 2)*, $T_A = 25°C$; $V_{CC1} = V_{CC2} = 12V$. S17, 21, 26 Open; V12 = 6V; V14 = 0V; V15 = 2.0V unless otherwise stated.

Symbol	Parameter	Conditions	Typical (Note 5)	Limit (Note 6)	Units
I_S	Supply Current	$V_{CC1} + V_{CC2}$, $R_L = \infty$ (Note 7)	70	95	mA(max)
V11	Video Input Reference Voltage		2.8	2.5	V(min)
				3.1	V(max)
I_b	Video Input Bias Current	Any One Amplifier	7	20	μA(max)
V_{14l}	Clamp Gate Low Input Voltage	Clamp Comparators On	1.2	0.8	V(max)
V_{14h}	Clamp Gate High Input Voltage	Clamp Comparators Off	1.6	2.0	V(min)
I_{14l}	Clamp Gate Low Input Current	V14 = 0V	−1	−5.0	μA(max)
I_{14h}	Clamp Gate High Input Current	V14 = 12V	0.07	0.2	μA(max)
I_{clamp+}	Clamp Cap Charge Current	V5, 8 or 10 = 0V	750	500	μA(min)
I_{clamp-}	Clamp Cap Discharge Current	V5, 8 or 10 = 5V	−750	500	μA(min)
V_{OL}	Video Output Low Voltage	V5, 8 or 10 = 0V	0.15	0.5	V(max)
V_{OH}	Video Output High Voltage	V5, 8, or 10 = 5V	7.5	7	V(min)
$\Delta V_{O(2V)}$	Video Output Offset Voltage	Between Any Two Amplifiers, V15 = 2V	2	±25	mV(max)
$\Delta V_{O(4V)}$	Video Output Offset Voltage	Between Any Two Amplifiers, V15 = 4V	2	±25	mV(max)



AC Electrical Characteristics

See Test Circuit *(Figure 2)*, T_A = 25°C, V_{CC1} = V_{CC2} = 12V. S17, 21, 26 Closed; V14 = 0V; V15 = 4V unless otherwise stated.

Symbol	Parameter	Conditions	Typical (Note 5)	Limit (Note 6)	Units
$A_{V\ max}$	Video Amplifier Gain	V12 = 12V, V_{IN} = 560 mV_{PP}	6.5	4.5	V/V(min)
$\Delta V_{V\ 5V}$	Attenuation @ 5V	Ref: $A_{V\ max}$, V12 = 5V	−8		dB
$\Delta A_{V\ 2V}$	Attenuation @ 2V	Ref: $A_{V\ max}$, V12 = 2V	−30		dB
$A_{V\ match}$	Absolute Gain Match @ A_V max	V12 = 12V (Note 8)	±0.3		dB
$\Delta A_{V\ track\ 1}$	Gain Change between Amplifiers	V12 = 5V (Notes 8, 9)	±0.1		dB
$\Delta A_{V\ track\ 2}$	Gain Change between Amplifiers	V12 = 2V (Notes 8, 9)	±0.3		dB
THD	Video Amplifier Distortion	V12 = 3V, V_O = 1 V_{PP}	1		%
f (−3 dB)	Video Amplifier Bandwidth (Notes 10, 11)	V12 = 12V, V_O = 4 V_{PP} (With 36 pF Peaking Cap from Pins 18, 22 and 27 to GND)	100		MHz
f (−3 dB)	Video Amplifier Bandwidth (Notes 10, 11)	V12 = 12V, V_O = 4 V_{PP} (No External Peaking Cap)	60		MHz
t_r/t_f	Output Rise/Fall Time (Note 10)	V_O = 4 V_{PP} (With 36 pF Peaking Cap from Pins 18, 22 and 27 to GND)	3.7		ns
t_r	Output Rise Time (Note 10)	V_O = 4 V_{PP} (No External Peaking Capacitor)	5.5		ns
t_f	Output Fall Time (Note 10)	V_O = 4 V_{PP} (No External Peaking Capacitor)	6.0		ns
$V_{sep\ 10\ kHz}$	Video Amplifier 10 kHz Isolation	V12 = 12V (Note 12)	−70		dB
$V_{sep\ 10\ MHz}$	Video Amplifier 10 MHz Isolation	V12 = 12V (Notes 10, 12)	−50		dB

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur.

Note 2: Operating Ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.

Note 3: V_{CC} supply pins 1, 13, 23, 28 must be externally wired together to prevent internal damage during V_{CC} power on/off cycles.

Note 4: Human body model, 100 pF discharged through a 1.5 kΩ resistor.

Note 5: Typical specifications are specified at +25°C and represent the most likely parametric norm.

Note 6: Tested limits are guaranteed to National's AOQL (Average Outgoing Quality Level).

Note 7: The supply current specified is the quiescent current for V_{CC1} and V_{CC2} with R_L = ∞, see *Figure 2*'s test circuit. The supply current for V_{CC2} (pin 23) also depends on the output load. With video output at 2V DC, the additional current through V_{CC2} is 18 mA for *Figure 2*'s test circuit.

Note 8: Measure gain difference between any two amplifiers. V_{IN} = 1 V_{PP}.

Note 9: ΔA_V track is a measure of the ability of any two amplifiers to track each other and quantifies the matching of the three attenuators. It is the difference in gain change between any two amplifiers with the contrast voltage (V12) at either 5V or 2V measured relative to an A_V max condition, V12 = 12V. For example, at A_V max the three amplifiers' gains might be 17.4 dB, 16.9 dB and 16.4 dB and change to 7.3 dB, 6.9 dB and 6.5 dB respectively for V12 = 5V. This yields the measured typical ±0.1 dB channel tracking.

Note 10: When measuring video amplifier bandwidth or pulse rise and fall times, a single sided with ground plane printed circuit board without socket is recommended. Video amplifier 10 MHz isolation test also requires this printed circuit board.

Note 11: Adjust input frequency from 10 kHz (A_V max reference level) to the −3 dB corner frequency ($f_{-3\ dB}$).

Note 12: Measure output levels of the other two undriven amplifiers relative to the driven amplifier to determine channel separation. Terminate the undriven amplifier inputs to simulate generator loading. Repeat test at f_{IN} = 10 MHz for V_{sep} = 10 MHz.

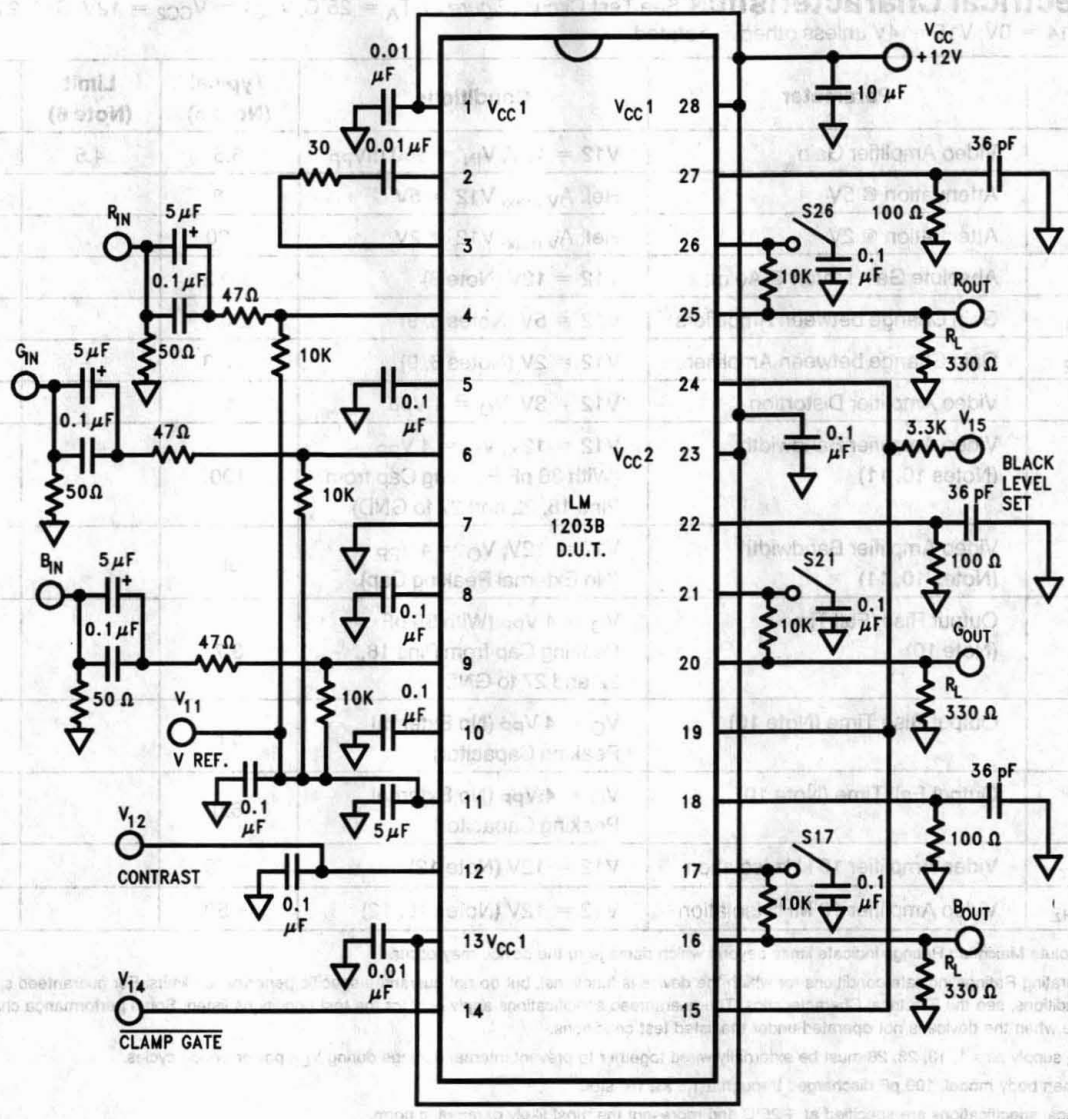


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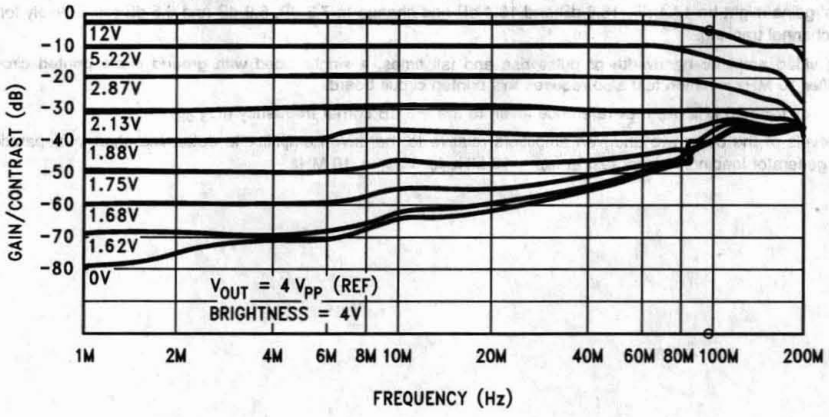
FIGURE 2. LM1203B Test Circuit

Typical Performance Characteristics V_{CC} = 12V, T_A = 25°C unless otherwise specified

Contrast vs Frequency



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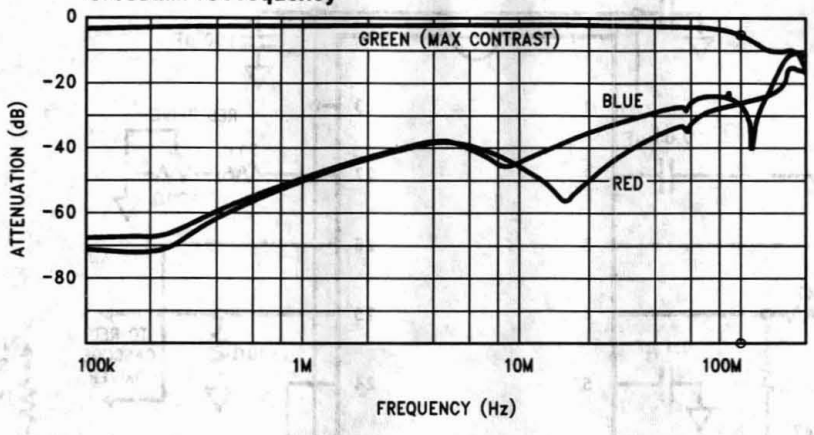
Typical Performance Characteristics V_{CC} = 12V, T_A = 25°C unless otherwise specified (Continued)

Crosstalk vs Frequency



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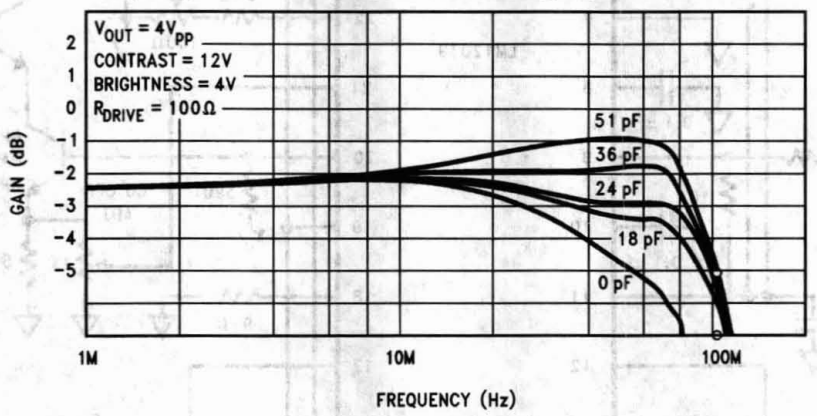
Frequency Response Using Various Peaking Caps



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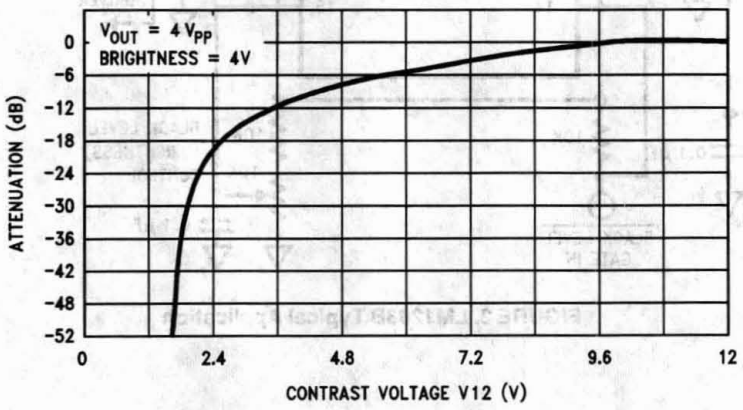
Attenuation vs Contrast Voltage



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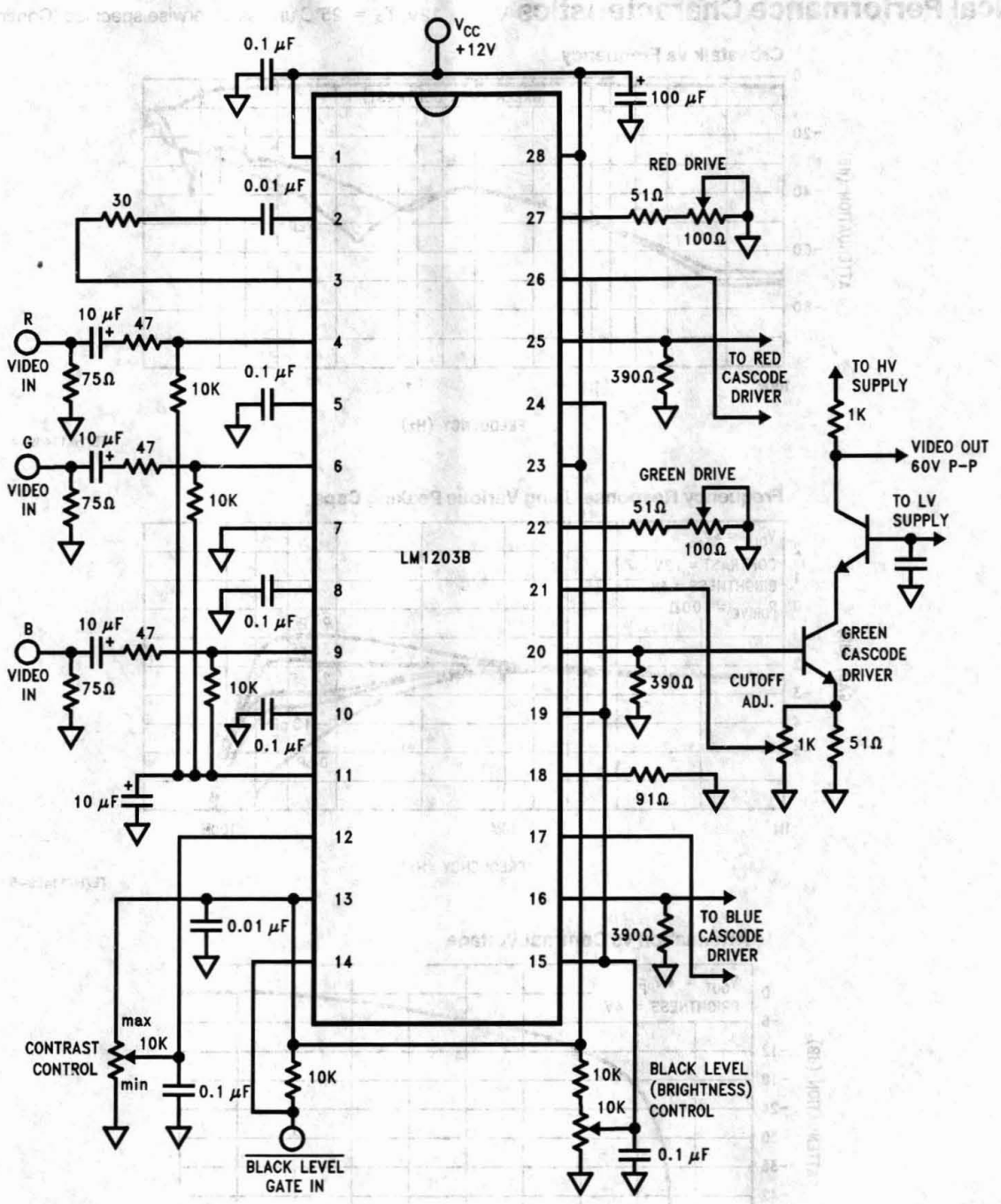

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FIGURE 3. LM1203B Typical Application

Applications Information

Figure 4 shows the block diagram of a typical analog RGB color monitor. The RGB monitor is used with CAD/CAM work stations, PC's, arcade games and in a wide range of other applications that benefit from the use of color display terminals. The RGB color monitor characteristics may differ in such ways as sweep rates, screen size, CRT color trio spacing (dot pitch), or in video amplifier bandwidths but will still be generally configured as shown in *Figure 4*. Separate horizontal and vertical sync signals may be required or they may be contained in the green video input signal. The video input signals are usually supplied by coax cable which is terminated in 75Ω at the monitor input and internally AC coupled to the video amplifiers. These input signals are approximately 1V peak to peak in amplitude and at the input of the high voltage video section, approxmiately 5V peak to peak. At the cathode of the CRT the video signals can be as high as 60V peak to peak. One important requirement of the three video amplifiers is that they match and track each other over the contrast and brightness control range. The *Figure 4* block labeled "VIDEO AMPLIFICATION WITH GAIN AND DC CONTROL" describes the function of the LM1203B which contains the three matched video amplifiers, contrast control and brightness control.

Circuit Description

Figure 5 is a block diagram of one of the video amplifiers along with the contrast and brightness controls. The contrast control is a DC-operated attenuator which varies the AC gain of all three amplifiers simultaneously while not introducing any signal distortions or tracking erros. The brightness control function requires a "sample and hold" circuit (black level clamp) which holds the DC bias of the video amplifiers and CRT cathodes constant during the black level reference portion of the video waveform. The clamp comparator, when gated on during this reference period, will charge or discharge the clamp capacitor until the plus input of the clamp comparator matches that of the minus input voltage which was set by the brightness control.

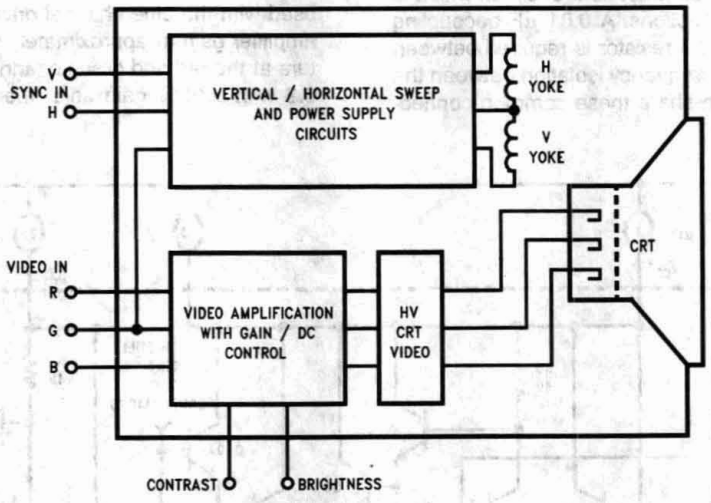

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FIGURE 4. Typical RGB Color Monitor Block Diagram

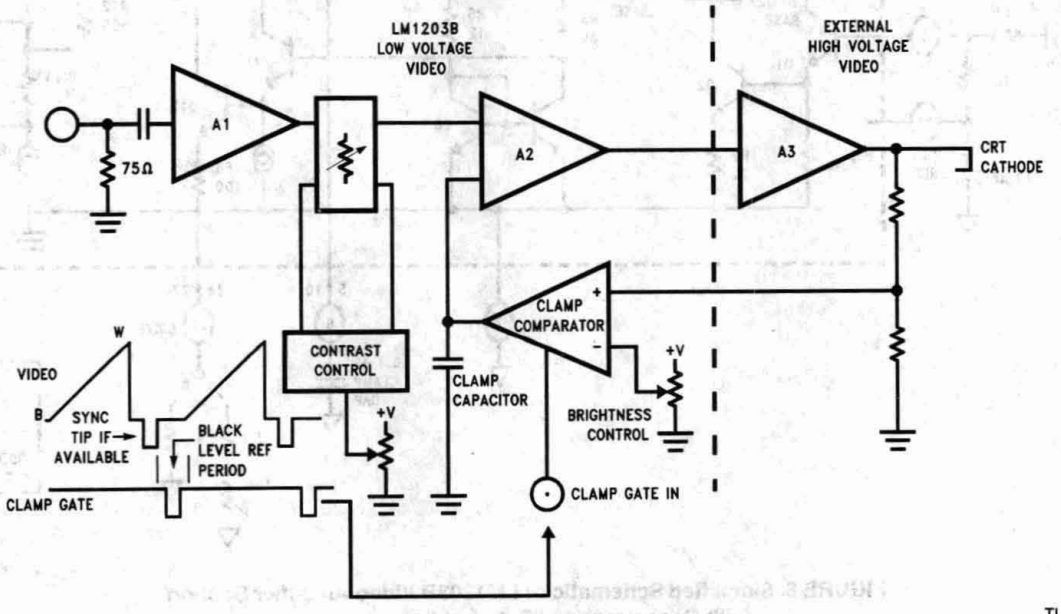

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FIGURE 5. Block Diagram of LM1203B Video Amplifier with Contrast and Black Level Control

Circuit Description (Continued)

VIDEO AMPLIFIER SECTION

Figure 6 is a simplified schematic of one of the three video amplifiers along with the recommended external components. The IC pin numbers are circled and all external components are shown outside the dashed line. The video input is applied to pin 6 via a 10 μF coupling capacitor and a 47Ω resistor. The resistor is added to limit the current through the input pin should the applied voltage rise above V_{CC} or drop below ground. The performance of the LM1203B is not degraded by the 47Ω resistor. However if EMI is a concern, this resistor can be increased to well over 100Ω where the rise and fall times will become longer. DC bias for the video input is through the 10k resistor connected to the 2.8V reference at pin 11. The low frequency roll-off of the amplifier is set by the 10k resistor and the 10 μF capacitor. Transistor Q1 buffers the video signal to the base of Q2. Q2's collector current is then directed to the V_{CC1} supply directly or through the 4k load resistor depending upon the differential DC voltage at the bases of Q3 and Q4. This differential DC voltage is generated by the contrast control circuit which is described in the following sections. A 0.01 μF decoupling capacitor in series with a 30Ω resistor is required between pins 2 and 3 to ensure high frequency isolation between the three video amplifiers which share these common connections. The video signal is buffered by Q5 and Q6 and DC level shifted by the voltage drop across R5. The magnitude of the current through R5 is determined by the voltage at pin 8. The voltage at pin 8 is set by the clamp comparator output current which charges or discharges the clamp hold capacitor during the black level period of the video waveform. Transistors Q9 and Q10 are darlington connected to ensure a minimum discharge of the clamp hold capacitor during the time that the clamp capacitor is gated off. Q7, Q8 and R6 form a current mirror which sets a voltage at the base of Q11. Q11 buffers the video signal to the base of Q12 which provides additional signal gain. The "Drive" pin allows the user to trim the Q12 gain of each amplifier to correct for gain differences in the CRT and high voltage cathode driver gain stages. A small capacitor (several pico-Farads) from the "Drive" pin to ground will cause high frequency peaking and slightly improve the amplifier's bandwidth.

For individual gain adjustment of each video channel, a 51Ω resistor in series with a 100Ω potentiometer should be used with the red and green channel drive pins. A 91Ω resistor used with the blue channel drive pin sets the blue channel amplifier gain at approximately 6.2. The 100Ω potentiometers at the red and green channel drive pins allow a gain of 6.2 with ±25% gain adjustment. The video signal at the

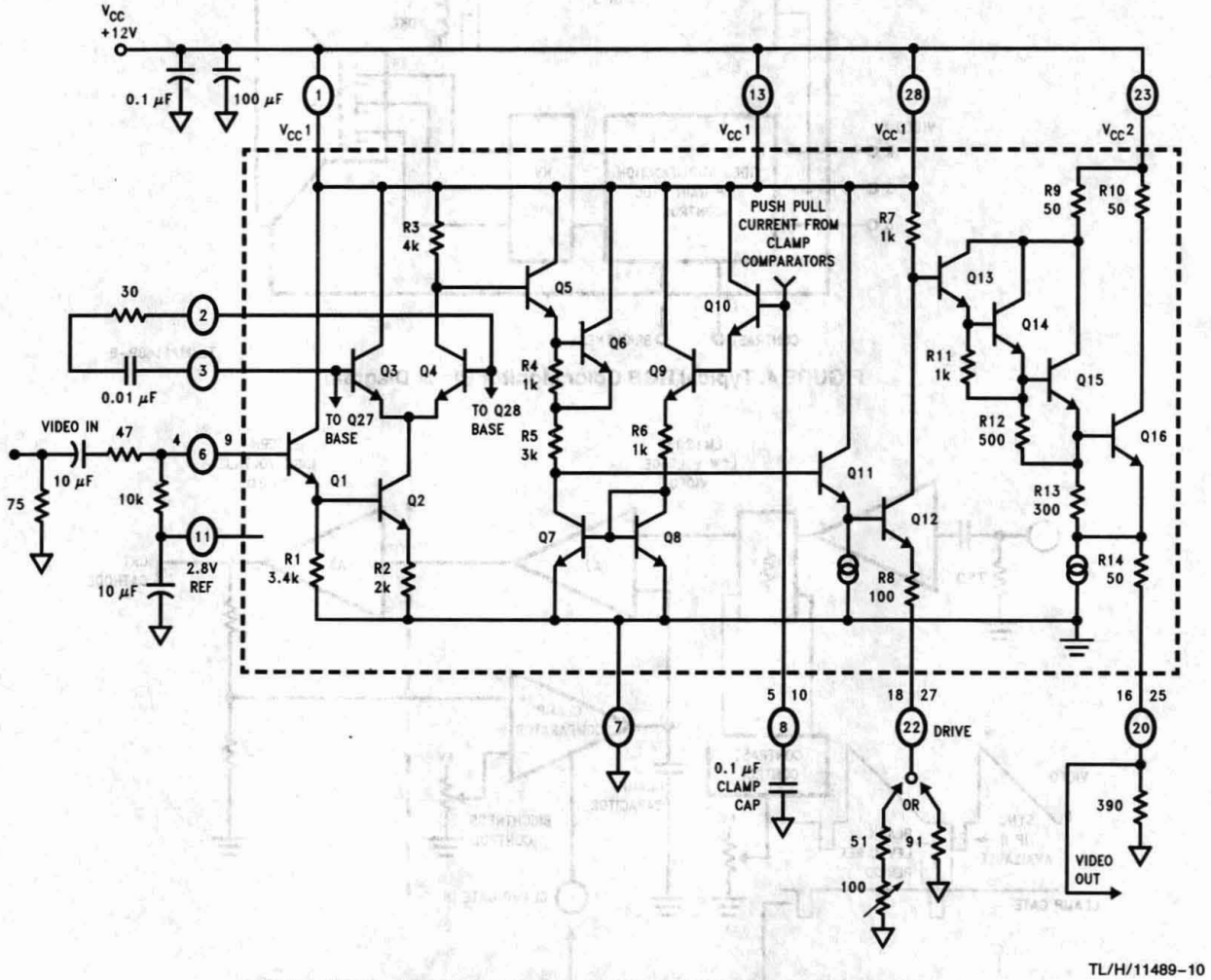

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FIGURE 6. Simplified Schematic of LM1203B Video Amplifier Section with Recommended External Components

Circuit Description (Continued)

collector of Q12 is buffered and level shifted down by Q13, Q14 and Q15 to the base of the output emitter follower Q16. A 50Ω decoupling resistor is included in series with the emitter of Q16 and the video output pin so as to prevent oscillations when driving capacitive loads. An external resistor should be connected between the video output pin and ground. The value of this resistor should not be less than 390Ω or else package power limitations may be exceeded under worse case conditions (high supply voltage, maximum current, maximum temperature). The collector current from the video output transistor of each video channel is returned to the power supply at V_{CC2}, pin 23. When making power dissipation calculations note that the data sheet specifies only the V_{CC1} and V_{CC2} supply current at 12V supply voltage with no pull down resistor at the output (i.e., $R_L = \infty$, see Test Circuit *Figure 2*). The IC power dissipation due to V_{CC2} is dependent upon the external video output pull down resistor.

INPUT REFERENCE AND CONTRAST CONTROL SECTION

Figure 7 shows the input reference and contrast control circuitry. A temperature compensated 2.8V reference voltage is made available at pin 11. The external DC biasing resistors shown should not be larger than 10k because minor differences in input bias currents of the individual video amplifiers may cause offsets in gain. *Figure 7* also shows how the contrast control circuit is configured. R21, R22, Q22, Q23, and Q24 establish a low impedance zero TC half supply voltage reference at the base of Q25. The differential amplifier formed by Q27, Q28 and feedback transistor Q29 along with R28 and R29 establish a differential base voltage for Q3 and Q4 in *Figure 6*. When externally adding or subtracting current from the collector of Q28, a new differential voltage is generated that reflects the change in the ratio of currents in Q27 and Q28. To allow voltage control of the current through Q28, resistor R27 is added between the collector Q28 and pin 12. A capacitor should be connected from pin 12 to ground to prevent noise from the contrast control potentiometer from entering the IC.

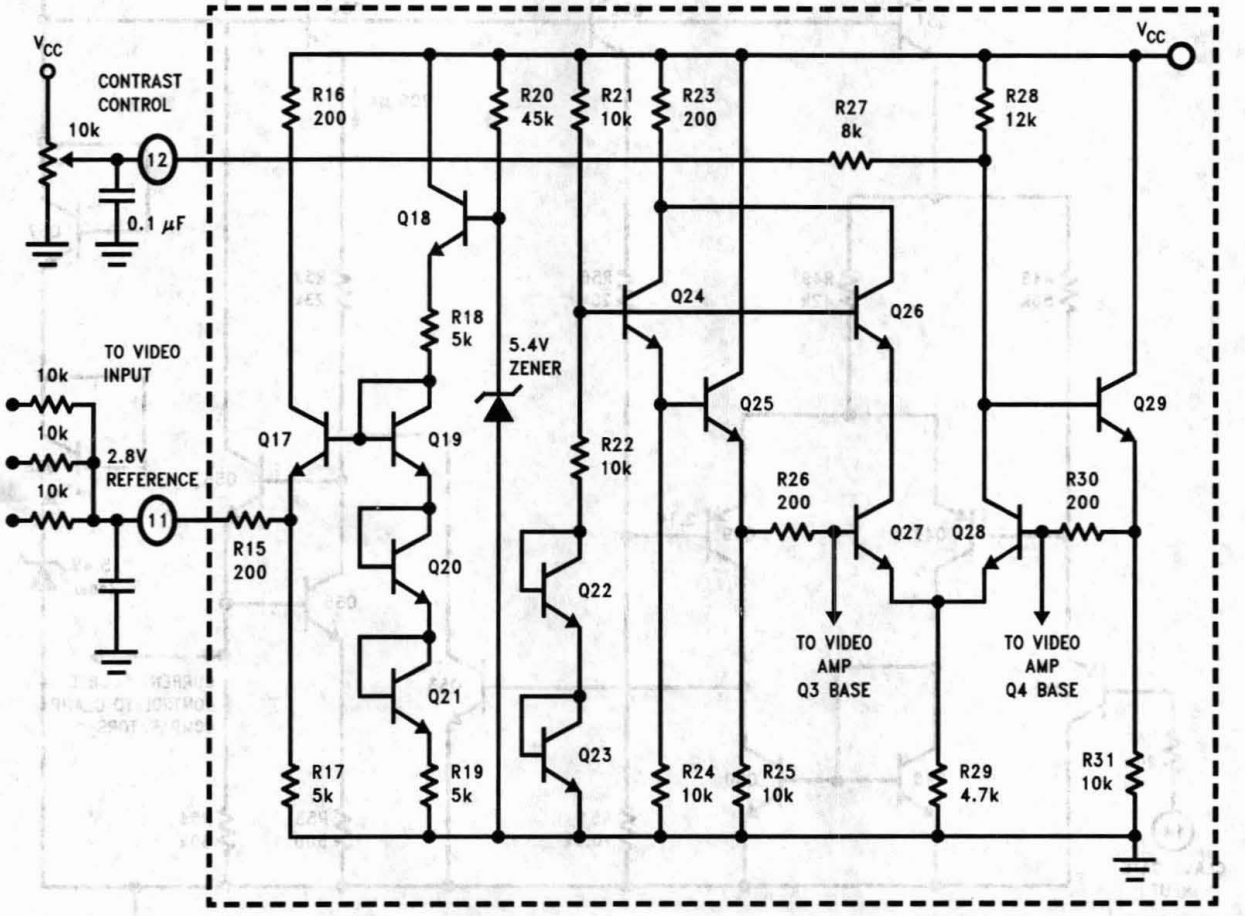

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FIGURE 7. Simplified Schematic of LM1203B Video Input Reference and Contrast Control Circuits

Circuit Description (Continued)

CLAMP GATE AND CLAMP COMPARATOR SECTION

Figures 8 and *9* show simplified schematics of the clamp gate and clamp comparator circuits. The clamp gate circuit *(Figure 8)* consists of a PNP input buffer transistor (Q46), a PNP emitter coupled pair (Q47 and Q49) referenced on one side to 2.1V and an output switch transistor Q53. When the clamp gate input at pin 14 is high (>1.5V) the Q53 switch is on and shunts the 200 μA current from current source Q54 to ground. When pin 14 is low (< 1.3V) the Q53 switch is off and the 200 μA current is mirrored by the current mirror comprised of Q55 and Q36 (see *Figure 9*). Consequently the clamp comparator comprised of the differential pair Q35 and Q37 is enabled. The input of each clamp comparator is similar to the clamp gate except that an NPN emitter coupled pair is used to control the current that will charge or discharge the clamp capacitors at pins 5, 8, and 10. PNP transistors are used at the inputs because they offer a number of advantages over NPNs. PNPs will operate with base voltages at or near ground and will usually have a greater emitter base breakdown voltage (BVebo). Because the differential input voltage to the clamp comparator during the video scan period could be greater than the BVebo of NPN transistors, a resistor (R37) with a value one half that of R36 or R39 is connected between the bases of Q34 and Q38. The clamp comparator's common mode range is from ground to approximately 9V and the maximum differential input voltage is V_{CC} and ground.

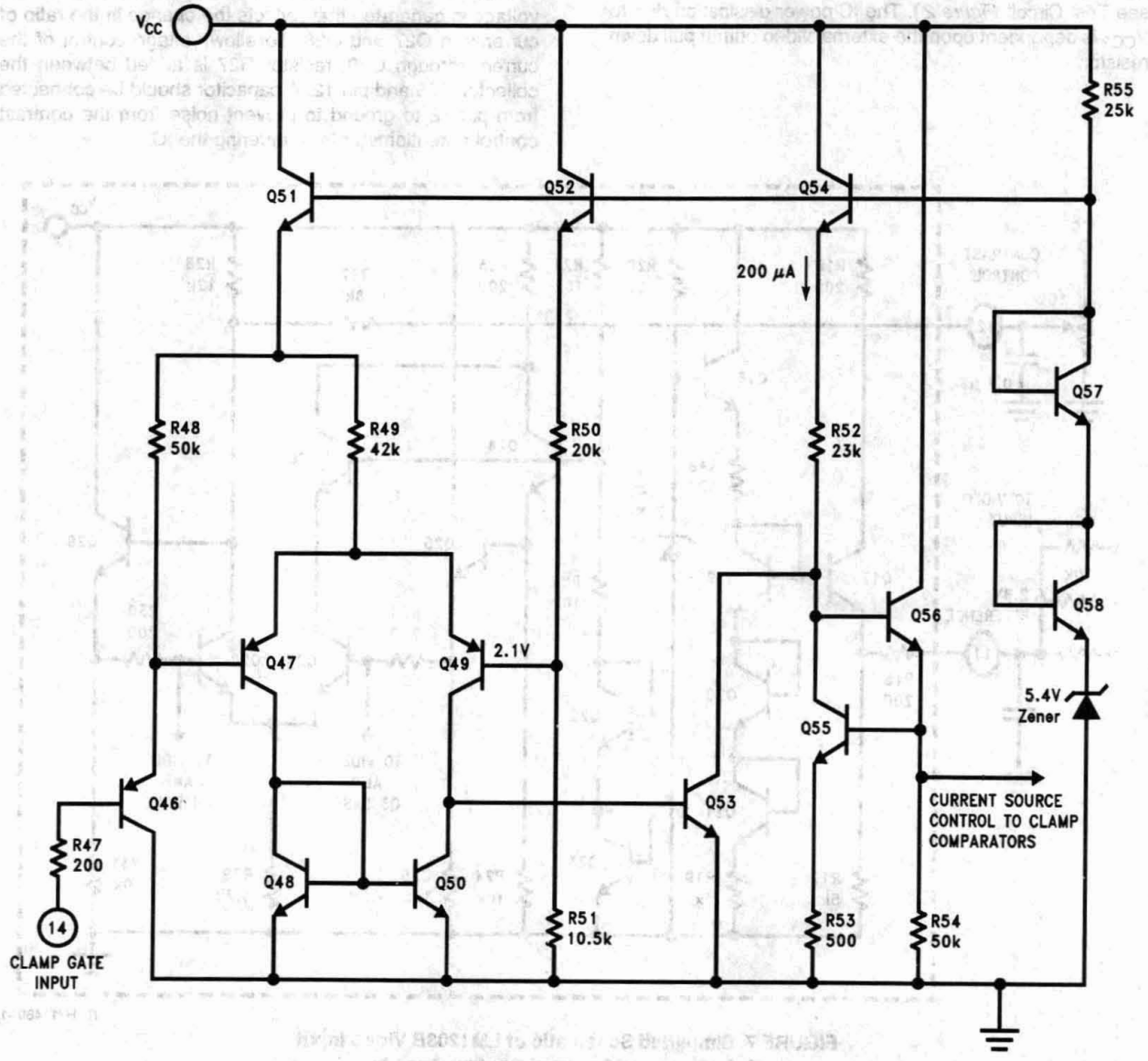

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FIGURE 8. Simplified Schematic of LM1203B Clamp Gate Circuit

Circuit Description (Continued)

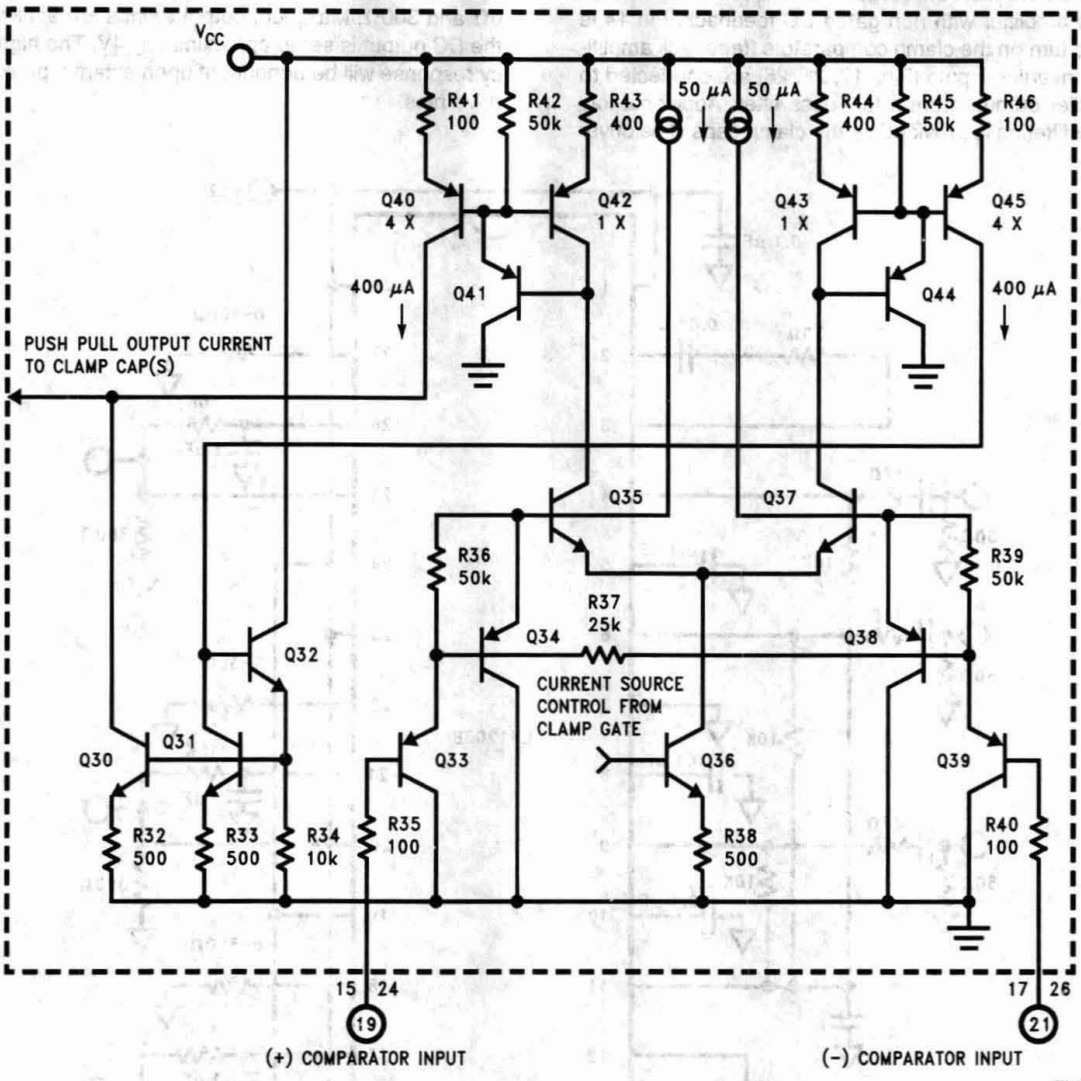

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FIGURE 9. Simplified Schematic of LM1203B Clamp Comparator Circuits

Additional Applications of the LM1203B

Figure 10 shows the configuration for a three channel high frequency amplifier with non gated DC feedback. Pin 14 is tied low to turn on the clamp comparators (feedback amplifiers). The inverting inputs (Pins 17, 21, 26) are connected to the amplifier outputs from a low pass filter. Additional low frequency filtering is provided by the clamp caps. The drive resistors can be made variable or fixed at values between 0Ω and 300Ω. Maximum output swings are achieved when the DC output is set to approximately 4V. The high frequency response will be dependent upon external peaking at the drive pins.

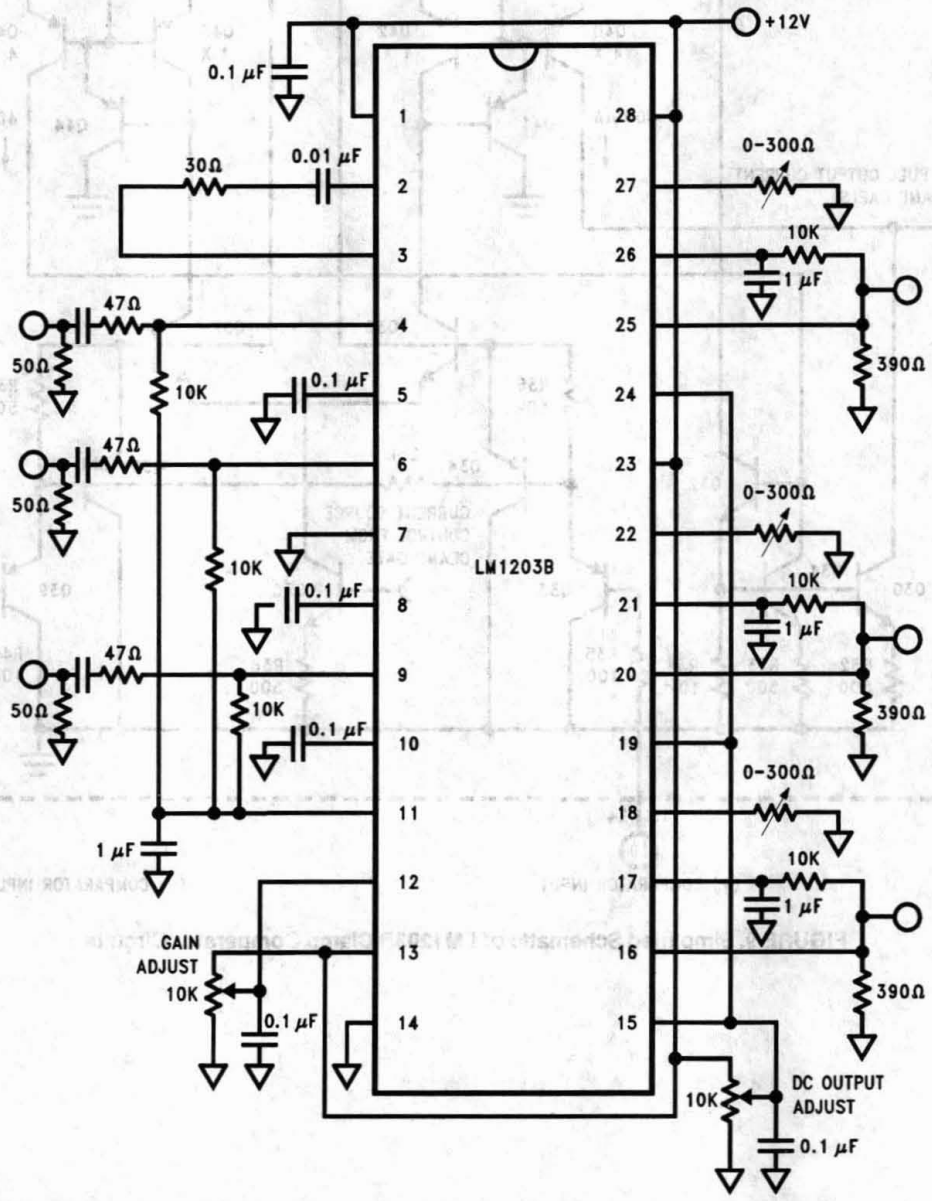

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FIGURE 10. Three Channel High Frequency Amplifier with Non-Gated DC Feedback (Non-Video Applications)

Additional Applications of the LM1203B (Continued)

Figure 11 shows a complete RGB video preamplifier circuit using the LM1203B. A quad Exclusive-OR gate (MM74HC86) is used to generate the back porch clamp signal from the composite sync input signal. The composite H Sync input signal may have either polarity. The back porch clamp signal applied to LM1203B's pin 14 allows clamping the video output signals to the black reference level, thereby providing DC restoration. The back porch clamp pulse width is determined by the time constant due to the product of R11 and C15. For fast horizontal scan rates, the back porch clamp pulse width can be made narrower by decreasing the value of R11 or C15 or both. Note that an MM74C86 Exclusive-Or gate may also be used, however, the pin out is different than that of the MM74HC86.

For optimum performance and maximum bandwidth, high speed buffer transistors (Q1, Q2, and Q3 in *Figure 11*) are recommended. The 2N5770 NPN transistors maintain high speed at high currents when driving the inputs of high voltage CRT drivers.

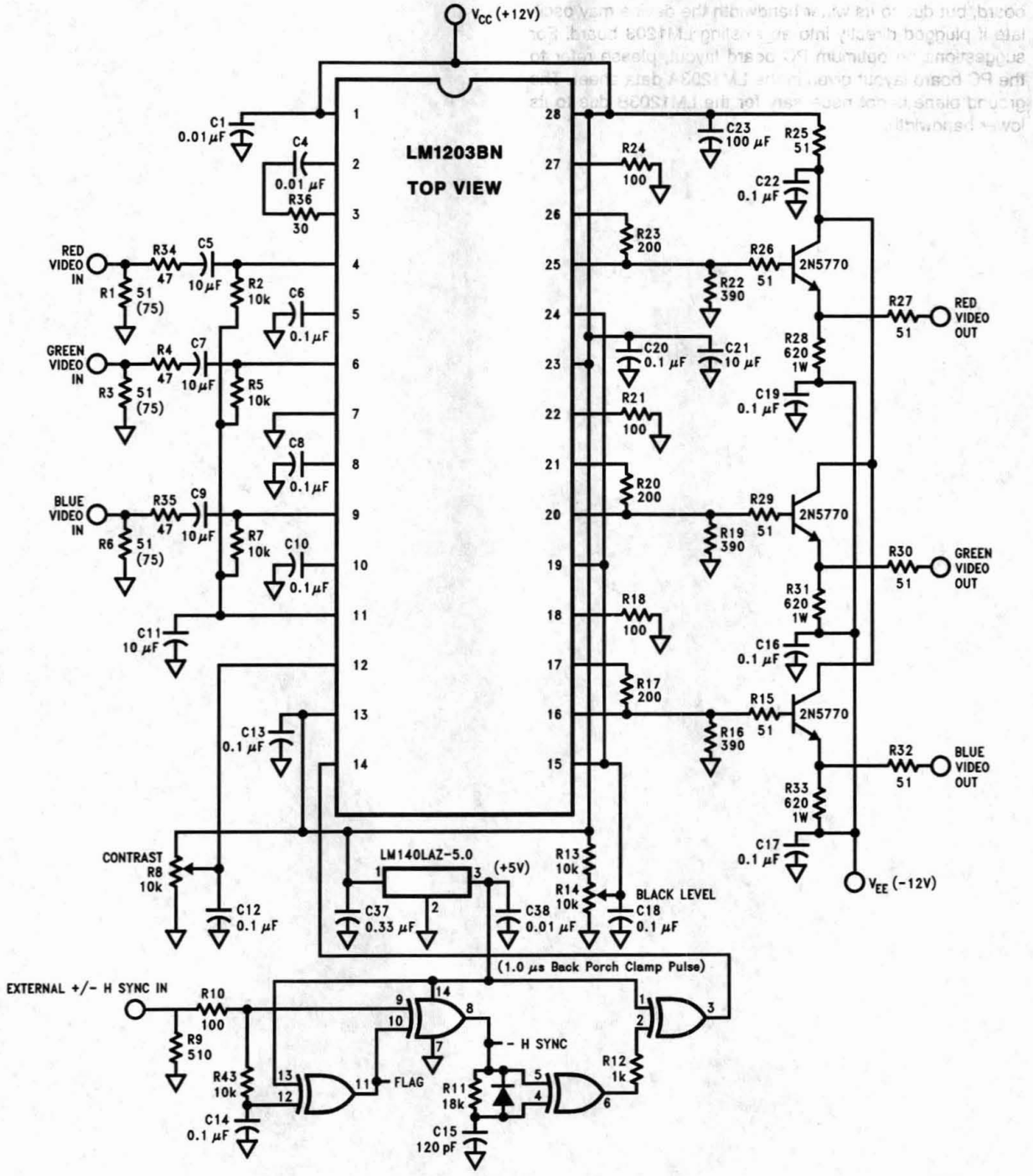

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FIGURE 11. LM1203B Applications Circuit

LM1203B versus LM1203

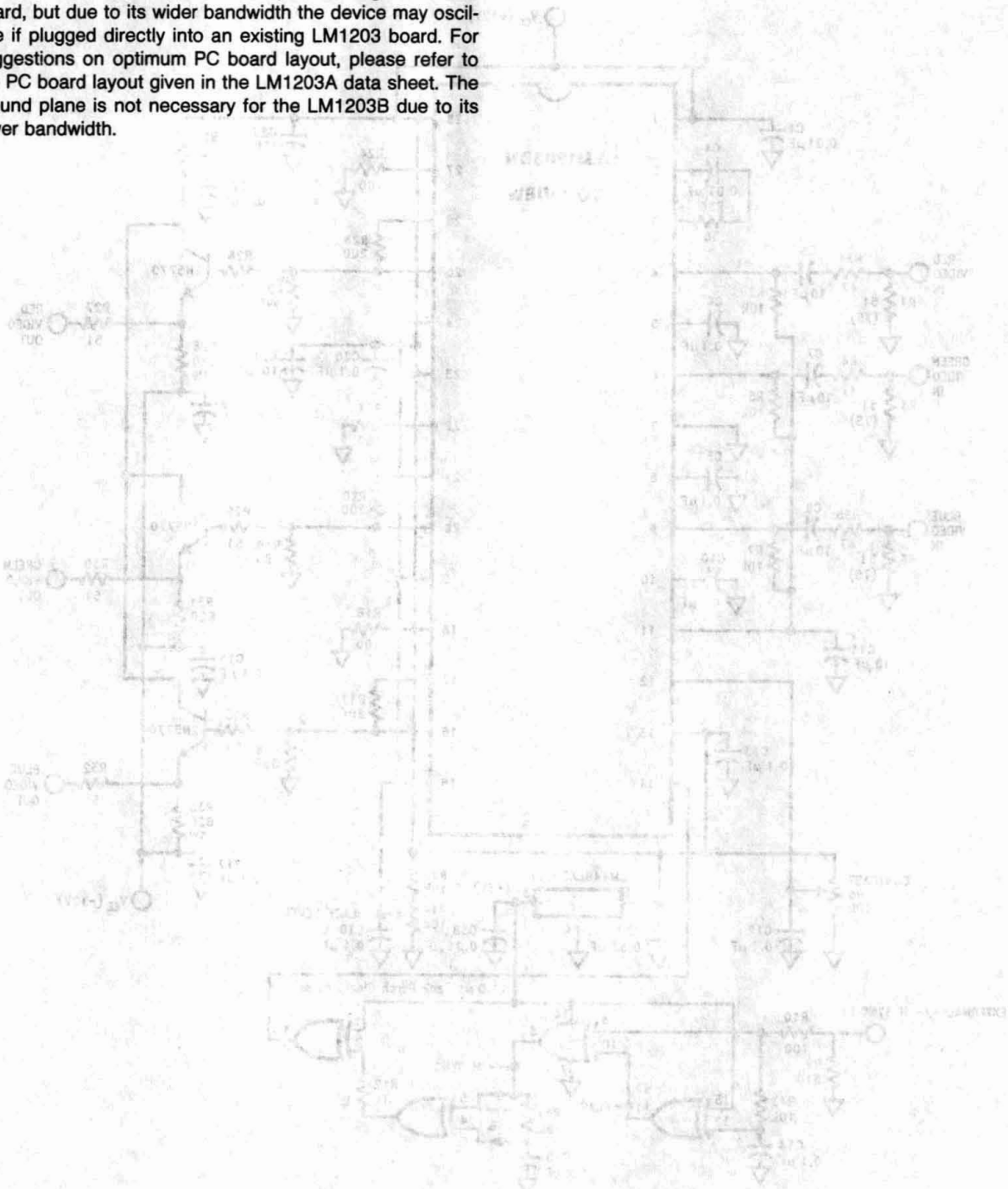
LM1203B is an improved version of the LM1203 RGB video amplifier system and is pin and function compatible with the LM1203. LM1203B's output voltage can swing as low as 0.15V as opposed to 0.9V for the LM1203. This eliminates the need for a level shift stage between the preamplifier and the CRT driver in most applications.

The LM1203B also offers faster rise and fall times of 3.7 ns versus 5 ns for the LM1203, resulting in 100 MHz bandwidth versus 70 MHz for LM1203. A peaking capacitor across the drive resistor is necessary to obtain these rise and fall times. The LM1203B is stable on a well layed out single sided PC board, but due to its wider bandwidth the device may oscillate if plugged directly into an existing LM1203 board. For suggestions on optimum PC board layout, please refer to the PC board layout given in the LM1203A data sheet. The ground plane is not necessary for the LM1203B due to its lower bandwidth.

The LM1203B also includes a built in power down spot killer to prevent a flash on the screen upon power down. In some preamplifiers, the video output signal may go high as the device is being powered down. This may cause a whiter than white level at the output of the CRT driver thus causing a flash on the screen.

Reference

Ott, Henry W., "Noise Reduction Techniques in Electronic Systems", John Wiley & Sons, New York, 1976.



National Semiconductor

LM1204 150 MHz RGB Video Amplifier System

General Description

The LM1204 is a triple 150 MHz video amplifier system designed specifically for high resolution RGB video display applications. In addition to three matched video amplifiers, the LM1204 contains a DC operated contrast control, a DC operated drive control for each amplifier, and a dual clamping system for both brightness control and video blanking. The LM1204 also contains a back porch clamp pulse generator which is activated by an externally supplied ±H/HV sync signal or by an external composite video signal. The ±H/HV sync input will have priority over the composite video input. A single −H/HV sync output is provided for the automatically selected sync input signal. The back porch clamp pulse width is user adjustable from 0.3 μs to 4 μs.

The LM1204 video output stage will directly drive most Hybrid or discrete CRT amplfier input stages without the need for an external buffer transistor. The device has been designed to operate from a 12V supply with all DC controls operating over a 0V to 4V range providing for an easy interface to serial digital buss controlled monitors.

Features

- Built-in video blanking function
- Built-in sync separator for composite video input
- Includes DC restoration of video signals
- Back porch clamp pulse width user adjustable
- DC control of brightness, contrast, blanking level, drive and cutoff
- DC controls are 0V to 4V for easy interfacing to a digitally controlled system

Key Specifications

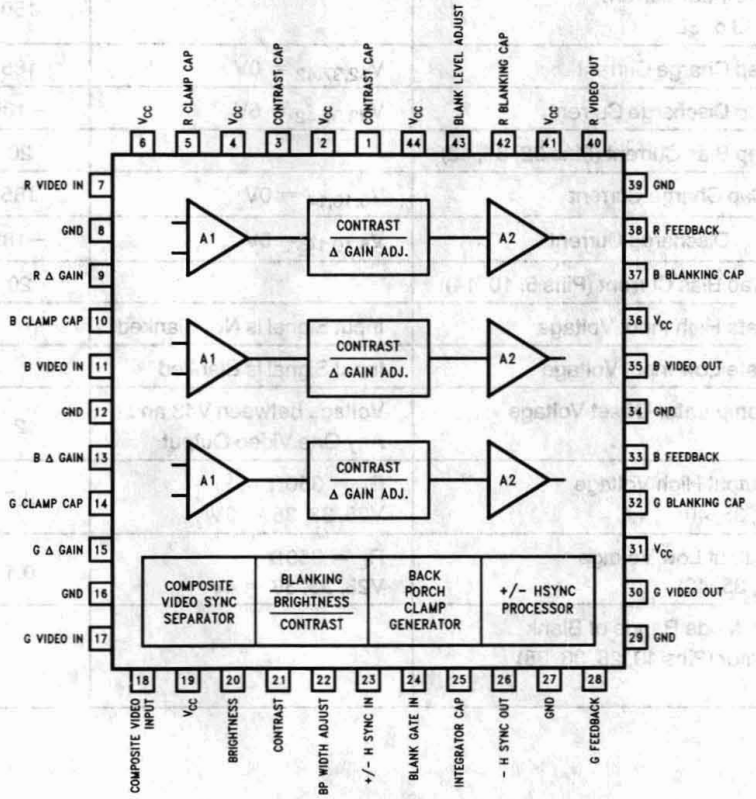
- 150 MHz large signal bandwidth (typ)
- 2.3 ns rise/fall times (typ)
- 0.1 dB contrast tracking (typ)
- ±3 dB drive (Δ gain) adjustments on R, G, B channels (typ)

Applications

- High resolution CRT monitors
- Video AGC amplifier
- Wideband amplifier with gain and DC offset control

Block Diagram and Connection Diagram

Top View



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Ordering Information

Order Number LM1204V
See NS Package Number V44A

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage, V_{CC} Pins 2, 4, 6, 19, 31, 41, 44 (Note 3)	13.5V
Peak Video Output Source Current (Any One Amplifier) Pins 30, 35 or 39	30 mA
Voltage at Any Input Pin, V_{IN}	GND ≤ V_{IN} ≤ V_{CC}
Maximum ±H Sync Input Voltage	5.5 V_{PP}
Power Dissipation, PD (Above 25°C	
Derate Based on θ_{JA} and T_J)	2.4W
Thermal Resistance, θ_{JA}	52 °C/W
Junction Temperature, T_J	150°C
ESD Susceptibility (Note 4)	2.5 kV
Storage Temperature	−65°C to 150°C
Lead Temperature	
Vapor Phase (60 seconds)	215°C
Infrared (15 seconds)	220°C

Operating Ratings (Note 2)

Temperature Range	0°C to 70°C
Supply Voltage, V_{CC}	10.8V ≤ V_{CC} ≤ 13.2V

DC Electrical Characteristics (Video Amplifier Section)

The following specifications apply for V_{CC} (pins 2, 4, 6, 19, 31, 36, 41 and 44) = 12V and T_A = 25°C unless otherwise specified. S1 = B, S2 = B, S3, 4, 5 closed, V9, 13, 15 = 2V, V20, 21, 22, 24, 43 = 0.5V unless otherwise specified; see test circuit, *Figure 1*.

Symbol	Parameter	Conditions	Typical (Note 5)	Limit (Note 6)	Units
I_S	Supply Current	No Video or Sync Input Signals, S1 = A	100	125	mA (Max)
I_B	Input Bias Current (Pin 9, 13, 15, 20, 21 or 22)	S1 = A	0.3	2	µA (Max)
I_{24h}	Blank Gate Input High Current	V24 = 4V	0.01	2	µA (Max)
I_{24l}	Blank Gate Input Low Current	V24 = 0V	2	5	µA (Max)
I_{FB}	Feedback Input Current (Pin 28, 33 or 38)		150		nA
I_{Blank+}	Blank Cap Charge Current	$V_{32,37,42}$ = 0V	185	75	µA (Min)
I_{Blank-}	Blank Cap Discharge Current	$V_{32,37,42}$ = 5V	−185	−75	µA (Min)
I_{BB}	Blank Cap Bias Current (Pins 32, 37, 42)		20		nA
I_{Clamp+}	Clamp Cap Charge Current	$V_{5,10,14}$ = 0V	185	75	µA (Min)
I_{Clamp-}	Blank Cap Discharge Current	$V_{5,10,14}$ = 5V	−185	−75	µA (Min)
I_{CB}	Clamp Cap Bias Current (Pins 5, 10, 14)		20		nA
V_{24h}	Blank Gate High Input Voltage	Input Signal is Not Blanked		2	V (Min)
V_{24l}	Blank Gate Low Input Voltage	Input Signal is Blanked		0.8	V (Max)
	Blank Comparator Offset Voltage	Voltage between V43 and Any One Video Output	2	50	mV (Max)
V_H	Video Output High Voltage (Pins 30, 35, 40)	R_L = 350Ω V28, 33, 38 = 0V	8.7	7	V(Min)
V_L	Video Output Low Voltage (Pins 30, 35, 40)	R_L = 350Ω V28, 33, 38 = 4V	0.1	0.5	V(Max)
V_{CM43}	Common Mode Range of Blank Comparator (Pins 43, 28, 33, 38)			0.5 4	V(Min) V(Max)

DC Electrical Characteristics (Sync Separator/Processor Section)

The following specifications apply for V_{CC} (Pins 2, 4, 6, 19, 31, 36, 41 and 44) = 12V and T_A = 25°C, unless otherwise specified. S1 = B, S2 = B, S3, 4, 5 closed, V9, 13, 15 = 2V, V20, 21, 22, 24, 43 = 0.5V, unless otherwise specified; see Test Circuit *Figure 1*.

Symbol	Parameter	Conditions	Typical (Note 5)	Limit (Note 6)	Units
$-H\ V_{OH}$	−H Sync Output Logic High (Pin 26)		4.2	2.4	V(Min)
$-H\ V_{OL}$	−H Sync Output Logic Low (Pin 26)		0.1	0.4	V(Max)
V_{23}	Quiescent DC Voltage at ±H Sync Input		3		V

AC Electrical Characteristics (Video Amplifier Section)

The following specifications apply for V_{CC} (Pins 2, 4, 6, 19, 31, 36, 41 and 44) = 12V and T_A = 25°C, unless otherwise specified. S1 = B, S2 = B, S3, 4, 5 closed, V9, 13, 15, 21, 24, 43 = 4V, V20 = 2V, unless otherwise specified; see Test Circuit *Figure 1*.

Symbol	Parameter	Conditions	Typical (Note 5)	Limit (Note 6)	Units
R_{IN}	Video Amplifier Input Resistance		20		kΩ
A_{Vmax}	Maximum Video Amplifier Gain	f_{IN} = 12 kHz	10	5.5	V/V(Min)
ΔA_{Vtrack}	Amplifier Gain (Contrast) Tracking (Note 7)		0.1		dB
ΔA_{V2V}	Attenuation at 2V	Ref: $A_{V_{max}}$ V21 = 2V	6		dB
$\Delta A_{V0.5V}$	Attenuation at 0.5V	Ref: $A_{V_{max}}$ V21 = 0.5V	28	20	dB(Min)
ΔGain	Δ Gain Range (Pins 9, 13, 15)	V9, 13, 15 = 0V to 4V	±3		dB
ΔV_O	Max Brightness Tracking Error (Note 8)		100		mV
$f_{-3\ dB}$	Video Amplifier Bandwidth (Note 9)	V_{OUT} = 3.5 V_{PP}	150		MHz
THD	Video Amplifier Distortion	V_{OUT} = 1 V_{PP}, f = 12 kHz	0.3		%
t_R	Video Output Rise Time (Note 9)	Square Wave Input V_{OUT} = 3.5 V_{PP}, R_L = 350Ω	2.0		ns
t_F	Video Output Fall Time (Note 9)	Square Wave Input V_{OUT} = 3.5 V_{PP}, R_L = 350Ω	2.3		ns
$V_{ISO\ (1\ MHz)}$	Video Amplifier 1 MHz Isolation (Notes 9, 10)		−50		dB
$V_{ISO\ (130\ MHz)}$	Video Amplifier 130 MHz Isolation (Notes 9, 10)		−10		dB

AC Electrical Characteristics (Sync Separator/Processor Section)

The following specifications apply for V_{CC} (Pins 2, 4, 6, 19, 31, 36, 41 and 44) = 12V and T_A = 25°C, unless otherwise specified. S1 = A, S2 = B, S3, 4, 5 closed, V9, 13, 15, 20, 21, 43 = 2V, unless otherwise specified; see Test Circuit *Figure 1* and Timing Diagram for input waveform.

Symbol	Parameter	Conditions	Typical (Note 5)	Limit (Note 6)	Units
$V_{18(Min)}$	Composite Video Input Voltage (Pin 18)	S2 = A, Input = 10% Duty Cycle, Test for Loss of BP Pulse at Pin 26		0.15	V_{PP} (Min)
$V_{18(Max)}$	Composite Video Input Voltage (Pin 18)			2	V_{PP} (Max)
V_{23}	±H Sync Input Voltage (Pin 23)	Input = 10% Duty Cycle		1.6	V_{PP} (Min)
	Back Porch Clamp Pulse Width at V_{24} = 1V	S2 = A, Pin 26 = BP Output	1	1.4	µs (Max)
	Back Porch Clamp Pulse Width at V_{24} = 4V		300	600	ns (Max)
	Maximum ±H Sync Input Frequency		600		KHz
D_{HI}	Max Duty Cycle of Active High H Sync (Pin 23)	Test for Loss of Sync at Pin 26	22		%
D_{LO}	Max Duty Cycle of Active Low H Sync (Pin 23)		22		%
t_{pdl1}	±H Sync Input to −H Sync Output Low Delay	Input = 10% Duty Cycle	100		ns
t_{pdh1}	±H Sync Input to −H Sync Output High Delay	Input = 10% Duty Cycle	65		ns
t_{pd1}	±H Sync Input Trailing Edge to Back Porch Clamp Output Delay	Input = 10% Duty Cycle, S2 = A	70		ns
t_{pdl2}	Composite Video Input to −H Sync Output Low Delay	Input = 10% Duty Cycle	106		ns
t_{pdh2}	Composite Video Input to −H Sync Output High Delay	Input = 10% Duty Cycle	68		ns
t_{pd2}	Composite Video Input Trailing Edge to Back Porch Clamp Output Delay	Input = 10% Duty Cycle S2 = A	78		ns
$t_{pdl2}-t_{pdl1}$	Composite Video and ±H Sync Input to −H Sync Output Delta Delay	Input = 10% Duty Cycle	6		ns

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur.

Note 2: Operating Ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.

Note 3: V_{CC} supply pins 2, 4, 6, 19, 31, 36, 41 and 44 must be externally wired together to prevent internal damage during V_{CC} power on/off cycle.

Note 4: Human body model, 100 pF discharged through a 1.5 kΩ resistor.

Note 5: Typical specifications are specified at +25°C and represent the most likely parametric norm.

Note 6: Tested limits are guaranteed to National's AOQL (Average Outgoing Quality Level).

Note 7: ΔA_V tracking is a measure of the ability of any two amplifiers to track each other and quantifies the matching of the three attenuators. It is the difference in gain change between any two amplifiers with the contrast voltage, V21, at either 4V or 2V measured relative to an A_V max condition V21 = 4V. For example, at A_V max, the three amplifier gains might be 17.4 dB, 16.9 dB and 16.4 dB and change to 7.3 dB, 6.9 dB and 6.5 dB respectively for V21 = 2V. This yields the measured typical ±0.1 dB channel tracking.

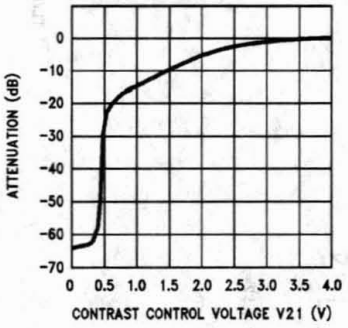
Note 8: Brightness tracking error is measured with all three video channels set for equal gain. The measured value is limited by the resolution of the measurement equipment.

Note 9: When measuring video amplifier bandwidth or pulse rise and fall times, a double sided full ground plane printed circuit board is recommended. Video amplifier isolation tests also require this printed circuit board. The measured rise and fall times are effective rise and fall times, taking into account the rise and fall times of the generator.

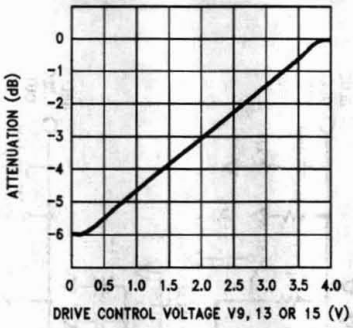
Note 10: Measure output levels of either undriven amplifier relative to the driven amplifier to determine channel isolation. Terminate the undriven amplifier inputs.

Typical Performance Characteristics V_{CC} = 12V, T_A = 25°C unless otherwise specified

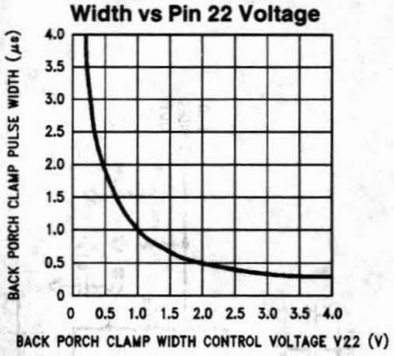
Attenuation vs Contrast Control Voltage (f = 12 kHz)



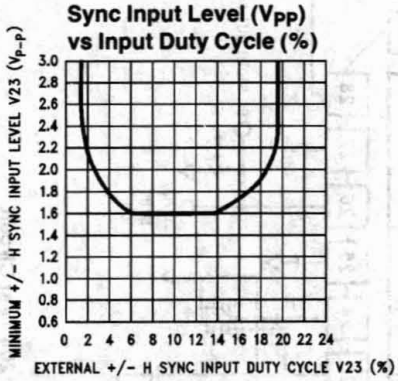
Attenuation vs Drive Control Voltage (f = 12 kHz)



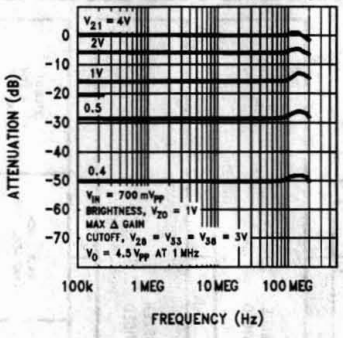
Back Porch Clamp Pulse Width vs Pin 22 Voltage



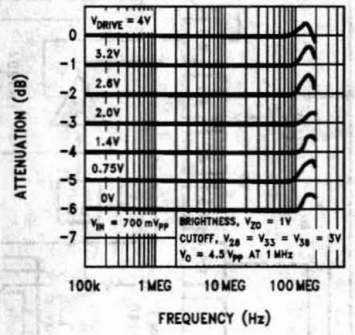
Minimum External ±H Sync Input Level (V_{PP}) vs Input Duty Cycle (%)



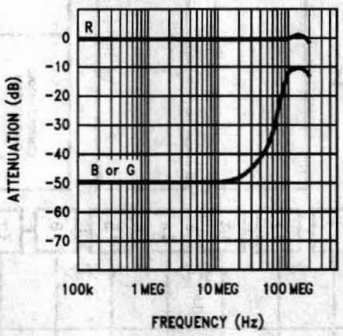
Contrast vs Frequency



Drive Control vs Frequency



Crosstalk vs Frequency



TL/H/11238–2

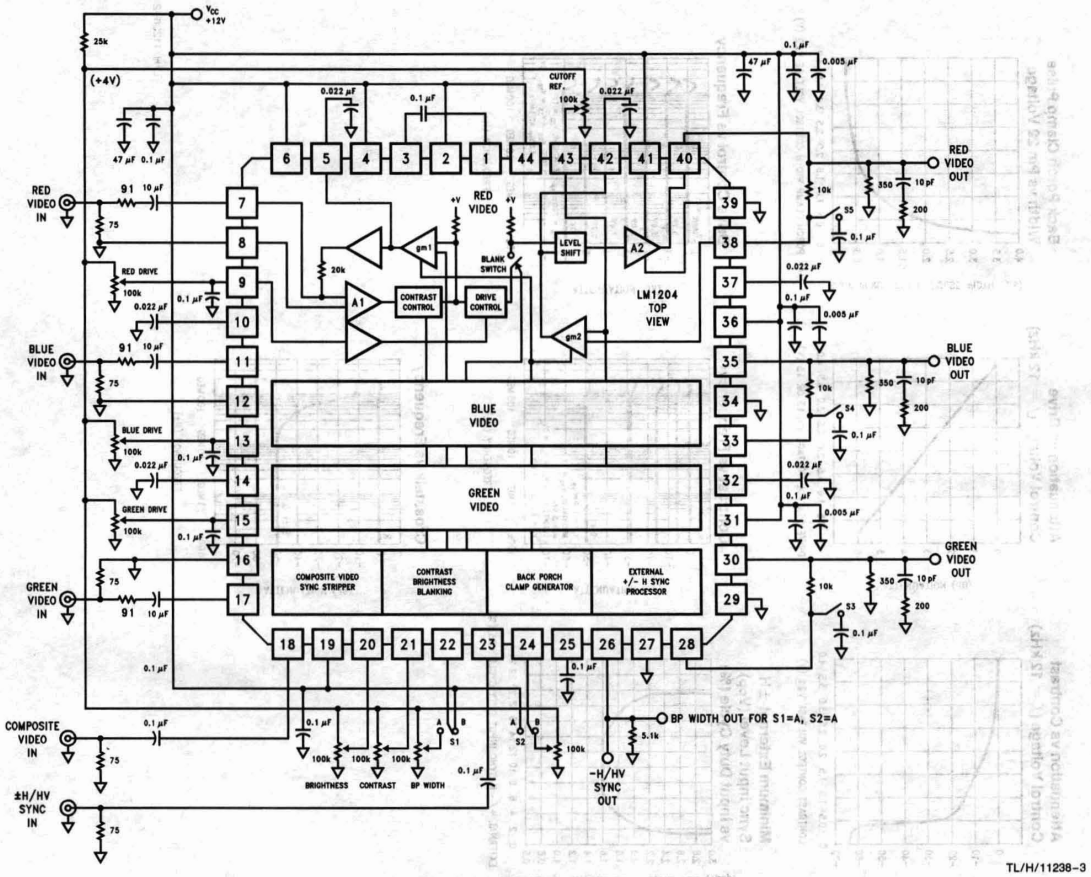


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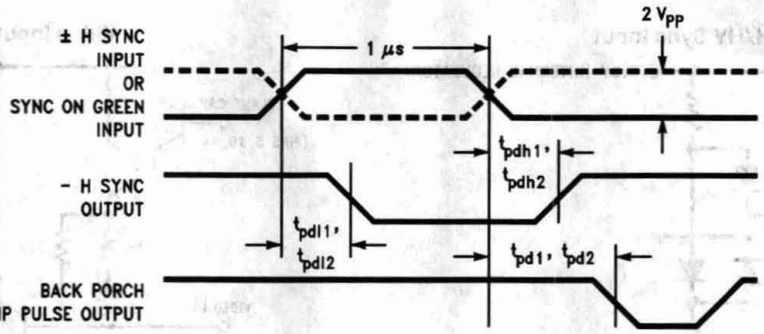
FIGURE 1. LM1204 Test Circuit

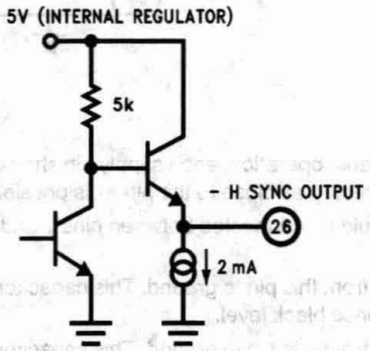
Timing Diagram



TL/H/11238–4

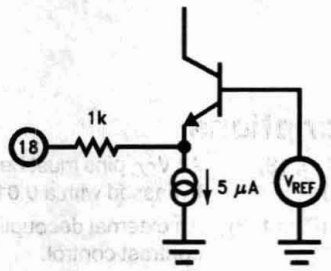
Input/Output Stages

–H Sync Output Stage



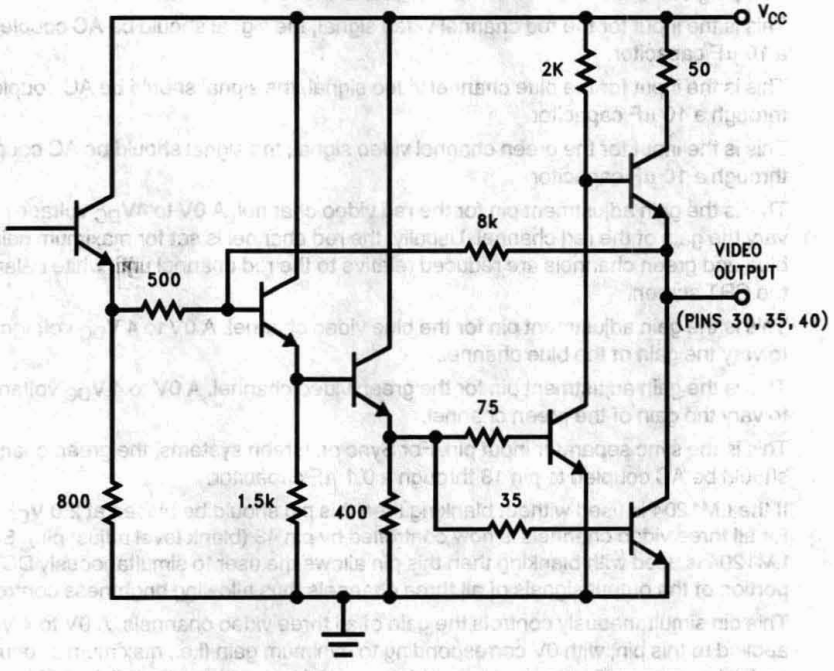
TL/H/11238–5

Composite Video Input



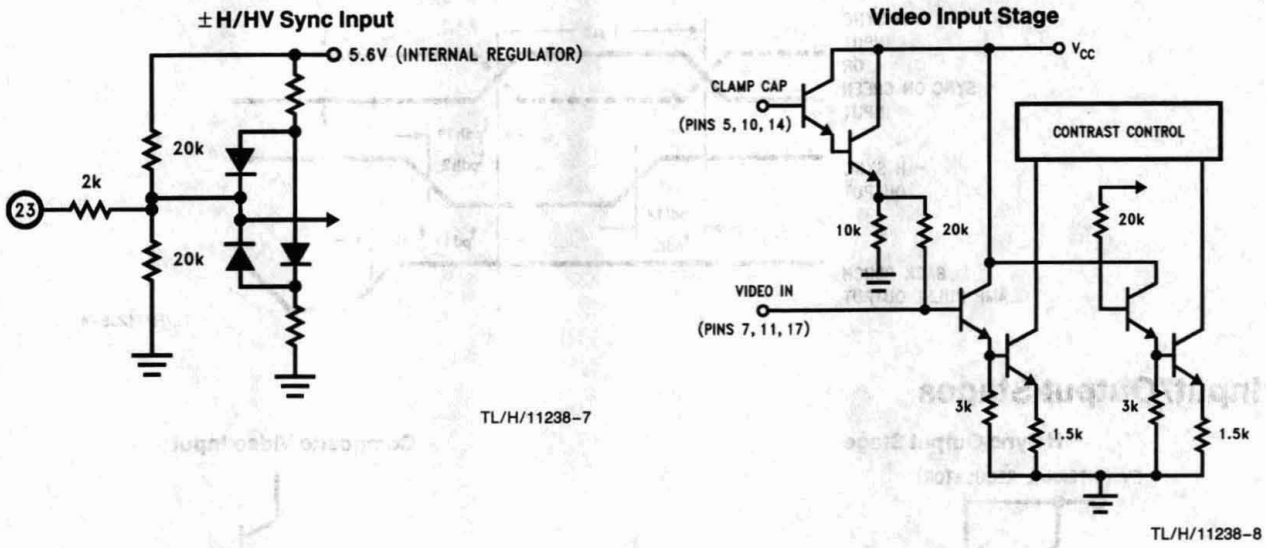
TL/H/11238–6

Video Output Stage



TL/H/11238–21

Input/Output Stages (Continued)



Pin Descriptions

V_{CC} (Pins 2, 4, 6, 19, 31, 36, 41, 44)	All V_{CC} pins must be externally wired together. For stable operation, each supply pin should be bypassed with a 0.01 μF and a 0.1 μF capacitor connected as close to the pin as is possible.
Contrast Cap (Pins 1, 3)	An external decoupling capacitor of value 0.1 μF should be connected between pins 1 and 3 for contrast control.
R Clamp Cap (Pin 5)	A 0.022 μF to 0.1 μF capacitor should be connected from this pin to ground. This capacitor allows clamping of the red channel video signal to the reference black level.
B Clamp Cap (Pin 10)	A 0.022 μF to 0.1 μF capacitor should be connected from this pin to ground. This capacitor allows clamping of the blue channel video signal to the reference black level.
G Clamp Cap (Pin 14)	A 0.022 μF to 0.1 μF capacitor should be connected from this pin to ground. This capacitor allows clamping of the green channel video signal to the reference black level.
R Video In (Pin 7)	This is the input for the red channel video signal, the signal should be AC coupled to the input through a 10 μF capacitor.
B Video In (Pin 11)	This is the input for the blue channel video signal, the signal should be AC coupled to the input through a 10 μF capacitor.
G Video In (Pin 17)	This is the input for the green channel video signal, the signal should be AC coupled to the input through a 10 μF capacitor.
R Δ Gain (Pin 9)	This is the gain adjustment pin for the red video channel. A 0V to 4V_{DC} voltage is applied to this pin to vary the gain of the red channel. Usually, the red channel is set for maximum gain and the gains of the blue and green channels are reduced relative to the red channel until white balance is achieved on the CRT screen.
B Δ Gain (Pin 13)	This is the gain adjustment pin for the blue video channel. A 0V to 4 V_{DC} voltage is applied to this pin to vary the gain of the blue channel.
G Δ Gain (Pin 15)	This is the gain adjustment pin for the green video channel. A 0V to 4 V_{DC} voltage is applied to this pin to vary the gain of the green channel.
Compose Video Input (Pin 18)	This is the sync separator input pin. For Sync on Green systems, the green channel video signal should be AC coupled to pin 18 through a 0.1 μF capacitor.
Brightness Control (Pin 20)	If the LM1204 is used without blanking then this pin should be biased at 2.0 V_{DC}. Brightness control for all three video channels is now controlled by pin 43 (blank level adjust pin). See *Figure 4*. If the LM1204 is used with blanking then this pin allows the user to simultaneously DC offset the video portion of the output signals of all three channels thus allowing brightness control (See *Figure 5*).
Contrast Control (Pin 21)	This pin simultaneously controls the gain of all three video channels. A 0V to 4 V_{DC} input voltage is applied to this pin, with 0V corresponding to minimum gain (i.e., maximum attenuation of video signal) and 4V corresponding to maximum gain (i.e., minimum attenuation of the video signal).

Pin Descriptions (Continued)

Back Porch Clamp Width Adjust (Pin 22)

The LM1204 provides DC restoration or clamping during the back porch interval of the video signal. The width of LM1204's internally generated back porch clamp signal can be varied by applying a 0V to 4 V_{DC} voltage to this pin. The back porch clamp signal width can be varied from approximately 0.3 μs to 4.0 μs by applying 4V to 0.5V respectively. By connecting the blank gate input pin (pin 24) to V_{CC}, the back porch clamp pulse can be monitored on the −H Sync output pin (pin 26). See *Figures 4* and *5*. By connecting pin 22 to V_{CC}, the LM1204 functions as a non-gated amplifier requiring no clamping. See Section 4 under application hints for further information.

±H Sync In (Pin 23)

This is the external sync input pin, it accepts a negative or positive polarity signal, either horizontal sync or a composite sync (1.2 V_{PP} minimum amplitude). The LM1204 also provides a negative polarity (TTL compatible) horizontal sync or composite sync output on pin 26. If the composite video input (pin 18) is not used then an H Sync signal should be AC coupled to this pin through a 0.1 μF capacitor. The ±H Sync input has priority over the composite video input if both signals are present.

Blank Gate In (Pin 24)

This is the blank gate input pin. The LM1204 allows video blanking at the preamplifier. If blanking is desired then a TTL compatible, negative polarity blanking signal should be applied to this pin. During the blanking interval, all three video outputs are level shifted to the blank level set by the voltage at pin 43. If blanking is not required then, pin 24 should be biased at 4V.

Connecting pin 24 to V_{CC} will cause pin 26 to output the internally generated back porch clamp signal. The user can observe the change in back porch width as the potential at pin 22 is varied (see *Figures 4* and *5*).

Integrator Cap (Pin 25)

A 0.1 μF capacitor should be connected from this pin to ground. This capacitor allows the LM1204 to integrate the ±H Sync input signal and genreate the proper polarity switch for −H Sync output.

−H Sync Out (Pin 26)

This output pin provides a negative polarity horizontal sync signal for other system uses. There is approximately 100 ns delay between the ±H Sync input signal at pin 23 and the −H Sync output signal at pin 26.

Connecting pin 24 to V_{CC} will cause pin 26 to output the internally generated back porch clamp signal. The user can observe the change in back porch clamp pulse width as the potential at pin 22 is varied (See *Figures 4* and *5*).

G Feedback (Pin 28)

This is the cutoff adjustment input for the green video channel. The green video output signal from pin 30 is fed back to this input through a potentiometer thus allowing the user to individually adjust the cutoff (black reference) level for each gun. The signal level at this pin should be between 0.5V and 4V.

B Feedback (Pin 33)

This is the cutoff adjustment input for the blue video channel. The blue video output signal from pin 35 is fed back to this input through a potentiometer thus allowing the user to individually adjust the cutoff (black reference) level for each gun. The signal level at this pin should be between 0.5V and 4V.

R Feedback (Pin 38)

This is the cutoff adjustment input for the red video channel. The red video output signal from pin 40 is fed back to this input through a potentiometer thus allowing the user to individualy adjust the cutoff (black reference) level for each gun. The signal level at this pin should be between 0.5V and 4V.

G Video Output (Pin 30)

This is the green channel video output.

B Video Output (Pin 35)

This is the blue channel video output.

R Video Output (Pin 40)

This is the red channel video output.

G Blank Clamp Cap (Pin 32)

A 0.022 μF to 0.1 μF capacitor should be connected from this pin to ground. This capacitor allows blanking for the green video channel.

B Blank Clamp Cap (Pin 37)

A 0.022 μF to 0.1 μF capacitor should be connected from this pin to ground. This capacitor allows blanking for the blue video channel.

R Blank Clamp Cap (Pin 42)

A 0.022 μF to 0.1 μF capacitor should be connected from this pin to ground. This capacitor allows blanking for the red video channel.

Blank Level Adjust (Pin 43)

This pin serves two functions depending on whether the LM1204 is used with blanking or without blanking. If blanking is not selected then pin 20 should be biased at 2.0 V_{DC} and pin 43 assumes the role of brightness control. Varying the potential at pin 43 will simultaneously DC offset the video output signals of all three channels (See *Figure 4*). If the LM1204 is used with blanking then during the blanking interval, all three video output signals will be level shifted to the blank level. The desired blank level can be set by adjusting the potential at pin 43. Brightness control is now made possible by varying the potential at pin 20. Adjusting the brightness control DC offsets the video portion of the signal relative to the fixed blank level (all channels are affected simultaneously). See *Figure 5*.

GND (Pins 8, 12 16, 27, 29, 34, 39)

Ground. All ground pins must be connected to the ground plane.

Applications Hints

The LM1204 is a wideband video amplifier system designed specifically for high resolution RGB CRT monitors. The device includes circuitry for DC restoration of video signals and also allows contrast and brightness control. DC restoration is done during the back porch interval of the video signal. An internal sync separator generates a back porch clamp signal either from a "Sync on Green" signal applied to the composite video input (pin 18) or from an externally supplied ±H Sync signal . The LM1204 first looks at the ±H Sync input (pin 23), if an external horizontal sync signal is not present then the device syncs off the composite video input. The internally generated back porch clamp pulse width is user adjustable.

A blanking function is also included. This allows the user to cutoff the beam current in the CRT's guns during the blanking interval thereby preventing horizontal retrace lines from being visible. Normally blanking is done by applying a high voltage pulse at the grid. However, blanking at the cathode using the LM1204 leads to ease of design and lowered cost.

Figure 2 shows the block diagram of the green video channel and the control logic. The two modes of operation, with and without blanking, are described below in detail.

1.0 Operation without Blanking

For operation without blanking, the blank gate input (pin 24) should be connected to +4V. This causes the blank comparator to connect switch S2 to position Y (See *Figure 2*).

Furthermore, the brightness control input pin (pin 20) should be biased at a potential between 1V (Min) and 3.8V (Max), it is best to bias this pin at 2V. The video signal is AC coupled to the input of the LM1204 as shown for the green channel in *Figure 2*. During the back porch interval of the video signal (See *Figure 3*), the internally generated back porch clamping pulse goes low, causing switches S1A and S1B to be closed. The closure of S1A causes g_m1 to charge capacitor C2 to a potential determined by the DC voltage at pin 20. This allows g_m1 to set up an average DC bias for the AC coupled video signal at the input of A1. When the back porch clamping pulse is high, S1A and S1B are opened. With S1A open, g_m1 is effectively disconnected from C2, C2 now holds the DC bias voltage. The transconductance stage g_m1 therefore functions as a sample and hold device and holds the input of A1 at the desired DC bias.

The LM1204 uses black level clamping at the back porch of the video signal to accomplish DC restoration. The transconductance stage g_m2 is enabled during the back porch clamp period to provide a sample and hold function. During the back porch clamp period, DC feedback from LM1204's video output is compared with the voltage set by potentiometer R9. Depending on A2's output voltage, C6 is either charged or discharged so that the feedback loop consisting of g_m2 and A2 is stabilized and the output is clamped to the black level. All this occurs during the back porch clamp period. During the video portion of the signal, g_m2 is disabled and C6 holds the fixed black level reference voltage. The beginning of each new line on the raster always starts from a fixed reference black level thus restoring the DC component of each line.

A2 is a summing amplifier that adds a DC offset component from g_m2 to the video signal from the multiplier. Adjusting R9 will DC offset the output signals of all three channels thus providing brightness control. Individual cutoff adjustment for each channel is done by varying the feedback voltage at each of the R, G and B feedback inputs (Pins 38, 28 and 33). For example, cutoff adjustment for the green channel is done by potentiometer R8 shown in *Figure 2*.

Adjusting the contrast control (potentiometer R3 in *Figure 2*) varies the peak to peak amplitude (includes sync tip if present) of all three video output signals relative to their black reference level. The Δ Gain adjust (pins 9, 15 and 13 for R, G, and B channels respectively) allows the user to individually adjust the AC gain of each channel. For example the AC gain of the green channel is adjusted using potentiometer R5 as shown in *Figure 2*. Normally the red channel is set for maximum gain and the gains of the blue and green channels are reduced until white balance is achieved on the CRT monitor's screen. *Figure 4* shows the adjustments for operation without blanking.

2.0 Operation with Blanking

Much of what was discussed in Section 1.0 also applies when the LM1204 is used with the blanking function. However, there are notable differences as described herein. For operation with blanking, a TTL compatible blanking signal must be applied to the blank gate input (pin 24).

During the blanking period, the blanking comparator connects switch S2 to position X (See *Figure 2*). This causes the LM1204 to level shift the video output signal to the blank level. Adjusting R9 will adjust the blank level of all three channels. Individual blank level adjustment for each channel is done by varying the feedback voltage at each of the R, G and B feedback inputs (pin 38, 28 and 33). In *Figure 2* this is done by adjusting potentiometer R8 for the green channel.

During the video portion of the video signal, S2 is connected to position Y. Brightness control is now accomplished by varying the potential at the brightness control pin (pin 20). Adjusting R6 offsets the video portion of all three output signals relative to the fixed blank level, restoring the DC level of the video signal. *Figure 5* shows the adjustments for operation with blanking.

3.0 Stability Considerations

For optimum performance and stable operation, a double sided PC board with adequate ground plane is essential. Moreover, soldering the LM1204 on to the PC board will yield best results. Each supply pin (pins 2, 4, 6, 19, 31, 36, 41 and 44) should be bypassed with a 0.01 μF and a 0.1 μF capacitor connected as close to the supply pin as is possible.

When driving the LM1204 from a 75Ω video source, the cable is terminated with 75Ω to minimize reflections caused by transmission line effects. However, the input impedance of LM1204 is capacitive and is also affected by the stray capacitance of the PC board. Thus the input impedance is a function of frequency. This changes the impedance of the cable termination. This can introduce overshoot and ringing in LM1204's pulse response. A 100Ω resistor in series with the blocking capacitor at the video input will minimize overshoot and ringing (see *Figure 8*). The value of the resistor is empirically determined. 100Ω is a good starting value.

Since the LM1204 is a wide bandwidth amplifier with high gain at high frequencies, the device may oscillate when driving a large capacitive/inductive load. To prevent oscillation, the amplifier's gain is rolled off at high frequencies. This is accomplished by an RC network comprised of a resistor in

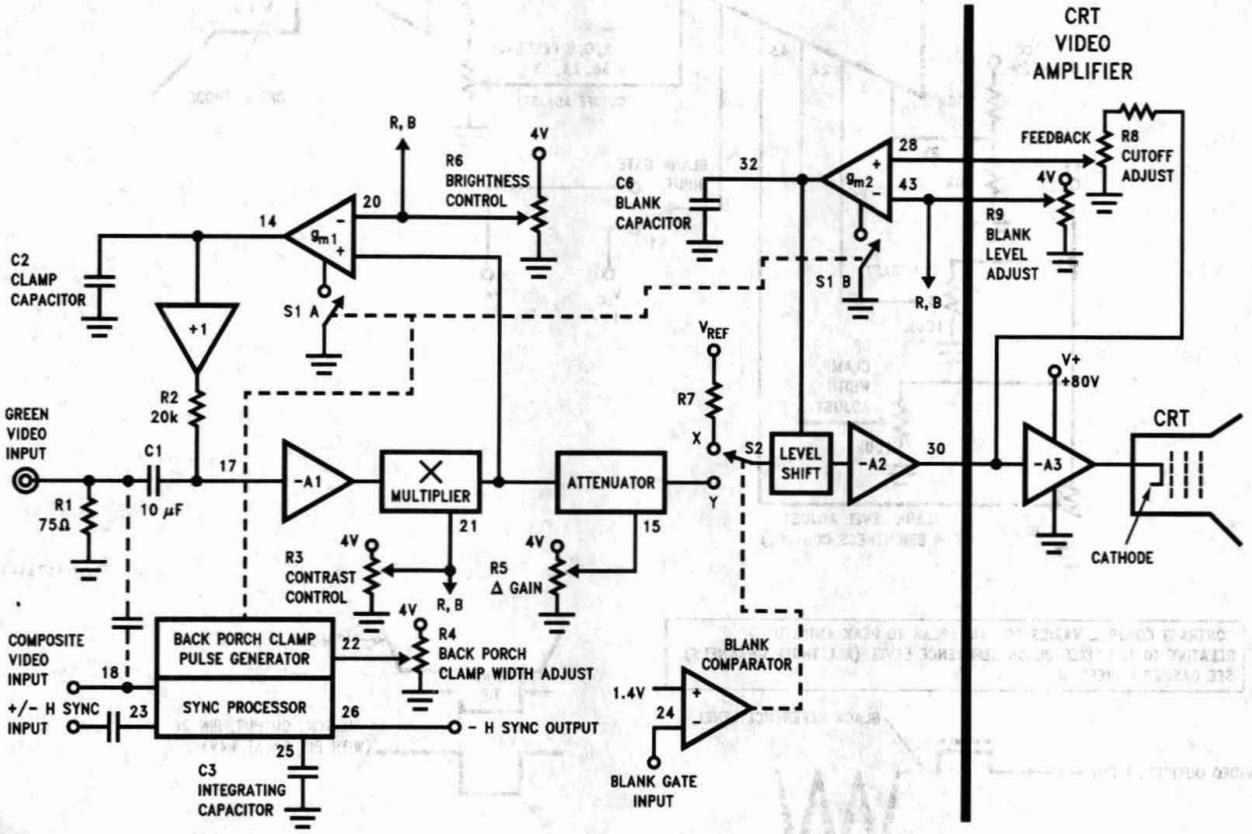
3.0 Stability Considerations (Continued)

series with a capacitor connected from the video output pin to ground (see Test Circuit, *Figure 1*). A 110Ω to 200Ω resistor in series with 10 pF is quite adequate for most applications. However, if oscillations don't cease then the value of the resistor should be decreased or the value of the capacitor should be increased or a combination of the two.

Non-Gated High Frequency Application

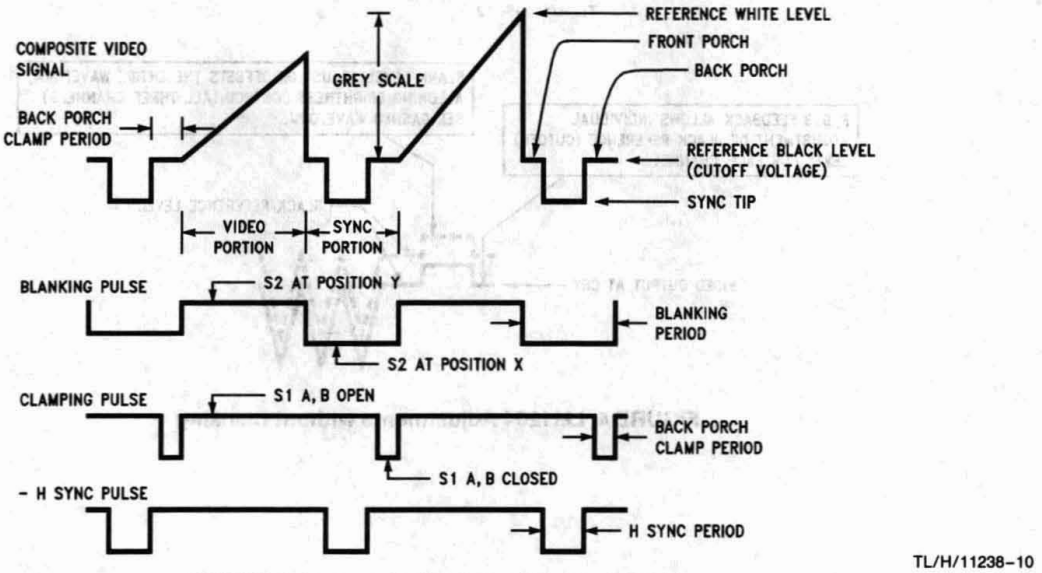
By connecting the back porch width adjust pin (pin 22) to V_{CC}, the LM1204 functions as a non-gated amplifier requiring no sync or blanking signals. *Figure 9* shows a triple high frequency amplifier with variable gain and DC offset control. In this mode of operation, filtered DC feedback must be provided to pins 28, 33 and 38 as shown in *Figure 9*.

LM1204



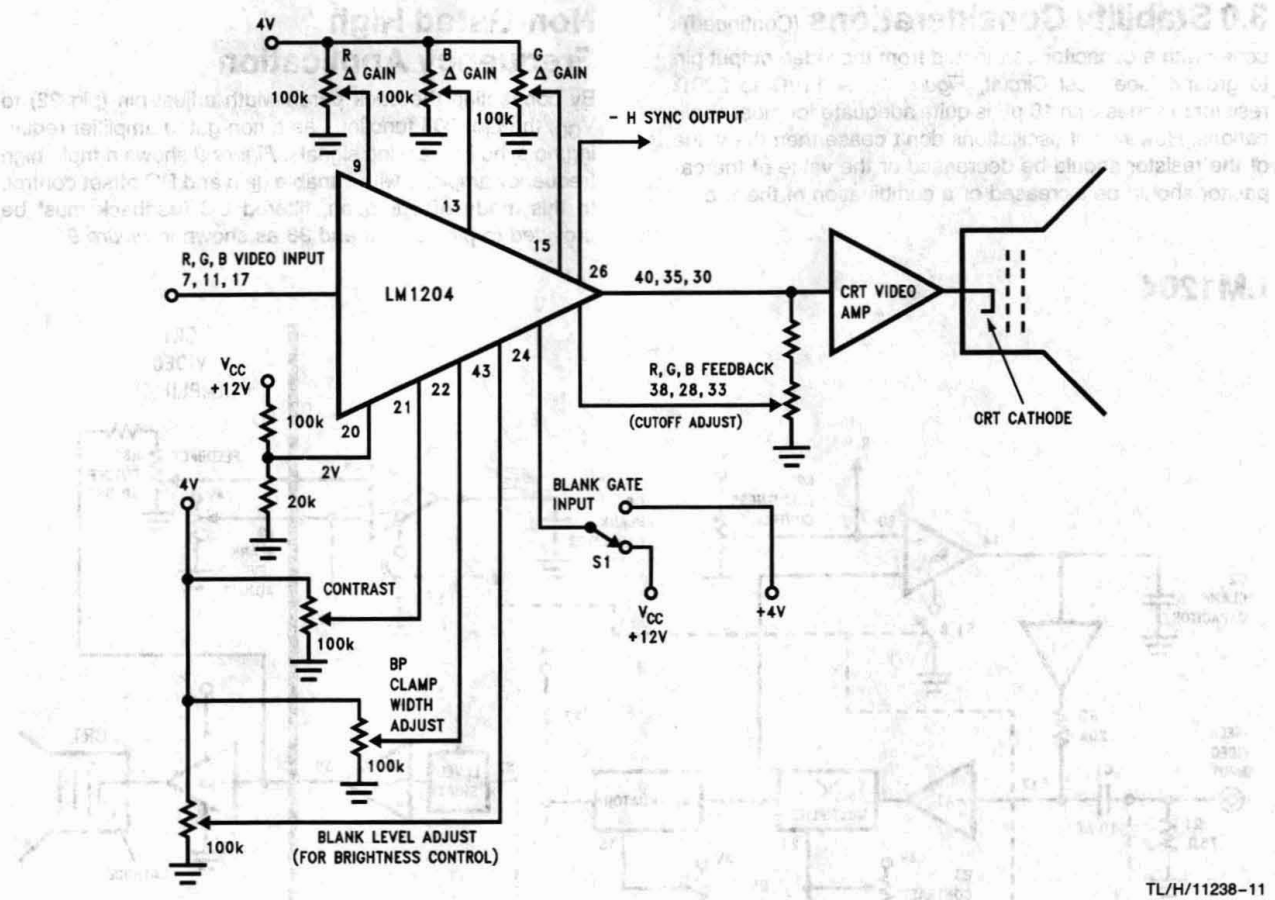
TL/H/11238–9

FIGURE 2. Block Diagram Showing Timing Circuitry and Green Video Channel



TL/H/11238–10

FIGURE 3. Composite Video and Timing Signals



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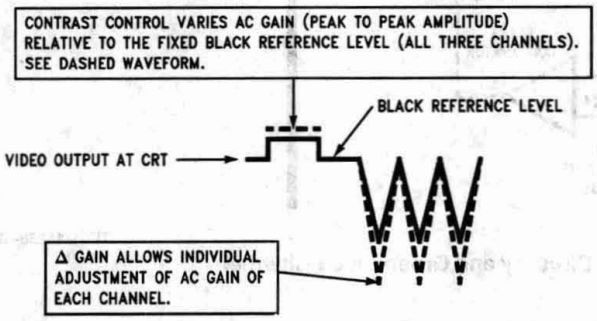
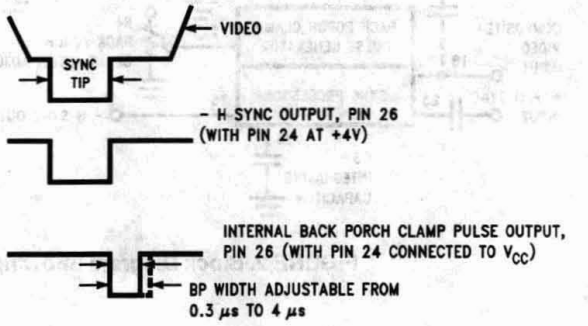

CONTRAST CONTROL VARIES AC GAIN (PEAK TO PEAK AMPLITUDE) RELATIVE TO THE FIXED BLACK REFERENCE LEVEL (ALL THREE CHANNELS). SEE DASHED WAVEFORM.
BLACK REFERENCE LEVEL
VIDEO OUTPUT AT CRT
Δ GAIN ALLOWS INDIVIDUAL ADJUSTMENT OF AC GAIN OF EACH CHANNEL.

TL/H/11238–12


VIDEO
SYNC
TIP
- H SYNC OUTPUT, PIN 26
(WITH PIN 24 AT +4V)
INTERNAL BACK PORCH CLAMP PULSE OUTPUT, PIN 26 (WITH PIN 24 CONNECTED TO V_{CC})
BP WIDTH ADJUSTABLE FROM
0.3 μs TO 4 μs

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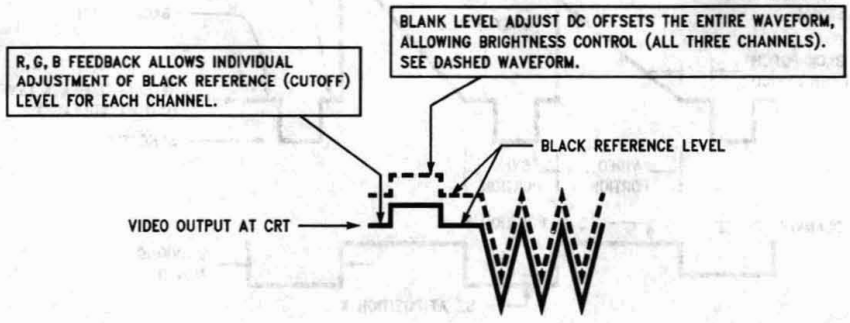
BLANK LEVEL ADJUST DC OFFSETS THE ENTIRE WAVEFORM, ALLOWING BRIGHTNESS CONTROL (ALL THREE CHANNELS). SEE DASHED WAVEFORM.
R, G, B FEEDBACK ALLOWS INDIVIDUAL ADJUSTMENT OF BLACK REFERENCE (CUTOFF) LEVEL FOR EACH CHANNEL.
BLACK REFERENCE LEVEL
VIDEO OUTPUT AT CRT

TL/H/11238–14

FIGURE 4. LM1204 Adjustments without Blanking

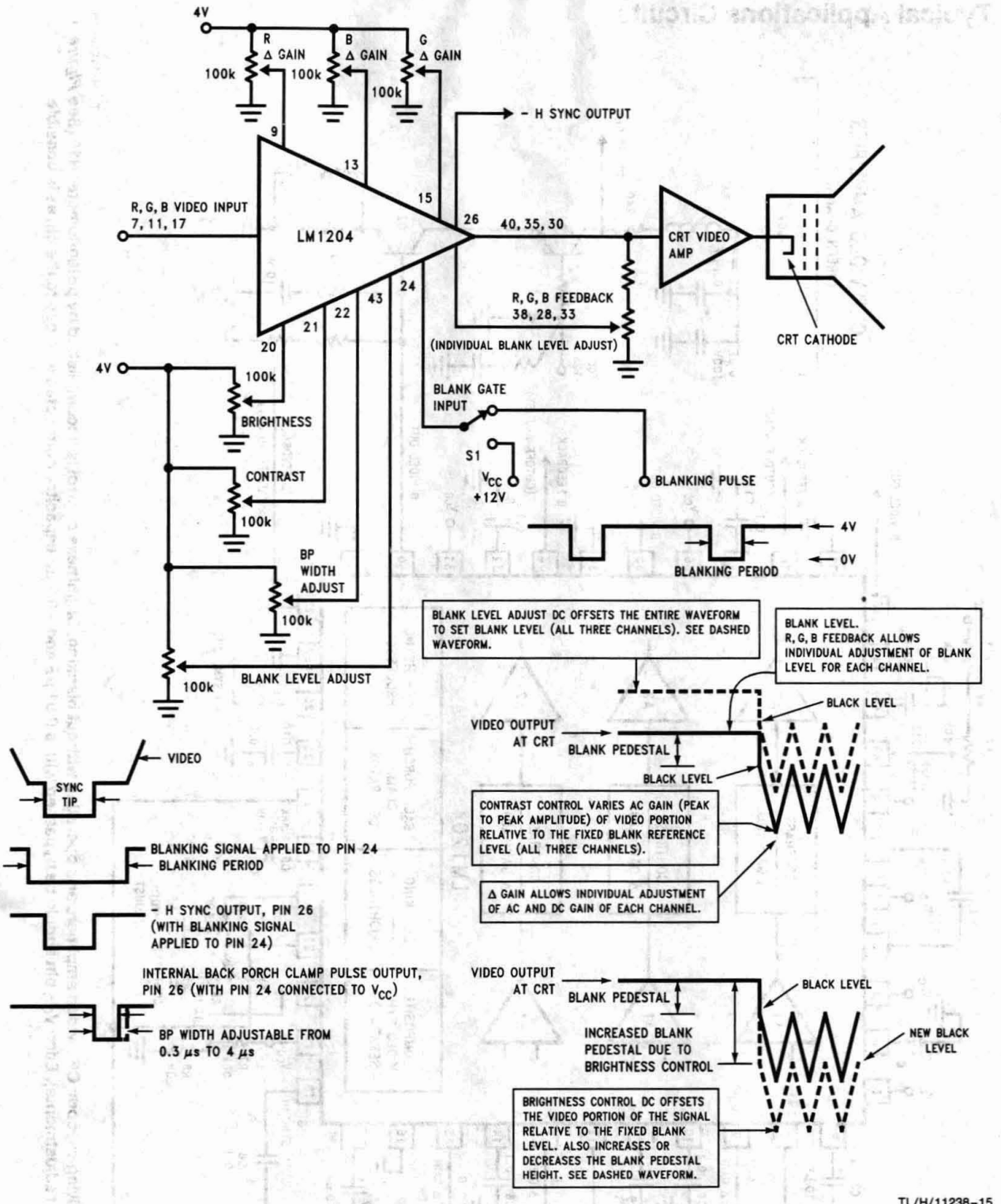

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FIGURE 5. LM1204 Adjustments with Blanking

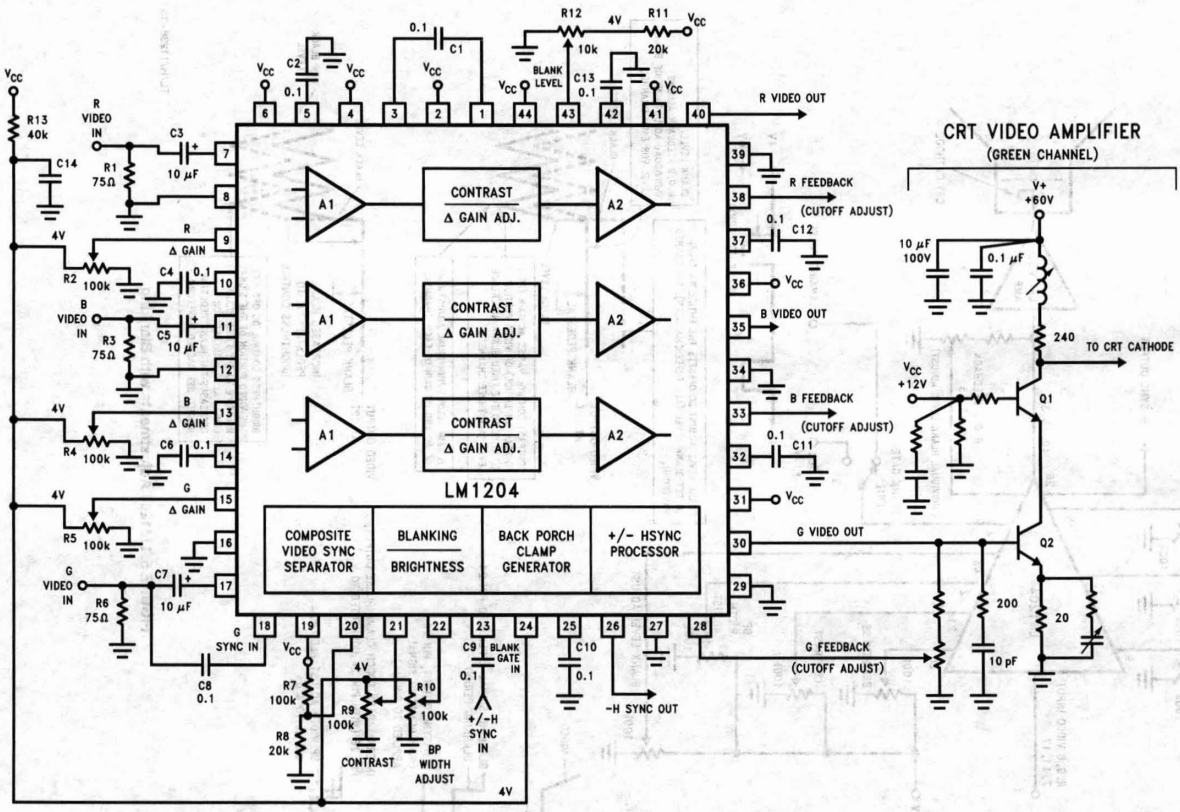

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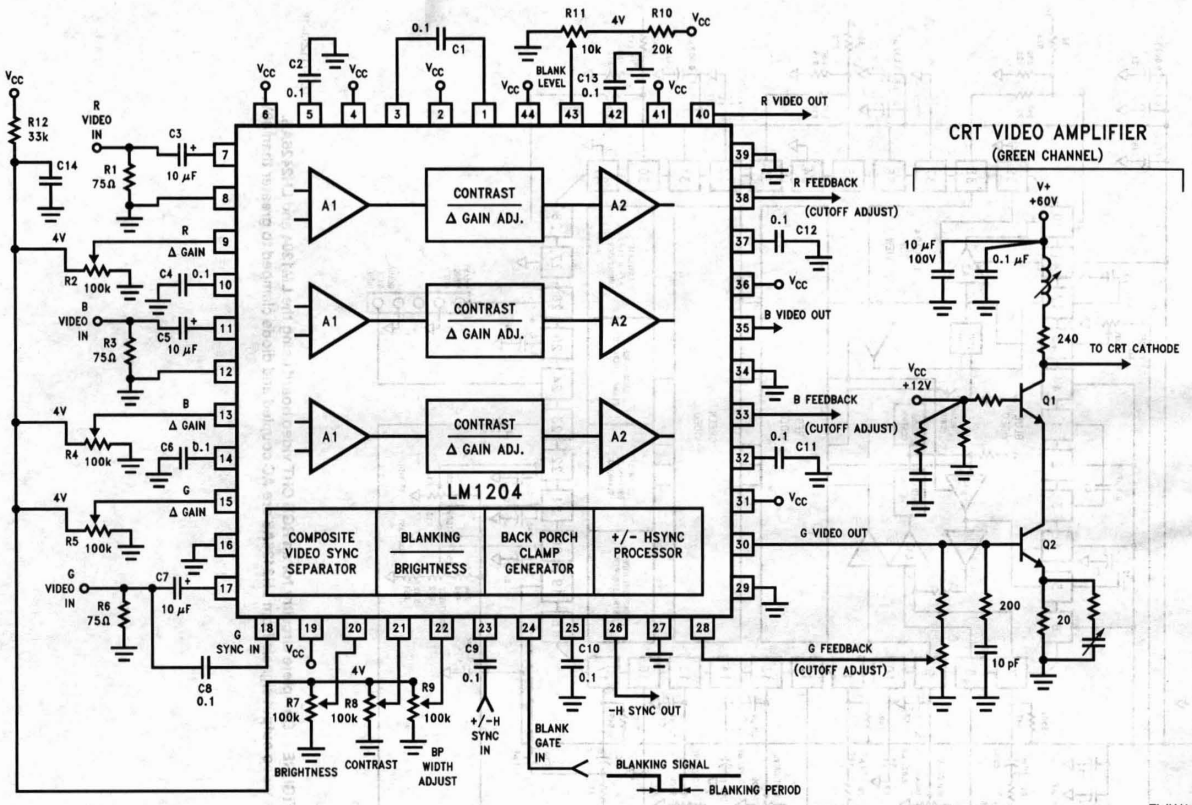
FIGURE 6. The LM1204 driving cascode CRT video amplifiers and operating without blanking. Brightness control is accomplished by potentiometer R12 (See *Figure 4* for explanation of adjustments). Each V_{CC} pin should be bypassed with a 0.01 µF and a 0.1 µF capacitor connected as close to the pin as is possible.



TL/H/11238–17

FIGURE 7. The LM1204 driving cascode CRT video amplifiers and operating with blanking. The video signal is level shifted to the user adjustable blank level during the blanking period. Brightness control DC offsets the video signal relative to the fixed blank level and is accomplished by potentiometer R7. See *Figure 5* for explanation of adjustments. Each V_{CC} pin should be bypassed with a 0.01 μF and a 0.1 μF capacitor connected as close to the pin as is possible.

Typical Applications Circuits (Continued)

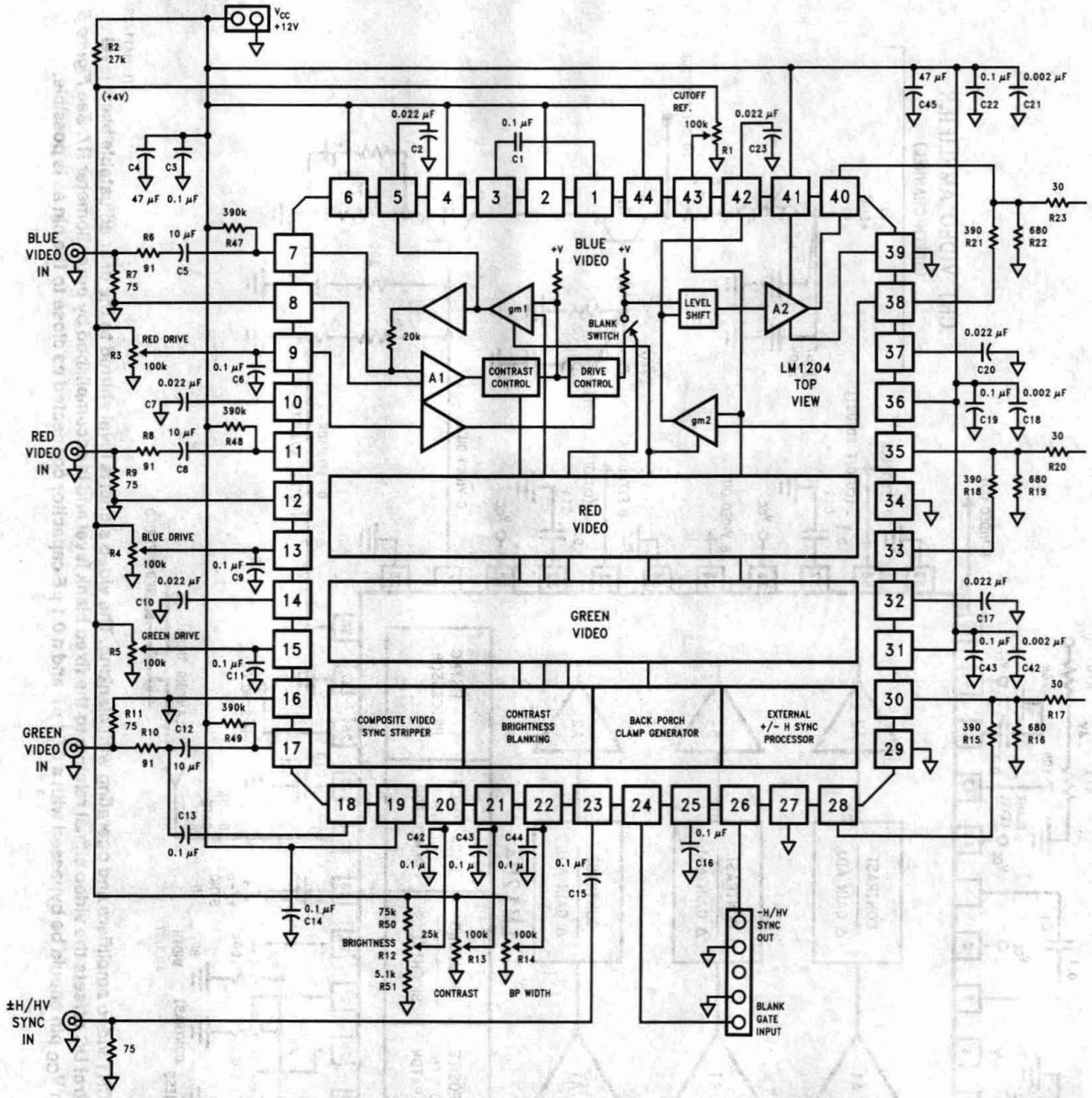


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FIGURE 8. Complete circuitry for an RGB CRT video board using the LM1204 and LH2426AS. The video output signals from LH2426AS are AC coupled and diode clamped to greater than 80V.

Typical Applications Circuits (Continued)

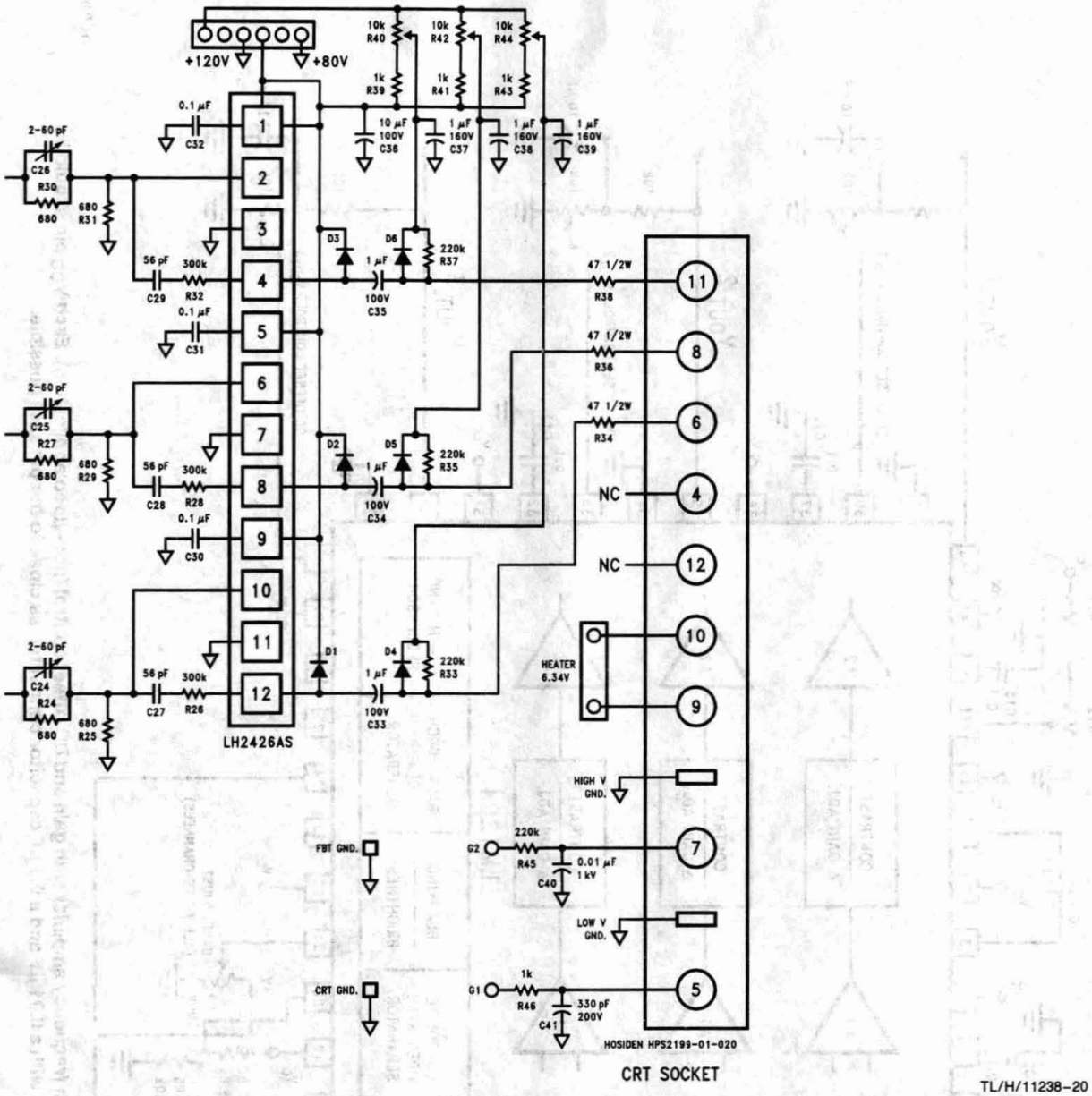

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FIGURE 8. (Continued)

Typical Applications Circuits (Continued)

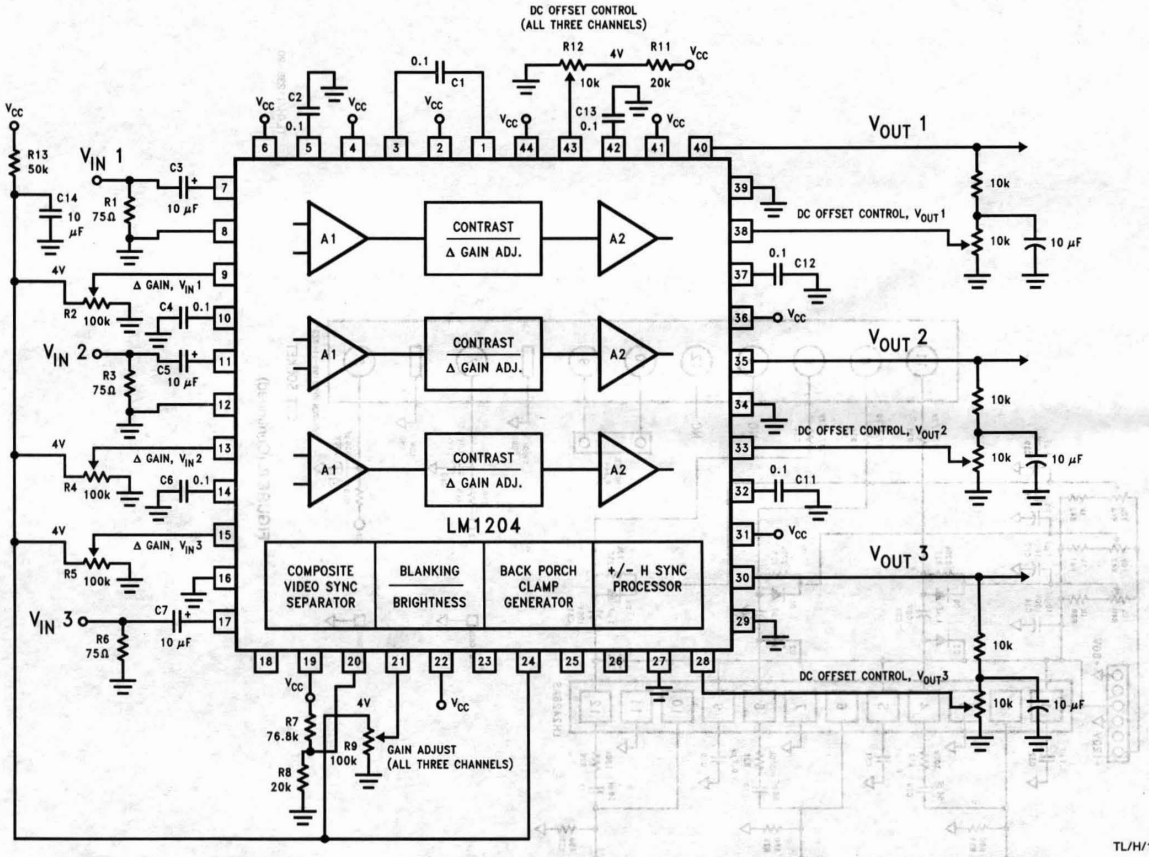

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FIGURE 9. Three channel high frequency amplifier with gain and DC offset control (non-video application). Each V_{CC} pin should be bypassed with a 0.01 µF and a 0.1 µF capacitor connected as close to the pin as is possible.

National Semiconductor

LM1205/LM1207
130 MHz/85 MHz RGB Video Amplifier System with Blanking

General Description

The LM1205/LM1207 is a very high frequency video amplifier system intended for use in high resolution RGB monitor applications. In addition to the three matched video amplifiers, the LM1205/LM1207 contains three gated single ended input black level clamp comparators for brightness control, three matched DC controlled attenuators for contrast control, and three DC controlled sub-contrast attenuators providing gain trim capability for white balance. All DC control inputs offer high input impedance and an operation range from 0V to 4V for easy interface to bus controlled alignment systems. The LM1205/LM1207 also contains a blanking circuit which clamps the video output voltage during blanking to within 0.1V above ground. This feature provides blanking capability at the cathodes of the CRT. A spot killer is provided for CRT phosphor protection during power-down.

Features

- Three wideband video amplifiers 130 MHz (LM1205) @ −3 dB (4 V_{PP} output)
- Matched (±0.1 dB or 1.2%) attenuators for contrast control
- Three externally gated single ended input comparators for cutoff and brightness control
- 0V to 4V, high input impedance DC contrast control (>40 dB range)
- 0V to 4V, high input impedance DC drive control for each video amplifier (−6 dB to 0 dB range)
- Spot killer, blanks output when V_{CC} < 10.6V
- Capable of 7 V_{PP} output swing (slight reduction in bandwidth)
- Output stage blanking
- Output stage directly drives most hybrid or discrete CRT drivers

Applications

- High resolution RGB CRT monitors
- Video AGC amplifiers
- Wideband amplifiers with gain and DC offset controls
- Interface amplifiers for LCD or CCD systems

Block and Connection Diagram

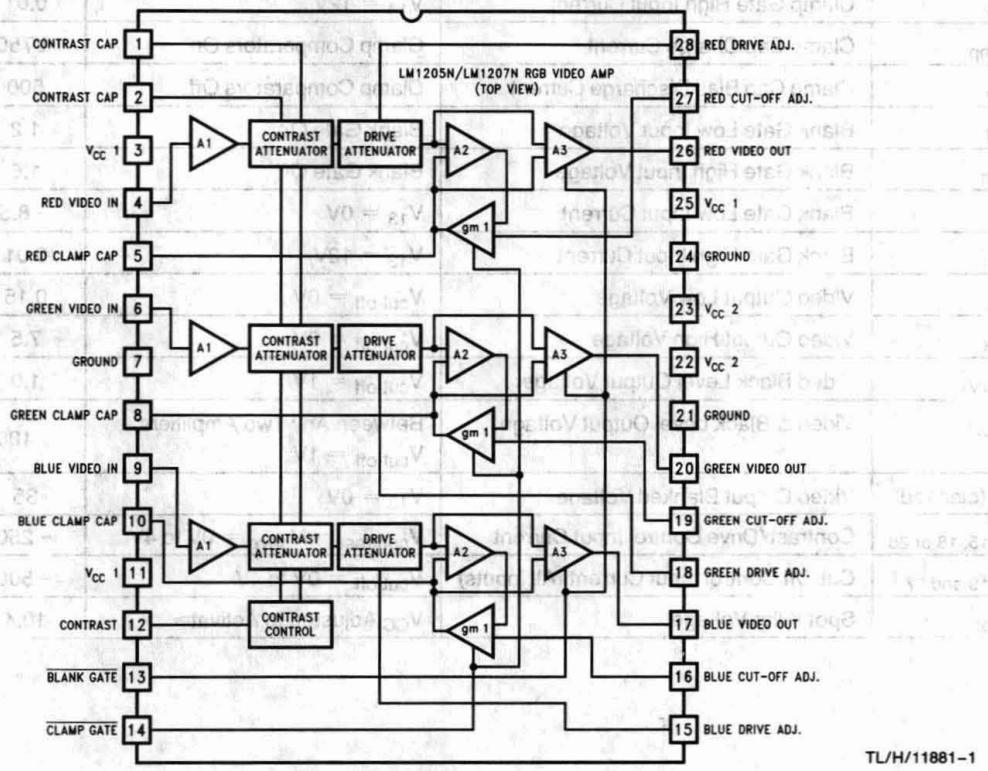

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FIGURE 1

Order Number LM1205N or LM1207N
See NS Package Number N28B

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC}) Pins 3, 11, 22, 23, 25 (Note 3)	15V
Peak Video Output Source Current (Any One Amp) Pins 17, 20 or 26	28 mA
Voltage at Any Input Pin (V_{IN})	$V_{CC} \geq V_{IN} \geq GND$
Power Dissipation (P_D) (Above 25°C Derate Based on θ_{JA} and T_J)	2.5W
Thermal Resistance (θ_{JA})	50°C/W
Junction Temperature (T_J)	150°C
ESD Susceptibility (Note 4)	2 kV
Pins 12, 13 and 14	1.9 kV
Storage Temperature	−65°C to 150°C
Lead Temperature (Soldering, 10 sec.)	265°C

Operating Ratings (Note 2)

Temperature Range	−20°C to 80°C
Supply Voltage (V_{CC})	$10.8V \leq V_{CC} \leq 13.2V$

DC Electrical Characteristics

See DC Test Circuit *(Figure 2)*, $T_A = 25°C$; $V_{CC1} = V_{CC2} = 12V$. $V_{12} = 4V$; $V_{14} = 0V$; $V_{cut\text{-}off} = 1.0V$; $V_{13} = 4V$; $V_{drive} = 4V$ unless otherwise stated.

Symbol	Parameter	Conditions	Typical (Note 5)	Limit (Note 6)	Units
I_S	Supply Current	$V_{CC1} + V_{CC2}$, $R_L = \infty$ (Note 7)	90	105	mA (max)
$V_{4, 6, 9}$	Video Amplifier Input Bias Voltage		2.8		V
R_{IN}	Video Input Resistance	Any One Amplifier	20		kΩ
V_{14l}	Clamp Gate Low Input Voltage	Clamp Comparators On	1.2	0.8	V (max)
V_{14h}	Clamp Gate High Input Voltage	Clamp Comparators Off	1.6	2.0	V (min)
I_{14l}	Clamp Gate Low Input Current	$V_{14} = 0V$	−1	−5	μA (max)
I_{14h}	Clamp Gate High Input Current	$V_{14} = 12V$	0.01	1.0	μA (max)
I_{clamp}	Clamp Cap Charge Current	Clamp Comparators On	±750	±500	μA (min)
I_{bias}	Clamp Cap Bias Discharge Current	Clamp Comparators Off	500		nA
V_{13l}	Blank Gate Low Input Voltage	Blank Gate On	1.2	0.8	V (max)
V_{13h}	Blank Gate High Input Voltage	Blank Gate Off	1.6	2.0	V (min)
I_{13l}	Blank Gate Low Input Current	$V_{13} = 0V$	−8.5	−11.0	μA (max)
I_{13h}	Blank Gate High Input Current	$V_{13} = 12V$	0.01	1.0	μA (max)
V_{OL}	Video Output Low Voltage	$V_{cut\text{-}off} = 0V$	0.15	0.5	V (max)
V_{OH}	Video Output High Voltage	$V_{cut\text{-}off} = 9V$	7.5	7	V (min)
$V_{O(1V)}$	Video Black Level Output Voltage	$V_{cut\text{-}off} = 1V$	1.0		V (Note 8)
$\Delta V_{O(1V)}$	Video Δ Black Level Output Voltage	Between Any Two Amplifiers, $V_{cut\text{-}off} = 1V$	±100		mV (max)
V_{OL}(blanked)	Video Output Blanked Voltage	$V_{13} = 0V$	35	70	mV (max)
$I_{12, 15, 18 \text{ or } 28}$	Contrast/Drive Control Input Current	$V_{contrast} = V_{drive} = 0V$ to 4V	−250		nA
$I_{16, 19 \text{ and } 27}$	Cut-Off Control Input Current (All Inputs)	$V_{cut\text{-}off} = 0V$ to 4V	−500		nA
V_{spot}	Spot Killer Voltage	V_{CC} Adjusted to Activate	10.4	10.8	V (max)

AC Electrical Characteristics

See AC Test Circuit *(Figure 3)*, T_A = 25°C; V_{CC1} = V_{CC2} = 12V. Manually adjust Video Output pins 17, 20, and 26 to 4V DC for the AC test unless otherwise stated. (Note 14)

Symbol	Parameter	Conditions		Typical (Note 5)	Limit (Note 6)	Units
$A_{V\ max}$	Video Amplifier Gain	V12 = 4V, V_{IN} = 635 mV_{PP}, V_{drive} = 4V		7.0	6.0	V/V (min)
				16.9	15.6	dB (min)
$\Delta A_{V\ 2V}$	Attenuation @ 2V	Ref: A_V max, V12 = 2V		−6		dB
$\Delta A_{V\ 0.25V}$	Attenuation @ 0.25V	Ref: A_V max, V12 = 0.25V		−40		dB
ΔDrive	Drive Control Range	V_{drive} = 0V to 4V, V12 = 4V		6		dB
$A_{V\ match}$	Absolute Gain Match @ A_V max	V12 = 4V, V_{drive} = 4V (Note 9)		±0.3		dB
$A_{V\ track1}$	Gain Change Between Amplifiers	V12 = 4V to 2V (Notes 9, 10)		±0.1		dB
THD	Video Amplifier Distortion	V_O = 1 V_{PP}, f = 10 kHz		1		%
f (−3 dB)	Video Amplifier Bandwidth (Notes 11, 12)	V12 = 4V, V_{drive} = 4V, V_O = 4 V_{PP}	LM1205	130		MHz
			LM1207	85		
t_r(Video)	Video Output Rise Time (Note 11)	V_O = 4 V_{PP}	LM1205	2.6		ns
			LM1207	4.3		
t_f(Video)	Video Output Fall Time (Note 11)	V_O = 4 V_{PP}	LM1205	3.6		ns
			LM1207	4.3		
V_{sep} 10 kHz	Video Amplifier 10 kHz Isolation	V12 = 4V (Note 13)		−70		dB
V_{sep} 10 MHz	Video Amplifier 10 MHz Isolation	V12 = 4V (Notes 11, 13)		−50		dB
t_r(Blank)	Blank Output Rise Time (Note 11)	Blank Output = 1 V_{PP}		7		ns
t_f(Blank)	Blank Output Fall Time (Note 11)	Blank Output = 1 V_{PP}		7		ns
t_{pw}(Clamp)	Min. Back Porch Clamp Pulse Width			200		ns

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur.

Note 2: Operating Ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.

Note 3: V_{CC} supply pins 3, 11, 22, 23, 25 must be externally wired together to prevent internal damage during V_{CC} power on/off cycles.

Note 4: Human body model, 100 pF discharged through a 1.5 kΩ resistor.

Note 5: Typical specifications are specified at +25°C and represent the most likely parametric norm.

Note 6: Tested limits are guaranteed to National's AOQL (Average Outgoing Quality Level).

Note 7: The supply current specified is the quiescent current for V_{CC1} and V_{CC2} with R_L = ∞, see *Figure 2's* test circuit. The supply current for V_{CC2} (pin 23) also depends on the output load. With video output at 1V DC, the additional current through V_{CC2} is 8 mA for *Figure 2's* test circuit.

Note 8: Output voltage is dependent on load resistor. Test circuit uses R_L = 390Ω.

Note 9: Measure gain difference between any two amplifiers. V_{IN} = 635 mV_{PP}.

Note 10: ΔA_V track is a measure of the ability of any two amplifiers to track each other and quantifies the matching of the three attenuators. It is the difference in gain change between any two amplifiers with the contrast voltage (V12) at either 4V or 2V measured relative to an A_V max condition, V12 = 4V. For example, at A_V max the three amplifiers' gains might be 17.1 dB, 16.9 dB and 16.8 dB and change to 11.2 dB, 10.9 dB, and 10.7 dB respectively for V12 = 2V. This yields the measured typical ± 0.1 dB channel tracking.

Note 11: When measuring video amplifier bandwidth or pulse rise and fall times, a double sided full ground plane printed circuit board without socket is recommended. Video amplifier 10 MHz isolation test also requires this printed circuit board. The reason for a double sided full ground plane PCB is that large measurement variations occur in single sided PCBs.

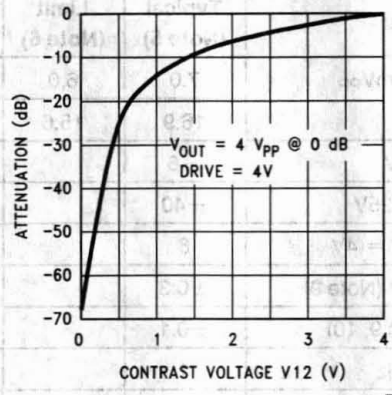
Note 12: Adjust input frequency from 10 MHz (A_V max reference level) to the −3 dB corner frequency ($f_{-3\ dB}$).

Note 13: Measure output levels of the other two undriven amplifiers relative to the driven amplifier to determine channel separation. Terminate the undriven amplifier inputs to simulate generator loading. Repeat test at f_{IN} = 10 MHz for $V_{sep\ 10\ MHz}$.

Note 14: During the AC tests the 4V DC level is the center voltage of the AC output signal. For example, if the output is 4 V_{PP} the signal will swing between 2V DC and 6V DC.

Typical Performance Characteristics V_{CC} = 12V, T_A = 25°C unless otherwise specified

Attenuation vs Contrast Voltage



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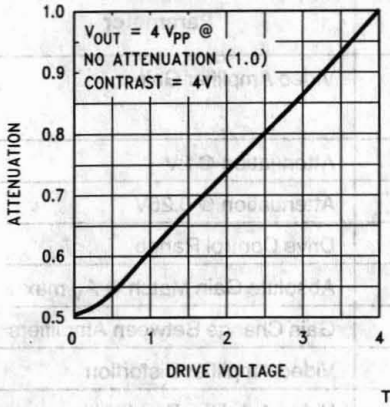
Attenuation vs Drive Voltage



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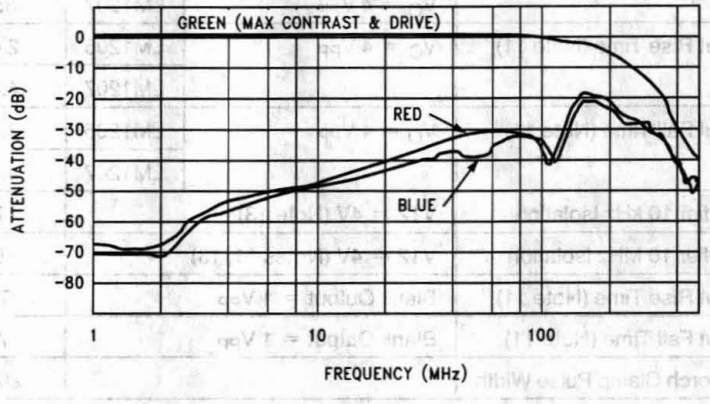
LM1205 Crosstalk vs Frequency



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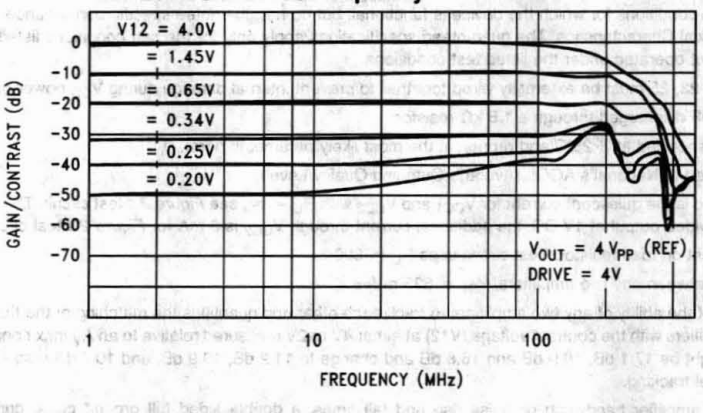
LM1205 Contrast vs Frequency



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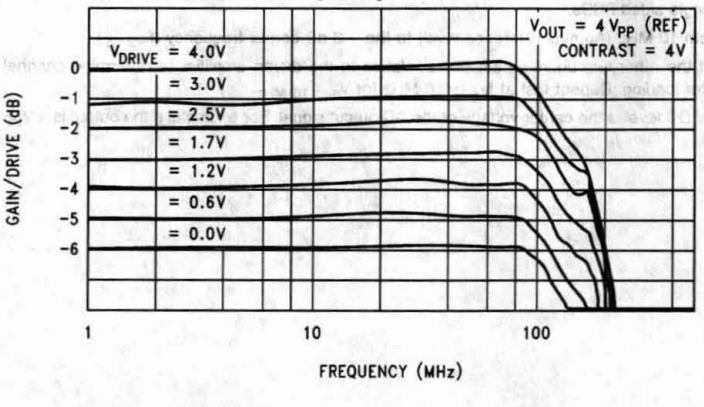
LM1205 Drive vs Frequency



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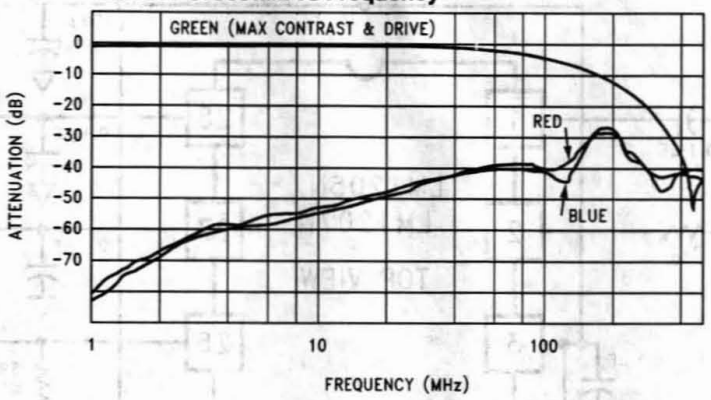
Typical Performance Characteristics V_{CC} = 12V, T_A = 25°C unless otherwise specified (Continued)

LM1207 Crosstalk vs Frequency



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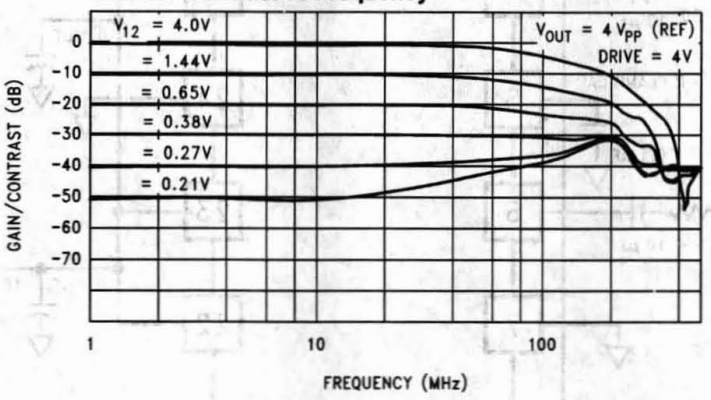
LM1207 Contrast vs Frequency



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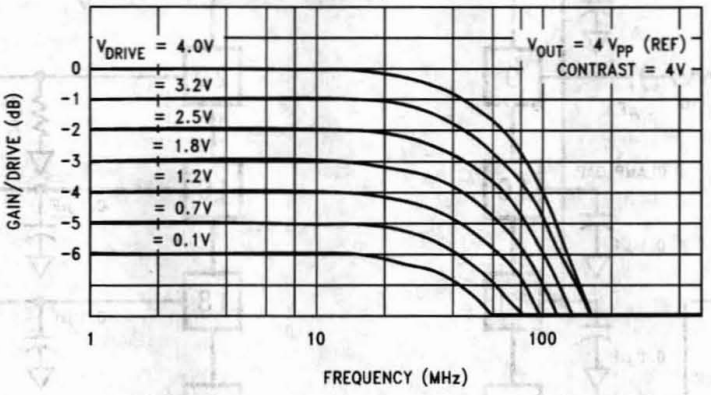
LM1207 Drive vs Frequency



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2

Applications Information

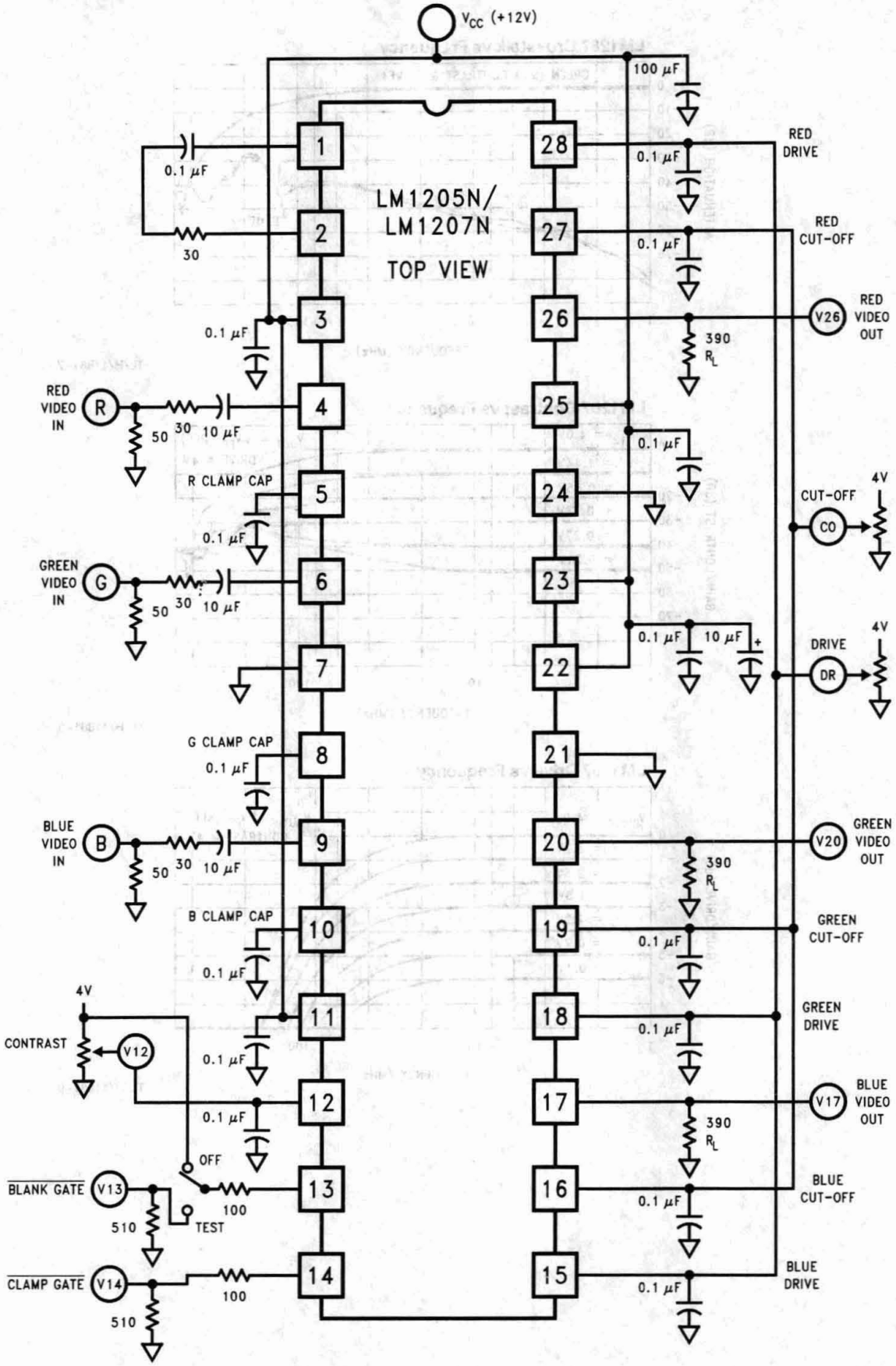

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FIGURE 2. LM1205N/LM1207N DC Test Circuit

Applications Information (Continued)

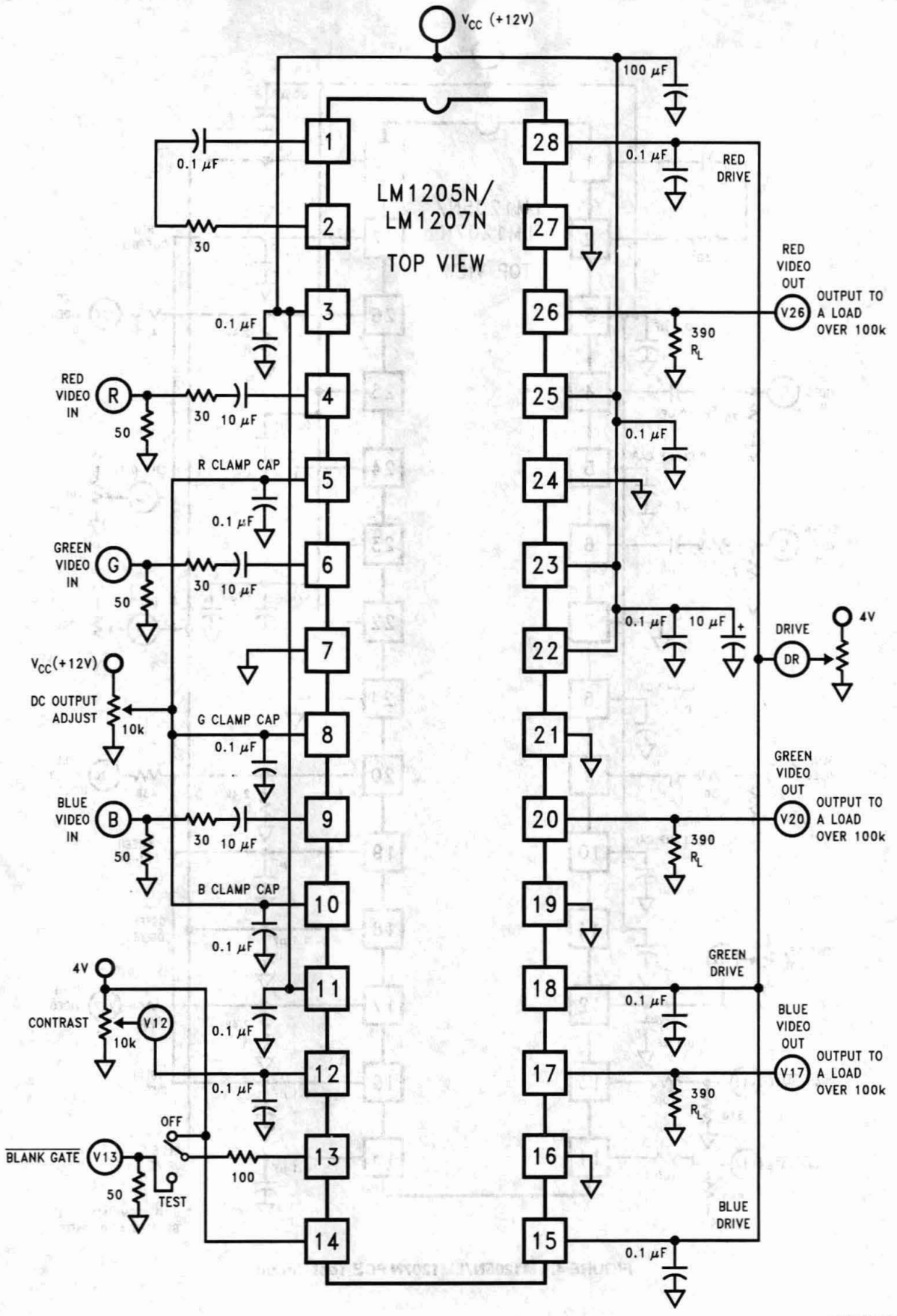

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FIGURE 3. LM1205N/LM1207N AC Test Circuit

Applications Information (Continued)

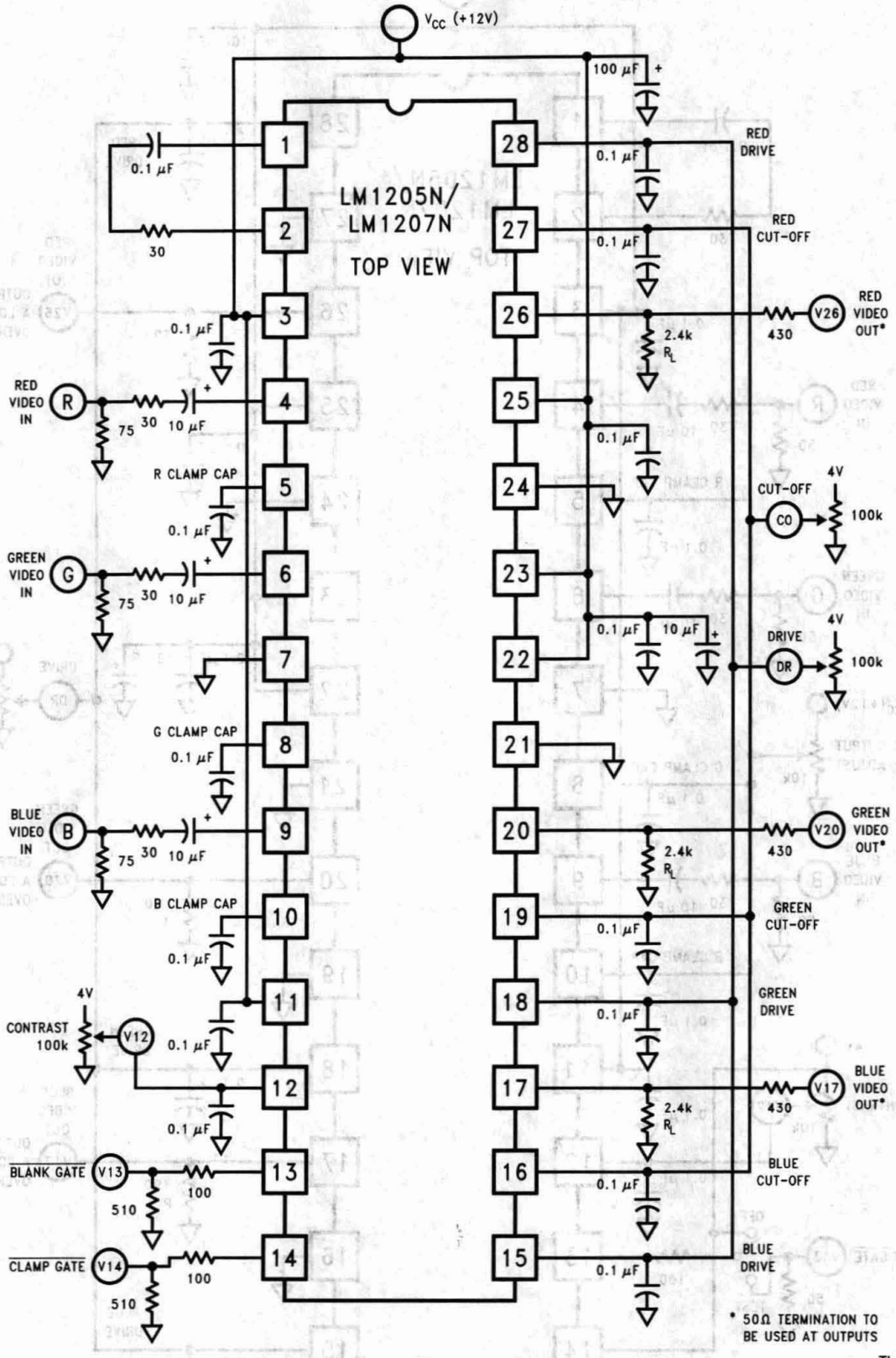

FIGURE 4. LM1205N/LM1207N PCB Test Circuit

Applications Information (Continued)

Figure 5 shows the block diagram of a typical analog RGB color monitor. The RGB monitor is used with CAD/CAM work stations, PC's, arcade games and in a wide range of other applications that benefit from the use of color display terminals. The RGB color monitor characteristics may differ in such ways as sweep rates, screen size, CRT color trio spacing (dot pitch), or in video amplifier bandwidths but will still be generally configured as shown in *Figure 5*. Separate horizontal and vertical sync signals may be required or they may be contained in the green video input signal. The video input signals are usually supplied by coax cable which is terminated into 75Ω at the monitor input and internally AC coupled to the video amplifiers. These input signals are approximately 1V peak to peak in amplitude and at the input of the high voltage video section, approximately 5V peak to peak. At the cathode of the CRT the video signals can be as high as 60V peak to peak. One important requirement of the three video amplifiers is that they match and track each other over the contrast and brightness control range. The *Figure 5* block labeled "VIDEO AMPLIFICATION WITH GAIN AND DC CONTROL" describes the function of the LM1205/LM1207 which contains the three matched video amplifiers, contrast control and brightness control. The LM1205/LM1207 also provides the capability to blank at the cathode of the CRT.

Functional Description

Figure 6 is a detailed block diagram of the green channel of the LM1205/LM1207 along with the recommended external components. The IC pin numbers are circled and all external components are shown outside the dashed line. The other two video channels are identical to the green channel, only the numbers to the pins unique to each channel are different. The input video is normally terminated into 75Ω. The termination resistor depends on the impedance of the coax cable being used, 75Ω being the most common impedance used in video applications. The video signal is AC coupled through a 10 μF capacitor to the input, pin 6. There is no standard for the DC level of a video signal, therefore the signal must be AC coupled to the LM1205/LM1207. Internal to the LM1205/LM1207 is a 2.8V reference, giving the input video an offset voltage of 2.8V. This voltage was selected to give the input video enough DC offset to guarantee that the lowest voltage of the video signal at pin 6 is far enough above ground to keep the LM1205/LM1207 in the active region. The 200Ω resistor at the input is for ESD protection and for current limiting during any voltage surge that may occur at the input, driving pin 6 above V_{CC}. The input video signal is buffered by −A1. In this circuit description an inverting amplifier is shown with a "−" (minus sign) in front of the amplifier designation. The output of −A1 goes to the contrast and drive attenuator sections.

The contrast and drive control sections are virtually identical. Both sections take a 0V to 4V input voltage, 4V giving the maximum gain for either the contrast or the drive. This is a high impedance input, allowing for an easy interface to 5V DACs. One may also use 100k potentiometers with no degradation in performance. The contrast control section is common to all three channels. It converts the input voltage at pin 12 to a couple of internal DC voltages that control the gain of the contrast attenuator. Referring to the Attenuation vs Contrast Voltage under typical performance characteristics note that a 4V control voltage results in no attenuation of the video signal. A 0.25V control voltage results in an attenuation of 40 dB. Again note that these internal control voltages are common to all three channels. To minimize crosstalk, these voltages go to pins 1 and 2. Minimizing crosstalk is done by adding the RC network shown in the block diagram *(Figure 6)*.

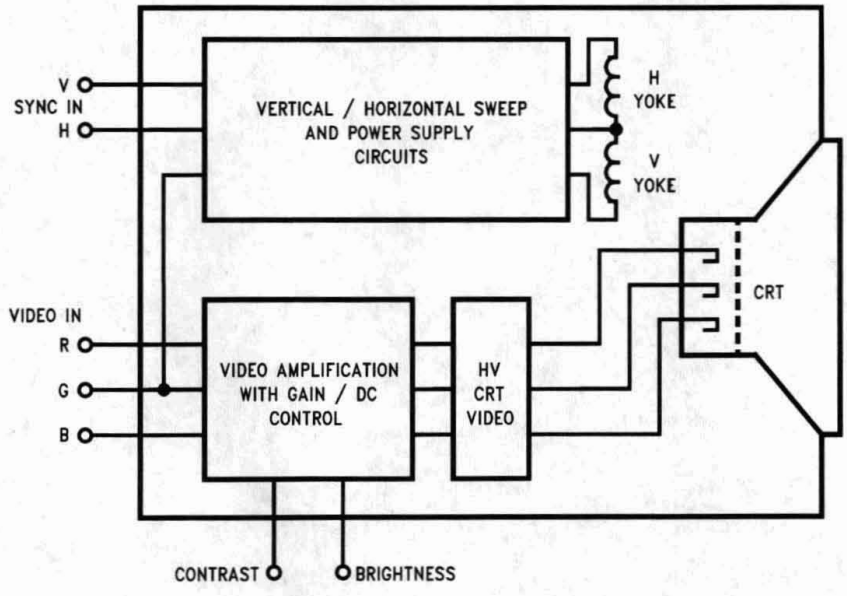

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FIGURE 5. Typical RGB Color Monitor Block Diagram

Functional Description (Continued)

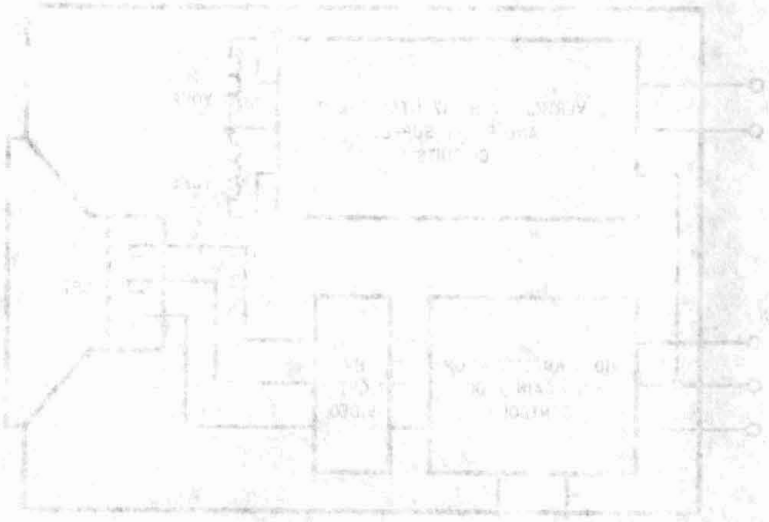
The 0V to 4V drive control signal comes in on pin 18. Each channel has its own drive section, therefore the crosstalk compensation needed for the contrast control voltages is not required for the drive control, thus no external pins for the drive control. The drive attenuator gives an attenuation range from 0 dB to −6 dB. A small gain adjustment range for the drive attenuator is desirable and intentionally designed because the drive is used only to balance the overall gain of each color channel, giving the correct color temperature on the CRT.

The output of the drive attenuator stage goes to A2, the amplifier in the DC restoration section. The video signal goes to the non-inverting input of A2. The inverting side of A2 goes to the output of gm1, the clamp comparator, and the clamp capacitor at pin 8.

During the back porch period of the video signal a negative going clamp pulse from pin 14 is applied to the clamp comparator, turning on the comparator. This period is where the black level of the video signal at the output of the LM1205/LM1207 is compared to the desired black level which is set at pin 19. *Figure 7* shows the timing of the clamp pulse relative to the video signal. The clamp capacitor is charged or discharged by gm1, generating the correction voltage needed at the inverting input of A2 to set the video output to the correct DC level. Removing the clamp pulse turns off gm1 with the correction voltage being maintained by the clamp capacitor during active video. Both the clamp pulse and the blank pulse at pin 13 are TTL voltage levels.

There are actually two output sections, −A3 and −A4. Both sections have been designed to be identical, except −A4 has more current drive capability. The output transistor shown is part of −A4, but has been shown separately so the user knows the configuration of the output stage. −A3 does not go to the outside world, it is used for feeding back the video signal for DC restoration. Its output goes directly to the inverting input of the clamp comparator via the voltage divider formed by the 500Ω and 4k resistors. −A4 will be close to the same output as −A3 and will temperature track due to the similar design of the two output stages. However, the current at the output of −A4 will be ten times the current at the output of −A3. To balance both outputs, a load resistance of 390Ω needs to be connected from pin 20, the green video output pin, to ground. Another input to −A4 is the blank pulse. When a negative going blank pulse is applied to pin 13, the output of the LM1205/LM1207 is driven to less than 0.1V above ground. Using the timing shown in *Figure 7* for the blank pulse, the output of the LM1205/LM1207 will be less than 0.1V during the inactive portion of the video signal. This is a "blacker than black" condition, blanking the CRT at the cathodes. By using the blank function of the LM1205/LM1207 no grid blanking is necessary. Note that the DC restoration is done by feeding back the video signal from −A3, but blanking is done at −A4. By using the two output stages, blanking can be done at the CRT cathodes, and at the same time activate the DC restoration loop.

V_{CC1} goes to pins 3, 11, and 25 (see *Figure 1*). These three pins are all internally connected. For proper operation of the LM1205/LM1207 it is necessary to connect **all** the V_{CC1} pins to the input power to the PCB and bypass each pin with a 0.1 μF capacitor. V_{CC2} is the input power at pins 22 and 23 for the three output stages. This is a separate power input from V_{CC1}, there are no internal connections between the two different power inputs. There must be a connection on the PCB between V_{CC1} and V_{CC2}. Pins 22 and 23 must be bypassed by a parallel connection of a 10 μF and 0.1 μF capacitors. The ground connections for the LM1205/LM1207 are at pins 7, 21, and 24. All three ground pins are internally connected, and these pins must also be connected externally to a good ground plane for proper operation of the LM1205/LM1207.



Functional Description (Continued)

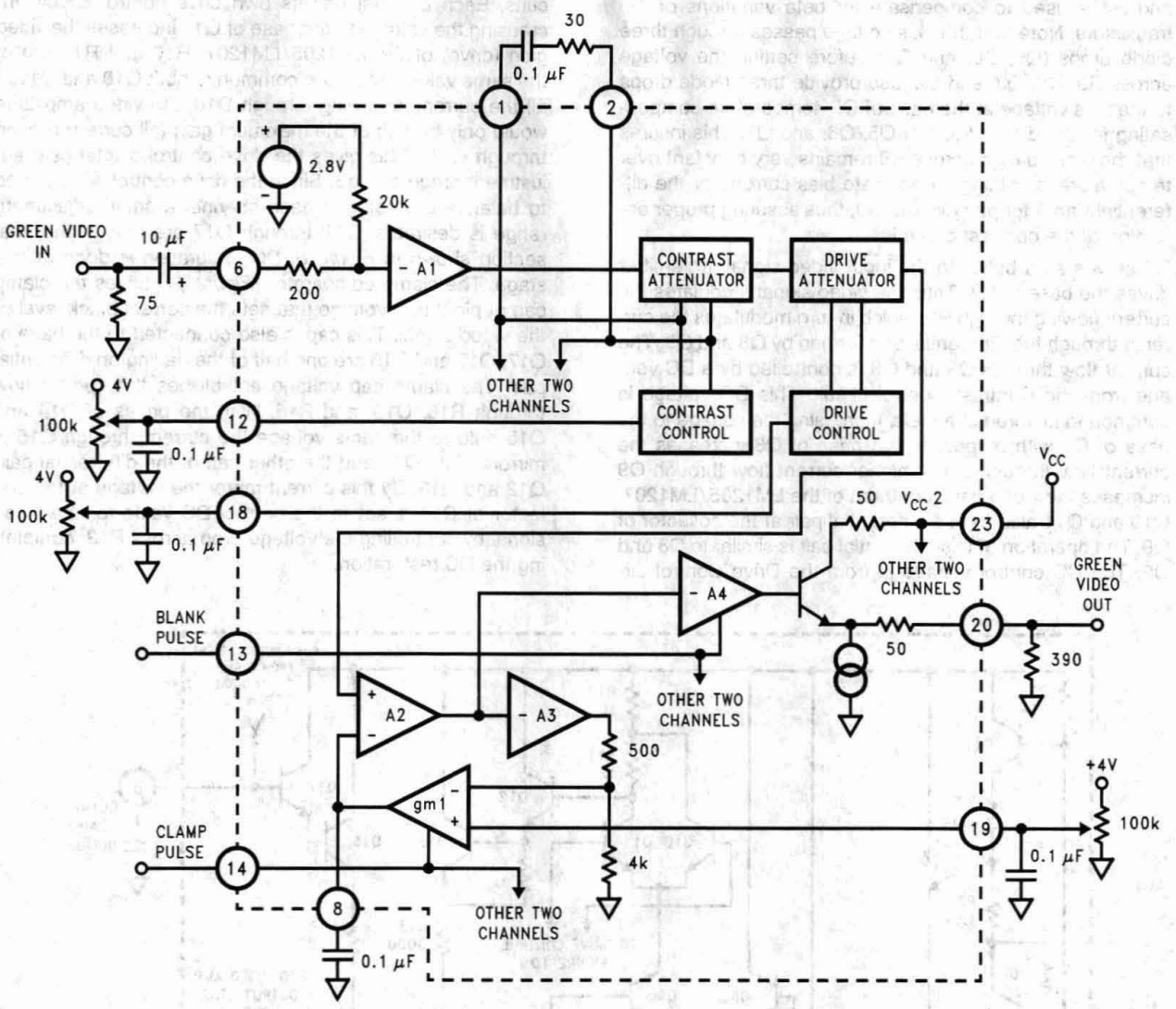


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FIGURE 6. Block Diagram of LM1205/LM1207 Video Amplifier

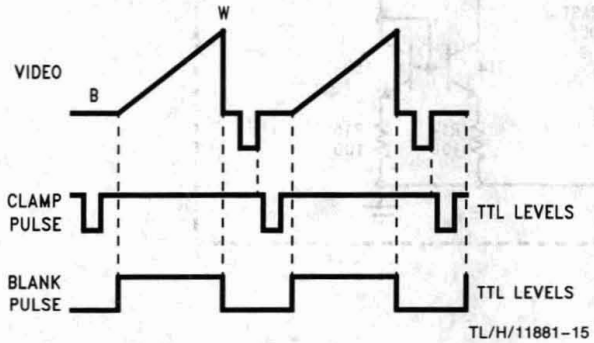

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FIGURE 7. Timing Diagram

Circuit Description

VIDEO AMPLIFIER INPUT STAGE

Figure 8 is a simplified schematic of one of the three video amplifiers input stage along with the recommended external components. The IC pin numbers are circled and all external components are shown outside the dashed line. The video input is applied to pin 6 via a 10 μF coupling capacitor and a 30Ω resistor. The resistor is added to limit the current through the input pin should an applied voltage surge rise above V_{CC} or drop below ground. The performance of the LM1205/LM1207 is not degraded by the 30Ω resistor. However, if EMI is a concern this resistor can be increased to well over 100Ω where the rise and fall times will start to become longer. DC bias to the input pin is provided by Q5 and its associated input circuitry. Z1 is a 5.6V zener that generates the input bias voltage. Q1 is a buffer to the zener reference voltage with 5.0V generated at its emitter. Q3 and Q4 are connected as diodes. Q2 is close to being a diode in this circuit. This configuration will give about 2.0V at the collector of Q2. R2 and R3 are a voltage divider, setting the base of Q5 to about 3.5V. This sets the emitter of Q5 to about 2.8V, the bias voltage of the video input. This bias voltage is necessary to assure that the entire video signal stays within the active operating region of the LM1205/LM1207. The bias voltage goes through R6, a 20k resistor, to the video input at pin 6. R4 and R6 are of the same value

Circuit Description (Continued)

and R4 is used to compensate for beta variations of the transistors. Note that the bias voltage passes through three diode drops (Q5, Q6, and Q7) before setting the voltage across R9. Q2, Q3, and Q4 also provide three diode drops to the bias voltage at the base of Q5, temperature compensating for the diode drops of Q5, Q6, and Q7. This insures that the bias voltage across R9 remains very constant over temperature, providing an accurate bias current for the differential transistor pair Q8 and Q9, thus assuring proper operation of the contrast control.

Q6 serves as a buffer to the input video signal. Its emitter drives the base of Q7. Thus the video signal modulates the current flowing through R9, which in turn modulates the currents through the differential pair formed by Q8 and Q9. The current flow through Q8 and Q9 is controlled by a DC voltage from the Contrast Control circuit. This DC voltage is common to all three channels. Increasing the voltage to the base of Q9 with respect to the base of Q8 increases the current flow through Q9. A higher current flow through Q9 increases the video gain (contrast) of the LM1205/LM1207. Q10 and Q11 also form a differential pair at the collector of Q9. The operation of this differential pair is similar to Q8 and Q9. The DC control voltage is from the Drive Control circuits. Each channel has its own drive control circuit. Increasing the voltage to the base of Q11 increases the video gain (drive) of the LM1205/LM1207. R10 and R11 are of the same value, but R10 is common to both Q10 and Q11. If all the current is flowing through Q10, the video amplitude would only be half of the maximum gain (all current flowing through Q11). This gives the drive control a total gain adjustment range of 6 dB. Since the drive control is only used to balance the color of each channel a small adjustment range is desirable. Q12 through Q17 are part of the final section shown in *Figure 8*. DC restoration is done at this stage. The clamp comparator *(Figure 11)* drives the clamp cap at pin 8 to a voltage that sets the correct black level of the video signal. This cap is also connected to the base of Q17. Q17 and Q16 are one half of the darlington differential pair. The clamp cap voltage establishes the current flow through R16, Q15, and R15. With the bases of Q14 and Q15 held to the same voltage the current through Q15 is mirrored into Q14 and the other half of the differential pair, Q12 and Q13. By this current mirror the voltage at the collector of Q14 is set to the correct DC value for the video signal by controlling the voltage drop across R13, completing the DC restoration.

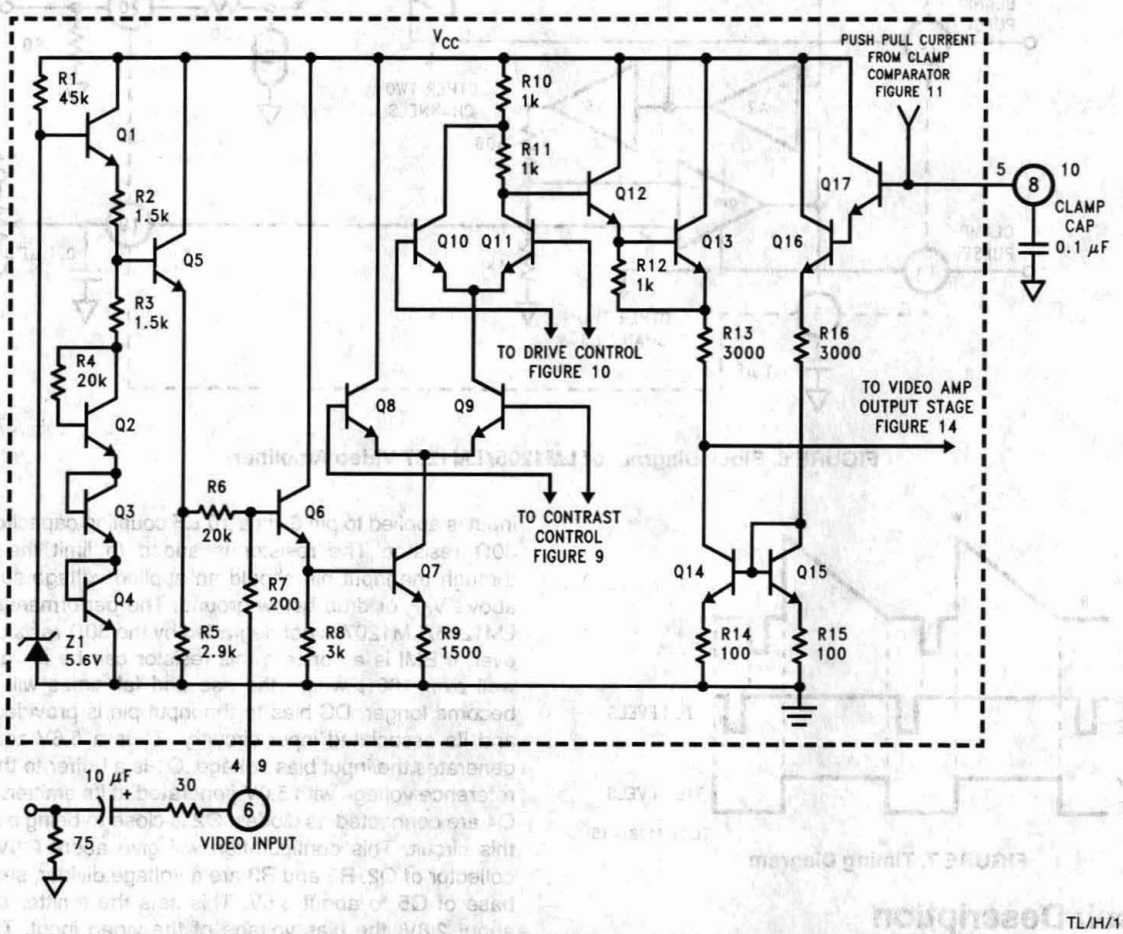

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FIGURE 8. Simplified Schematic of LM1205/LM1207 Video Amplifier Input Stage

Circuit Description (Continued)

CONTRAST CONTROL

Figure 9 is a simplified schematic of the Contrast Control circuit. The output of this circuit is common to all three channels. A reference voltage is generated by Z2, Q34, Q35, R30, and R31. Q36, Q39, and Q41 are all current sources that are controlled by the reference voltage. The contrast signal has a 0V to 4V range with its input at pin 12. R32 is used for current limiting any voltage surge that may occur at pin 12. Note that the input stage (Q37, Q38, and Q42) are all PNP transistors. This configuration is necessary for operation down to near ground. At Q44 the input voltage is converted to a current by R33. The input stage will apply the same voltage across R33 as is applied at the input and with no temperature variations from the transistors. Q37 is connected to a current source (Q36) to keep a constant current flow through Q37 and a predictable diode voltage for the base-emitter of Q37. Q40 is connected as a diode and is biased by the current source Q39. The current through Q40 is mirrored into Q43, giving a current bias for Q42. Again this is done to give a predictable diode voltage for Q42. Q41 is a current source for both Q38 and Q42. With the current through Q42 already established, the rest of the current from Q41 flows through Q38. As one can see the input voltage is accurately reflected across R33 with no temperature coefficients from the input stage of the contrast control circuit.

Pin 1 of the contrast control output is held at a constant voltage two diode drops below $\frac{1}{2}V_{CC}$. To generate this reference the base of Q51 is held at exactly $\frac{1}{2}V_{CC}$. R44 and R45 form a voltage divider. With both Q53 and Q54 connected as diodes the voltage at the junction of R44 and R45 is $\frac{1}{2}V_{CC}$ plus one diode drop. Q52 is a buffer to this reference voltage, generating exactly $\frac{1}{2}V_{CC}$ at its emitter. Q51 is used to drive the bases of Q49 and Q50 to one diode drop below the reference voltage. Q50 is used to further buffer the reference voltage to the base of Q9 (see *Figure 8*) and the corresponding transistors in the other channels. Q48 is used to bias the collector of Q49 to $\frac{1}{2}V_{CC}$, the same voltage as the collector of Q47 when the differential pair is balanced. This keeps the characteristics of Q47 and Q49 well matched. Going back to Q44 and R33; these parts set up a current source that varies the current through R36. With a 2V contrast voltage the differential pair is balanced, meaning that the voltage drop across R36 is $\frac{1}{2}V_{CC}$. Q45 buffers the voltage at R36, driving the bases of Q46 and Q47. Q46 further buffers the voltage, driving the base of Q8 (see *Figure 8*) and the corresponding transistors in the other two channels. In the balanced condition the voltage at pin 2 will also be two diode drops below $\frac{1}{2}V_{CC}$, giving a well balanced drive to the differential pair consisting of Q8 and Q9 in the video amplifier input stage. With the contrast voltage set to 0V, the voltage at pin 2 will increase by about 400 mV to 500 mV. A 4V contrast voltage decreases the voltage at pin 2 by about 400 mV to 500 mV from the balanced condition. Reviewing *Figure 8* note that decreasing the voltage at pin 2 will decrease the current flow through Q8. Thus the current flow through Q9 increases, increasing the gain of the LM1205/LM1207. So increasing the contrast control voltage at pin 12 increases the gain of the LM1205/LM1207. The contrast control voltage from Q46 and Q50 is common to all three channels. To minimize crosstalk it is necessary to add a decoupling capacitor of 0.1 μF across R37 and R40. Since this can only be done externally, these two nodes are brought out to pins 1 and 2. The 30Ω resistor is added in series with the capacitor for improving stability. To prevent a destructive current surge due to shorting either pins 1 or 2 to ground R38 was added for current limiting.

DRIVE CONTROL

Figure 10 is a simplified schematic of the Drive Control circuit. Each channel has its own drive control circuit. This circuit is almost identical to *Figure 9*, the contrast control circuit. It will be easier to cover the differences between the two circuits instead of going through virtually the same circuit description. Note that the input stage is **exactly** the same. The generation of the reference voltage at the right hand side of *Figure 10* is slightly different than the circuit in *Figure 9*. In the drive control circuit the reference voltage at the base of Q72 is to be $\frac{2}{3}V_{CC}$. In the contrast control circuit the reference voltage at the base of Q51 was to be $\frac{1}{2}V_{CC}$. To generate the $\frac{2}{3}V_{CC}$ R57 and R58 form a 2 to 1 voltage divider. With the two to one ratio it is now necessary to have three transistors connected as diodes, which are Q74, Q75, and Q76. Q73 is the buffer for this voltage divider and its emitter is exactly $\frac{2}{3}V_{CC}$ with temperature compensation. R52 and R53 also differ from their corresponding resistors in *Figure 9*, R36 and R39. The value difference is so the base of Q66 is also at $\frac{2}{3}V_{CC}$ when the input drive voltage is at 2V. R38 in *Figure 9* was needed for current limiting at the output pins. Since each channel has its own drive control circuit no filtering is required, eliminating the need for external pins. With no external pins no current limiting is necessary, thus the 1k resistor is not used in the drive control circuit.

Circuit Description (Continued)

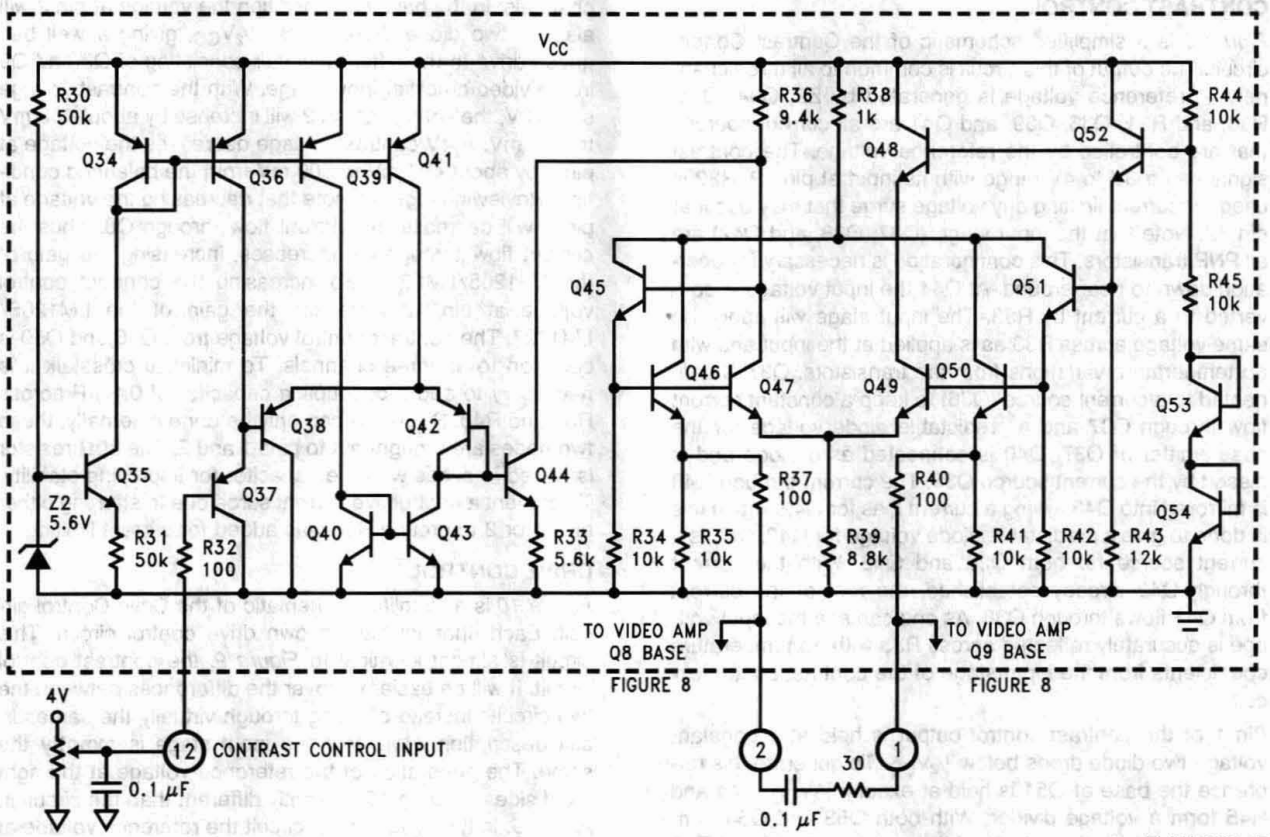

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FIGURE 9. Simplified Schematic of LM1205/LM1207 Contrast Control

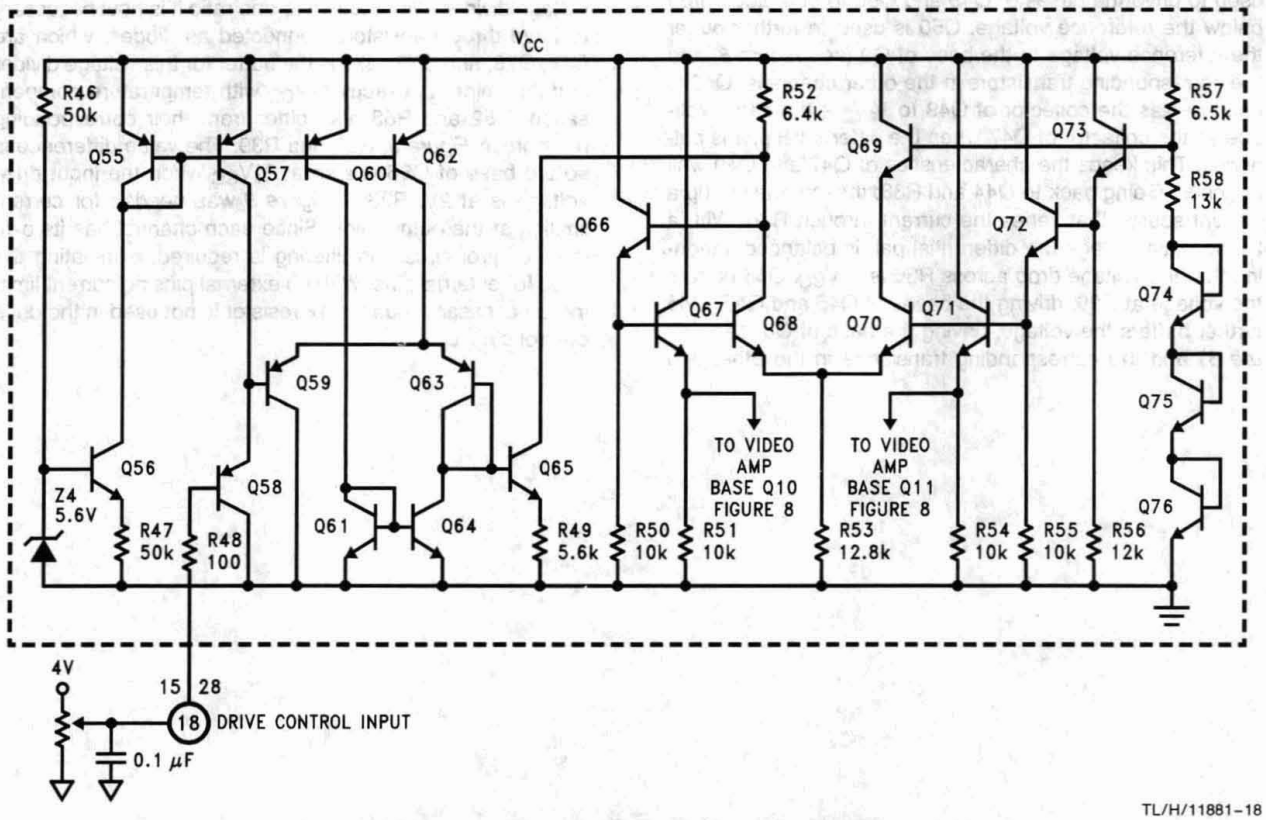

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FIGURE 10. Simplified Schematic of LM1205/LM1207 Drive Control

Circuit Description (Continued)

CLAMP COMPARATOR CIRCUIT

Figure 11 is a simplified schematic of the clamp comparator circuit. Q85 and its input transistors, Q81 and Q82 are one half of the differential pair. The base of Q81 is connected to pin 19 via R62. This is the positive input to the comparator. Q88 and its input transistors, Q90 and Q91 are the other half of the differential pair. The base of Q92 is connected to the junction of R19 and R20 in *Figure 14* via R73. This is the negative input to the comparator. R73 is included only to match the input characteristics of the positive input, which requires the 100Ω resistor. The negative comparator input is the feedback from the output stage as briefly described in the block diagram and covered in more detail in the output stage circuit description. Q86 is the current source for the differential pair. It is turned on and off by the output of the clamp gate circuit *(Figure 12)*. Q102 of the clamp gate circuit has a current flow of about 225 μA when it is turned on. This current is mirrored into Q86. Assume that the inputs to the comparator are equal, making the differential pair balanced. In this condition Q85 and Q88 each have a current flow of 113 μA. Looking at the Q85 side of the circuit, Q84 will also have 113 μA of current flow. Q80 is set up as a current mirror to Q84, but its emitter resistor is one fourth the emitter resistance of Q84. Thus the current flow for Q80 is four times the current flow thru Q84, or 450 μA. Q83 has been added to help drive the base of Q80, increasing the accuracy of the current mirror. The collector of Q80 directly charges the capacitor as a current source of 450 μA. R65 is added to discharge the charge stored in the bases of Q80 and Q84. This is necessary to quickly turn off the current charge of the clamp capacitor as the comparator section is turned off. Q87, Q89, and Q90 work in exactly the same way. However, the collector of Q91 drives another current mirror with the 450 μA. This current flows thru Q78. Q77 is a current mirror with Q78, thus 450 μA also flows thru Q77. Q79 has been added to help drive the base of Q77, again adding to the accuracy of the current mirror. Since Q77 is on the ground side of the circuit it discharges the clamp capacitor with 450 μA. In this balanced condition the charge and discharge current are equal, thus the voltage across the clamp capacitor remains unchanged.

Going back to the input stages, note that both inputs, Q81 and Q92, are driven by a 50 μA current source. This keeps both transistors turned on even when the differential pair, Q85 and Q88, is turned off. Q82 and Q90 are added to help drive the bases of Q85 and Q88 respectively. R64 and R72 are added to help discharge the charge stored in the bases of Q85 and Q88 as these two transistors are turned off. Since the input stage remains active the differential pair is quickly turned off. The comparator can also be more quickly turned on with the input stages remaining active. R67 is used to assure that the potential difference across the differential pair is minimal during turnoff. Without R67 there could be a little extra charge or discharge of the clamp capacitor during turnoff, creating an error in the black level of the video signal. Now assume that the input to pin 19 is slightly higher than the reference voltage to the negative input of the comparator. The voltage at the base of Q85 is now higher than the base of Q88. This creates an increased current flow thru Q85 and an equal decrease of current flow thru Q88. This current change is multiplied by four in the increase of current flow thru Q80. Likewise the current flow thru Q77 and Q91 is decreased by four times the current change in Q88. In the extreme case the current flow thru Q80 can increase to 900 μA and there would be no current flow thru Q77. Q80 does charge the clamp capacitor, thus the voltage across the capacitor will increase. The above is all reversed when the input to Q92 rises above the input level of Q81. If the base of Q86, the current source to the differential pair, is forced close to ground, then there is no current flow thru Q86 and the differential pair, Q85 and Q88. With the current flow thru the differential pair set the zero, all the current mirrors would also have no current flow. Thus the voltage on the camp capacitor would remain constant, the desired result during active video.

Circuit Description (Continued)

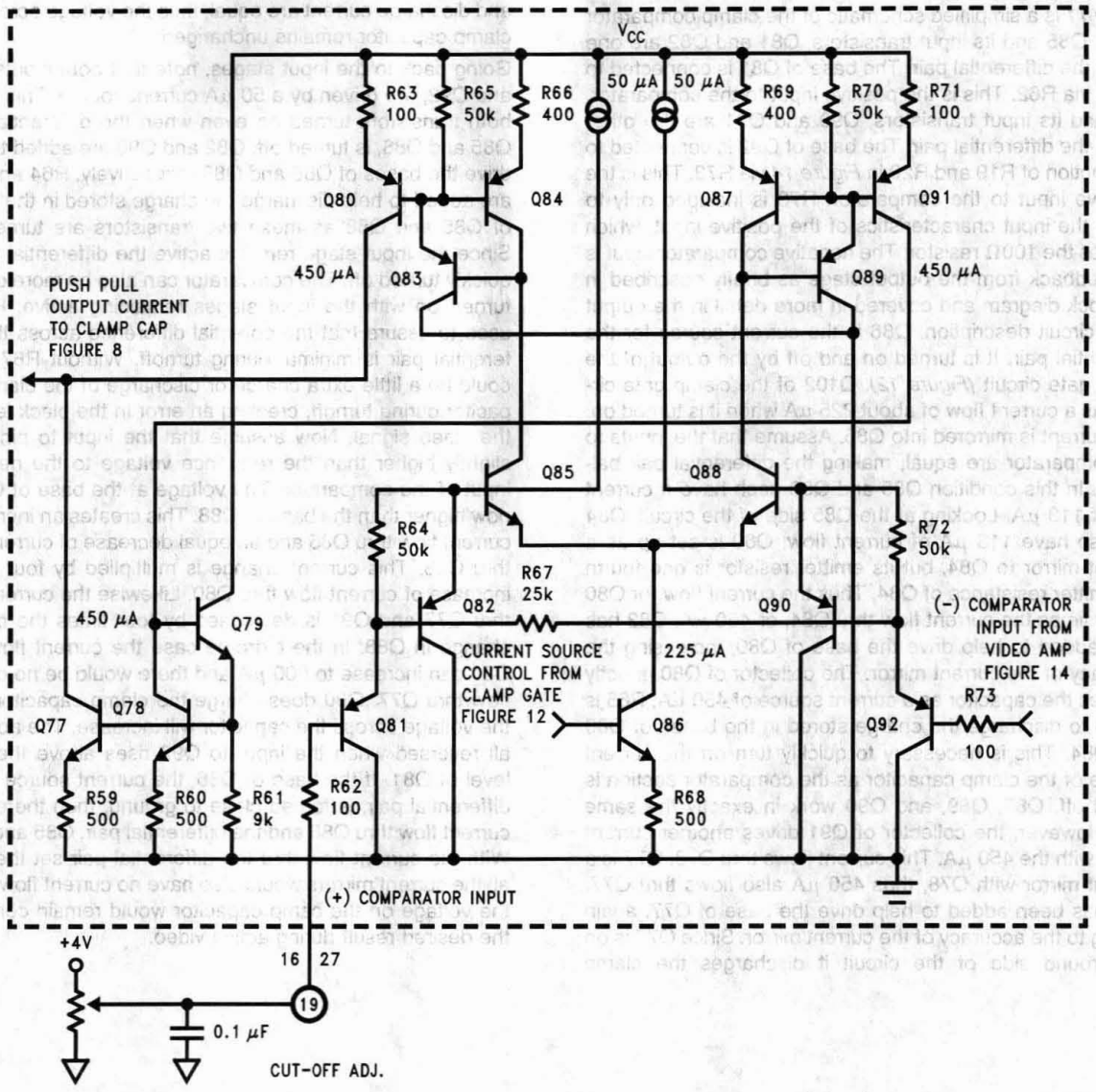

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FIGURE 11. Simplified Schematic of LM1205/LM1207 Clamp Comparator Circuit

CLAMP GATE CIRCUIT

Figure 12 is a simplified schematic of the Clamp Gate circuit. A voltage reference is setup by Z3 and by Q104 and Q105 connected as diodes, generating a 7V base drive to Q94, Q99 and Q101. Q94 is used to bias the input stage. This stage is designed to accept TTL levels at pin 14. Q95 and Q97 form a differential pair. The base of Q97 is set to 2.1V by Q99 driving the voltage divider formed by R77 and R78. In a balanced condition the base of Q95 is also at 2.1V. Q96 is connected as a diode and the current flow thru it is mirrored into Q98. Also the input to pin 14 would be one diode drop below 2.1V, or around 1.4V. R74 is added to the input for current limiting during any possible voltage surge at pin 14. With no resistors at the emitters of Q96 and Q98 this circuit will quickly switch. Below 1.4V (1.2V typical) Q95 is turned on and Q97 is turned off. Above 1.4V (1.6V typical) Q97 is turned on and Q95 is turned off. With Q97 turned on Q100 is also turned on. This pulls the current thru R79 to ground, turning off Q102 and Q103. Remember Q102 is a current mirror to Q86 in the clamp comparator. With Q102 turned off, the clamp comparator is also turned off. When the input signal goes below 1.2V, Q97 and Q100 will be turned off. This allows Q102 to turn on, turning on the clamp

Circuit Description (Continued)

comparators of the three video channels. Q103 is added to help drive the base of Q86 in the clamp comparator, increasing the accuracy of the current mirror. Q101 drives R79 and R80. This sets the current thru Q102, thus setting the current thru Q86 of the clamp comparator.

BLANK GATE CIRCUIT

Figure 13 is a simplified schematic of the Blank Gate circuit. With the exception of the simple output stage and the spot killer circuit, this circuit is almost identical to the clamp gate circuit. The only difference is that the output stage is driven from the opposite side of the differential pair. Thus Q111 is connected as a diode instead of Q109. With the input at pin 13 at a low level Q108 is turned on, also turning on Q29, the output transistor. Q29 is part of the blanking circuit in the output stage shown in *Figure 14*. When Q29 is turned on the output is clamped to a blanking level that is "blacker than black", allowing blanking to be done on the cathodes of the CRT.

The spot killer circuit is used to force the outputs of the LM1205/LM1207 into blanking when the V_{CC} drops below 10.6V. Forcing the outputs to a blacker-than-black level will drive the cathode driver stage well above the black level, cutting off the beam current in the CRT. This prevents the bright spot from occurring when the monitor is turned off, preserving the phosphor of the CRT. The CRT will also have its beam current cut off during the time the monitor is first turned on. This is not a critical period for the CRT since the filaments have not warmed up to generate a current flow.

The comparator along with R89, R90, and Q115 all form the spot killer circuit. Q115 acts the same as Q106. When Q115 has a high signal at its base it is turned off and the outputs of the LM1205/LM1207 are in the normal operating mode. A low signal at the base of Q115 turns on this transistor, blanking the outputs of the LM1205/LM1207. Q115 is driven by the output of the comparator. The inverting input of the comparator is connected to an internal 1.2V reference. The non-inverting side is connected to a resistor divider network, R89 and R90. When V_{CC} is above 10.6V the non-inverting input is above the 1.2V reference, therefore the output of the comparator is high. This high output turns off Q115. Once the V_{CC} drops below 10.6V the comparator's output goes low, turning on Q115 which forces the outputs into the blanking mode.

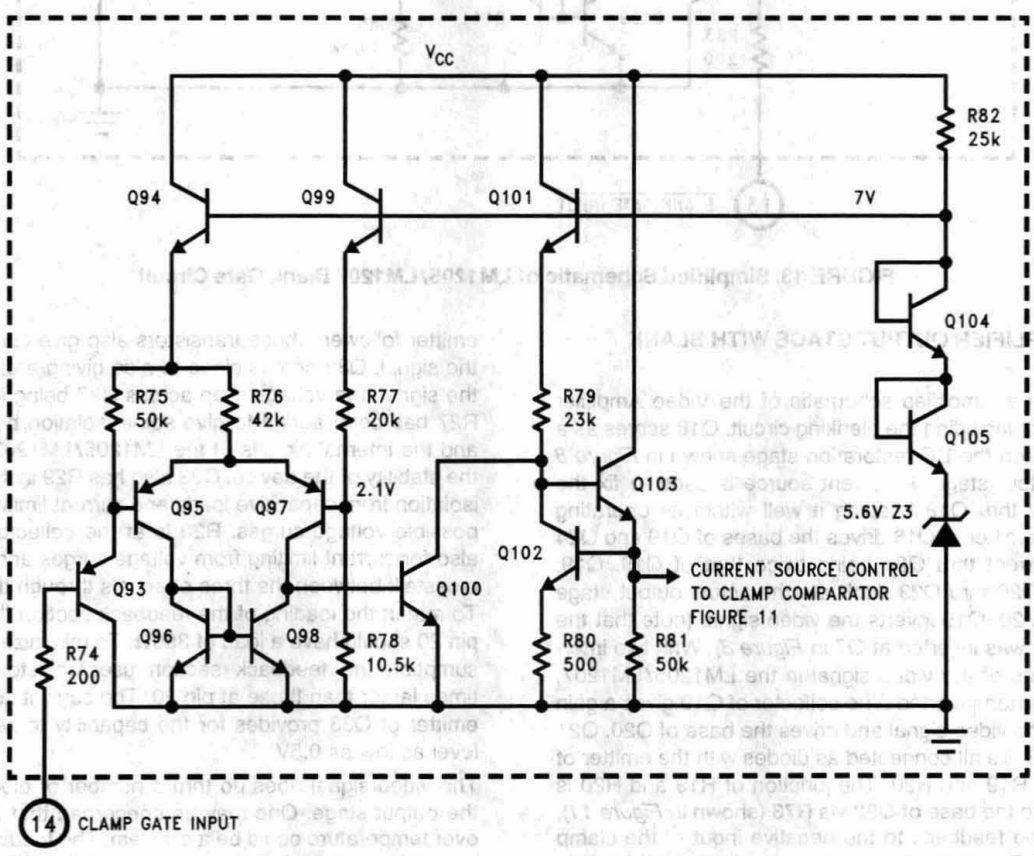

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FIGURE 12. Simplified Schematic of LM1205/LM1207 Clamp Gate Circuit

Circuit Description (Continued)

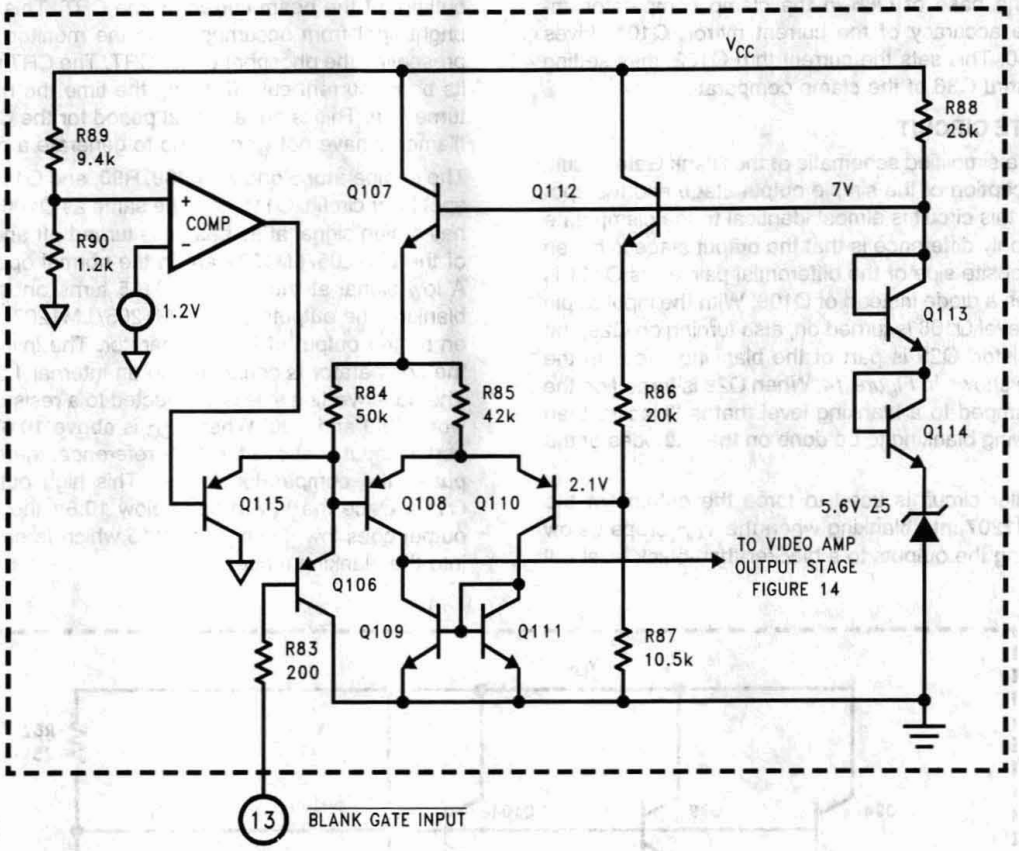

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FIGURE 13. Simplified Schematic of LM1205/LM1207 Blank Gate Circuit

VIDEO AMPLIFIER OUTPUT STAGE WITH BLANK CIRCUIT

Figure 14 is a simplified schematic of the Video Amplifier Output Stage including the blanking circuit. Q18 serves as a buffer between the DC restoration stage shown in *Figure 8* and the output stage. A current source is used to fix the current flow thru Q18 keeping it well within its operating range. The emitter of Q18 drives the bases of Q19 and Q24 with the current thru Q24 being twice that of Q19. Q19, along with Q20 thru Q23 duplicate the actual output stage going to pin 20. Q19 inverts the video signal (note that the video signal was inverted at Q7 in *Figure 8*). With two internal inversions of the video signal in the LM1205/LM1207, the output is non-inverted. The collector of Q19 gives a gain of −10 to the video signal and drives the base of Q20. Q21 through Q23 are all connected as diodes with the emitter of Q23 driving R19 and R20. The junction of R19 and R20 is connected to the base of Q92 via R73 (shown in *Figure 11*), this being the feedback to the negative input of the clamp comparator. This stage is independent of the actual output stage at pin 20, but is where the feedback is done for DC restoration. Therefore it is possible to blank the actual output stage below the black level without affecting the DC restoration feedback loop. Q24 is the equivalent part of Q19 in the actual output stage. It also inverts the video signal with a gain of −10 and drives the base of Q30. Q30 thru Q32 each give a diode drop to the level of the video signal, similar to being connected as diodes. Being connected as emitter-followers these transistors also give current gain to the signal. Q33 comes close to also giving a diode drop to the signal, the voltage drop across R27 being insignificant. R27 has been added to give some isolation between Q33 and the internal circuits of the LM1205/LM1207, adding to the stability of the device. Q33 also has R29 in its emitter for isolation from capacitive loads and current limiting from any possible voltage surges. R28 is at the collector of Q33 is also for current limiting from voltage surges and minimizing crosstalk between the three channels through the V_{CC} line. To match the loading of the feedback section the output at pin 20 should have a load of 390Ω. To minimize power consumption the feedback section uses resistor values 10 times larger than those at pin 20. The current source at the emitter of Q33 provides for the capability to set the black level as low as 0.5V.

The video signal does go thru a number of diode drops at the output stage. One may be concerned that the tracking over temperature could be a problem. The feedback section has been designed to temperature track the output stage. The feedback for DC restoration eliminates the temperature coefficients of the diode junctions. The remaining section to be covered is the blanking section. This section comprises of Q25 thru Q29. Q26 thru Q28 are connected as diodes. Q25 provides current gain to this stage to adequately pull down the base of Q30 during blanking and also adding another diode potential. During blanking the base of Q30 will be four diode drops above ground, plus the saturation volt-

Circuit Description (Continued)

age of Q29. There are also four diode drops from the base of Q30 to the output, pin 20. Therefore during blanking pin 20 will be less than 100 mV above ground, enabling the designer to blank at the cathode of the CRT. R23 is added to quickly turn off Q25 by discharging its base when the blanking signal is removed.

Figure 14 also shows the power and ground pins to the LM1205/LM1207. All the V_{CC1} pins (pins 3, 11, 25) are all internally connected together. A 0.1 μF bypass capacitor must be located close to each pin and connected to ground. Further bypassing is done by a 100 μF capacitor. This capacitor needs to be located on the board close to the LM1205/LM1207. Pins 22 and 23 are the V_{CC2} pins. A 10 μF and a 0.1 μF bypass capacitors must be located close to pins 22 and 23. Correct bypassing of pins 22 and 23 is **very important**. If the bypassing is not adequate then the outputs of the LM1205/LM1207 will have ringing, or even worse they may oscillate. The ground side of the bypass capacitors at pins 22 and 23 must be returned to a ground plane with no interruptions from other traces between these capacitors and the ground pins 21 and 24 of the LM1205/LM1207.

Applications of the LM1205/LM1207

Figure 15 is the schematic of the demonstration board designed at National. *Figure 16* is the actual layout of the demonstration board. Note that the schematic shown in *Figure 15* is almost identical to the schematic shown in *Figure 4*. The only difference between the two schematics is that in *Figure 15* each channel has individual adjustments for both drive and cutoff, making this circuit a good design for monitor applications. Each CRT will have a slightly different cutoff voltage for each color, making it necessary to provide separate adjustments in order to accurately set the cutoff for each color. The gain of each color of the CRT is also slightly different; if the color temperature of the display is to be accurately set then each channel of the LM1205/LM1207 must have individual gain adjustments. Thus each channel has its own drive control. Once the drive control is set, the gain between the three color channels will closely track as the contrast is adjusted. All the jumpers needed to design a single sided PC board are shown in the schematic. The resistors and jumpers with no reference designation are the connections between the PC board and the connectors mounted on the PC board. CN1 thru CN8 are BNC connectors.

A 30Ω resistor is in series with each of the video inputs. A voltage surge may occur at these inputs when either the inputs are first connected to another system, or when the system is powered up before the monitor is turned on. If this voltage surge exceeds the supply voltage (at ground potential if the monitor is not powered up) of the LM1205/LM1207, or goes below ground, current will flow through the parasitic devices of the LM1205/LM1207. This current is limited by the 30Ω resistors, preventing a potential catastrophic failure. A 100Ω resistor is added to the Blank Gate

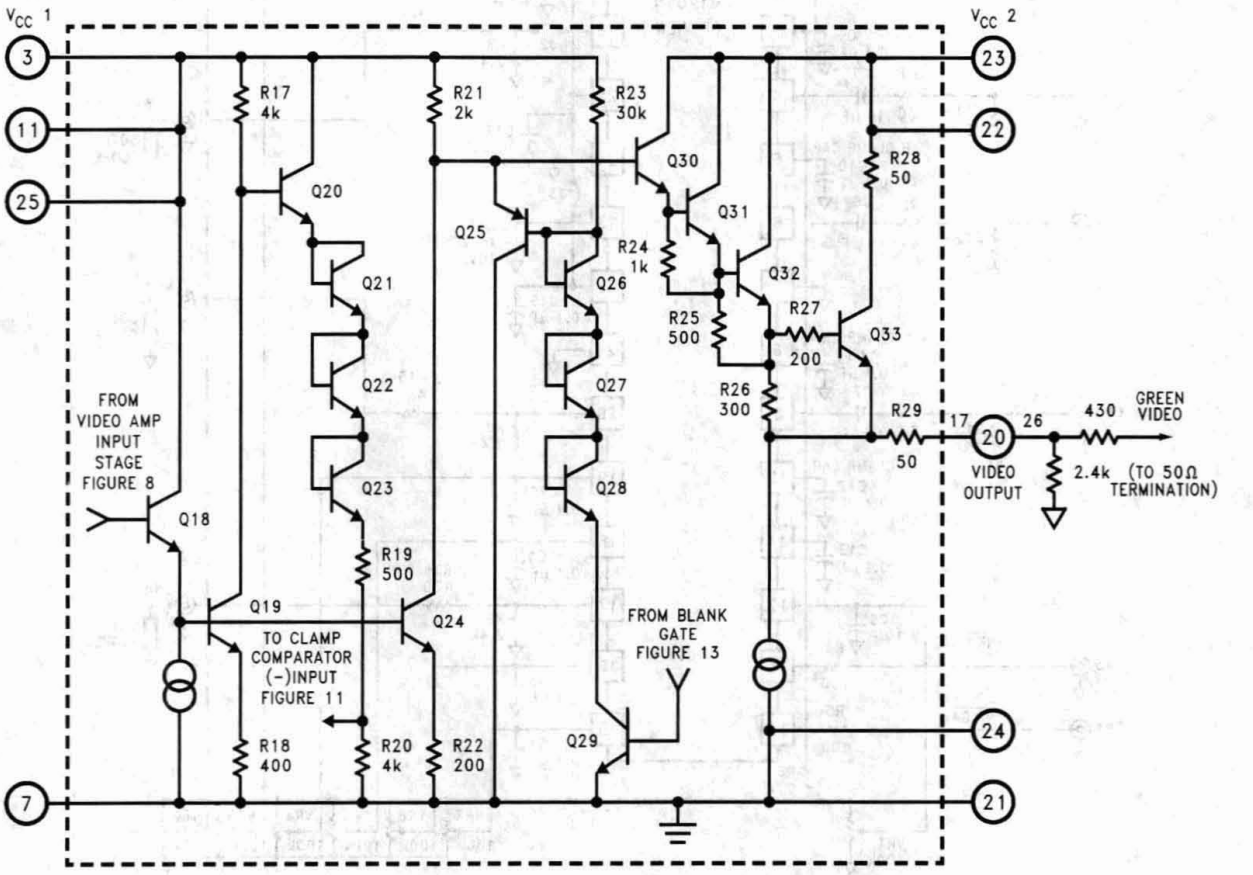

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FIGURE 14. Simplified Schematic of LM1205/LM1207 Video Amplifier Output Stage with Blank Circuit

Applications of the LM1205/LM1207 (Continued)

and Clamp Gate inputs. These two resistors also limit the current during a voltage surge. A larger resistor is required because these inputs are DC coupled, allowing the current to continuously flow into these inputs before the monitor is turned on. 100Ω resistors are not recommended at the video inputs because this resistance value will start to roll off the frequency response of the LM1205/LM1207.

Note that the layout shown in *Figure 16* does have a very extensive ground plane. One must remember that the LM1205/LM1207 is a 130 MHz/85 MHz part and a single sided board is difficult to successfully design. A ground plane similar to the layout shown in *Figure 16* must be provided for good performance of the LM1205/LM1207 when using either a single sided or double sided board. The layout of this board demonstrates the importance of grounding. The results of this layout are shown in *Figures 17a* through *17d*. In these photographs the LM1205 rise time was 2.25 ns and its fall time was 3.00 ns. For the LM1207, the rise time was 4.10 ns and the fall time 3.85 ns. The output was a 4 V_{PP} signal and the cutoff voltage was set to 2V. The overshoot will subsequently be filtered out by the loading effects of the CRT driver stage and the CRT itself. When the LM1205/LM1207 is designed into a video board one must keep the ground to the CRT driver stage separate from the ground of the LM1205/LM1207, connecting the two grounds together only at one point. National Semiconductor also manufactures a line of CRT drivers. Please contact National for additional information. These drivers greatly simplify the driver design allowing for shorter design cycles. Of course the LM1205/LM1207 can also be designed with a discrete driver stage. *Figure 18* shows a design using a simple cascode CRT driver. The LM1205/LM1207 block would be the same schematic as shown in *Figure 15*.

REFERENCES

Zahid Rahim, "Guide to CRT Video Design," Application Note 861, National Semiconductor Corp., Jan. 1993

Ott, Henry W. *Noise Reduction Techniques in Electronic Systems,* John Wiley & Sons, New York, 1976

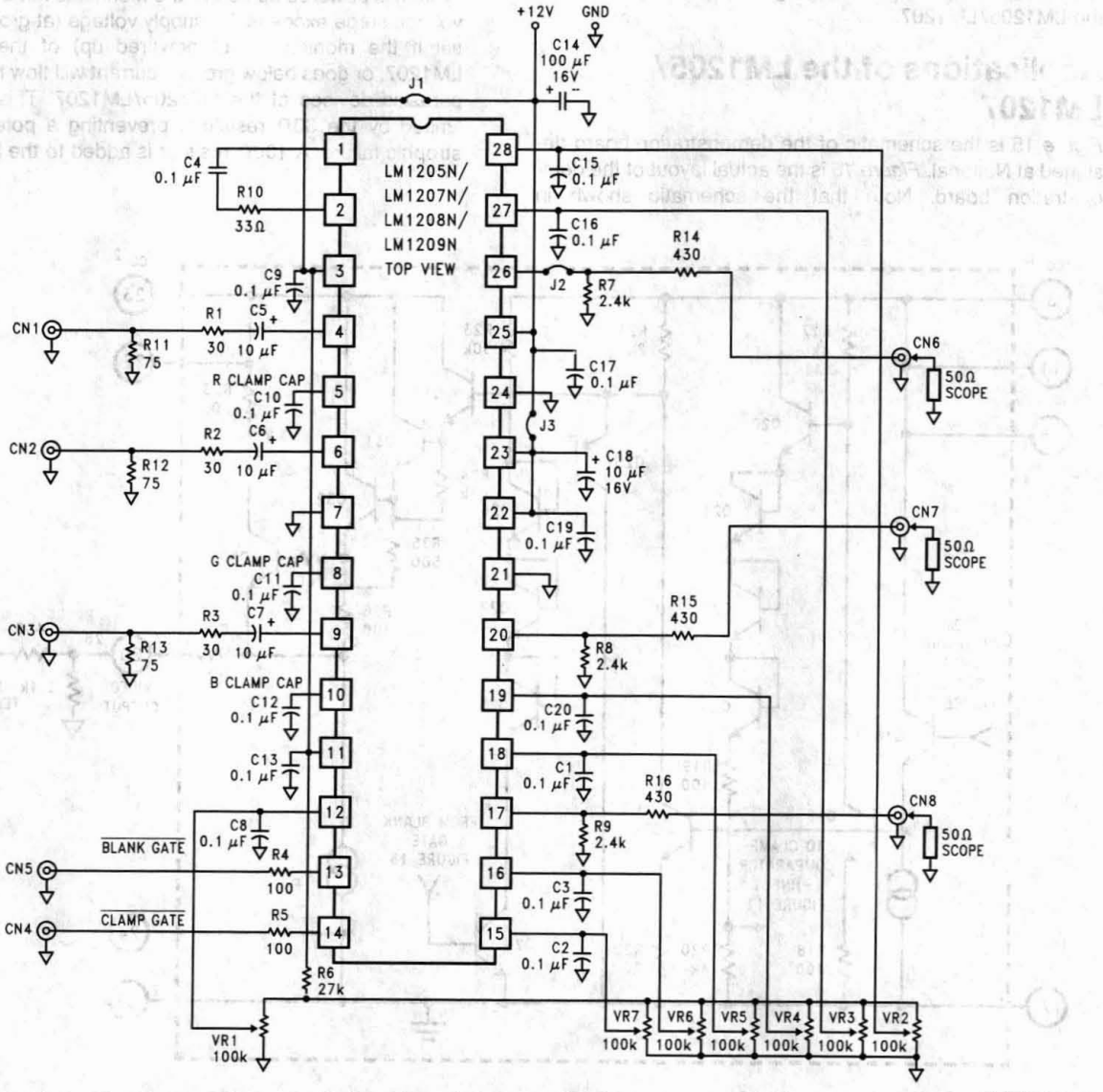

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FIGURE 15. Demonstration Board Schematic

Applications of the LM1205/LM1207 (Continued)

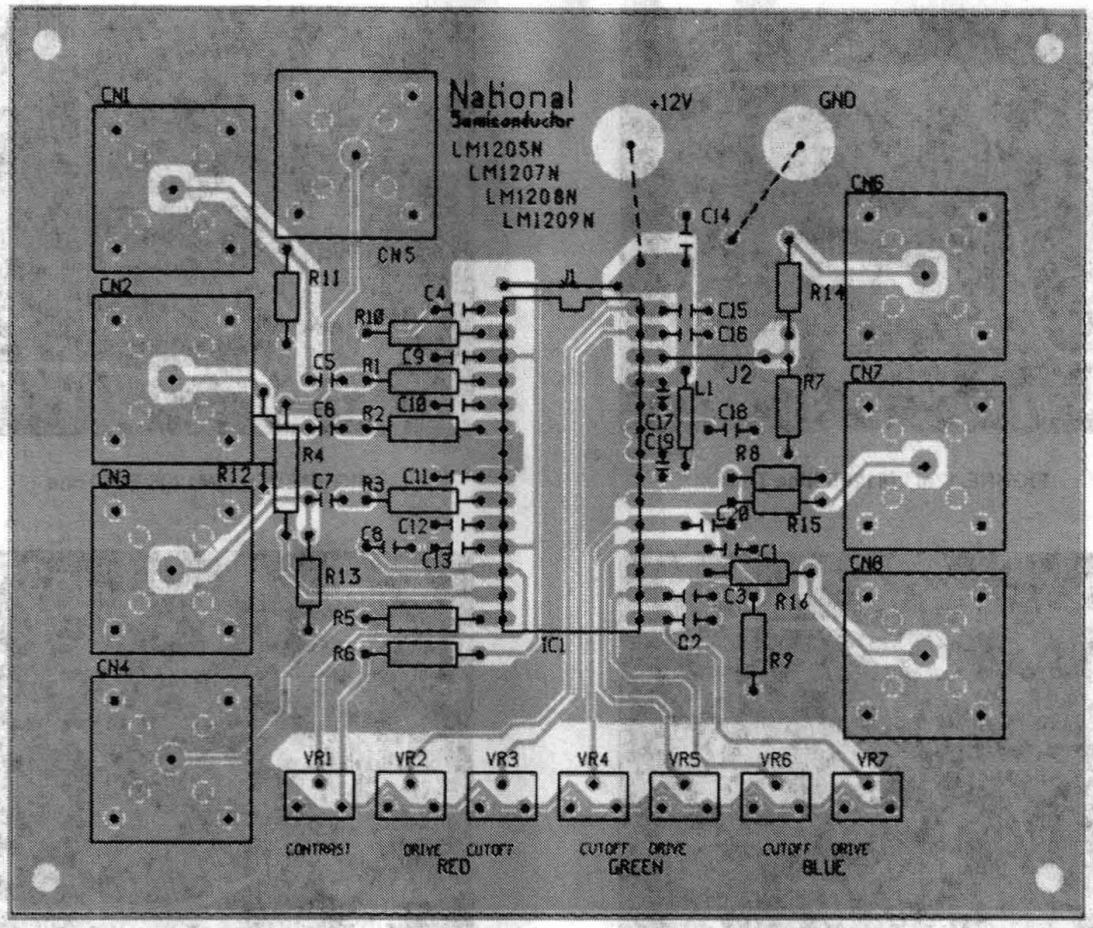

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FIGURE 16. Demonstration Board Layout

Applications of the LM1205/LM1207 (Continued)

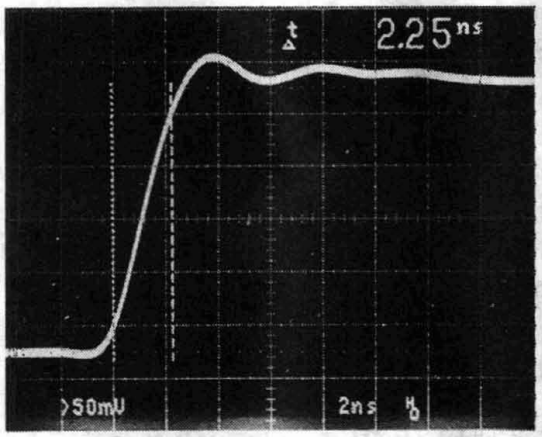

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FIGURE 17a. LM1205 Rise Time

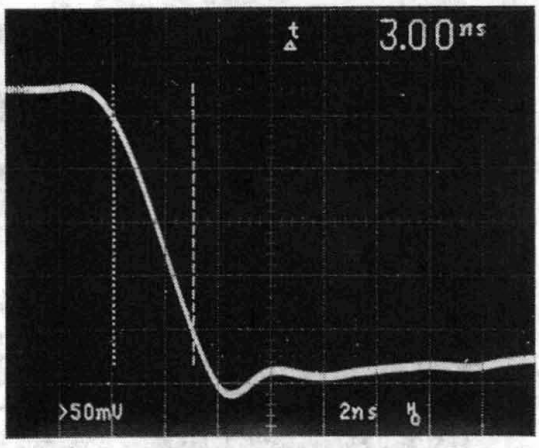

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FIGURE 17b. LM1205 Fall Time

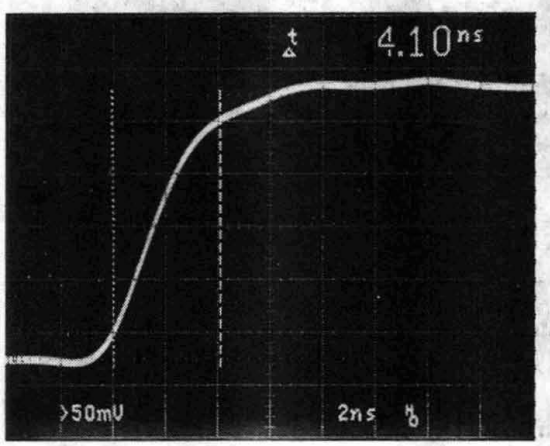

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FIGURE 17c. LM1207 Rise Time

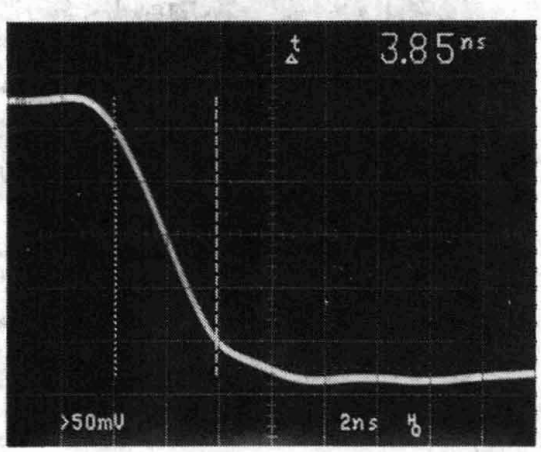

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FIGURE 17d. LM1207 Fall Time

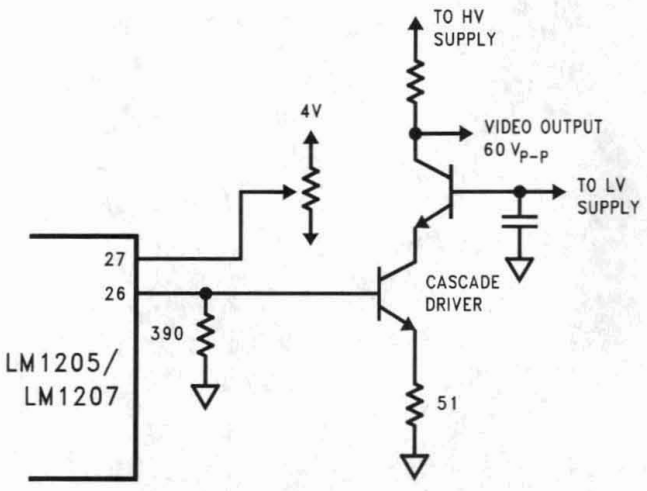

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FIGURE 18. LM1205/LM1207 Typical Application

National Semiconductor

LM1208/LM1209
130 MHz/100 MHz RGB Video Amplifier System with Blanking

General Description

The LM1208/LM1209 is a very high frequency video amplifier system intended for use in high resolution RGB monitor applications. In addition to the three matched video amplifiers, the LM1208/LM1209 contains three gated single ended input black level clamp comparators for brightness control, three matched DC controlled attenuators for contrast control, and three DC controlled drive attenuators providing independent full range gain control in each channel for wide range white balance. All DC control inputs offer high input impedance and an operation range from 0V to 4V for easy interface to bus controlled alignment systems. The LM1208/LM1209 also contains a blanking circuit which clamps the video output voltage during blanking to within 0.1V above ground. This feature provides blanking capability at the cathodes of the CRT. A spot killer is provided for CRT phosphor protection during power-down.

Features

- Three wideband video amplifiers 130 MHz @ −3 dB (4 V_{PP} output)
- Matched (±0.1 dB or 1.2%) attenuators for contrast control
- Three externally gated single ended input comparators for cutoff and brightness control
- 0V to 4V, high input impedance DC contrast control (>40 dB range)
- 0V to 4V, high input impedance DC full range gain control (Drive) for each video channel (>40 dB range)
- Spot killer, blanks outputs when V_{CC} < 10.6V
- Capable of 7 V_{PP} output swing (slight reduction in bandwidth)
- Output stage blanking
- Output stage directly drives most hybrid or discrete CRT drivers

Applications

- High resolution RGB CRT monitors
- Video AGC amplifiers
- Wideband amplifiers with gain and DC offset controls
- Interface amplifiers for LCD or CCD systems

Block and Connection Diagram

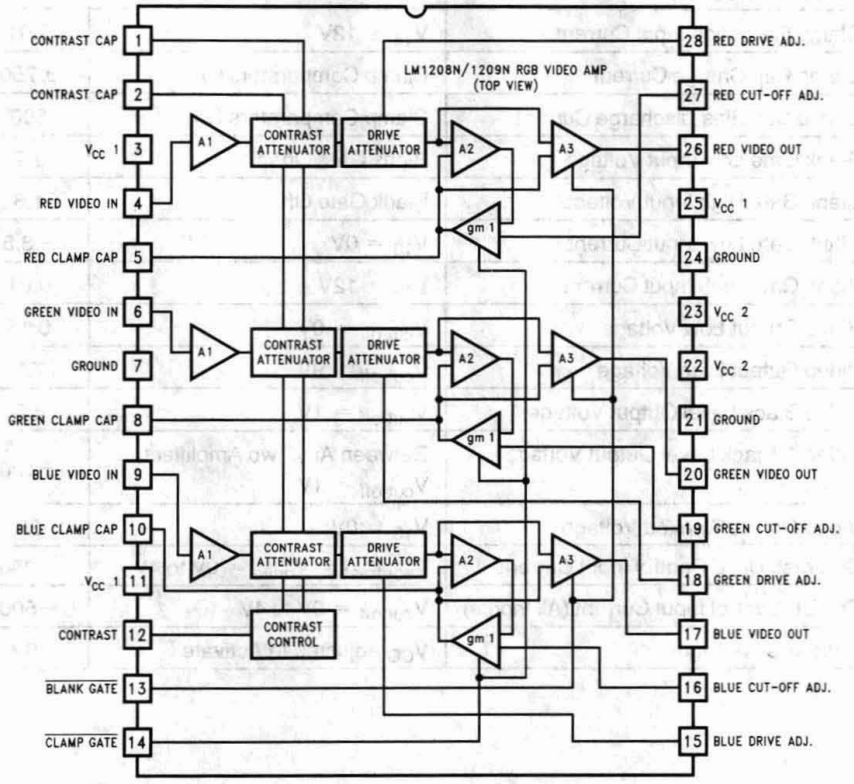

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FIGURE 1

Order Number LM1208N or LM1209N
See NS Package Number N28B

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC}) Pins 3, 11, 22, 23, 25 (Note 3)	15V
Peak Video Output Source Current (Any One Amp) Pins 17, 20 or 26	28 mA
Voltage at Any Input Pin (V_{IN})	$V_{CC} \geq V_{IN} \geq GND$
Power Dissipation (P_D) (Above 25°C Derate Based on θ_{JA} and T_J)	2.5W
Thermal Resistance (θ_{JA})	50°C/W
Junction Temperature (T_J)	150°C
ESD Susceptibility (Note 4)	2 kV
Pins 12, 13, and 14	1.9 kV
Storage Temperature	−65°C to 150°C
Lead Temperature (Soldering, 10 sec.)	265°C

Operating Ratings (Note 2)

Temperature Range	−20°C to 80°C
Supply Voltage (V_{CC})	$10.8V \leq V_{CC} \leq 13.2V$

DC Electrical Characteristics

See DC Test Circuit *(Figure 2)*, $T_A = 25°C$; $V_{CC1} = V_{CC2} = 12V$. $V_{12} = 4V$; $V_{14} = 0V$; $V_{cut\text{-}off} = 1.0V$; $V_{13} = 4V$; $V_{drive} = 4V$ unless otherwise stated.

Symbol	Parameter	Conditions	Typical (Note 5)	Limit (Note 6)	Units
I_S	Supply Current	$V_{CC1} + V_{CC2}$, $R_L = \infty$ (Note 7)	90	105	mA (max)
$V_{4, 6, 9}$	Video Amplifier Input Bias Voltage		2.8		V
R_{IN}	Video Input Resistance	Any One Amplifier	20		kΩ
V_{14l}	Clamp Gate Low Input Voltage	Clamp Comparators On	1.2	0.8	V (max)
V_{14h}	Clamp Gate High Input Voltage	Clamp Comparators Off	1.6	2.0	V (min)
I_{14l}	Clamp Gate Low Input Current	$V_{14} = 0V$	−1	−5	μA (max)
I_{14h}	Clamp Gate High Input Current	$V_{14} = 12V$	0.01	1.0	μA (max)
I_{clamp}	Clamp Cap Charge Current	Clamp Comparators On	±750	±500	μA (min)
I_{bias}	Clamp Cap Bias Discharge Current	Clamp Comparators Off	500		nA
V_{13l}	Blank Gate Low Input Voltage	Blank Gate On	1.2	0.8	V (max)
V_{13h}	Blank Gate High Input Voltage	Blank Gate Off	1.6	2.0	V (min)
I_{13l}	Blank Gate Low Input Current	$V_{13} = 0V$	−8.5	−11.0	μA (max)
I_{13h}	Blank Gate High Input Current	$V_{13} = 12V$	0.01	1.0	μA (max)
V_{OL}	Video Output Low Voltage	$V_{cut\text{-}off} = 0V$	0.15	0.5	V (max)
V_{OH}	Video Output High Voltage	$V_{cut\text{-}off} = 9V$	7.5	7	V (min)
$V_{O(1V)}$	Video Black Level Output Voltage	$V_{cut\text{-}off} = 1V$	1.0		V (Note 8)
$\Delta V_{O(1V)}$	Video Δ Black Level Output Voltage	Between Any Two Amplifiers, $V_{cut\text{-}off} = 1V$	±100		mV (max)
V_{OL}(blanked)	Video Output Blanked Voltage	$V_{13} = 0V$	35	70	mV (max)
$I_{12, 15, 18 \text{ or } 28}$	Contrast/Drive Control Input Current	$V_{contrast} = V_{drive} = 0V$ to 4V	−250		nA
$I_{16, 19 \text{ and } 27}$	Cut-Off Control Input Current (All Inputs)	$V_{cut\text{-}off} = 0V$ to 4V	−500		nA
V_{SPOT}	Spot Killer Voltage	V_{CC} Adjusted to Activate	10.4	10.8	V (max)

AC Electrical Characteristics

See AC Test Circuit *(Figure 3)*, $T_A = 25°C$; $V_{CC1} = V_{CC2} = 12V$. Manually adjust Video Output pins 17, 20, and 26 to 4V DC for the AC test unless otherwise stated. (Note 14).

Symbol	Parameter	Conditions		Typical (Note 5)	Limit (Note 6)	Units
$A_{V\ max}$	Video Amplifier Gain	V12 = 4V, V_{IN} = 635 mV_{PP} V_{drive} = 4V		7.0	6.0	V/V (min)
				16.9	15.6	dB (min)
$\Delta A_{V\ 2V}$	Contrast Attenuation @ 2V	Ref: A_V max, V12 = 2V		−6		dB
$\Delta A_{V\ 0.25V}$	Contrast Attenuation @ 0.25V	Ref: A_V max, V12 = 0.25V		−40		dB
$\Delta Drive_{2V}$	Drive Attenuation @2V	Ref: A_V max, V_{drive} = 2V		−6		dB
$\Delta Drive_{0.25V}$	Drive Attenuation @0.25V	Ref: A_V max, V_{drive} = 0.25V		−40		dB
$A_{V\ match}$	Absolute Gain Match @ A_V max	V12 = 4V, V_{drive} = 4V (Note 9)		±0.3		dB
$A_{V\ track1}$	Gain Change Between Amplifiers	V12 = 4V to 2V (Notes 9, 10)		±0.1		dB
THD	Video Amplifier Distortion	V_O = 1 V_{PP}, f = 10 kHz		1		%
f (−3 dB)	Video Amplifier Bandwidth (Notes 11, 12)	V12 = 4V, V_{drive} = 4V, V_O = 4 V_{PP}	LM1208	130		MHz
			LM1209	100		
t_r(Video)	Video Output Rise Time (Note 11)	V_O = 4 V_{PP}	LM1208	2.8		ns
			LM1209	3.2		
t_f(Video)	Video Output Fall Time (Note 11)	V_O = 4 V_{PP}	LM1208	3.4		ns
			LM1209	3.6		
V_{sep} 10 kHz	Video Amplifier 10 kHz Isolation	V12 = 4V (Note 13)		−70		dB
V_{sep} 10 MHz	Video Amplifier 10 MHz Isolation	V12 = 4V (Notes 11, 13)		−50		dB
t_r(Blank)	Blank Output Rise Time (Note 11)	Blank Output = 1 V_{PP}		7		ns
t_f(Blank)	Blank Output Fall Time (Note 11)	Blank Output = 1 V_{PP}		7		ns
t_{pw}(Clamp)	Min. Back Porch Clamp Pulse Width			200		ns

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur.

Note 2: Operating Ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.

Note 3: V_{CC} supply pins 3, 11, 22, 23, 25 must be externally wired together to prevent internal damage during V_{CC} power on/off cycles.

Note 4: Human body model, 100 pF discharged through a 1.5 kΩ resistor.

Note 5: Typical specifications are specified at +25°C and represent the most likely parametric norm.

Note 6: Tested limits are guaranteed to National's AOQL (Average Outgoing Quality Level).

Note 7: The supply current specified is the quiescent current for V_{CC1} and V_{CC2} with $R_L = \infty$, see *Figure 2's* test circuit. The supply current for V_{CC2} (pin 23) also depends on the output load. With video output at 1V DC, the additional current through V_{CC2} is 8 mA for *Figure 2's* test circuit.

Note 8: Output voltage is dependent on load resistor. Test circuit uses $R_L = 390\Omega$.

Note 9: Measure gain difference between any two amplifiers. V_{IN} = 635 mV_{PP}.

Note 10: ΔA_V track is a measure of the ability of any two amplifiers to track each other and quantifies the matching of the three attenuators. It is the difference in gain change between any two amplifiers with the contrast voltage (V12) at either 4V or 2V measured relative to an A_V max condition, V12 = 4V. For example, at A_V max the three amplifiers' gains might be 17.1 dB, 16.9 dB and 16.8 dB and change to 11.2 dB, 10.9 dB, and 10.7 dB respectively for V12 = 2V. This yields the measured typical ± 0.1 dB channel tracking.

Note 11: When measuring video amplifier bandwidth or pulse rise and fall times, a double sided full ground plane printed circuit board without socket is recommended. Video amplifier 10 MHz isolation test also requires this printed circuit board. The reason for a double sided full ground plane PCB is that large measurement variations occur in single sided PCBs.

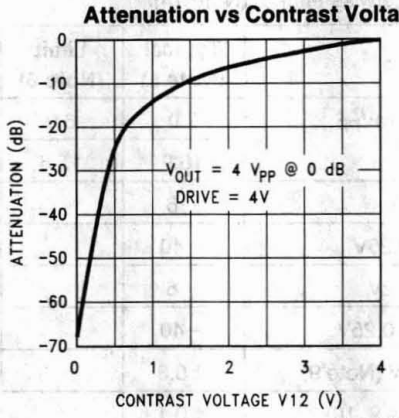
Note 12: Adjust input frequency from 10 MHz (A_V max reference level) to the −3 dB corner frequency ($f_{-3\ dB}$).

Note 13: Measure output levels of the other two undriven amplifiers relative to the driven amplifier to determine channel separation. Terminate the undriven amplifier inputs to simulate generator loading. Repeat test at f_{IN} = 10 MHz for $V_{sep\ 10\ MHz}$.

Note 14: During the AC tests the 4V DC level is the center voltage of the AC output signal. For example, if the output is 4 V_{PP} the signal will swing between 2V DC and 6V DC.

Typical Performance Characteristics (V_{CC} = 12V, T_A = 25°C unless otherwise specified)

Attenuation vs Contrast Voltage



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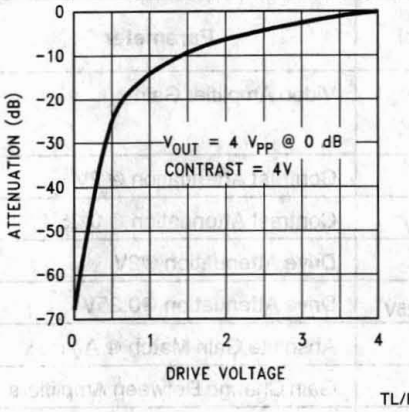
Attenuation vs Drive Voltage



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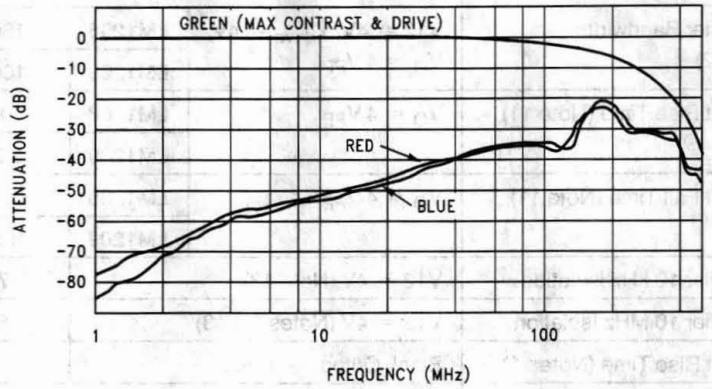
LM1208 Crosstalk vs Frequency



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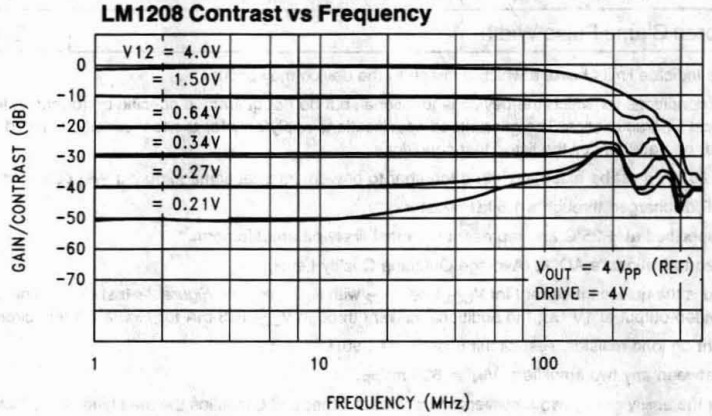
LM1208 Contrast vs Frequency



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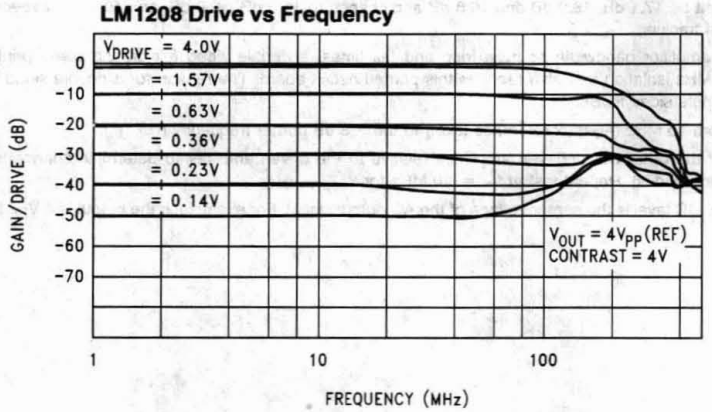
LM1208 Drive vs Frequency



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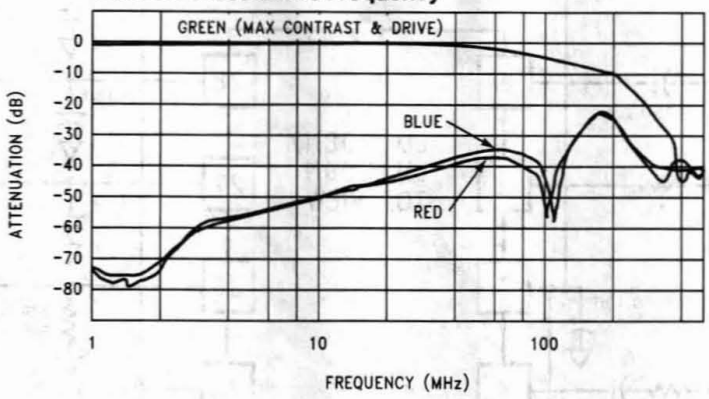
Typical Performance Characteristics (V_{CC} = 12V, T_A = 25°C unless otherwise specified) (Continued)

LM1209 Crosstalk vs Frequency



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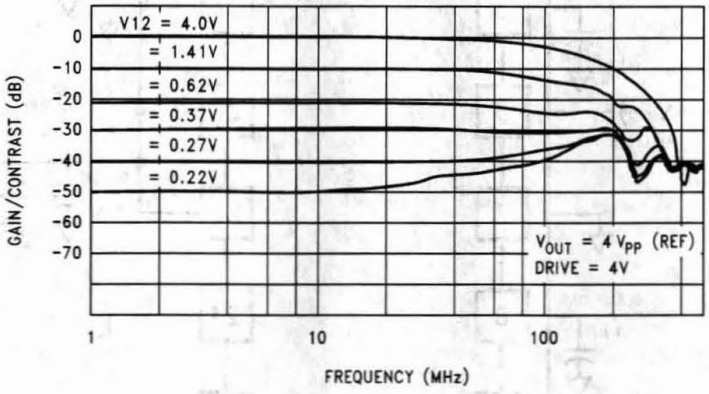
LM1209 Contrast vs Frequency



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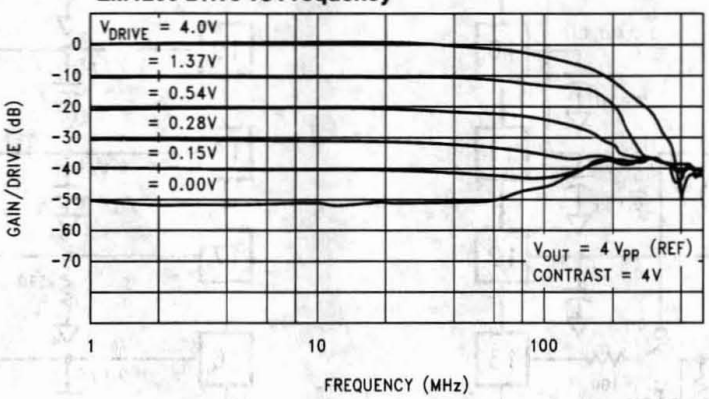
LM1209 Drive vs Frequency



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2

Applications Information

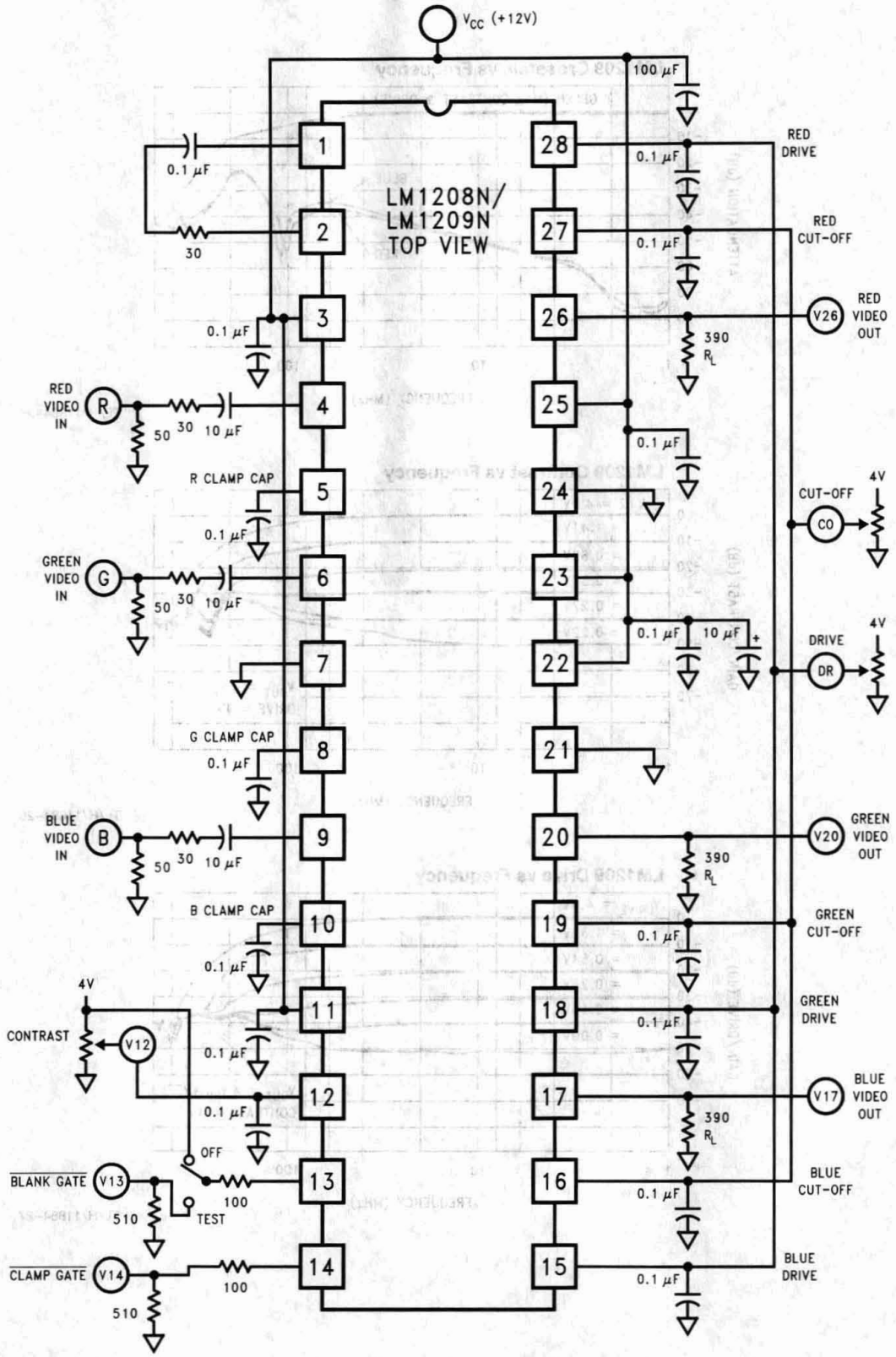

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FIGURE 2. LM1208N/LM1209N DC Test Circuit

Applications Information (Continued)

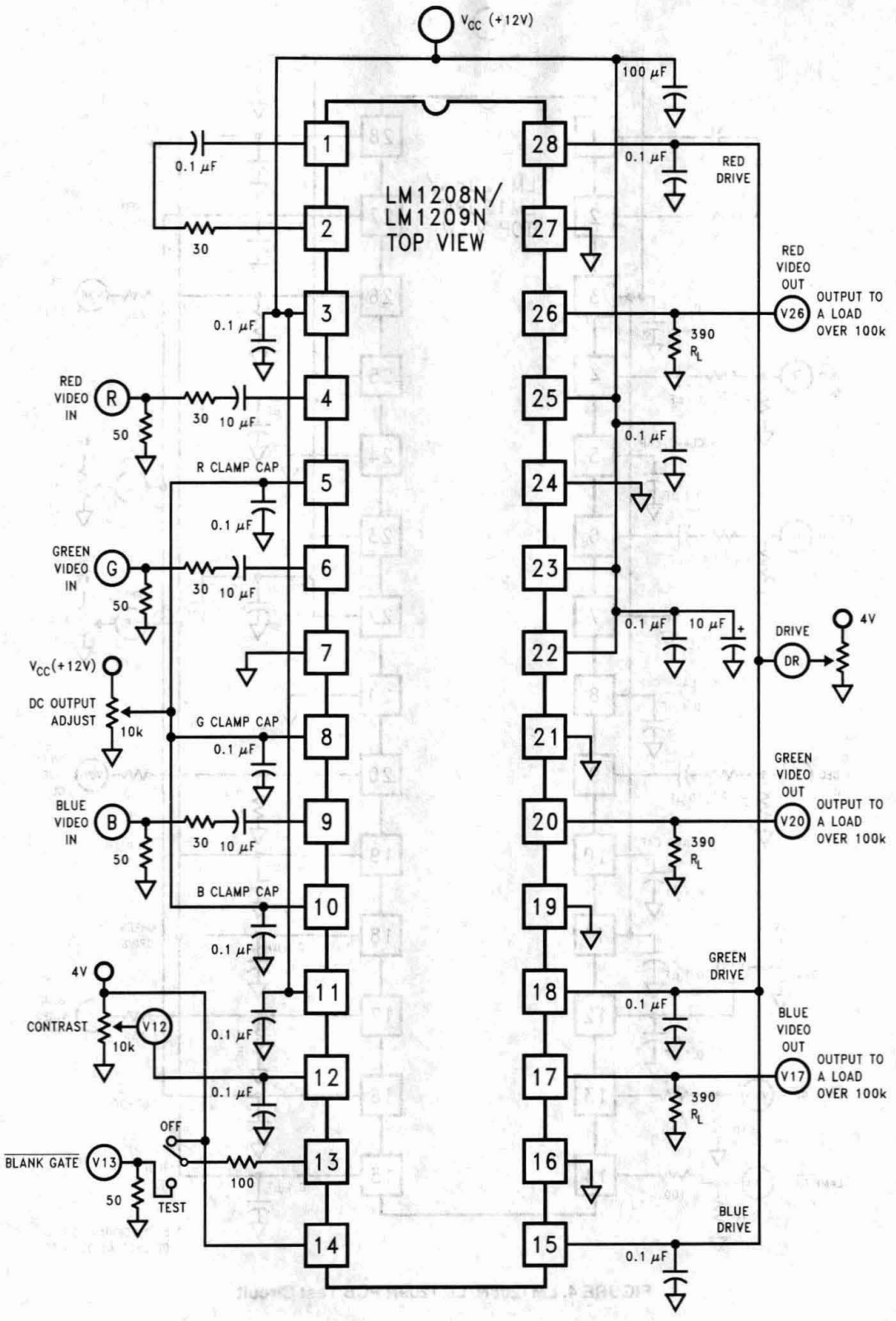

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FIGURE 3. LM1208N/LM1209N AC Test Circuit

Applications Information (Continued)

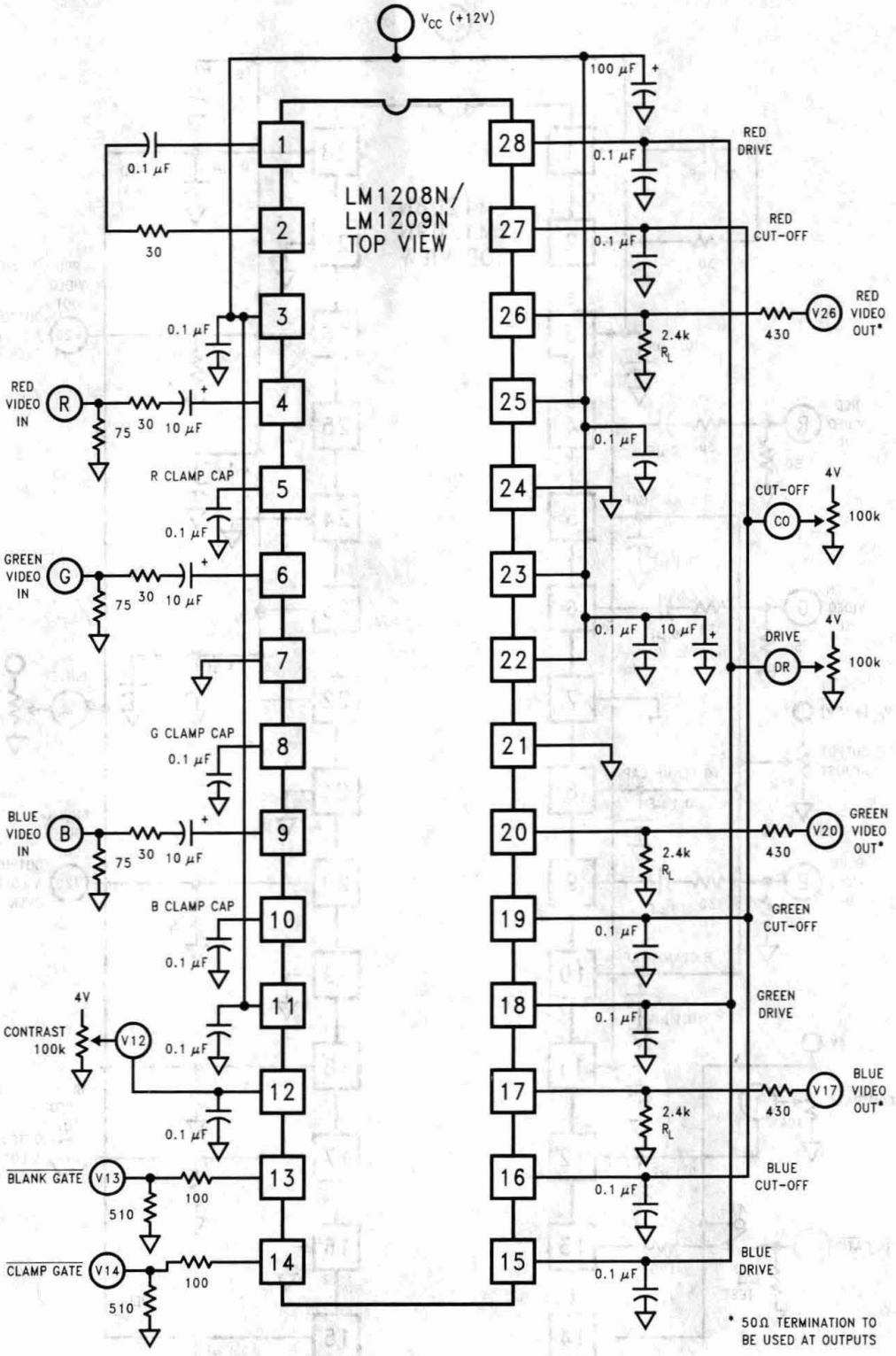

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FIGURE 4. LM1208N/LM1209N PCB Test Circuit

Applications Information (Continued)

Figure 5 shows the block diagram of a typical analog RGB color monitor. The RGB monitor is used with CAD/CAM work stations, PC's, arcade games and in a wide range of other applications that benefit from the use of color display terminals. The RGB color monitor characteristics may differ in such ways as sweep rates, screen size, CRT color trio spacing (dot pitch), or in video amplifier bandwidths but will still be generally configured as shown in *Figure 5*. Separate horizontal and vertical sync signals may be required or they may be contained in the green video input signal. The video input signals are usually supplied by coax cable which is terminated into 75Ω at the monitor input and internally AC coupled to the video amplifiers. These input signals are approximately 1V peak to peak in amplitude and at the input of the high voltage video section, approximately 5V peak to peak. At the cathode of the CRT the video signals can be as high as 60V peak to peak. One important requirement of the three video amplifiers is that they match and track each other over the contrast and brightness control range. The *Figure 5* block labeled "VIDEO AMPLIFICATION WITH GAIN AND DC CONTROL" describes the function of the LM1208/LM1209 which contains the three matched video amplifiers, contrast control and brightness control. The LM1208/LM1209 also provides the capability to blank at the cathode of the CRT.

Functional Description

Figure 6 is a detailed block diagram of the green channel of the LM1208/LM1209 along with the recommended external components. The IC pin numbers are circled and all external components are shown outside the dashed line. The other two video channels are identical to the green channel, only the numbers to the pins unique to each channel are different. The input video is normally terminated into 75Ω. The termination resistor depends on the impedance of the coax cable being used, 75Ω being the most common impedance used in video applications. The video signal is AC coupled through a 10 μF capacitor to the input, pin 6. There is no standard for the DC level of a video signal, therefore the signal must be AC coupled to the LM1208/LM1209. Internal to the LM1208/LM1209 is a 2.8V reference, giving the input video an offset voltage of 2.8V. This voltage was selected to give the input video enough DC offset to guarantee that the lowest voltage of the video signal at pin 6 is far enough above ground to keep the LM1208/LM1209 in the active region. The 200Ω resistor at the input is for ESD protection and for current limiting during any voltage surge that may occur at the input, driving pin 6 above V_{CC}. The input video signal is buffered by −A1. In this circuit description an inverting amplifier is shown with a "−" (minus sign) in front of the amplifier designation. The output of −A1 goes to the contrast and drive attenuator sections.

The contrast and drive control sections are virtually identical. Both sections take a 0V to 4V input voltage, 4V giving the maximum gain for either the contrast or the drive. This is a high impedance input, allowing for an easy interface to 5V DACs. One may also use 100k potentiometers with no degradation in performance. The contrast control section is common to all three channels. It converts the input voltage at pin 12 to a couple of internal DC voltages that control the gain of the contrast attenuator. Referring to the Attenuation vs Contrast Voltage under typical performance characteristics note that a 4V control voltage results in no attenuation of the video signal. A 0.25V control voltage results in an attenuation of 40 dB. Again note that these internal control voltages are common to all three channels. To minimize crosstalk, these voltages go to pins 1 and 2. Minimizing crosstalk is done by adding the RC network shown in the block diagram *(Figure 6)*.

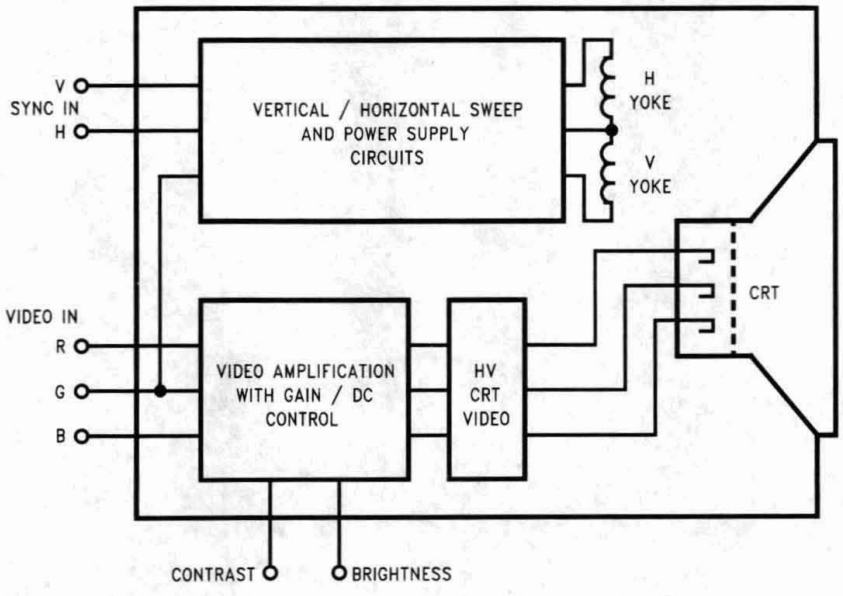

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FIGURE 5. Typical RGB Color Monitor Block Diagram

Functional Description (Continued)

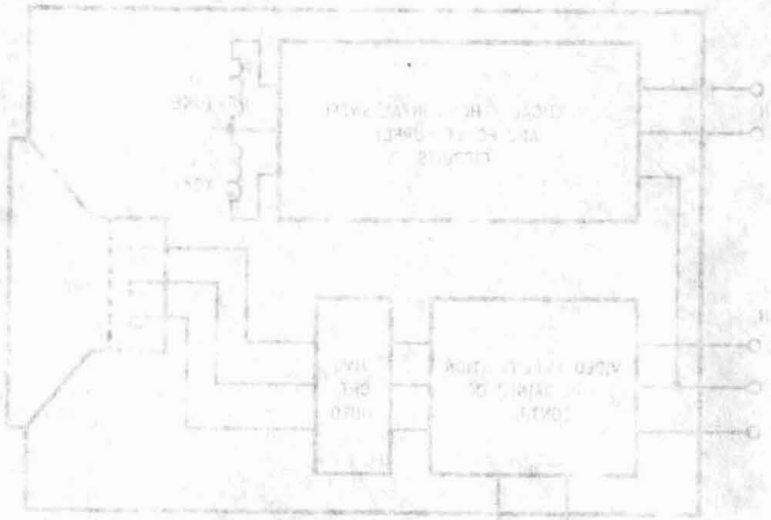
The 0V to 4V drive control signal comes in on pin 18. Each channel has its own drive section, therefore the crosstalk compensation needed for the contrast control voltages is not required for the drive control, thus no external pins for the drive control. The drive attenuator features a full range gain control over 40 dB. This gives no attenuation of the video signal with a 4V control voltage. A 0.25V control voltage results in an attenuation of 40 dB.

The output of the drive attenuator stage goes to A2, the amplifier in the DC restoration section. The video signal goes to the non-inverting input of A2. The inverting side of A2 goes to the output of gm1, the clamp comparator, and the clamp capacitor at pin 8.

During the back porch period of the video signal a negative going clamp pulse from pin 14 is applied to the clamp comparator, turning on the comparator. This period is where the black level of the video signal at the output of the LM1208/LM1209 is compared to the desired black level which is set at pin 19. *Figure 7* shows the timing of the clamp pulse relative to the video signal. The clamp capacitor is charged or discharged by gm1, generating the correction voltage needed at the inverting input of A2 to set the video output to the correct DC level. Removing the clamp pulse turns off gm1 with the correction voltage being maintained by the clamp capacitor during active video. Both the clamp pulse and the blank pulse at pin 13 are TTL voltage levels.

There are actually two output sections, −A3 and −A4. Both sections have been designed to be identical, except −A4 has more current drive capability. The output transistor shown is part of −A4, but has been shown separately so the user knows the configuration of the output stage. −A3 does not go to the outside world, it is used for feeding back the video signal for DC restoration. Its output goes directly to the inverting input of the clamp comparator via the voltage divider formed by the 500Ω and 4k resistors. −A4 will be close to the same output as −A3 and will temperature track due to the similar design of the two output stages. However, the current at the output of −A4 will be ten times the current at the output of −A3. To balance both outputs, a load resistance of 390Ω needs to be connected from pin 20, the green video output pin, to ground. Another input to −A4 is the blank pulse. When a negative going blank pulse is applied to pin 13, the output of the LM1208/LM1209 is driven to less than 0.1V above ground. Using the timing shown in *Figure 7* for the blank pulse, the output of the LM1208/LM1209 will be less than 0.1V during the inactive portion of the video signal. This is a "blacker than black" condition, blanking the CRT at the cathodes. By using the blank function of the LM1208/LM1209 no grid blanking is necessary. Note that the DC restoration is done by feeding back the video signal from −A3, but blanking is done at −A4. By using the two output stages, blanking can be done at the CRT cathodes, and at the same time activate the DC restoration loop.

V_{CC1} goes to pins 3, 11 and 25 (see *Figure 1*). These three pins are all internally connected. For proper operation of the LM1208/LM1209 it is necessary to connect **all** the V_{CC1} pins to the input power to the PCB and bypass each pin with a 0.1 μF capacitor. V_{CC2} is the input power at pins 22 and 23 for the three output stages. This is a separate power input from V_{CC1}, there are no internal connections between the two different power inputs. There must be a connection on the PCB between V_{CC1} and V_{CC2}. Pins 22 and 23 must be bypassed by a parallel connection of a 10 μF and 0.1 μF capacitors. The ground connections for the LM1208/LM1209 are at pins 7, 21, and 24. All three ground pins are internally connected, and these pins must also be connected externally to a good ground plane for proper operation of the LM1208/LM1209.



Functional Description (Continued)

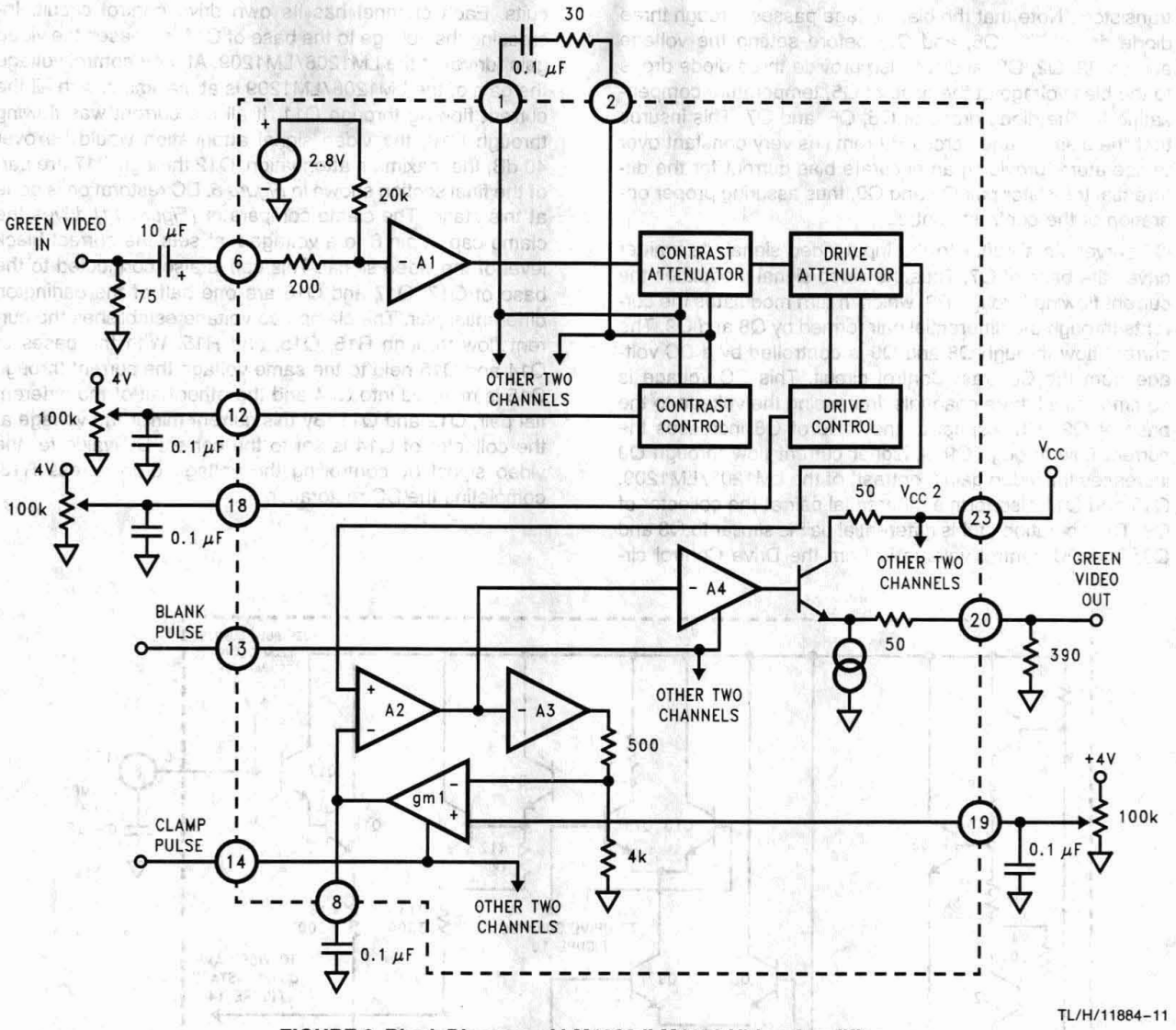


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FIGURE 6. Block Diagram of LM1208/LM1209 Video Amplifier

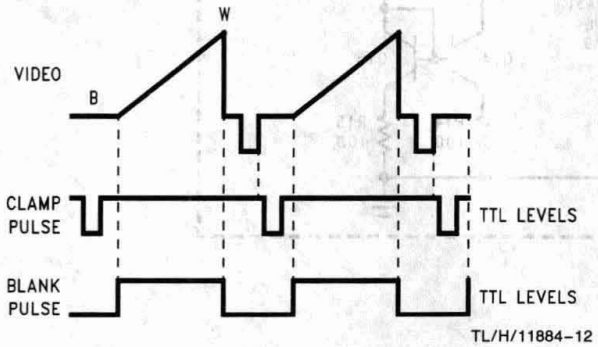

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FIGURE 7. Timing Diagram

Circuit Description

VIDEO AMPLIFIER INPUT STAGE

Figure 8 is a simplified schematic of one of the three video amplifiers input stage along with the recommended external components. The IC pin numbers are circled and all external components are shown outside the dashed line. The video input is applied to pin 6 via a 10 μF coupling capacitor and a 30Ω resistor. The resistor is added to limit the current through the input pin should an applied voltage surge rise above V_{CC} or drop below ground. The performance of the LM1208/LM1209 is not degraded by the 30Ω resistor. However, if EMI is a concern this resistor can be increased to well over 100Ω where the rise and fall times will start to become longer. DC bias to the input pin is provided by Q5 and its associated input circuitry. Z1 is a 5.6V zener that generates the input bias voltage. Q1 is a buffer to the zener reference voltage with 5.0V generated at its emitter. Q3 and Q4 are connected as diodes. Q2 is close to being a diode in this circuit. This configuration will give about 2.0V at the collector of Q2. R2 and R3 are a voltage divider, setting the base of Q5 to about 3.5V. This sets the emitter of Q5 to about 2.8V, the bias voltage of the video input. This bias voltage is necessary to assure that the entire video signal stays within the active operating region of the LM1208/LM1209. The bias voltage goes through R6, a 20k resistor, to the video input at pin 6. R4 and R6 are of the same value and R4 is used to compensate for beta variations of the

Circuit Description (Continued)

transistors. Note that the bias voltage passes through three diode drops (Q5, Q6, and Q7) before setting the voltage across R9. Q2, Q3, and Q4 also provide three diode drops to the bias voltage at the base of Q5, temperature compensating for the diode drops of Q5, Q6, and Q7. This insures that the bias voltage across R9 remains very constant over temperature, providing an accurate bias current for the differential transistor pair Q8 and Q9, thus assuring proper operation of the contrast control.

Q6 serves as a buffer to the input video signal. Its emitter drives the base of Q7. Thus the video signal modulates the current flowing through R9, which in turn modulates the currents through the differential pair formed by Q8 and Q9. The current flow through Q8 and Q9 is controlled by a DC voltage from the Contrast Control circuit. This DC voltage is common to all three channels. Increasing the voltage to the base of Q9 with respect to the base of Q8 increases the current flow through Q9. A higher current flow through Q9 increases the video gain (contrast) of the LM1208/LM1209. Q10 and Q11 also form a differential pair at the collector of Q9. The operation of this differential pair is similar to Q8 and Q9. The DC control voltage is from the Drive Control circuits. Each channel has its own drive control circuit. Increasing the voltage to the base of Q11 increases the video gain (drive) of the LM1208/LM1209. At a 4V control voltage the gain of the LM1208/LM1209 is at maximum, with all the current flowing through Q11. If all the current was flowing through Q10, the video signal attenuation would be over 40 dB, the maximum attenuation. Q12 through Q17 are part of the final section shown in *Figure 8*. DC restoration is done at this stage. The clamp comparator *(Figure 11)* drives the clamp cap at pin 8 to a voltage that sets the correct black level of the video signal. This cap is also connected to the base of Q17. Q17 and Q16 are one half of the darlington differential pair. The clamp cap voltage establishes the current flow through R16, Q15, and R15. With the bases of Q14 and Q15 held to the same voltage the current through Q15 is mirrored into Q14 and the other half of the differential pair, Q12 and Q13. By this current mirror the voltage at the collector of Q14 is set to the correct DC value for the video signal by controlling the voltage drop across R13, completing the DC restoration.

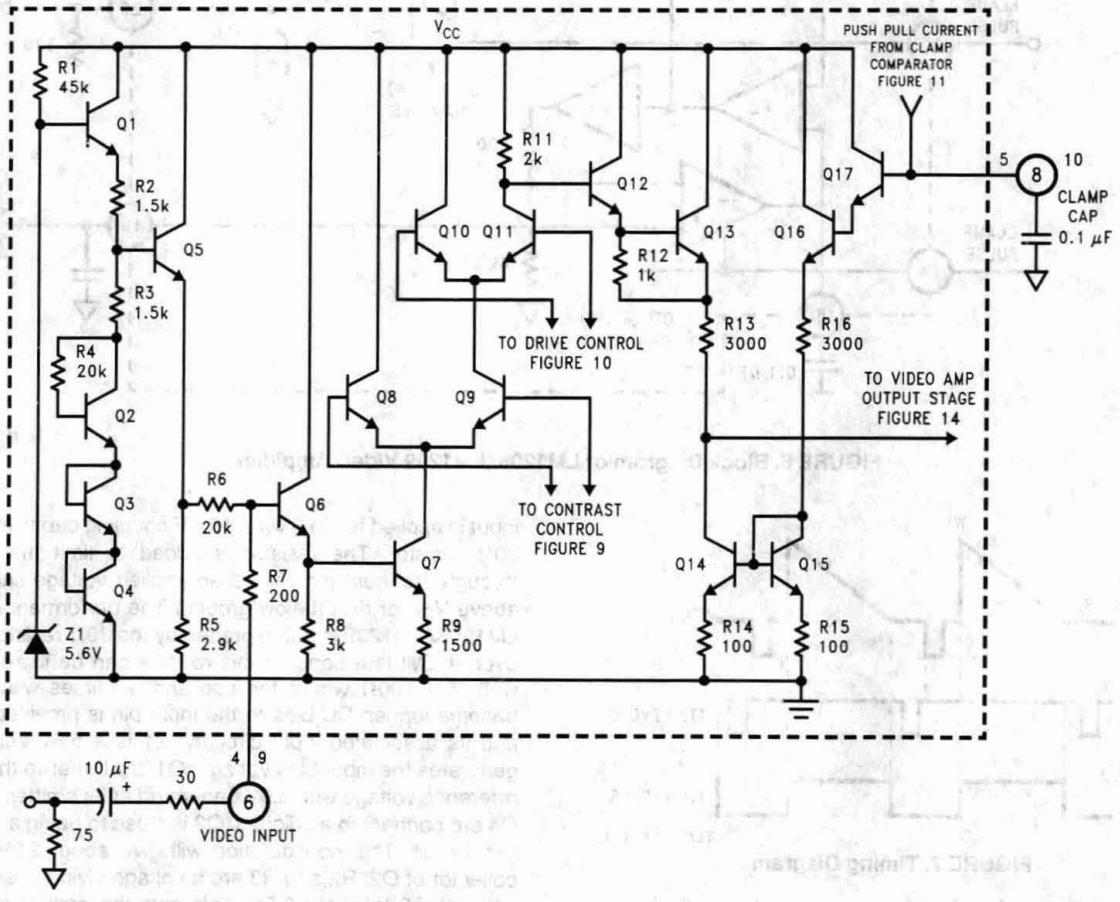

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FIGURE 8. Simplified Schematic of LM1208/LM1209 Video Amplifier Input Stage

Circuit Description (Continued)

CONTRAST CONTROL

Figure 9 is a simplified schematic of the Contrast Control circuit. The output of this circuit is common to all three channels. A reference voltage is generated by Z2, Q34, Q35, R30, and R31. Q36, Q39, and Q41 are all current sources that are controlled by the reference voltage. The contrast signal has a 0V to 4V range with its input at pin 12. R32 is used for current limiting any voltage surge that may occur at pin 12. Note that the input stage (Q37, Q38, and Q42) are all PNP transistors. This configuration is necessary for operation down to near ground. At Q44 the input voltage is converted to a current by R33. The input stage will apply the same voltage across R33 as is applied at the input and with no temperature variations from the transistors. Q37 is connected to a current source (Q36) to keep a constant current flow through Q37 and a predictable diode voltage for the base-emitter of Q37. Q40 is connected as a diode and is biased by the current source Q39. The current through Q40 is mirrored into Q43, giving a current bias for Q42. Again this is done to give a predictable diode voltage for Q42. Q41 is a current source for both Q38 and Q42. With the current through Q42 already established, the rest of the current from Q41 flows through Q38. As one can see the input voltage is accurately reflected across R33 with no temperature coefficients from the input stage of the contrast control circuit.

Pin 1 of the contrast control output is held at a constant voltage two diode drops below $\frac{1}{2}V_{CC}$. To generate this reference the base of Q51 is held at exactly $\frac{1}{2}V_{CC}$. R44 and R45 form a voltage divider. With both Q53 and Q54 connected as diodes the voltage at the junction of R44 and R45 is $\frac{1}{2}V_{CC}$ plus one diode drop. Q52 is a buffer to this reference voltage, generating exactly $\frac{1}{2}V_{CC}$ at its emitter. Q51 is used to drive the bases of Q49 and Q50 to one diode drop below the reference voltage. Q50 is used to further buffer the reference voltage to the base of Q9 (see *Figure 8*) and the corresponding transistors in the other channels. Q48 is used to bias the collector of Q49 to $\frac{1}{2}V_{CC}$, the same voltage as the collector of Q47 when the differential pair is balanced. This keeps the characteristics of Q47 and Q49 well matched. Going back to Q44 and R33; these parts set up a current source that varies the current through R36. With a 2V contrast voltage the differential pair is balanced, meaning that the voltage drop across R36 is $\frac{1}{2}V_{CC}$. Q45 buffers the voltage at R36, driving the bases of Q46 and Q47. Q46 further buffers the voltage, driving the base of Q8 (see *Figure 8*) and the corresponding transistors in the other two channels. In the balanced condition the voltage at pin 2 will also be two diode drops below $\frac{1}{2}V_{CC}$, giving a well balanced drive to the differential pair consisting of Q8 and Q9 in the video amplifier input stage. With the contrast voltage set to 0V, the voltage at pin 2 will increase by about 400 mV to 500 mV. A 4V contrast voltage decreases the voltage at pin 2 by about 400 mV to 500 mV from the balanced condition. Reviewing *Figure 8* note that decreasing the voltage at pin 2 will decrease the current flow through Q8. Thus the current flow through Q9 increases, increasing the gain of the LM1208/LM1209. So increasing the contrast control voltage at pin 12 increases the gain of the LM1208/LM1209. The contrast control voltage from Q46 and Q50 is common to all three channels. To minimize crosstalk it is necessary to add a decoupling capacitor of 0.1 μF across R37 and R40. Since this can only be done externally, these two nodes are brought out to pins 1 and 2. The 30Ω resistor is added in series with the capacitor for improving stability. To prevent a destructive current surge due to shorting either pins 1 or 2 to ground R38 was added for current limiting.

DRIVE CONTROL

Figure 10 is a simplified schematic of the Drive Control circuit. Each channel has its own drive control circuit. This circuit is almost identical to *Figure 9*, the contrast control circuit. It will be easier to cover the differences between the two circuits instead of going through virtually the same circuit description. Note that the input stage is **exactly** the same. The generation of the reference voltage at the right hand side of *Figure 10* is slightly different than the circuit in *Figure 9*. In the drive control circuit the reference voltage at the base of Q72 is to be $\frac{2}{3}V_{CC}$. In the contrast control circuit the reference voltage at the base of Q51 was to be $\frac{1}{2}V_{CC}$. To generate the $\frac{2}{3}V_{CC}$ R57 and R58 form a 2 to 1 voltage divider. With the two to one ratio it is now necessary to have three transistors connected as diodes, which are Q74, Q75, and Q76. Q73 is the buffer for this voltage divider and its emitter is exactly $\frac{2}{3}V_{CC}$ with temperature compensation. R52 and R53 also differ from their corresponding resistors in *Figure 9*, R36 and R39. The value difference is so the base of Q66 is also at $\frac{2}{3}V_{CC}$ when the input drive voltage is at 2V. R38 in *Figure 9* was needed for current limiting at the output pins. Since each channel has its own drive control circuit no filtering is required, eliminating the need for external pins. With no external pins no current limiting is necessary, thus the 1k resistor is not used in the drive control circuit.

Circuit Description (Continued)

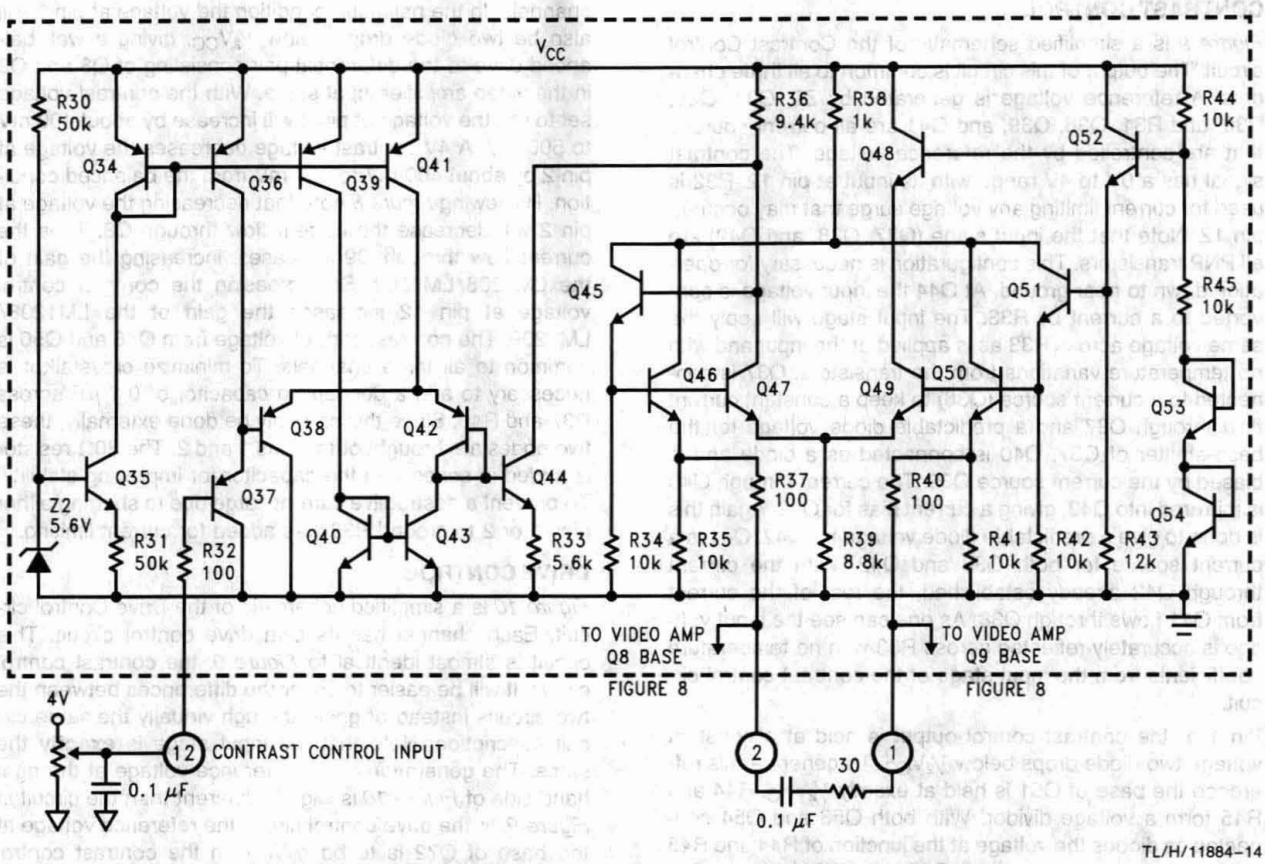

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FIGURE 9. Simplified Schematic of LM1208/LM1209 Contrast Control

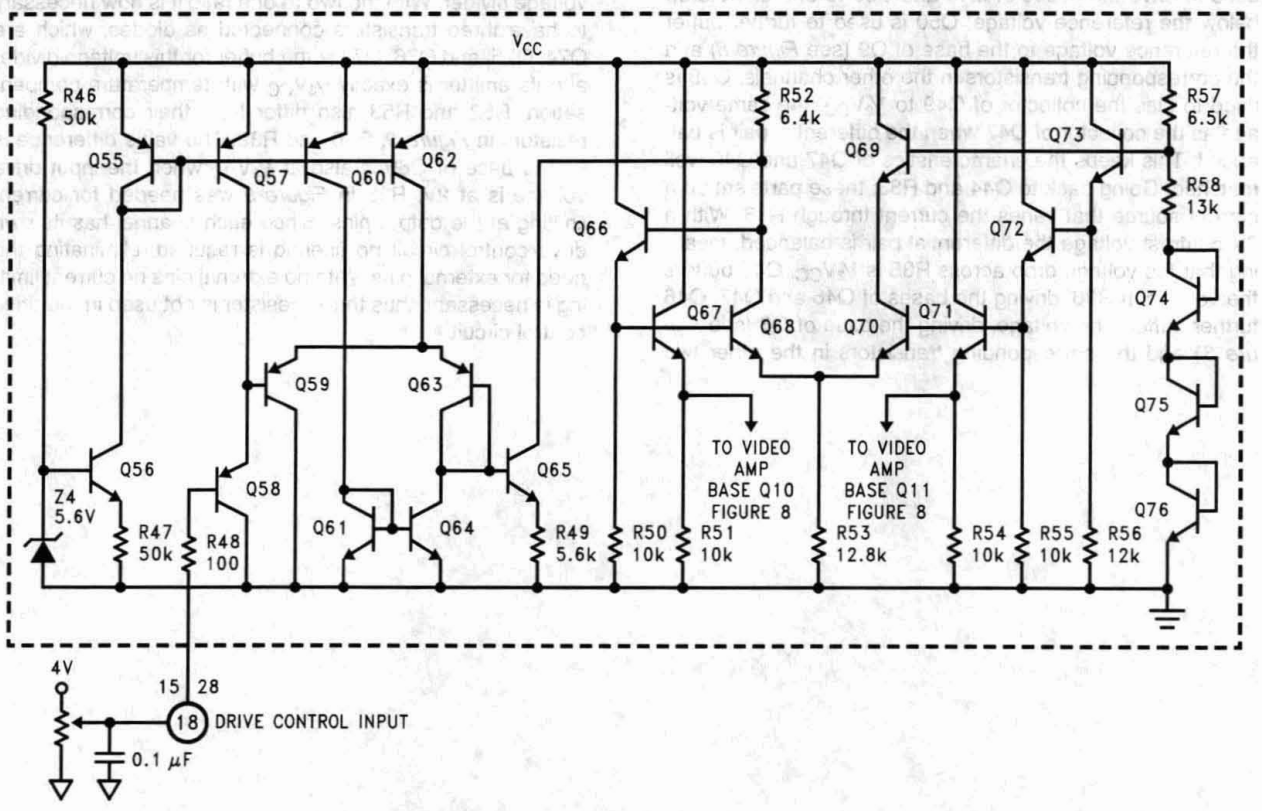

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FIGURE 10. Simplified Schematic of LM1208/LM1209 Drive Control

Circuit Description (Continued)

CLAMP COMPARATOR CIRCUIT

Figure 11 is a simplified schematic of the clamp comparator circuit. Q85 and its input transistors, Q81 and Q82 are one half of the differential pair. The base of Q81 is connected to pin 19 via R62. This is the positive input to the comparator. Q88 and its input transistors, Q90 and Q91 are the other half of the differential pair. The base of Q92 is connected to the junction of R19 and R20 in *Figure 14* via R73. This is the negative input to the comparator. R73 is included only to match the input characteristics of the positive input, which requires the 100Ω resistor. The negative comparator input is the feedback from the output stage as briefly described in the block diagram and covered in more detail in the output stage circuit description. Q86 is the current source for the differential pair. It is turned on and off by the output of the clamp gate circuit *(Figure 12)*. Q102 of the clamp gate circuit has a current flow of about 225 μA when it is turned on. This current is mirrored into Q86. Assume that the inputs to the comparator are equal, making the differential pair balanced. In this condition Q85 and Q88 each have a current flow of 113 μA. Looking at the Q85 side of the circuit, Q84 will also have 113 μA of current flow. Q80 is set up as a current mirror to Q84, but its emitter resistor is one fourth the emitter resistance of Q84. Thus the current flow for Q80 is four times the current flow thru Q84, or 450 μA. Q83 has been added to help drive the base of Q80, increasing the accuracy of the current mirror. The collector of Q80 directly charges the capacitor as a current source of 450 μA. R65 is added to discharge the charge stored in the bases of Q80 and Q84. This is necessary to quickly turn off the current charge of the clamp capacitor as the comparator section is turned off. Q87, Q89, and Q90 work in exactly the same way. However, the collector of Q91 drives another current mirror with the 450 μA. This current flows thru Q78. Q77 is a current mirror with Q78, thus 450 μA also flows thru Q77. Q79 has been added to help drive the base of Q77, again adding to the accuracy of the current mirror. Since Q77 is on the ground side of the circuit it discharges the clamp capacitor with 450 μA. In this balanced condition the charge and discharge current are equal, thus the voltage across the clamp capacitor remains unchanged.

Going back to the input stages, note that both inputs, Q81 and Q92, are driven by a 50 μA current source. This keeps both transistors turned on even when the differential pair, Q85 and Q88, is turned off. Q82 and Q90 are added to help drive the bases of Q85 and Q88 respectively. R64 and R72 are added to help discharge the charge stored in the bases of Q85 and Q88 as these two transistors are turned off. Since the input stage remains active the differential pair is quickly turned off. The comparator can also be more quickly turned on with the input stages remaining active. R67 is used to assure that the potential difference across the differential pair is minimal during turnoff. Without R67 there could be a little extra charge or discharge of the clamp capacitor during turnoff, creating an error in the black level of the video signal. Now assume that the input to pin 19 is slightly higher than the reference voltage to the negative input of the comparator. The voltage at the base of Q85 is now higher than the base of Q88. This creates an increased current flow thru Q85 and an equal decrease of current flow thru Q88. This current change is multiplied by four in the increase of current flow thru Q80. Likewise the current flow thru Q77 and Q91 is decreased by four times the current change in Q88. In the extreme case the current flow thru Q80 can increase to 900 μA and there would be no current flow thru Q77. Q80 does charge the clamp capacitor, thus the voltage across the capacitor will increase. The above is all reversed when the input to Q92 rises above the input level of Q81. If the base of Q86, the current source to the differential pair, is forced close to ground, then there is no current flow thru Q86 and the differential pair, Q85 and Q88. With the current flow thru the differential pair set the zero, all the current mirrors would also have no current flow. Thus the voltage on the camp capacitor would remain constant, the desired result during active video.

Circuit Description (Continued)

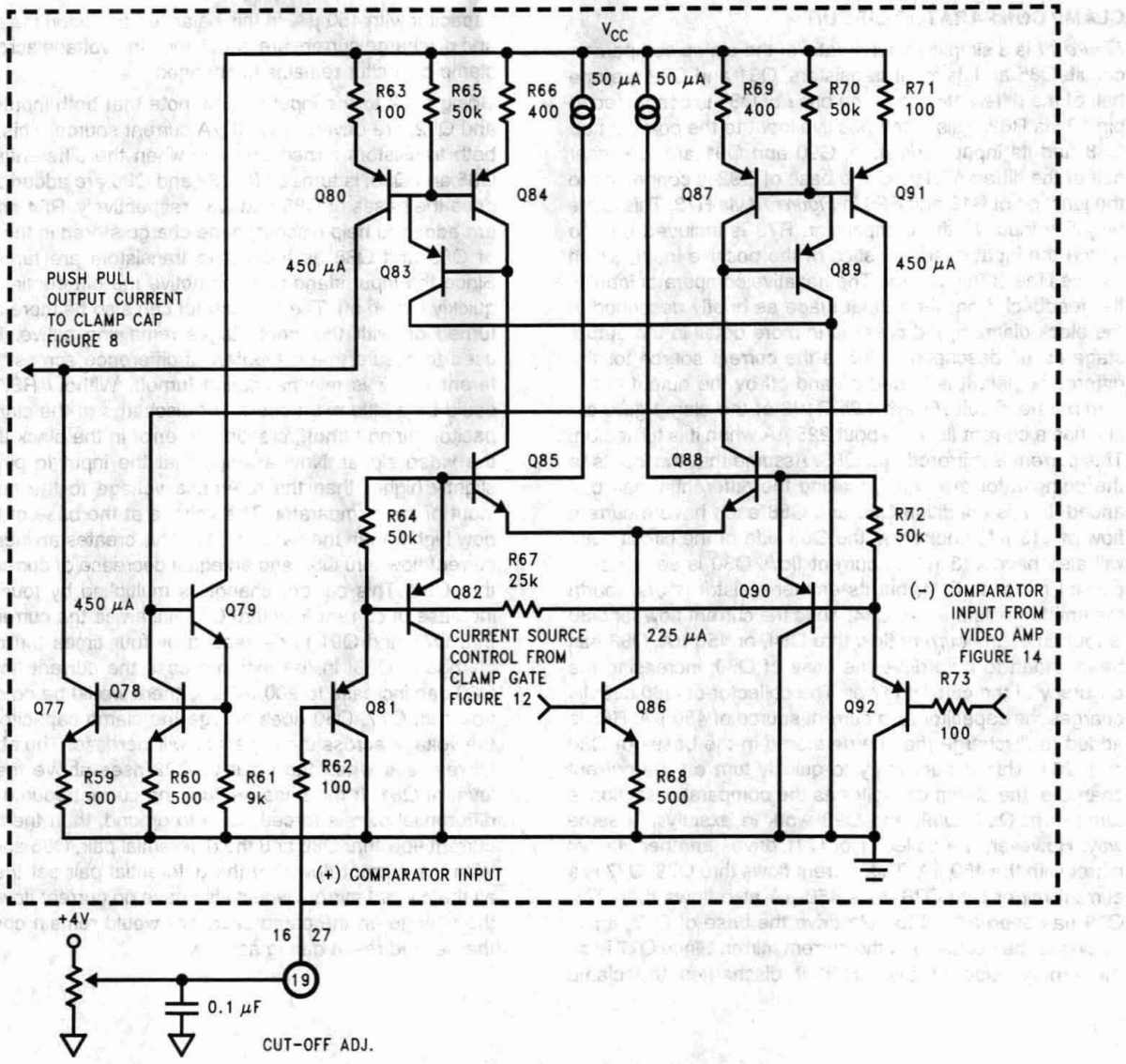

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FIGURE 11. Simplified Schematic of LM1208/LM1209 Clamp Comparator Circuit

CLAMP GATE CIRCUIT

Figure 12 is a simplified schematic of the Clamp Gate circuit. A voltage reference is setup by Z3 and by Q104 and Q105 connected as diodes, generating a 7V base drive to Q94, Q99 and Q101. Q94 is used to bias the input stage. This stage is designed to accept TTL levels at pin 14. Q95 and Q97 form a differential pair. The base of Q97 is set to 2.1V by Q99 driving the voltage divider formed by R77 and R78. In a balanced condition the base of Q95 is also at 2.1V. Q96 is connected as a diode and the current flow thru it is mirrored into Q98. Also the input to pin 14 would be one diode drop below 2.1V, or around 1.4V. R74 is added to the input for current limiting during any possible voltage surge at pin 14. With no resistors at the emitters of Q96 and Q98 this circuit will quickly switch. Below 1.4V (1.2V typical) Q95 is turned on and Q97 is turned off. Above 1.4V (1.6V typical) Q97 is turned on and Q95 is turned off. With Q97 turned on Q100 is also turned on. This pulls the current thru R79 to ground, turning off Q102 and Q103. Remember Q102 is a current mirror to Q86 in the clamp comparator. With Q102 turned off, the clamp comparator is also turned off. When the input signal goes below 1.2V, Q97 and Q100 will be turned off. This allows Q102 to turn on, turning on the clamp

Circuit Description (Continued)

comparators of the three video channels. Q103 is added to help drive the base of Q86 in the clamp comparator, increasing the accuracy of the current mirror. Q101 drives R79 and R80. This sets the current thru Q102, thus setting the current thru Q86 of the clamp comparator.

BLANK GATE CIRCUIT

Figure 13 is a simplified schematic of the Blank Gate circuit. With the exception of the simple output stage and the spot killer circuit, this circuit is almost identical to the clamp gate circuit. The only difference is that the output stage is driven from the opposite side of the differential pair. Thus Q111 is connected as a diode instead of Q109. With the input at pin 13 at a low level Q108 is turned on, also turning on Q29, the output transistor. Q29 is part of the blanking circuit in the output stage shown in *Figure 14*. When Q29 is turned on the output is clamped to a blanking level that is "blacker than black", allowing blanking to be done on the cathodes of the CRT.

The spot killer circuit is used to force the outputs of the LM1208/LM1209 into blanking when the V_{CC} drops below 10.6V. Forcing the outputs to a blacker-than-black level will drive the cathode driver stage well above the black level, cutting off the beam current in the CRT. This prevents the bright spot from occurring when the monitor is turned off, preserving the phosphor of the CRT. The CRT will also have its beam current cut off during the time the monitor is first turned on. This is not a critical period for the CRT since the filaments have not warmed up to generate a current flow.

The comparator along with R89, R90, and Q115 all form the spot killer circuit. Q115 acts the same as Q106. When Q115 has a high signal at its base it is turned off and the outputs of the LM1208/LM1209 are in the normal operating mode. A low signal at the base of Q115 turns on this transistor, blanking the outputs of the LM1208/LM1209. Q115 is driven by the output of the comparator. The inverting input of the comparator is connected to an internal 1.2V reference. The non-inverting side is connected to a resistor divider network, R89 and R90. When V_{CC} is above 10.6V the non-inverting input is above the 1.2V reference, therefore the output of the comparator is high. This high output turns off Q115. Once the V_{CC} drops below 10.6V the comparator's output goes low, turning on Q115 which forces the outputs into the blanking mode.

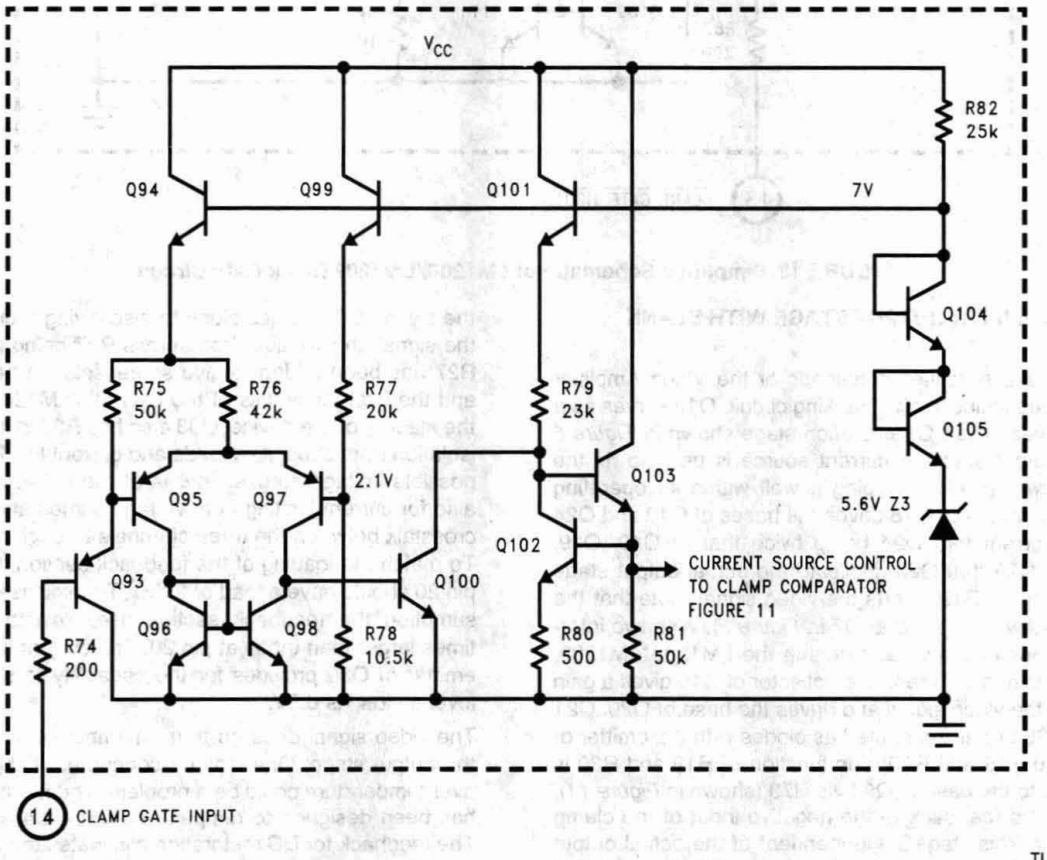

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FIGURE 12. Simplified Schematic of LM1208/LM1209 Clamp Gate Circuit

Circuit Description (Continued)

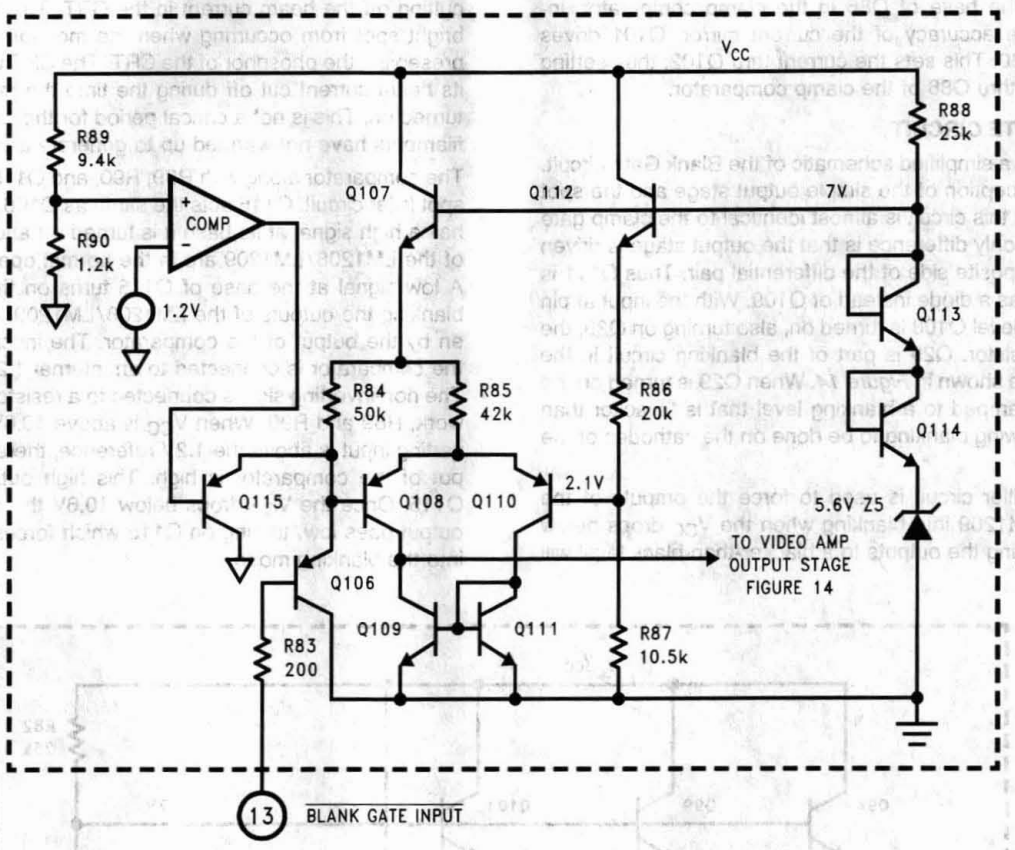

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FIGURE 13. Simplified Schematic of LM1208/LM1209 Blank Gate Circuit

VIDEO AMPLIFIER OUTPUT STAGE WITH BLANK CIRCUIT

Figure 14 is a simplified schematic of the Video Amplifier Output Stage including the blanking circuit. Q18 serves as a buffer between the DC restoration stage shown in *Figure 8* and the output stage. A current source is used to fix the current flow thru Q18 keeping it well within its operating range. The emitter of Q18 drives the bases of Q19 and Q24 with the current thru Q24 being twice that of Q19. Q19, along with Q20 thru Q23 duplicate the actual output stage going to pin 20. Q19 inverts the video signal (note that the video signal was inverted at Q7 in *Figure 8*). With two internal inversions of the video signal in the LM1208/LM1209, the output is non-inverted. The collector of Q19 gives a gain of −10 to the video signal and drives the base of Q20. Q21 through Q23 are all connected as diodes with the emitter of Q23 driving R19 and R20. The junction of R19 and R20 is connected to the base of Q92 via R73 (shown in *Figure 11*), this being the feedback to the negative input of the clamp comparator. This stage is independent of the actual output stage at pin 20, but is where the feedback is done for DC restoration. Therefore it is possible to blank the actual output stage below the black level without affecting the DC restoration feedback loop. Q24 is the equivalent part of Q19 in the actual output stage. It also inverts the video signal with a gain of −10 and drives the base of Q30. Q30 thru Q32 each give a diode drop to the level of the video signal, similar to being connected as diodes. Being connected as emitter-followers these transistors also give current gain to the signal. Q33 comes close to also giving a diode drop to the signal, the voltage drop across R27 being insignificant. R27 has been added to give some isolation between Q33 and the internal circuits of the LM1208/LM1209, adding to the stability of the device. Q33 also has R29 in its emitter for isolation from capacitive loads and current limiting from any possible voltage surges. R28 is at the collector of Q33 is also for current limiting from voltage surges and minimizing crosstalk between the three channels through the V_{CC} line. To match the loading of the feedback section the output at pin 20 should have a load of 390Ω. To minimize power consumption the feedback section uses resistor values 10 times larger than those at pin 20. The current source at the emitter of Q33 provides for the capability to set the black level as low as 0.5V.

The video signal does go thru a number of diode drops at the output stage. One may be concerned that the tracking over temperature could be a problem. The feedback section has been designed to temperature track the output stage. The feedback for DC restoration eliminates the temperature coefficients of the diode junctions. The remaining section to be covered is the blanking section. This section comprises of Q25 thru Q29. Q26 thru Q28 are connected as diodes. Q25 provides current gain to this stage to adequately pull down the base of Q30 during blanking and also adding another diode potential. During blanking the base of Q30 will be four diode drops above ground, plus the saturation volt-

Circuit Description (Continued)

age of Q29. There are also four diode drops from the base of Q30 to the output, pin 20. Therefore during blanking pin 20 will be less than 100 mV above ground, enabling the designer to blank at the cathode of the CRT. R23 is added to quickly turn off Q25 by discharging its base when the blanking signal is removed.

Figure 14 also shows the power and ground pins to the LM1208/LM1209. All the V_{CC1} pins (pins 3, 11, 25) are all internally connected together. A 0.1 μF bypass capacitor must be located close to each pin and connected to ground. Further bypassing is done by a 100 μF capacitor. This capacitor needs to be located on the board close to the LM1208/LM1209. Pins 22 and 23 are the V_{CC2} pins. These pins may need a ferrite bead in series with the input power. A 10 μF and a 0.1 μF bypass capacitors must be located close to pins 22 and 23. Correct bypassing of pins 22 and 23 is **very important**. If the bypassing is not adequate then the outputs of the LM1208/LM1209 will have ringing, or even worse they may oscillate. The ground side of the bypass capacitors at pins 22 and 23 must be returned to a ground plane with no interruptions from other traces between these capacitors and the ground pins 21 and 24 of the LM1208/LM1209.

Applications of the LM1208/LM1209

Figure 15 is the schematic of the demonstration board designed at National. *Figure 16* is the actual layout of the demonstration board. Note that the schematic shown in *Figure 15* is almost identical to the schematic shown in *Figure 4*. The only difference between the two schematics is that in *Figure 15* each channel has individual adjustments for both drive and cutoff, making this circuit a good design for monitor applications. Each CRT will have a slightly different cutoff voltage for each color, making it necessary to provide separate adjustments in order to accurately set the cutoff for each color. The gain of each color of the CRT is also slightly different; if the color temperature of the display is to be accurately set then each channel of the LM1208/LM1209 must have individual gain adjustments. Thus each channel has its own drive control. Once the drive control is set, the gain between the three color channels will closely track as the contrast is adjusted. All the jumpers needed to design a single sided PC board are shown in the schematic. The resistors and jumpers with no reference designation are the connections between the PC board and the connectors mounted on the PC board. CN1 thru CN8 are BNC connectors.

A 30Ω resistor is in series with each of the video inputs. A voltage surge may occur at these inputs when either the inputs are first connected to another system, or when the system is powered up before the monitor is turned on. If this voltage surge exceeds the supply voltage (at ground potential if the monitor is not powered up) of the LM1208/LM1209, or goes below ground, current will flow through the parasitic devices of the LM1208/LM1209. This current is limited by the 30Ω resistors, preventing a potential catastrophic failure. A 100Ω resistor is added to the Blank Gate and Clamp Gate inputs. These two resistors also limit

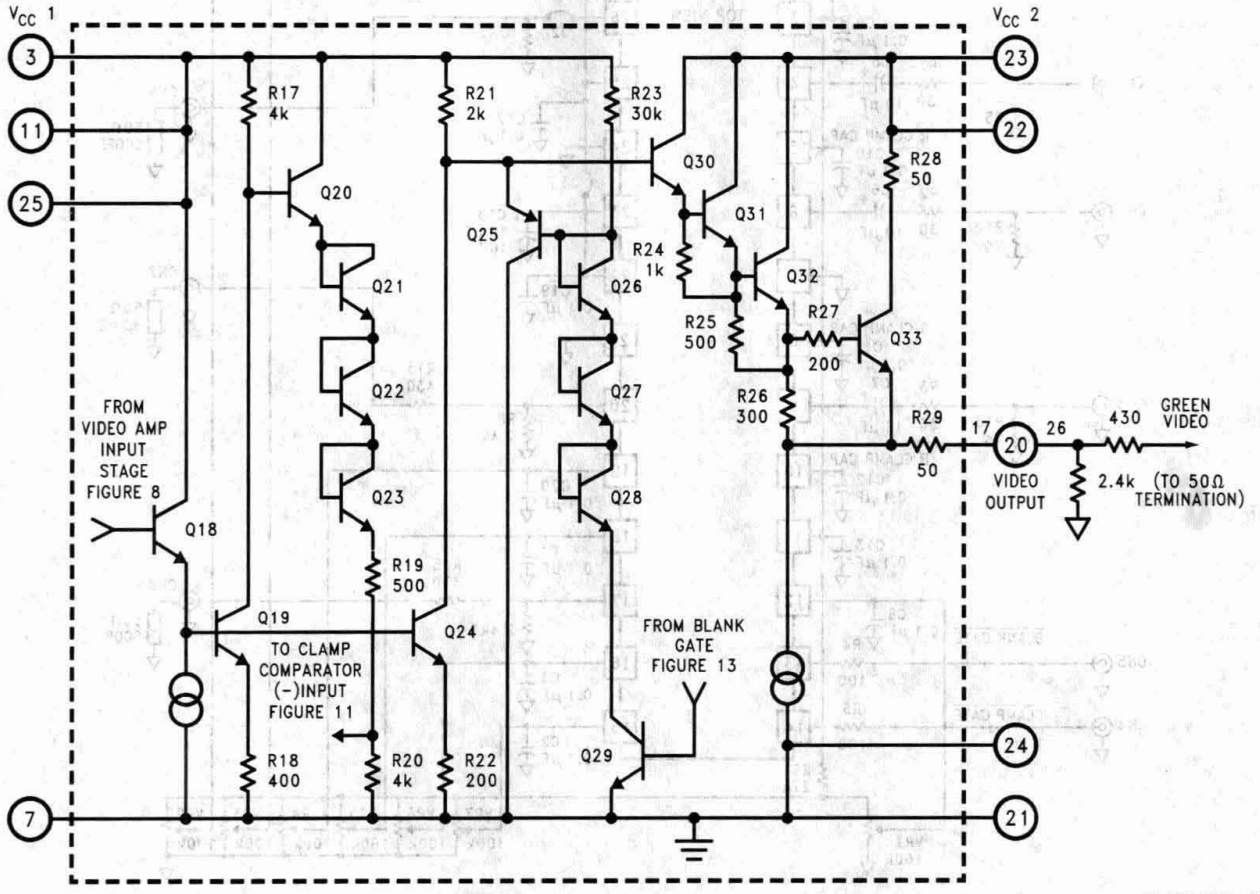

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FIGURE 14. Simplified Schematic of LM1208/LM1209 Video Amplifier Output Stage with Blank Circuit

Applications of the LM1208/LM1209 (Continued)

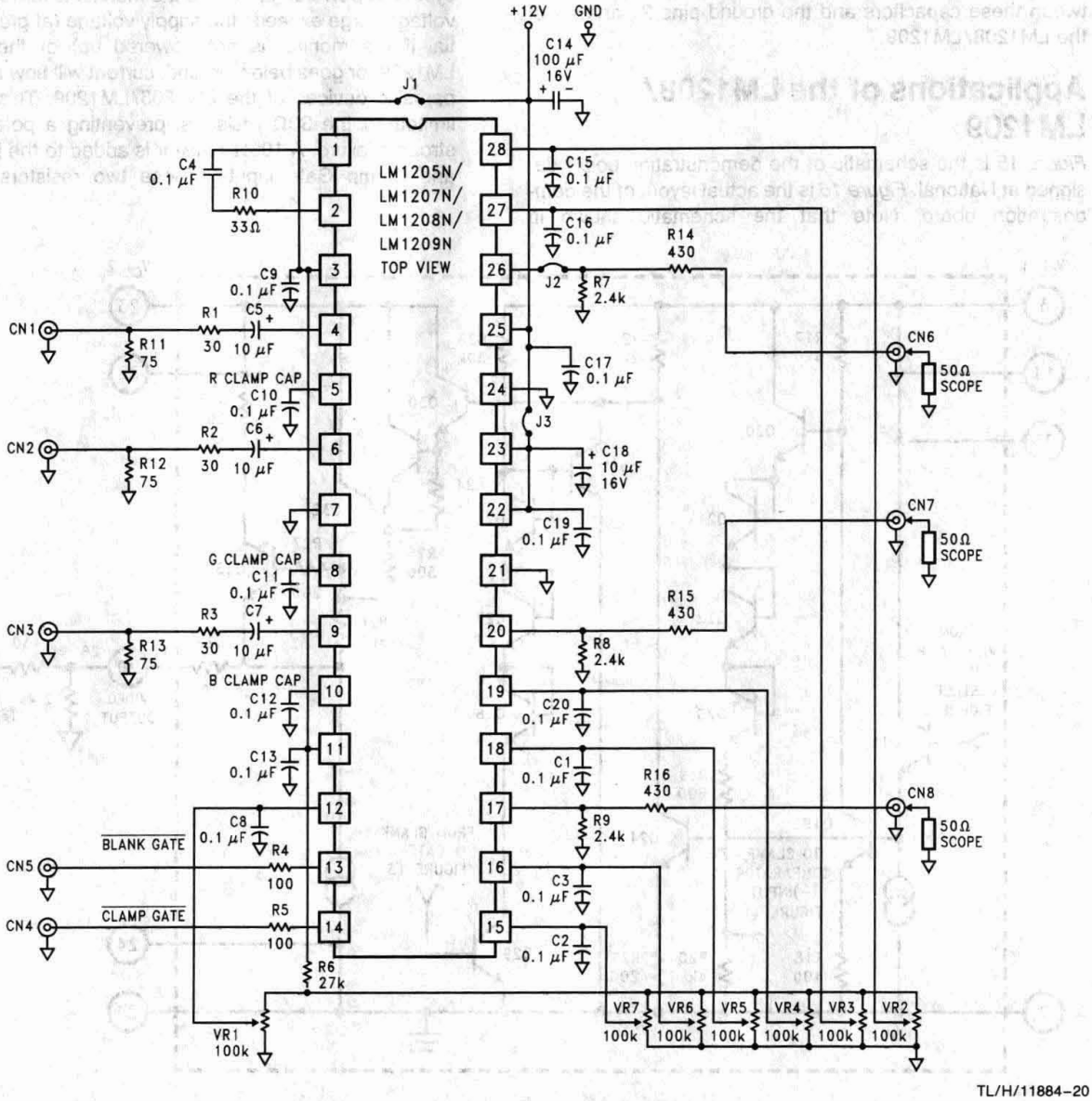
the current during a voltage surge. A larger resistor is required because these inputs are DC coupled, allowing the current to continuously flow into these inputs before the monitor is turned on. 100Ω resistors are not recommended at the video inputs because this resistance value will start to roll off the frequency response of the LM1208/LM1209.

Note that the layout shown in *Figure 16* does have a very extensive ground plane. One must remember that the LM1208/LM1209 is a 130 MHz/100 MHz part and a single sided board is difficult to successfully design. A ground plane similar to the layout shown in *Figure 16* must be provided for good performance of the LM1208/LM1209 when using either a single sided or double sided board. The layout of this board demonstrates the importance of grounding. The results of this layout are shown in *Figures 17a* through *17d*. In these photographs the LM1208 rise time was 2.40 ns and the fall time was 3.00 ns. For the LM1209, the rise time was 3.05 ns and the fall time was 3.45 ns. The output was a 4 V_{PP} signal and the cutoff voltage was set to 2V. The overshoot will subsequently be filtered out by the loading effects of the CRT driver stage and the CRT itself. When the LM1208/LM1209 is designed into a video board one must keep the ground to the CRT driver stage separate from the ground of the LM1208/LM1209, connecting the two grounds together only at one point. National Semiconductor also manufactures a line of CRT drivers. Please contact National for additional information. These drivers greatly simplify the driver design allowing for shorter design cycles. Of course the LM1208/LM1209 can also be designed with a discrete driver stage. *Figure 18* shows a design using a simple cascode CRT driver. The LM1208/LM1209 block would be the same schematic as shown in *Figure 15.*

REFERENCES

Zahid Rahim, "Guide to CRT Video Design," Application Note 861, National Semiconductor Corp., Jan. 1993

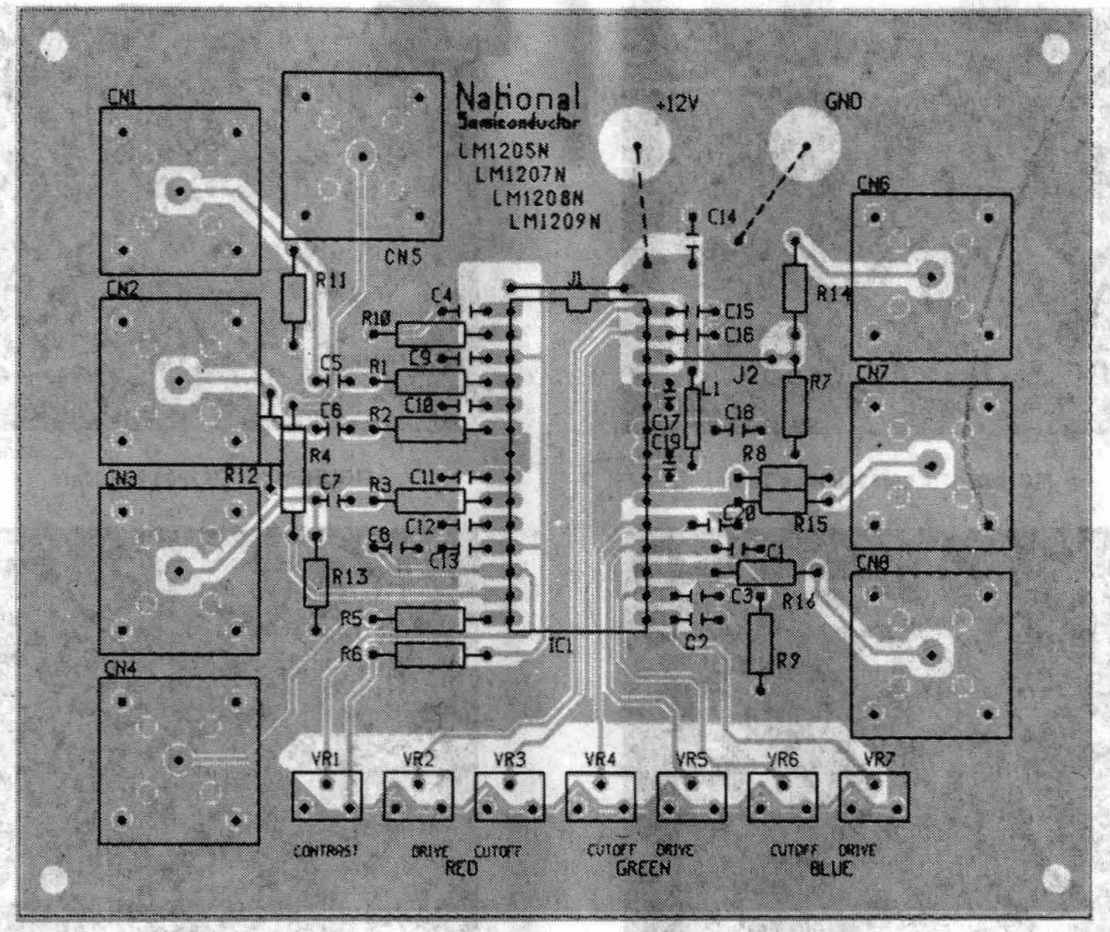
Ott, Henry W. *Noise Reduction Techniques in Electronic Systems,* John Wiley & Sons, New York, 1976



TL/H/11884–20

FIGURE 15. Demonstration Board Schematic

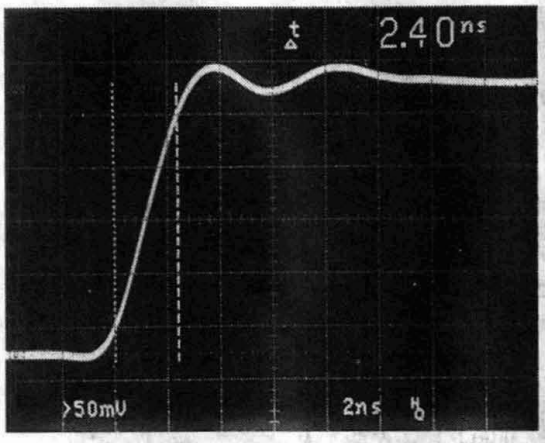
Applications of the LM1208/LM1209 (Continued)



TL/H/11884–21

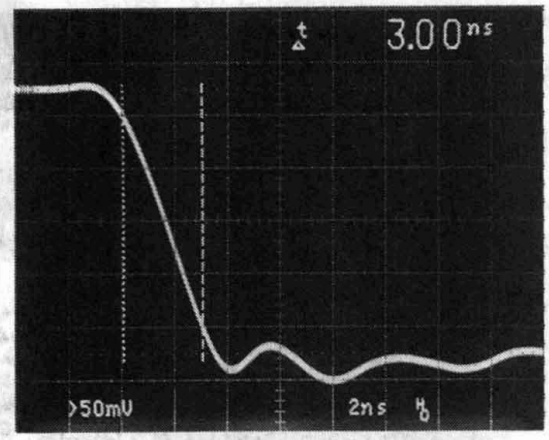
FIGURE 16. Demonstration Board Layout

Applications of the LM1208/LM1209 (Continued)



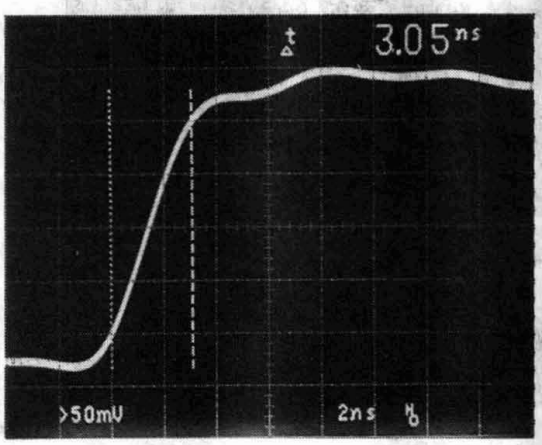
TL/H/11884–22

FIGURE 17a. LM1208 Rise Time



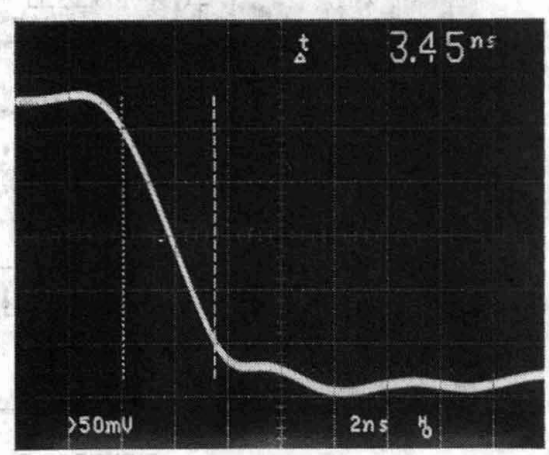
TL/H/11884–23

FIGURE 17b. LM1208 Fall Time



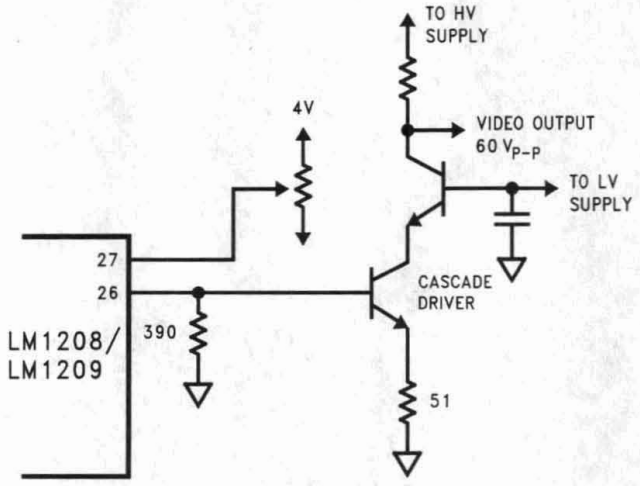
TL/H/11884–28

FIGURE 17c. LM1209 Rise Time



TL/H/11884–29

FIGURE 17d. LM1209 Fall Time



TL/H/11884–24

FIGURE 18. LM1208/LM1209 Typical Application

National Semiconductor

PRELIMINARY

LM1212
230 MHz Video Amplifier System with OSD Blanking

General Description

The LM1212 is a very high frequency video amplifier system intended for use in high resolution monochrome or RGB color monitor applications with OSD. In addition to the wideband video amplifier the LM1212 contains a gated differential input black level clamp comparator for brightness control, a DC controlled attenuator for contrast control and a DC controlled sub contrast attenuator for drive control. The DC control for the contrast attenuator is pinned out separately to provide a more accurate control system for RGB color monitor applications. All DC controls offer a high input impedance and operate over a 0V–4V range for easy interface to bus controlled alignment systems. During the OSD window, the output is blanked to < 0.4V. The LM1212 operates from a nominal 12V supply but can be operated with supply voltages down to 8V for applications that require reduced IC package power dissipation characteristics.

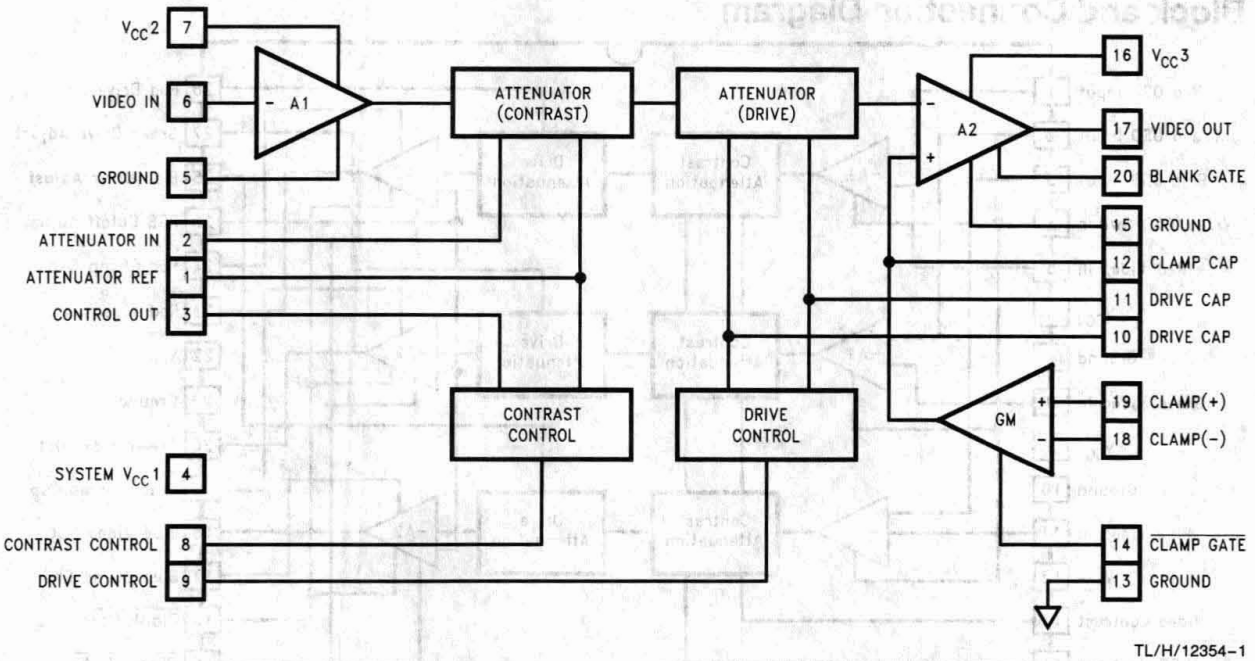
Features

- Wideband video amplifier ($f_{-3\,dB}$ = 230 MHz at V_O = 4 V_{PP})
- t_r, t_f = 1.5 ns at V_O = 4 V_{PP}
- Externally gated comparator for brightness control
- 0V to 4V high input impedance DC contrast control (> 40 dB range)
- 0V to 4V high input impedance DC drive control (±3 dB range)
- Ouput blanked to < 0.4V for OSD window
- Easy to parallel three LM1212s for optimum color tracking in RGB systems
- Output stage clamps to 0.65V and provides up to 9V output voltage swing
- Output stage directly drives most hybrid or discrete CRT amplifier stages

Applications

- High resolution CRT monitors with OSD
- Video switches
- Video AGC amplifier
- Wideband amplifier with gain and DC offset control

Block and Connection Diagram



TL/H/12354–1

Order Number LM1212M or LM1212N
See NS Package Number M20B or N20A

National Semiconductor

ADVANCE INFORMATION

LM1281
85 MHz RGB Video Amplifier System with On Screen Display (OSD)

General Description

The LM1281 is a full feature video amplifier with OSD inputs, all within a 28-pin package. This part is intended for use in monitors with resolutions up to 1024 x 768. The video section of the LM1281 features three matched video amplifiers with blanking. All of the video amplifier adjustments feature high input impedance 0V to 4V DC controls, providing easy interfacing to bus controlled alignment systems. The OSD section features three TTL inputs and a DC contrast control. The switching between the OSD and video section is controlled by a single TTL input. Although the OSD signals are TTL inputs, these signals are internally processed to match the OSD low level to within 100 mV of the video black level. When adjusting the drive controls for color balance of the video signal, the color balance of the OSD display will track these color adjustments. The LM1281 also features an internal spot killer circuit to protect the CRT when the monitor is turned off. For applications without OSD insertion please refer to the LM1205 or LM1208 data sheets.

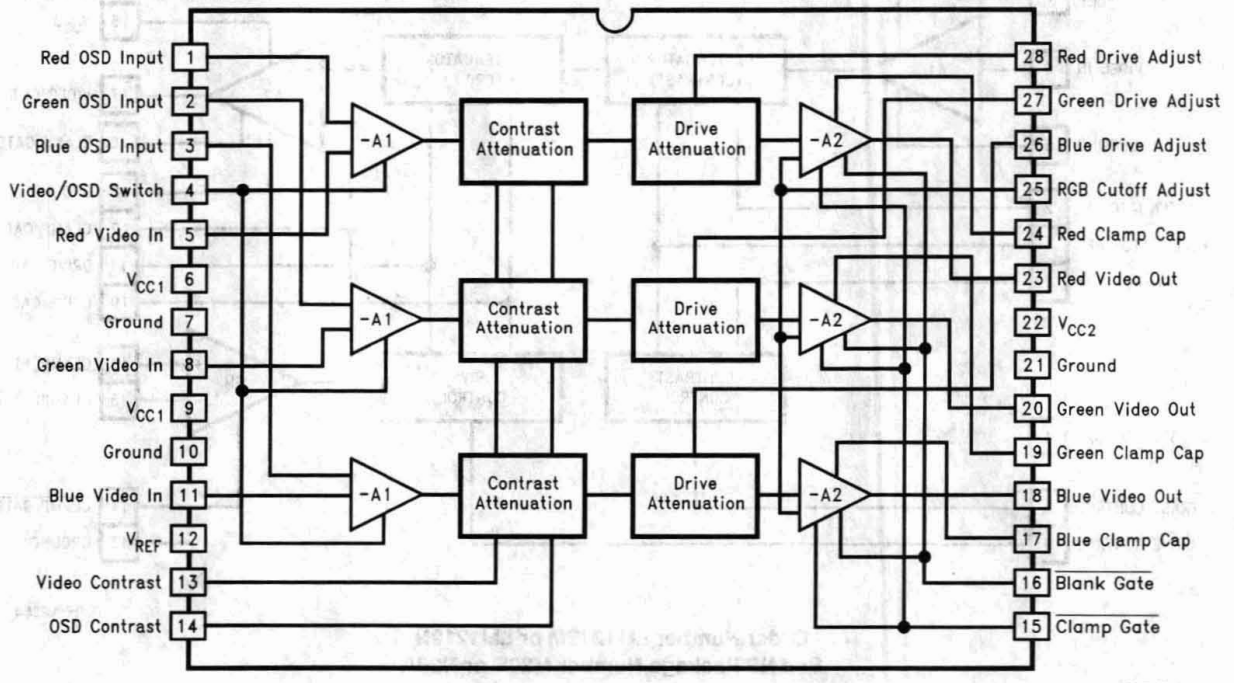
Features

- Three wideband video amplifiers 85 MHz @ −3 dB (4 V_{PP} output)
- TTL OSD inputs, 50 MHz bandwidth
- On chip blanking, outputs under 0.1 V when blanked
- Video/OSD switch speed of 7 ns
- Independent drive control for each channel for color balance
- 0V to 4V, high impedance DC contrast control with over 40 dB range
- 0V to 4V, high impedance DC drive control (0 dB to −12 dB range)
- 0V to 4V, high impedance DC OSD contrast control with over 40 dB range
- Capable of 7 V_{PP} output swing (slight reduction in bandwidth)
- Output stage directly drives most hybrid or discrete CRT drivers

Applications

- High resolution RGB CRT monitors requiring OSD capability

Block and Connection Diagram



TL/H/12355–1

FIGURE 1. Order Number LM1281N
See NS Package Number N28B

National Semiconductor

LM2416/LM2416C Triple 50 MHz CRT Driver

General Description

The LM2416 contains three wide bandwidth, large signal amplifiers designed for large voltage swings. The amplifiers have a gain of −13. The device is intended for use in color CRT monitors and is a low cost solution to designs conforming to VGA, Super VGA and the IBM® 8514 graphics standard.

The part is housed in the industry standard 11-lead TO-220 molded power package. The heat sink is floating and may be grounded for ease of manufacturing and RFI shielding.

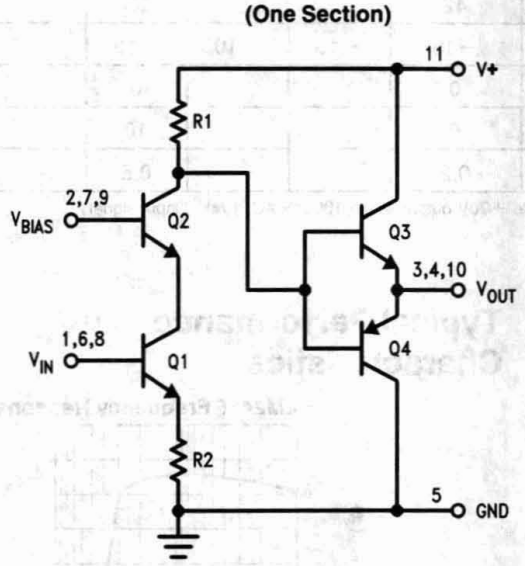
Features

- 50 Vpp output at 45 MHz drives CRT directly
- Rise/fall time typically 8 ns with 8 pF load
- 65V output swing capability

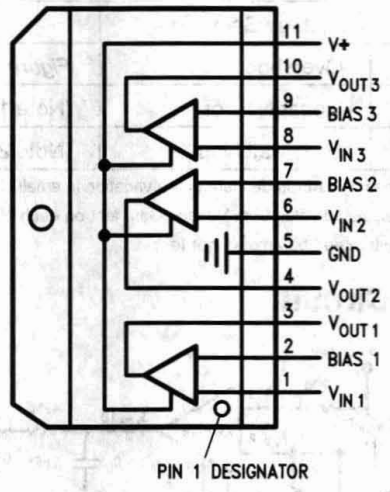
Applications

- CRT driver for RGB monitors
- High voltage amplifiers

Schematic and Connection Diagram



TL/K/10738–1



TL/K/10738–2

Top View

Order Number LM2416T or LM2416CT
See NS Package Number TA11B

2

Absolute Maximum Ratings

Supply Voltage, V^+	+85V
Power Dissipation, P_D	10W
Storage Temperature Range, T_{STG}	−25°C to +100°C
Operating Temperature Range, T_{CASE}	−20°C to +90°C
Lead Temperature (Soldering, <10 sec.)	300°C
ESD Tolerance	4 kV

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Electrical Characteristics

$V^+ = 80V$, $C_L = 8$ pF, DC input bias, $V_{IN} = 3.6\ V_{DC}$. 50 V_{PP} output swing, $V_{BIAS} = +12V$. See *Figure 1*. $T_A = 25°C$ unless otherwise noted.

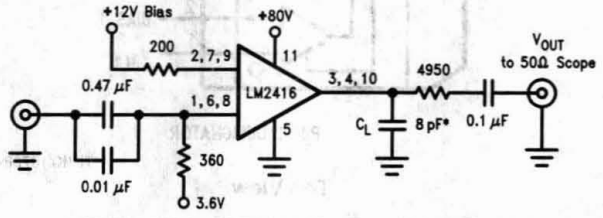
Symbol	Parameter	Conditions	LM2416			LM2416C			Units
			Min	Typical	Max	Min	Typ	Max	
I_{CC}	Supply Current (per Amplifier)	No Input or Output Load	18	22	26	16	22	28	mA
V_{OUT}	Output Offset Voltage	$V_{IN} = 3.6V$	38	42	46	35	42	48	V_{DC}
t_r	Rise Time	10% to 90% (Note 3)		8	13		12	16	ns
t_f	Fall Time	10% to 90% (Note 3)		8	13		12	16	ns
BW	Bandwidth	−3 dB		42			35		MHz
A_V	Voltage Gain		−11	−13	−15	−10	−13	−16	V/V
OS	Overshoot	*Figure 1*		0			0		%
LE	Linearity Error	(Note 1)		8			10		%
ΔA_V	Gain Matching	(Note 2)		0.2			0.5		dB

Note 1: Linearity Error is defined as the variation in small signal gain from +20V to +70V output with a 100 mV AC, 1 MHz, input signal.

Note 2: Calculated value from Voltage Gain test on each channel.

Note 3: Guaranteed parameter, not tested.

Test Circuit



TL/K/10738–3

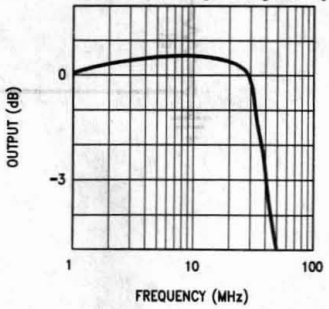
* 8 pF is total load capacitance. It includes all parasitic capacitance.

FIGURE 1. Test Circuit (One Section)

Figure 1 shows a typical test circuit for evaluation of the LM2416. This circuit is designed to allow testing of the LM2416 in a 50Ω environment such as a pulse generator, oscilloscope or network analyzer.

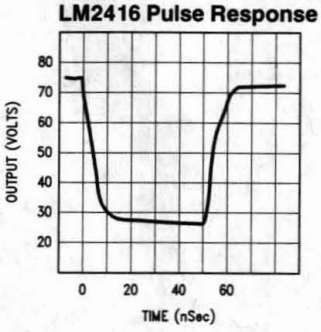
Typical Performance Characteristics

LM2416 Frequency Response



TL/K/10738–4

LM2416 Pulse Response



TL/K/10738–5

LM2416—Theory of Operation

The LM2416 is a high voltage triple CRT driver suitable for VGA, Super VGA, IBM 8514 and 1K by 768 non-interlaced display applications. The LM2416 features 80 volt operation and low power dissipation. The part is housed in the industry standard 11 lead TO-220 molded power package. The heat sink is floating and may be grounded for ease of manufacturing and RFI shielding.

The circuit diagram of the LM2416 is shown in *Figure 2*. Q1 and R2 provides a conversion of input voltage to current, while Q2 acts as a common base or cascode amplifier stage to drive the load resistor R1. Emitter followers Q3 and Q4 isolate the impedance of R1 from the capacitance of the CRT cathode, and make the circuit relatively insensitive to load capacitance. The gain of this circuit is $-R1/R2$ and is fixed at -13. The bandwidth of the circuit is set by the collector time constant formed by the load resistor R1 and associated capacitance of Q2, Q3, Q4, and stray layout capacitance. Proprietary transistor design allows for high bandwidth with low operating power.

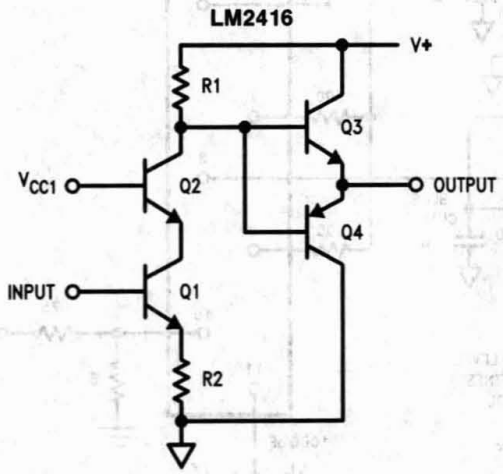


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FIGURE 2. LM2416 CRT Driver (One Section)

Thermal Considerations

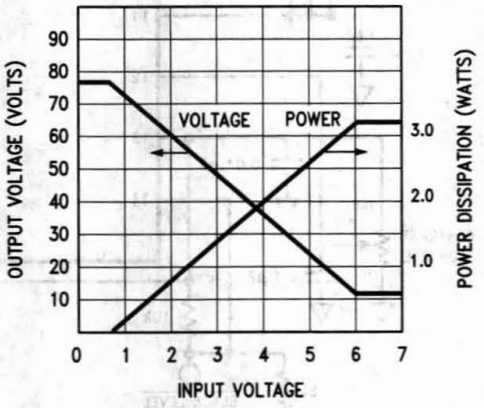
The transfer characteristics of the amplifier are shown in *Figure 3*. Power supply current increases as the input signal increases and consequently power dissipation also increases.

The LM2416 cannot be used without heat sinking. *Figure 3* shows the power dissipated in each channel over the operating voltage range of the device. Typical "average" power dissipation with the device output voltage at one half the supply voltage is 1.8W per channel for a total dissipation of 5.4W package dissipation. Under white screen conditions, i.e.: 15V output, dissipation increases to 3W per channel or 9W total. The LM2416 case temperature must be maintained below 90°C. If the maximum expected ambient temperature is 50°C, then a heat sink is needed with thermal resistance equal to or less than:

$$R_{th} = \frac{(90 - 50°C)}{9W} = 4.4°C/W$$

The Thermalloy #6400 is one example of a heatsink that meets this requirement.

WARNING: THE LM2416 IS NOT PROTECTED AGAINST OUTPUT SHORT CIRCUITS. The minimum resistance the LM2416 can drive is 600Ω to ground or V^+.



TL/K/10738–7

FIGURE 3. LM2416 DC Characteristics

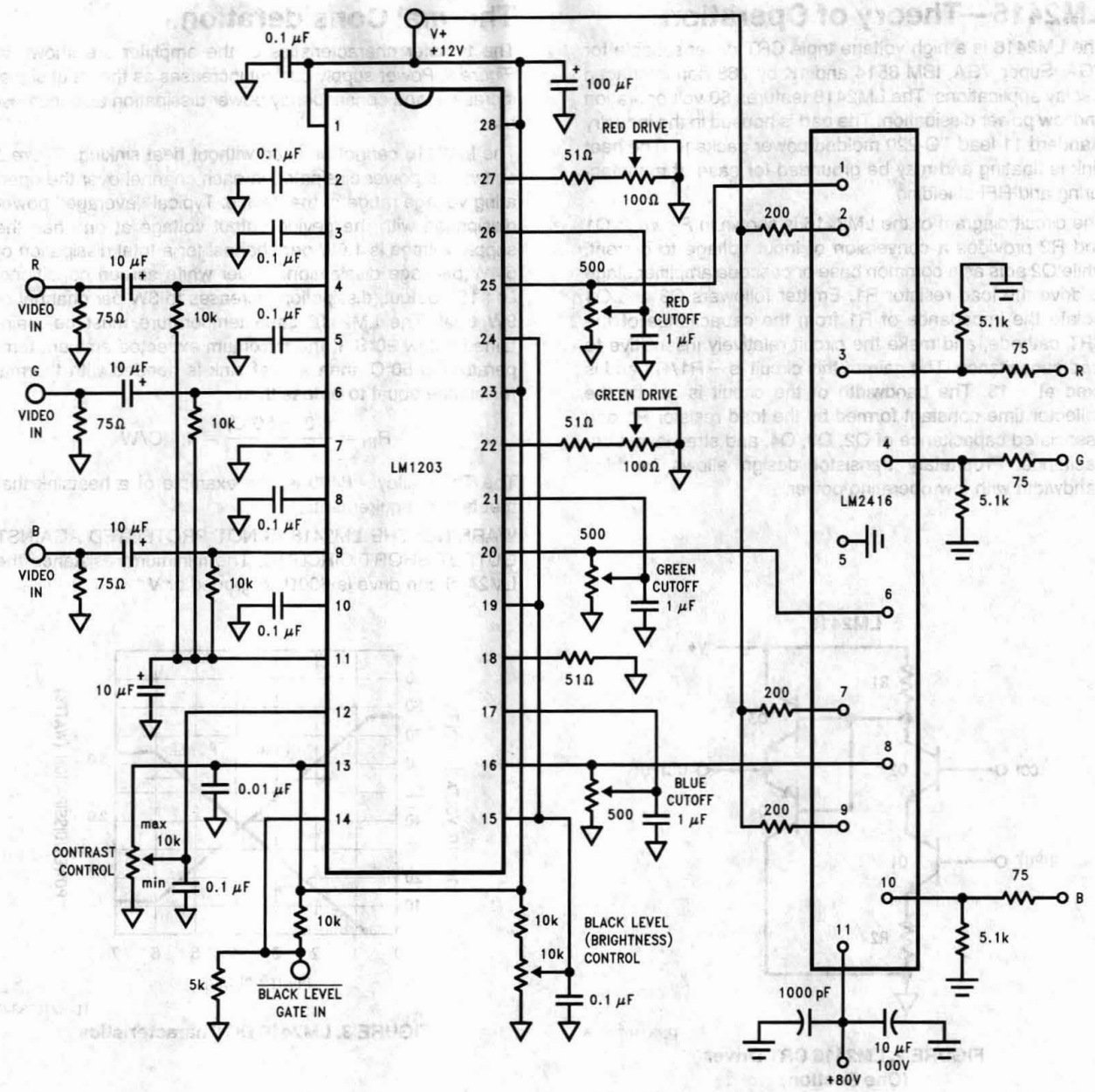


FIGURE 4. Typical Application LM1203-LM2416 Application

A typical application of the LM2416 is shown in *Figure 4*. Used in conjunction with a LM1203, a complete video channel from monitor input to CRT cathode is shown. Performance is satisfactory for all applications to 1k by 768 non-interlaced. Typical rise-fall times are 12 ns, with better than 50V p-p drive signals available to an 8 pF load. In this application, feedback is local to the LM1203. An alternative scheme would be feedback from the output of the LM2416 to the positive clamp inputs of the LM1203. This would provide slightly better black level control of the system.

National Semiconductor

LM2418 Triple 30 MHz CRT Driver

General Description

The LM2418 contains three large signal voltage amplifiers designed to directly drive CRT cathodes for VGA Color Graphics Displays. Output swings greater than 50 V_{PP} are achieved with a 90V power supply. The nominal voltage gain of each amplifier is −19 with gain matching of 1.0 dB between amplifiers.

Packaging is the industry standard molded 11 lead TO-220. The heatsink tab is isolated and may be grounded to improve RFI shielding and simplify assembly.

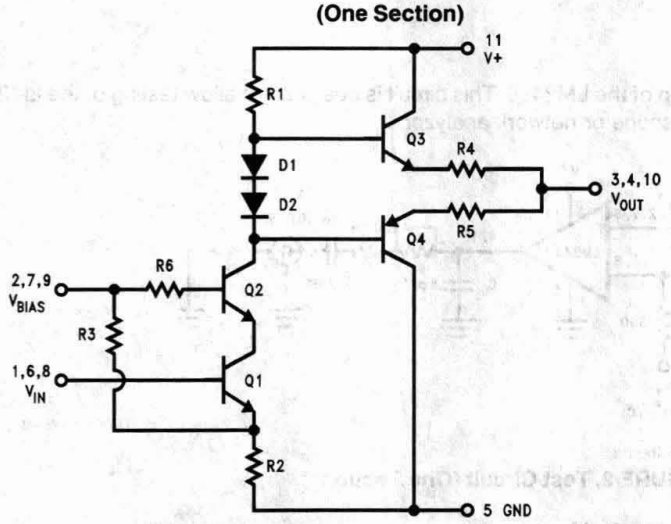
Features

- 50 Vpp output at 30 MHz drives CRT directly
- Rise/fall time typically 12 ns with 8 pF load
- 65V output swing capability
- Optimized output stage for low crossover distortion
- Gain matching of 1 dB
- Voltage gain of −19
- Includes oscillation supression resistors

Applications

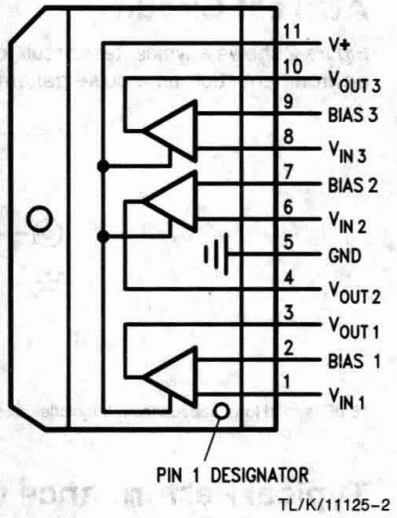
- CRT driver for RGB monitors
- High voltage amplifiers

Schematic and Connection Diagram



TL/K/11125–1

FIGURE 1



TL/K/11125–2

Top View

Order Number LM2418T
See NS Package Number TA11B

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage, V^+	+95V
Storage Temperature Range, T_{STG}	−25°C to +100°C
Operating Temperature Range, T_{CASE}	−20°C to +100°C
Lead Temperature (Soldering, <10 sec.)	300°C
ESD Tolerance	tbd

Electrical Characteristics

$V^+ = 90V$, $C_L = 8$ pF, DC input bias, $V_{IN} = 3.6\ V_{DC}$, 50 V_{PP} output swing, $V_{BIAS} = +12V$, $T_A = 25°C$ unless otherwise noted.

Symbol	Parameter	Conditions	LM2418			Units
			Min	Typ	Max	
I_{CC}	Supply Current (per Amplifier)	No Input or Output Load		18	26	mA
V_{OUT}	Output Offset Voltage	$V_{IN} = 3.6V$	46	53	60	V_{DC}
t_r	Rise Time	10% to 90% (Note 3)		12	20	ns
t_f	Fall Time	10% to 90% (Note 3)		12	20	ns
BW	Bandwidth	−3 dB		30		MHz
A_V	Voltage Gain		−17	−19	−23	V/V
OS	Overshoot			5		%
LE	Linearity Error	(Note 1)		8		%
ΔA_V	Gain Matching	(Note 2)		1.0		dB

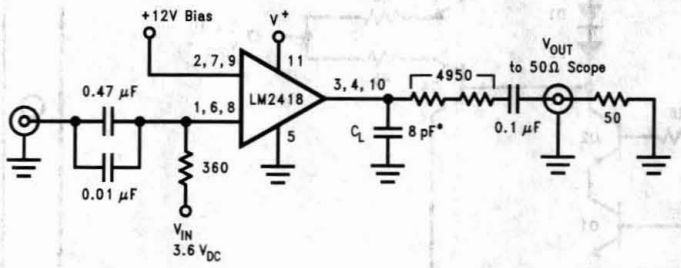
Note 1: Linearity Error is defined as the variation in small signal gain from +20V to +70V output with a 100 mV AC, 1 MHz, input signal.

Note 2: Calculated value from Voltage Gain test on each channel.

Note 3: Guaranteed parameter, not tested.

AC Test Circuit

Figure 2 shows a typical test circuit for evaluation of the LM2418. This circuit is designed to allow testing of the LM2418 in a 50Ω environment such as a pulse generator, oscilloscope or network analyzer.



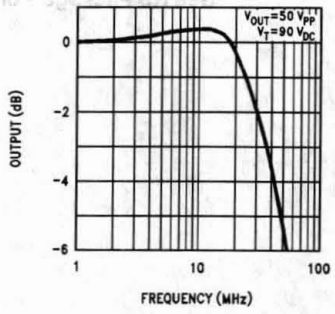
TL/K/11125–3

*8 pF is total load capacitance. It includes all parasitic capacitance.

FIGURE 2. Test Circuit (One Section)

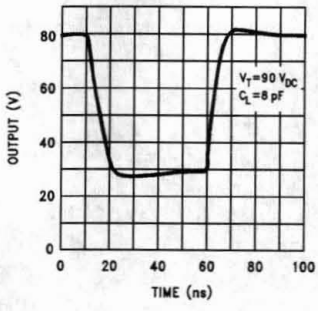
Typical Performance Characteristics

LM2418 Frequency Response



TL/K/11125–4

LM2418 Pulse Response



TL/K/11125–5

FIGURE 3

LM2418—Theory of Operation

The LM2418 is a high voltage triple CRT driver suitable for VGA display applications. The LM2418 features 90V operation and low power dissipation. The part is housed in the industry standard 11-lead TO-220 molded power package. The heat sink is electrically isolated from the circuitry and may be grounded for ease of manufacturing and RFI shielding.

The circuit diagram of the LM2418 is shown in *Figure 1*. Q1 and R2 provide a conversion of input voltage to current, while Q2 acts as a common base or cascode amplifier stage to drive the load resistor R1. Emitter followers Q3 and Q4 isolate the impedance of R1 from the capacitance of the CRT cathode, and make the circuit relatively insensitive to load capacitance. The gain of this circuit is $-R1/R2$ and is fixed at -19. The bandwidth of the circuit is set by the collector time constant formed by the load resistor R1 and associated capacitance of Q2, Q3, Q4, and stray layout capacitance. Diodes D1 and D2 provide forward bias to the output stage to reduce crossover distortion at low signal levels, while R3 provides a DC bias offset to match the output level characteristics of the LM1203 RGB Video Amplifier System. Proprietary transistor design allows for high bandwidth with low operating power.

Figure 2 shows a typical test circuit for evaluation of the LM2418. This circuit is designed to allow testing of the LM2418 in a 50Ω environment such as a pulse generator and a scope, or a network analyzer. In this test circuit, two resistors in series totaling 4.95 kΩ form a wideband low capacitance probe to match the output of the LM2418 to a 50Ω cable and load. Typical AC performance of the circuit is shown in *Figure 3*. The input signal is AC coupled to the base of Q1, while a DC bias of 12V is applied to the base of Q2 (See *Figure 2*).

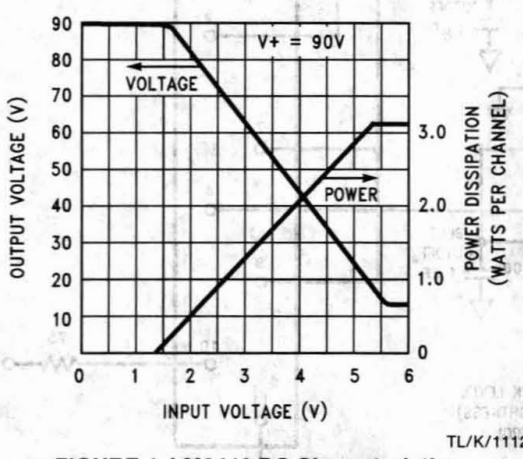
Thermal Considerations

The transfer characteristics of the amplifier are shown in *Figures 4* and *5*. Power supply current increases as the input signal increases and consequently power dissipation also increases.

The LM2418 cannot be used without heat sinking. *Figure 5* shows the power dissipated in each channel over the operating voltage range of the device. Typical "average" power dissipation with the device output voltage at one half the supply voltage is 1.8W per channel for a total dissipation of 5.4W package dissipation. Under white screen conditions, i.e., 20V output, dissipation increases to 3.0W per channel or 9W total. The LM2418 case temperature must be maintained below 100°C. If the maximum expected ambient temperature is 60°C, then a maximum heat sink thermal resistance can be calculated:

$$R_{th} = \frac{(100°C - 60°C)}{9W} = 4.4°C/W$$

PRECAUTION: THE LM2418 IS NOT PROTECTED AGAINST OUTPUT SHORT CIRCUITS. The minimum resistance the LM2418 can drive is 800Ω to ground or V^+.



TL/K/11125–7

FIGURE 4. LM2418 DC Characteristics

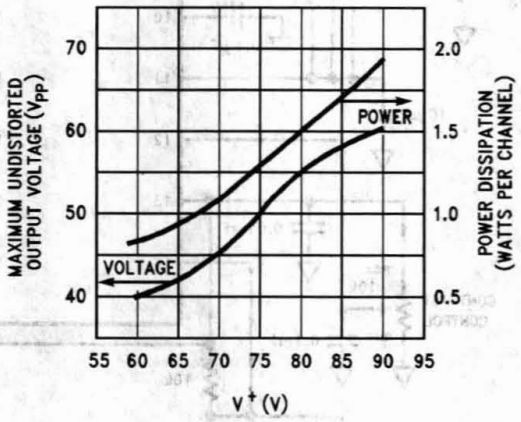


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FIGURE 5. LM2418 Output Swing and Power Characteristics

Typical Application

A typical application of the LM2418 is shown in *Figure 6*. Used in conjunction with an LM1203, a complete video channel from monitor input to CRT cathode is shown. Performance is satisfactory for all applications up to 640 by 480 lines. Typical rise/fall times of this circuit are 15 ns, with better than 50 V_{PP} drive signals available to a 10 pF load. In this application, feedback is local to the LM1203, an alternative scheme would feed back from the output of the LM2418 to the positive clamp inputs of the LM1203. This would provide better black level control of the system.

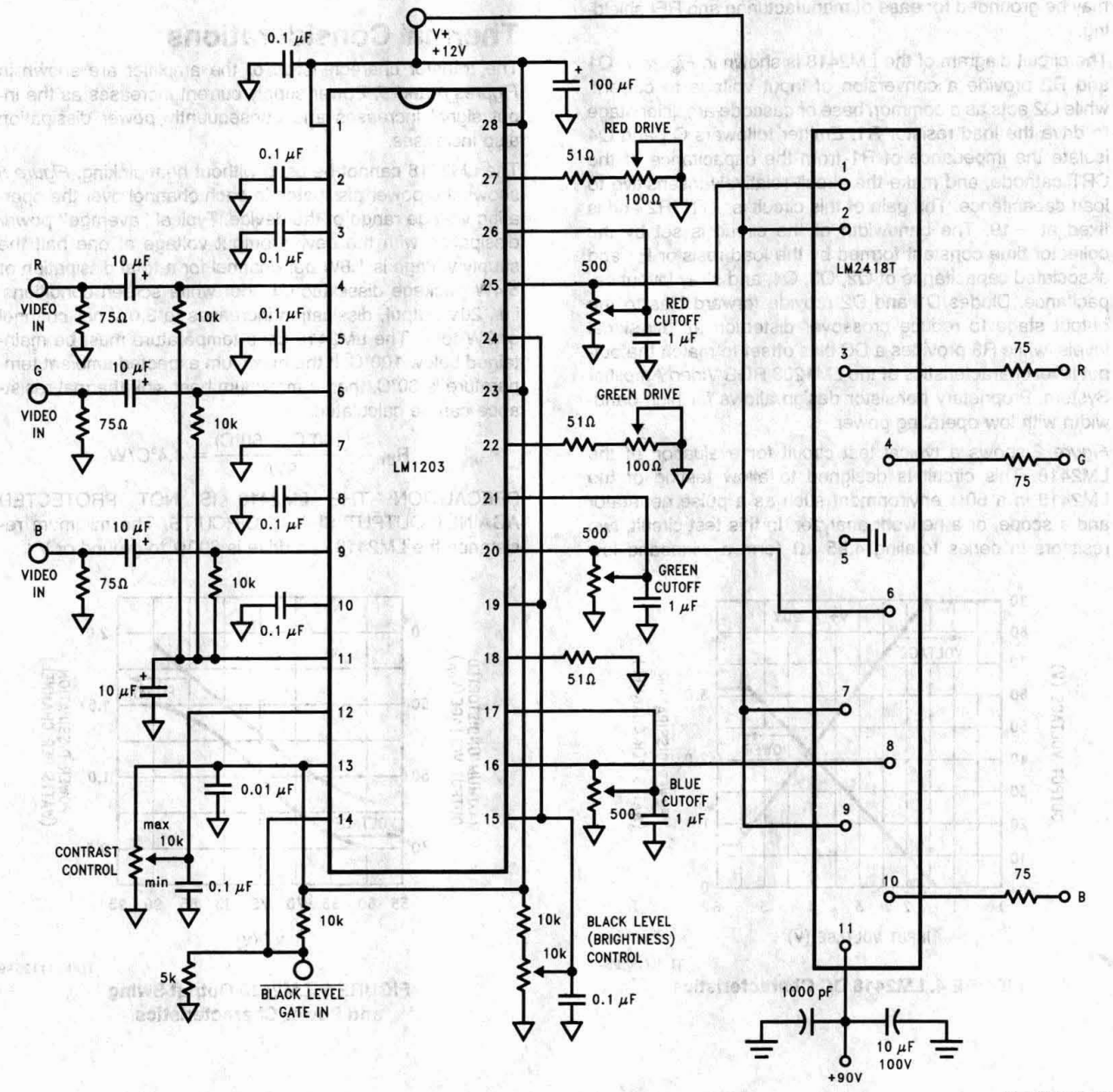

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FIGURE 6. Typical Application LM1203-LM2418 Application

National Semiconductor

LM2419
Triple 65 MHz CRT Driver

General Description

The LM2419 contains three wide bandwidth, large signal amplifiers designed for large voltage swings. The amplifiers have a gain of −15. The device is intended for use in color CRT monitors and is a low cost solution to designs conforming to 1024 x 768 display resolution.

The device is mounted in the industry standard 11-lead TO-220 molded power package. The heat sink is electrically isolated and may be grounded for ease of manufacturing and EMI/RFI shielding.

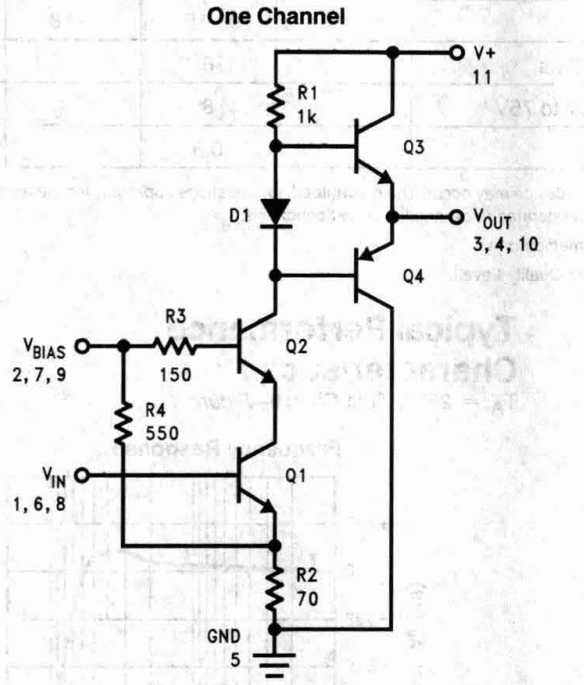
Features

- 50 V_{PP} output swing at 65 MHz
- Rise/Fall time 5 ns with 12 pF load
- 60 V_{PP} output swing capability
- Pin and function compatible with LM2416
- No low frequency tilt compensation required

Applications

- CRT driver for SVGA, IBM 8514 and 1024 x 768 display resolution RGB monitors

Schematic and Connection Diagrams



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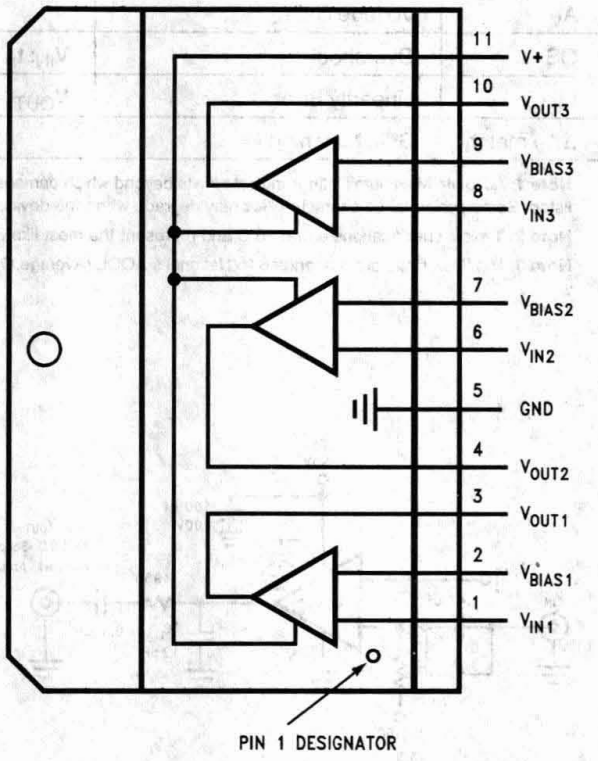

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Order Number LM2419T
See NS Package Number TA11B

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V^+)	+85V
Storage Temperature (T_{STG})	−25°C to +100°C
Operating Case Temperature, T_{Case}	−20°C to +90°C
Lead Temperature (soldering <10 sec.)	300°C
ESD Tolerance	2 kV

Electrical Characteristics

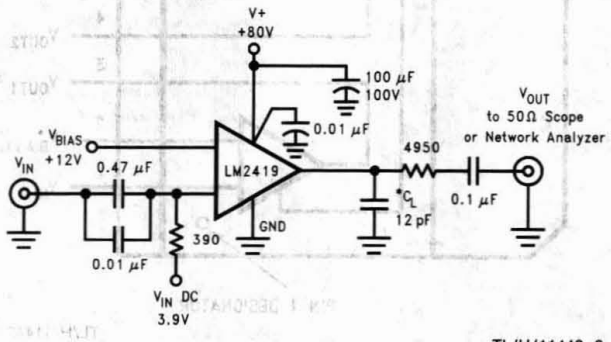
Unless otherwise specified, the following specifications apply for V^+ = 80V, DC input bias, $V_{IN\ DC}$ = 3.9V; 50 V_{PP} output swing; frequency = 1 MHz; V_{Bias} = 12V; C_L = 12 pF; T_A = 25°C; see test circuit, *Figure 1*.

Symbol	Parameter	Conditions	Min (Note 3)	Typ (Note 2)	Max (Note 3)	Units (Limit)
I_{CC}	Supply Current (per Amplifier)	Input/Output Open Circuit		27	40	mA
I_B	Bias Current (Pins 2 or 7 or 9)			11		mA
V_{OUT}	Output Offset Voltage		40	50	60	V
t_r	Rise Time	10% to 90%		5		ns
t_f	Fall Time	90% to 10%		5		ns
A_V	Voltage Gain		−13	−15	−18	V/V
OS	Overshoot	V_{IN}: t_r, t_f < 2 ns		8		%
LE	Linearity Error	V_{OUT} = 25V to 75V		8		%
ΔA_V match	Gain Matching			0.3		dB

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. The guaranteed specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.

Note 2: Typical specifications are at 25°C and represent the most likely parametric norm.

Note 3: Min/Max limits are guaranteed to National's AOQL (Average Outgoing Quality Level).



TL/H/11442–3

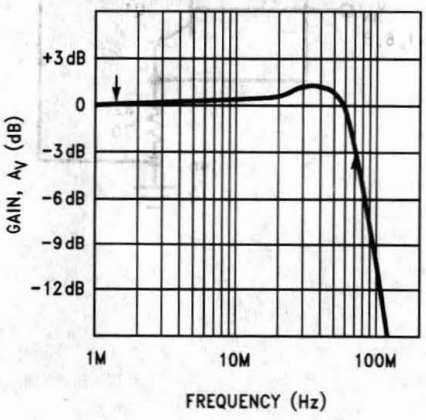
*12 pF is the total load capacitance and includes the test fixture capacitance.

FIGURE 1. Test Circuit (One Section)

Typical Performance Characteristics

T_A = 25°C, Test Circuit—*Figure 1*

Frequency Response



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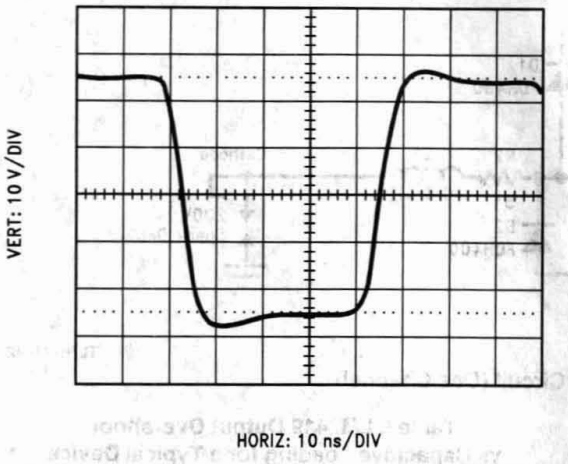
Typical Performance Characteristics (Continued)

T_A = 25°C, Test Circuit—*Figure 1*

Pulse Response



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Test Circuit

Figure 1 shows a typical test circuit for evaluation of the LM2419. The input signal is AC coupled into the input of LM2419 and is referenced to 3.9V DC using an external 3.9V DC bias through a 390Ω resistor. The test circuit is designed to allow testing of the LM2419 in a 50Ω environment such as a 50Ω oscilloscope or network analyzer. The 4950Ω resistor in series with the output of the LM2419 forms a 100:1 voltage divider when connected to a 50Ω oscilloscope or network analyzer.

Theory of Operation

The LM2419 is a high voltage triple CRT driver suitable for SVGA, IBM 8514 and 1024 x 768 display resolution monitors. The device is packaged in the industry standard 11 lead TO-220 molded power package. The heat sink is electrically isolated and may be grounded for ease of manufacturing and RFI/EMI shielding.

The schematic diagram of LM2419 is shown in *Figure 2*. Q1 and R2 provide a conversion of the input voltage to current while Q2 acts as a common base amplifier to drive the load resistor, R1. Resistor R4 along with R2 sets up the DC bias at the base of Q1. Emitter followers Q3 and Q4 isolate R1 from the capacitive load at the output, thus making the rise and fall times relatively insensitive to the load capacitance.

The gain of the amplifier is $-R1/(R2 \parallel R4)$ and is fixed at approximately -15. The bandwidth of LM2419 is primarily limited by the time constant due to R1 and the capacitances associated with D1, Q2, Q3 and Q4. Diode D1 is used to provide some bias voltage for Q3 and Q4 so as to reduce small signal cross over distortion. Resistor R3 is used to prevent Q2 from oscillating at high frequencies.

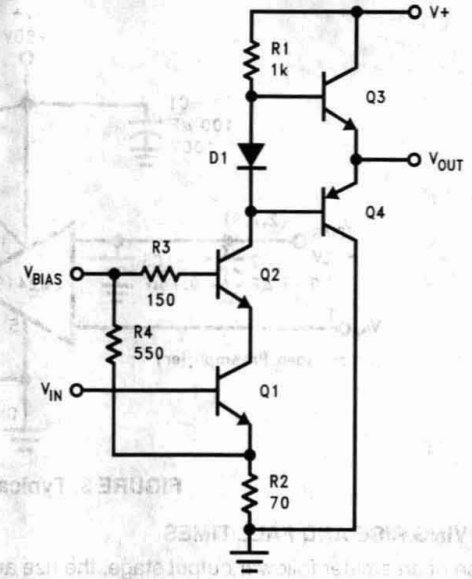

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FIGURE 2. Schematic Diagram of One Section of LM2419

Application Hints

POWER SUPPLY BYPASS

Since the LM2419 is a wide-bandwidth amplifier with greater than 10,000 V/μs slew rate, proper power supply bypassing is critical for optimum performance. Improper power supply bypassing can result in large overshoot, ringing and oscillation. A 0.01 μF ceramic capacitor should be connected as close to the supply pin as is practical (preferably less than ¼" from the supply pin). The lead length of the 0.01 μF ceramic capacitor should be as small as is practical. In addition, 10 μF–100 μF electrolytic capacitor should be connected from the supply pin to ground. The electrolytic capacitor should be placed reasonably close to the LM2419's supply pin.

ARC PROTECTION

The LM2419 must be protected from arcing within the CRT. To limit the arcover voltage, a 200V spark gap is recommended at the cathode. Clamp diodes D1 and D2 (as shown in *Figure 3*) are used to clamp the voltage at the output of LM2419 to a safe level. The clamp diodes used should have high current rating, low series impedance and low shunt capacitance. Resistor R2 in *Figure 3* limits the arcover current while R1 limits the current into LM2419 and reduces the power dissipation of the output transistors when the output is stressed beyond the supply voltage. Having large value resistors for R1 and R2 would be desirable but this has the effect of reducing rise and fall times.

Application Hints (Continued)

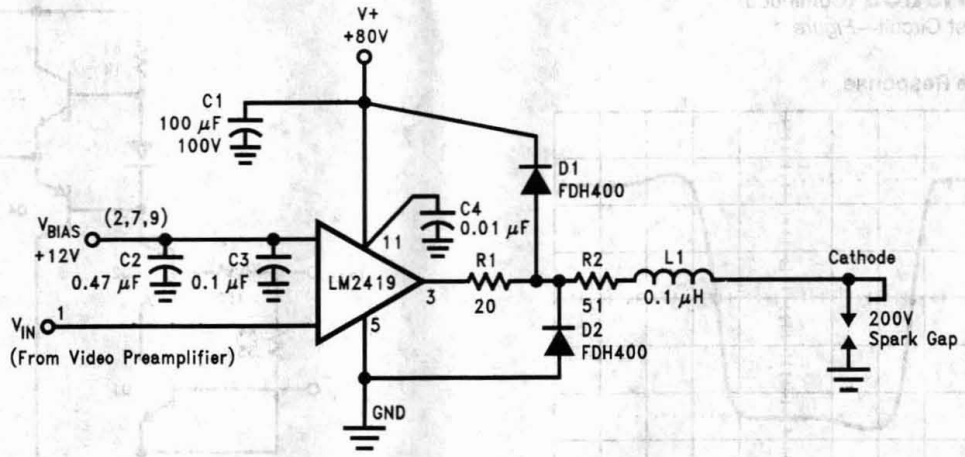

FIGURE 3. Typical Application Circuit (One Channel)

IMPROVING RISE AND FALL TIMES

Because of an emitter follower output stage, the rise and fall times of the LM2419 are relatively unaffected by capacitive loading. However, the series resistors R1 and R2 (see *Figure 3*) will reduce the rise and fall times when driving the CRT's cathode which appears as a capacitive load. The capacitance at the cathode typically ranges from 8 pF to 12 pF.

To improve the rise and fall times at the cathode, a small inductor is often used in series with the output of the amplifier. The inductor L1 in *Figure 3* peaks the amplifier's frequency response at the cathode, thus improving rise and fall times. The inductor value is empirically determined and is dependent on the load. An inductor value of 0.1 μH is a good starting value. Note that peaking the amplifier's frequency response will increase the overshoot.

REDUCING OVERSHOOT

LM2419's overshoot is a function of both the input signal rise and fall times and the capacitive loading. The overshoot is increased by either more capacitive loading or faster rise and fall times of the input signal.

Table I shows the overshoot for a typical device with different capacitive loads and different input signal rise and fall times. As can be observed from Table I, overshoot is large for large capacitive loads and faster input signal rise and fall times. In an actual application, the LM2419 is driven from a preamplifier with rise and fall times of 3 ns to 7 ns. When driven from LM1203 preamplifier (see application circuit, *Figure 6*) the overshoot is 10% with 12 pF capacitive load. The overshoot can be reduced by including a resistor in series with LM2419's output as in *Figure 3*. Larger value resistors for R1 and R2 would reduce overshoot but this also increases the rise and fall times at the output. Frequency peaking using an inductor in series with the output may restore the bandwidth.

Table I. LM2419 Output Overshoot vs Capacitive Loading for a Typical Device

Input Signal t_r/t_f	C_L			
	5 pF	8 pF	11 pF	15 pF
1.2 ns	4%	6%	7%	8%
7 ns	4%	5%	6%	7%

GAIN VS OUTPUT DC LEVEL

Figure 4 shows LM2419's gain versus output DC level. A 100 mV_{PP} AC signal is applied at the LM2419's input and the input signal's DC level is swept. As can be seen from *Figure 4*, the amplifier's gain is constant at approximately 15.4 (V_{OUT} = 1.54 V_{PP}) for output DC level between 35V and 65V. Thus the amplifier's output response is linear for output voltage between 35V and 65V. If the output voltage is less than 35V or more than 70V, the amplifier's output response becomes non-linear (note the change in gain, *Figure 4*). For optimum performance, it is recommended that LM2419's output low voltage be at 25V or above. For a 50 V_{PP} swing, the output high voltage is 75V. With an output signal swing from 25V to 75V, LM2419's linearity error is measured at 8%.

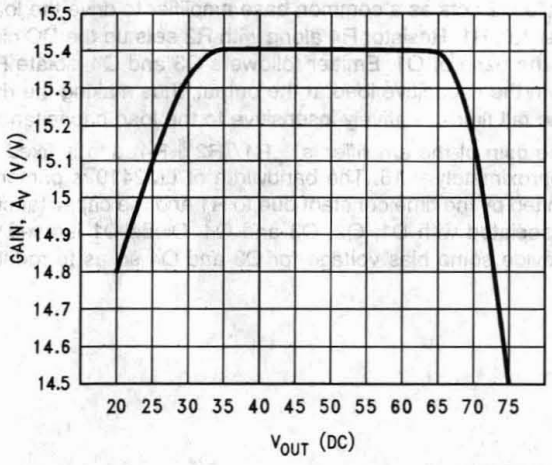

FIGURE 4. Gain vs V_{OUT} (DC), V_{IN} = 100 mV_{PP}

Application Hints (Continued)

THERMAL CONSIDERATIONS

LM2419's transfer characteristic and power dissipation versus DC input voltage is shown in *Figure 5*. Power supply current increases as the input voltage increases, consequently power dissipation increases. For the LM2419, the worst case power dissipation occurs when a white screen is displayed on the CRT. Considering a 20% black retrace time in a 1024 x 768 display resolution application, the average power dissipation for continuous white screen is less than 4W per channel with 50 V_{PP} output signal (black level at 75V and white level at 25V). Although the total power dissipation is less than 12W for a continuous white screen, the heat sink should be selected for 13W power dissipation because of the variation in power dissipation from part to part.

For thermal and gain linearity considerations, the output low voltage (white level) should be maintained above 20V. If the device is operated at an output low voltage below 20V, the power dissipation might exceed 4.7W per channel (i.e., 14W power dissipation for the device). Note that the device can be operated at lower power by reducing the peak to peak video output voltage to less than 50V and clamping the video black level close to the supply voltage.

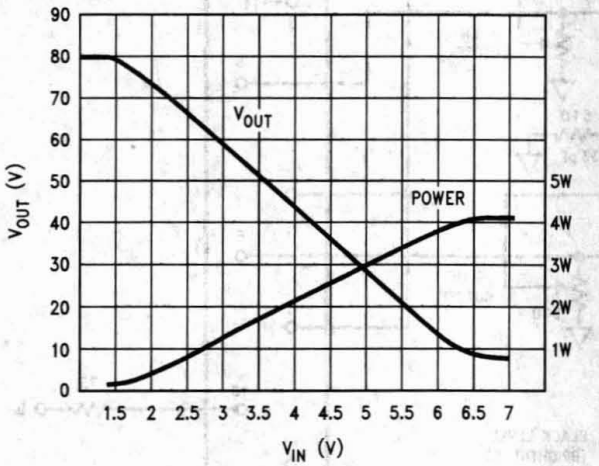

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FIGURE 5. V_{OUT} and Power Dissipation vs V_{IN}

The LM2419 requires that the package be properly heat sunk under all operating conditions. Maximum ratings require that the device case temperature be limited to 90°C maximum. Thus for 50°C maximum ambient temperature and 13W maximum power dissipation, the thermal resistance of the heat sink should be:

$$\theta_{sa} \leq (90-50)°C/13W = 3°C/W$$

SHORT CIRCUIT PROTECTION

The output of LM2419 is not short circuit protected. Shorting the output to either ground or to V^+ will destroy the device. The minimum DC load resistance the LM2419 can drive without damage is 1.6 kΩ to ground or V^+. However, driving a 1.6 kΩ load for an extended period of time is not recommended because of power dissipation considerations. If the LM2419 is used to drive a resistive load then the load should be 10 kΩ or greater.

RGB Video Application

A complete video section for an RGB CRT monitor is shown in *Figure 6*. The LM1203 video preamplifier and the LM2419 include almost all the circuitry required between the video input connection and the CRT's cathodes. However, an externally generated back porch clamp signal is required to accomplish DC restoration of the video signal.

Figure 6's circuit is excellent choice for a non-interlaced 1024 x 768 display resolution application. With 50 V_{PP} output swing and 12 pF load, the rise/fall time for *Figure 6*'s circuit was measured at 7.5 ns. In this application, feedback is local to the LM1203. For detailed information on the LM1203, please refer to the LM1203 data sheet.

PC BOARD LAYOUT CONSIDERATIONS

For optimum performance, adequate ground plane, isolation between channels, good supply bypassing and minimizing unwanted feedback are necessary. Moreover, the length of the signal trace from the preamplifier to the LM2419 and from the LM2419 to the cathode should be as short as is practical. The following book is highly recommended:

Ott, Henry W, *Noise Reduction Techniques in Electronic Systems*, John Wiley & Sons, New York, 1976.

Application Hints (Continued)

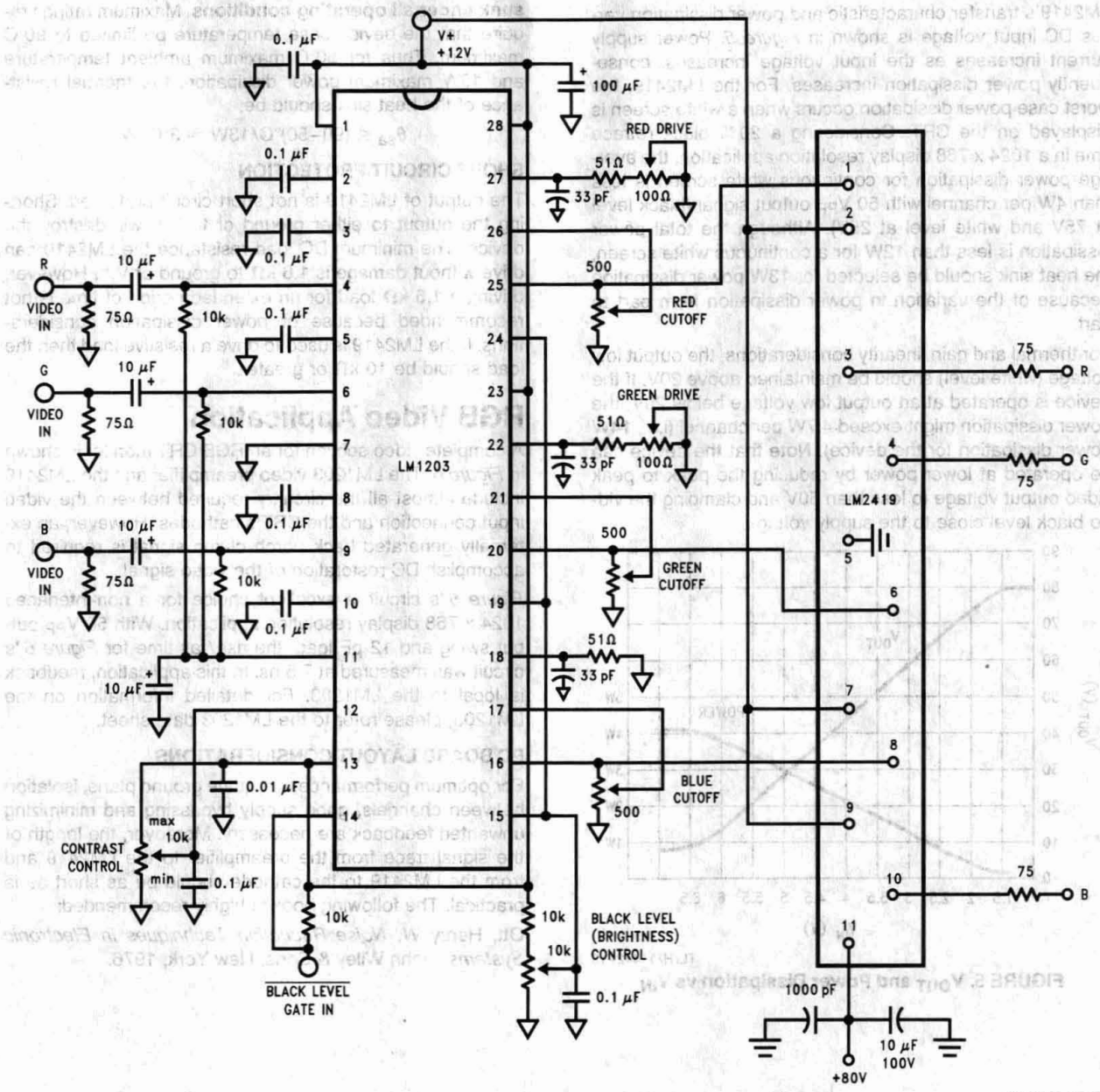

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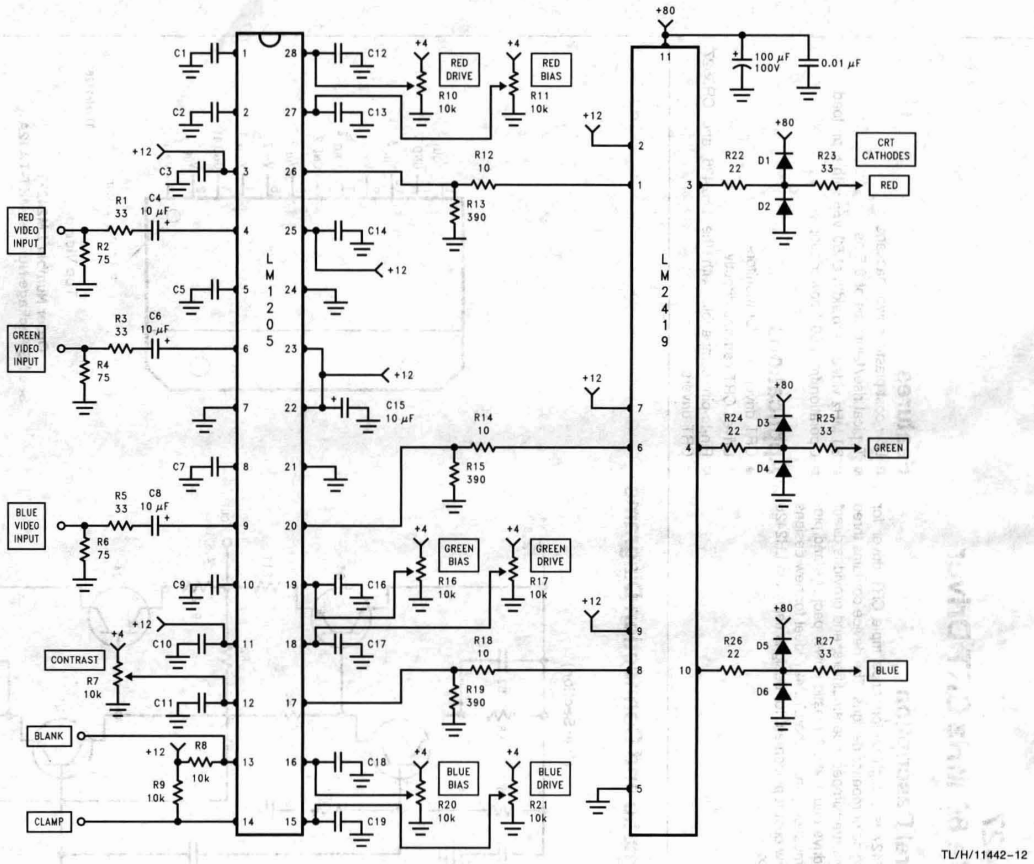
FIGURE 6. Typical VGA/SVGA Application



Diodes FDH400

Unmarked capacitors 0.1 µF

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FIGURE 7. Typical SVGA/XGA Application

National Semiconductor

LM2427
Triple 80 MHz CRT Driver

General Description

The LM2427 is a high performance triple CRT driver for simplifying color monitor designs. The device contains three large signal transimpedance amplifiers, and provides direct cathode drive capability. A plastic power package and pin-to-pin compatibility make the LM2427 ideal for new designs or as a low cost replacement for designs using the LH2426 or CR5527.

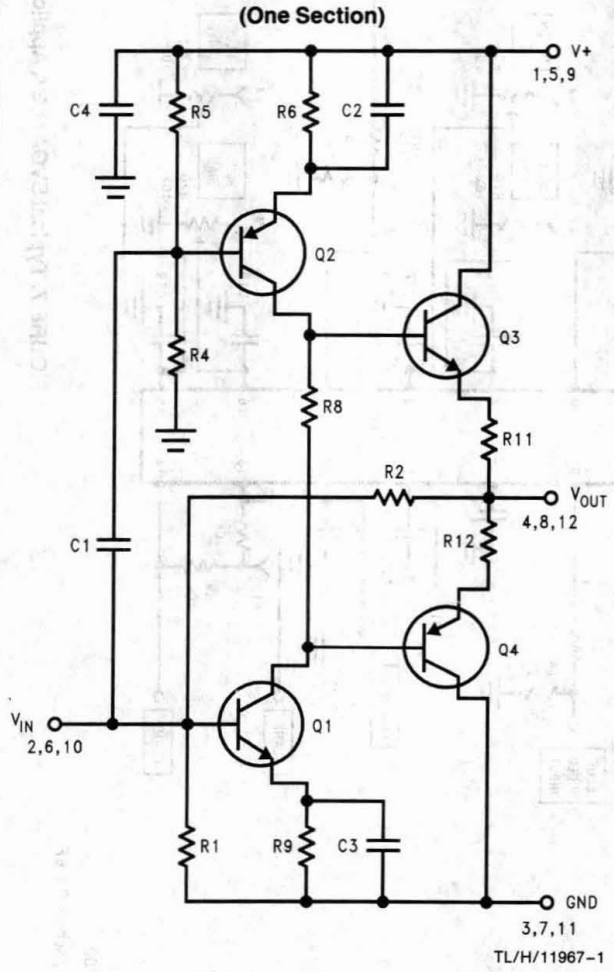
Features

- Low-cost plastic power package
- Typical rise/fall times of 3.5 ns
- 80 MHz video bandwidth at 50 V_{PP} with 8 pF load
- Operation from 80V power supply

Applications

- CRT driver for color monitors
- Drives CRT cathode directly
- Pin-to-pin compatible with the LH2426 and CR5527 CRT drivers

Schematic and Connection Diagrams



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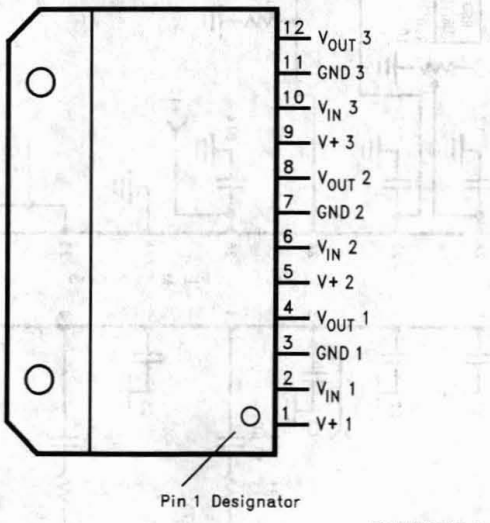

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Top View

Order Number LM2427T
See NS Package Number MKT-TA12A

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage, V+	+85V
Safe Operating Power Consumption	14W
Storage Temperature Range, T_{STG}	−25°C to +100°C
Operating Temperature Range, T_{CASE}	−20°C to +90°C
Lead Temperature (Soldering, 10 sec.)	300°C
ESD Tolerance	TBD

Electrical Characteristics

V+ = 80V, R_G = 430Ω, C1 = 47 pF, C_L = 8 pF, 50 V_{PP} output swing with 40V DC offset. See *Figure 1*. T_{CASE} = 25°C unless otherwise noted.

Symbol	Parameter	Conditions	LM2427			Units
			Min	Typical	Max	
I_{CC}	Supply Current (per Amplifier)	No Input or Output Load		24	30	mA
V_{INDC}	Input Offset Voltage		1.4	1.6	1.8	V
V_{OUTDC}	Output Offset Voltage		34	40	46	V
t_R	Rise Time	10% to 90% (Note 1)		3.5		ns
t_F	Fall Time	90% to 10% (Note 1)		3.5		ns
A_V	Voltage Gain		−11	−13	−14	V/V
LE	Linearity Error	V_{OUT} from +10V to +70V (Note 2)		5		%
ΔA_V	Gain Matching	(Note 3)		0.2		dB

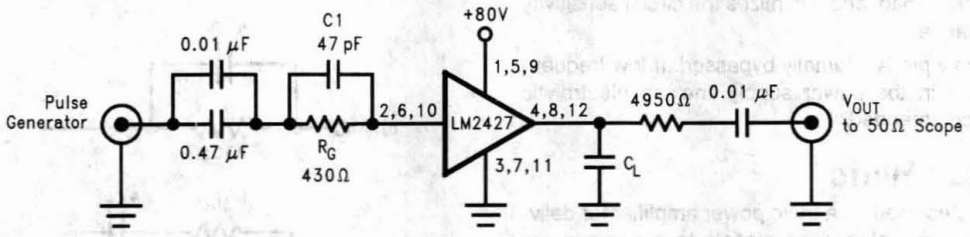
Note 1: Input signal: t_r, t_f < 1.5 ns, f_{in} = 1 MHz.

Note 2: Linearity error is defined as: The variation in small signal gain from +20V to +70V output with a 100 mVAC, 1 MHz, input signal.

Note 3: Calculated value from voltage gain test on each channel.

Typical Performance Characteristics

Typical Test Circuit (One Section)



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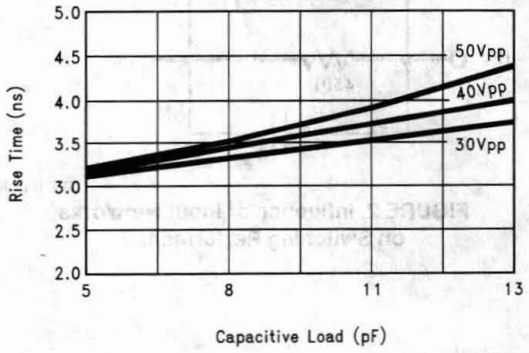
Note: C_L, total load capacitance, includes all parasitic capacitances.

FIGURE 1. Test Circuit (One Section)
This test circuit is used for both characteristic plots.

Typical Rise Time vs Capacitive Loading



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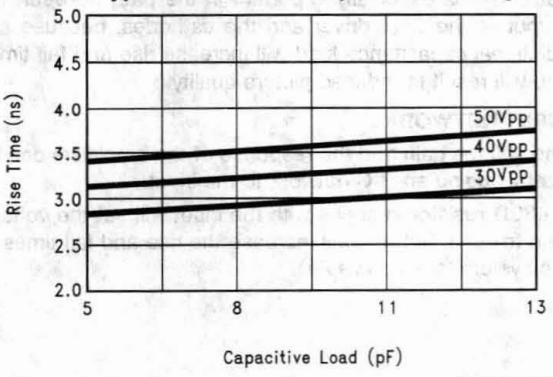
Typical Fall Time vs Capacitive Loading



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Test Circuit

Figure 1 shows a typical test circuit for evaluation of the LM2427. This circuit is designed to allow testing of the LM2427 in a 50Ω environment, such as a pulse generator, oscilloscope or network analyzer. The 4950Ω resistor in series with the output of the LM2427 forms a 100:1 voltage divider when connected to a 50Ω-input oscilloscope or network analyzer. To calibrate pulse generator, set to 2.4 V_{PP} into 50Ω.

THEORY OF OPERATION

The LM2427 is a triple channel transimpedance amplifier for CRT's, suitable for SVGA, XGA, IBM and Macintosh display resolution monitors. The LM2427 is pin-to-pin compatible with the LH2426 and CR5527 CRT drivers. The device is packaged in the industry standard 12-lead SIP TO-220 molded plastic power package. The heat sink is electrically isolated and may be grounded for ease of manufacturing and RFI/EMI shielding.

Applying an input current to the LM2427 will result in an output voltage. An input current of about ±4.5 mA will provide a full output swing of ±25V. A resistor in series with the input converts the device into a voltage amplifier; with a resistor value of 430Ω the voltage gain becomes −13.

The LM2427 is a two stage amplifier configured in a push-pull configuration (see schematic on front page). Q2 is biased by resistors R4 and R5, Q1 gets its bias through a 5700Ω feedback resistor and the input biasing current. The bases of Q1 and Q2 are capacitively coupled and, therefore, Q2 will be actively driven.

The emitter resistors of Q1 and Q2 are bypassed with small capacitors. This increases the gain of the stage for high frequencies and increases the bandwidth of the amplifier.

Emitter followers Q3 and Q4 isolate the input stage from the output capacitance load, and minimizes the circuit sensitivity to load capacitance.

The power supply pin is internally bypassed. If low frequencies are present in the power supply line, an electrolytic capacitor is recommended.

Application Hints

The LM2427 is designed as a triple power amplifier for delivering red, green, and blue video signals to a cathode ray tube (CRT). It can provide a 50V output swing and energize a 12 ns pixel at a CRT cathode with 8 pF of capacitance.

As with any CRT driver, when designing a video amplifier board with the LM2427, careful attention should be paid at reducing stray capacitance along the entire video signal path. This is especially important in the path between the output of the CRT driver and the cathodes, because any additional capacitance load will increase rise and fall times and will result in reduced picture quality.

INPUT NETWORKS

The voltage gain and the response of the amplifiers can be set by adding an R-C network to the input.

A 430Ω resistor in series with the input will set the voltage gain to −13, but this will increase the rise and fall times of the system (see *Figure 2a*).

Bypassing the resistor with a capacitor of about 47 pF will restore the rise and fall times but will result in some overshoot. *(Figure 2b)*

Adding a resistor in series with the 47 pF capacitor will reduce the overshoot but also increases the rise and fall times. *(Figure 2c)*

The addition of a second capacitor offers a compromise between the above networks by improving the rise and fall times at the expense of some overshoot. *(Figure 2d)*

Suggested values for the resistors and capacitors are shown, however, optimum values may differ depending upon the stray inductances and capacitances present in different board layouts.

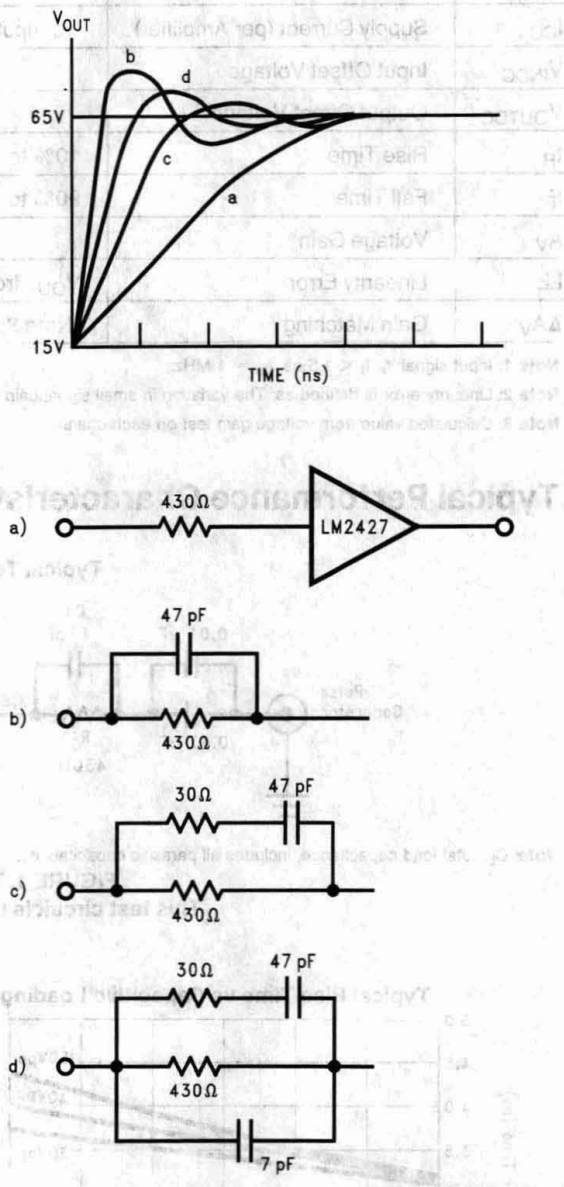

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FIGURE 2. Influence of Input Networks on Switching Performance

Application Hints (Continued)

TILT AND OVERSHOOT COMPENSATION

When a low frequency square is displayed on a monitor screen, some tilt may appear on the video signal due to the large power and thermal dissipation changes in the input transistors. This problem is illustrated in *Figure 3.*

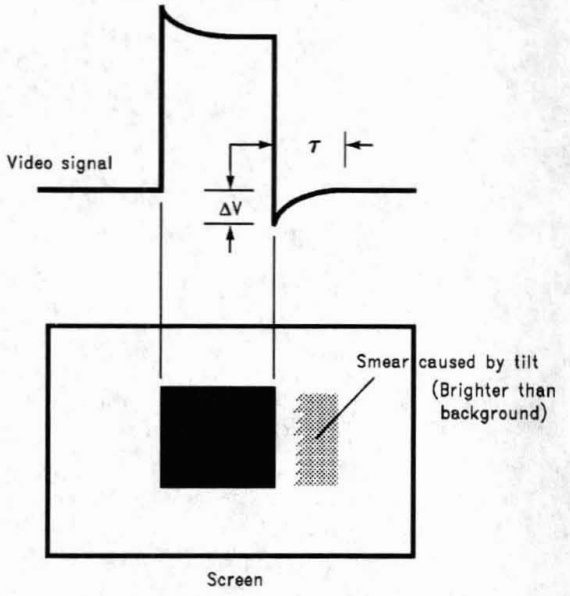

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FIGURE 3. Tilt on a Low Frequency Signal and Its Effects

The tilt can be compensated by adding an external RC feedback network as shown in *Figure 4.* The RC feedback helps by reducing the gain of the amplifier during the edge transition for a duration corresponding to τ. The values of R and C should be selected so that the gain is reduced ($\Delta V = 0$) for the duration of the tilt (τ).

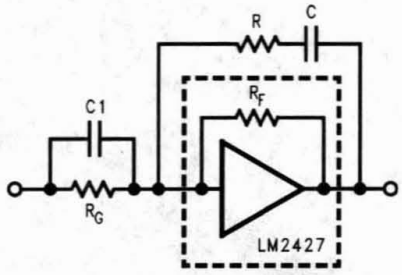

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FIGURE 4. RC Feedback Network for Tilt Compensation

To find the value of resistor R, the following formula can be used:

$$R = \frac{(100 - x\%)}{x\%} R_F$$

where x% is the percentage value of ΔV to the peak-to-peak output swing (V_{PP}). R_F is internally fixed to 5700Ω. The value of capacitor C is determined by:

$$C = \tau / R$$

where τ is the duration of the tilt.

For optimum results in a specific application, the values for R and C may need to be tested and adjusted in the given application board.

PROTECTING AMPLIFIER OUTPUT FROM TUBE ARCING

During normal CRT operation, internal arcing may occasionally occur. Spark gap protectors will limit the maximum voltage, but to a value that is much higher than allowable on the LM2427. This fast, high voltage, high energy pulse can damage the LM2427 output stage. The addition of two current limiting resistors of 50Ω to 100Ω total, and clamping diodes D1 and D2, will provide protection but will slow down the response. The diodes should have a fast transient response, high peak current rating, low series impedance and low shunt capacitance. FDH400 or equivalent diodes are recommended. Adding a series peaking inductor of 100 nH to 150 nH will restore the bandwidth and provide additional protection. (See *Figure 5*)

The value of the inductor can be calculated from:

$$Lp = \frac{(R_O + R_1 + R_2)^2}{2.4} C_L$$

where C_L is the total load and R_O is the intrinsic high frequency output resistance of the amplifier, generally 160Ω.

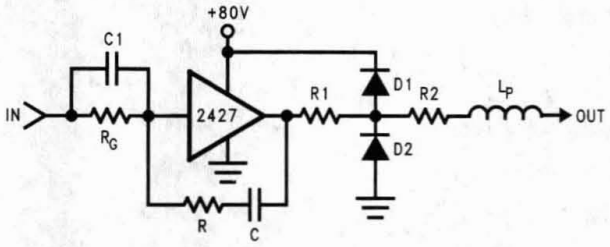

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FIGURE 5. One Section of the LM2427 with Tilt Compensation, Arc Protection and Peaking Inductance L_P in the Output

SHORT CIRCUIT PROTECTION WARNING!

To provide maximum output speed, the LM2427 does not have short circuit protection. Shorting the output can destroy the device.

SUPPLY BYPASSING

Although the LM2427 has internal supply bypassing, some values of supply line inductance can cause ringing in the supply lines. If this occurs, an additional bypass capacitor or a low-pass filter should be placed as close as possible to the supply (V+) pins of the LM2427.

CAPACITIVE LOADS

The LM2427 is designed to drive capacitive loads, however, the very high output slew rate of about 13,700 V/μs can result in charging currents of over 200 mA into a 20 pF load. These very high currents can damage the output transistors.

HEAT SINKING

Power consumption by the LM2427 will depend on the supply voltage used, the output loading, the peak-to-peak output swing and the operating frequency. Since the LM2427 will dissipate up to 14W, an external heatsink is always required. The maximum allowed case temperature is 90°C. To calculate maximum heatsink thermal resistance, use the following formula:

$$R_{th} = \frac{(90°C - \text{Max Ambient})}{14}.$$

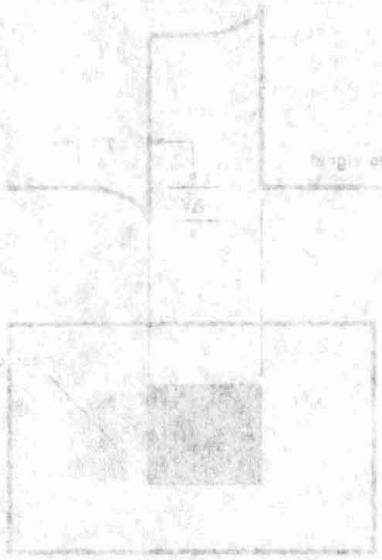
PC BOARD LAYOUT CONSIDERATIONS

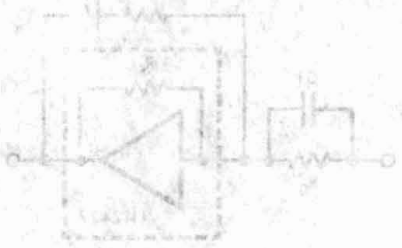
Input pins 2, 6 and 10 are amplifier summing junctions. All connections to these points should be as short as possible and should be separated from other signals. The components connected to these pins should be located close to the LM2427, and the total conductor length connected to these points should be no more than one inch.

For optimum performance, an adequate ground plane, isolation between channels, good supply bypassing and minimizing unwanted feedback are necessary. Also, the length of the signal traces from the preamplifier to the LM2427 and from the LM2427 to the CRT cathode should be as short as possible. The following references are recommended:

Ott, Henry W., *"Noise Reduction Techniques in Electronic Systems"*, John Wiley & Sons, New York, 1976.

"Guide to CRT Video Design", National Semiconductor Application Note 861.





National Semiconductor

PRELIMINARY

LM1291
Video PLL System for Continuous Sync Monitors

General Description

The LM1291 is an integrated horizontal time base solution specifically designed to operate in continuous sync video monitors. It accepts all presently defined computer sync signals and generates the drive signal for a horizontal (line) output stage. The system automatically selects the active input based on the following (highest to lowest) priority: (1) separate H and V sync, (2) HV (composite) sync, and (3) composite video. Polarity-corrected H/HV and V sync outputs are provided, along with logic flags which show the respective input polarities.

The IC contains an FVC (frequency-to-voltage convertor) which sets the free-running frequency of the VCO (voltage-controlled oscillator). This technique allows operation over the entire frequency range, 30 kHz–125 kHz, using just one optimized set of external components.

A second phase detector is included which compensates for storage time variation in the horizontal output transistor; the picture's horizontal position is thus independent of temperature and component variance.

The LM1291 provides DC control pins for H Drive duty cycle and H Drive phase.

Features

- VCO precision trimmed on chip—no trimming or loop tuning required
- No costly high-precision components needed
- Low phase jitter (1.3 ns at 100 kHz)
- DC controlled H phase and duty cycle
- Frequency agile—30 kHz to 125 kHz with no external adjustment
- Video mute signal indicates changes in H input frequency
- Input signal prioritization
- Clamp pulse position and width control
- Clamp pulse continues in absence of H sync
- Resistor-programmable minimum and maximum VCO frequency
- X-ray shutdown input
- Under-voltage lockout for $V_{CC} < 9.5V$
- Horizontal output transistor forced off during flyback pulse

Applications

- Horizontal and vertical sync processor for continuous sync monitors
- Wide frequency range phase-locked loop

Connection Diagram

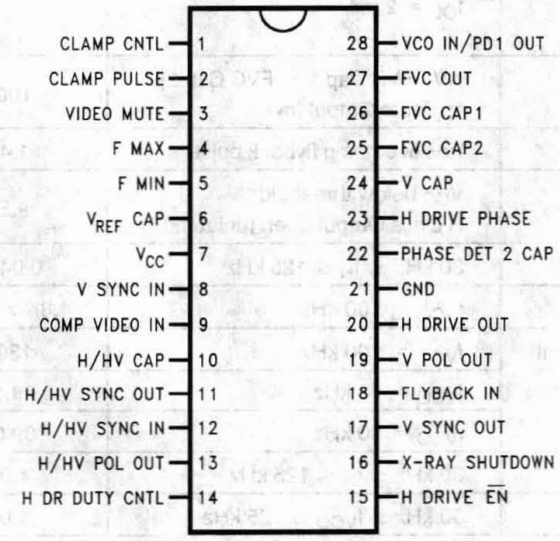


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FIGURE 1

Order Number LM1291N
See NS Package Number N28B

Absolute Maximum Ratings (Notes 1 & 3)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	14V
Input Voltage, V_{DC}	
Pins 15, 23	5V
Pins 4, 5	8V
Pins 8, 28	10V
Pins 1, 9, 12, 14, 16, 18	V_{CC}
Power Dissipation (P_D) (Above 25°C Derate Based on θ_{JA} and T_J)	2.5W
Thermal Resistance (θ_{JA})	50°C/W
Junction Temperature (T_J)	150°C
ESD Susceptibility (Note 5)	2 kV
Storage Temperature	−65°C to +150°C
Lead Temperature (Soldering, 10 sec.)	265°C

Operating Ratings (Note 2)

Operating Temperature Range	−20°C to +80°C
Supply Voltage (V_{CC})	$10.8V \le V_{CC} \le 13.2V$

Electrical Characteristics See Test Circuit *(Figure 2)*; $T_A = 25°C$; $V_{CC} = 12V$

Parameter	Conditions	Typical (Note 6)	Limit (Note 7)	Units
Supply Current		30	40	mA (max)
Jitter	H Sync frequency = 100 kHz (Note 8)	1.3		ns p-p
Minimum composite video input voltage	Pin 9, cap coupled (0.01 μF), sync tip to black level		0.14	V_{PP} (min)
DC clamp level, composite video input		2.0		V_{DC}
Clamp charging current, composite video input		1		mA
H/HV sync input amplitude	Cap coupled, 10% duty cycle		1.0	V_{PP} (min)
V sync input amplitude	Cap coupled, 1% duty cycle		1.0	V_{PP} (min)
High level output voltage V_{OH}, (Pins 2, 11, 13, 17, 19)	$I_{OH} = -100\ \mu A$	4.3	4.0	V_{DC} (min)
Low level output voltage V_{OL}, (Pins 2, 11, 13, 17, 19)	$I_{OL} = 1.6$ mA	0.25	0.4	V_{DC} (max)
Video Mute low level output voltage	$I_{OL} = 2$ mA		0.4	V_{DC} (max)
Mute detection voltage threshold	ΔV, |FVC Cap 1 − FVC Cap 2| for Mute Output low	100		mV
Flyback input threshold	Positive-going flyback pulse	1.4		V
Under-voltage lockout	V_{CC} below threshold: H Drive Output open (unlatched)	9.5		V
Frequency to voltage gain	$30\ kHZ \le f_H \le 125$ kHz	0.047		V/kHz
VCO gain constant	$f_{VCO} = 100$ kHz	1.34×10^5		Rad/s/V
PD1 Phase Detector gain constant	$f_{VCO} = 100$ kHz	130		μA/Radian
	$f_{VCO} = 60$ kHz	78.1		
	$f_{VCO} = 30$ kHz	39.0		
Frequency to voltage linearity	$30\ kHz \le f_H \le 125$ kHz	1.0		%
VCO linearity	$30\ kHz \le f_{VCO} \le 125$ kHz	1.0		%

Electrical Characteristics See Test Circuit *(Figure 2)*; T_A = 25°C; V_{CC} = 12V (Continued)

Parameter	Conditions	Typical (Note 6)	Limit (Note 7)	Units
H Drive duty cycle control gain	DC input 0V–4V; 30%–70% allowed	0.1		T_H/V
H Drive Phase control gain	(Note 9)	47		°/V
PD1 Phase detector leakage current + VCO input bias current			1	μA (max)
H Drive low level output voltage	I_{OL} = 100 mA		0.8	V (max)
H Drive $\overline{EN}$ low level input voltage	H Drive output active		0.8	V (max)
H Drive $\overline{EN}$ high level input voltage	H Drive output open (unlatched)		2.0	V (min)
X-ray Shutdown threshold voltage	Above threshold H Drive Output Open (Latched)	1.72	1.65 1.8	V (min) V(max)
H/HV Sync out propagation delay change	H/HV in vs. Comp Video in	32		ns
Clamp Pulse width	(back porch) R_{SET} = 15k; V_{SET} = 0V	0.4		μs
	(back porch) R_{SET} = 15k; V_{SET} = 1.5V	1.4		μs
	(sync tip) R_{SET} = 15k; V_{SET} = 4V	0.6		μs
Clamp Pulse Delay	(back porch) Trailing edge H/HV Sync In to leading edge clamp pulse	0.1		μs
	(sync tip) Leading edge H/HV Sync In to leading edge clamp pulse	0.025 T_H		s
Internal Ref voltage at pin 6	No load	8.2		V

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur.

Note 2: Operating Ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.

Note 3: All voltages are measured with respect to GND, unless otherwise specified.

Note 4: The maximum power dissipation must be derated at elevated temperatures and is dictated by T_{Jmax}, θ_{JA} and the ambient temperature, T_A. The maximum allowable power dissipation at any elevated temperature is $P_D = (T_{Jmax} - T_A)/\theta_{JA}$ or the number given in the Absolute Maximum Ratings, whichever is lower. For this device, T_{Jmax} = 150°C. The typical thermal resistance (θ_{JA}) of these parts when board mounted follow: LM1291N 50°C/W.

Note 5: Human Body model, 100 pF capacitor discharged through a 1.5 kΩ resistor.

Note 6: Typicals are at $T_A = T_J$ = 25°C and represent most likely parametric norm.

Note 7: Tested limits are guaranteed to National's AOQL (Average Outgoing Quality Level).

Note 8: Measured with hp 53310A Modulation Domain Analyzer, 50 ms sample window.

Note 9: Phase limits: $+\left(0.35 - \frac{t_{DFB}}{T_H}\right), -0.15$, expressed as a fraction of the horizontal period T_H, where t_{DFB} is the horizontal output transistor turn-off delay from the rising edge of H Drive to the FBP peak. A positive phase value represents a phase lead of the FBP peak with reference to the leading edge of H sync.

Test Circuit

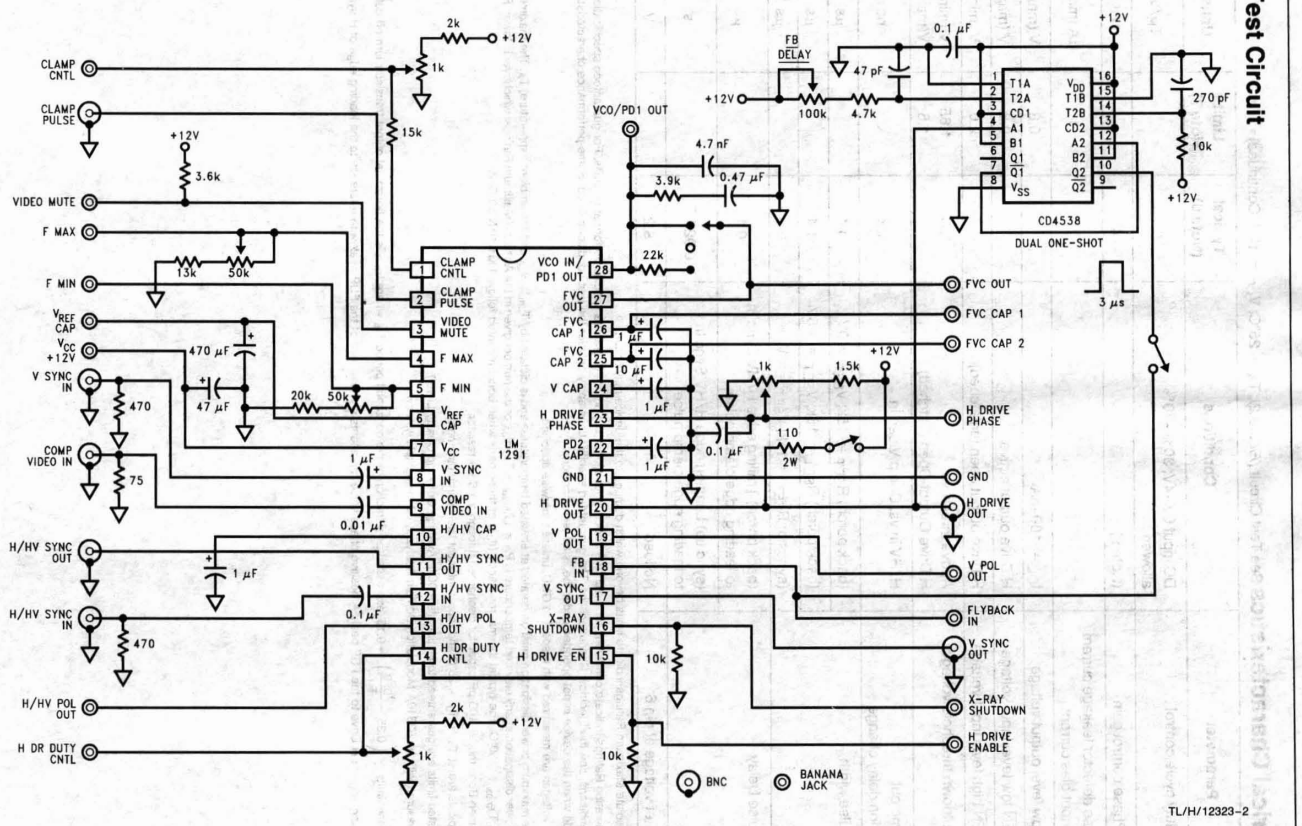

FIGURE 2

Block Diagram

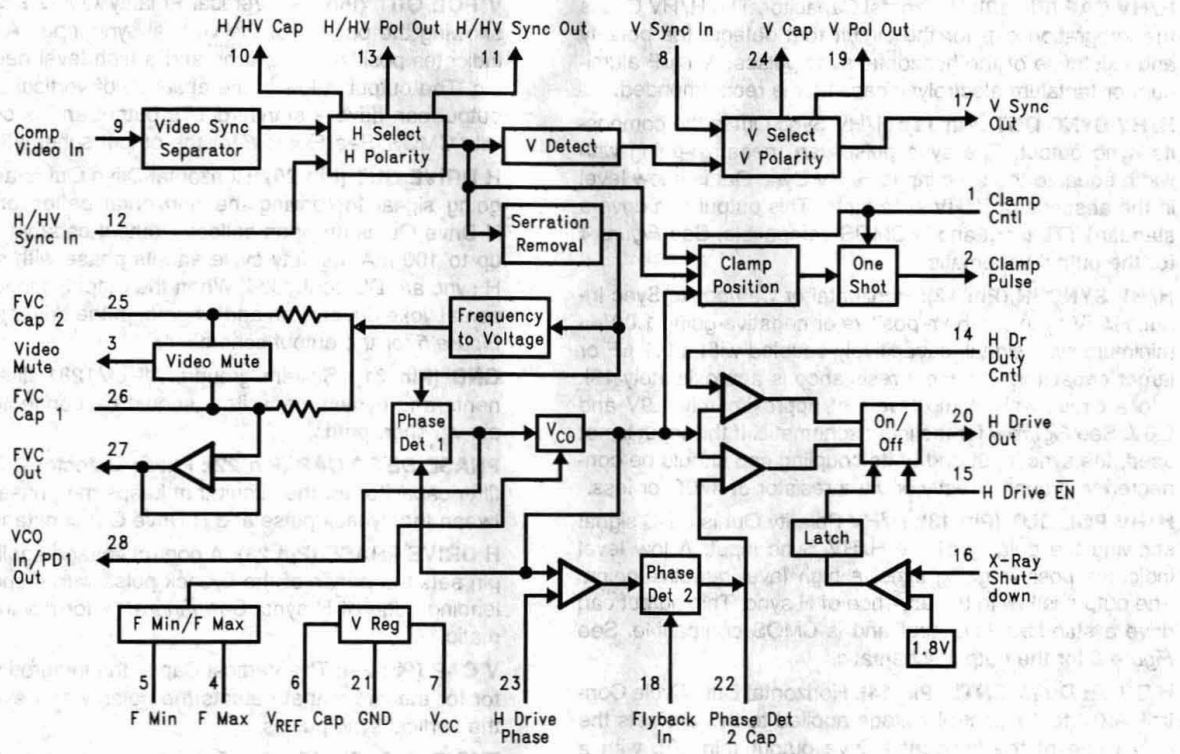

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FIGURE 3

Pin Descriptions

See *Figures 4* through *19* for input and output schematics.

CLAMP CNTL (Pin 1): Clamp Control. See CLAMP PULSE (Pin 2) description. A control voltage of 0V to 4V applied to this pin through a 15k resistor sets the position and width of the negative-going clamp pulse. A voltage below 2V positions the pulse on the back porch of the horizontal sync pulse and decreasing voltage narrows the pulse. A voltage above 2V sets the pulse within the H sync pulse (slightly delayed from the leading edge) and increasing voltage narrows the pulse. At the boundary of the switchover between the two modes, there is a narrow region of uncertainty resulting in oscillation, which should be no problem in most applications. If there is no H Sync and this pin is high, a clamp pulse will be generated from the VCO. This feature is useful with On Screen Displays which must display a message in the absence of sync inputs.

Note: The VCO frequency goes to F MIN in the absence of H sync.

CLAMP PULSE (Pin 2): This output provides a negative-going pulse for DC restoration or clamping in video systems. The pulse can be positioned coincident with the H sync pulse or on the back porch. The pulse width can be adjusted with the clamp control voltage.

VIDEO MUTE (Pin 3): This "open collector" output goes low if there is a sudden change in H sync frequency. It can be used to blank video or for other chores. The rate and amount of frequency change causing Video Mute is set by the values of the capacitors at FVC 1 (Pin 26) and FVC 2 (Pin 25). Video Mute is high in the absence of H sync. See *Figure 5* for the output schematic.

F MAX (Pin 4): Maximum VCO Frequency. A resistor to ground sets the upper limit of the VCO in case of too high H sync frequency. F MAX is approximately $1.8 \times 10^9/(R_{MAX} + 500\Omega)$.

F MIN (Pin 5): Minimum VCO Frequency. A resistor to ground sets the lower limit of the VCO. This is the frequency that the VCO goes to in the absence of H sync. F MIN is approximately 7.5 kHz + $5.6 \times 10^8/(R_{MIN} + 500\Omega)$.

V_{REF} CAP (Pin 6): This is the output of the internal bandgap based 8.2V reference, which needs bypassing for low noise. The bypass cap should be connected via a short path to pin 21 (ground). The path should not be connected to any part of the circuit that has noise currents. The capacitor should be a minimum of 470 μF aluminum or tantalum electrolytic capacitor.

V_{CC} (Pin 7): V_{CC} (12V nominal) should be bypassed to ground (Pin 21) via a short path with a minimum of 47 μF aluminum or tantalum electrolytic capacitor.

V SYNC IN (Pin 8): Vertical Sync Input. V sync can be a positive or negative going 1.0 V_{PP} minimum signal, capacitively coupled with a 1 μF or larger capacitor. The input resistance is approximately 50k and is biased at 5.2V. V SYNC IN has priority over composite sync and composite video. See *Figure 6* for the input schematic.

COMP VIDEO IN (Pin 9): Composite Video Input. This is the sync input used for composite video; i.e., sync on green, and is the default input when no signals are present at V SYNC IN and H/HV IN. The signal must have negative going sync tips which are at least 0.14V below black level. See *Figure 7* for the input schematic.

Pin Descriptions (Continued)

H/HV CAP (Pin 10): Horizontal Capacitor. The H/HV Cap is the integration cap for the circuit that detects the polarity and existence of the horizontal sync pulses. A 1 μF aluminum or tantalum electrolytic capacitor is recommended.

H/HV SYNC OUT (Pin 11): H/HV Sync Out is the composite sync output. The sync pulses are negative-going with width equal to the sync input. H/HV Sync Out is a low level in the absence of H/HV sync input. This output can drive a standard TTL input and is CMOS compatible. See *Figure 4* for the output schematic.

H/HV SYNC IN (Pin 12): Horizontal or Composite Sync Input. H/HV sync can be a positive or negative-going 1.0 V_{PP} minimum sync signal, capacitively coupled with a 0.1 μF or larger capacitor. The input resistance is approximately 18k into a circuit with clamp levels of approximately 1.9V and 2.6V. See *Figure 8* for the input schematic. If this input is not used, the sync input end of its coupling cap should be connected to ground directly or via a resistor of 470Ω or less.

H/HV POL OUT (Pin 13): H/HV Polarity Out is a DC signal showing the polarity of the H/HV Sync input. A low level indicates positive-going sync, a high level negative-going. The output is low in the absence of H sync. This output can drive a standard TTL input and is CMOS compatible. See *Figure 9* for the output schematic.

H DRIVE DUTY CNTL (Pin 14): Horizontal Duty Cycle Control. A 0V to 4V control voltage applied to this pin sets the duty cycle of the horizontal drive output (pin 20), with a range of approximately 30% to 70%. 2V sets the duty cycle to 50%. See *Figure 10* for the input schematic.

H DRIVE $\overline{EN}$ (Pin 15): Horizontal Drive Enable. This pin turns the Horizontal Drive Output on and off with a TTL level signal, with low on and high off. See *Figure 11* for the input schematic.

X-RAY SHUTDOWN (Pin 16): This pin turns off the Horizontal Drive Output if its voltage equals or exceeds an internal reference of approximately 1.7V. The output is latched high, and V_{CC} has to be reduced to below approximately 2V to clear the latched condition; i.e., power must be turned off. This feature provides "X-Ray protection" by checking CRT anode voltage level through a resistive divider from a power supply voltage that is proportional to the CRT voltage. See *Figure 12* for the input schematic.

V SYNC OUT (Pin 17): Vertical Sync Out is a negative going pulse occurring approximately 0.3 horizontal lines after the beginning of the vertical interval. V Sync Out is a low level in the absence of vertical sync. V Sync Out width is the same as V Sync In, and is 3 to 5 lines longer for H/HV Sync In and Comp Video In. This output can drive a standard TTL input and is compatible with CMOS. See *Figure 4* for the output schematic.

FLYBACK IN (Pin 18): This is a positive-going pulse from the horizontal deflection circuit that is compared to the VCO phase in phase detector 2, whose output is used to control the phase of Horizontal Drive Out. This compensates for time delay changes in the horizontal deflection circuitry with temperature, etc. to keep the display position constant. See *Figure 13* for the input schematic.

V POL OUT (Pin 19): Vertical Polarity Out is a DC signal showing the polarity of the vertical sync input. A low level indicates positive-going sync and a high level negative-going. The output is low in the absence of vertical sync. This output can drive a standard TTL output and is compatible with CMOS. See *Figure 9* for the output schematic.

H DRIVE OUT (Pin 20): Horizontal Drive Out is a negative-going signal for driving the horizontal deflection system. H Drive Out is an open collector output capable of sinking up to 100 mA. Its duty cycle and its phase with respect to H sync are DC controlled. When the output is low, the horizontal yoke driver is on and when high the driver is off. See *Figure 5* for the output schematic.

GND (Pin 21): System ground. All LM1291 filter components and bypass capacitors should be connected to this pin via short paths.

PHASE DET 2 CAP (Pin 22): Phase Detector 2 Cap is the filter capacitor for the circuit that keeps the phase error between the flyback pulse and H Drive Out constant.

H DRIVE PHASE (Pin 23): A control voltage applied to this pin sets the phase of the flyback pulse with respect to the leading edge of H sync. See *Figure 14* for the input schematic.

V CAP (Pin 24): The Vertical Cap is the integration capacitor for the circuit that detects the polarity and existence of the vertical sync pulses.

FVC CAP 2 (Pin 25): The Frequency to Voltage Converter Capacitor 2 is the filter capacitor for the longer time constant filter for the Video Mute comparator.

FVC CAP 1 (Pin 26): The Frequency to Voltage Converter Capacitor 1 is the filter capacitor for the Frequency to Voltage Converter and is also the shorter time constant filter for the Video Mute comparator.

FVC OUT (Pin 27): The Frequency to Voltage Converter Output is a DC voltage proportional to frequency and is used to set the free-running frequency of the Voltage Controlled Oscillator. This signal goes to the VCO input via a resistor which is part of the PLL filter. The voltage range is approximately 0.6V to 6.0V for 15 kHz to 125 kHz. See *Figure 15* for the output schematic.

VCO IN/PD1 OUT (Pin 28): The Voltage Controlled Oscillator input and Phase Detector 1 output are connected internally at this pin. The phase locked loop filter components are connected here. See Circuit Description for information about this pin.

Input/Output Schematics

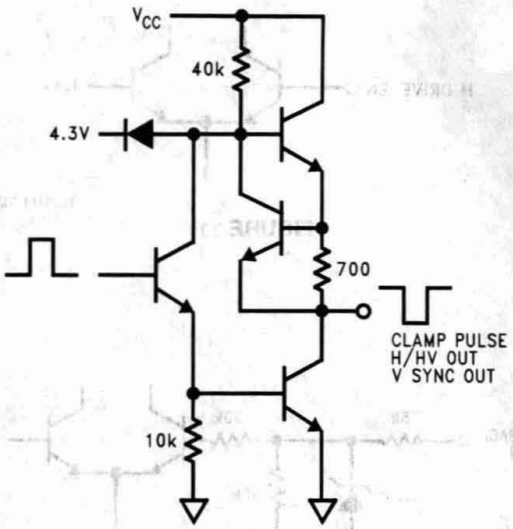

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FIGURE 4

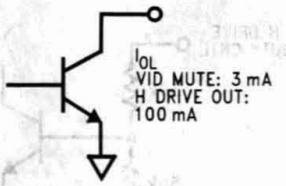

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FIGURE 5

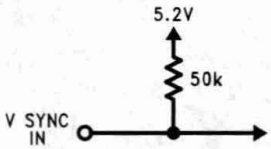

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FIGURE 6

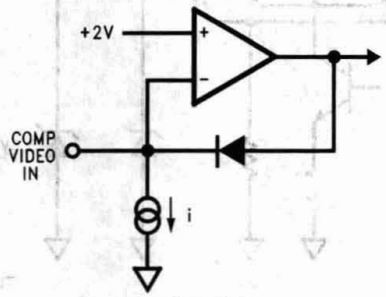

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FIGURE 7

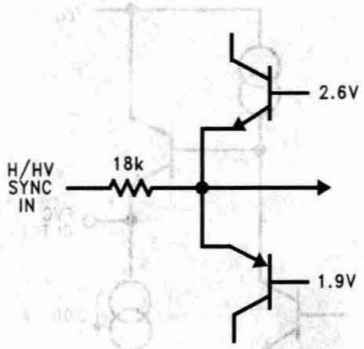

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FIGURE 8

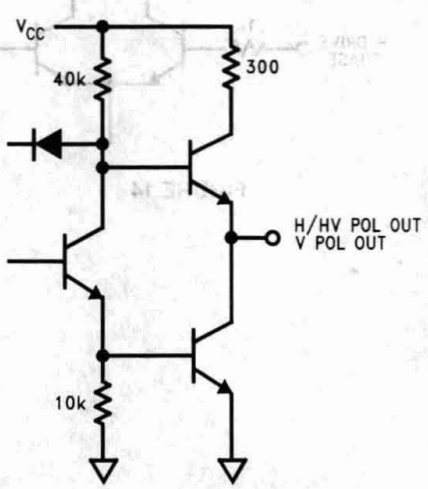

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FIGURE 9

Input/Output Schematics (Continued)

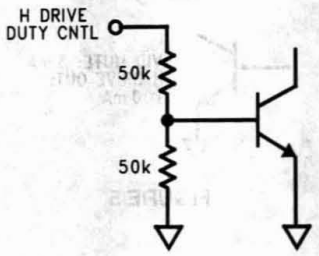

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FIGURE 10

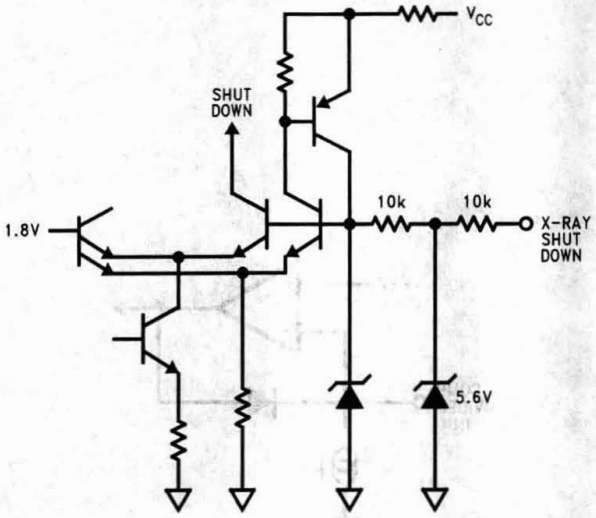

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FIGURE 12

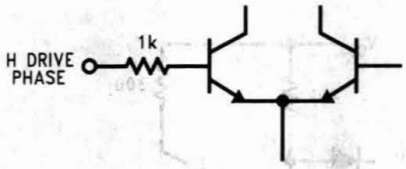

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FIGURE 14

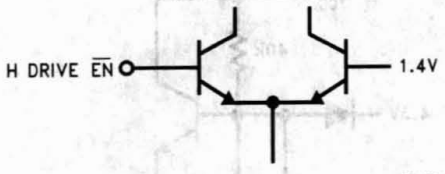

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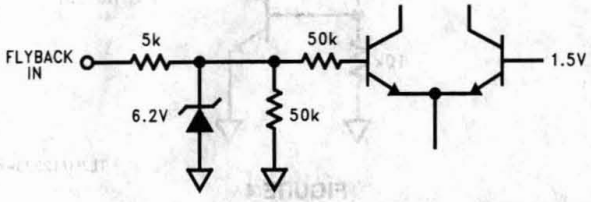
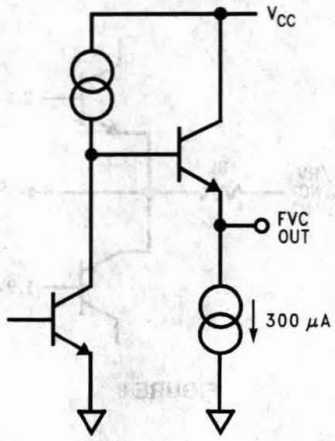
FIGURE 11



TL/H/12323–13

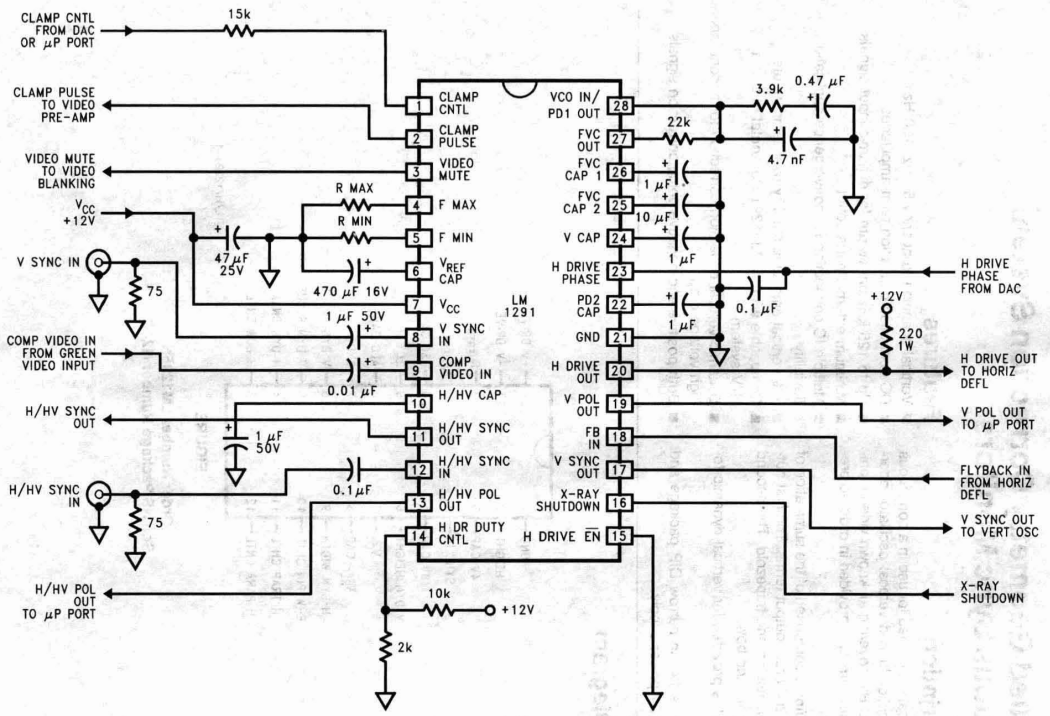
FIGURE 13



TL/H/12323–15

FIGURE 15

Typical Application



TL/H/12323–16

FIGURE 16

National Semiconductor

PRELIMINARY

LM1295
DC Controlled Geometry Correction System for Continuous Sync Monitors

General Description

The LM1295 is specifically designed for use in a continuous sync monitor. The injection-locked vertical oscillator operates from 50 Hz to 100 Hz, covering all known video monitors. A differential output current is provided in order to prevent ground interaction.

The IC provides two outputs composed of the summation of DC controlled 1st and 2nd order output terms. The first output corrects for EW pincushion and trapezoid. The second corrects for parallelogram and bow.

A DC controlled output is provided for vertical dynamic focus correction.

The IC is packaged in a 24-pin narrow DIP package and operates on a single 12V power supply.

Features

- Vertical scanning frequency 50 Hz–100 Hz
- DC controlled correction term amplitudes
- Up to 125 kHz bandwidth for dynamic input signals
- Minimum external parts count
- Multiple IC connection for convergence applications flexibility
- 1% vertical amplitude stability over temperature
- Compatible with the LM1291 Horizontal PLL in a H/V system
- Dynamic vertical deflection correction for second anode high voltage drop
- Both positive and negative going correction signals

Connection Diagram

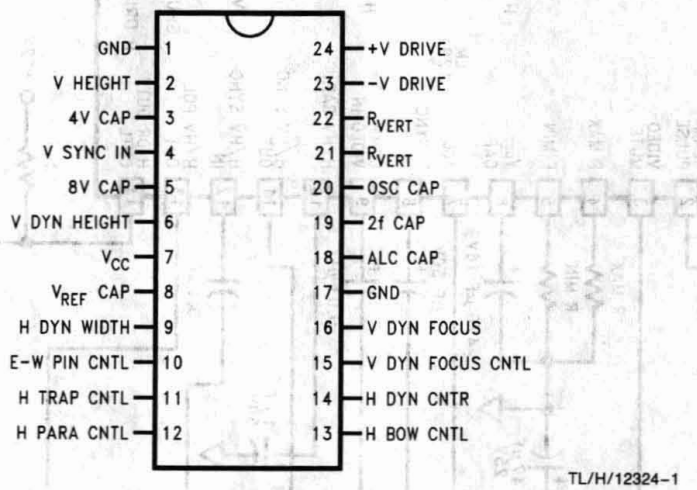


FIGURE 1

Order Number LM1295N
See NS Package Number N24C

Absolute Maximum Ratings (Notes 1 and 3)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	14V
Input Voltage (DC, pins 1, 2, 6, 10, 11, 12, 13, 15)	5V
Input Voltage (AC, Pin 4)	5 V_{PP}
Power Dissipation (Note 4) (Above 25°C Derate Based on θ_{JA} and T_J)	1.8W
Thermal Resistance (θ_{JA})	70°C/W
Junction Temperature (T_J)	150°C
ESD Susceptibility (Note 5)	1.8 kV
Storage Temperature	−65°C to +150°C
Lead Temperature (Soldering, 10 sec.)	265°C

Operating Ratings (Note 2)

Operating Temperature Range	−20°C to +80°C
Supply Voltage (V_{CC})	10.8V ≤ V_{CC} ≤ 13.2V
Input Voltage (DC, pins 2, 6, 10, 11, 12, 13, 15)	4V
Input Voltage (AC, pin 4)	4 V_{PP}

Electrical Characteristics See Test Circuit *(Figure 2)*; T_A = 25°C; V_{CC} = 12V.

Symbol	Parameter	Conditions	Typical (Note 6)	Limit (Note 7)	Units
I_{CC}	Supply Current	All Control Inputs = 3V	25	35	mA (max)
Vref	Internal ref voltage at pin 8		8.2		V
Rin	Input resistance	Pins 6, 10–13, 15	50	30	kΩ (min)
Ffr	Free-run frequency		45		Hz
F_{max}	Maximum frequency		100		Hz
Cntlbw	Control inputs bandwidth	Pins 6, 10–13, 15	125		kHz
Vhts	Vertical height temperature stability	V Height = 4V, V Dyn Height = 3V, T_A = 0°C to 70°C (Note 10)	1		%
Vdiff	Vertical differential output current	V Height = 4V, V Dyn Height = 4V, Pin 24 minus Pin 23		1	mA (min)
Vsynh Vsynl	V sync high input voltage V sync low input voltage			2.4 0.8	V (min) V (max)
Vcmrr	Vertical output CMRR	V_O = 1V to 4V, V Height = 2V, V Dyn Height = 3V	30		dB
Vpssr	Vertical output PSSR	V_{CC} = 10.8V to 13.2V, V Height = 2V, V Dyn Height = 3V	30		dB
Vop-p	Vertical peak output voltage	R_L = 10k	6	5	V_{PP} (min)
Vrerr	Vertical ramp distortion	(Note 8) V Height = 4V, V Dyn Height = 3V	1		%
Vsoerr	Vertical parabola distortion	(Note 9) V Height = 2.2V, V Dyn Height = 3V	8		%
CRfo	First order (ramp) correction, H Dyn Cntr (pin 14)	Pin 12 = 0V Pin 12 = 4V V Dyn Height = 3V, V Height = 4V, parabola nulled	2.50 2.25		V_{PP}
CRfo	First order (ramp) correction, H Dyn Width (pin 9)	Pin 11 = 0V Pin 11 = 4V V Dyn Height = 3V, V Height = 4V, parabola nulled	0.85 0.75		V_{PP}

Electrical Characteristics See Test Circuit *(Figure 2)*; T_A = 25°C; V_{CC} = 12V. (Continued)

Symbol	Parameter	Conditions	Typical (Note 6)	Limit (Note 7)	Units
CPso	Parabola correction range, H Dyn Cntr (pin 14), H Dyn Width (pin 9), V Dyn Focus (pin 16)	Pins 10, 13, 15 = 0V Pins 10, 13, 15 = 4V V Dyn Height = 3V, V Height = 4V, ramp nulled for H Dyn Cntr and H Dyn Width	1.2 1.0		V_{PP}
Vodc	Output DC bias	Pins 9, 14 and 16; all control inputs at 2.2V	4.0		V_{DC}
I_O	Output current	Pins 9, 14 and 16	5.0		mA

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur.

Note 2: Operating Ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.

Note 3: All voltages are measured with respect to GND, unless otherwise specified.

Note 4: The maximum power dissipation must be derated at elevated temperatures and is dictated by T_{Jmax}, θ_{JA} and the ambient temperature, T_A. The maximum allowable power dissipation at any temperature is $P_D = (T_{Jmax} - T_A)/\theta_{JA}$ or the number given in the Absolute Maximum Ratings, whichever is lower. For this device, T_{Jmax} = 150°C. The typical thermal resistance (θ_{JA}) of these parts when board mounted follow: LM1295N 70°C/W.

Note 5: Human body model, 100 pF capacitor discharged through a 1.5 kΩ resistor.

Note 6: Typicals are at $T_A = T_J$ = 25°C and represent most likely parametric norm.

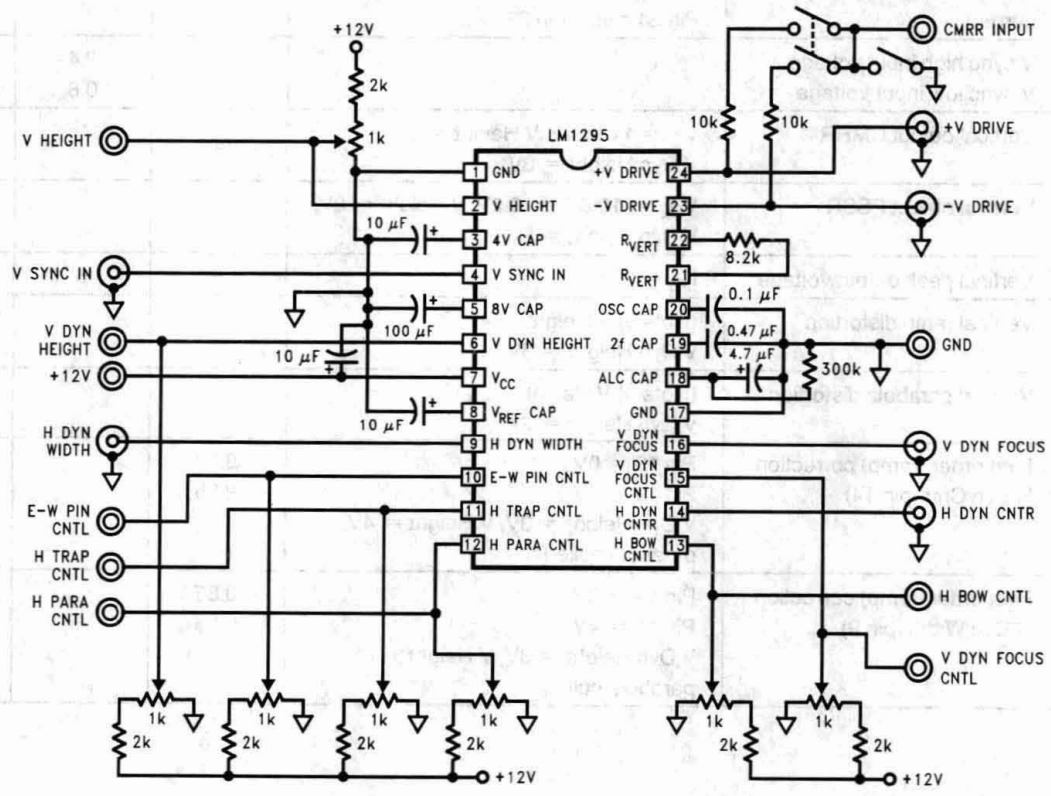
Note 7: Tested limits are guaranteed to National's AOQL (Average Outgoing Quality Level).

Note 8: The deviation from a straight line drawn through measured points at 5% and 95% of the ramp is used to calculate distortion.
Distortion = 100 (deviation, volts)/(95% value − 5% value, volts). Deviations are measured at ⅓ and ⅔ of the ramp time period.

Note 9: The deviation from a theoretical parabola drawn through the apex of the actual parabola is used to calculate distortion.
Distortion = 100 (deviation, volts)/(theoretical parabola, volts) at measuring point. Nine points are measured.

Note 10: The amplitude stability versus temperature is typically 1% or less when a standard 10k 5% ¼W carbon film resistor is connected between pins 21 and 22 and located close to the package. The negative temperature coefficient of the resistor corrects for the negative temperature coefficient of the LM1295. The typical amplitude stability of the LM1295 by itself is 2%.

Test Circuit



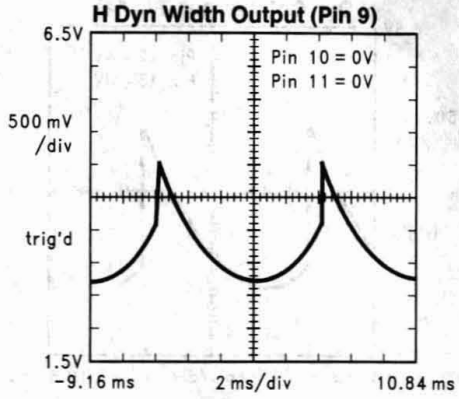
TL/H/12324–2

FIGURE 2

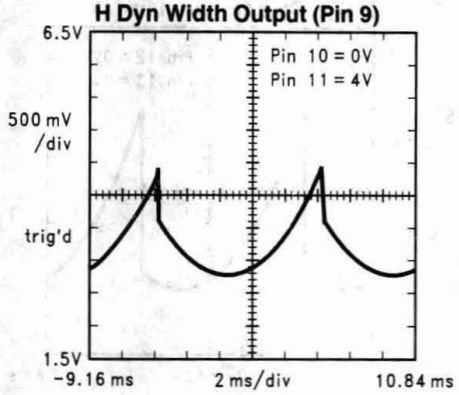
Typical Performance Characteristics

T_A = 25°C, F = 100 Hz, V_{Height} = 4V, $V_{Dyn\ Height}$ = 3V, Test Circuit—*Figure 2*

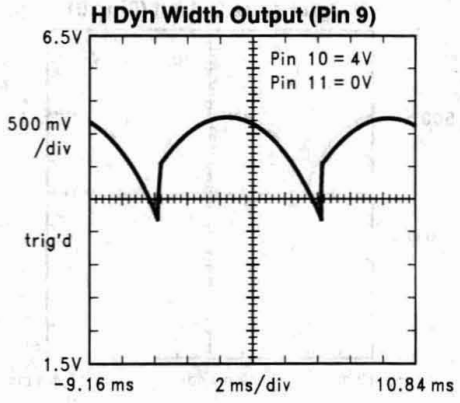
H Dyn Width Output (Pin 9)



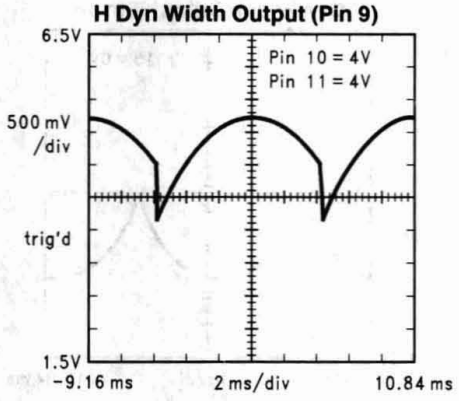
H Dyn Width Output (Pin 9)



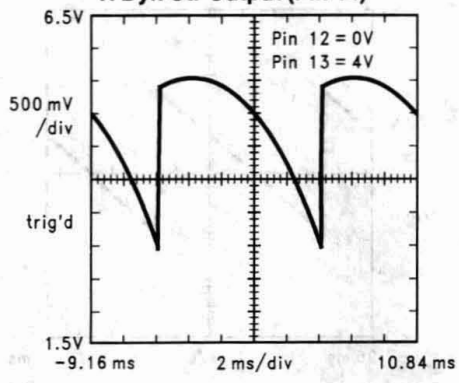
H Dyn Width Output (Pin 9)



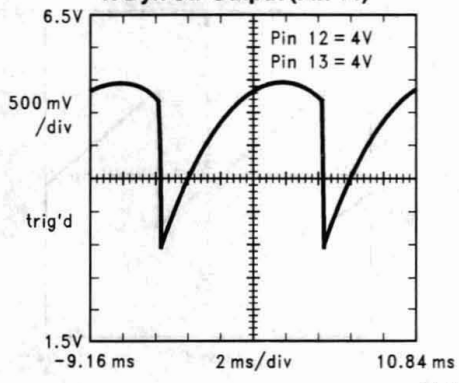
H Dyn Width Output (Pin 9)



H Dyn Ctr Output (Pin 14)



H Dyn Ctr Output (Pin 14)



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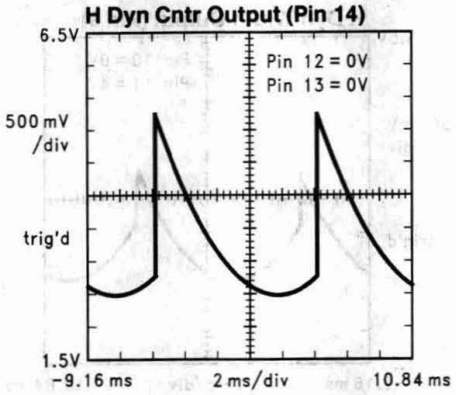
2

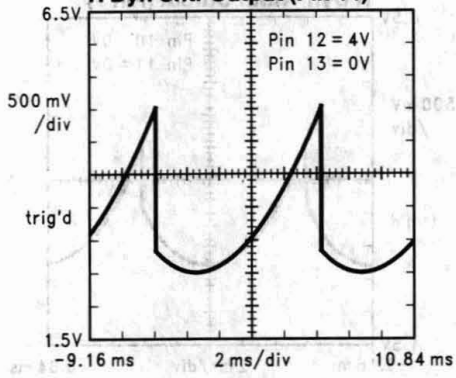
Typical Performance Characteristics (Continued)

T_A = 25°C, F = 100 Hz, V_{Height} = 4V, $V_{Dyn\ Height}$ = 3V, Test Circuit—*Figure 2*

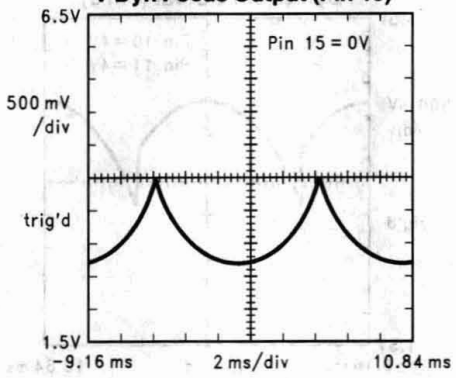
H Dyn Cntr Output (Pin 14)



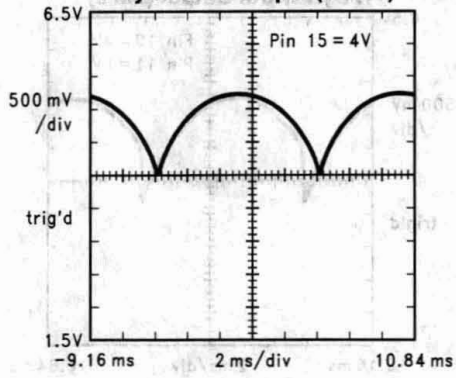
H Dyn Cntr Output (Pin 14)



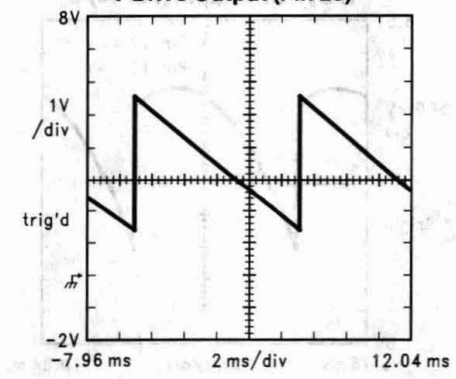
V Dyn Focus Output (Pin 16)



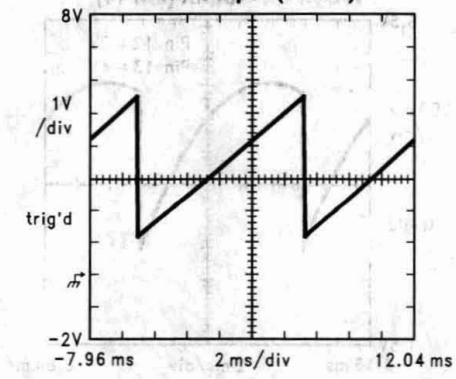
V Dyn Focus Output (Pin 16)



−V Drive Output (Pin 23)



+V Drive Output (Pin 24)



TL/H/12324–11

Circuit Description

(See *Figure 3*, Block Diagram)

The LM1295 has outputs which provide signals for correcting the following CRT distortions: Vertical de-focusing, East-West pincushion, horizontal trapezoid, horizontal parallelogram and horizontal bow. The amount and polarity of the corrections are controlled by voltages between 0V and 4V. The corrections track the vertical output amplitude.

The LM1295 has five major sections: the vertical oscillator/amplifier, the parabolic function generator and three voltage-controlled channels with the correction term outputs.

VERTICAL OSCILLATOR

The vertical oscillator is an injection-locked ramp generator with automatic level control. The automatic level control maintains the oscillator output ramp height with changes in input frequency. The oscillator requires negative-going TTL level vertical sync pulses, wider than 200 ns, to lock. In the absence of vertical sync, the oscillator free runs at the low end of the frequency range, typical 48 Hz. The vertical output amplitude is controlled by a voltage between 0V and 4V on the V Height input with a range of about 1.8 to 1, and by a voltage between 3V and 4V on the Vertical Dynamic Height input with a range of about 1.3 to 1. The control bandwidth of the V Height input is low due to the automatic level control, but that of the Vertical Dynamic Height is greater than 125 kHz. The oscillator has a circuit, requiring an external capacitor, 2f Cap, that prevents the oscillator from locking at twice the vertical sync frequency. The oscillator ramp voltage is converted into differential currents superimposed on DC currents of about 315 μA for each output. The voltage to current conversion gain is inversely proportional to the value of the resistor connected between the Rvert pins (21 and 22). Differential current outputs are provided instead of voltage to avoid ground noise. The ramp voltage goes to the parabolic function generator and to two multipliers used as voltage controlled amplifiers, one for horizontal trapezoid correction and the other for horizontal parallelogram correction.

PARABOLIC FUNCTION GENERATOR

The parabolic function generator makes a parabolic waveform from the vertical ramp. Its output goes to three multipliers used as voltage controlled amplifiers, one each for V Dyn Focus, E-W Pin, and H Bow.

VOLTAGE CONTROLLED AMPLIFIERS

The V Dyn Focus voltage controlled amplifier is controlled by the V Dyn Focus Cntl input. Its output goes to an op amp whose output is V Dyn Focus. The voltage controlled amplifier has zero gain at approx. 2V input, maximum positive gain at 4V, and maximum negative gain at 0V. The E-W Pin, H Bow, H Trap and H Para voltage controlled amplifiers are identical to the V Dyn Focus stage, each adjusted by its corresponding Cntl input. The bandwidth of the Cntl inputs is greater than 125 kHz. The E-W Pin and H Bow amplifiers have the parabolic waveform as their input, and the H Trap and H Para amplifiers have the vertical ramp as their input. The parabolic waveform and the ramp amplitudes track the vertical output amplitude so the correction amplitudes follow accordingly. The outputs of the E-W Pin amplifier (parabola) and the H Trap amplifier (ramp) are summed together in an op amp summing circuit, with H Trap weight $\frac{1}{3}$ that of E-W Pin. The output of the summing amplifier is H Dyn Width, used for correcting E-W pincushion and horizontal trapezoid distortion. The outputs of the H Bow amplifier (parabola) and the H Para amplifier (ramp) are summed together similarly, with H Bow and H Para equally weighted. The output of the summing amplifier is H Dyn Cntr, used for correcting horizontal bow and horizontal parallelogram distortion. All three op amp outputs are identical structures and are typical low output impedance type op amp outputs, capable of sinking or sourcing 5 mA minimum.

Block Diagram

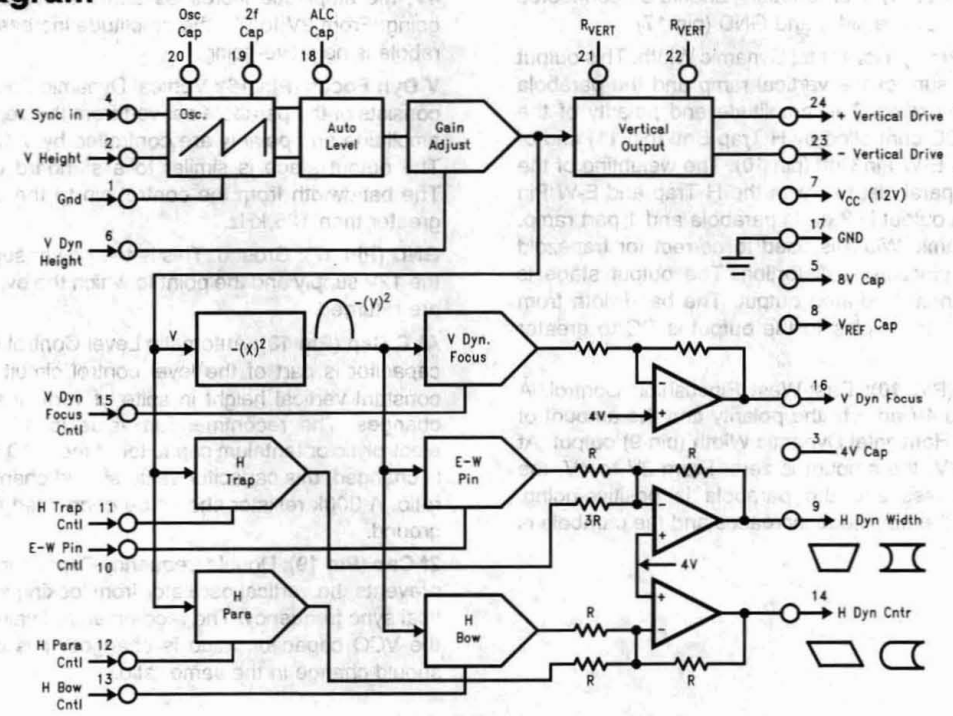


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FIGURE 3

Pin Descriptions

See *Figures 4* through *8* for Input and Output schematics.

GND (Pin 1): This pin should be connected to the power ground at pin 17.

V Height (Pin 2): Vertical Height. A voltage between 0V and 4V on this pin controls the amplitude of the +V and −V Drive currents, with increasing voltage giving increasing current. The control range is approximately 1.8 to 1. The response time is slow, being limited by the automatic level control loop.

4 V Cap (Pin 3): 4 Volt Cap Capacitor. A 10 μF capacitor, aluminum electrolytic or tantalum, should be connected between pin 3 (positive side) and GND (pin 17) to bypass the internal 4V reference.

V Sync In (Pin 4): Vertical Sync Input. The vertical sync input takes a negative-going TTL level pulse which injection locks the vertical oscillator to the vertical sync frequency if it is above the LM1295 minimum frequency. The input threshold level is approximately 2V, so pulses other than TTL level are satisfactory as long as they cross the 2V threshold with at least a 400 mV margin either side. The input should be DC coupled. The minimum pulse width is approximately 200 ns.

8 V Cap (Pin 5): 8 Volt Capacitor. A 100 μF capacitor, aluminum electrolytic or tantalum, should be connected between pin 5 (positive side) and GND (pin 17) to bypass the internal 8V reference.

V Dyn Height (Pin 6): Vertical Dynamic Height. A voltage between 3V and 4V on this pin controls the amplitude of the +V and −V Drive currents with increasing voltage giving increasing current. The control range is approximately 1.3 to 1. The bandwidth of this input is DC to greater than 125 kHz in contrast to the slow Vertical Height input.

V_{CC} (Pin 7): Power, 12V nominal. V_{CC} should be bypassed to GND (pin 17) with a 10 μF aluminum electrolytic or tantalum capacitor.

Vref Cap (Pin 8): Voltage Reference Cap. A 10 μF capacitor, aluminum electrolytic or tantalum, should be connected between pin 8 (positive side) and GND (pin 17).

H Dyn Width (Pin 9): Horizontal Dynamic Width. This output consists of the sum of the vertical ramp and the parabola derived from the ramp. The amplitude and polarity of the ramp signal is DC controlled by H Trap Cntl (pin 11) and of the parabola by E-W Pin Cntl (pin 10). The weighting of the ramp is ⅓ the parabola; i.e., with the H Trap and E-W Pin Cntls at 4V, the output is 3 parts parabola and 1 part ramp. Horizontal Dynamic Width is used to correct for trapezoid and east-west pincushion distortion. The output stage is similar to a standard op-amp output. The bandwidth from either of the 2 control pins to the output is DC to greater than 125 kHz.

E-W Pin Cntl (Pin 10): East-West Pincushion Control. A voltage of 0V to 4V adjusts the polarity and the amount of parabola in the Horizontal Dynamic Width (pin 9) output. At approximately 2V, the amount is zero. From 2V to 4V, the amplitude increases and the parabola is positive-going. From 2V to 0V, the amplitude increases and the parabola is negative-going.

H Trap Cntl (Pin 11): Horizontal Trapezoid Control. A voltage of 0V to 4V adjusts the polarity and the amount of vertical ramp in the Horizontal Dynamic Width (pin 9) output. At approximately 2V, the amount is zero. From 2V to 4V, the amplitude increases and the ramp is positive-going. From 2V to 0V, the amplitude increases and the ramp is negative-going.

H Para Cntl (Pin 12): Horizontal Parallelogram Control. A voltage of 0V to 4V adjusts the polarity and the amount of vertical ramp in the Horizontal Dynamic Center (pin 14) output. At approximately 2V, the amount is zero. From 2V to 4V, the amplitude increases and the ramp is positive-going. From 2V to 0V, the amplitude increases and the ramp is negative-going.

H Bow Cntl (Pin 13): Horizontal Bow Control. A voltage of 0V to 4V adjusts the polarity and the amount of parabola in the Horizontal Dynamic Center (pin 14) output. At approximately 2V, the amount is zero. From 2V to 4V, the amplitude increases and the parabola is positive-going. From 2V to 0V, the amplitude increases and the parabola is negative-going.

H Dyn Cntr (Pin 14): Horizontal Dynamic Center. This output consists of the sum of the vertical ramp and the parabola derived from the ramp. The amplitude and polarity of the ramp signal is DC controlled by H Para Cntl (pin 12) and of the parabola by H Bow Cntl (pin 13). The difference between this output and the Horizontal Dynamic Width output is in the weighting of the ramp, which is equal to the parabola; i.e., with the H Para and H Bow Cntls at 4V, the output is 1 part parabola and 1 part ramp. Horizontal Dynamic Center is used to correct for parallelogram and bow distortion. The output stage is similar to a standard op-amp output. The bandwidth from either of the 2 control pins to the output is DC to greater than 125 kHz.

V Dyn Focus Cntl (Pin 15): Vertical Dynamic Focus Control. A voltage of 0V to 4V adjusts the polarity and the amount of parabola in the Vertical Dynamic Focus (pin 16) output. At approximately 2V, the amount is zero. From 2V to 4V, the amplitude increases and the parabola is positive-going. From 2V to 0V, the amplitude increases and the parabola is negative-going.

V Dyn Focus (Pin 16): Vertical Dynamic Focus. This output consists of the parabola derived from the vertical ramp. The amplitude and polarity are controlled by V Dyn Focus Cntl. The output stage is similar to a standard op-amp output. The bandwidth from the control pin to the output is DC to greater than 125 kHz.

GND (Pin 17): Ground. This is the power supply ground for the 12V supply and the point to which the bypass capacitors are returned.

ALC Cap (Pin 18): Automatic Level Control Capacitor. This capacitor is part of the level control circuit that maintains constant vertical height in spite of vertical sync frequency changes. The recommended value is 4.7 μF, aluminum electrolytic or tantalum capacitor. If the VCO capacitor value is changed, this capacitor value should change in the same ratio. A 300k resistor should be connected from this pin to ground.

2f Cap (Pin 19): Double frequency Capacitor. This capacitor prevents the vertical oscillator from locking at twice the vertical sync frequency. The recommended value is 0.47 μF. If the VCO capacitor value is changed, this capacitor value should change in the same ratio.

Pin Descriptions (Continued)

Osc Cap (Pin 20): Oscillator Capacitor. This is the vertical oscillator capacitor. The recommended value is 0.1 μF. The value can be changed to change the minimum frequency.

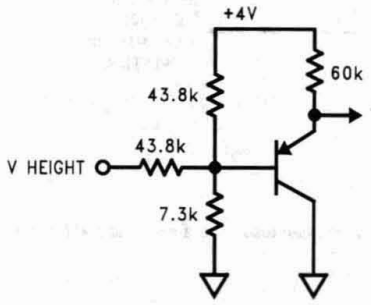
Rvert (Pin 21): Vertical Resistor. One end of the Vertical Resistor connects to this pin. This resistor determines the gain of the vertical ramp current generator. The gain is inversely proportional to the resistance. It is recommended that this be a standard 5% ¼W carbon film resistor whose negative temperature coefficient corrects for the negative temperature coefficient of the LM1295. The resistor should be located near the LM1295. The recommended value is 10 kΩ.

Rvert (Pin 22): Vertical Resistor. The other end of the Vertical Resistor connects to this pin.

− V Drive (Pin 23): − Vertical Drive. This is the negative-going vertical ramp output current of the differential pair. The ramp current waveform is superimposed on a direct current of approximately 315 μA. The waveform amplitude is determined by the Vertical Height (pin 2) control voltage and the Vertical Dynamic Height (pin 6) control voltage. The current can be converted into voltage by a resistor (typically 10 kΩ) to ground or by a differential amplifier using the differential currents as inputs. The voltage compliance of the output is typically 6V.

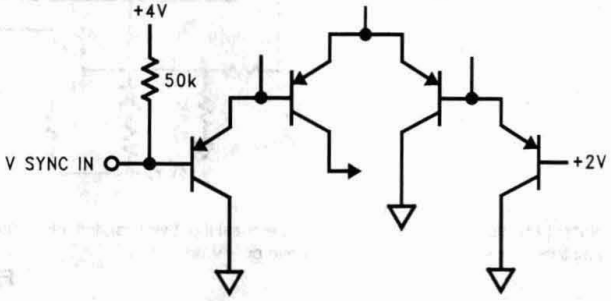
+ V Drive (Pin 24): + Vertical Drive. This is the same as − V Drive except it is the positive-going output current of the differential pair.

Input/Output Schematics



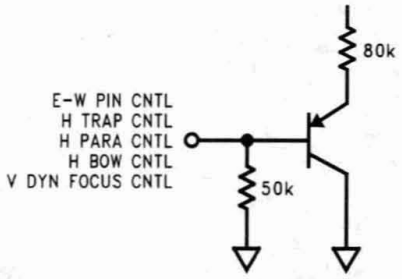
TL/H/12324–4

FIGURE 4



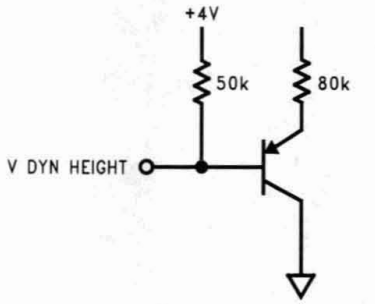
TL/H/12324–5

FIGURE 5



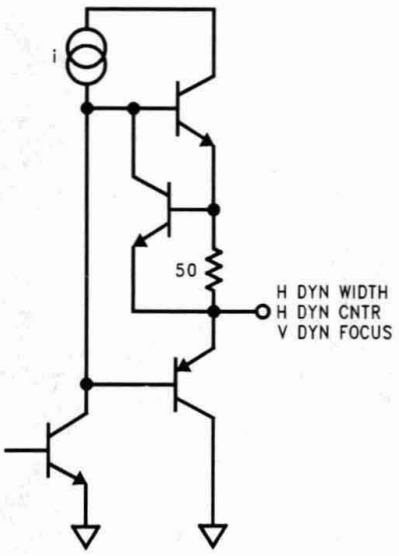
TL/H/12324–6

FIGURE 6



TL/H/12324–7

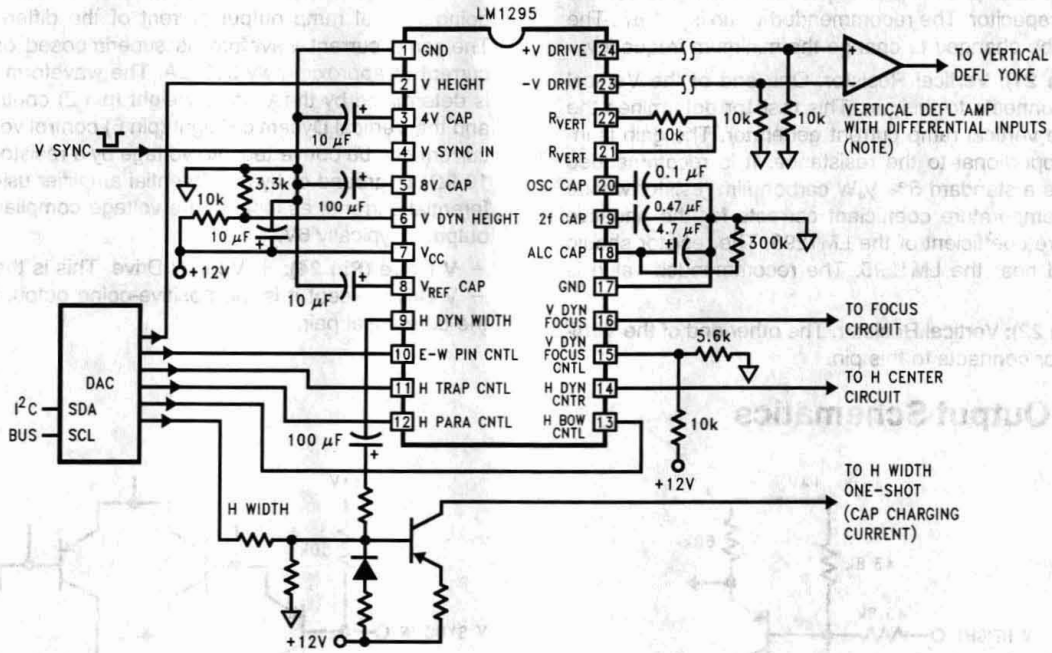
FIGURE 7



TL/H/12324–8

FIGURE 8

Typical Application



TL/H/12324–9

Note: LM1295 is designed to drive a differential input vertical deflection amplifier. The LM1295, however, can also drive a single-ended input vertical deflection amplifier by just using either the +V drive or −V drive pins.

FIGURE 9

National Semiconductor

LM1391 Phase-Locked Loop

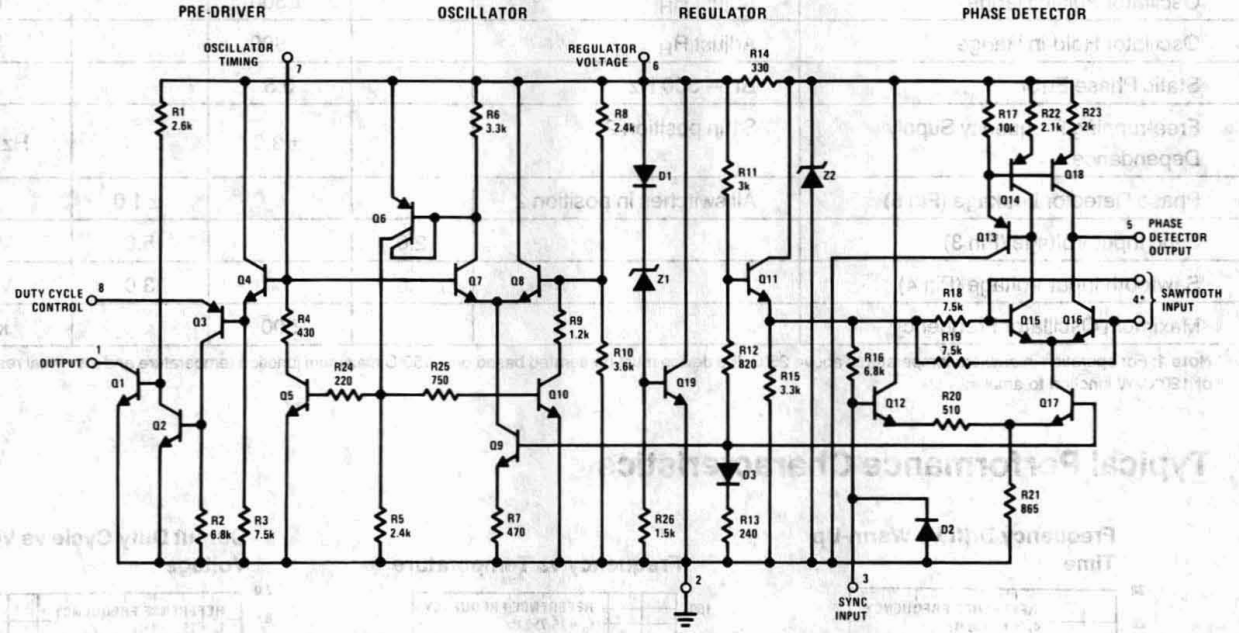
General Description

The LM1391 integrated circuit has been designed primarily for use in the horizontal section of TV receivers, but may find use in other low frequency signal processing applications. It includes a stable VCO, linear pulse phase detector, and variable duty cycle output driver.

Features

- Internal active regulator for improved supply rejection
- Uncommitted collector of output transistor
- Output transistor with low saturation and high voltage swing
- APC of the oscillator with a synchronizing signal
- DC controlled output duty cycle
- ±300 Hz typical pull-in
- Linear balanced phase detector
- Low thermal frequency drift
- Small static phase error
- Adjustable DC loop gain

Schematic Diagram



TL/H/7889–1

(*) Pin 4 Base of Q16 (LM1391) for use with (+) flyback pulse

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Current	40 mA_{DC}
Output Voltage	40 V_{DC}
Output Current	30 mA_{DC}
Sync Input Voltage (Pin 3)	5.0 Vp-p
Flyback Input Voltage (Pin 4)	5.0 Vp-p
Power Dissipation (Package Limitation) Plastic Package (Note 1)	1000 mW
Operating Temperature Range (Ambient)	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec.)	260°C

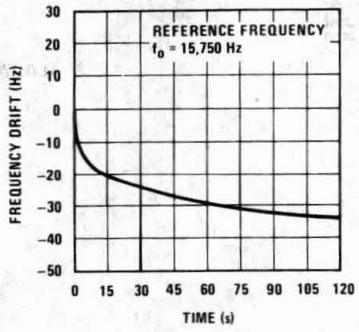
Electrical Characteristics T_A = 25°C (see test circuit, all switches in position 1)

Parameter	Conditions	Min	Typ	Max	Units
Regulated Voltage (Pin 6)	I_6 = 22 mA_{DC}	8.0	8.6	9.2	V_{DC}
Supply Current (Pin 6)			20		mA_{DC}
Collector-Emitter Saturation Voltage of Output Transistor (Pin 1)	I_{C1} = 20 mA		0.30	0.40	V_{DC}
Pin 4 Voltage			2.0		V_{DC}
Oscillator Pull-in Range	Adjust R_H		±300		Hz
Oscillator Hold-in Range	Adjust R_H		±900		Hz
Static Phase Error	Δf = 300 Hz		0.5		μs
Free-running Frequency Supply Dependance	S1 in position 2		±3.0		Hz/V_{DC}
Phase Detector Leakage (Pin 5)	All switches in position 2			±1.0	μA
Sync Input Voltage (Pin 3)		2.0		5.0	Vp-p
Sawtooth Input Voltage (Pin 4)		1.0		3.0	Vp-p
Maximum Oscillator Frequency			500		kHz

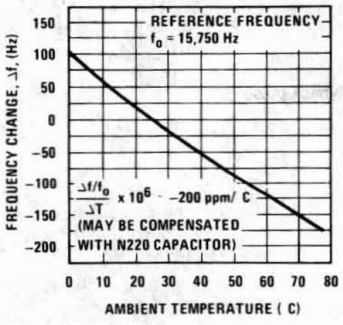
Note 1: For operation in ambient temperatures above 25°C, the device must be derated based on a 150°C maximum junction temperature and a thermal resistance of 120°C/W junction to ambient.

Typical Performance Characteristics

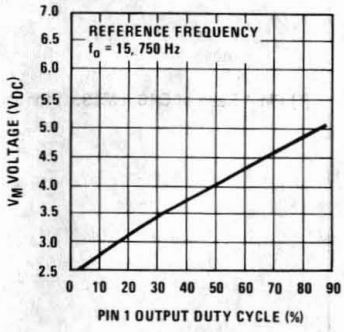
Frequency Drift vs Warm-Up Time



Frequency vs Temperature



Output Duty Cycle vs V_M Voltage



TL/H/7889–3

Application Information

The following equations may be considered when using the LM1391 in a particular application.

$$R201 = R301 = \frac{V_{CC} - 8.6}{0.02}\ \Omega$$

$$f_O \cong \frac{1}{0.6\ R_O C_O}\ \text{Hz}\quad 1.5k \le R_O < 51k$$

$$R204 \cong 10\ R_O$$

$$C203 = C204 \cong \frac{1}{600\ f_O(\text{Hz})}\ \text{F}$$

DC Loop Gain $\mu\beta \cong 3.2 \times 10^{-5}\ R_O f_O$ Hz/rad

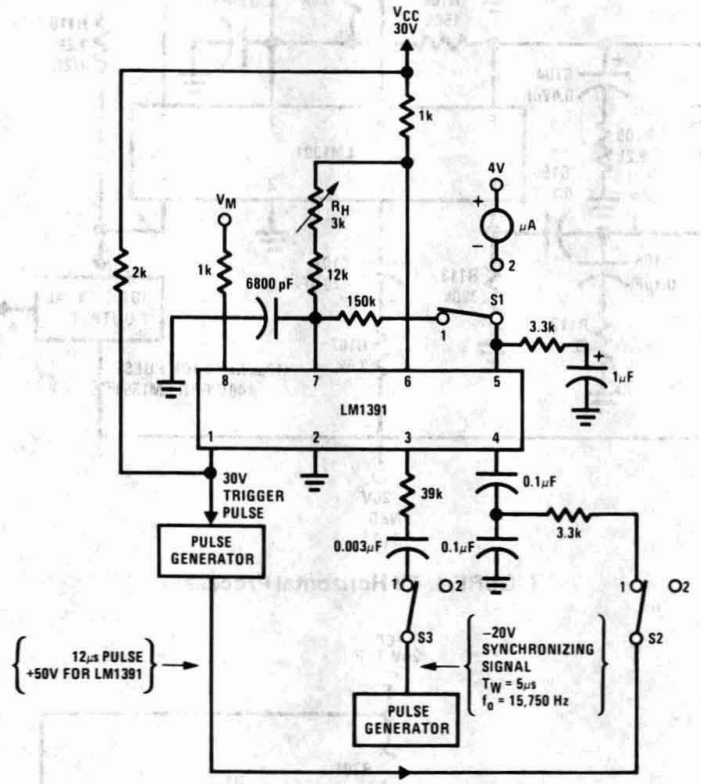
Noise Bandwidth

$$f_{nn} \cong \frac{1 + 2\pi \frac{R_X^2}{R_Y} C_C\ \mu\beta}{4 R_X C_C}\ \text{Hz}$$

Damping Factor

$$K \cong \frac{\pi}{2} \frac{R_X^2}{R_Y} C_C\ \mu\beta$$

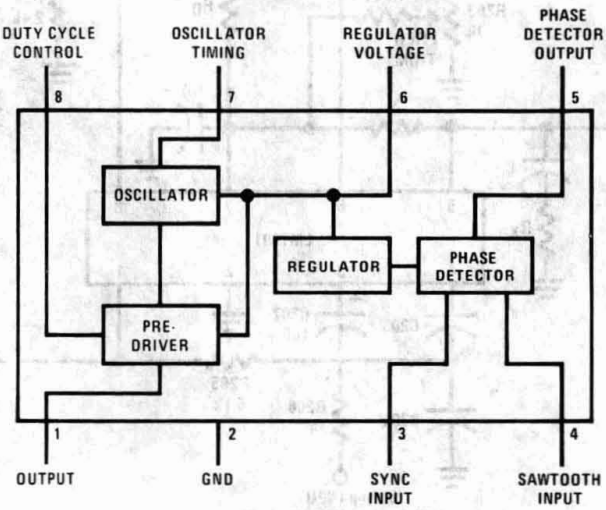
Test Circuit



TL/H/7889–4

Connection Diagram

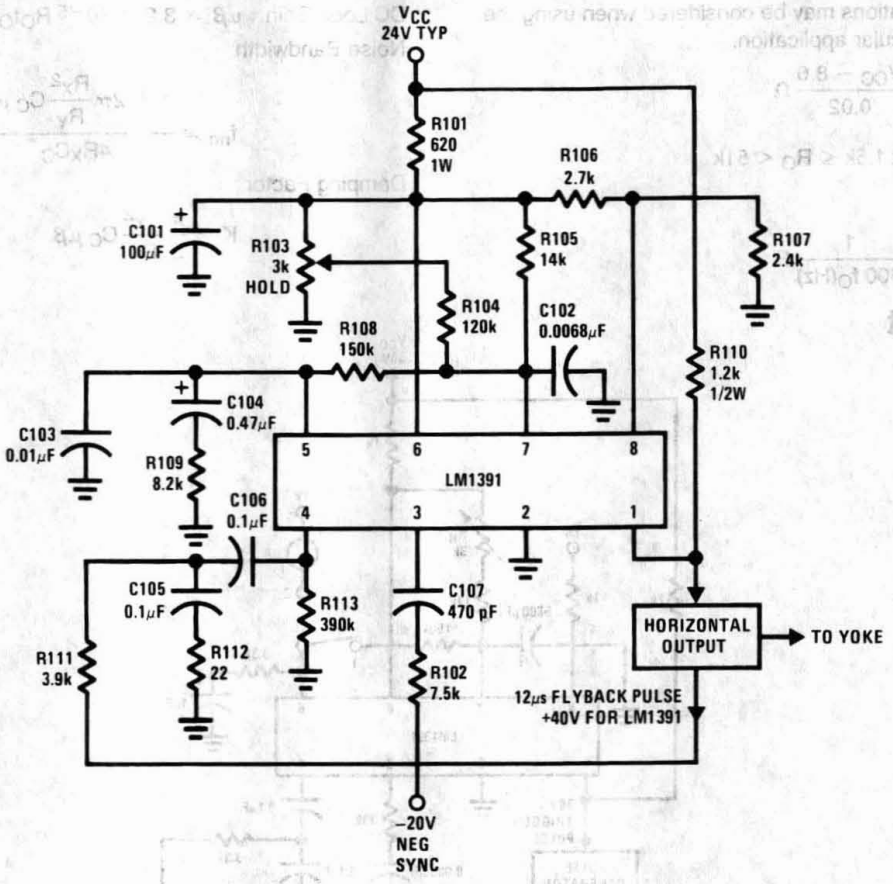
Dual-In-Line Package



TL/H/7889–2

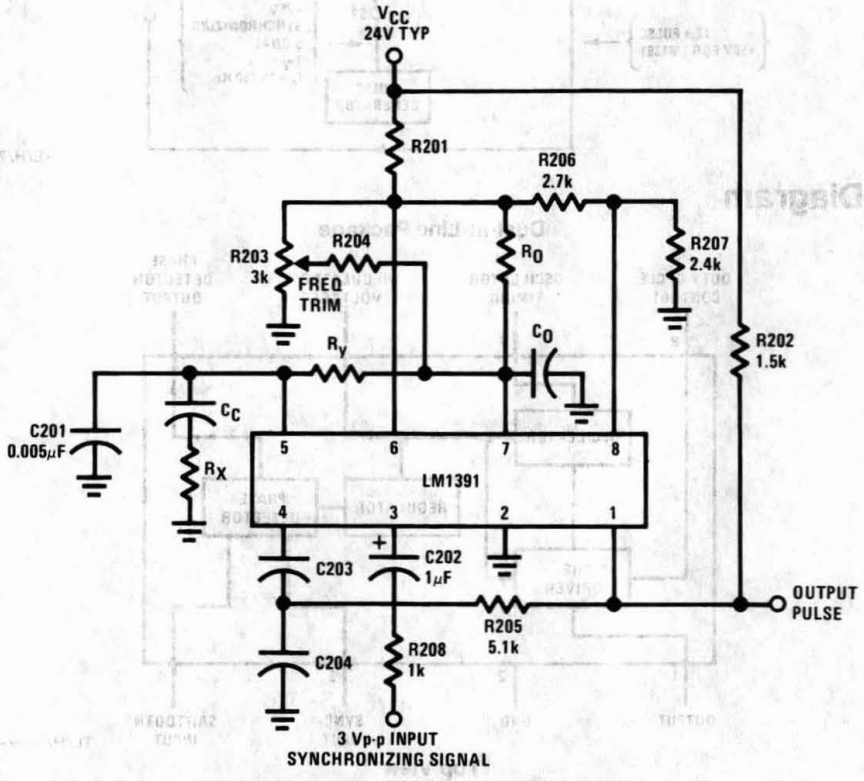
Top View
Order Number LM1391N
See NS Package Number N08E

Typical Applications



TL/H/7889–5

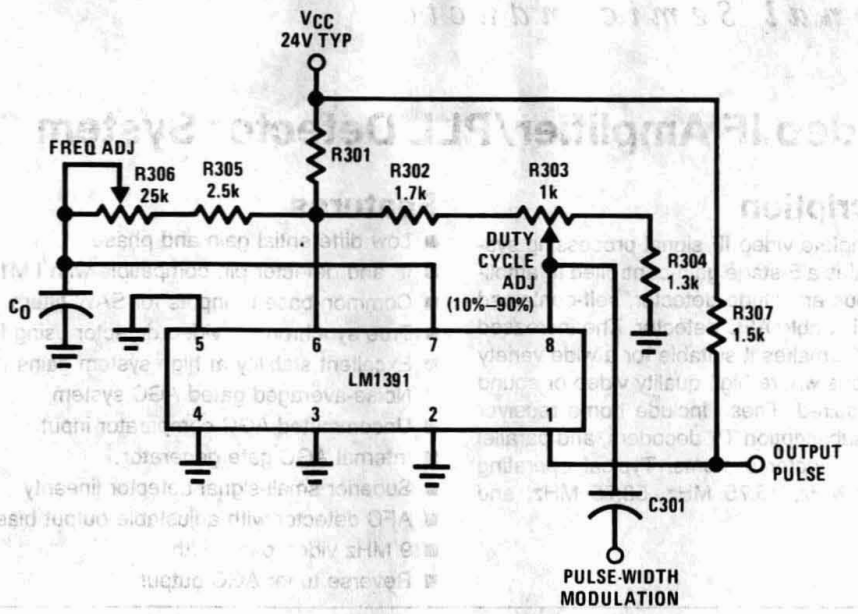
FIGURE 1. TV Horizontal Processor



TL/H/7889–6

FIGURE 2. General Purpose Phase-Lock Loop (See Applications Information)

Typical Applications (Continued)



TL/H/7889–7

FIGURE 3. Variable Duty Cycle Oscillator (See Applications Information)

National Semiconductor

LM1823 Video IF Amplifier/PLL Detector System

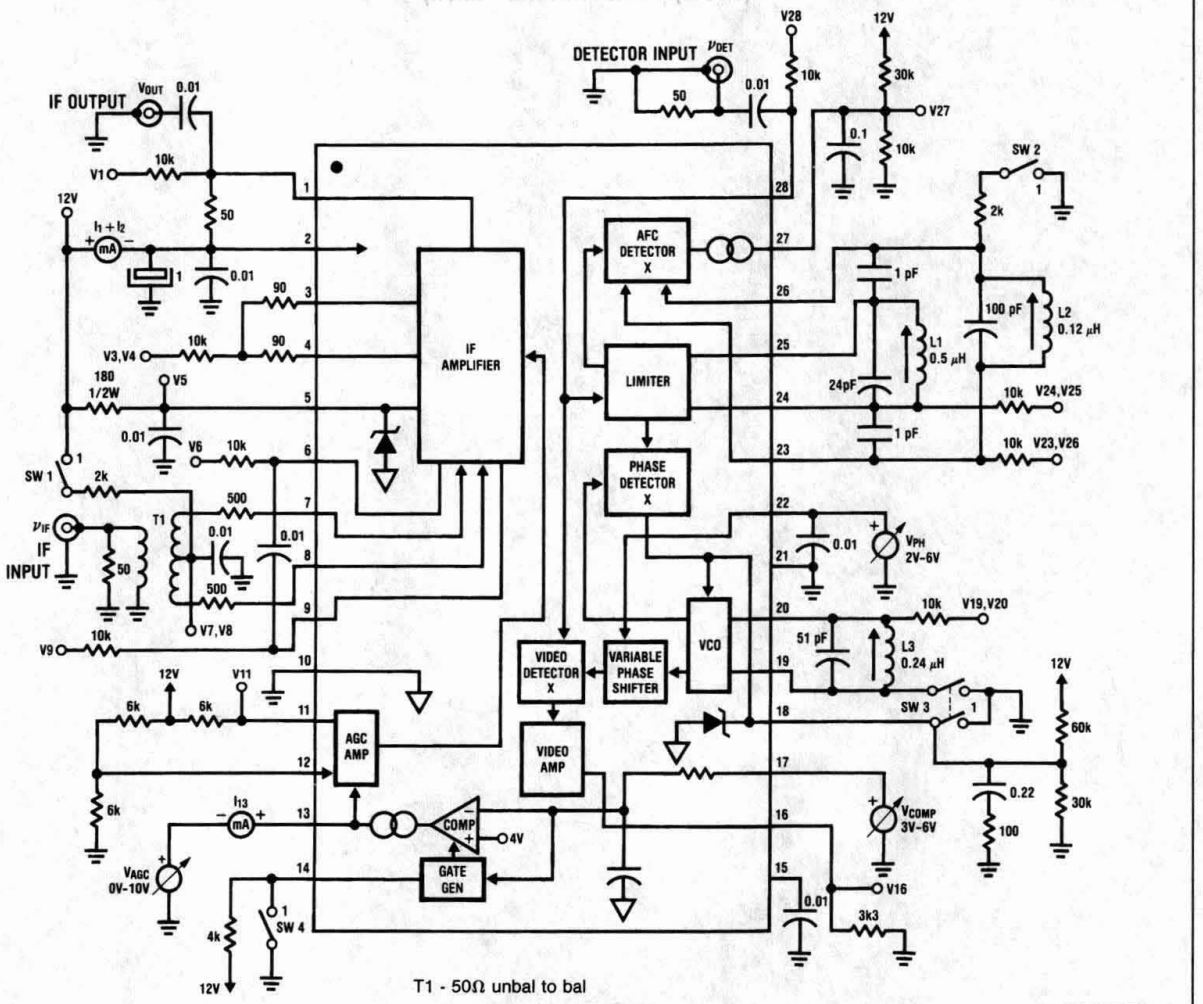
General Description

The LM1823 is a complete video IF signal processing system on a chip. It contains a 5-stage gain-controlled IF amplifier, a PLL synchronous amplitude detector, self-contained gated AGC, and a switchable AFC detector. The increased flexibility of the LM1823 makes it suitable for a wide variety of television applications where high quality video or sound carrier recovery is required. These include home receiver video IFs, cable and subscription TV decoders, and parallel sound IF/intercarrier detector systems. Typical operating frequencies are 38.9 MHz, 45.75 MHz, 58.75 MHz, and 61.25 MHz.

Features

- Low differential gain and phase
- IF and detector pin compatible with LM1822
- Common-base IF inputs for SAW filters
- True synchronous video detector using PLL
- Excellent stability at high system gains
- Noise-averaged gated AGC system
- Uncommitted AGC comparator input
- Internal AGC gate generator
- Superior small-signal detector linearity
- AFC detector with adjustable output bias
- 9 MHz video bandwidth
- Reverse tuner AGC output

Test Circuit Measure parameters at indicated test points



T1 - 50Ω unbal to bal
Mini-Circuits Lab TM01-1T

L1 - 9½T
L2 - 4½T
L3 - 6½T
} #22 wire on 3/16" form with HF core, shielded

All caps in µF unless noted

TL/H/5222–1

Order Number LM1823N
See NS Package N28B

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Power Supply Voltage, V2	15V
IF Supply Current, I_5	60mA
AGC Gate Voltage, V14	±5V
Video Output Current, I_{16}	10 mA
PLL Filter Current, I_{18}	5 mA
Detector Input Signal, v_{DET}	1 Vrms
Power Dissipation	2W
Thermal Resistance, θ_{JA}	50° C/W
Junction Temperature	125°C
Operating Temperature Range	0°C to 70°C
Storage Temperature Range	−65°C to +150°C
Lead Temp. (Soldering, 10 seconds)	260°C

DC Electrical Characteristics PARAMETERS GUARANTEED BY ELECTRICAL TESTING

$T_A = 25°C$, Test Circuit, $v_{IF} = v_{DET} = 0$, $V_{PH} = 4V$, $V_{COMP} = 4V$, and all switches in position 0 (open) unless noted.

Parameter	Conditions	Min	Typ	Max	Units
12V Supply Current, $I_1 + I_2$	$V_{AGC} = 6.7V$. $V_{COMP} = 6V$	35	60	80	mA
IF Regulator Voltage, V5	$V_{AGC} = 6.7V$, SW4 Position 1	5.8	6.4	7.0	V
IF Input Voltage, V7, V8	$V_{AGC} = 2V$, SW 2, 3, 4 Position 1	3.2	3.7	4.1	V
IF Decouple Offset, V6–V9	$V_{AGC} = 2V$, SW 2, 3, 4 Position 1		0	±30	mV
IF Peaker Voltage (Max Gain), V3, V4	$V_{AGC} = 2V$, SW 2, 3, 4 Position 1	2.3	3.0	3.6	V
IF Output Current, I1	$V_{AGC} = 9V$, SW 2, 3, 4 Position 1, Measure V1, $I_1 = (12 - V1)/50$	3.1	5.5	7.8	mA
IF Peaker Voltage (Min Gain), V3, V4	$V_{AGC} = 9V$, SW 2, 3, 4 Position 1	5.5	6.2		V
Detector Input Voltage, V28	$V_{AGC} = 6.7V$, SW 1, 4 Position 1	4.3	4.9	5.5	V
Limiter Tank Voltage, V24, V25	$V_{AGC} = 6.7V$, SW 1, 4 Position 1	6.4	7.0	7.6	V
AFC Tank Voltage, V23, V26	$V_{AGC} = 6.7V$, SW 1, 4 Position 1	4.3	4.9	5.5	V
VCO Tank Voltage, V19, V20	$V_{AGC} = 6.7V$, SW 1, 4 Position 1	4.7	5.2	5.7	V
AGC Sync Threshold, V17	SW 1, 2 Position 1, Adjust V_{COMP} for $I_{13} = 0$	3.8	4.0	4.2	V
AGC Filter Leakage Current, I_{13}	SW 1, 2, 4 Position 1		0	±5	μA
AGC Filter Charge Current, I_{13}	SW 1, 2 Position 1, $V_{COMP} = 3.5V$	1.6	2.2	2.8	mA
AGC Filter Discharge Current, I_{13}	SW 1, 2 Position 1, $V_{COMP} = 4.5V$	−0.45	−0.70	−0.90	mA
RF AGC Leakage current, I_{11}	$V_{AGC} = 2V$, All Switches Position 1, Measure V11, $I_{11} = (12 - V11)/6000$		0	20	μA
RF AGC Output Current, I_{11}	$V_{AGC} = 10V$, All Switches Position 1, Measure V11, $I_{11} = (12 - V11)/6000$	1.5	1.8		mA

Detector AC Set-Up Procedure SW 1, 4 position 1, $V_{AGC} = 0V$

1. Apply $v_{DET} = 10$ mVrms, 45.75 MHz CW at the detector input. Tune L1 for maximum AC signal at pin 25, measured with a 10x FET probe or through a 1 pF capacitor to prevent loading of the limiter tank.
2. Increase v_{DET} to 60 mVrms. Adjust L3 until the PLL locks, as indicated by a DC voltage at the video output pin 16.
3. With the detector locked, adjust L3 for 4.0V at pin 18.
4. Adjust V_{PH} for maximum detector efficiency by monitoring pin 16 for a minimum DC voltage.
5. Adjust L2 for 3.0V at pin 27 (on sensitive slope of AFC curve).

AC Electrical Characteristics PARAMETERS GUARANTEED BY ELECTRICAL TESTING

$T_A = 25°C$, Test Circuit, detector set-up as above, f = 45.75 MHz, $V_{AGC} = 6.7V$, $V_{COMP} = 4V$, and all switches in position 0 (open) unless noted.

Parameter	Conditions	Min	Typ	Max	Units
IF Amplifier Gain, v_{OUT}/v_{IF} (Note 1)	$V_{AGC} = 2V$, SW 2, 3, 4 Position 1, $v_{IF} = 500\ \mu$Vrms	25	35		dB
V_{AGC} for 15 dB Gain Reduction	SW 2, 3, 4 Position 1, $v_{IF} = 2.8$ mVrms, Adjust V_{AGC} for Same v_{OUT} as Gain Test	4.2	4.6	5.0	V
V_{AGC} for 45 dB Gain Reduction	SW 2, 3, 4 Position 1, $v_{IF} = 89$ mVrms, Adjust V_{AGC} for Same v_{OUT} as Gain Test	5.1	5.5	6.1	V
Zero Carrier Level, V16	SW 1, 2, 4 Position 1, $v_{DET} = 0$	6.6	7.4	8.4	V
Detected Output Level, ΔV16	SW 1, 2, 4 Position 1, $v_{DET} = 60$ m/Vrms, Measure Change in V16 from Zero Carrier Test	2	3	4.3	V
Overload Output Voltage, V16	SW 1, 2, 4 Position 1, $v_{DET} = 600$ mVrms		2	3	V
AFC Output Voltage (OFF), V27	SW 1, 2, 4 Position 1, $v_{DET} = 0$	2.8	3.0	3.2	V
AFC Minimum Output Voltage, V27	SW 1, 4 Position 1, $v_{DET} = 60$ mVrms, 46.75 MHz		0.5	1.0	V
AFC Maximum Output Voltage, V27	SW 1, 4 Position 1, $v_{DET} = 60$ mVrms, 44.75 MHz	9	10		V
PLL Pull-In Range, Δf	SW 1, 4 Position 1, $v_{DET} = 60$ mVrms, Vary Frequency and Measure the Difference between Lock Points	2	3		MHz

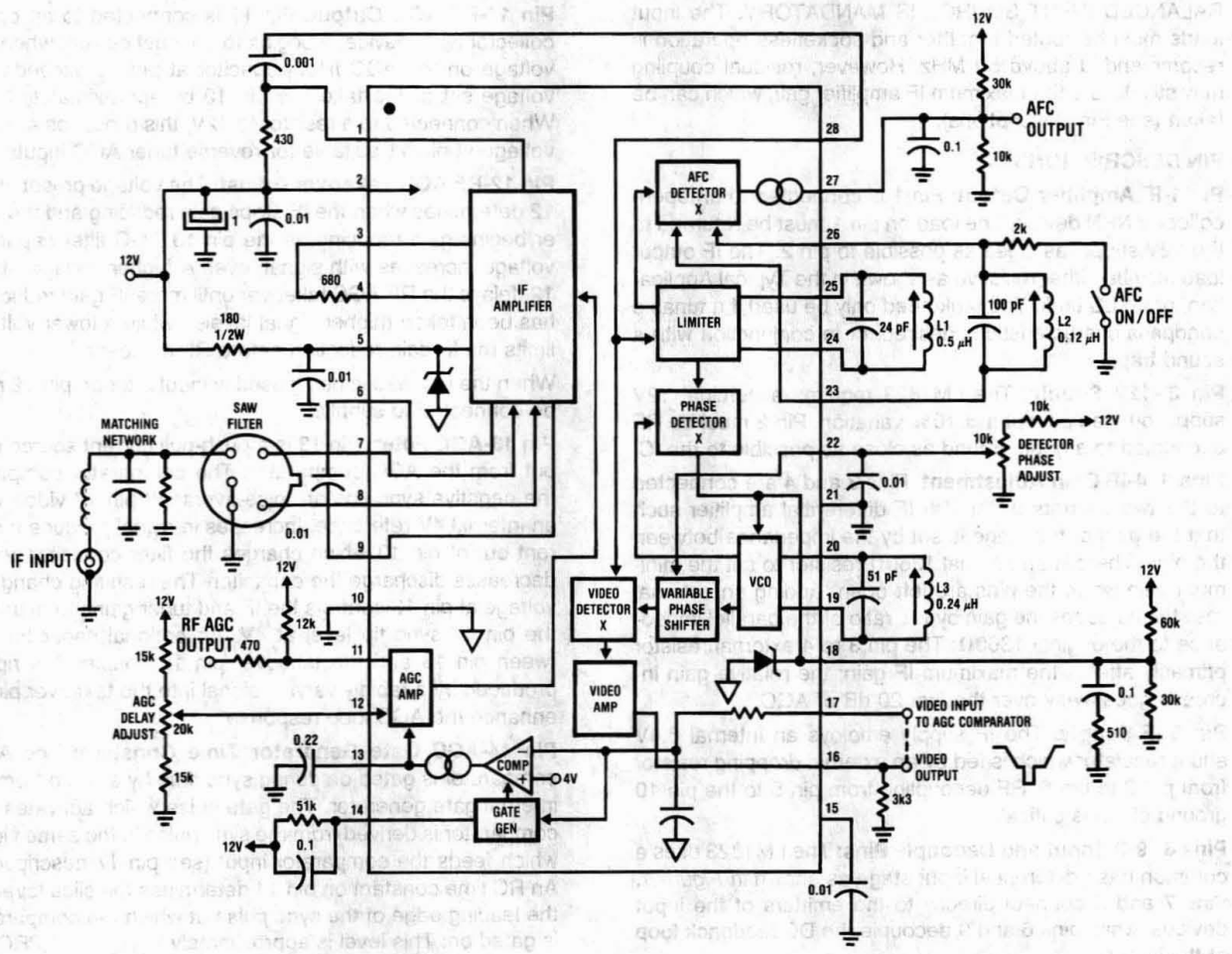
Note 1: The IF amplifier gain is specified with the IF output connected to a 50Ω measurement system which results in a 25Ω loaded impedance. The gain in an actual application will typically be 26 dB higher.

Design Parameters NOT TESTED OR GUARANTEED Typical Application Circuit

Parameter	Typ	Units
Maximum System Operating Frequency	70	MHz
IF Input Impedance (Differential Pin 7–8), 45 MHz	60	Ω
IF Output Impedance, 45 MHz	10	kΩ
IF Gain Control Range	55	dB
Detector Input Impedance, 45 MHz	2	kΩ
Detector Output Bandwidth, −3 dB	9	MHz
Detector Differential Gain (Note 2)	3	%
Detector Differential Phase (Note 2)	1	deg
Detector Output Harmonic Levels below 3 Vp-p Video	−40	dB
VCO Temperature Coefficient	−150	ppm/°C

Note: 2: Differential gain and phase measured with the limiter tank adjusted for minimum differential phase.

Typical Application 45.75 MHz (see Application Notes)



TL/H/5222–2

SAW Filter - MuRata SAF45MC/MA

L1 - 9½T } #22 wire
L2 - 4½T } on 3.16" form with
L3 - 6½T } HF core, shielded

All caps in μF unless noted

Application Notes Refer to Typical Application Circuit

COMMENTS ON RF Coupling

The LM1823 is a high gain RF system which is critically dependent on the ground plane and positioning of the external components. For this reason, it is suggested that the printed circuit layout shown in *Figure 3* be strictly adhered to.

The most sensitive points in the system to unwanted RF coupling are the IF input pins 6–9. There are two different signals which can cause different problems when coupling into the IF inputs. If the IF output is coupling to the input, it can cause bandpass tilting, peaking, and in extreme cases, oscillation. The other signal which can couple to the IF inputs is the PLL detector VCO. This VCO coupling can cause AFC skewing, non-symmetrical detector pull-in, and failure of the detector to acquire lock at weak signal levels. These input coupling problems will be most acute at maximum gain and will decrease as the IF is gain reduced by AGC action.

The differential IF inputs offer a large amount of inherent rejection to unwanted RF coupling. Therefore, A FULLY BALANCED INPUT SOURCE IS MANDATORY. The input leads must be routed together and socketless operation is recommended above 50 MHz. However, residual coupling may still dictate the maximum IF amplifier gain which can be taken (see Pin Descriptions).

PIN DESCRIPTIONS

Pin 1-IF Amplifier Output: Pin 1 is connected to an open-collector NPN device. The load on pin 1 must be returned to the 12V supply as close as possible to pin 2. The IF output load may be either resistive as shown in the Typical Application, or an LC tank. The tank need only be used if a tunable bandpass characteristic is desired, or in conjunction with a sound trap.

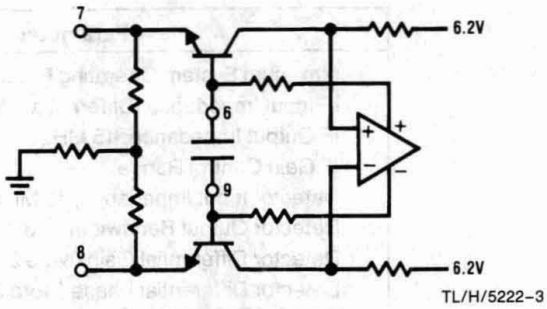
Pin 2–12V Supply: The LM1823 requires a nominal 12V supply but can accept a ±10% variation. Pin 2 must be RF decoupled to a good ground as close as possible to the IC.

Pins 3, 4-IF Gain Adjustment: Pins 3 and 4 are connected to the two emitters of the 4th IF differential amplifier such that the gain of the stage is set by the impedance between the pins. There is an internal 1360Ω resistor to set the minimum gain when the pins are left open. Adding an external resistor increases the gain by the ratio of the parallel impedance to the original 1360Ω. The pin 3 to 4 external resistor primarily affects the maximum IF gain; the relative gain increase goes away over the first 20 dB of AGC.

Pin 5-IF Supply: The IF supply employs an internal 6.4V shunt regulator which is fed by an external dropping resistor from pin 2 to pin 5. RF decoupling from pin 5 to the pin 10 ground plane is critical.

Pins 6–9-IF Input and Decouple Pins: The LM1823 uses a common-base differential input stage as shown in *Figure 1*. Pins 7 and 8 connect directly to the emitters of the input devices, while pins 6 and 9 decouple the DC feedback loop at the bases.

The gain of a common-base amplifier depends inversely on the source impedance. The LM1823 is designed to operate from differential impedances in the 500Ω to 2000Ω range, which is typical for surface acoustic wave (SAW) filters. Alternatively, the IF may be used with a transformer input configuration similar to that shown in the Test Circuit, as long as the required source impedance is maintained. In all cases a balanced source must be used.



TL/H/5222–3

FIGURE 1. IF Input Stage

Both the input network to pins 7 and 8 and decoupling capacitor between pin 6 and pin 9 must be as close to the device as is physically possible to minimize RF coupling.

Pin 10-IF Ground: Pin 10 grounds the IF and AGC circuits in the LM1823. It is separate from the detector and chip substrate grounds to prevent internal coupling.

Pin 11-RF AGC Output: Pin 11 is connected to an open-collector NPN device. It begins to conduct current when the voltage on the AGC filter capacitor at pin 13 exceeds the voltage set at the takeover pin 12 by approximately 0.6V. When connected to a resistor to 12V, this produces a falling voltage at pin 11 suitable for reverse tuner AGC inputs.

Pin 12-RF AGC Takeover Adjust: The voltage preset at pin 12 determines when the IF stops gain reducing and the tuner begins gain reducing as the pin 13 AGC filter capacitor voltage increases with signal level. A higher voltage at pin 12 delays the RF AGC takeover until more IF gain reduction has been taken (higher signal levels), while a lower voltage limits the IF gain reduction before RF takeover.

When the LM1823 is being used without a tuner, pin 12 may be connected to supply.

Pin 13-AGC Filter: Pin 13 is a push-pull current source output from the AGC comparator. The comparator compares the negative sync tips of noise-averaged pin 17 video with an internal 4V reference. Increases in signal produce a current out of pin 13 which charges the filter capacitor, while decreases discharge the capacitor. The resulting change in voltage at pin 13 controls the IF and tuner gains to maintain the pin 17 sync tip level at 4V. An optional capacitor between pin 13 and the takeover pin 12 couples the ripple produced by a rapidly varying signal into the takeover pin to enhance the AGC loop response.

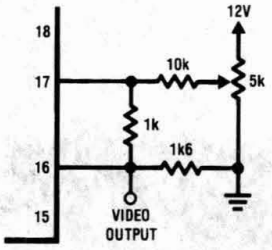
Pin 14-AGC Gate Generator Time Constant: The AGC comparator is gated on during sync time by a pulse from an internal gate generator. The gate pulse which activates the comparator is derived from the sync pulse in the same video which feeds the comparator input (see pin 17 description). An RC time constant on pin 14 determines the slice level on the leading edge of the sync pulse at which the comparator is gated on. This level is approximately $V_{SLICE} = 1/(2RC)$ in millivolts above the sync tip, and should be set at ≤25% of the sync amplitude. Note that V_{SLICE} only determines when the AGC comparator turns on, and is unrelated to the comparator reference.

In the Typical Application, $V_{SLICE} = 100$ mV, or 10% of a 1V sync pulse. Increasing V_{SLICE} improves the AGC recovery from step changes in signal level but increases the risk of video interaction. When modifying the time constant, change the capacitor value only.

Application Notes (Continued) Refer to Typical Application Circuit

Pin 15-Supply Decouple: Pin 15 is an additional connection to the 12V supply to allow RF decoupling on the detector side of the chip.

Pin 16-Video Output: Pin 16 is a Darlington NPN emitter-follower output supplying negative sync video. With no detector input signal the pin 16 voltage sits at the zero carrier level, representing peak white. As the input signal level increases, the pin 16 voltage decreases towards black. The sync pulses are normally the most negative portion of the recovered video.



TL/H/5222–4

FIGURE 2. Adjustable Recovered Video Level

Pin 17-AGC Comparator Input: External negative sync video is fed to the AGC comparator and gate generator via pin 17. An internal low pass filter removes high frequency noise and transients. The peak-to-peak video level with the AGC loop active is determined by the difference between the zero carrier level at pin 17 and the 4V sync tip level being held by the AGC comparator (see pin 13 description).

When the LM1823 is being used to recover normal video, pin 17 may simply be returned to pin 16. This results in a nominal 3 Vp-p video level, but which is subject to variations in the pin 16 zero carrier level. The network shown in *Figure 2* can be used to change the zero carrier at pin 17, thus providing an adjustable recovered video level. The pin 16 video level should be maintained at between 1 Vp-p minimum and 4 Vp-p maximum.

In suppressed sync systems, the recovered video at pin 16 may require processing to restore normal sync amplitude before being fed to pin 17. In this case, it is mandatory that a DC path be maintained for the zero carrier level through any external circuitry. Any DC level shift between pins 16 and 17 will have the effect of changing the video level as previously described.

Pin 18-PLL Filter: Pin 18 is connected to both the output of the phase detector and the control input of the VCO. The polarity of the VCO control characteristic is such that increasing the pin 18 voltage increases the VCO frequency. An external resistive divider at pin 18 serves two functions. The divider parallel impedance sets the gain of the phase detector, while the divider ratio places the quiescent voltage at the center of the VCO control characteristic. The 20 kΩ impedance, ⅓ supply divider shown in the Typical Application has been chosen to provide optimum performance. The series capacitor and resistor to ground complete the PLL filter.

An internal zener clamp to ground at pin 18 prevents the phase detector output from pulling the VCO control input over 5.6V. For this reason, external voltages should not be forced at pin 18 to avoid damaging the clamp.

Pins 19, 20-VCO Tank: A parallel LC tank between pins 19 and 20 sets the VCO center frequency. The tank Q is RpL/Xc, where RpL is the coil Rp loaded by an internal 1500Ω resistor. Increasing the Q (larger C) improves stability but reduces the VCO control range. The tank shown in the Typical Application will yield a loaded Q of around 15, providing stable operation with a control range in excess of 2 MHz.

Pin 21-Substrate Ground: Pin 21 grounds the chip substrate along with all of the AFC and PLL detector grounds.

Pin 22-Detector Phase Adjust: The video detector requires a reference signal in phase with the input signal carrier for maximum detection efficiency. However, the action of the PLL inherently sets the VCO phase in quadrature (at 90 degrees) with the limiter output. Therefore a variable phase shift network, controlled by pin 22, is used internally between the VCO and video detector to insure proper phasing. Pin 22 requires an adjustment voltage centered at ⅓ supply with ±2V of control range.

The pin 22 adjustment procedure described in the Detector AC Set-Up Procedure is an open loop approach where the voltage is adjusted for maximum detected output with a fixed detector input signal. In the Typical Application, with the detector input being fed from the IF amplifier and the AGC loop active, the pin 22 adjustment is made by maximizing the AGC filter voltage at pin 13. In all cases the detector phase adjustment must be performed after the limiter is tuned.

Pins 23, 26-AFC Tank: A parallel LC tank between pins 23 and 26 sets the center of the AFC characteristic. The internal resistance is typically 20 kΩ, so that Q will be dominated by the coil Rp. The L/C ratio shown in the Typical Application maximizes Q to provide a steep AFC output slope.

A quadrature input signal is required at the AFC tank to operate the AFC detector. This signal is derived by light capacitive coupling from the limiter tank. For applications at 45 MHz and above, the stray printed circuit capacitance from the adjacent limiter tank couples sufficient signal for proper operation. However, at lower IF frequencies, small (1 pF–5 pF) capacitors may be required between the adjacent pins as shown in the Test Circuit.

A second function of pins 23 and 26 allows turning the AFC detector OFF by grounding either side of the AFC tank. Up to 2 kΩ may be placed in series with the switch connection to prevent unbalancing the tank.

Pins 24, 25-Limiter Tank: A parallel LC tank between pins 24 and 25 forms the tuned load for a single stage limiting amplifier which strips amplitude information from the signals feeding the AFC and phase detectors. The amplifier has a small signal gain of approximately 50, with internal Schottky diodes across the tank to limit the output amplitude to 500 mVp-p.

The linearity of the detector video outputs depends directly on limiter tuning. Making the limiter adjustment based on maximum signal level at pins 24, 25 as outlined in the Detector AC Set-Up Procedure results in nearly optimum output linearity. However, to completely null the output differential phase the limiter should be adjusted while monitoring this parameter.

Pin 27-AFC Detector Output: Pin 27 is push-pull current source output from the AFC detector. The polarity is such that pin 27 sources current when the input signal is below the center frequency, and sinks current above the center frequency. An external resistive divider sets both the gain and quiescent output voltage of the AFC. Although the net-

Application Notes (Continued) Refer to Typical Application Circuit

work shown in the Typical Application sets up the output at ¼ supply, it could easily be changed to ½ supply by using equal-valued resistors. When setting up the AFC detector, the tank should always be tuned so the output is at the quiescent divider voltage with the desired center frequency applied.

Pin 28-Detector Input: Pin 28 is internally DC-biased and requires an AC-coupled input signal. The network between pins 1 and 28 should not allow over 1 Vrms at the input during signal transients to prevent overloading the detector. When a tank is being used for the IF output load, a capacitive divider may be used from pin 1 to pin 28 in which the series equivalent capacitance resonates with the coil.

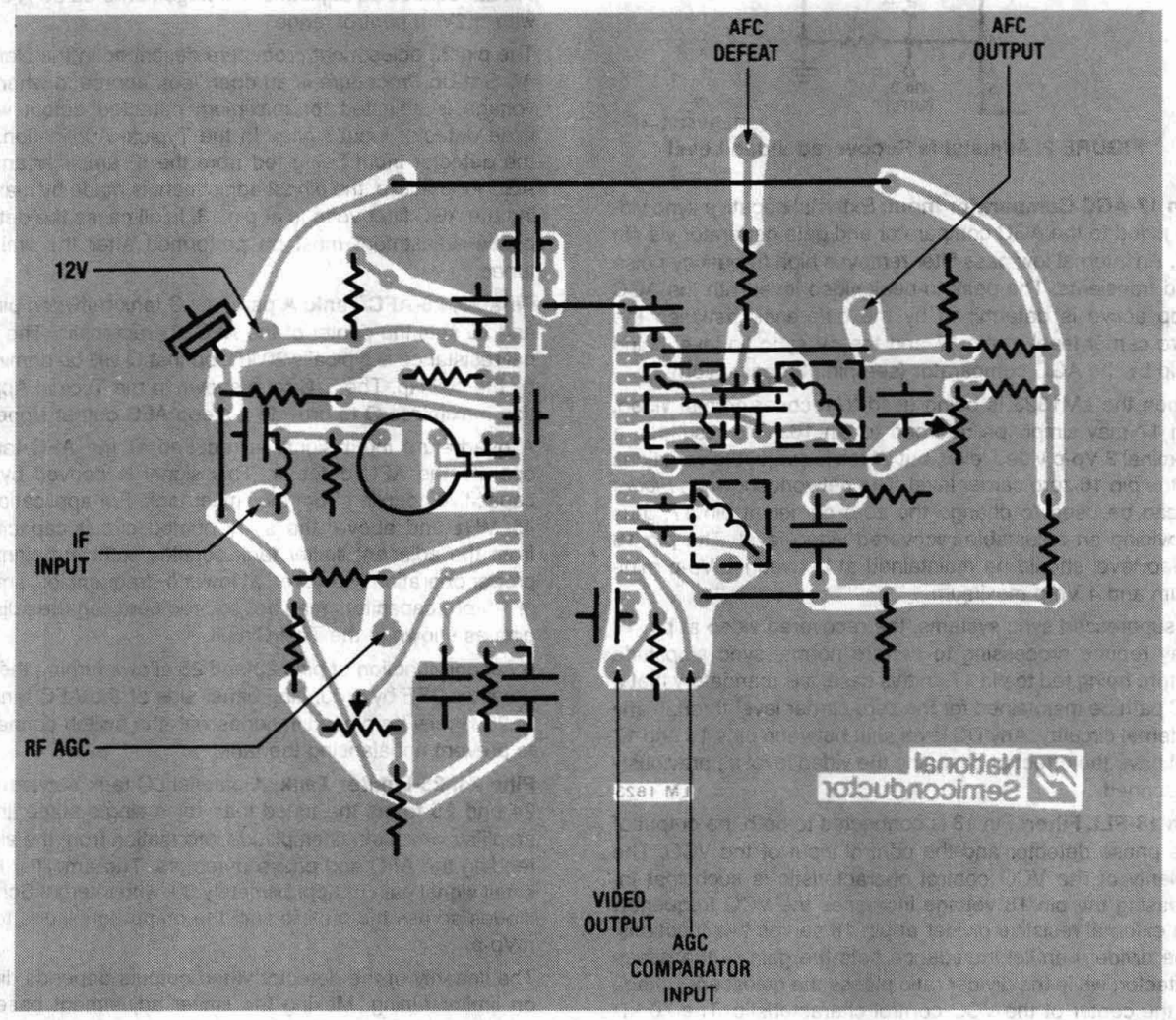


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FIGURE 3. Printed Circuit Layout (Component Side).

National Semiconductor

LM1881 Video Sync Separator

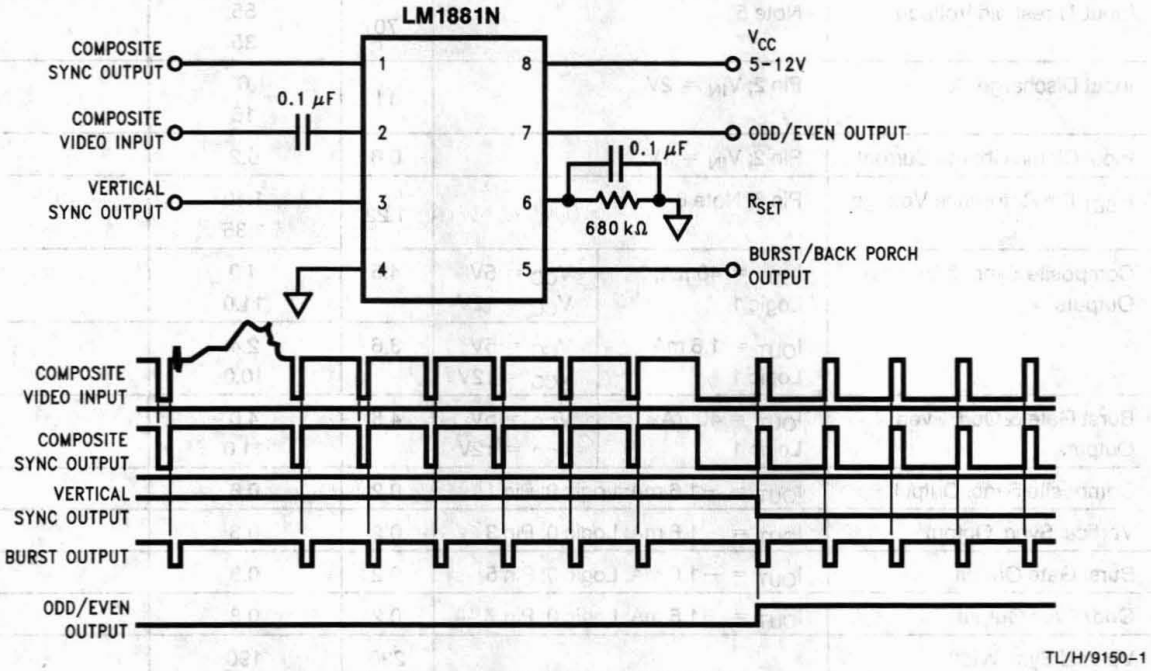
General Description

The LM1881 Video sync separator extracts timing information including composite and vertical sync, burst/back porch timing, and odd/even field information from standard negative going sync NTSC, PAL*, and SECAM video signals with amplitude from 0.5V to 2V p-p. The integrated circuit is also capable of providing sync separation for non-standard, faster horizontal rate video signals. The vertical output is produced on the rising edge of the first serration in the vertical sync period. A default vertical output is produced after a time delay if the rising edge mentioned above does not occur within the externally set delay period, such as might be the case for a non-standard video signal.

Features

- AC coupled composite input signal
- >10 kΩ input resistance
- <10 mA power supply drain current
- Composite sync and vertical outputs
- Odd/even field output
- Burst gate/back porch output
- Horizontal scan rates to 150 kHz
- Edge triggered vertical output
- Default triggered vertical output for non-standard video signal (video games-home computers)

Connection Diagram



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Order Number LM1881M or LM1881N
See NS Package Number M08A or N08E

*PAL in this datasheet refers to European broadcast TV standard "Phase Alternating Line", and not to Programmable Array Logic.

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	13.2V
Input Voltage	3 Vpp (V_{CC} = 5V) 6 Vpp (V_{CC} ≥ 8V)
Output Sink Currents; Pins 1, 3, 5	5 mA
Output Sink Current; Pin 7	2 mA
Package Dissipation (Note 1)	1100 mW
Operating Temperature Range	0°C − 70°C
Storage Temperature Range	−65°C to +150°C
ESD Susceptibility (Note 2)	2 kV
Soldering Information	
Dual-In-Line Package (10 sec.)	260°C
Small Outline Package	
Vapor Phase (60 sec.)	215°C
Infrared (15 sec.)	220°C

See AN-450 "Surface Mounting Methods and their Effect on Product Reliability" for other methods of soldering surface mount devices.

Electrical Characteristics

V_{CC} = 5V; Rset = 680 kΩ; T_A = 25°C; Unless otherwise specified

Parameter	Conditions		Typ	Tested Limit (Note 3)	Design Limit (Note 4)	Units (Limits)
Supply Current	Outputs at Logic 1	V_{CC} = 5V V_{CC} = 12V	5.2 5.5	10 12		mAmax mAmax
DC Input Voltage	Pin 2		1.5	1.3 1.8		Vmin Vmax
Input Threshold Voltage	Note 5		70	55 85		mVmin mVmax
Input Discharge Current	Pin 2; V_{IN} = 2V		11	6 16		μAmin μAmax
Input Clamp Charge Current	Pin 2; V_{IN} = 1V		0.8	0.2		mAmin
R_{SET} Pin Reference Voltage	Pin 6; Note 6		1.22	1.10 1.35		Vmin Vmax
Composite Sync. & Vertical Outputs	I_{OUT} = 40 μA; Logic 1	V_{CC} = 5V V_{CC} = 12V	4.5	4.0 11.0		Vmin Vmin
	I_{OUT} = 1.6 mA Logic 1	V_{CC} = 5V V_{CC} = 12V	3.6	2.4 10.0		Vmin Vmin
Burst Gate & Odd/Even Outputs	I_{OUT} = 40 μA; Logic 1	V_{CC} = 5V V_{CC} = 12V	4.5	4.0 11.0		Vmin Vmin
Composite Sync. Output	I_{OUT} = −1.6 mA; Logic 0; Pin 1		0.2	0.8		Vmax
Vertical Sync. Output	I_{OUT} = −1.6 mA; Logic 0; Pin 3		0.2	0.8		Vmax
Burst Gate Output	I_{OUT} = −1.6 mA; Logic 0; Pin 5		0.2	0.8		Vmax
Odd/Even Output	I_{OUT} = −1.6 mA; Logic 0; Pin 7		0.2	0.8		Vmax
Vertical Sync Width			230	190 300		μsmin μsmax
Burst Gate Width	2.7 kΩ from Pin 5 to V_{CC}		4	2.5 4.7		μsmin μsmax
Vertical Default Time	Note 7		65	32 90		μsmin μsmax

Note 1: For operation in ambient temperatures above 25°C, the device must be derated based on a 150°C maximum junction temperature and a package thermal resistance of 110° C/W, junction to ambient.

Note 2: ESD susceptibility test uses the "human body model, 100 pF discharged through a 1.5 kΩ resistor".

Note 3: Typicals are at T_J = 25°C and represent the most likely parametric norm.

Note 4: Tested Limits are guaranteed to National's AOQL (Average Outgoing Quality Level).

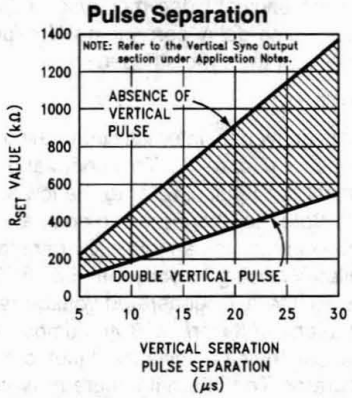
Note 5: Relative difference between the input clamp voltage and the minimum input voltage which produces a horizontal output pulse.

Note 6: Careful attention should be made to prevent parasitic capacitance coupling from any output pin (Pins 1, 3, 5, and 7) to the R_{SET} pin (Pin 6).

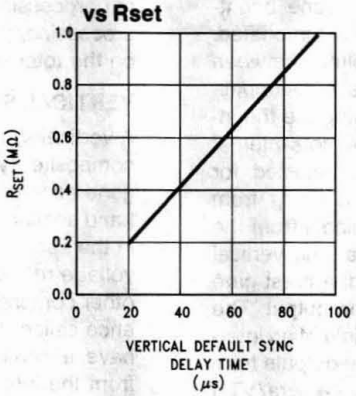
Note 7: Delay time between the start of vertical sync (at input) and the vertical output pulse.

Typical Performance Characteristics

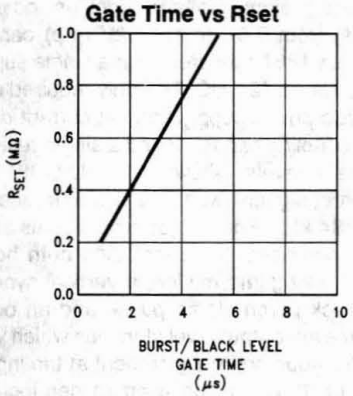
R_{set} Value Selection vs Vertical Serration Pulse Separation


NOTE: Refer to the Vertical Sync Output section under Application Notes.
ABSENCE OF VERTICAL PULSE
DOUBLE VERTICAL PULSE
RSET VALUE (kΩ)
VERTICAL SERRATION PULSE SEPARATION (μs)

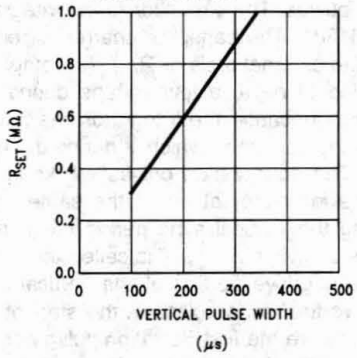
Vertical Default Sync Delay Time vs Rset



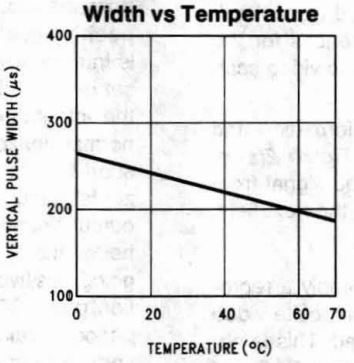
Burst/Black Level Gate Time vs Rset



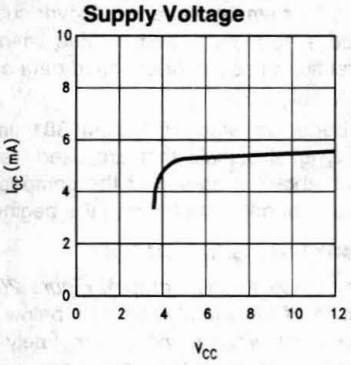
Vertical Pulse Width vs Rset



Vertical Pulse Width vs Temperature



Supply Current vs Supply Voltage



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2

Application Notes

The LM1881 is designed to strip the synchronization signals from composite video sources that are in, or similar to, the N.T.S.C. format. Input signals with positive polarity video (increasing signal voltage signifies increasing scene brightness) from 0.5V (p-p) to 2V (p-p) can be accommodated. The LM1881 operates from a single supply voltage between 5V DC and 12V DC. The only required external components beside power supply and set current decoupling are the input coupling capacitor and a single resistor that sets internal current levels, allowing the LM1881 to be adjusted for source signals with line scan frequencies differing from 15.734 kHz. Four major sync signals are available from the I/C: composite sync including both horizontal and vertical scan timing information; a vertical sync pulse; a burst gate or back porch clamp pulse; and an odd/even output. The odd/even output level identifies which video field of an interlaced video source is present at the input. The outputs from the LM1881 can be used to gen-lock video camera/VTR signals with graphics sources, provide identification of video fields for memory storage, recover suppressed or contaminated sync signals, and provide timing references for the extraction of coded or uncoded data on specific video scan lines.

To better understand the LM1881 timing information and the type of signals that are used, refer to *Figure 2(a–e)* which shows a portion of the composite video signal from the end of one field through the beginning of the next field.

COMPOSITE SYNC OUTPUT

The composite sync output, *Figure 2(b)*, is simply a reproduction of the signal waveform below the composite video black level, with the video completely removed. This is obtained by clamping the video signal sync tips to 1.5V DC at Pin 2 and using a comparator threshold set just above this voltage to strip the sync signal, which is then buffered out to Pin 1. The threshold separation from the clamped sync tip is nominally 70 mV which means that for the minimum input level of 0.5V (p-p), the clipping level is close to the halfway point on the sync pulse amplitude (shown by the dashed line on *Figure 2(a)*). This threshold separation is independent of the signal amplitude, therefore, for a 2V (p-p) input the clipping level occurs at 11% of the sync pulse amplitude. The charging current for the input coupling capacitor is 0.8 mA, whereas the discharge current is only 11 μA, typically. This allows relatively small capacitor values to be used—0.1 μF is generally recommended.

Normally the signal source for the LM1881 is assumed to be clean and relatively noise-free, but some sources may have excessive video peaking, causing high frequency video and chroma components to extend below the black level reference. Some video discs keep the chroma burst pulse present throughout the vertical blanking period so that the burst actually appears on the sync tips for three line periods instead of at black level. A clean composite sync signal can be generated from these sources by filtering the input signal. When the source impedance is low, typically 75Ω, a 620Ω resistor in series with the source and a 510 pF capacitor to ground will form a low pass filter with a corner frequency of 500 kHz. This bandwidth is more than sufficient to pass the sync pulse portion of the waveform; however, any subcarrier content in the signal will be attenuated by almost 18 dB, effectively taking it below the comparator threshold. Filtering will also help if the source is contaminated with thermal noise. The output waveforms will become delayed from between 40 ns to as much as 200 ns due to this filter. This much delay will not usually be significant but it does contribute to the sync delay produced by any additional signal processing. Since the original video may also undergo processing, the need for time delay correction will depend on the total system, not just the sync stripper.

VERTICAL SYNC OUTPUT

A vertical sync output is derived by internally integrating the composite sync waveform *(Figure 3)*. To understand the generation of the vertical sync pulse, refer to the lower left hand section *Figure 3*. Note that there are two comparators in the section. One comparator has an internally generated voltage reference called V_1 going to one of its inputs. The other comparator has an internally generated voltage referance called V_2 going to one of its inputs. Both comparators have a common input at their noninverting input coming from the internal integrator. The internal integrator is used for integrating the composite sync signal. This signal comes from the input side of the composite sync buffer and are **positive** going sync pulses. The capacitor to the integrator is internal to the LM1881. The capacitor charge current is set by the value of the external resistor R_{set}. The output of the integrator is going to be at a low voltage during the normal horizontal lines because the integrator has a very short time to charge the capacitor, which is during the horizontal sync period. The equalization pulses will keep the output voltage of the integrator at about the same level, below the V_1. During the vertical sync period the narrow going positive pulses shown in *Figure 2* is called the serration pulse. The wide negative portion of the vertical sync period is called the vertical sync pulse. At the start of the vertical sync period, before the first Serration pulse occurs, the integrator now charges the capacitor to a much higher voltage. At the first serration pulse the integrator output should be between V_1 and V_2. This would give a high level at the output of the comparator with V_1 as one of its inputs. This high is clocked into the "D" flip-flop by the falling edge of the serration pulse (remember the sync signal is inverted in this section of the LM1881). The "Q" output of the "D" flip-flop goes through the OR gate, and sets the R/S flip-flop. The output of the R/S flip-flop enables the internal oscillator and also clocks the ODD/EVEN "D" flip-flop. The ODD/EVEN field pulse operation is covered in the next section. The output of the oscillator goes to a divide by 8 circuit, thus resetting the R/S flip-flop after 8 cycles of the oscillator. The frequency of the oscillator is established by the internal capacitor going to the oscillator and the external R_{set}. The "$\overline{Q}$" output of the R/S flip-flop goes to pin 3 and is the actual vertical sync output of the LM1881. By clocking the "D" flip-flop at the start of the first serration pulse means that the vertical sync output pulse starts at this point in time and lasts for eight cycles of the internal oscillator as shown in *Figure 2*.

How R_{set} affects the integrator and the internal oscillator is shown under the Typical Performance Characteristics. The first graph is "R_{set} Value Selection vs Vertical Serration Pulse Separation". For this graph to be valid, the vertical sync pulse should last for at least 85% of the horizontal half line (47% of a full horizontal line). A vertical sync pulse from any standard should meet this requirement; both NTSC and PAL do meet this requirement (the serration pulse is the remainder of the period, 10% to 15% of the horizontal

Application Notes (Continued)

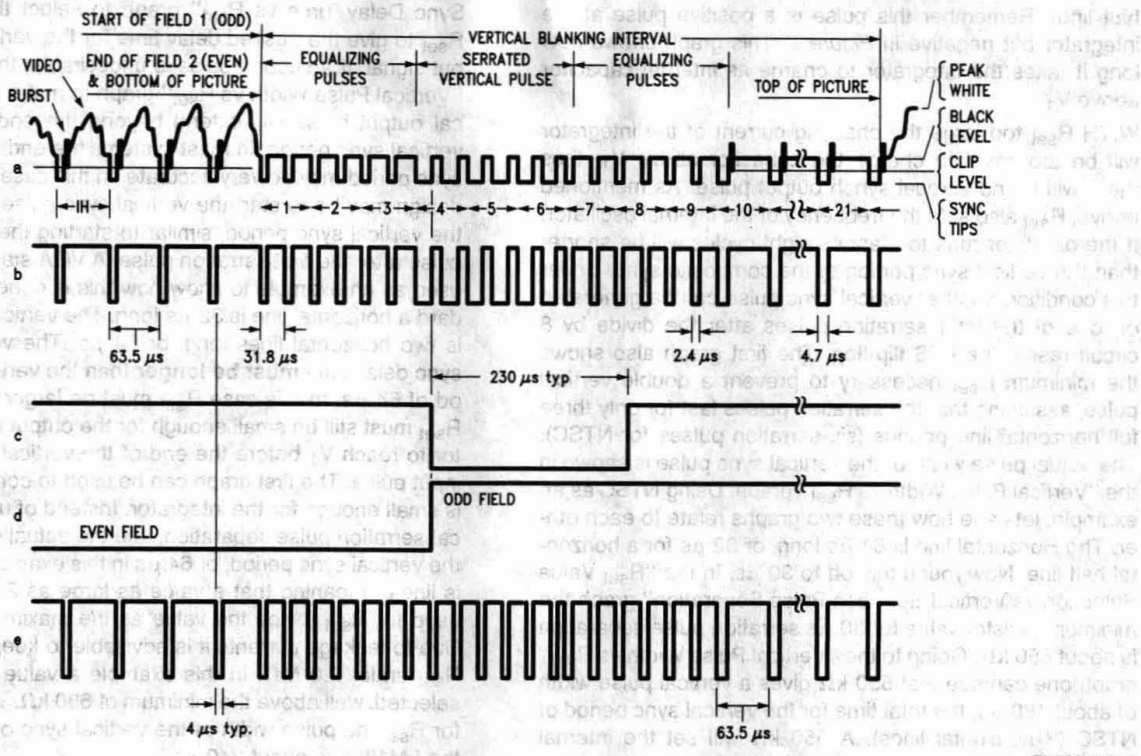

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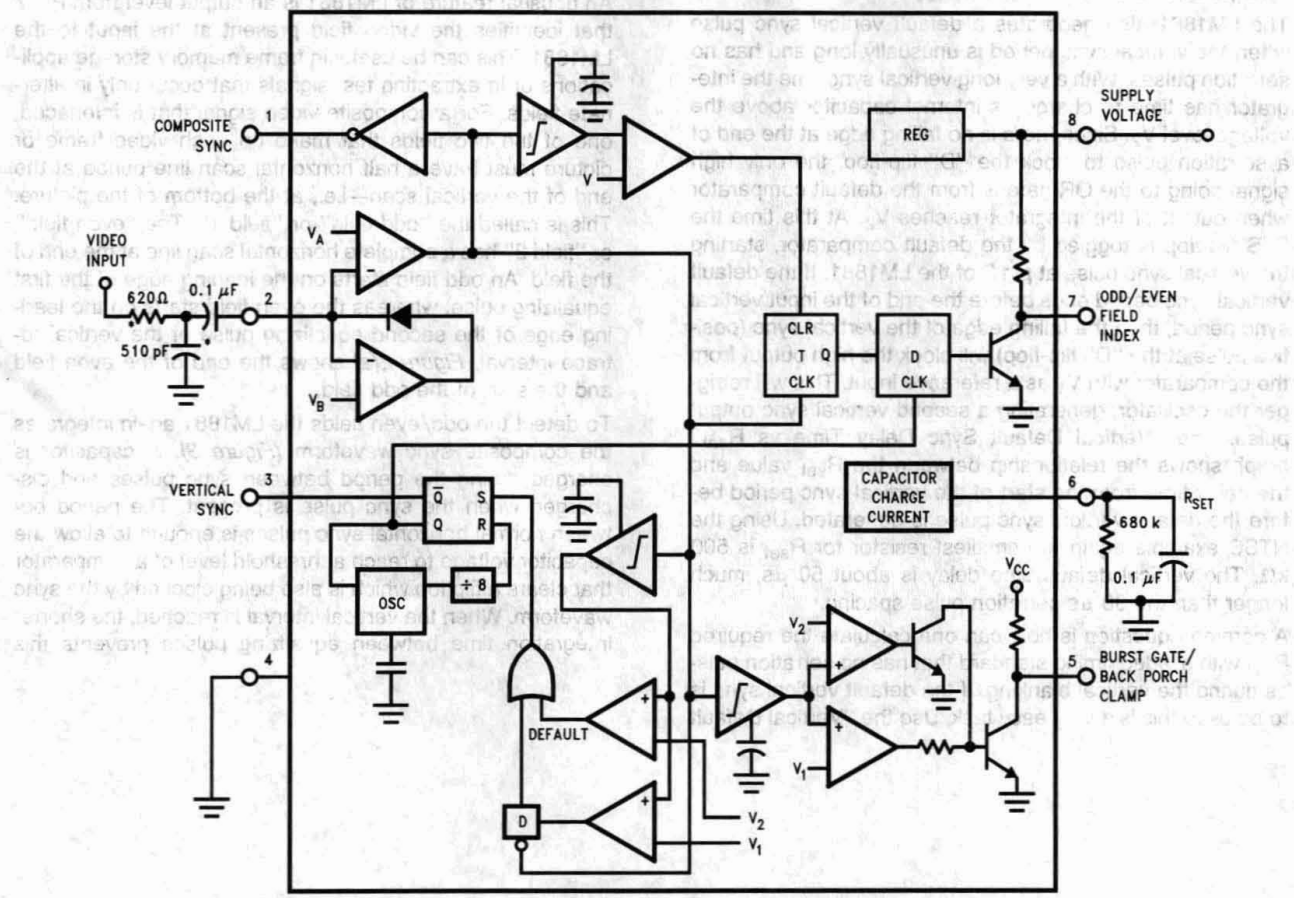
FIGURE 2. (a) Composite Video; (b) Composite Sync; (c) Vertical Output Pulse; (d) Odd/Even Field Index; (e) Burst Gate/Back Porch Clamp



*Components Optional, See Text

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FIGURE 3

Application Notes (Continued)

half line). Remember this pulse is a positive pulse at the integrator but negative in *Figure 2*. This graph shows how long it takes the integrator to charge its internal capacitor above V_1.

WITH R_{set} too large the charging current of the integrator will be too small to charge the capacitor above V_1, thus there will be no vertical synch output pulse. As mentioned above, R_{set} also sets the frequency of the internal oscillator. If the oscillator runs too fast its eight cycles will be shorter than the vertical sync portion of the composite sync. Under this condition another vertical sync pulse can be generated on one of the later serration pulses after the divide by 8 circuit resets the R/S flip-flop. The first graph also shows the minimum R_{set} necessary to prevent a double vertical pulse, assuming that the serration pulses last for only three full horizontal line periods (six serration pulses for NTSC). The actual pulse width of the vertical sync pulse is shown in the "Vertical Pulse Width vs R_{set}" graph. Using NTSC as an example, lets see how these two graphs relate to each other. The Horizontal line is 64 μs long, or 32 μs for a horizontal half line. Now round this off to 30 μs. In the "R_{set} Value Selection vs Vertical Serration Pulse Separation" graph the minimum resistor value for 30 μs serration pulse separation is about 550 kΩ. Going to the "Vertical Pulse Width vs R_{set}" graph one can see that 550 kΩ gives a vertical pulse width of about 180 μs, the total time for the vertical sync period of NTSC (3 horizontal lines). A 550 kΩ will set the internal oscillator to a frequency such that eight cycles gives a time of 180 μs, just long enough to prevent a double vertical sync pulse at the vertical sync output of the LM1881.

The LM1881 also generates a default vertical sync pulse when the vertical sync period is unusually long and has no serration pulses. With a very long vertical sync time the integrator has time to charge its internal capacitor above the voltage level V_2. Since there is no falling edge at the end of a serration pulse to clock the "D" flip-flop, the only high signal going to the OR gate is from the default comparator when output of the integrator reaches V_2. At this time the R/S flip-flop is toggled by the default comparator, starting the vertical sync pulse at pin 3 of the LM1881. If the default vertical sync period ends before the end of the input vertical sync period, then the falling edge of the vertical sync (positive pulse at the "D" flip-flop) will clock the high output from the comparator with V_1 as a reference input. This will retrigger the oscillator, generating a second vertical sync output pulse. The "Vertical Default Sync Delay Time vs R_{set}" graph shows the relationship between the R_{set} value and the delay time from the start of the vertical sync period before the default vertical sync pulse is generated. Using the NTSC example again the smallest resistor for R_{set} is 500 kΩ. The vertical default time delay is about 50 μs, much longer than the 30 μs serration pulse spacing.

A common question is how can one calculate the required R_{set} with a video timing standard that has no serration pulses during the vertical blanking. If the default vertical sync is to be used this is a very easy task. Use the "Vertical Default Sync Delay Time vs R_{set}" graph to select the necessary R_{set} to give the desired delay time for the vertical sync output signal. If a second pulse is undesirable, then check the "Vertical Pulse Width vs R_{set}" graph to make sure the vertical output pulse will extend beyond the end of the input vertical sync period. In most systems the end of the vertical sync period may be very accurate. In this case the preferred design may be to start the vertical sync pulse at the end of the vertical sync period, similar to starting the vertical sync pulse after the first serration pulse. A VGA standard is to be used as an example to show how this is done. In this standard a horizontal line is 32 μs long. The vertical sync period is two horizontal lines long, or 64 μs. The vertical default sync delay time **must be longer** than the vertical sync period of 64 μs. In this case R_{set} must be larger than 680 kΩ. R_{set} must still be small enough for the output of the integrator to reach V_1 before the end of the vertical period of the input pulse. The first graph can be used to confirm that R_{set} is small enough for the integrator. Instead of using the vertical serration pulse separation, use the actual pulse width of the vertical sync period, or 64 μs in this example. This graph is linear, meaning that a value as large as 2.7 MΩ can be used for R_{set} (twice the value as the maximum at 30 μs). Due to leakage currents it is advisable to keep the value of R_{set} under 2.0 MΩ. In this example a value of 1.0 MΩ is selected, well above the minimum of 680 kΩ. With this value for R_{set} the pulse width of the vertical sync output pulse of the LM1881 is about 340 μs.

ODD/EVEN FIELD PULSE

An unusual feature of LM1881 is an output level from Pin 7 that identifies the video field present at the input to the LM1881. This can be useful in frame memory storage applications or in extracting test signals that occur only in alternate fields. For a composite video signal that is interlaced, one of the two fields that make up each video frame or picture must have a half horizontal scan line period at the end of the vertical scan—i.e., at the bottom of the picture. This is called the "odd field" or "field 1". The "even field" or "field 2" has a complete horizontal scan line at the end of the field. An odd field starts on the leading edge of the first equalizing pulse, whereas the even field starts on the leading edge of the second equalizing pulse of the vertical retrace interval. *Figure 2(a)* shows the end of the even field and the start of the odd field.

To detect the odd/even fields the LM1881 again integrates the composite sync waveform *(Figure 3)*. A capacitor is charged during the period between sync pulses and discharged when the sync pulse is present. The period between normal horizontal sync pulses is enough to allow the capacitor voltage to reach a threshold level of a comparator that clears a flipflop which is also being clocked by the sync waveform. When the vertical interval is reached, the shorter integration time between equalizing pulses prevents this

Application Notes (Continued)

threshold from being reached and the Q output of the flip-flop is toggled with each equalizing pulse. Since the half line period at the end of the odd field will have the same effect as an equalizing pulse period, the Q output will have a different polarity on successive fields. Thus by comparing the Q polarity with the vertical output pulse, an odd/even field index is generated. Pin 7 remains low during the even field and high during the odd field.

BURST/BACKPORCH OUTPUT PULSE

In a composite video signal, the chroma burst is located on the backporch of the horizontal blanking period. This period, approximately 4.8 μs long, is also the black level reference for the subsequent video scan line. The LM1881 generates a pulse at Pin 5 that can be used either to retrieve the chroma burst from the composite video signal (thus providing a subcarrier synchronizing signal) or as a clamp for the DC restoration of the video waveform. This output is obtained simply by charging an internal capacitor starting on the trailing edge of the horizontal sync pulses. Simultaneously the output of Pin 5 is pulled low and held until the capacitor charge circuit times out—4 μs later. A shorter output burst gate pulse can be derived by differentiating the burst output using a series C-R network. This may be necessary in applications which require high horizontal scan rates in combination with normal (60–120 Hz) vertical scan rates.

APPLICATIONS

Apart from extracting a composite sync signal free of video information, the LM1881 outputs allow a number of interesting applications to be developed. As mentioned above, the burst gate/backporch clamp pulse allows DC restoration of the original video waveform for display or remodulation on an R.F. carrier, and retrieval of the color burst for color synchronization and decoding into R.G.B. components. For frame memory storage applications, the odd/even field level allows identification of the appropriate field ensuring the correct read or write sequence. The vertical pulse output is particularly useful since it begins at a precise time—the rising edge of the first vertical serration in the sync waveform. This means that individual lines within the vertical blanking period (or anywhere in the active scan line period) can easily be extracted by counting the required number of transitions in the composite sync waveform following the start of the vertical output pulse.

The vertical blanking interval is proving popular as a means to transmit data which will not appear on a normal T.V. receiver screen. Data can be inserted beginning with line 10 (the first horizontal scan line on which the color burst appears) through to line 21. Usually lines 10 through 13 are not used which leaves lines 14 through 21 for inserting signals, which may be different from field to field. In the U.S., line 19 is normally reserved for a vertical interval reference signal (VIRS) and line 21 is reserved for closed caption data for the hearing impaired. The remaining lines are used in a number of ways. Lines 17 and 18 are frequently used during studio processing to add and delete vertical interval test signals (VITS) while lines 14 through 18 and line 20 can be used for Videotex/Teletext data. Several institutions are proposing to transmit financial data on line 17 and cable systems use the available lines in the vertical interval to send decoding data for descrambler terminals.

Since the vertical output pulse from the LM1881 coincides with the leading edge of the first vertical serration, sixteen positive or negative transitions later will be the start of line 14 in either field. At this point simple counters can be used to select the desired line(s) for insertion or deletion of data.

VIDEO LINE SELECTOR

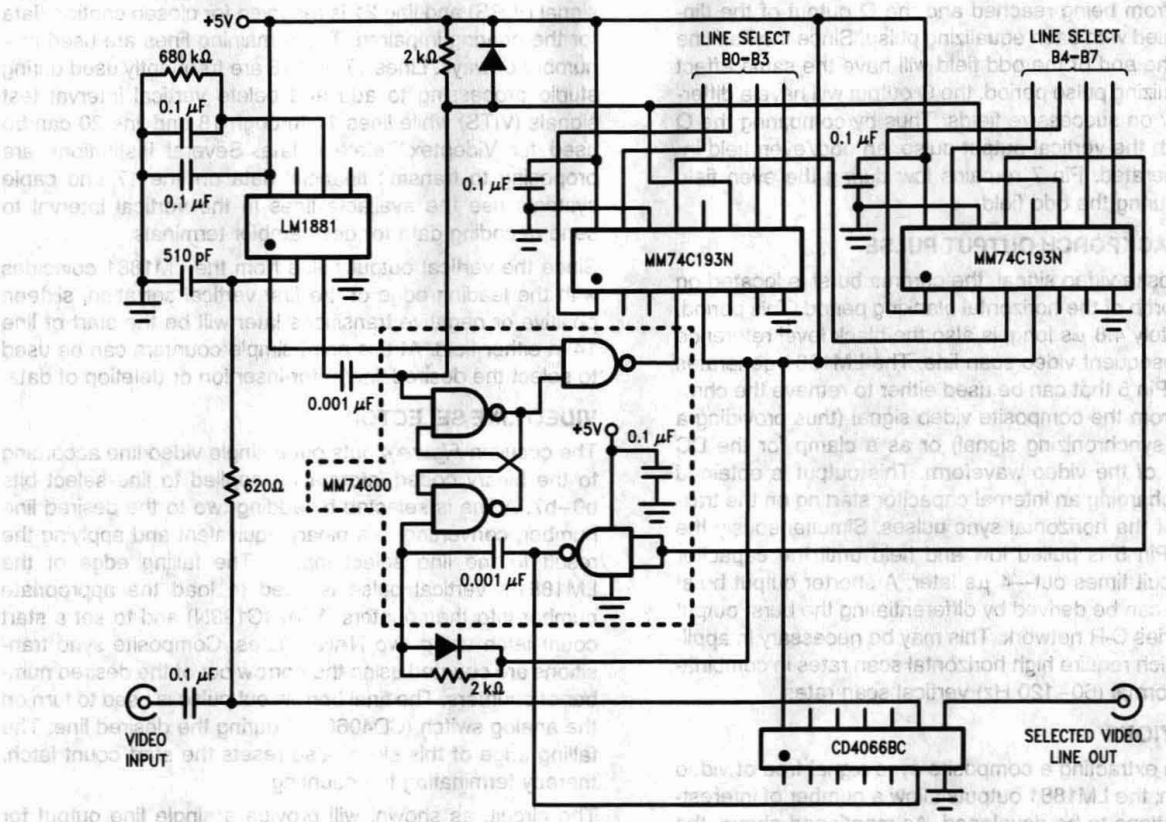
The circuit in *Figure 4* puts out a single video line according to the binary coded information applied to line select bits b0–b7. A line is selected by adding two to the desired line number, converting to a binary equivalent and applying the result to the line select inputs. The falling edge of the LM1881's vertical pulse is used to load the appropriate number into the counters (MM74C193N) and to set a start count latch using two NAND gates. Composite sync transitions are counted using the borrow out of the desired number of counters. The final borrow out pulse is used to turn on the analog switch (CD4066BC) during the desired line. The falling edge of this signal also resets the start count latch, thereby terminating the counting.

The circuit, as shown, will provide a single line output for each field in an interlaced video system (television) or a single line output in each frame for a non-interlaced video system (computer monitor). When a particular line in only one field of an interlaced video signal is desired, the odd/even field index output must be used instead of the vertical output pulse (invert the field index output to select the odd field). A single counter is needed for selecting lines 3 to 14; two counters are needed for selecting lines 15 to 253; and three counters will work for up to 2046 lines. An output buffer is required to drive low impedance loads.

MULTIPLE CONTIGUOUS VIDEO LINE SELECTOR WITH BLACK LEVEL RESTORATION

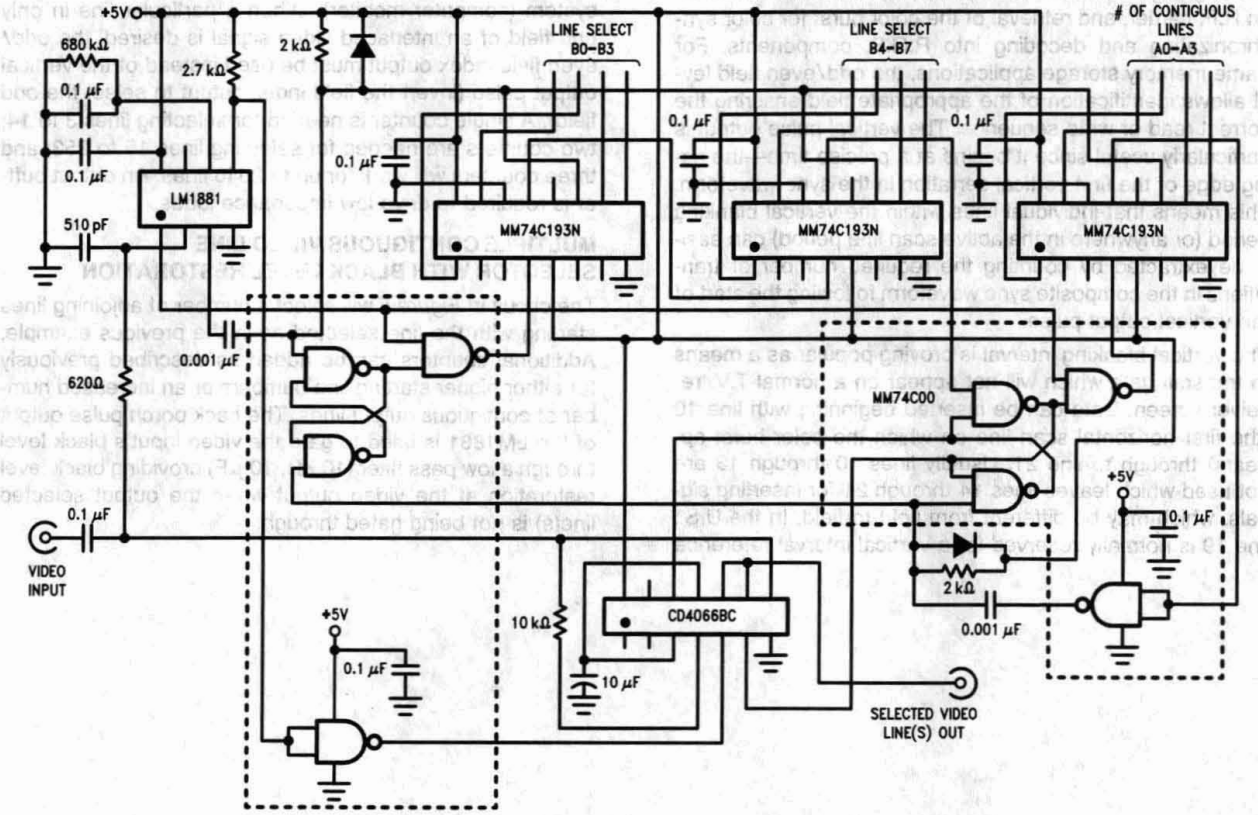
The circuit in *Figure 5* will select a number of adjoining lines starting with the line selected as in the previous example. Additional counters can be added as described previously for either higher starting line numbers or an increased number of contiguous output lines. The back porch pulse output of the LM1881 is used to gate the video input's black level through a low pass filter (10 kΩ, 10 μF) providing black level restoration at the video output when the output selected line(s) is not being gated through.

Typical Applications



TL/H/9150–5

FIGURE 4. Video Line Selector



TL/H/9150–6

FIGURE 5. Multiple Contiguous Video Line Selector With Black Level Restoration

National Semiconductor

LM1882•54ACT/74ACT715
LM1882-R•54ACT/74ACT715-R
Programmable Video Sync Generator

General Description

The 'ACT715/LM1882 and 'ACT715-R/LM1882-R are 20-pin TTL-input compatible devices capable of generating Horizontal, Vertical and Composite Sync and Blank signals for televisions and monitors. All pulse widths are completely definable by the user. The devices are capable of generating signals for both interlaced and noninterlaced modes of operation. Equalization and serration pulses can be introduced into the Composite Sync signal when needed.

Four additional signals can also be made available when Composite Sync or Blank are used. These signals can be used to generate horizontal or vertical gating pulses, cursor position or vertical Interrupt signal.

These devices make no assumptions concerning the system architecture. Line rate and field/frame rate are all a function of the values programmed into the data registers, the status register, and the input clock frequency.

The 'ACT715/LM1882 is mask programmed to default to a Clock Disable state. Bit 10 of the Status Register, Register 0, defaults to a logic "0". This facilitates (re)programming before operation.

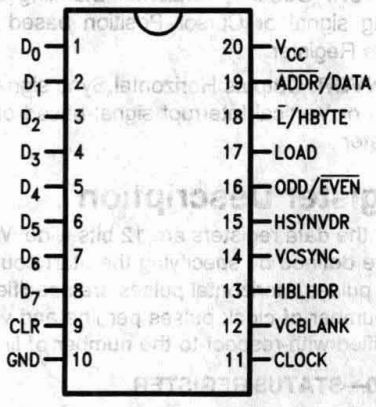
The 'ACT715-R/LM1882-R is the same as the 'ACT715/LM1882 in all respects except that the 'ACT715-R/LM1882-R is mask programmed to default to a Clock Enabled state. Bit 10 of the Status Register defaults to a logic "1". Although completely (re)programmable, the 'ACT715-R/LM1882-R version is better suited for applications using the default 14.31818 MHz RS-170 register values. This feature allows power-up directly into operation, following a single CLEAR pulse.

Features

- Maximum Input Clock Frequency > 130 MHz
- Interlaced and non-interlaced formats available
- Separate or composite horizontal and vertical Sync and Blank signals available
- Complete control of pulse width via register programming
- All inputs are TTL compatible
- 8 mA drive on all outputs
- Default RS170/NTSC values mask programmed into registers
- 4 KV minimum ESD immunity
- 'ACT715-R/LM1882-R is mask programmed to default to a Clock Enable state for easier start-up into 14.31818 MHz RS170 timing

Connection Diagrams

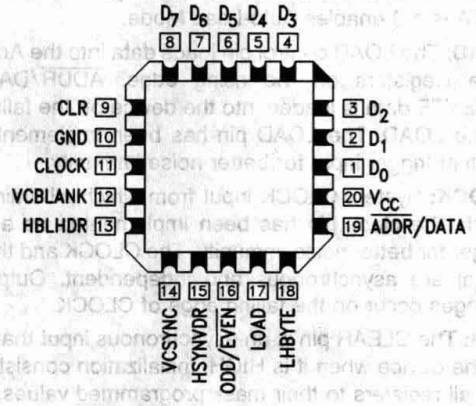
Pin Assignment for DIP and SOIC



TL/F/10137–1

Order Number LM1882CN or LM1882CM
For Default RS-170, Order Number LM1882-RCN or LM1882-RCM

Pin Assignment for LCC



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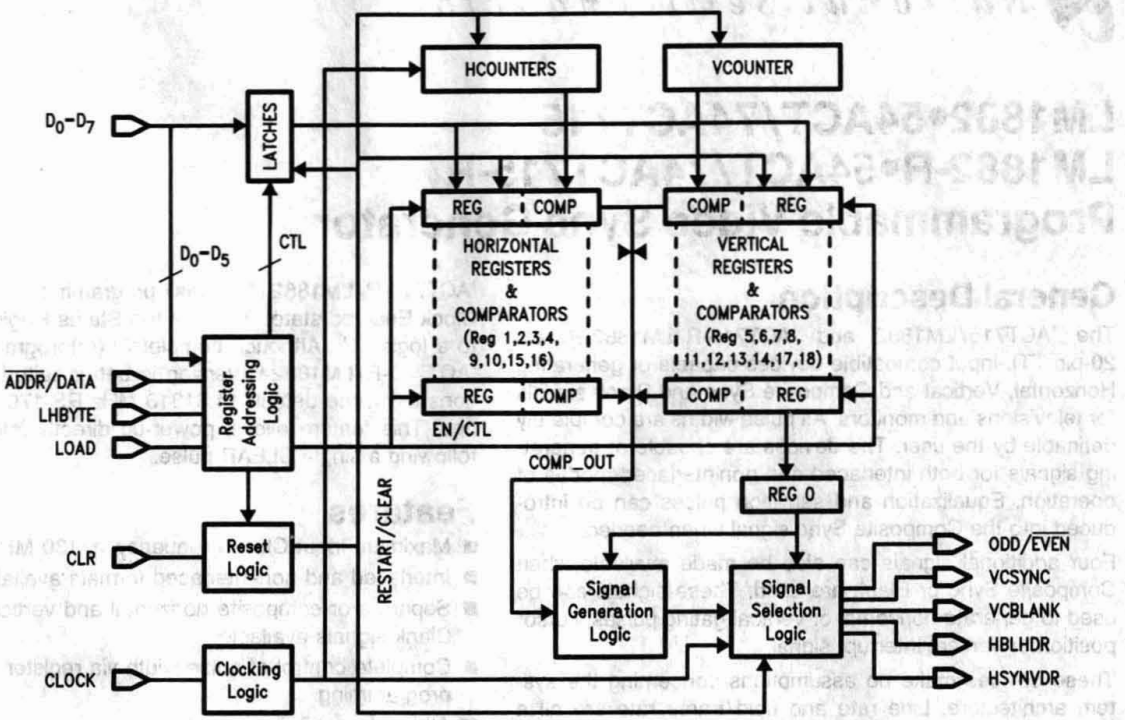
2

Logic Block Diagram



TL/F/10137–3

Pin Description

There are a Total of 13 inputs and 5 outputs on the 'ACT715/LM1882.

Data Inputs D0–D7: The Data Input pins connect to the Address Register and the Data Input Register.

ADDR/DATA: The ADDR/DATA signal is latched into the device on the falling edge of the LOAD signal. The signal determines if an address (0) or data (1) is present on the data bus.

L/HBYTE: The L/HBYTE signal is latched into the device on the falling edge of the LOAD signal. The signal determines if data will be read into the 8 LSB's (0) or the 4 MSB's (1) of the Data Registers. A 1 on this pin when an ADDR/DATA is a 0 enables Auto-Load Mode.

LOAD: The LOAD control pin loads data into the Address or Data Registers on the rising edge. ADDR/DATA and L/HBYTE data is loaded into the device on the falling edge of the LOAD. The LOAD pin has been implemented as a Schmitt trigger input for better noise immunity.

CLOCK: System CLOCK input from which all timing is derived. The clock pin has been implemented as a Schmitt trigger for better noise immunity. The CLOCK and the LOAD signal are asynchronous and independent. Output state changes occur on the falling edge of CLOCK.

CLR: The CLEAR pin is an asynchronous input that initializes the device when it is HIGH. Initialization consists of setting all registers to their mask programmed values, and initializing all counters, comparators and registers. The CLEAR pin has been implemented as a Schmitt trigger for better noise immunity. A CLEAR pulse should be asserted by the user immediately after power-up to ensure proper initialization of the registers—even if the user plans to (re)program the device.

Note: A CLEAR pulse will disable the CLOCK on the 'ACT715/LM1882 and will enable the CLOCK on the 'ACT715-R/LM1882-R.

ODD/EVEN: Output that identifies if display is in odd (HIGH) or even (LOW) field of interlace when device is in interlaced mode of operation. In noninterlaced mode of operation this output is always HIGH. Data can be serially scanned out on this pin during Scan Mode.

VCSYNC: Outputs Vertical or Composite Sync signal based on value of the Status Register. Equalization and Serration pulses will (if enabled) be output on the VCSYNC signal in composite mode only.

VCBLANK: Outputs Vertical or Composite Blanking signal based on value of the Status Register.

HBLHDR: Outputs Horizontal Blanking signal, Horizontal Gating signal or Cursor Position based on value of the Status Register.

HSYNVDR: Outputs Horizontal Sync signal, Vertical Gating signal or Vertical Interrupt signal based on value of Status Register.

Register Description

All of the data registers are 12 bits wide. Width's of all pulses are defined by specifying the start count and end count of all pulses. Horizontal pulses are specified with-respect-to the number of clock pulses per line and vertical pulses are specified with-respect-to the number of lines per frame.

REG0—STATUS REGISTER

The Status Register controls the mode of operation, the signals that are output and the polarity of these outputs. The default value for the Status Register is 0 (000 Hex) for the 'ACT715/LM1882 and is "512" (200 Hex) for the 'ACT715-R/LM1882-R.

Register Description (Continued)

Bits 0–2

B_2	B_1	B_0	VCBLANK	VCSYNC	HBLHDR	HSYNVDR
0	0	0 (DEFAULT)	CBLANK	CSYNC	HGATE	VGATE
0	0	1	VBLANK	CSYNC	HBLANK	VGATE
0	1	0	CBLANK	VSYNC	HGATE	HSYNC
0	1	1	VBLANK	VSYNC	HBLANK	HSYNC
1	0	0	CBLANK	CSYNC	CURSOR	VINT
1	0	1	VBLANK	CSYNC	HBLANK	VINT
1	1	0	CBLANK	VSYNC	CURSOR	HSYNC
1	1	1	VBLANK	VSYNC	HBLANK	HSYNC

Bits 3–4

B_4	B_3	Mode of Operation
0 (DEFAULT)	0	Interlaced Double Serration and Equalization
0	1	Non Interlaced Double Serration
1	0	Illegal State
1	1	Non Interlaced Single Serration and Equalization

Double Equalization and Serration mode will output equalization and serration pulses at twice the HSYNC frequency (i.e., 2 equalization or serration pulses for every HSYNC pulse). Single Equalization and Serration mode will output an equalization or serration pulse for every HSYNC pulse. In Interlaced mode equalization and serration pulses will be output during the VBLANK period of every odd and even field. Interlaced Single Equalization and Serration mode is not possible with this part.

Bits 5–8

Bits 5 through 8 control the polarity of the outputs. A value of zero in these bit locations indicates an output pulse active LOW. A value of 1 indicates an active HIGH pulse.

B5— VCBLANK Polarity

B6— VCSYNC Polarity

B7— HBLHDR Polarity

B8— HSYNVDR Polarity

Bits 9–11

Bits 9 through 11 enable several different features of the device.

B9— Enable Equalization/Serration Pulses (0)
Disable Equalization/Serration Pulses (1)

B10— Disable System Clock (0)
Enable System Clock (1)

Default values for B10 are "0" in the 'ACT715/LM1882 and "1" in the 'ACT715-R/LM1882-R.

B11— Disable Counter Test Mode (0)
Enable Counter Test Mode (1)

This bit is not intended for the user but is for internal testing only.

HORIZONTAL INTERVAL REGISTERS

The Horizontal Interval Registers determine the number of clock cycles per line and the characteristics of the Horizontal Sync and Blank pulses.

REG1— Horizontal Front Porch

REG2— Horizontal Sync Pulse End Time

REG3— Horizontal Blanking Width

REG4— Horizontal Interval Width # of Clocks per Line

VERTICAL INTERVAL REGISTERS

The Vertical Interval Registers determine the number of lines per frame, and the characteristics of the Vertical Blank and Sync Pulses.

REG5— Vertical Front Porch

REG6— Vertical Sync Pulse End Time

REG7— Vertical Blanking Width

REG8— Vertical Interval Width # of Lines per Frame

EQUALIZATION AND SERRATION PULSE SPECIFICATION REGISTERS

These registers determine the width of equalization and serration pulses and the vertical interval over which they occur.

REG 9— Equalization Pulse Width End Time

REG10— Serration Pulse Width End Time

REG11— Equalization/Serration Pulse Vertical Interval Start Time

REG12— Equalization/Serration Pulse Vertical Interval End Time

VERTICAL INTERRUPT SPECIFICATION REGISTERS

These Registers determine the width of the Vertical Interrupt signal if used.

REG13— Vertical Interrupt Activate Time

REG14— Vertical Interrupt Deactivate Time

CURSOR LOCATION REGISTERS

These 4 registers determine the cursor position location, or they generate separate Horizontal and Vertical Gating signals.

REG15— Horizontal Cursor Position Start Time

REG16— Horizontal Cursor Position End Time

REG17— Vertical Cursor Position Start Time

REG18— Vertical Cursor Position End Time

Signal Specification

HORIZONTAL SYNC AND BLANK SPECIFICATIONS

All horizontal signals are defined by a start and end time. The start and end times are specified in number of clock cycles per line. The start of the horizontal line is considered pulse 1 not 0. All values of the horizontal timing registers are referenced to the falling edge of the Horizontal Blank signal (see *Figure 1*). Since the first CLOCK edge, CLOCK #1, causes the first falling edge of the Horizontal Blank reference pulse, edges referenced to this first Horizontal edge are n + 1 CLOCKs away, where "n" is the width of the timing in question. Registers 1, 2, and 3 are programmed in this manner. The horizontal counters start at 1 and count until HMAX. The value of HMAX must be divisible by 2. This

2

Signal Specification (Continued)

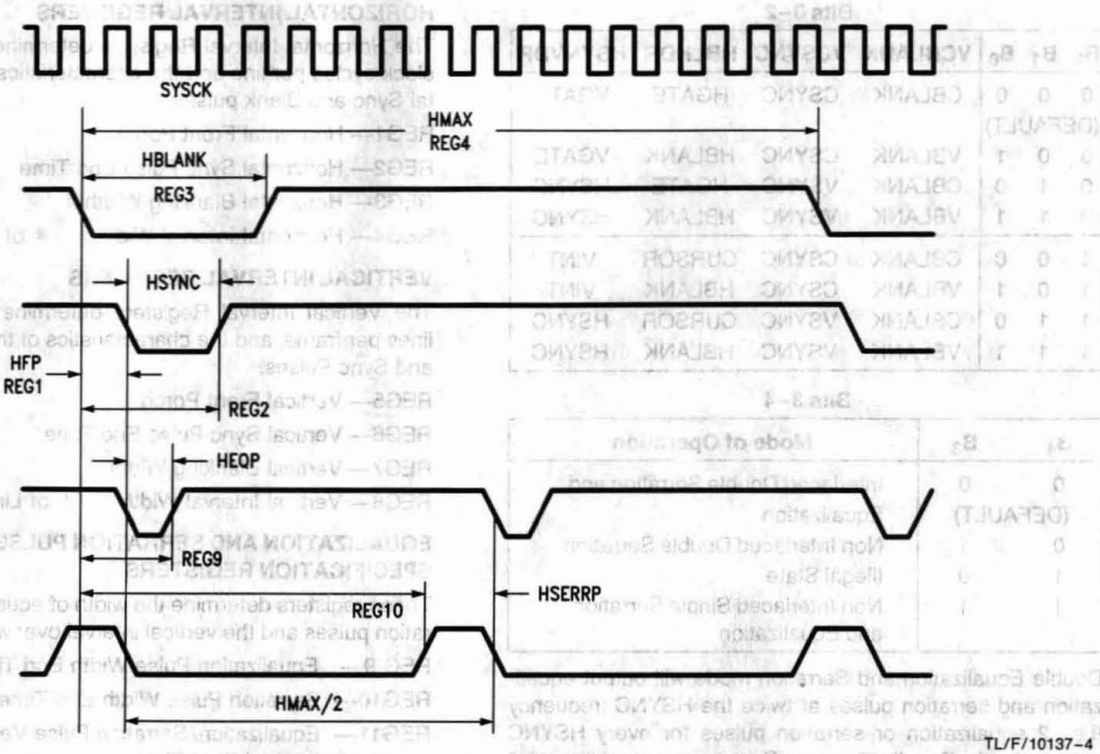


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FIGURE 1. Horizontal Waveform Specification

limitation is imposed because during interlace operation this value is internally divided by 2 in order to generate serration and equalization pulses at 2 × the horizontal frequency. Horizontal signals will change on the falling edge of the CLOCK signal. Signal specifications are shown below.

Horizontal Period (HPER) = REG(4) × ckper

Horizontal Blanking Width = [REG(3) − 1] × ckper

Horizontal Sync Width = [REG(2) − REG(1)] × ckper

Horizontal Front Porch = [REG(1) − 1] × ckper

VERTICAL SYNC AND BLANK SPECIFICATION

All vertical signals are defined in terms of number of lines per frame. This is true in both interlaced and noninterlaced modes of operation. Care must be taken to not specify the Vertical Registers in terms of lines per field. Since the first CLOCK edge, CLOCK #1, causes the first falling edge of the Vertical Blank (first Horizontal Blank) reference pulse, edges referenced to this first edge are n + 1 lines away, where "n" is the width of the timing in question. Registers 5, 6, and 7 are programmed in this manner. Also, in the interlaced mode, vertical timing is based on half-lines. Therefore registers 5, 6, and 7 must contain a value twice the total horizontal (odd and even) plus 1 (as described above). In non-interlaced mode, all vertical timing is based on whole-lines. Register 8 is always based on whole-lines and does not add 1 for the first clock. The vertical counter starts at the value of 1 and counts until the value of VMAX. No restrictions exist on the values placed in the vertical registers. Vertical Blank will change on the leading edge of HBLANK. Vertical Sync will change on the leading edge of HSYNC. (See *Figure 2A*.)

Vertical Frame Period (VPER) = REG(8) × hper

Vertical Field Period (VPER/n) = REG(8) × hper/n

Vertical Blanking Width = [REG(7) − 1] × hper/n

Vertical Syncing Width = [REG(6) − REG(5)] × hper/n

Vertical Front Porch = [REG(5) − 1] × hper/n

where n = 1 for noninterlaced
n = 2 for interlaced

COMPOSITE SYNC AND BLANK SPECIFICATION

Composite Sync and Blank signals are created by logically ANDing (ORing) the active LOW (HIGH) signals of the corresponding vertical and horizontal components of these signals. The Composite Sync signal may also include serration and/or equalization pulses. The Serration pulse interval occurs in place of the Vertical Sync interval. Equalization pulses occur preceding and/or following the Serration pulses. The width and location of these pulses can be programmed through the registers shown below. (See *Figure 2B*.)

Horizontal Equalization PW = [REG(9) − REG(1)] × ckper
REG 9 = (HFP) + (HEQP) + 1

Horizontal Serration PW = [REG(4)/n + REG(1) − REG(10)] × ckper
REG 10 = (HFP) + (HPER/2) − (HSERR) + 1

Where n = 1 for noninterlaced single serration/equalization
n = 2 for noninterlaced double serration/equalization
n = 2 for interlaced operation

Signal Specification (Continued)

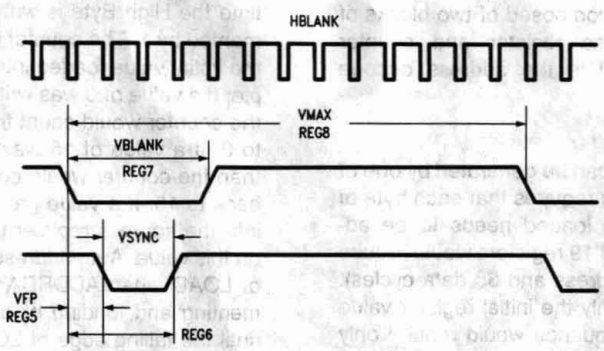

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FIGURE 2A. Vertical Waveform Specification

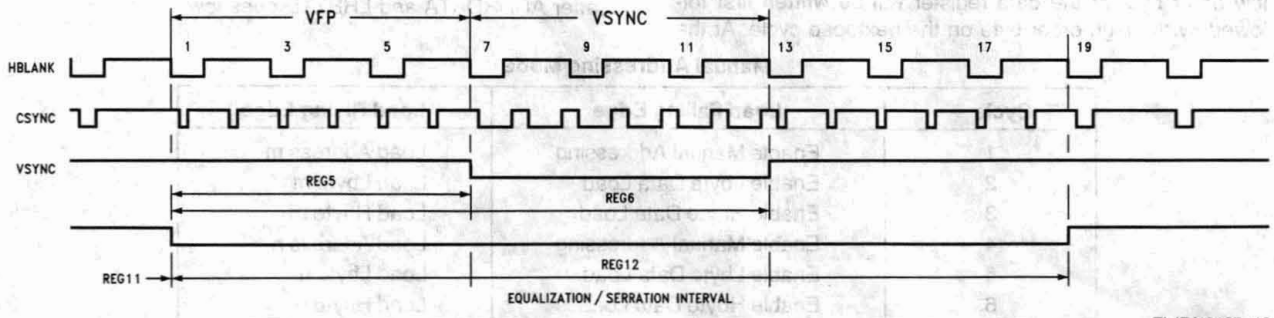

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FIGURE 2B. Equalization/Serration Interval Programming

HORIZONTAL AND VERTICAL GATING SIGNALS

Horizontal Drive and Vertical Drive outputs can be utilized as general purpose Gating Signals. Horizontal and Vertical Gating Signals are available for use when Composite Sync and Blank signals are selected and the value of Bit 2 of the Status Register is 0. The Vertical Gating signal will change in the same manner as that specified for the Vertical Blank.

Horizontal Gating Signal Width = [REG(16) − REG(15)] × ckper

Vertical Gating Signal Width = [REG(18) − REG(17)] × hper

CURSOR POSITION AND VERTICAL INTERRUPT

The Cursor Position and Vertical Interrupt signal are available when Composite Sync and Blank signals are selected and Bit 2 of the Status Register is set to the value of 1. The Cursor Position generates a single pulse of n clocks wide during every line that the cursor is specified. The signals are generated by logically ORing (ANDing) the active LOW (HIGH) signals specified by the registers used for generating Horizontal and Vertical Gating signals. The Vertical Interrupt signal generates a pulse during the vertical interval specified. The Vertical Interrupt signal will change in the same manner as that specified for the Vertical Blanking signal.

Horizontal Cursor Width = [REG(16) − REG(15)] × ckper

Vertical Cursor Width = [REG(18) − REG(17)] × hper

Vertical Interrupt Width = [REG(14) − REG(13)] × hper

Addressing Logic

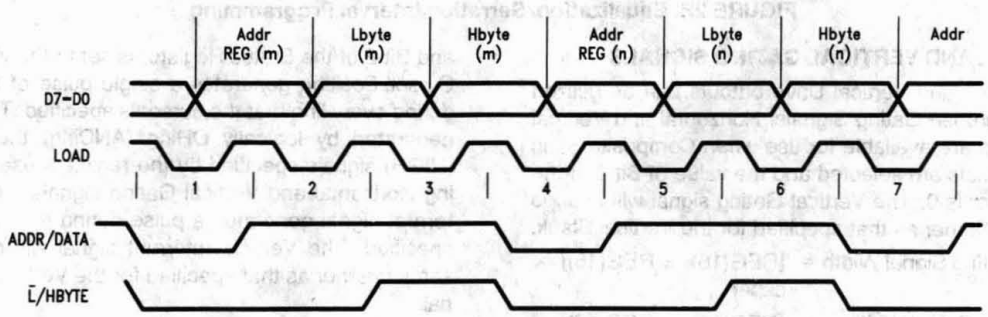
The register addressing logic is composed of two blocks of logic. The first is the address register and counter (ADDRCNTR), and the second is the address decode (ADDRDEC).

ADDRCNTR LOGIC

Addresses for the data registers can be generated by one of two methods. Manual addressing requires that each byte of each register that needs to be loaded needs to be addressed. To load both bytes of all 19 registers would require a total of 57 load cycles (19 address and 38 data cycles). Auto Addressing requires that only the initial register value be specified. The Auto Load sequence would require only 39 load cycles to completely program all registers (1 address and 38 data cycles). In the auto load sequence the low order byte of the data register will be written first followed by the high order byte on the next load cycle. At the time the High Byte is written the address counter is incremented by 1. The counter has been implemented to loop on the initial value loaded into the address register. For example: If a value of 0 was written into the address register then the counter would count from 0 to 18 before resetting back to 0. If a value of 15 was written into the address register then the counter would count from 15 to 18 before looping back to 15. If a value greater than or equal to 18 is placed into the address register the counter will continuously loop on this value. Auto addressing is initiated on the falling edge of LOAD when ADDRDATA is 0 and LHBYTE is 1. Incrementing and loading of data registers will not commence until the falling edge of LOAD after ADDRDATA goes to 1. The next rising edge of LOAD will load the first byte of data. Auto Incrementing is disabled on the falling edge of LOAD after ADDRDATA and LHBYTE goes low.

Manual Addressing Mode

Cycle #	Load Falling Edge	Load Rising Edge
1	Enable Manual Addressing	Load Address m
2	Enable Lbyte Data Load	Load Lbyte m
3	Enable Hbyte Data Load	Load Hbyte m
4	Enable Manual Addressing	Load Address n
5	Enable Lbyte Data Load	Load Lbyte n
6	Enable Hbyte Data Load	Load Hbyte n



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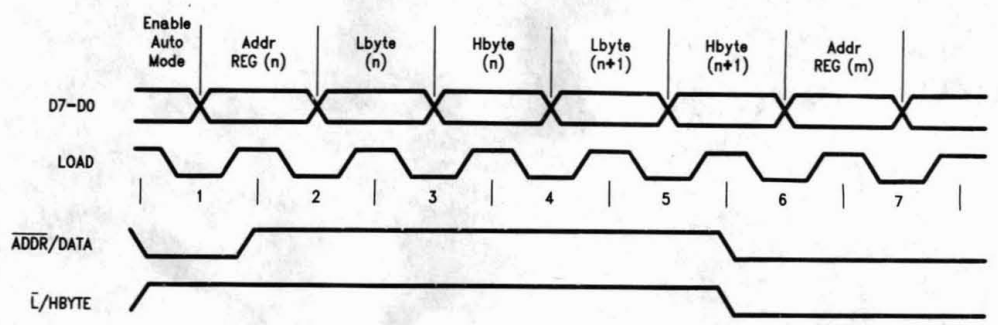
Auto Addressing Mode

Cycle #	Load Falling Edge	Load Rising Edge
1	Enable Auto Addressing	Load Start Address n
2	Enable Lbyte Data Load	Load Lbyte (n)
3	Enable Hbyte Data Load	Load Hbyte (n); Inc Counter
4	Enable Lbyte Data Load	Load Lbyte (n + 1)
5	Enable Hbyte Data Load	Load Hbyte (n + 1); Inc Counter
6	Enable Manual Addressing	Load Address



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Addressing Logic (Continued)

ADDRDEC LOGIC

The ADDRDEC logic decodes the current address and generates the enable signal for the appropriate register. The enable values for the registers and counters change on the falling edge of LOAD. Two types of ADDRDEC logic is enabled by 2 pair of addresses, Addresses 22 or 54 (Vectored Restart logic) and Addresses 23 or 55 (Vectored Clear logic). Loading these addresses will enable the appropriate logic and put the part into either a Restart (all counter registers are reinitialized with preprogrammed data) or Clear (all registers are cleared to zero) state. Reloading the same ADDRDEC address will not cause any change in the state of the part. The outputs during these states are frozen and the internal CLOCK is disabled. Clocking the part during a Vectored Restart or Vectored Clear state will have no effect on the part. To resume operation in the new state, or disable the Vectored Restart or Vectored Clear state, another non-ADDRDEC address must be loaded. Operation will begin in the new state on the rising edge of the non-ADDRDEC load pulse. It is recommended that an unused address be loaded following an ADDRDEC operation to prevent data registers from accidentally being corrupted. The following Addresses are used by the device.

Address 0	Status Register REG0
Address 1–18	Data Registers REG1–REG18
Address 19–21	Unused
Address 22/54	Restart Vector (Restarts Device)
Address 23/55	Clear Vector (Zeros All Registers)
Address 24–31	Unused
Address 32–50	Register Scan Addresses
Address 51–53	Counter Scan Addresses
Address 56–63	Unused

At any given time only one register at most is selected. It is possible to have no registers selected.

VECTORED RESTART ADDRESS

The function of addresses 22 (16H) or 54 (36H) are similar to that of the CLR pin except that the preprogramming of the registers is not affected. It is recommended but not required that this address is read after the initial device configuration load sequence. A 1 on the ADDRDATA pin (Auto Addressing Mode) will not cause this address to automatically increment. The address will loop back onto itself regardless of the state of ADDRDATA unless the address on the Data inputs has been changed with ADDRDATA at 0.

VECTORED CLEAR ADDRESS

Addresses 23 (17H) or 55 (37H) is used to clear all registers to zero simultaneously. This function may be desirable to use prior to loading new data into the Data or Status Registers. This address is read into the device in a similar fashion as all of the other registers. A 1 on the ADDRDATA pin (Auto Addressing Mode) will not cause this address to automatically increment. The address will loop back onto itself regardless of the state of ADDRDATA unless the address on the Data inputs has been changed with ADDRDATA at 0.

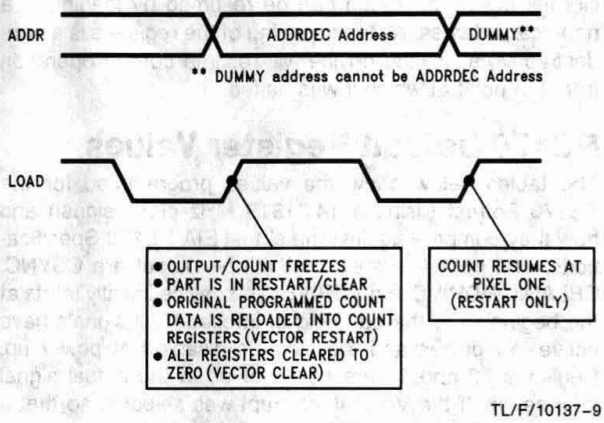
ADDR
ADDRDEC Address
DUMMY**
** DUMMY address cannot be ADDRDEC Address
LOAD
• OUTPUT/COUNT FREEZES
• PART IS IN RESTART/CLEAR
• ORIGINAL PROGRAMMED COUNT DATA IS RELOADED INTO COUNT REGISTERS (VECTOR RESTART)
• ALL REGISTERS CLEARED TO ZERO (VECTOR CLEAR)
COUNT RESUMES AT PIXEL ONE (RESTART ONLY)
TL/F/10137–9

FIGURE 3. ADDRDEC Timing

GEN LOCKING

The 'ACT715/LM1882 and 'ACT715-R/LM1882-R is designed for master SYNC and BLANK signal generation. However, the devices can be synchronized (slaved) to an external timing signal in a limited sense. Using Vectored Restart, the user can reset the counting sequence to a given location, the beginning, at a given time, the rising edge of the LOAD that removes Vector Restart. At this time the next CLOCK pulse will be CLOCK 1 and the count will restart at the beginning of the first odd line.

Preconditioning the part during normal operation, before the desired synchronizing pulse, is necesasry. However, since LOAD and CLOCK are asynchronous and independent, this is possible without interruption or data and performance corruption. If the defaulted 14.31818 MHz RS-170 values are being used, preconditioning and restarting can be minimized by using the CLEAR pulse instead of the Vectored Restart operation. The 'ACT715-R/LM1882-R is better suited for this application because it eliminates the need to program a 1 into Bit 10 of the Status Register to enable the CLOCK. Gen Locking to another count location other than the very beginning or separate horizontal/vertical resetting is not possible with the 'ACT715/LM1882 nor the 'ACT715-R/LM1882-R.

SCAN MODE LOGIC

A scan mode is available in the ACT715/LM1882 that allows the user to non-destructively verify the contents of the registers. Scan mode is invoked through reading a scan address into the address register. The scan address of a given register is defined by the Data register address + 32. The internal Clocking signal is disabled when a scan address is read. Disabling the clock freezes the device in it's present state. Data can then be serially scanned out of the data registers through the ODD/EVEN Pin. The LSB will be scanned out first. Since each register is 12 bits wide, completely scanning out data of the addressed register will require 12 CLOCK pulses. More than 12 CLOCK pulses on the same register will only cause the MSB to repeat on the output. Re-scanning the same register will require that register to be reloaded. The value of the two horizontal counters and 1 vertical counter can also be scanned out by using address numbers 51–53. Note that before the part will scan out the data, the LOAD signal must be brought back HIGH.

Addressing Logic (Continued)

Normal device operation can be resumed by loading in a non-scan address. As the scanning of the registers is a non-destructive scan, the device will resume correct operation from the point at which it was halted.

RS170 Default Register Values

The tables below show the values programmed for the RS170 Format (using a 14.31818 MHz clock signal) and how they compare against the actual EIA RS170 Specifications. The default signals that will be output are CSYNC, CBLANK, HDRIVE and VDRIVE. The device initially starts at the beginning of the odd field of interlace. All signals have active low pulses and the clock is disabled at power up. Registers 13 and 14 are not involved in the actual signal information. If the Vertical Interrupt was selected so that a pulse indicating the active lines would be output.

Reg	D Value H		Register Description
REG0	0	000	Status Register (715/LM1882)
REG0	1024	400	Status Register (715-R/LM1882-R)
REG1	23	017	HFP End Time
REG2	91	05B	HSYNC Pulse End Time
REG3	157	09D	HBLANK Pulse End Time
REG4	910	38E	Total Horizontal Clocks
REG5	7	007	VFP End Time
REG6	13	00D	VSYNC Pulse End Time
REG7	41	029	VBLANK Pulse End Time
REG8	525	20D	Total Vertical Lines
REG9	57	039	Equalization Pulse End Time
REG10	410	19A	Serration Pulse Start Time
REG11	1	001	Pulse Interval Start Time
REG12	19	013	Pulse Interval End Time
REG13	41	029	Vertical Interrupt Activate Time
REG14	526	20E	Vertical Interrupt Deactivate Time
REG15	911	38F	Horizontal Drive Start Time
REG16	92	05C	Horizontal Drive End Time
REG17	1	001	Vertical Drive Start Time
REG18	21	015	Vertical Drive End Time

	Rate	Period
Input Clock	14.31818 MHz	69.841 ns
Line Rate	15.73426 kHz	63.556 μs
Field Rate	59.94 Hz	16.683 ms
Frame Rate	29.97 Hz	33.367 ms

RS170 Horizontal Data

Signal	Width	μs	%H	Specification (μs)
HFP	22 Clocks	1.536		1.5 ±0.1
HSYNC Width	68 Clocks	4.749	7.47	4.7 ±0.1
HBLANK Width	156 Clocks	10.895	17.15	10.9 ±0.2
HDRIVE Width	91 Clocks	6.356	10.00	0.1H ±0.005H
HEQP Width	34 Clocks	2.375	3.74	2.3 ±0.1
HSERR Width	68 Clocks	4.749	7.47	4.7 ±0.1
HPER iod	910 Clocks	63.556	100	

RS170 Vertical Data

VFP	3 Lines	190.67		6 EQP Pulses
VSYNC Width	3 Lines	190.67		6 Serration Pulses
VBLANK Width	20 Lines	1271.12	7.62	0.075V ± 0.005V
VDRIVE Width	11.0 Lines	699.12	4.20	0.04V ± 0.006V
VEQP Intrvl	9 Lines		3.63	9 Lines/Field
VPERiod (field)	262.5 Lines	16.683 ms		16.683 ms/Field
VPERiod (frame)	525 Lines	33.367 ms		33.367 ms/Frame

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Diode Current (I_{IK})	
$V_I = -0.5V$	−20 mA
$V_I = V_{CC} + 0.5V$	+20 mA
DC Input Voltage (V_I)	−0.5V to V_{CC} +0.5V
DC Output Diode Current (I_{OK})	
$V_O = -0.5V$	−20 mA
$V_O = V_{CC} + 0.5V$	+20 mA
DC Output Voltage (V_O)	−0.5V to V_{CC} +0.5V
DC Output Source or Sink Current (I_O)	±15 mA
DC V_{CC} or Ground Current per Output Pin (I_{CC} or I_{GND})	±20 mA
Storage Temperature (T_{STG})	−65°C to +150°C
Junction Temperature (T_J)	
Ceramic	175°C
Plastic	140°C

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature and output/input loading variables. National does not recommend operation of FACT™ circuits outside databook specifications.

Recommended Operating Conditions

Supply Voltage (V_{CC})	4.5V to 5.5V
Input Voltage (V_I)	0V to V_{CC}
Output Voltage (V_O)	0V to V_{CC}
Operating Temperature (T_A)	
74ACT	−40°C to +85°C
54ACT	−55°C to +125°C
Minimum Input Edge Rate ($\Delta V/\Delta t$)	
V_{IN} from 0.8V to 2.0V	
V_{CC} @ 4.5V, 5.5V	125 mV/ns

DC Characteristics For 'ACT Family Devices over Operating Temperature Range (unless otherwise specified)

Symbol	Parameter	V_{CC} (V)	ACT/LM1882 $T_A = +25°C$, $C_L = 50$ pF		54ACT/LM1882 $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF	74ACT/LM1882 $T_A = -40°C$ to $+85°C$	Units	Conditions
			Typ	Guaranteed Limits				
V_{OH}	Minimum High Level Output Voltage	4.5	4.49	4.4	4.4	4.4	V	$I_{OUT} = -50\ \mu A$
		5.5	5.49	5.4	5.4	5.4	V	
		4.5		3.86	3.7	3.76	V	*$V_{IN} = V_{IL}/V_{IH}$
		5.5		4.86	4.7	4.76	V	$I_{OH} = -8$ mA
V_{OL}	Maximum Low Level Output Voltage	4.5	0.001	0.1	0.1	0.1	V	$I_{OUT} = 50\ \mu A$
		5.5	0.001	0.1	0.1	0.1	V	
		4.5		0.36	0.5	0.44	V	*$V_{IN} = V_{IL}/V_{IH}$
		5.5		0.36	0.5	0.44	V	$I_{OH} = +8$ mA
I_{OLD}	Minimum Dynamic Output Current	5.5			32.0	32.0	mA	$V_{OLD} = 1.65V$
I_{OHD}	Minimum Dynamic Output Current	5.5			−32.0	−32.0	mA	$V_{OHD} = 3.85V$
I_{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	±1.0	μA	$V_I = V_{CC}$, GND
I_{CC}	Supply Current Quiescent	5.5		8.0	160	80	μA	$V_{IN} = V_{CC}$, GND
I_{CCT}	Maximum I_{CC}/Input	5.5	0.6		1.6	1.5	mA	$V_{IN} = V_{CC} - 2.1V$

*All outputs loaded; thresholds on input associated with input under test.

Note 1: Test Load 50 pF, 500Ω to Ground.

AC Electrical Characteristics

Symbol	Parameter	V_{CC} (V)	ACT/LM1882 $T_A = +25°C$, $C_L = 50$ pF			54ACT/LM1882 $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74ACT/LM1882 $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units
			Min	Typ	Max	Min	Max	Min	Max	
f_{MAXI}	Interlaced f_{MAX} (HMAX/2 is ODD)	5.0	170	190		130		150		MHz
f_{MAX}	Non-Interlaced f_{MAX} (HMAX/2 is EVEN)	5.0	190	220		145		175		MHz
t_{PLH1} t_{PHL1}	Clock to Any Output	5.0	4.0	13.0	15.5	3.5	19.5	3.5	18.5	ns
t_{PLH2} t_{PHL2}	Clock to ODDEVEN (Scan Mode)	5.0	4.5	15.0	17.0	3.5	22.0	3.5	20.5	ns
t_{PLH3}	Load to Outputs	5.0	4.0	11.5	16.0	3.0	20.0	3.0	19.5	ns

AC Operating Requirements

Symbol	Parameter	V_{CC} (V)	ACT/LM1882 $T_A = +25°C$		54ACT/LM1882 $T_A = -55°C$ to $+125°C$	74ACT/LM1882 $T_A = -40°C$ to $+85°C$	Units
			Typ	Guaranteed Minimums			
	Control Setup Time						
t_{sc}	ADDR/DATA to LOAD−	5.0	3.0	4.0	4.5	4.5	ns
t_{sc}	L/HBYTE to LOAD−		3.0	4.0	4.5	4.5	ns
t_{sd}	Data Setup Time D7–D0 to LOAD+	5.0	2.0	4.0	4.5	4.5	ns
	Control Hold Time						
t_{hc}	LOAD− to ADDR/DATA	5.0	0	1.0	1.0	1.0	ns
	LOAD− to L/HBYTE		0	1.0	1.0	1.0	ns
t_{hd}	Data Hold Time LOAD+ to D7–D0	5.0	1.0	2.0	2.0	2.0	ns
t_{rec}	LOAD+ to CLK (Note 1)	5.0	5.5	7.0	8.0	8.0	ns
	Load Pulse Width						
t_{wld-}	LOW	5.0	3.0	5.5	5.5	5.5	ns
t_{wld+}	HIGH	5.0	3.0	5.0	7.5	7.5	ns
t_{wclr}	CLR Pulse Width HIGH	5.0	5.5	6.5	9.5	9.5	ns
t_{wck}	CLOCK Pulse Width (HIGH or LOW)	5.0	2.5	3.0	4.0	3.5	ns

Note 1: Removal of Vectored Reset or Restart to Clock.

Capacitance

Symbol	Parameter	Typ	Units	Conditions
C_{IN}	Input Capacitance	7.0	pF	$V_{CC} = 5.0V$
C_{PD}	Power Dissipation Capacitance	17.0	pF	$V_{CC} = 5.0V$

AC Operating Requirements (Continued)

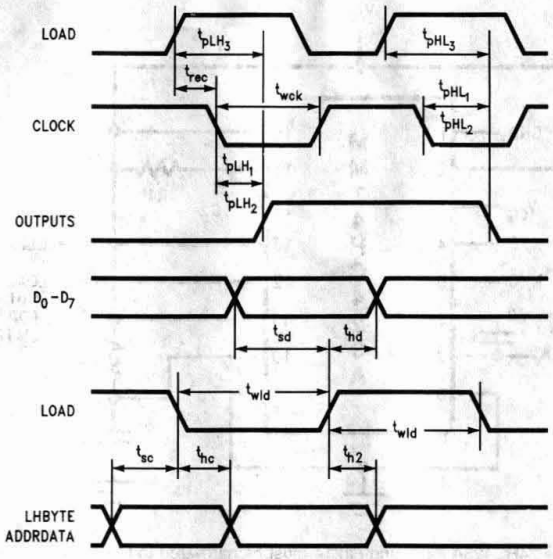

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FIGURE 4. AC Specifications

Additional Applications Information

POWERING UP

The 'ACT715/LM1882 default value for Bit 10 of the Status Register is 0. This means that when the CLEAR pulse is applied and the registers are initialized by loading the default values the CLOCK is disabled. Before operation can begin, Bit 10 must be changed to a 1 to enable CLOCK. If the default values are needed (no other programming is required) then *Figure 5* illustrates a hardwired solution to facilitate the enabling of the CLOCK after power-up. Should control signals be difficult to obtain, *Figure 6* illustrates a possible solution to automatically enable the CLOCK upon power-up. Use of the 'ACT715-R/LM1882-R eliminates the need for most of this circuitry. Modifications of the *Figure 6* circuit can be made to obtain the lone CLEAR pulse still needed upon power-up.

Note that, although during a Vectored Restart none of the preprogrammed registers are affected, some signals are affected for the duration of one frame only. These signals are the Horizontal and Vertical Drive signals. After a Vectored Restart the beginning of these signals will occur at the first CLK. The end of the signals will occur as programmed. At the completion of the first frame, the signals will resume to their programmed start and end time.

PREPROGRAMMING "ON-THE-FLY"

Although the 'ACT715/LM1882 and 'ACT715-R/LM1882-R are completely programmable, certain limitations must be set as to when and how the parts can be reprogrammed. Care must be taken when reprogramming any End Time registers to a new value that is lower than the current value. Should the reprogramming occur when the counters are at a count after the new value but before the old value, then the counters will continue to count up to 4096 before rolling over.

For this reason one of the following two precautions are recommended when reprogramming "on-the-fly". The first recommendation is to reprogram horizontal values during the horizontal blank interval only and/or vertical values during the vertical blank interval only. Since this would require delicate timing requirements the second recommendation may be more appropriate.

The second recommendation is to program a Vectored Restart as the final step of reprogramming. This will ensure that all registers are set to the newly programmed values and that all counters restart at the first CLK position. This will avoid overrunning the counter end times and will maintain the video integrity.

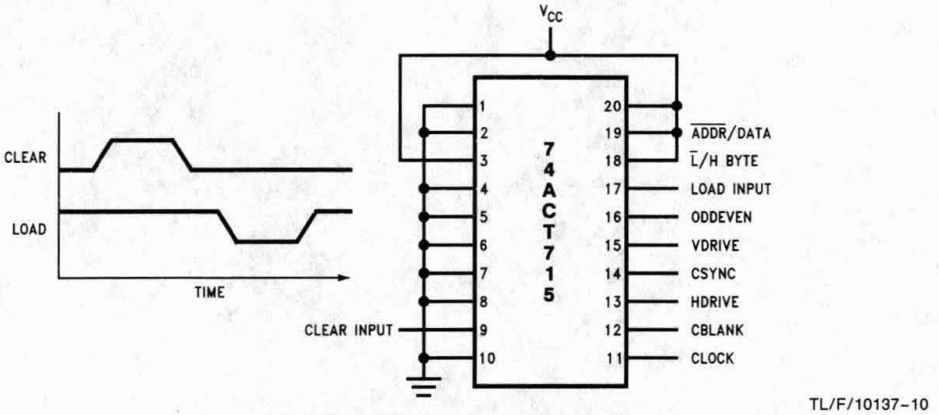

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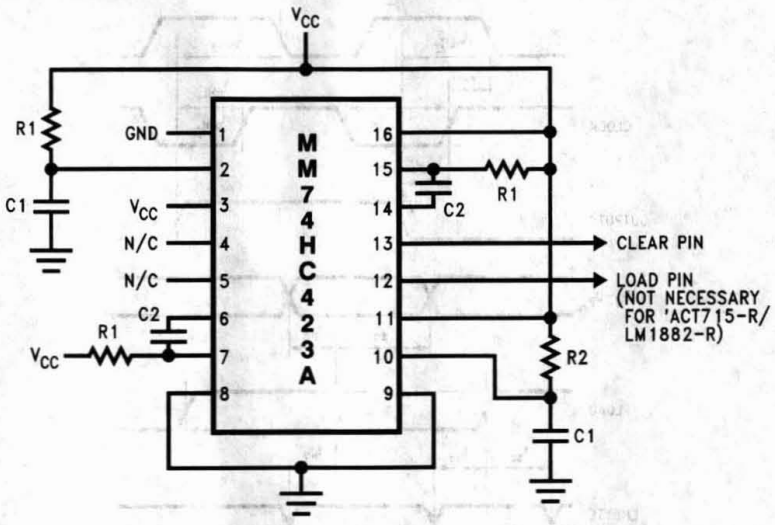
FIGURE 5. Default RS170 Hardwire Configuration

Additional Applications Information (Continued)



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Note: A 74HC221A may be substituted for the 74HC423A Pin 6 and Pin 14 must be hardwired to GND

Components

R1: 4.7k C1: 10 μF
R2: 10k C2: 50 pF

FIGURE 6. Circuit for Clear and Load Pulse Generation

National Semiconductor

LM2889 TV Video Modulator

General Description

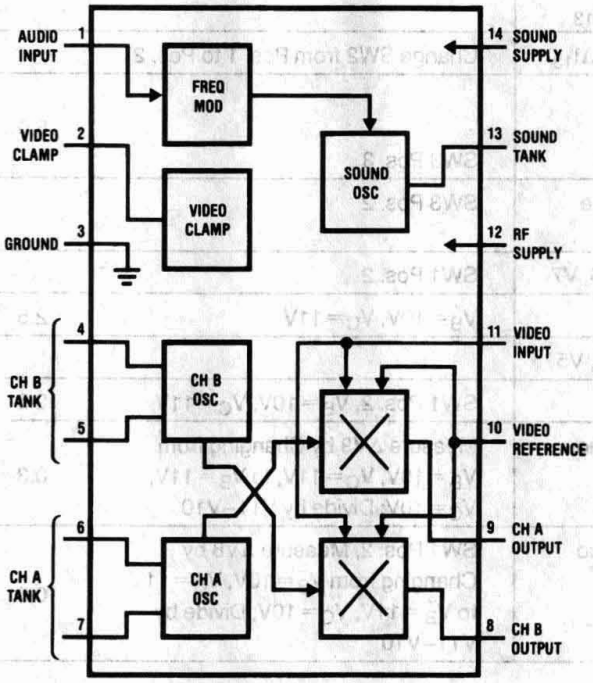
The LM2889 is designed to interface audio and video signals to the antenna terminals of a TV receiver. It consists of a sound subcarrier oscillator and FM modulator, video clamp, and RF oscillators and modulators for two low-VHF channels.

The LM2889 allows video information from VTRs, video disk systems, games, test equipment, or similar sources to be displayed on black and white or color TV receivers.

Features

- Pin for pin compatible with LM1889 RF section
- Low distortion FM sound modulator (less than 1% THD)
- Video clamp for AC-coupled video
- Low sound oscillator harmonic levels
- 10V to 16V supply operation
- DC channel switching
- Excellent oscillator stability
- Low intermodulation products

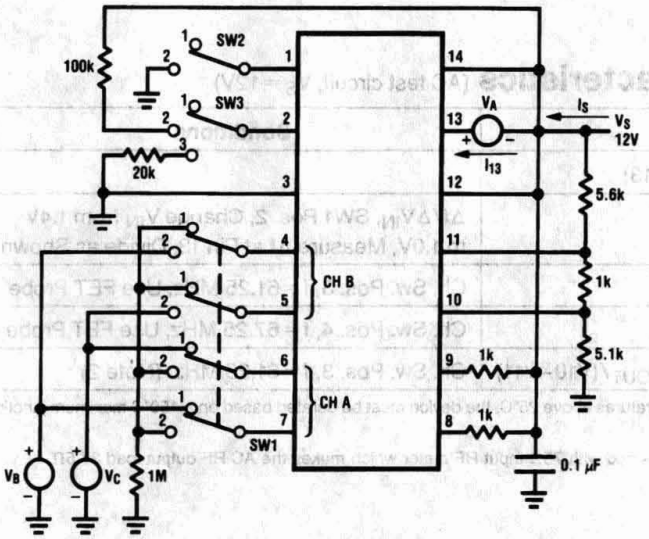
Block and Connection Diagrams (Dual-In-Line Package)



TOP VIEW

Order Number LM2889N
See NS Package Number N14A

DC Test Circuit



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Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	$18V_{DC}$
Power Dissipation Package (Note 1)	700 mW
Operating Temperature Range	0°C to +70°C
Storage Temperature Range	−55°C to +150°C
(V14−V13) Max	$\pm 5V_{DC}$
(V12−V8) Max	$7V_{DC}$
(V12−V9) Max	$7V_{DC}$
Lead Temperature (Soldering, 10 seconds)	260°C

DC Electrical Characteristics

(DC test circuit, all switches normally pos. 1, $V_S = 12V$, $V_A = 2V$, $V_B = V_C = 10V$)

Parameter	Conditions	Min	Typ	Max	Units
Supply Current I_S		10	16	25	mA
Sound Oscillator Current ΔI_{13}	Change V_A from −2V to +2V	0.2	0.35	0.6	mA
Sound Oscillator Zener Current I_{13}			0.85		mA
Sound Modulator Audio Current ΔI_{13}	Change SW2 from Pos. 1 to Pos. 2		0.9		mA
Video Clamp Voltage V2 Unloaded Loaded	 SW3 Pos. 3	 5.0	 5.25 5.1	 5.5	 V_{DC} V_{DC}
Video Clamp Capacitor Discharge Current $(V_S - V2)/10^5$	SW3 Pos. 2		20		μA
Ch. A Oscillator OFF Voltage, V6, V7	SW1 Pos. 2		2		mV_{DC}
Ch. A Oscillator Current Level I_7	$V_B = 10V$, $V_C = 11V$	2.5	3.5	5.0	mA
Ch. B Oscillator OFF Voltage V4, V5			2		mV_{DC}
Ch. B Oscillator Current Level I_4	SW1 Pos. 2, $V_B = 10V$, $V_C = 11V$	2.5	3.5	5.0	mA
Ch. A Modulator Conversion Ratio $\Delta V9/(V11\text{-}V10)$	Measure ΔV9 by Changing from $V_B = 10V$, $V_C = 11V$, to $V_B = 11V$, $V_C = 10V$; Divide by V11−V10	0.3	0.50	0.75	V/V
Ch. B Modulator Conversion Ratio $\Delta V8/(V11-V10)$	SW1 Pos. 2, Measure ΔV8 by Changing from $V_B = 10V$, $V_C = 11V$, to $V_B = 11V$, $V_C = 10V$; Divide by V11−V10	0.3	0.50	0.75	V/V

AC Electrical Characteristics (AC test circuit, $V_S = 12V$)

Parameter	Conditions	Min	Typ	Max	Units
Sound Carrier Oscillator Level (V13)			3.4		Vp-p
Sound Modulator Deviation	$\Delta f/\Delta V_{IN}$, SW1 Pos. 2, Change V_{IN} from 1.4V to 1.0V, Measure Δf at Pin 13, Divide as Shown		250		Hz/mV
Ch. 3 RF Oscillator Level $\nu 6$, $\nu 7$	Ch. Sw. Pos. 3, f = 61.25 MHz, Use FET Probe		550		mVp-p
Ch. 4 RF Oscillator Level, $\nu 4$, $\nu 5$,	Ch. Sw. Pos. 4, f = 67.25 MHz, Use FET Probe		550		mVp-p
RF Modulator Conversion Gain $\nu_{OUT}/(V10-V11)$	Ch. Sw. Pos. 3, f = 61.25 MHz. (Note 2)		10		mVrms/V

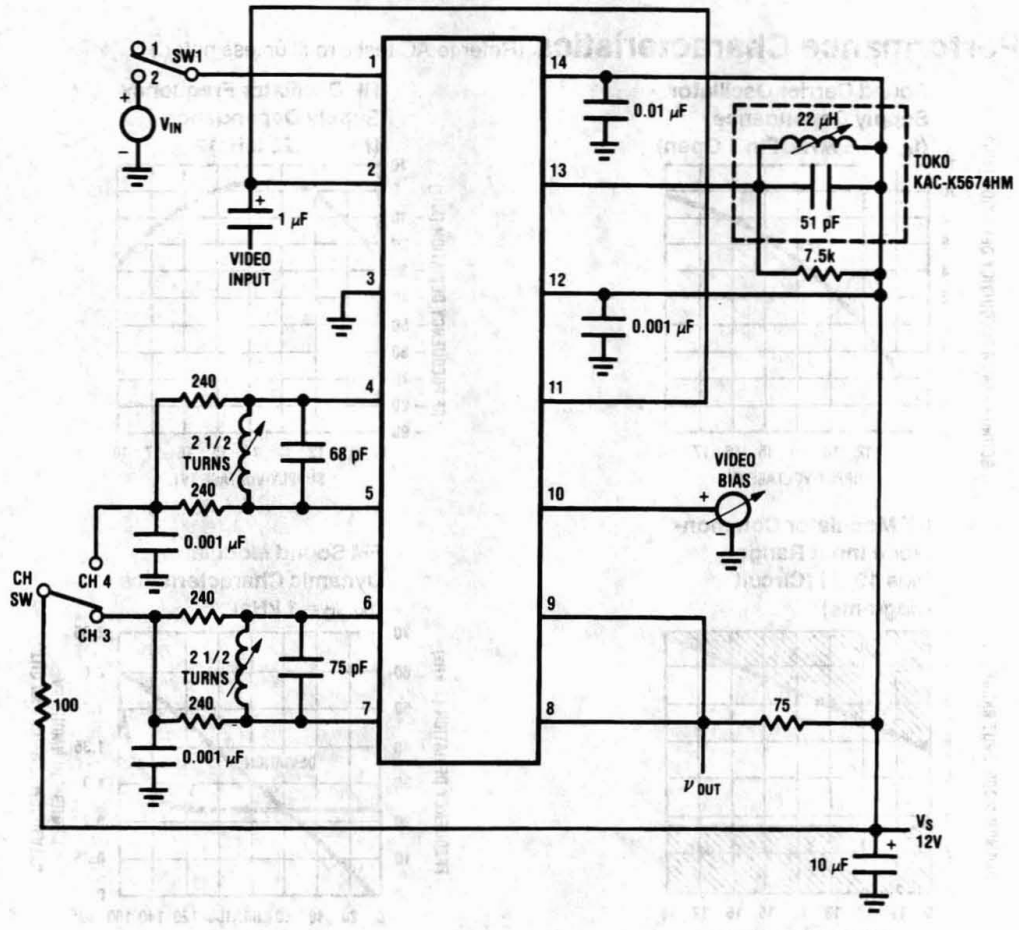
Note 1: For operation in ambient temperatures above 25°C, the device must be derated based on a 150°C maximum junction temperature and a thermal resistance of 80°C/W junction to ambient.

Note 2: Conversion gain shown is measured with 75Ω input RF meter which makes the AC RF output load 37.5Ω.

Design Characteristics (AC test circuit, $V_S = 12V$)

Parameter	Typ	Units
Sound Modulator Audio THD at ±25 kHz Deviation, V_{IN} must be 1 kHz Source, Demodulate as Shown in *Figure 1*	0.8	%
Sound Modulator Input Impedance (Pin 1)	1.5	kΩ
Sound Modulator Bandwidth	100	kHz
Oscillator Supply Dependence, Sound Carrier, RF	See Curves	
Oscillator Temperature Dependence (IC Only)		
Sound Carrier	−15	ppm/°C
RF	−50	ppm/°C
RF Oscillator Maximum Operating Frequency (Temperature Stability Degraded)	100	MHz
RF Modulator		
Carrier Suppression (Adjust Video Bias for Minimum RF Carrier at ν_{OUT} and Reference to ν_{OUT} with 3V Offset at Pins 10 and 11, See Applications Information, RF Modulation Section)	30	dB
3.58 MHz Differential Gain	5	%
Differential Phase	3	degrees
2.5V Vp-p Video, 87.5% Mod		
Output Harmonics below RF Carrier		
2nd, 3rd	−12	dB
4th and Above	−20	dB
Input Impedance, Pin 10, Pin 11	1 MΩ//2 pF	

AC Test Circuit



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Test Circuit

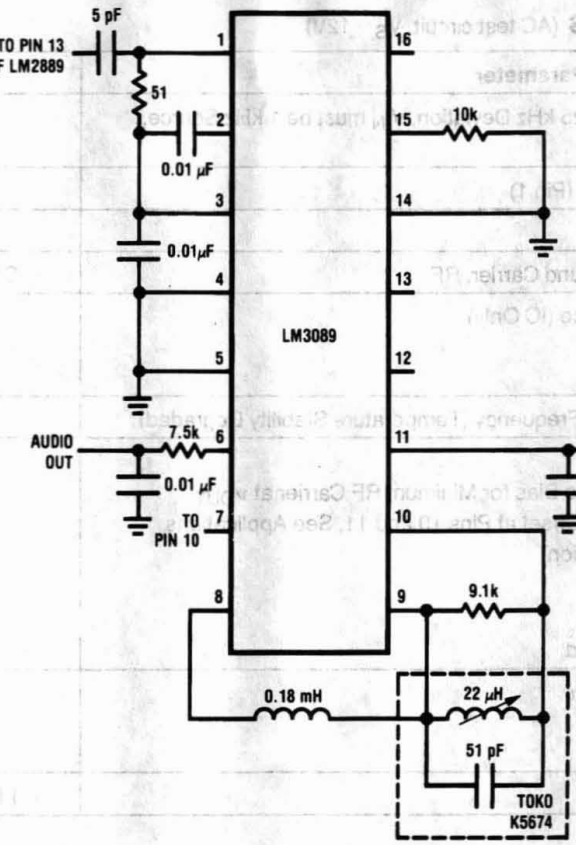
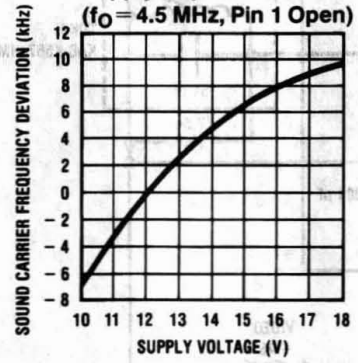


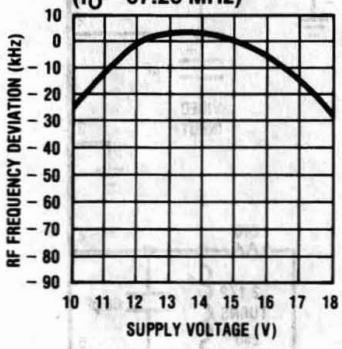
FIGURE 1. 4.5 MHz Sound FM Demodulator

Typical Performance Characteristics (Refer to AC test circuit unless noted)

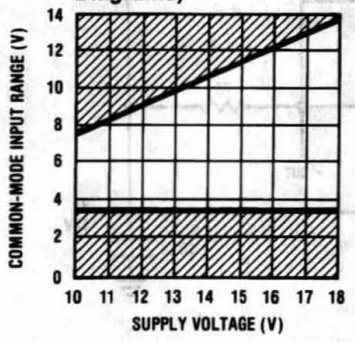
Sound Carrier Oscillator Supply Dependence (f_O = 4.5 MHz, Pin 1 Open)



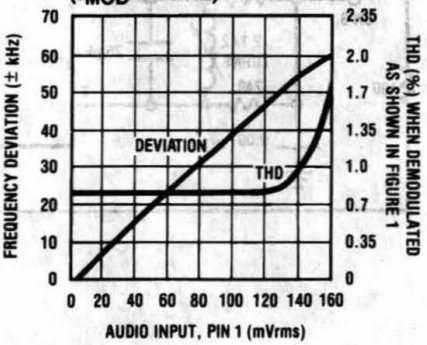
RF Oscillator Frequency Supply Dependence (f_O = 67.25 MHz)



RF Modulator Common-Mode Input Range Pins 10, 11 (Circuit Diagrams)



FM Sound Modulator Dynamic Characteristics (f_{MOD} = 1 kHz)



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Circuit Description (Refer to Circuit Diagrams)

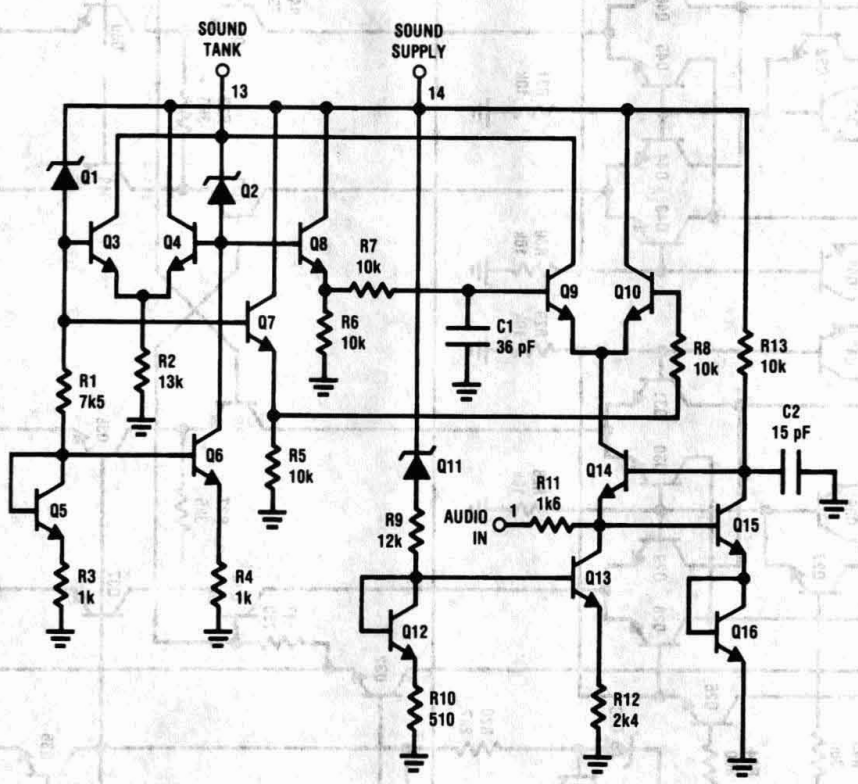
The sound carrier oscillator is formed by differential amplifier Q3, Q4 operated with positive feedback from the pin 13 tank to the base of Q4. Frequency modulation is obtained by varying the 90 degree phase shifted current of Q9. Q14's emitter is a virtual ground, so the voltage at pin 1 determines the current R11, which ultimately modulates the collector current of Q9.

The video clamp is comprised of devices Q58-Q60. The clamp voltage is set by resistors R40, R41, R49, and R50. The ΔV_{BE}/R42 current sets the capacitor discharge current. Q59 and the above mentioned resistor string help maintain a temperature stable clamp voltage.

The channel B oscillator consists of devices Q24 and Q25 cross-coupled through level-shift zener diodes Q22 and Q23. A current regulator consisting of devices Q17–Q21 is used to achieve good RF stability over temperature and supply. The channel B modulator consists of multiplier devices Q28–Q31, Q34 and Q35. The top quad is coupled to the channel B tank through isolating devices Q26 and Q27. A DC potential between pins 10 and 11 offsets the lower pair to produce an output RF carrier at pin 8. That carrier is then modulated by both the sound subcarrier at pin 10 and the composite video signal at pin 11. The channel A modulator shares pin 10 and 11 buffers, Q32 and Q33, with channel B and operates in an identical manner.

The current flowing through channel B oscillator diodes Q22, Q23 is turned around in Q36–Q38 to source current for the channel B RF modulator. In the same manner, the channel A oscillator Q54–Q57 uses turn-around Q49–Q51 to source the channel A modulator. One oscillator at a time may be activated by its current turn-around, and the other oscillator/modulator combination remains off.

Circuit Diagrams



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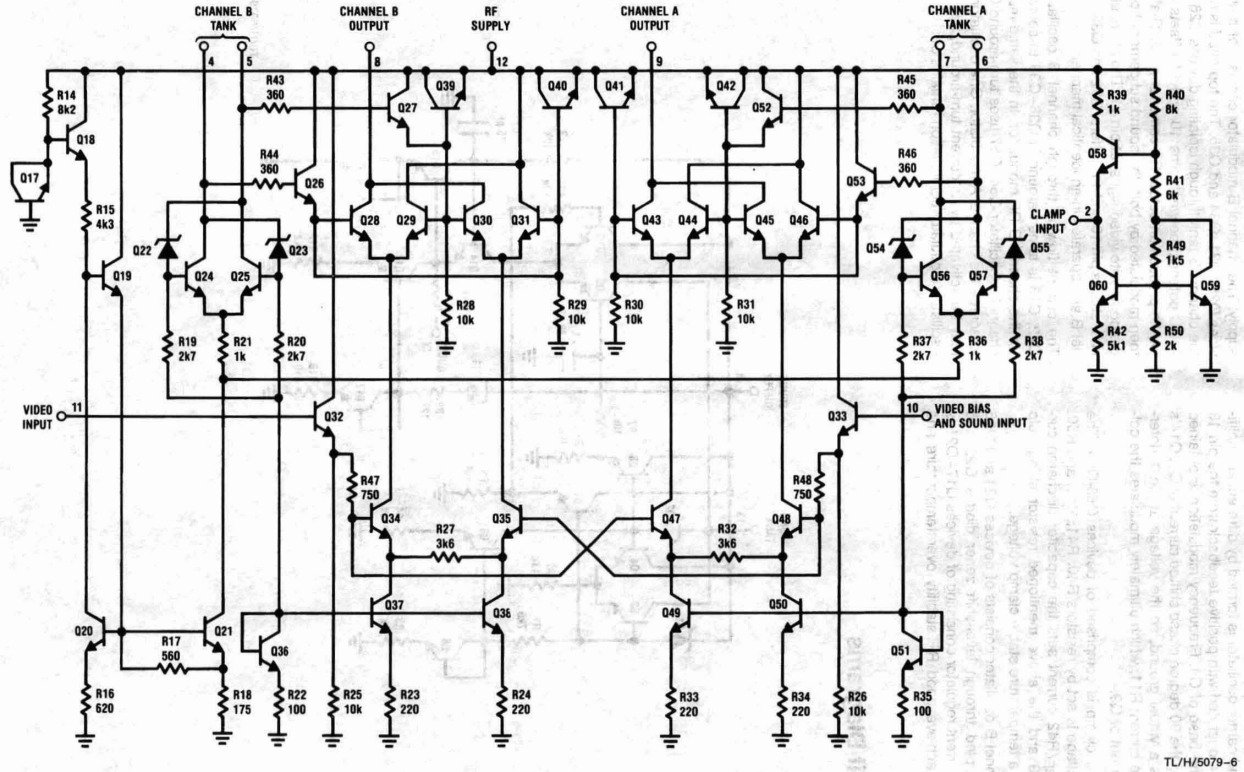
Circuit Diagrams (Continued)



Applications Information

SOUND FM MODULATOR

Frequency deviation is determined by the Q of the tank circuit at pin 13 and the current entering the audio input, pin 1. This current is set by the input voltage V_{IN}, the device input impedance (1.5 kΩ), and any impedance network connected externally. A signal of 60 mVrms at pin 1 will yield about ±25 kHz deviation when configured as shown in *Figure 2*.

VIDEO CLAMP

When video is not available at DC levels within the RF modulator common-mode range, or if the DC level of the video is not temperature stable, then it should be AC-coupled as shown in the typical applications circuit (*Figure 2*). The clamp holds the horizontal sync pulses at 5.2V for $V_S = 12V$. The clamp coupling capacitor is charged during every sync pulse and discharged when video information is present. The discharge current is approximately 20 μA. This current and the amount of acceptable tilt over a line of video determines the value of the coupling capacitor C1. For most applications 1 μF is sufficient.

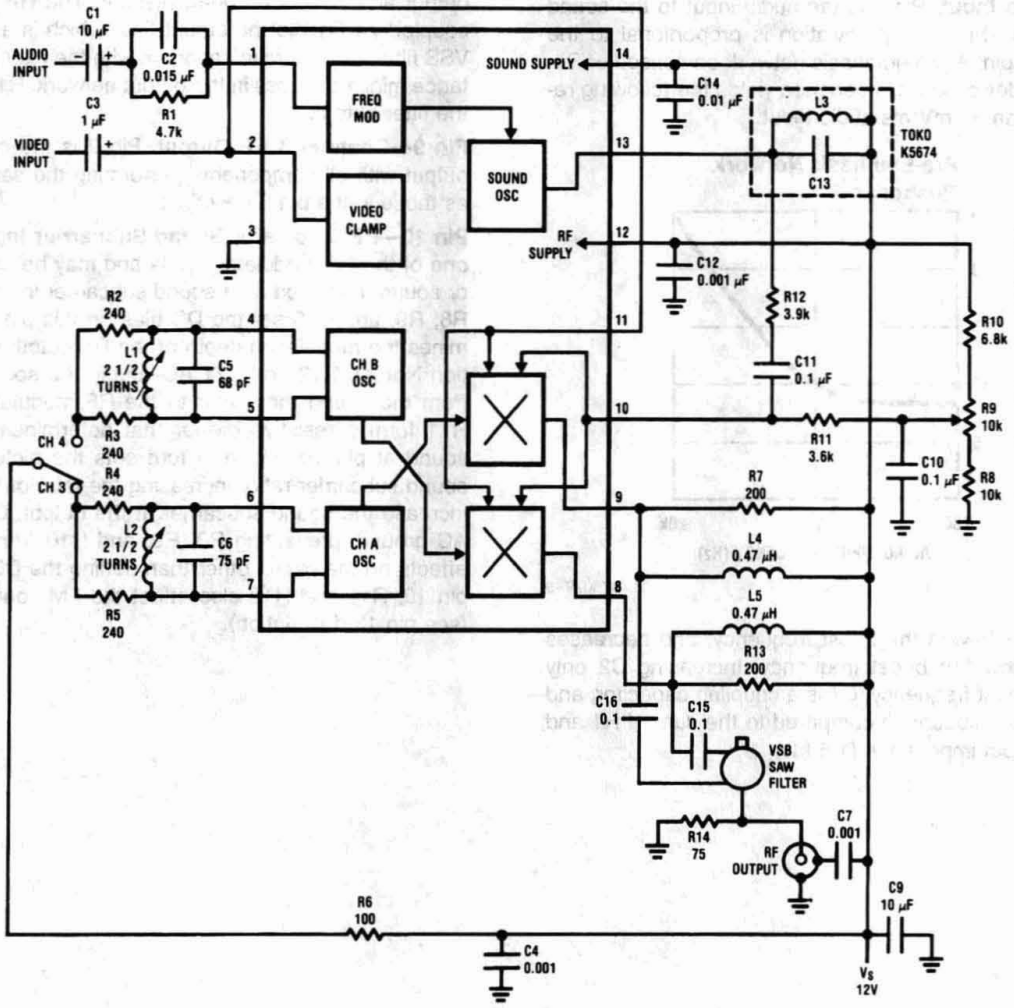
RF MODULATION

Two RF channels are available, with carrier frequencies up to 100 MHz being determined by L-C tank circuits at pins 4/ 5 and 6/7. The signal inputs (pins 10 and 11) are common to both modulators, but removing the power supply from an RF oscillator will also disable that modulator.

The offset between the two signal pins determines the level of the RF carrier output. To preserve the DC content of the video signal, amplitude modulation of the RF carrier is done in one direction only, with increasing video (toward peak white) decreasing the carrier level. This means the active composite video signal at pin 11 must be offset with respect to pin 10 and the sync pulse should produce the largest offset.

The largest video signal (peak white) should not be able to suppress the carrier completely, particularly if sound transmission is needed. This requires that pin 10 be biased above the largest expected video signal. Because peak white level is often difficult to define, a good rule to follow is to bias pin 10 at a level which is four times the sync amplitude above the sync tip level at pin 11. For example, the DC bias at pin 10 with 0.5V sync clamped to 5.2V on pin 11, should be $5.2 + (4 \times 0.5) = 7.2V$.

Typical Application

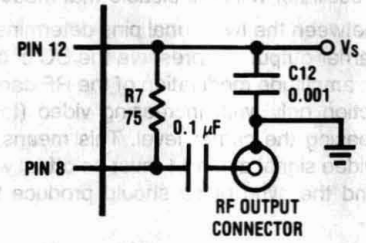


TL/H/5079–7

FIGURE 2. Two Channel Video Modulator with FM Sound

Applications Information (Continued)

When the signal inputs are exactly balanced, ideally there is no RF carrier at the output. Circuit board layout is critical to this measurement. For optimum performance, the output and supply decoupling circuitry should be configured as shown in *Figure 3*.



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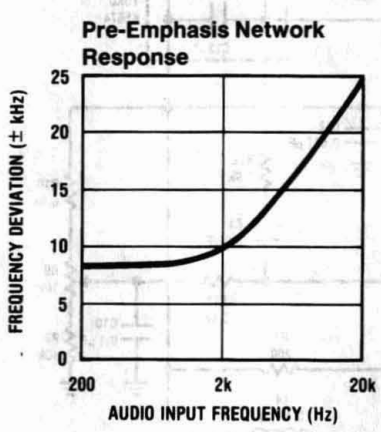
RF decouple supply directly to output ground.

FIGURE 3. Correct RF Supply Decoupling

The video clamp level is derived from a resistive divider connected to supply (V_S). To maintain good supply rejection, pin 10, which is biased externally, should also be referenced to supply (see *Figure 2*).

Pin Description (Refer to *Figure 2*)

Pin 1—Audio Input: Pin 1 is the audio input to the sound FM generator. Frequency deviation is proportional to the signal at this pin. A pre-emphasis network comprised of R1, C2, and the device input impedance yields the following response with an 80 mVrms audio input.



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Increasing R1 lowers the boost frequency, and decreases deviation below the boost frequency. Increasing C2 only lowers the boost frequency. C1 is a coupling capacitor, and must be a low impedance compared to the sum of R1 and the device input impedance (1.5 kΩ).

Pin 2—Video Clamp: The video clamp restores the DC component to AC-coupled video. The video is AC-coupled to the clamp via C3. Decreasing C3 will cause a larger tilt between vertical sync pulses in the clamped video waveform.

Pin 3—Ground: Although separate on the chip level, all ground terminate at pin 3.

Pins 4/5—Channel 4 Oscillator: Pins 4 and 5 are the collector outputs of the channel 4 oscillator. L1 and C5 set the oscillator frequency defined by $f_O = 0.159/\sqrt{L1C5}$. Increasing L1 will decrease the oscillator frequency while decreasing L1 will increase the oscillator frequency. Decreasing C5 will increase the oscillator frequency and lower the tank Q causing possible drift problems. R2 and R3 are the oscillator loads which determine the oscillator amplitude and the tank Q. Increasing these resistors increases the Q and the oscillator amplitude, possibly overdriving the RF modulator, which will increase output RF harmonics. Decreasing R2 and R3 reduces the tank Q and may cause increased drift. C4 is an RF decoupling capacitor. Increasing C4 may result in less effective decoupling at RF. Decreasing C4 may introduce RF to supply coupling.

Pins 6/7—Channel 3 Oscillator; Pins 6 and 7 are the channel 3 oscillator outputs. Every component at these pins has the same purpose and effect as those at pins 4 and 5.

Pin 8—Channel 4 RF Output: Pin 8 is the channel 4 RF output and R13 is the load resistor. The RF signal is AC coupled via C15 to the output filter which is a two channel VSB filter. L5 is parallel resonant with the filter input capacitance minimizing loss in the output network. R14 terminated the filter output.

Pin 9—Channel 3 RF Output: Pin 9 is the channel 3 RF output with all components performing the same functions as those in the pin 8 description.

Pin 10—RF Modulator Sound Subcarrier Input: Pin 10 is one of the RF modulator inputs and may be used for video or sound. It is used as a sound subcarrier input in *Figure 2*. R8, R9, and R10 set the DC bias on this pin which determines the modulation depth of the RF output (see Application Notes). R12 and C11 AC-couple the sound subcarrier from the sound modulator to the RF modulator. R12 and R11 form a resistive divider that determines the level of sound at pin 10, which in turn sets the picture carrier to sound subcarrier ratio. Increasing the ratio of R11/R12 will increase the sound subcarrier at the output. C10 forms an AC ground, preventing R8, R9, and R10 from having any effects on the circuit other than setting the DC potential at pin 10. R11 and R12 also effect the FM sound modulator (see pin 13 description).

Pin Description (Continued)

Pin 11—Video Input: Pin 11, when configured as shown, is the RF modulator video input. In this application, video is coupled directly from the video clamp. Alternatively, video could be DC-coupled directly to pin 11 if it is already within the DC common-mode input range of the RF modulator (see curves). In any case, the video sync tip at pin 11 must have a constant DC level independent of video content. Because of circuit symmetry, pins 10 and 11 may be interchanged.

Pin 12—RF Supply: Pin 12 is the RF supply, with C12 and C7 serving as RF decouple capacitors. Increasing C12 or C7 may result in less effective RF decoupling, while decreasing them may cause supply interaction. It is important that C7 be grounded at the RF output ground.

Pin 13—Sound Tank: Pin 13 is the collector output of the sound oscillator. L3 and C13 determine the oscillating frequency by the relationship $f_O = 0.159/\sqrt{L3C13}$. Increasing L3 or C13 will lower the operating frequency, while decreasing them will raise the frequency. L3 and C13 also help define the Q of the tank, on which FM modulator deviation level depends. As C13 increases, Q increases, and frequency deviation decreases. Likewise, decreasing C13 increases deviation. The other factor concerning Q is the external resistance across the tank. The series combination R11 + R12 usually dominates the tank Q. Decreasing this resistive network will decrease Q and increase deviation. It should be noted that because the level of phase modulation of the 4.5 MHz signal remains constant, variation in Q will not effect distortion of the frequency modulation process if the audio at pin 1 is left constant. The amplitude of the sound subcarrier is directly proportional to Q, so increasing the unloaded Q or either of the resistors mentioned above will increase the sound subcarrier amplitude. For proper operation of the frequency modulator, the sound subcarrier amplitude should be greater than 2 Vp-p.

Pin 14—Sound Supply: Pin 14 is the sound supply and C14 is an RF decouple capacitor. Decreasing C14 may result in increased supply interaction.

Printed Circuit Layout

Printed circuit board layout is critical in preventing RF feedthrough. The location of RF bypass capacitors on supply is very important. *Figure 4* shows an example of a properly layed out circuit board. It is recommended that this layout be used.

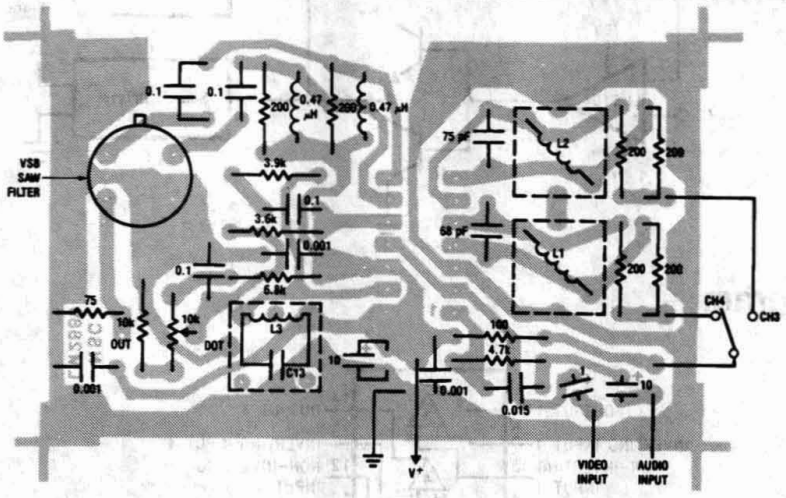

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FIGURE 4. Printed Circuit Board and Component Diagram (Component Side 1X)

National Semiconductor

LM6104
Quad Gray Scale Current Feedback Amplifier

General Description

The LM6104 quad amplifier meets the requirements of battery operated liquid crystal displays by providing high speed while maintaining low power consumption.

Combining this high speed with high integration, the LM6104 conserves valuable board space in portable systems with a cost effective, surface mount quad package.

Built on National's advanced high speed VIP™ (Vertically Integrated PNP) process, the LM6104 current feedback architecture is easily compensated for speed and loading conditions. These features make the LM6104 ideal for buffering grey levels in liquid crystal displays.

Features (Typical unless otherwise noted)

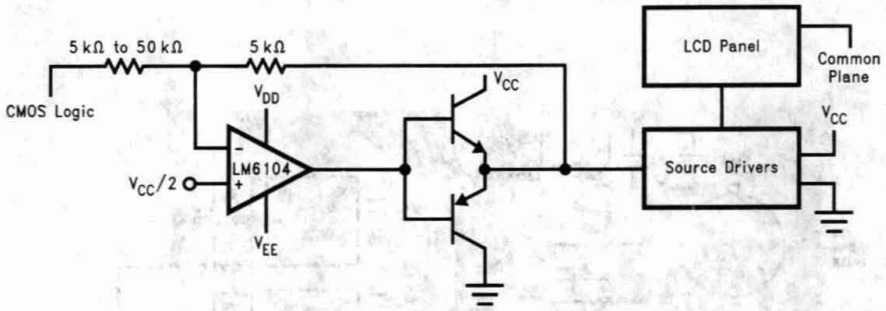
- Low power — I_S = 875 μA/amplifier
- Slew rate — 100V/μs
- −3dB bandwidth (R_F = 1 kΩ) — 30 MHz
- High output drive — ±5V into 100Ω
- Wide operating range — V_S = 5V to ±12V
- High integration — Quad surface mount

Applications

- Grey level buffer for liquid crystal displays
- Column buffer for portable LCDs
- Video distribution amplifiers, video line drivers
- Hand-held, high speed signal conditioning

Typical Application

LCD Buffer Application for Grey Levels



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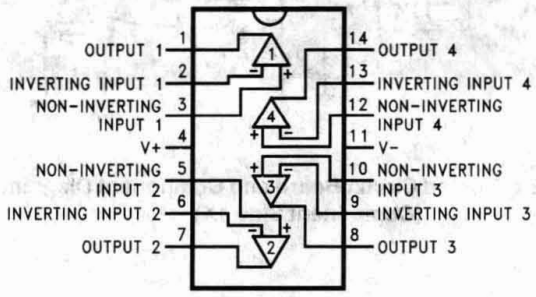
Connection Diagram



TL/H/11979–2

Order Number LM6104M
See NS Package Number M14A

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	24V
Differential Input Voltage	±6V
Input Voltage	±Supply Voltage
Inverting Input Current	15 mA
Soldering Information	
Vapor Phase (60s)	215°C
Infrared (15s)	220°C
Storage Temperature Range	$-65°C \le T_J \le +150°C$
Maximum Junction Temperature	150°C
ESD Rating (Note 2)	2000V

Operating Ratings

Supply Voltage Range	4.75V to 24V
Junction Temperature Range (Note 3)	
LM6104M	$-20° \le T_J \le +80°C$

Electrical Characteristics

The following specifications apply for $V+ = 8V$, $V- = -5V$, $R_L = R_F = 2\ k\Omega$ and $0° \le T_J \le 60°C$ unless otherwise noted.

Symbol	Parameter	Conditions	LM6104M		Units
			Typical (Note 4)	Limits (Note 5)	
V_{OS}	Input Offset Voltage		10	30	mV max
I_B	Inverting Input Bias Current		5.0	20	μA max
	Non-Inverting Input Bias Current		0.5	2	μA max
I_S	Supply Current	$V_O = 0V$	3.5	4.0	mA max
I_{SC}	Output Source Current	$V_O = 0V$ $I_{IN(-)} = -100\ \mu A$	60	45	mA min
	Output Sink Current	$V_O = 0V$ $I_{IN(-)} = 100\ \mu A$	60	45	mA min
V_O	Positive Output Swing	$I_{IN(-)} = -100\ \mu A$	6.5	6.1	V min
	Negative Output Swing	$I_{IN(-)} = 100\ \mu A$	−3.5	−3.1	V max
PSRR	Power Supply Rejection Ratio	$V_S = \pm 4$ to $\pm 10V$	70	60	dB min
		100 mV pp @ 100 kHz	40	30	dB min
R_T	Transresistance		10	5	MΩ min
SR	Slew Rate	(Note 6)	100	55	V/μs min
BW	Bandwidth	$A_V = -1$ $R_{IN} = R_F = 2\ k\Omega$	7.5	5.0	MHz
	Amp-to-Amp Isolation	$R_L = 2\ k\Omega$ $F = 1\ MHz$	60		dB
CMVR	Common Mode Voltage Range		$V+ - 1.4V$ $V- + 1.4V$		V
CMRR	Common Mode Rejection Ratio		60		dB
t_S	Settling Time	0.05%, 5V Step, $A_V = -1$ $R_F = R_S = 2\ k\Omega$, $V_S = \pm 5V$	240		ns

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications do not apply when operating the device beyond its rated operating conditions. Operating ratings indicate conditions the device is intended to be functional, but device parameter specifications may not be guaranteed under the conditions.

Note 2: Human body model 1.5 kΩ and 100 pF. This is a class 2 device rating.

Note 3: Thermal resistance of the SO package is 98°C/W. When operating at $T_A = 80°C$, maximum power dissipation is 700 mW.

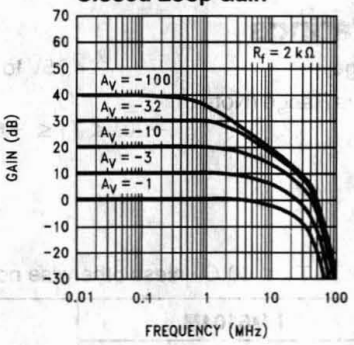
Note 4: Typical values represent the most likely parametric norm.

Note 5: All limits guaranteed at operating temperature extremes.

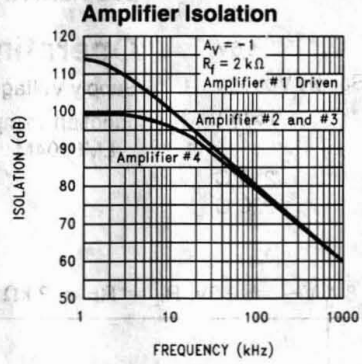
Note 6: $A_V = -1$ with $R_{IN} = R_F = 2\ k\Omega$. Slew rate is calculated from the 25% to the 75% point on both rising and falling edges. Output swing is −0.6V to +5.6V and 5.6V to 0.6V.

Typical Performance Characteristics

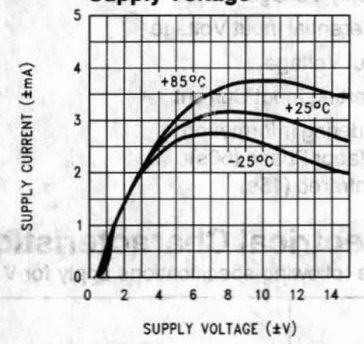
Frequency Response vs Closed Loop Gain



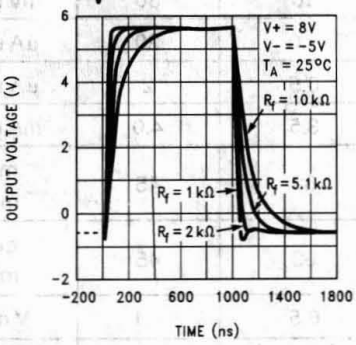
Amplifier to Amplifier Isolation



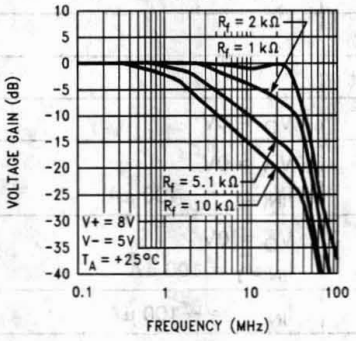
Supply Current vs Supply Voltage



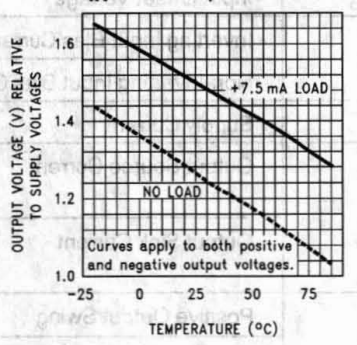
Large Signal Pulse Response
$A_V = -1$



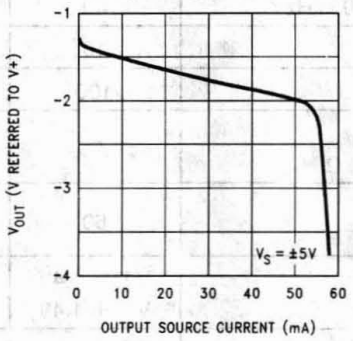
Frequency Response vs R_F
$A_V = -1, R_F = R_G$



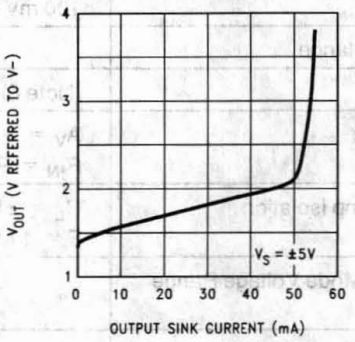
V_{OUT} Referred to Supplies
$V_S = \pm 5V$
$I_{IN} = \pm 100\ \mu A$



LM6104 Output Voltage vs Source Current



LM6104 Output Voltage vs Sink Current



TL/H/11979–3

Applications Information

CURRENT FEEDBACK TOPOLOGY

The small-signal bandwidth of conventional voltage feedback amplifiers is inversely proportional to the closed-loop gain based on the gain-bandwidth concept. In contrast, the current feedback amplifier topology, such as the LM6104, enables a signal bandwidth that is relatively independent of the amplifier's gain (see typical curve Frequency Response vs Closed Loop Gain).

FEEDBACK RESISTOR SELECTION: R_F

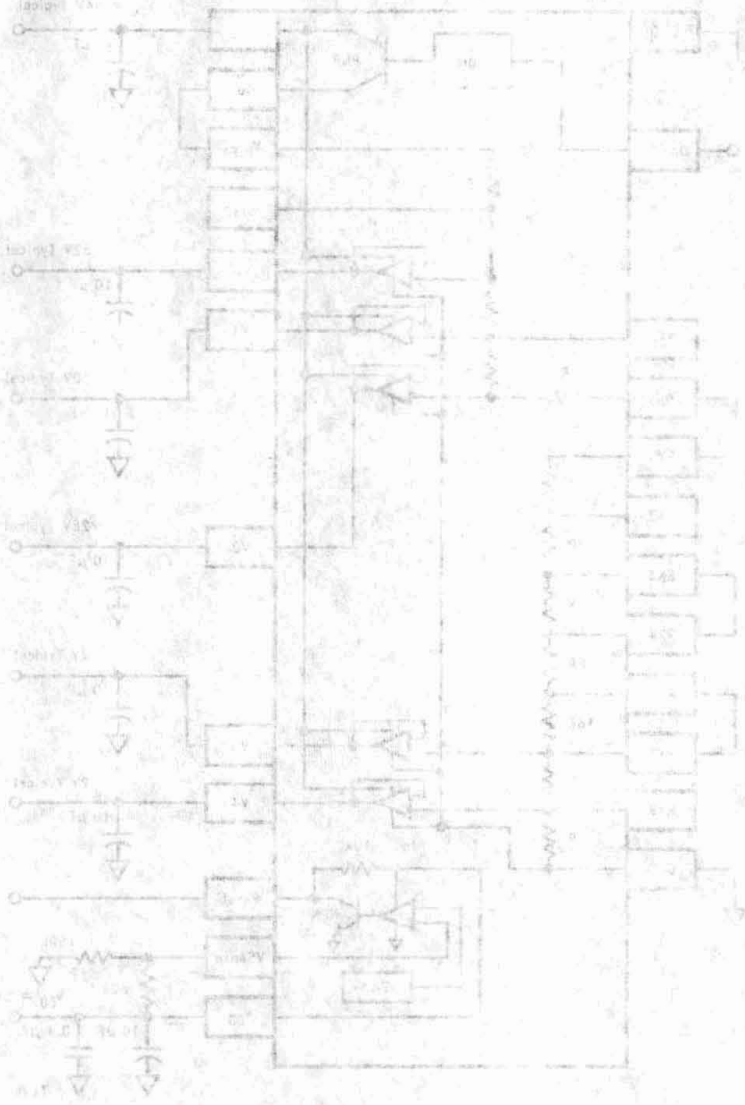
Current feedback amplifier bandwidth and slew rate are controlled by R_F. R_F and the amplifier's internal compensation capacitor set the dominant pole in the frequency response. The amplifier, therefore, always requires a feedback resistor, even in unity gain.

Bandwidth and slew rate are inversely proportional to the value of R_F (see typical curve Frequency Response vs R_F). This makes the amplifier especially easy to compensate for a desired pulse response (see typical curve Large Signal Pulse Response). Increased capacitive load driving capability is also achieved by increasing the value of R_F.

The LM6104 has guaranteed performance with a feedback resistor of 2 kΩ.

CAPACITIVE FEEDBACK

It is common to place a small lead capacitor in parallel with feedback resistance to compensate voltage feedback amplifiers. Do not place a capacitor across R_F to limit the bandwidth of current feedback amplifiers. The dynamic impedance of capacitors in the feedback path of the LM6104, as with any current feedback amplifier, will cause instability.



National Semiconductor

PRELIMINARY

LM8305—STN LCD Display Bias Voltage Source

General Description

The LM8305M contains five buffered voltage sources to provide the voltage ratios required to drive a standard STN LCD display panel using a time-multiplexed voltage waveform to activate, or deactivate, a pixel once every picture frame. The internal resistor array features a binary weighted array to allow the user to select the proper ratio for the display being driven. The user can use an external resistor to set the ratio, if desired.

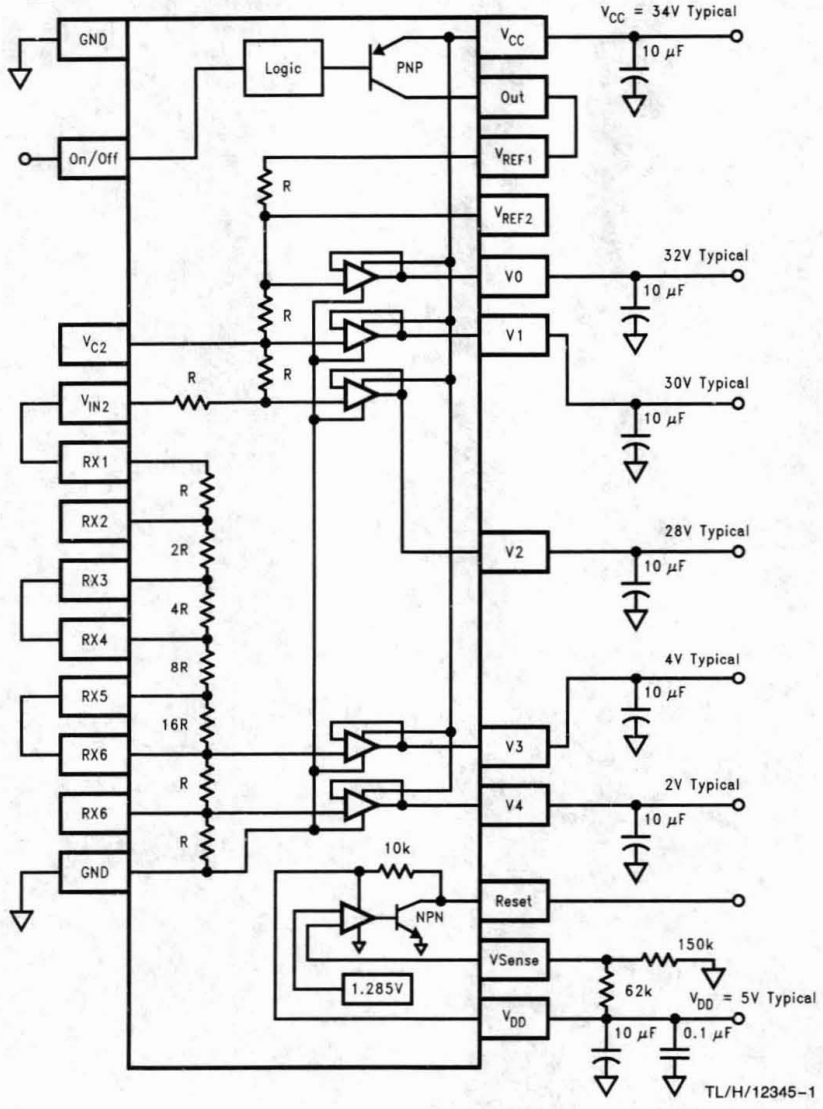
The LM8305 has a maximum operating supply voltage of 50V to support higher multiplexing rates.

The LM8305 also features an internal high side PNP switch, and an independent voltage comparator with an internal bandgap reference.

Features

- High operating voltages, 50V maximum
- Internal resistor array with binary weighting
- Ratios from 1/6 to 1/37
- Optional external resistors
- High-side PNP switch from V_{CC}
- Separate voltage comparator circuit with band-gap voltage reference
- Surface mount 24-pin package

Typical Application



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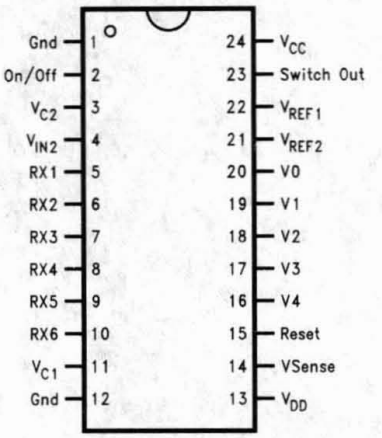
Connection Diagram



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Top View

See NS Package Number M24B
Order Number LM8305M

National Semiconductor

LMC6008
8 Channel Buffer

General Description

The LMC6008 octal buffer is designed for use in an active matrix liquid-crystal display (AMLCD), specifically to buffer the gray-level voltages going to the inputs of the column driver integrated circuits. In an 8-gray-level (512 color) or 16-gray-level (4096 color) AMLCD, the function of the column drivers is to switch the gray-level voltage inputs to the AMLCD columns. Thus, the voltage buffers must be able to drive the column capacitance of the entire display panel. The LMC6008 AC characteristics, including settling time, are specified for a capacitive load of 0.1 μF for this reason.

The LMC6008 contains 4 high-speed buffers and 4 low-power buffers. The high-speed buffers can provide an output current of at least 250 mA (minimum), and the low-power buffers can provide at least 150 mA (minimum). The high-speed buffers are intended to be used for the highest gray-level voltages (V0, V1, V2, V3 in an 8-gray AMLCD). By including the 2 types of buffers, the LMC6008 is able to provide this function while consuming a supply current of only 6.5 mA (maximum). The buffers are a rail-to-rail design, which typically swing to within 30 mV of either supply.

The LMC6008 also contains a standby function which puts the buffer into a high-impedance mode. The supply current in the standby mode is a low 500 μA max. Also, a thermal limit circuit is included to protect the device from overload conditions.

Features

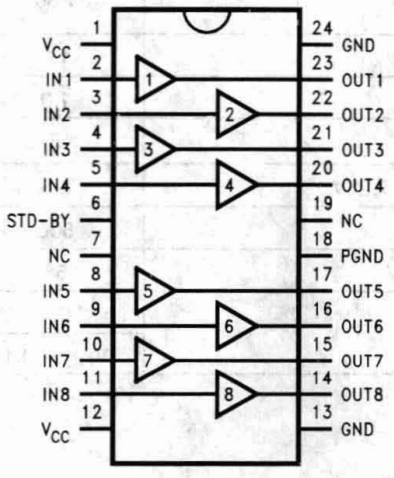
- High Output Current:
  - High Speed Buffers — 250 mA min
  - Low Power Buffers — 150 mA min
- Slew Rate:
  - High Speed Buffers — 1.7 V/μs
  - Low Power Buffers — 0.85V/μs
- Settling Time, C_L = 0.1 μF — 16 μs max
- Wide Input/Output Range — 0.1V to V_{CC} − 0.1V min
- Supply Voltage Range — 5V to 16V
- Supply Current — 6.5 mA max
- Standby Mode Current — 500 μA

Applications

- AMLCD voltage buffering
- Multi-voltage buffering

Connection Diagram

24-Pin SO



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Top View

Note: Buffers 1, 3, 5 and 7 are High Speed and Buffers 2, 4, 6 and 8 are Low Speed.

Ordering Information

Package	Temperature Range −40°C to +85°C	NSC Drawing	Transport Media
24-Pin Surface Mount	LMC6008IM	M24B	Rail
	LMC6008IMX	M24B	Tape & Reel

2

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

ESD Tolerance (Note 2)	2000V
Voltage at Input Pin	$V^+ + 0.4V$, $V^- - 0.4V$
Voltage at Output Pin	$V^+ + 0.4V$, $V^- - 0.4V$
Supply Voltage ($V^+ - V^-$)	16V
Lead Temperature (soldering, 10 sec.)	260°C
Storage Temperature Range	−55°C to +150°C
Junction Temperature (Note 4)	150°C
Power Dissipation (Note 4)	Internally Limited

Operating Ratings (Note 1)

Supply Voltage	$4.5V \le V^+ \le 16V$
Temperature Range	−20°C to +100°C
Thermal Resistance (θ_{JA})	
M Package, 24-Pin Surface Mount	50°C/W

DC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for $T_J = 25°C$, $V_{CC} = 14.5V$ and $R_L = 0$.

Symbol	Parameter	Conditions	Typ (Note 5)	LMC6008 Limit (Note 6)	Units
V_{OS}	Input Offset Voltage	$R_S = 10\ k\Omega$		25	mV max
A_V	$V_O = 10\ V_{PP}$			0.985	V/V
I_B	Input Bias Current			300	nA max
I_{LP}	Peak Load Current	Hi Speed Buffers $V_O = 13\ V_{PP}$		−250	mA max
				+250	mA min
I_{LP}	Peak Load Current	Lo Speed Buffers $V_O = 13\ V_{PP}$		−150	mA max
				+150	mA min
V_{ERR}	Output Voltage Difference (Note 9)		35		mV max
V_{IH}	Standby Logic HIgh Voltage			3.30	V min
V_{IL}	$I_{STANDBY}$ Logic Low Voltage			1.80	V max
I_{IH}	Standby High Input Current			1.0	μA max
I_{IL}	Standby Low Input Current			1.0	μA max
$I_{O\ (STD-BY)}$	Output Leakage Current	V_{STD-BY} = High		5	μA max
I_{CC}	Supply Current	V_{IL} = Low, $V_{IN} = 7.25V$		6.5	mA max
I_{STD-BY}	Standby Current	V_{STD-BY} = High		500	μA max
PSRR	Power Supply Rejection Ratio	$5V < V_{CC} < 14.5V$		55	dB min
V_O	Voltage Output Swing			0.1	V min
				$V_{CC} - 0.1$	V max

AC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for T_J = 25°C, V_{CC} = 14.5V and R_L = 0Ω.

Symbol	Parameter	Conditions	Typ (Note 5)	LMC6008 Limit (Note 6)	Units
SR	Slew Rate	Buffers 1, 3, 5, 7 (Note 3)		1.70	V/μs min
		Buffers 2, 4, 6, 8 (Note 3)		0.85	V/μs min
t_S	Settling Time	(Notes 3, 7)		16	μs max
t_{ON}	Standby Response Time ON			10	μs max
t_{OFF}	Standby Response Time OFF			10	μs max
PBW	Power Bandwidth	V_O = 10 V_{PP} for Hi-Speed V_O = 5 V_{PP} for Lo-Speed (Note 3)		45	KHz min
C_L	Load Capacitance			0.1	μF max

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating ratings indicate conditions for which the device is intended to be functional, but specific performance is not guaranteed. For guaranteed specifications and the test conditions, see the Electrical Characteristics.

Note 2: Human body model, 1.5 kΩ in series with 100 pF.

Note 3: The Load is a series connection of a 0.1 μF capacitor and a 1Ω resistor.

Note 4: The maximum power dissipation is a function of $T_{J(max)}$, θ_{JA}, and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(max)} - T_A)/\theta_{JA}$, where the junction-to-ambient thermal resistance θ_{JA} = 50°C/W. If the maximum allowable power dissipation is exceeded, the thermal limit circuit will limit the die temperature to approximately 160°C. All numbers apply for packages soldered directly into a PC board.

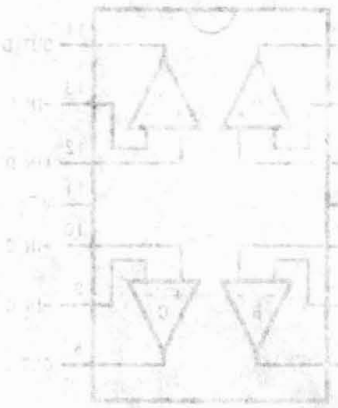
Note 5: Typical Values represent the most likely parametric norm.

Note 6: All limits are guaranteed by testing or statistical analysis.

Note 7: The settling time is measured from the input transition to a point 50 mV of the final value, for both rising and falling transitions. The input swing is 0.5V to 13.5V for buffers 1, 3, 5, 7 and 3.75V to 10.25V for buffers 2, 4, 6, 8. Input rise time should be less than 1 μs.

Note 8: High-Speed Buffers are 1, 3, 5, 7 and Low-Speed Buffers are 2, 4, 6, 8.

Note 9: Output Voltage Difference is the difference between the highest and lowest buffer output voltage when all buffer inputs are at identical voltages.



National Semiconductor

PRELIMINARY

LM6152 Dual and LM6154 Quad High Speed/Low Power 45 MHz Rail-to-Rail I/O Operational Amplifiers

General Description

Using patent pending circuit topologies, the LM6152/54 provides new levels of speed vs power performance in applications where low voltage supplies or power limitations made compromise necessary. With only 1.5 mA/amp supply current, the 45 MHz bandwidth of this device supports new portable applications where higher power devices unacceptably drain battery life.

In addition, the LM6152/54 can be driven by voltages that exceed both power supply rails, thus eliminating concerns over exceeding the common-mode voltage range. The rail-to-rail output swing capability provides the maximum possible dynamic range at the output. This is particularly important when operating on low supply voltages. The LM6152/54 can also drive capacitive loads without oscillating.

Operating on supplies of 1.8V to over 24V, the LM6152/54 is excellent for a very wide range of applications, from battery operated systems with large bandwidth requirements to high speed instrumentation.

Features (For 5V Supply)

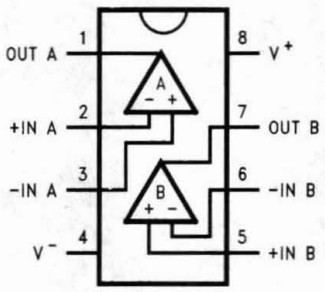
- Rail-to-rail input CMVR — −0.25V to 5.25V (max/min)
- Rail-to-rail output swing — 0.01V to 4.99V (max/min)
- Wide gain-bandwidth: — 45 MHz (typ) @ 50 kHz
- Slew rate — 30 V/μs (typ)
- Low supply current — 1.5/Amp (typ)
- Wide supply range — 1.8V to 24V
- Fast settling time:
  - Gain — 108 dB (typ) with R_L = 10k
- PSRR — 87 dB (typ)

Applications

- Portable high speed instrumentation
- 5V signal conditioning amplifiers/ADC buffers
- Bar code scanners
- Wireless communications

Connection Diagrams

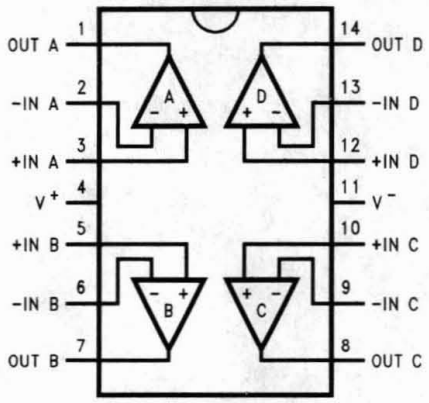
8-Pin DIP/SO



TL/H/12350–1

Top View

14-Pin DIP/SO



TL/H/12350–2

Top View

Ordering Information

Package	Temperature Range	NSC Drawing
	Industrial −40°C to +85°C	
8-Pin Molded DIP	LM6142AIN, LM6142BIN	N08E
8-Pin Small Outline	LM6142AIM, LM6142BIM	M08A
14-Pin Molded DIP	LM6144AIN, LM6144BIN	N14A
14-Pin Small Outline	LM6144AIM, LM6144BIM	M14A

National Semiconductor

LM6161/LM6261/LM6361
High Speed Operational Amplifier

General Description

The LM6161 family of high-speed amplifiers exhibits an excellent speed-power product in delivering 300 V/μs and 50 MHz unity gain stability with only 5 mA of supply current. Further power savings and application convenience are possible by taking advantage of the wide dynamic range in operating supply voltage which extends all the way down to +5V.

These amplifiers are built with National's VIP™ (Vertically Integrated PNP) process which provides fast PNP transistors that are true complements to the already fast NPN devices. This advanced junction-isolated process delivers high speed performance without the need for complex and expensive dielectric isolation.

Features

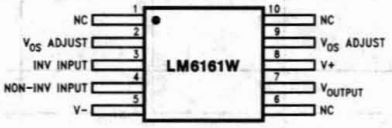
- High slew rate — 300 V/μs
- High unity gain freq — 50 MHz
- Low supply current — 5 mA
- Fast settling — 120 ns to 0.1%
- Low differential gain — <0.1%
- Low differential phase — 0.1°
- Wide supply range — 4.75V to 32V
- Stable with unlimited capacitive load
- Well behaved; easy to apply

Applications

- Video amplifier
- High-frequency filter
- Wide-bandwidth signal conditioning
- Radar
- Sonar

Connection Diagrams

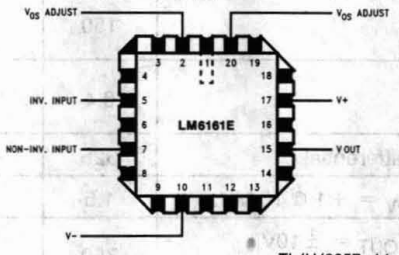
10-Lead Flatpak



TL/H/9057–13

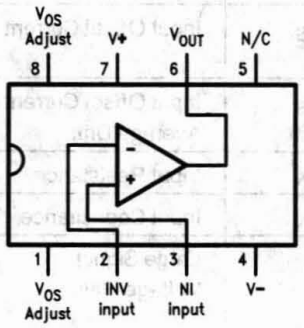
See NS Package Number W10A

20-Lead LCC



TL/H/9057–14

See NS Package Number E20A



TL/H/9057–5

See NS Package Number J08A, N08E or M08A

Temperature Range			Package	NSC Drawing
Military −55°C ≤ T_A ≤ +125°C	Industrial −25°C ≤ T_A ≤ +85°C	Commercial 0°C ≤ T_A ≤ +70°C		
	LM6261N	LM6361N	8-Pin Molded DIP	N08E
LM6161J/883 5962-8962101PA		LM6361J	8-Pin Ceramic DIP	J08A
	LM6261M	LM6361M	8-Pin Molded Surface Mt.	M08A
LM6161E/883 5962-89621012A			20-Lead LCC	E20A
LM6161W/883 5962-8962101HA			10-Pin Ceramic Flatpak	W10A

2

Absolute Maximum Ratings (Note 12)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage ($V^+ - V^-$)	36V
Differential Input Voltage (Note 8)	±8V
Common-Mode Voltage Range (Note 10)	($V^+ - 0.7V$) to ($V^- - 7V$)
Output Short Circuit to GND (Note 1)	Continuous
Soldering Information	
Dual-In-Line Package (N, J)	
Soldering (10 sec.)	260°C
Small Outline Package (M)	
Vapor Phase (60 sec.)	215°C
Infrared (15 sec.)	220°C

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.

Storage Temp Range	−65°C to +150°C
Max Junction Temperature	150°C
ESD Tolerance (Notes 6 and 7)	±700V

Operating Ratings (Note 12)

Temperature Range (Note 2)	
LM6161	$-55°C \le T_J \le +125°C$
LM6261	$-25°C \le T_J \le +85°C$
LM6361	$0°C \le T_J \le +70°C$
Supply Voltage Range	4.75V to 32V

DC Electrical Characteristics

The following specifications apply for Supply Voltage = ±15V, $V_{CM} = 0$, $R_L \ge 100\ k\Omega$ and $R_S = 50\Omega$ unless otherwise noted. **Boldface** limits apply for $T_J = T_{MIN}$ to T_{MAX}; all other limits $T_J = 25°C$.

Symbol	Parameter	Conditions	Typ	LM6161 Limit (Notes 3, 11)	LM6261 Limit (Note 3)	LM6361 Limit (Note 3)	Units
V_{OS}	Input Offset Voltage		5	7 **10**	7 **9**	20 **22**	mV Max
V_{OS} Drift	Input Offset Voltage Average Drift		10				µV/°C
I_b	Input Bias Current		2	3 **6**	3 **5**	5 **6**	µA Max
I_{OS}	Input Offset Current		150	350 **800**	350 **600**	1500 **1900**	nA Max
I_{OS} Drift	Input Offset Current Average Drift		0.4				nA/°C
R_{IN}	Input Resistance	Differential	325				kΩ
C_{IN}	Input Capacitance	$A_V = +1$ @ 10 MHz	1.5				pF
A_{VOL}	Large Signal Voltage Gain	$V_{OUT} = \pm 10V$, $R_L = 2\ k\Omega$ (Note 9)	750	550 **300**	550 **400**	400 **350**	V/V Min
		$R_L = 10\ k\Omega$ (Note 9)	2900				V/V
V_{CM}	Input Common-Mode Voltage Range	Supply = ±15V	+14.0	+13.9 **+13.8**	+13.9 **+13.8**	+13.8 **+13.7**	Volts Min
			−13.2	−12.9 **−12.7**	−12.9 **−12.7**	−12.8 **−12.7**	Volts Min
		Supply = +5V (Note 4)	4.0	3.9 **3.8**	3.9 **3.8**	3.8 **3.7**	Volts Min
			1.8	2.0 **2.2**	2.0 **2.2**	2.1 **2.2**	Volts Max
CMRR	Common-Mode Rejection Ratio	$-10V \le V_{CM} \le +10V$	94	80 **74**	80 **76**	72 **70**	dB Min
PSRR	Power Supply Rejection Ratio	$\pm 10V \le V^{\pm} \le \pm 16V$	90	80 **74**	80 **76**	72 **70**	dB Min
V_O	Output Voltage Swing	Supply = ±15V and $R_L = 2\ k\Omega$	+14.2	+13.5 **+13.3**	+13.5 **+13.3**	+13.4 **+13.3**	Volts Min
			−13.4	−13.0 **−12.7**	−13.0 **−12.8**	−12.9 **−12.8**	Volts Min

DC Electrical Characteristics (Continued)

The following specifications apply for Supply Voltage = ±15V, V_{CM} = 0, $R_L \geq 100\ k\Omega$ and $R_S = 50\Omega$ unless otherwise noted. **Boldface** limits apply for $T_J = T_{MIN}$ to T_{MAX}; all other limits T_J = 25°C.

Symbol	Parameter	Conditions	Typ	LM6161 Limit (Notes 3, 11)	LM6261 Limit (Note 3)	LM6361 Limit (Note 3)	Units
V_O (Continued)	Output Voltage Swing (Continued)	Supply = +5V and R_L = 2 kΩ (Note 4)	4.2	3.5 **3.3**	3.5 **3.3**	3.4 **3.3**	Volts Min
			1.3	1.7 **2.0**	1.7 **1.9**	1.8 **1.9**	Volts Max
	Output Short Circuit Current	Source	65	30 **20**	30 **25**	30 **25**	mA Min
		Sink	65	30 **20**	30 **25**	30 **25**	mA Min
I_S	Supply Current		5.0	6.5 **6.8**	6.5 **6.7**	6.8 **6.9**	mA Max

AC Electrical Characteristics

The following specifications apply for Supply Voltage = ±15V, V_{CM} = 0, $R_L \geq 100\ k\Omega$ and $R_S = 50\Omega$ unless otherwise noted. **Boldface** limits apply for $T_J = T_{MIN}$ to T_{MAX}; all other limits T_J = 25°C.

Symbol	Parameter	Conditions	Typ	LM6161 Limit (Notes 3, 11)	LM6261 Limit (Note 3)	LM6361 Limit (Note 3)	Units
GBW	Gain-Bandwidth Product	@ f = 20 MHz	50	40 **30**	40 **35**	35 **32**	MHz Min
		Supply = ±5V	35				MHz
SR	Slew Rate	A_V = +1 (Note 8)	300	200 **180**	200 **180**	200 **180**	V/μs Min
		Supply = ±5V (Note 8)	200				V/μs
PBW	Power Bandwidth	V_{OUT} = 20 V_{PP}	4.5				MHz
t_S	Settling Time	10V Step to 0.1% A_V = −1, R_L = 2 kΩ	120				ns
ϕm	Phase Margin		45				Deg
A_D	Differential Gain	NTSC, A_V = +4	<0.1				%
ϕD	Differential Phase	NTSC, A_V = +4	0.1				Deg
e_{np-p}	Input Noise Voltage	f = 10 kHz	15				$nV/\sqrt{Hz}$
i_{np-p}	Input Noise Current	f = 10 kHz	1.5				$pA/\sqrt{Hz}$

Note 1: Continuous short-circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 150°C.

Note 2: The typical junction-to-ambient thermal resistance of the molded plastic DIP (N) is 105°C/W, the molded plastic SO (M) package is 155°C/W, and the cerdip (J) package is 125°C/W. All numbers apply for packages soldered directly into a printed circuit board.

Note 3: Limits are guaranteed by testing or correlation.

Note 4: For single supply operation, the following conditions apply: V^+ = 5V, V^- = 0V, V_{CM} = 2.5V, V_{OUT} = 2.5V. Pin 1 & Pin 8 (Vos Adjust) are each connected to Pin 4 (V^-) to realize maximum output swing. This connection will degrade V_{OS}, V_{OS} Drift, and Input Voltage Noise.

Note 5: $C_L \leq 5$ pF.

Note 6: In order to achieve optimum AC performance, the input stage was designed without protective clamps. Exceeding the maximum differential input voltage results in reverse breakdown of the base-emitter junction of one of the input transistors and probable degradation of the input parameters (especially Vos, Ios, and Noise).

Note 7: The average voltage that the weakest pin combinations (those involving Pin 2 or Pin 3) can withstand and still conform to the datasheet limits. The test circuit used consists of the human body model of 100 pF in series with 1500Ω.

Note 8: V_{IN} = 8V step. For supply = ±5V, V_{IN} = 5V step.

Note 9: Voltage Gain is the total output swing (20V) divided by the input signal required to produce that swing.

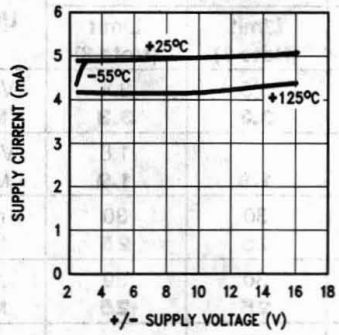
Note 10: The voltage between V^+ and either input pin must not exceed 36V.

Note 11: A military RETS electrical test specification is available on request. At the time of printing, the RETS6161X specs complied with all **Boldface** limits in this column.

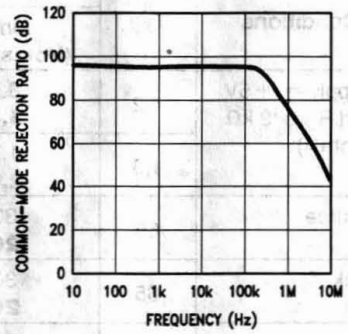
Note 12: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed.

Typical Performance Characteristics (R_L = 10 kΩ, T_A = 25°C unless otherwise specified)

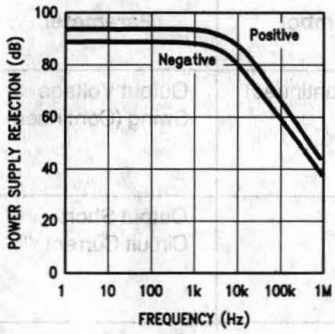
Supply Current vs Supply Voltage



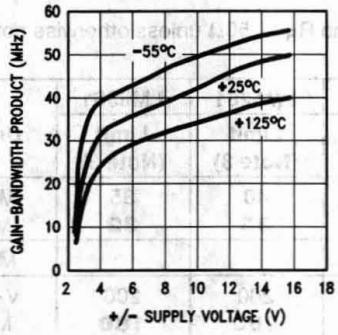
Common-Mode Rejection Ratio



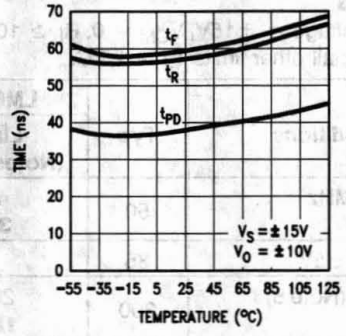
Power Supply Rejection Ratio



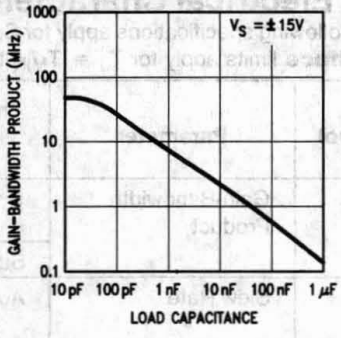
Gain-Bandwidth Product



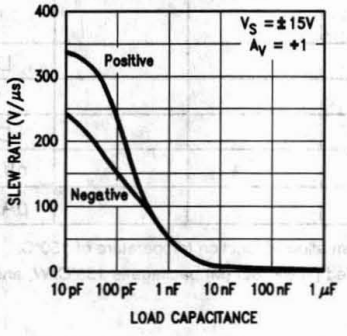
Propagation Delay Rise and Fall Times



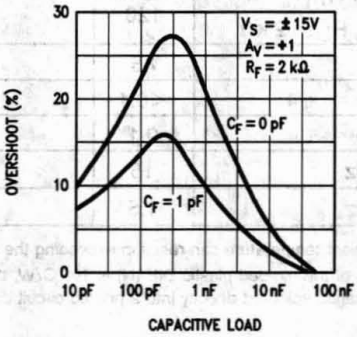
Gain-Bandwidth Product vs Load Capacitance



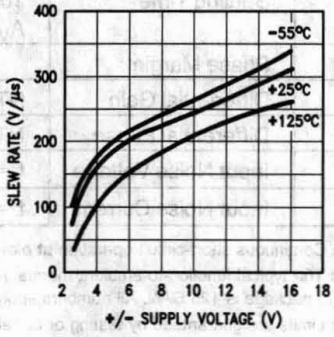
Slew Rate vs Load Capacitance



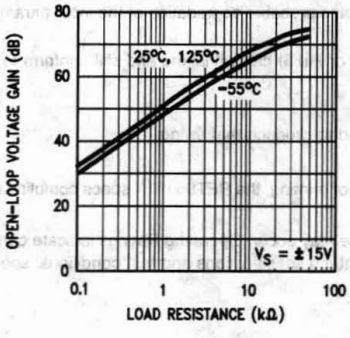
Overshoot vs Capacitive Load



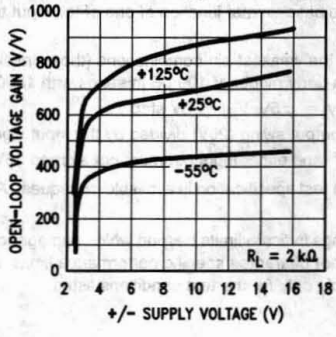
Slew Rate



Voltage Gain vs Load Resistance



Gain vs Supply Voltage

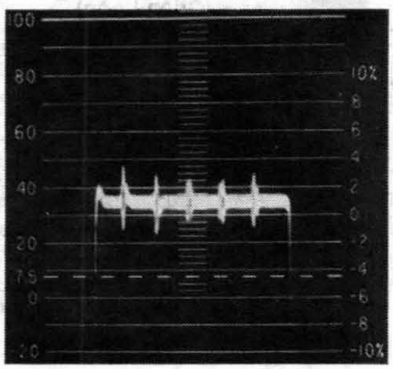


TL/H/9057–6

Typical Performance Characteristics

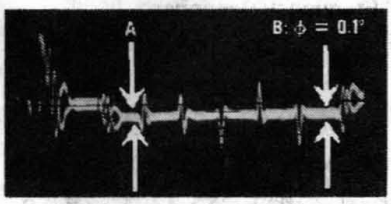
(R_L = 10 kΩ, T_A = 25°C unless otherwise specified) (Continued)

Differential Gain (Note)



TL/H/9057–7

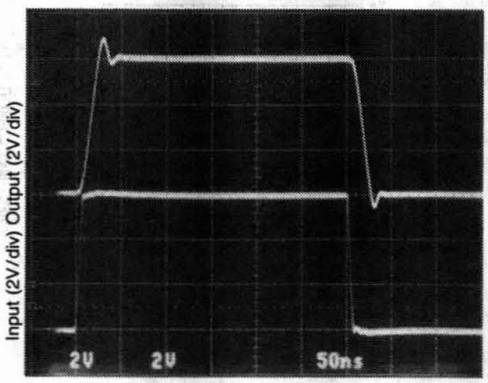
Differential Phase (Note)



TL/H/9057–8

Note: Differential gain and differential phase measured for four series LM6361 op amps configured as unity-gain followers, in series with an LM6321 buffer. Error added by LM6321 is negligible. Test performed using Tektronix Type 520 NTSC test system.

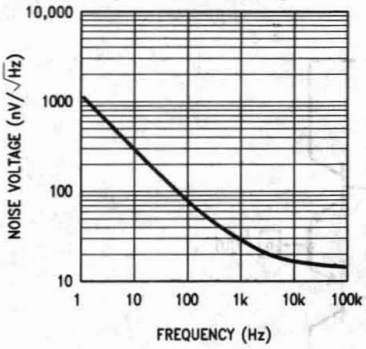
Step Response; Av = +1



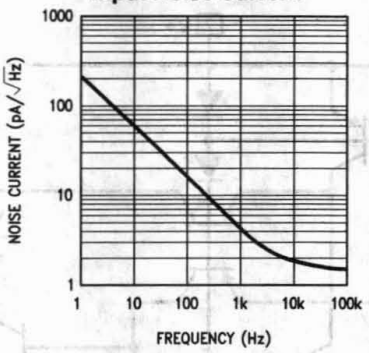
(50 ns/div)

TL/H/9057–1

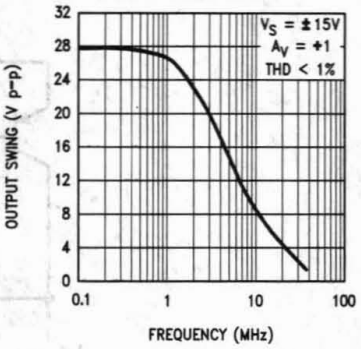
Input Noise Voltage



Input Noise Current



Power Bandwidth

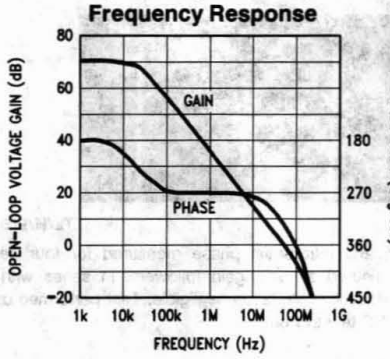


TL/H/9057–9

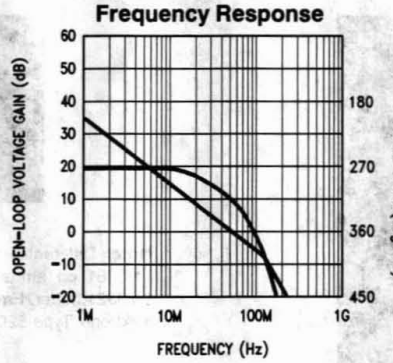
Typical Performance Characteristics

(R_L = 10 kΩ, T_A = 25°C unless otherwise specified) (Continued)

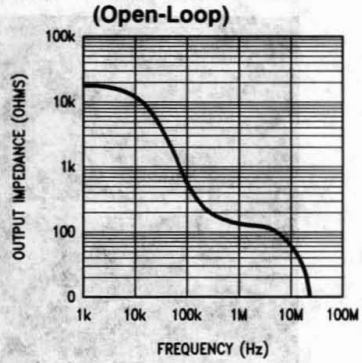
Open-Loop Frequency Response



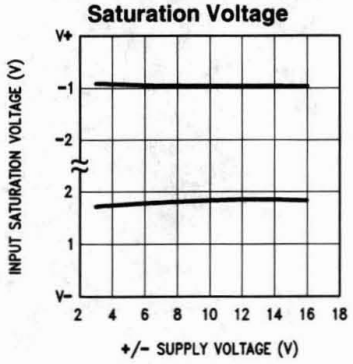
Open-Loop Frequency Response



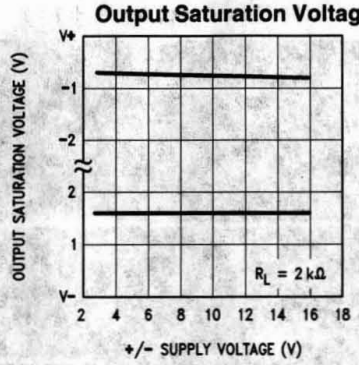
Output Impedence (Open-Loop)



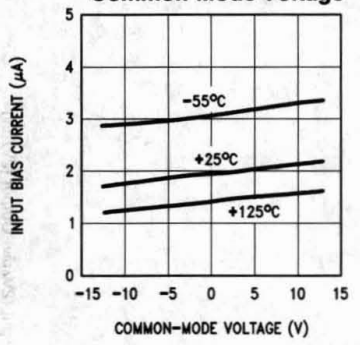
Common-Mode Input Saturation Voltage



Output Saturation Voltage

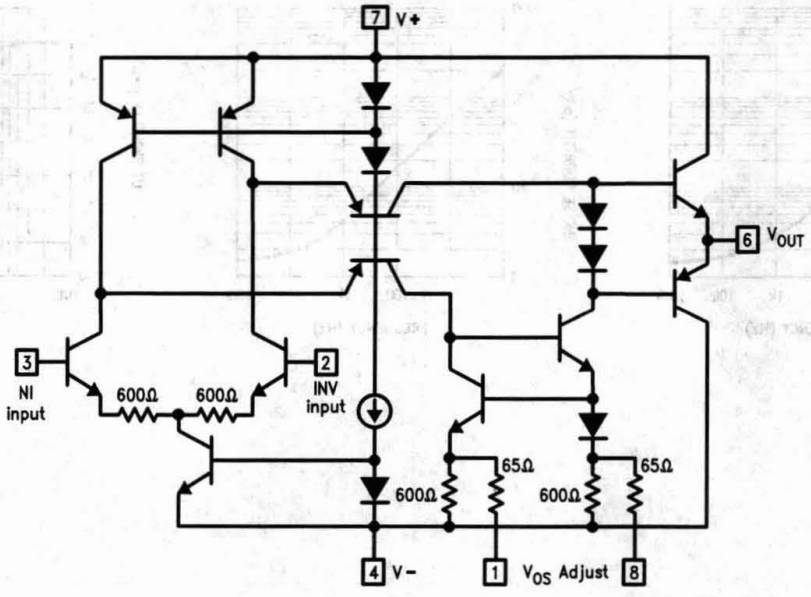


Bias Current vs Common-Mode Voltage



TL/H/9057–12

Simplified Schematic



TL/H/9057–3

Applications Tips

The LM6361 has been compensated for unity-gain operation. Since this compensation involved adding emitter-degeneration resistors to the op amp's input stage, the open-loop gain was reduced as the stability increased. Gain error due to reduced A_{VOL} is most apparent at high gains; thus, for gains between 5 and 25, the less-compensated LM6364 should be used, and the uncompensated LM6365 is appropriate for gains of 25 or more. The LM6361, LM6364, and LM6365 have the same high slew rate, regardless of their compensation.

The LM6361 is unusually tolerant of capacitive loads. Most op amps tend to oscillate when their load capacitance is greater than about 200 pF (especially in low-gain circuits). The LM6361's compensation is effectively increased with load capacitance, reducing its bandwidth and increasing its stability.

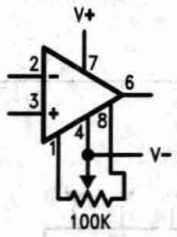
Power supply bypassing is not as critical for the LM6361 as it is for other op amps in its speed class. Bypassing will, however, improve the stability and transient response and is recommended for every design. 0.01 μF to 0.1 μF ceramic capacitors should be used (from each supply "rail" to ground); if the device is far away from its power supply source, an additional 2.2 μF to 10 μF of tantalum may provide extra noise reduction.

Keep all leads short to reduce stray capacitance and lead inductance, and make sure ground paths are low-impedance, especially where heavier currents will be flowing. Stray capacitance in the circuit layout can cause signal coupling across adjacent nodes and can cause gain to unintentionally vary with frequency.

Breadboarded circuits will work best if they are built using generic PC boards with a good ground plane. If the op amps are used with sockets, as opposed to being soldered into the circuit, the additional input capacitance may degrade circuit performance.

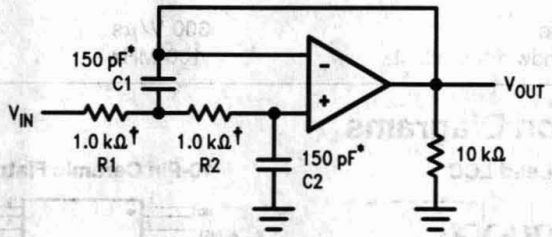
Typical Applications

Offset Voltage Adjustment



TL/H/9057–4

1 MHz Low-Pass Filter



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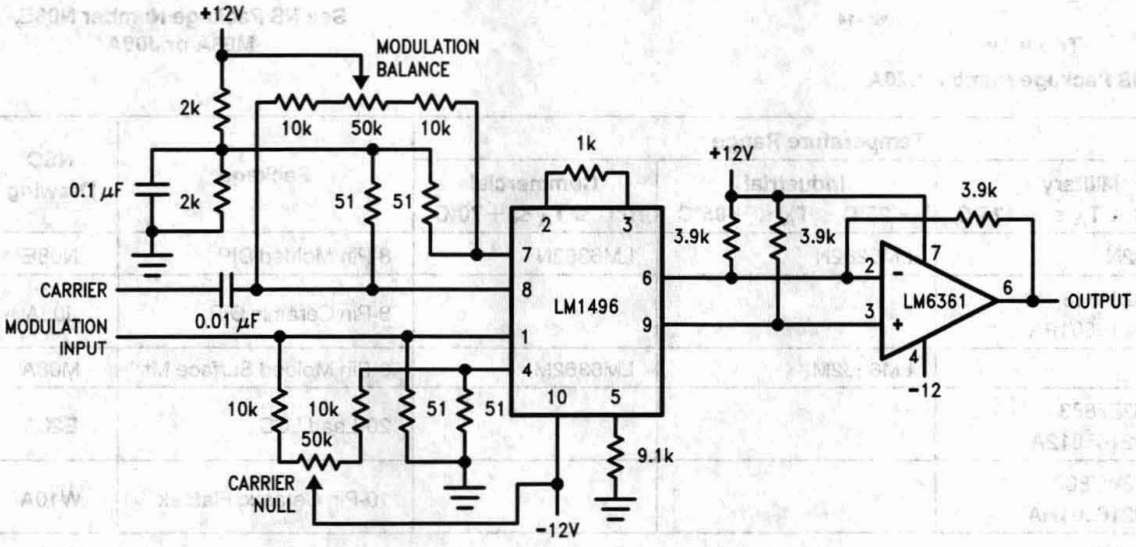
†1% tolerance

*Matching determines filter precision

$f_c = (2\pi \sqrt{(R1\ R2\ C1\ C2)})^{-1}$

Modulator with Differential-to-Single-Ended Converter



TL/H/9057–11

National Semiconductor

LM6162/LM6262/LM6362
High Speed Operational Amplifier

General Description

The LM6362 family of high-speed amplifiers exhibits an excellent speed-power product, delivering 300 V/μs and 100 MHz gain-bandwidth product (stable for gains as low as +2 or −1) with only 5 mA of supply current. Further power savings and application convenience are possible by taking advantage of the wide dynamic range in operating supply voltage which extends all the way down to +5V.

These amplifiers are built with National's VIP™ (Vertically Integrated PNP) process which provides fast transistors that are true complements to the already fast NPN devices. This advanced junction-isolated process delivers high speed performance without the need for complex and expensive dielectric isolation.

Features

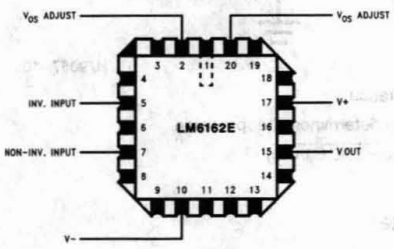
- High slew rate 300 V/μs
- High gain-bandwidth product 100 MHz
- Low supply current 5 mA
- Fast settling time 120 ns to 0.1%
- Low differential gain <0.1%
- Low differential phase <0.1°
- Wide supply range 4.75V to 32V
- Stable with unlimited capacitive load
- Well behaved; easy to apply

Applications

- Video amplifier
- Wide-bandwidth signal conditioning for image processing (FAX, scanners, laser printers)
- Hard disk drive preamplifier
- Error amplifier for high-speed switching regulator

Connection Diagrams

20-Lead LCC

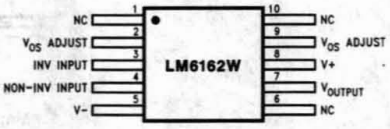


TL/H/11061–14

Top View

See NS Package Number E20A

10-Pin Ceramic Flatpak



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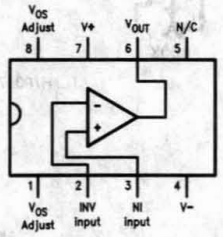
Top View

See NS Package Number W10A



TL/H/11061–2

See NS Package Number N08E, M08A or J08A

Temperature Range			Package	NSC Drawing
Military $-55°C \le T_A \le +125°C$	**Industrial** $-25°C \le T_A \le +85°C$	**Commercial** $0°C \le T_A \le +70°C$		
LM6162N	LM6262N	LM6362N	8-Pin Molded DIP	N08E
LM6162J/883 5962-9216501PA			8-Pin Ceramic DIP	J08A
	LM6262M	LM6362M	8-Pin Molded Surface Mt.	M08A
LM6162E/883 5962-92165012A			20-Lead LCC	E20A
LM6162W/883 5962-9216501HA			10-Pin Ceramic Flatpak	W10A

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage ($V^+ - V^-$)	36V
Differential Input Voltage (Note 2)	±8V
Common-Mode Input Voltage (Note 3)	$(V^+ - 0.7V)$ to $(V^- - 0.3V)$
Output Short Circuit to GND (Note 4)	Continuous
Soldering Information	
Dual-In-Line Package (N)	
Soldering (10 seconds)	260°C
Small Outline Package (M)	
Vapor Phase (60 seconds)	215°C
Infrared (15 seconds)	220°C

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.

Storage Temperature Range	$-65°C \le T_J \le +150°C$
Max Junction Temperature	150°C
ESD Tolerance (Note 5)	±1100V

Operating Ratings

Temperature Range (Note 6)	
LM6162	$-55°C \le T_J \le +125°C$
LM6262	$-25°C \le T_J \le +85°C$
LM6362	$0°C \le T_J \le +70°C$
Supply Voltage Range	4.75V to 32V

DC Electrical Characteristics

These limits apply for supply voltage = ±15V, V_{CM} = 0V, and $R_L \ge 100\ k\Omega$, unless otherwise specified. Limits in standard typeface are for $T_A = T_J = 25°C$; limits in **boldface type** apply over the **Operating Temperature Range**.

Symbol	Parameter	Conditions	Typical (Note 7)	LM6162 Limit (Note 8)	LM6262 Limit (Note 8)	LM6362 Limit (Note 8)	Units
V_{OS}	Input Offset Voltage		±3	±5 **±8**	±5 **±8**	±13 **±15**	mV max
$\frac{\Delta V_{OS}}{\Delta Temp}$	Input Offset Voltage Average Drift		7				µV/°C
I_{bias}	Input Bias Current		2.2	3 **6**	3 **5**	4 **6**	µA max
I_{OS}	Input Offset Current		±150	±350 **±800**	±350 **±600**	±1500 **±1900**	nA max
$\frac{\Delta I_{OS}}{\Delta Temp}$	Input Offset Current Average Drift		0.3				nA/°C
R_{IN}	Input Resistance	Differential	180				kΩ
C_{IN}	Input Capacitance		2.0				pF
A_{VOL}	Large Signal Voltage Gain	$V_{OUT} = \pm 10V$, $R_L = 2\ k\Omega$ (Note 9)	1400	1000 **500**	1000 **700**	800 **650**	V/V min
		$R_L = 10\ k\Omega$	6500				V/V
V_{CM}	Input Common-Mode Voltage Range	Supply = ±15V	+14.0	+13.9 **+13.8**	+13.9 **+13.8**	+13.8 **+13.7**	V min
			−13.2	−12.9 **−12.7**	−12.9 **−12.7**	−12.9 **−12.8**	V max
		Supply = +5V (Note 10)	4.0	3.9 **3.8**	3.9 **3.8**	3.8 **3.7**	V min
			1.6	1.8 **2.0**	1.8 **2.0**	1.9 **2.0**	V max
CMRR	Common-Mode Rejection Ratio	$-10V \le V_{CM} \le +10V$	100	83 **79**	83 **79**	76 **74**	dB min
PSRR	Power Supply Rejection Ratio	$\pm 10V \le V_S \le \pm 16V$	93	83 **79**	83 **79**	76 **74**	dB min
V_O	Output Voltage Swing	Supply = ±15V, $R_L = 2\ k\Omega$	+14.2	+13.5 **+13.3**	+13.5 **+13.3**	+13.4 **13.3**	V min
			−13.4	−13.0 **−12.7**	−13.0 **−12.8**	−12.9 **−12.8**	V max

2

DC Electrical Characteristics (Continued)

These limits apply for supply voltage = ±15V, V_{CM} = 0V, and $R_L \geq 100\ k\Omega$, unless otherwise specified. Limits in standard typeface are for $T_A = T_J = 25°C$; limits in **boldface type** apply over the **Operating Temperature Range**.

Symbol	Parameter	Conditions	Typical (Note 7)	LM6162 Limit (Note 8)	LM6262 Limit (Note 8)	LM6362 Limit (Note 8)	Units
V_O	Output Voltage Swing	Supply = +5V and R_L = 2 kΩ (Note 10)	4.2	3.5 **3.3**	3.5 **3.3**	3.4 **3.3**	V min
			1.3	1.7 **2.0**	1.7 **1.9**	1.8 **1.9**	V max
I_{OSC}	Output Short Circuit Current	Sourcing	65	30 **20**	30 **25**	30 **25**	mA min
		Sinking	65	30 **20**	30 **25**	30 **25**	mA min
I_S	Supply Current		5.0	6.5 **6.8**	6.5 **6.7**	6.8 **6.9**	mA max

AC Electrical Characteristics

These limits apply for supply voltage = ±15V, V_{CM} = 0V, $R_L \geq 100\ k\Omega$, and $C_L \leq 5$ pF, unless otherwise specified. Limits in standard typeface are for $T_A = T_J = 25°C$; limits in **boldface type** apply over the **Operating Temperature Range**.

Symbol	Parameter	Conditions	Typical (Note 7)	LM6162 Limit (Note 8)	LM6262 Limit (Note 8)	LM6362 Limit (Note 8)	Units
GBW	Gain-Bandwidth Product	f = 20 MHz	100	80 **55**	80 **65**	75 **65**	MHz min
		Supply = ±5V	70				MHz
SR	Slew Rate	A_V = +2 (Note 11)	300	200 **180**	200 **180**	200 **180**	V/μs min
		Supply = ±5V	200				V/μs
PBW	Power Bandwidth	V_{OUT} = 20 V_{PP}	4.5				MHz
t_s	Settling Time	10V step, to 0.1% A_V = −1, R_L = 2 kΩ	100				ns
ϕ_m	Phase Margin	A_V = +2	45				deg
	Differential Gain	NTSC, A_V = +2	<0.1				%
	Differential Phase	NTSC, A_V = +2	<0.1				deg
e_n	Input Noise Voltage	f = 10 kHz	10				nV/√Hz
i_n	Input Noise Current	f = 10 kHz	1.2				pA/√Hz

Note 1: Absolute maximum ratings indicate limits beyond which damage to the component may occur. Electrical specifications do not apply when operating the device beyond its rated operating conditions.

Note 2: The ESD protection circuitry between the inputs will begin to conduct when the differential input voltage reaches 8V.

Note 3: a) In addition, the voltage between the V^+ pin and either input pin must not exceed 36V.
b) When the voltage applied to an input pin is driven more than 0.3V below the negative supply pin voltage, a substrate diode begins to conduct. Current through this pin must then be kept less than 20 mA to limit damage from self-heating.

Note 4: Although the output current is internally limited, continuous short-circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 150°C.

Note 5: This value is the average voltage that the weakest pin combinations can withstand and still conform to the datasheet limits. The test circuit used consists of the human body model, 100 pF in series with 1500Ω.

Note 6: The typical thermal resistance, junction-to-ambient, of the molded plastic DIP (N package) is 105°C/W. For the molded plastic SO (M package), use 155°C/W. All numbers apply for packages soldered directly into a printed circuit board.

Note 7: Typical values are for T_J = 25°C, and represent the most likely parametric norm.

Note 8: Limits are guaranteed, by testing or correlation.

Note 9: Voltage Gain is the total output swing (20V) divided by the magnitude of the input signal required to produce that swing.

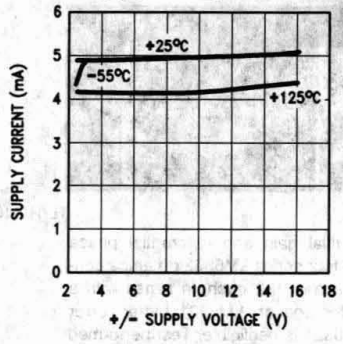
Note 10: For single-supply operation, the following conditions apply: V^+ = 5V, V^- = 0V, V_{CM} = 2.5V, V_{OUT} = 2.5V. Pin 1 and Pin 8 (V_{OS} Adjust pins) are each connected to pin 4 (V^-) to realize maximum output swing. This connection will increase the offset voltage.

Note 11: V_{IN} = 10V step. For ±5V supplies, V_{IN} = 1V step.

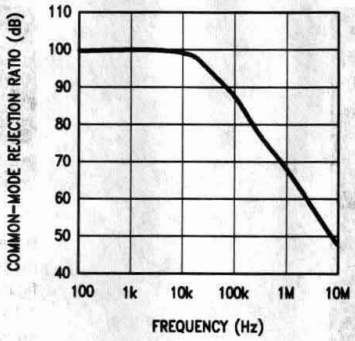
Note 12: A military RETS electrical test specification is available on request.

Typical Performance Characteristics $R_L = 10\ k\Omega$, $T_A = 25°C$ unless otherwise noted

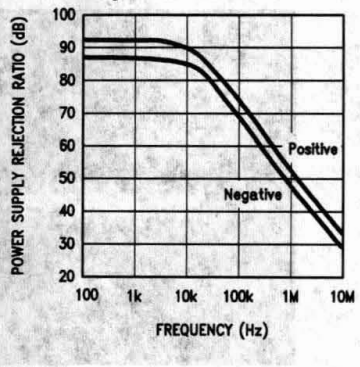
Supply Current vs Supply Voltage



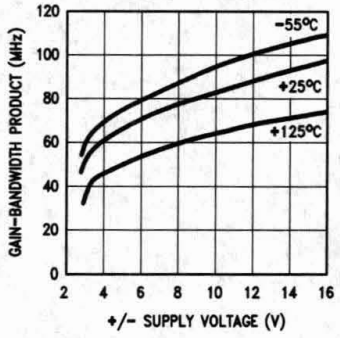
Common-Mode Rejection Ratio



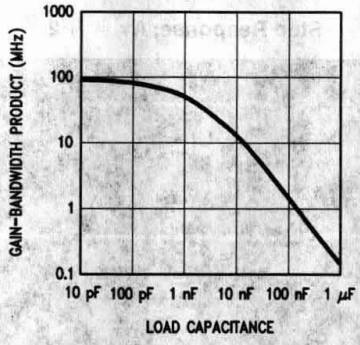
Power Supply Rejection Ratio



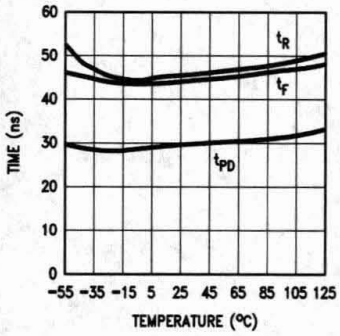
Gain-Bandwidth Product vs Supply Voltage



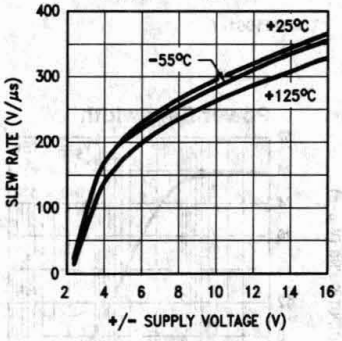
Gain-Bandwidth Product vs Load Capacitance



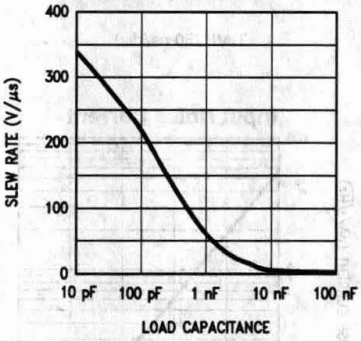
Propagation Delay, Rise and Fall Times



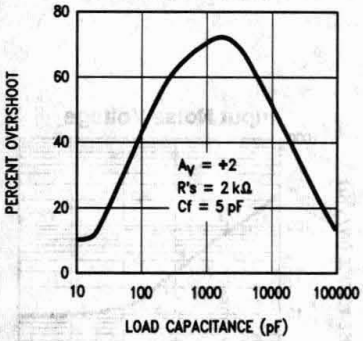
Slew Rate vs Supply Voltage



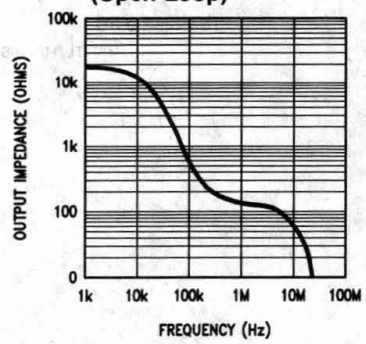
Slew Rate vs Load Capacitance



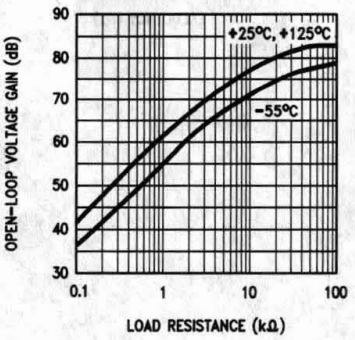
Overshoot vs Load Capacitance



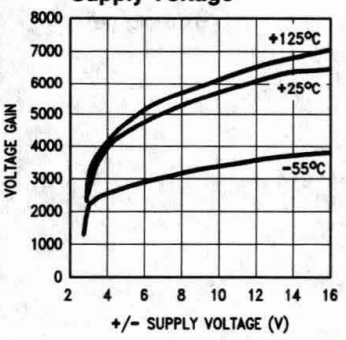
Output Impedance (Open-Loop)



Voltage Gain vs Load Resistance



Voltage Gain vs Supply Voltage



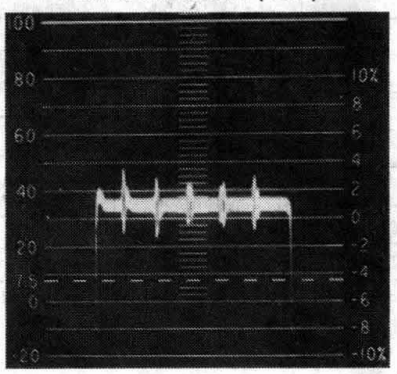
TL/H/11061–3

2

Typical Performance Characteristics (Continued)

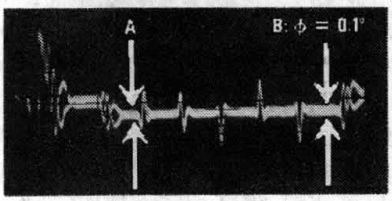
R_L = 10 kΩ, T_A = 25°C unless otherwise noted

Differential Gain (Note)



TL/H/11061–4

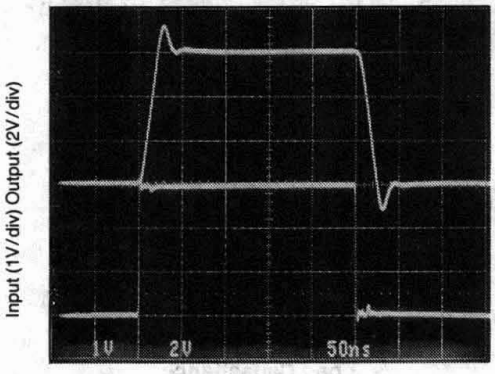
Differential Phase (Note)



TL/H/11061–5

Note: Differential gain and differential phase measured for four series LM6362 op amps configured with gain of +2 each, in series with a 1:16 attenuator and an LM6321 buffer. Error added by LM6321 is negligible. Test performed using Tektronix Type 520 NTSC test system.

Step Response; Av = +2



TIME (50 ns/div)

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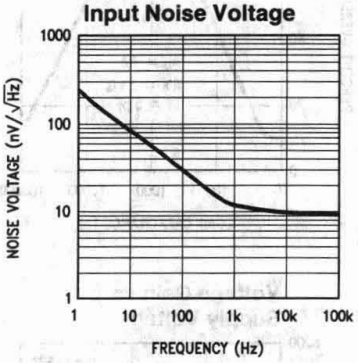
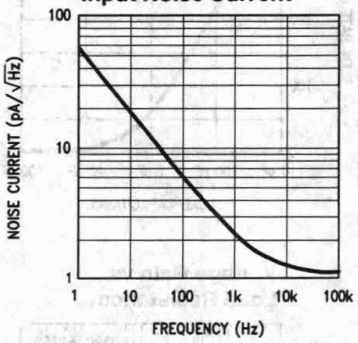
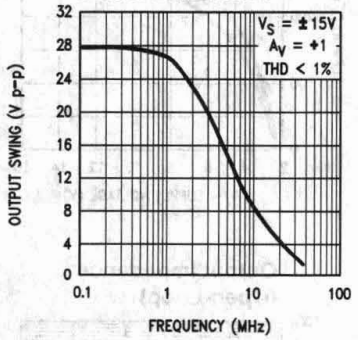
Input Noise Voltage



Input Noise Current



Power Bandwidth

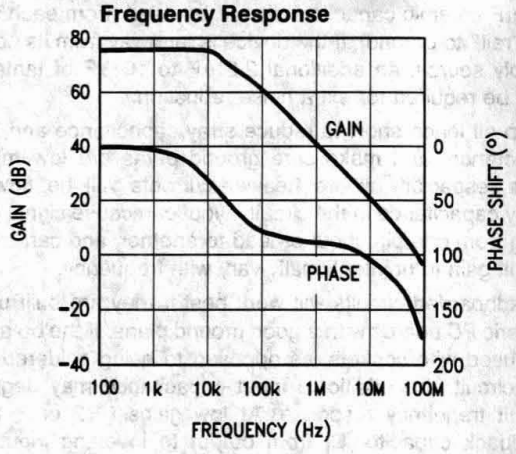


TL/H/11061–7

Typical Performance Characteristics (Continued)

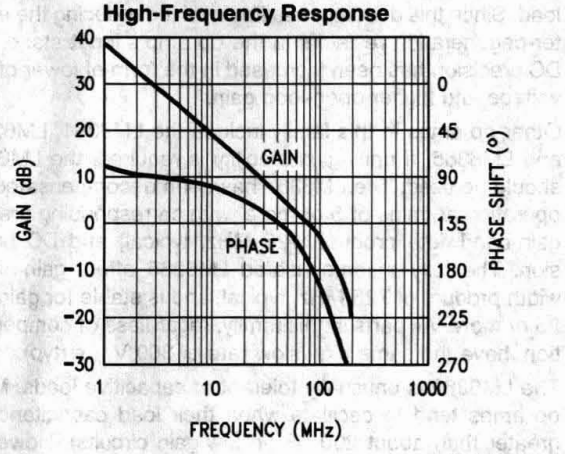
R_L = 10 kΩ, T_A = 25°C unless otherwise noted

Open-Loop Frequency Response



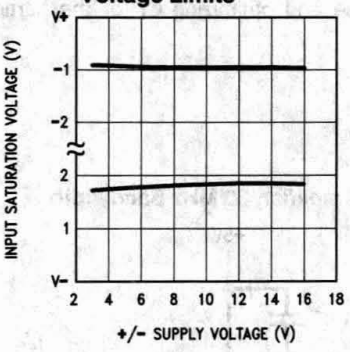
TL/H/11061–8

Open-Loop High-Frequency Response

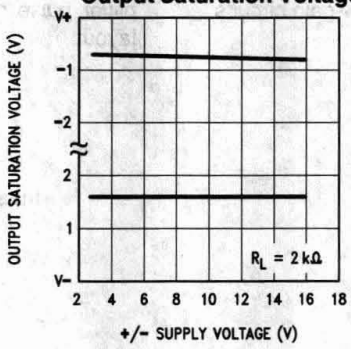


TL/H/11061–9

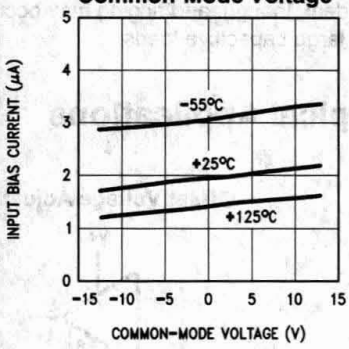
Common-Mode Input Voltage Limits



Output Saturation Voltage

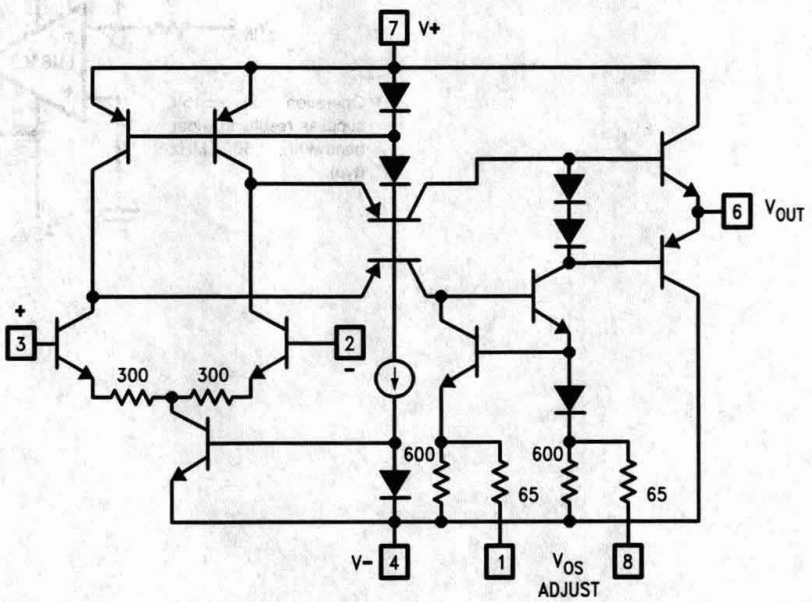


Bias Current vs Common-Mode Voltage



TL/H/11061–10

Simplified Schematic



TL/H/11061–1

Application Tips

The LM6362 has been decompensated for a wider gain-bandwidth product than the LM6361. However, the LM6362 still offers stability at gains of 2 (and −1) or greater over the specified ranges of temperature, power supply voltage, and load. Since this decompensation involved reducing the emitter-degeneration resistors in the op amp's input stage, the DC precision has been increased in the form of lower offset voltage and higher open-loop gain.

Other op amps in this family include the LM6361, LM6364, and LM6365. If unity-gain stability is required, the LM6361 should be used. The LM6364 has been decompensated for operation at gains of 5 or more, with corresponding greater gain-bandwidth product (125 MHz, typical) and DC precision. The fully-uncompensated LM6365 offers gain-bandwidth product of 725 MHz, typical, and is stable for gains of 25 or more. All parts in this family, regardless of compensation, have the same high slew rate of 300 V/μs (typ).

The LM6362 is unusually tolerant of capacitive loads. Most op amps tend to oscillate when their load capacitance is greater than about 200 pF (in low-gain circuits). However, load capacitance on the LM6362 effectively increases its compensation capacitance, thus slowing the op amp's response and reducing its bandwidth. The compensation is not ideal, though, and ringing may occur in low-gain circuits with large capacitive loads.

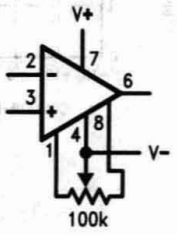
Power supply bypassing is not as critical for LM6362 as it is for other op amps in its speed class. However, bypassing will improve the stability and transient response of the LM6362, and is recommended for every design. 0.01 μF to 0.1 μF ceramic capacitors should be used (from each supply "rail" to ground); if the device is far away from its power supply source, an additional 2.2 μF to 10 μF of tantalum may be required for extra noise reduction.

Keep all leads short to reduce stray capacitance and lead inductance, and make sure ground paths are low-impedance, especially where heavier currents will be flowing. Stray capacitance in the circuit layout can cause signal coupling from one pin, input or lead to another, and can cause circuit gain to unintentionally vary with frequency.

Breadboarded circuits will work best if they are built using generic PC boards with a good ground plane. If the op amps are used with sockets, as opposed to being soldered into the circuit, the additional input capacitance may degrade circuit frequency response. At low gains (+2 or −1), a feedback capacitor C_f from output to inverting input will compensate for the phase lag caused by capacitance at the inverting input. Typically, values from 2 pF to 5 pF work well; however, best results can be obtained by observing the amplifier pulse response and optimizing C_f for the particular layout.

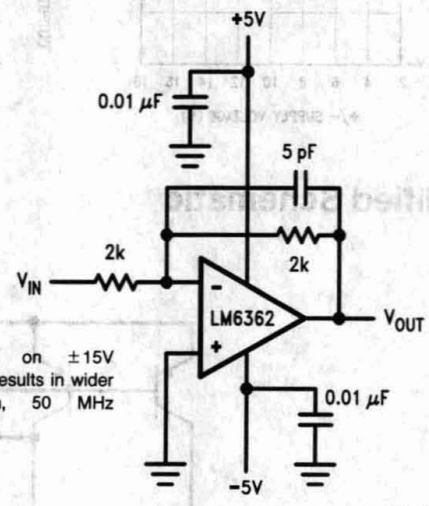
Typical Applications

Offset Voltage Adjustment



TL/H/11061–11

Inverting Amplifier, 30 MHz Bandwidth



Operation on ±15V supplies results in wider bandwidth, 50 MHz (typ).

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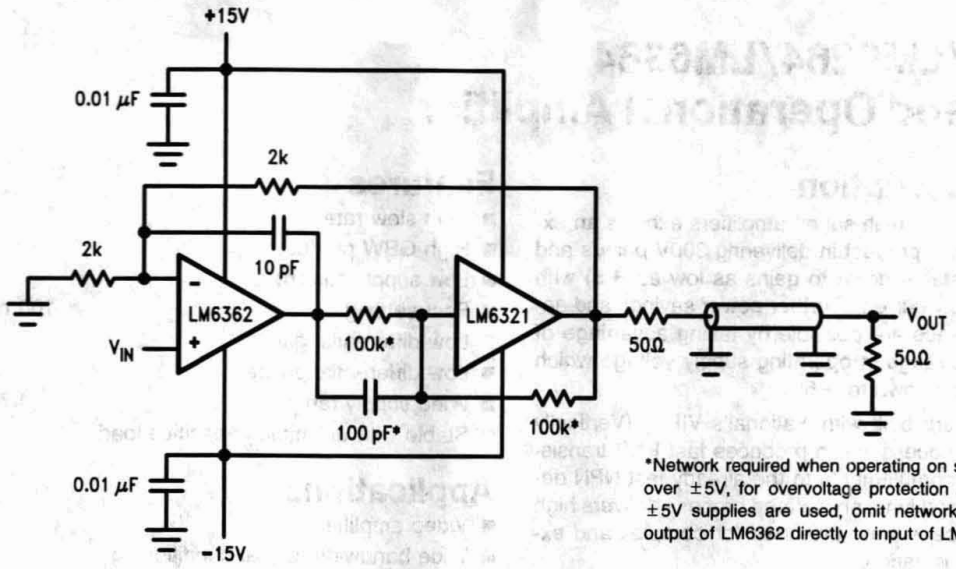
Typical Applications (Continued)

Video Cable Driver



*Network required when operating on supply voltage over ±5V, for overvoltage protection of LM6321. If ±5V supplies are used, omit network and connect output of LM6362 directly to input of LM6321.

TL/H/11061–13

National Semiconductor

LM6164/LM6264/LM6364 High Speed Operational Amplifier

General Description

The LM6164 family of high-speed amplifiers exhibits an excellent speed-power product in delivering 300V per μs and 175 MHz GBW (stable down to gains as low as +5) with only 5 mA of supply current. Further power savings and application convenience are possible by taking advantage of the wide dynamic range in operating supply voltage which extends all the way down to +5V.

These amplifiers are built with National's VIP™ (Vertically Integrated PNP) process which produces fast PNP transistors that are true complements to the already fast NPN devices. This advanced junction-isolated process delivers high speed performance without the need for complex and expensive dielectric isolation.

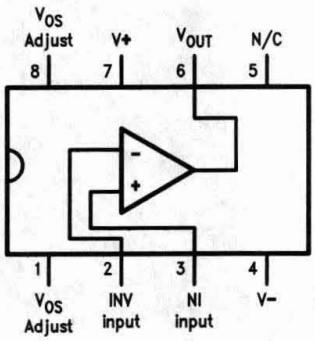
Features

■ High slew rate	300 V/μs
■ High GBW product	175 MHz
■ Low supply current	5 mA
■ Fast settling	100 ns to 0.1%
■ Low differential gain	<0.1%
■ Low differential phase	<0.1°
■ Wide supply range	4.75V to 32V
■ Stable with unlimited capacitive load	

Applications

- Video amplifier
- Wide-bandwidth signal conditioning
- Radar
- Sonar

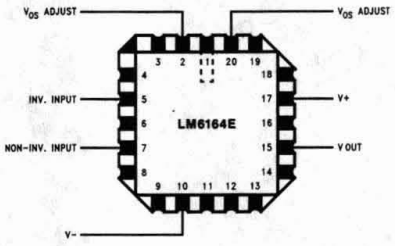
Connection Diagrams



TL/H/9153-8

NS Package Number J08A, M08A or N08E

20-Lead LCC

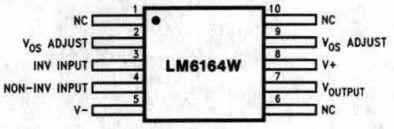


TL/H/9153-14

Top View

NS Package Number E20A

10-Lead Flatpak



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Top View

NS Package Number W10A

Temperature Range			Package	NSC Drawing
Military $-55°C \le T_A \le +125°C$	**Industrial** $-25°C \le T_A \le +85°C$	**Commercial** $0°C \le T_A \le +70°C$		
	LM6264N	LM6364N	8-Pin Molded DIP	N08E
LM6164J/883 5962-8962401PA			8-Pin Ceramic DIP	J08A
		LM6364M	8-Pin Molded Surface Mt.	M08A
LM6164E/883 5962-89624012A			20-Lead LCC	E20A
LM6164W/883 5962-8962401HA			10-Pin Ceramic Flatpak	W10A

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage ($V^+ - V^-$)	36V
Differential Input Voltage (Note 6)	±8V
Common-Mode Input Voltage (Note 10)	$(V^+ - 0.7V)$ to $(V^- - 7V)$
Output Short Circuit to Gnd (Note 1)	Continuous
Soldering Information	
Dual-In-Line Package (N, J)	
Soldering (10 sec.)	260°C
Small Outline Package (M)	
Vapor Phase (60 sec.)	215°C
Infrared (15 sec.)	220°C

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.

Storage Temperature Range	−65°C to +150°C
Max Junction Temperature (Note 2)	150°C
ESD Tolerance (Notes 6 & 7)	±700V

Operating Ratings

Temperature Range (Note 2)	
LM6164	$-55°C \le T_J \le +125°C$
LM6264	$-25°C \le T_J \le +85°C$
LM6364	$0°C \le T_J \le +70°C$
Supply Voltage Range	4.75V to 32V

DC Electrical Characteristics

The following specifications apply for Supply Voltage = ±15V, V_{CM} = 0, $R_L \ge 100\ k\Omega$ and $R_S = 50\Omega$ unless otherwise noted. **Boldface** limits apply for $T_A = T_J = T_{MIN}$ to T_{MAX}; all other limits $T_A = T_J = 25°C$.

Symbol	Parameter	Conditions	Typ	LM6164 Limit (Notes 3, 11)	LM6264 Limit (Note 3)	LM6364 Limit (Note 3)	Units
V_{OS}	Input Offset Voltage		2	4 **6**	4 **6**	9 **11**	mV max
V_{OS} Drift	Input Offset Voltage Average Drift		6				µV/°C
I_b	Input Bias Current		2.5	3 **6**	3 **5**	5 **6**	µA max
I_{OS}	Input Offset Current		150	350 **800**	350 **600**	1500 **1900**	mA max
I_{OS} Drift	Input Offset Current Average Drift		0.3				nA/°C
R_{IN}	Input Resistance	Differential	100				kΩ
C_{IN}	Input Capacitance		3.0				pF
A_{VOL}	Large Signal Voltage Gain	$V_{OUT} = \pm 10V$, $R_L = 2\ k\Omega$ (Note 9)	2.5	1.8 **0.9**	1.8 **1.2**	1.3 **1.1**	V/mV min
		$R_L = 10\ k\Omega$	9				
V_{CM}	Input Common-Mode Voltage Range	Supply = ±15V	+14.0	+13.9 **+13.8**	+13.9 **+13.8**	+13.8 **+13.7**	V min
			−13.5	−13.3 **−13.1**	−13.3 **−13.1**	−13.2 **−13.1**	V min
		Supply = +5V (Note 4)	4.0	3.9 **3.8**	3.9 **3.8**	3.8 **3.7**	V min
			1.5	1.7 **1.9**	1.7 **1.9**	1.8 **1.9**	V max
CMRR	Common-Mode Rejection Ratio	$-10V \le V_{CM} \le +10V$	105	86 **80**	86 **82**	80 **78**	dB min
PSRR	Power Supply Rejection Ratio	$\pm 10V \le V\pm \le \pm 16V$	96	86 **80**	86 **82**	80 **78**	dB min

DC Electrical Characteristics

The following specifications apply for Supply Voltage = ±15V, V_{CM} = 0, $R_L \geq 100\ k\Omega$ and $R_S = 50\Omega$ unless otherwise noted. **Boldface** limits apply for $T_A = T_J = T_{MIN}$ to T_{MAX}; all other limits $T_A = T_J = 25°C$. (Continued)

Symbol	Parameter	Conditions	Typ	LM6164 Limit (Notes 3, 11)	LM6264 Limit (Note 3)	LM6364 Limit (Note 3)	Units
V_O	Output Voltage Swing	Supply = +5V and R_L = 2 kΩ	+14.2	+13.5 **+13.3**	+13.5 **+13.3**	+13.4 **+13.3**	V min
			−13.4	−13.0 **−12.7**	−13.0 **−12.8**	−12.9 **−12.8**	V min
		Supply = +5V and R_L = 2 kΩ (Note 9)	4.2	3.5 **3.3**	3.5 **3.3**	3.4 **3.3**	V min
			1.3	1.7 **2.0**	1.7 **1.9**	1.8 **1.9**	V max
	Output Short Circuit Current	Source	65	30 **20**	30 **25**	30 **25**	mA min
		Sink	65	30 **20**	30 **25**	30 **25**	mA min
I_S	Supply Current		5.0	6.5 **6.8**	6.5 **6.7**	6.8 **6.9**	mA min

AC Electrical Characteristics

The following specifications apply for Supply Voltage = ±15V, V_{CM} = 0, $R_L \geq 100\ k\Omega$ and $R_S = 50\Omega$ unless otherwise noted. **Boldface** limits apply for $T_A = T_J = T_{MIN}$ to T_{MAX}; all other limits $T_A = T_J = 25°C$.

Symbol	Parameter	Conditions	Typ	LM6164 Limit (Notes 3, 11)	LM6264 Limit (Note 3)	LM6364 Limit (Note 3)	Units
GBW	Gain-Bandwidth Product	F = 20 MHz	175	140 **100**	140 **120**	120 **100**	MHz min
		Supply = ±5V	120				
SR	Slew Rate	A_V = +5 (Note 8)	300	200 **180**	200 **180**	200 **180**	V/μs min
		Supply = ±5V	200				
PBW	Power Bandwidth	V_{OUT} = 20 V_{PP}	4.5				MHz
T_S	Settling Time	10V Step to 0.1% A_V = −4, R_L = 2 kΩ	100				ns
ϕ_m	Phase Margin	A_V = +5	45				Deg
A_D	Differential Gain	NTSC, A_V = +10	<0.1				%
ϕ_D	Differential Phase	NTSC, A_V = +10	<0.1				Deg
e_{np-p}	Input Noise Voltage	F = 10 kHz	8				$nV/\sqrt{Hz}$
i_{np-p}	Input Noise Current	F = 10 kHz	1.5				$pA/\sqrt{Hz}$

Note 1: Continuous short-circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 150°C.

Note 2: The typical junction-to-ambient thermal resistance of the molded plastic DIP (N) is 105°C/Watt, the molded plastic SO (M) package is 155°C/Watt, and the cerdip (J) package is 125°C/Watt. All numbers apply for packages soldered directly into a printed circuit board.

Note 3: Limits are guaranteed by testing or correlation.

Note 4: For single supply operation, the following conditions apply: V+ = 5V, V− = 0V, V_{CM} = 2.5V, V_{OUT} = 2.5V. Pin 1 & Pin 8 (V_{OS} Adjust) are each connected to Pin 4 (V−) to realize maximum output swing. This connection will degrade V_{OS}.

Note 5: $C_L \leq 5$ pF.

Note 6: In order to achieve optimum AC performance, the input stage was designed without protective clamps. Exceeding the maximum differential input voltage results in reverse breakdown of the base-emitter junction of one of the input transistors and probable degradation of the input parameters (especially V_{OS}, I_{OS}, and Noise).

Note 7: The average voltage that the weakest pin combinations (those involving Pin 2 or Pin 3) can withstand and still conform to the datasheet limits. The test circuit used consists of the human body model of 100 pF in series with 1500Ω.

Note 8: V_{IN} = 4V step. For supply = ±5V, V_{IN} = 1V step.

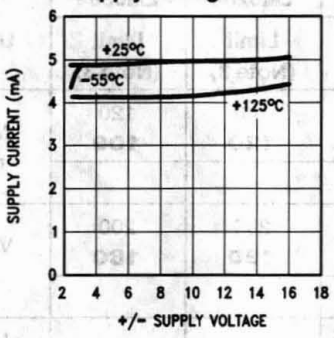
Note 9: Voltage Gain is the total output swing (20V) divided by the input signal required to produce that swing.

Note 10: The voltage between V+ and either input pin must not exceed 36V.

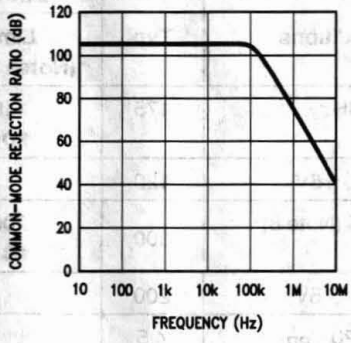
Note 11: A military RETS electrical test specification is available on request. At the time of printing, the LM6164J/883 RETS spec complied with the **Boldface** limits in this column. The LM6164J/883 may also be procured as Standard Military Drawing #5962-8962401PA.

Typical Performance Characteristics (R_L = 10 kΩ, T_A = 25°C unless otherwise specified)

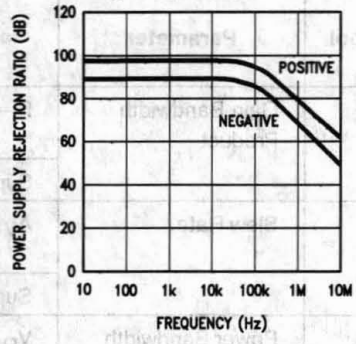
Supply Current vs Supply Voltage



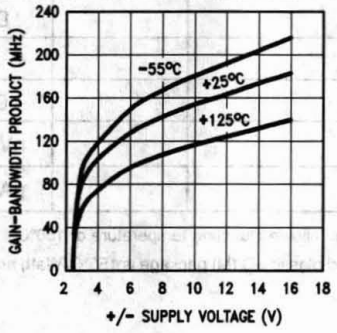
Common-Mode Rejection Ratio



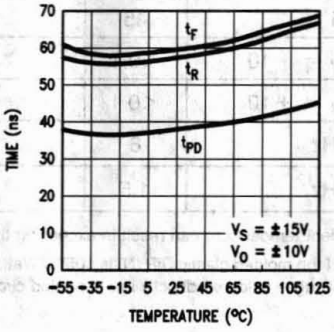
Power Supply Rejection Ratio



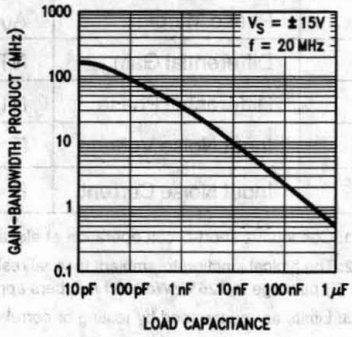
Gain-Bandwidth Product



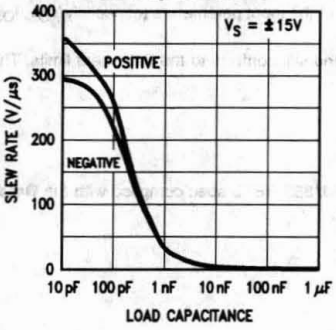
Propagation Delay Rise and Fall Time



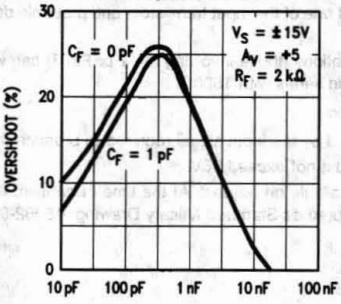
Gain-Bandwidth Product vs Load Capacitance



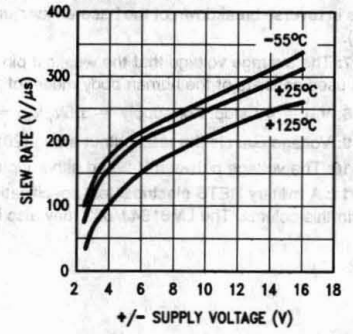
Slew Rate vs Load Capacitance



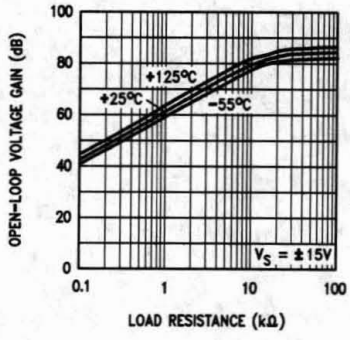
Overshoot vs Load Capacitance



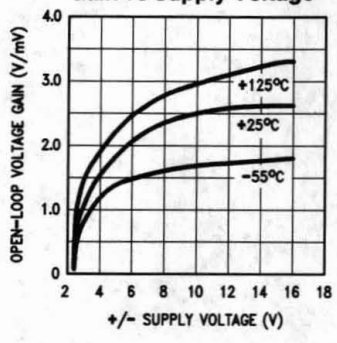
Slew Rate



Voltage Gain vs Load Resistance



Gain vs Supply Voltage

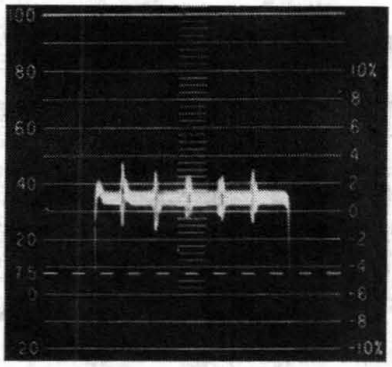


TL/H/9153–5

Typical Performance Characteristics

(R_L = 10 kΩ, T_A = 25°C unless otherwise specified) (Continued)

Differential Gain (Note)



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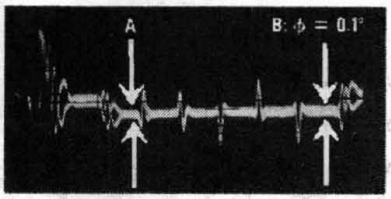
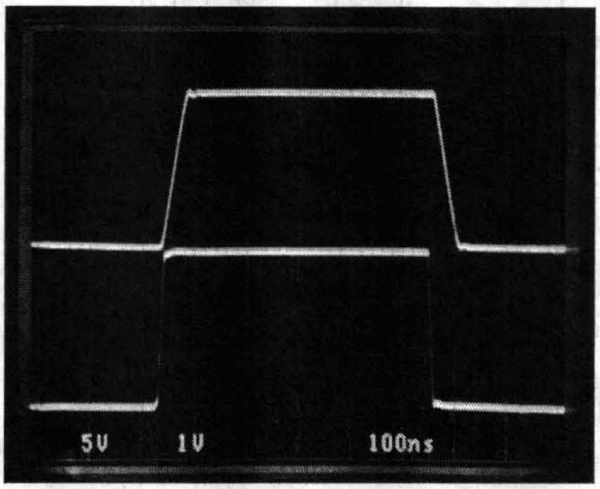
Differential Phase (Note)



TL/H/9153–7

Note: Differential gain and differential phase measured for four series LM6364 op amps in series with an LM6321 buffer. Error added by LM6321 is negligible. Test performed using Tektronix Type 520 NTSC test system. Configured with a gain of +5 (each output attenuated by 80%)

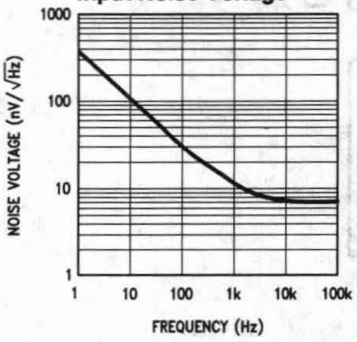
Step Response; Av = +5



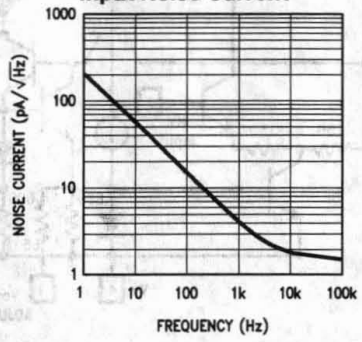
TL/H/9153–1

TIME (50 ns/div)

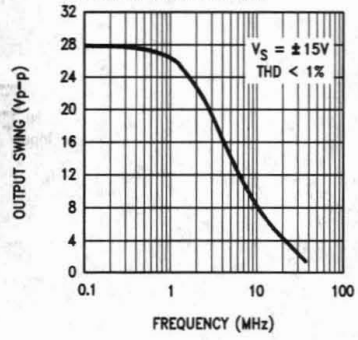
Input Noise Voltage



Input Noise Current



Power Bandwidth



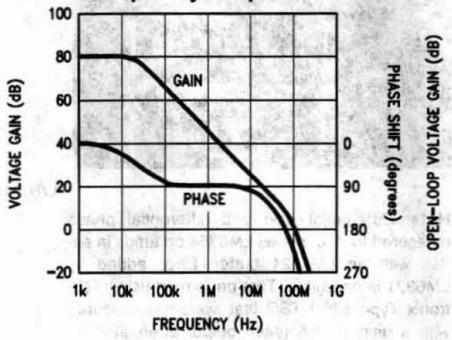
TL/H/9153–9

2

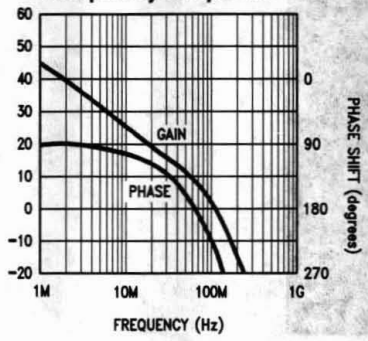
Typical Performance Characteristics

(R_L = 10 kΩ, T_A = 25°C unless otherwise specified) (Continued)

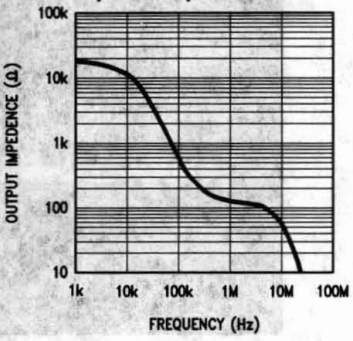
Open-Loop Frequency Response



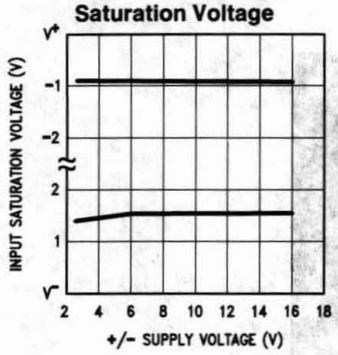
Open-Loop Frequency Response



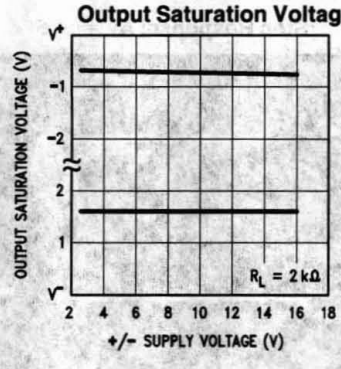
Output Resistance Open-Loop



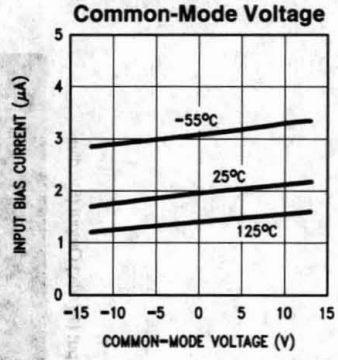
Common-Mode Input Saturation Voltage



Output Saturation Voltage

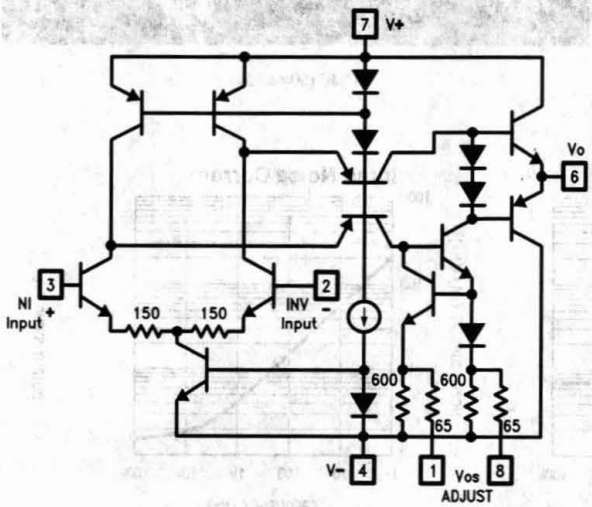


Bias Current vs Common-Mode Voltage



TL/H/9153–13

Simplified Schematic



TL/H/9153–3

Applications Tips

The LM6364 has been compensated for gains of 5 or greater (over specified ranges of temperature, power supply voltage, and load). Since this compensation involved adding emitter-degeneration resistors in the op amp's input stage, the open-loop gain was reduced as the stability increased. Gain error due to reduced A_{VOL} is most apparent at high gains; thus, the uncompensated LM6365 is appropriate for gains of 25 or more. If unity-gain operation is desired, the LM6361 should be used. The LM6361, LM6364, and LM6365 have the same high slew rate (typically 300 V/μs), regardless of their compensation.

The LM6364 is unusually tolerant of capacitive loads. Most op amps tend to oscillate when their load capacitance is greater than about 200 pF (in low-gain circuits). However, load capacitance on the LM6364 effectively increases its compensation capacitance, thus slowing the op amp's response and reducing its bandwidth. The compensation is not ideal, though, and ringing or oscillation may occur in low-gain circuits with large capacitive loads. To overcompensate the LM6364 for operation at gains less than 5, a series resistor-capacitor network should be added between the input pins (as shown in the Typical Applications, Noise Gain Compensation) so that the high-frequency noise gain rises to at least 5.

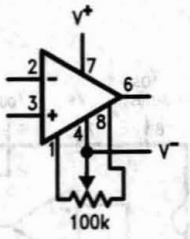
Power supply bypassing will improve the stability and transient response of the LM6364, and is recommended for every design. 0.01 μF to 0.1 μF ceramic capacitors should be used (from each supply "rail" to ground); if the device is far away from its power supply source, an additional 2.2 μF to 10 μF (tantalum) may be required for extra noise reduction.

Keep all leads short to reduce stray capacitance and lead inductance, and make sure ground paths are low-impedance, especially where heavier currents will be flowing. Stray capacitance in the circuit layout can cause signal coupling between adjacent nodes, so that circuit gain unintentionally varies with frequency.

Breadboarded circuits will work best if they are built using generic PC boards with a good ground plane. If the op amps are used with sockets, as opposed to being soldered into the circuit, the additional input capacitance may degrade circuit performance.

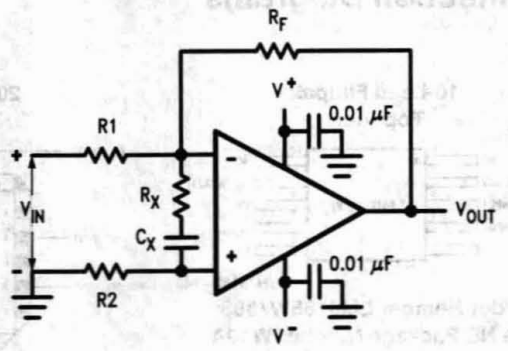
Typical Applications

Offset Voltage Adjustment



TL/H/9153–10

Noise-Gain Compensation for Gains ≤ 5

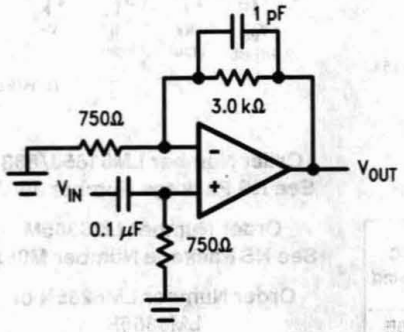


TL/H/9153–11

$R_X C_X \geq (2\pi \cdot 25\ \text{MHz})^{-1}$

$5\ R_X = R_1 + R_F(1 + R_1/R_2)$

Video-Bandwidth Amplifier



TL/H/9153–12

National Semiconductor

LM6165/LM6265/LM6365
High Speed Operational Amplifier

General Description

The LM6165 family of high-speed amplifiers exhibits an excellent speed-power product in delivering 300 V/μs and 725 MHz GBW (stable for gains as low as +25) with only 5 mA of supply current. Further power savings and application convenience are possible by taking advantage of the wide dynamic range in operating supply voltage which extends all the way down to +5V.

These amplifiers are built with National's VIP™ (Vertically Integrated PNP) process which produces fast PNP transistors that are true complements to the already fast NPN devices. This advanced junction-isolated process delivers high speed performance without the need for complex and expensive dielectric isolation.

Features

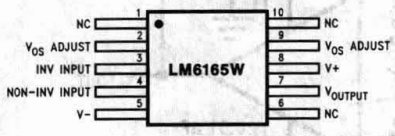
- High slew rate — 300 V/μs
- High GBW product — 725 MHz
- Low supply current — 5 mA
- Fast settling — 80 ns to 0.1%
- Low differential gain — <0.1%
- Low differential phase — <0.1°
- Wide supply range — 4.75V to 32V
- Stable with unlimited capacitive load

Applications

- Video amplifier
- Wide-bandwidth signal conditioning
- Radar
- Sonar

Connection Diagrams

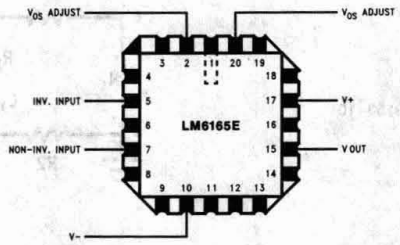
10-Lead Flatpak
Top View



TL/H/9152–14

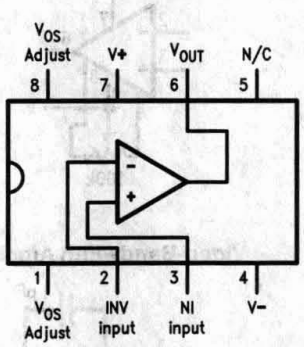
Order Number LM6165W/883
See NS Package Number W10A

20-Lead LCC
Top View



TL/H/9152–15

Order Number LM6165E/883
See NS Package Number E20A



TL/H/9152–8

Order Number LM6165J/883
See NS Package Number J08A

Order Number LM6365M
See NS Package Number M08A

Order Number LM6265N or LM6365N
See NS Package Number N08E

Temperature Range			Package	NSC Drawing
Military $-55°C \le T_A \le +125°C$	Industrial $-25°C \le T_A \le +85°C$	Commercial $0°C \le T_A \le +70°C$		
	LM6265N	LM6365N	8-Pin Molded DIP	N08E
LM6165J/883 5962-8962501PA			8-Pin Ceramic DIP	J08A
		LM6365M	8-Pin Molded Surface Mt.	M08A
LM6165E/883 5962-89625012A			20-Lead LCC	E20A
LM6165W883 5962-8962501HA			10-Pin Ceramic Flatpak	W10A

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage ($V^+ - V^-$)	36V
Differential Input Voltage (Note 6)	±8V
Common-Mode Voltage Range (Note 10)	$(V^+ - 0.7V)$ to $(V^- - 7V)$
Output Short Circuit to GND (Note 1)	Continuous
Soldering Information	
Dual-In-Line Package (N, J)	
Soldering (10 sec.)	260°C
Small Outline Package (M)	
Vapor Phase (60 sec.)	215°C
Infrared (15 sec.)	220°C

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.

Storage Temp Range	−65°C to +150°C
Max Junction Temperature (Note 2)	150°C
ESD Tolerance (Notes 6 and 7)	±700V

Operating Ratings

Temperature Range (Note 2)	
LM6165, LM6165J/883	$-55°C \le T_J \le +125°C$
LM6265	$-25°C \le T_J \le +85°C$
LM6365	$0°C \le T_J \le +70°C$
Supply Voltage Range	4.75V to 32V

DC Electrical Characteristics

The following specifications apply for Supply Voltage = ±15V, $V_{CM} = 0$, $R_L \ge 100\ k\Omega$ and $R_S = 50\Omega$ unless otherwise noted. **Boldface** limits apply for $T_A = T_J = T_{MIN}$ to T_{MAX}; all other limits $T_A = T_J = 25°C$.

Symbol	Parameter	Conditions	Typ	LM6165 Limit (Notes 3, 11)	LM6265 Limit (Note 3)	LM6365 Limit (Note 3)	Units
V_{OS}	Input Offset Voltage		1	3 **4**	3 **4**	6 **7**	mV Max
V_{OS} Drift	Input Offset Voltage Average Drift		3				µV/°C
I_b	Input Bias Current		2.5	3 **6**	3 **5**	5 **6**	µA Max
I_{OS}	Input Offset Current		150	350 **800**	350 **600**	1500 **1900**	nA Max
I_{OS} Drift	Input Offset Current Average Drift		0.3				nA/°C
R_{IN}	Input Resistance	Differential	20				kΩ
C_{IN}	Input Capacitance		6.0				pF
A_{VOL}	Large Signal Voltage Gain (Note 9)	$V_{OUT} = \pm 10V$, $R_L = 2\ k\Omega$	10.5	7.5 **5.0**	7.5 **6.0**	5.5 **5.0**	V/mV Min
		$R_L = 10\ k\Omega$	38				
V_{CM}	Input Common-Mode Voltage Range	Supply = ±15V	+14.0	+13.9 **+13.8**	+13.9 **+13.8**	+13.8 **+13.7**	V Min
			−13.6	−13.4 **−13.2**	−13.4 **−13.2**	−13.3 **−13.2**	V Min
		Supply = +5V (Note 4)	4.0	3.9 **3.8**	3.9 **3.8**	3.8 **3.7**	V Min
			1.4	1.6 **1.8**	1.6 **1.8**	1.7 **1.8**	V Max
CMRR	Common-Mode Rejection Ratio	$-10V \le V_{CM} \le +10V$	102	88 **82**	88 **84**	80 **78**	dB Min
PSRR	Power Supply Rejection Ratio	$\pm 10V \le V^{\pm} \le \pm 16V$	104	88 **82**	88 **84**	80 **78**	dB Min
V_O	Output Voltage Swing	Supply = ±15V, $R_L = 2\ k\Omega$	+14.2	+13.5 **+13.3**	+13.5 **+13.3**	+13.4 **+13.3**	V Min
			−13.4	−13.0 **−12.7**	−13.0 **−12.8**	−12.9 **−12.8**	V Min

2

DC Electrical Characteristics (Continued)

The following specifications apply for Supply Voltage = ±15V, V_{CM} = 0, $R_L \geq 100\ k\Omega$ and $R_S = 50\Omega$ unless otherwise noted. **Boldface** limits apply for $T_A = T_J = T_{MIN}$ to T_{Max}; all other limits $T_A = T_J = 25°C$.

Symbol	Parameter	Conditions	Typ	LM6165 Limit (Notes 3, 11)	LM6265 Limit (Note 3)	LM6365 Limit (Note 3)	Units
V_O (Continued)	Output Voltage Swing (Continued)	Supply = +5V R_L = 2 kΩ (Note 4)	4.2	3.5 **3.3**	3.5 **3.3**	3.4 **3.3**	V Min
			1.3	1.7 **2.0**	1.7 **1.9**	1.8 **1.9**	V Max
	Output Short Circuit Current	Source	65	30 **20**	30 **25**	30 **25**	mA Min
		Sink	65	30 **20**	30 **25**	30 **25**	mA Min
I_S	Supply Current		5.0	6.5 **6.8**	6.5 **6.7**	6.8 **6.9**	mA Max

AC Electrical Characteristics

The following specifications apply for Supply Voltage = ±15V, V_{CM} = 0, $R_L \geq 100\ k\Omega$ and $R_S = 50\Omega$ unless otherwise noted. **Boldface** limits apply for $T_A = T_J = T_{MIN}$ to T_{MAX}; all other limits $T_A = T_J = 25°C$. (Note 5)

Symbol	Parameter	Conditions	Typ	LM6165 Limit (Notes 3, 11)	LM6265 Limit (Note 3)	LM6365 Limit (Note 3)	Units
GBW	Gain Bandwidth Product	F = 20 MHz	725	575 **350**	575	500	MHz Min
		Supply = ±5V	500				
SR	Slew Rate	A_V = +25 (Note 8)	300	200 **180**	200	200	V/μs Min
		Supply = ±5V	200				
PBW	Power Bandwidth Product	V_{OUT} = 20 V_{PP}	4.5				MHz
t_S	Settling Time	10V Step to 0.1% A_V = −25, R_L = 2 kΩ	80				ns
ϕ_m	Phase Margin	A_V = +25	45				Deg
A_D	Differential Gain	NTSC, A_V = +25	<0.1				%
ϕ_D	Differential Phase	NTSC, A_V = +25	<0.1				Deg
e_{np-p}	Input Noise Voltage	F = 10 kHz	5				$nV/\sqrt{Hz}$
i_{np-p}	Input Noise Current	F = 10 kHz	1.5				$pA/\sqrt{Hz}$

Note 1: Continuous short-circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 150°C.

Note 2: The typical junction-to-ambient thermal resistance of the molded plastic DIP (N) is 105°C/Watt, and the molded plastic SO (M) package is 155°C/Watt, and the cerdip (J) package is 125°C/Watt. All numbers apply for packages soldered directly into a printed circuit board.

Note 3: All limits guaranteed by testing or correlation.

Note 4: For single supply operation, the following conditions apply: V+ = 5V, V− = 0V, V_{CM} = 2.5C, V_{OUT} = 2.5V. Pin 1 & Pin 8 (V_{OS} Adjust) are each connected to Pin 4 (V−) to realize maximum output swing. This connection will degrade V_{OS}.

Note 5: $C_L \leq 5$ pF.

Note 6: In order to achieve optimum AC performance, the input stage was designed without protective clamps. Exeeding the maximum differential input voltage results in reverse breakdown of the base-emitter junction of one of the input transistors and probable degradation of the input parameters (especially V_{OS}, I_{OS}, and Noise).

Note 7: The average voltage that the weakest pin combinations (those involving Pin 2 or Pin 3) can withstand and still conform to the datasheet limits. The test circuit used consists of the human body model of 100 pF in series with 1500Ω.

Note 8: V_{IN} = 0.8V step. For supply = ±5V, V_{IN} = 0.2V step.

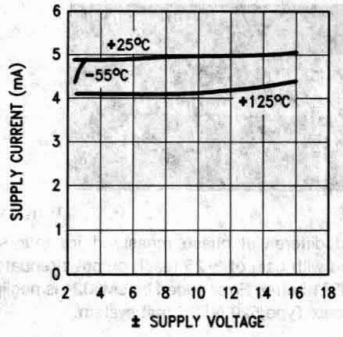
Note 9: Voltage Gain is the total output swing (20V) divided by the input signal required to produce that swing.

Note 10: The voltage between V^+ and either input pin must not exceed 36V.

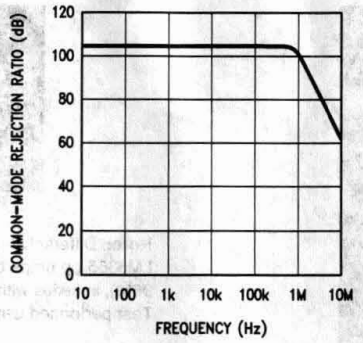
Note 11: A military RETS electrical test specification is available on request. At the time of printing, the LM6165J/883 RETS spec complied with the **Boldface** limits in this column. The LM6165J/883 may also be procured as Standard Military Drawing #5962-8962501PA.

Typical Performance Characteristics $R_L = 10\ k\Omega$, $T_A = 25°C$ unless otherwise specified

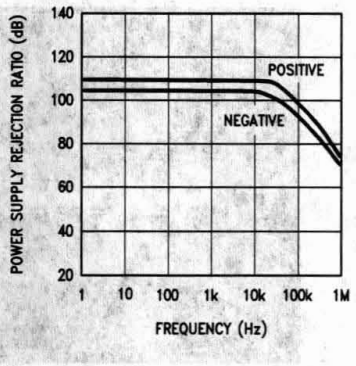
Supply Current vs Supply Voltage



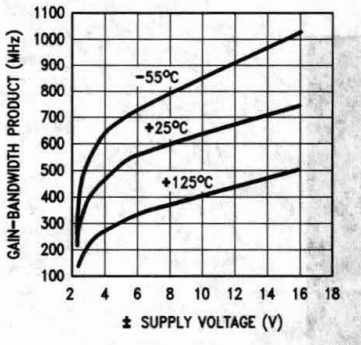
Common-Mode Rejection Ratio



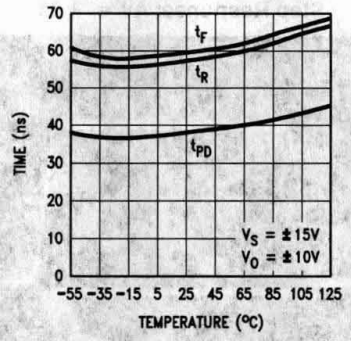
Power Supply Rejection Ratio



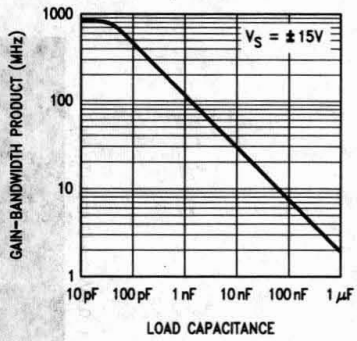
Gain-Bandwidth Product



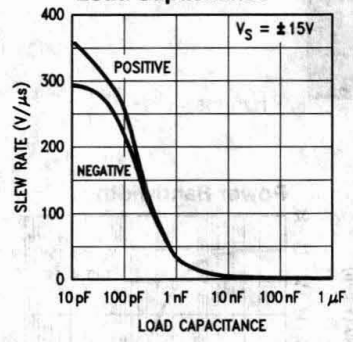
Propagation Delay, Rise and Fall Times



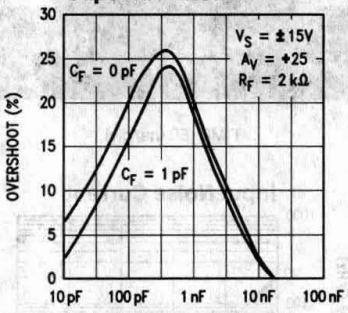
Gain-Bandwidth Product vs Load Capacitance



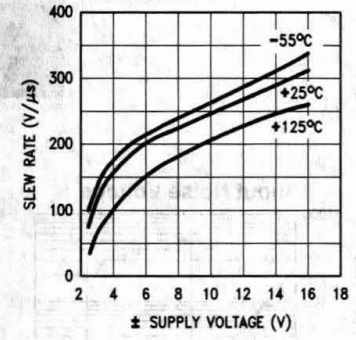
Slew Rate vs Load Capacitance



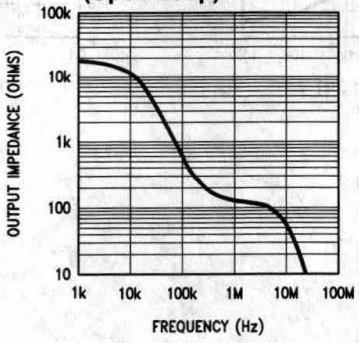
Overshoot vs Capacitive Load



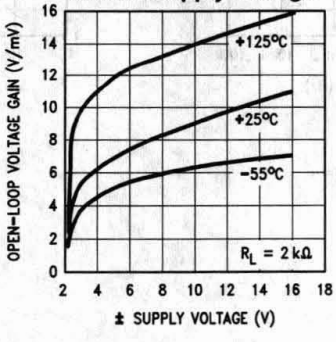
Slew Rate



Output Impedance (Open-Loop)



Gain vs Supply Voltage

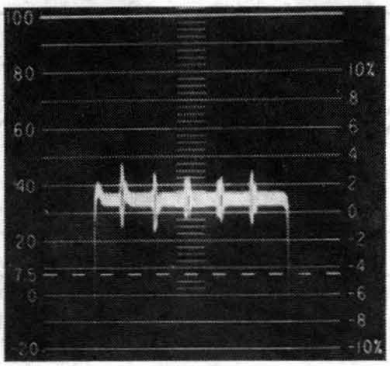


TL/H/9152–5

Typical Performance Characteristics (Continued)

R_L = 10 kΩ, T_A = 25°C unless otherwise specified

Differential Gain (Note)



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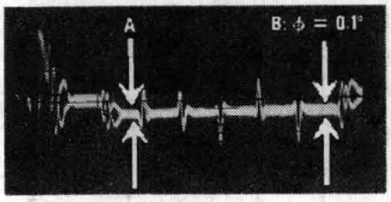
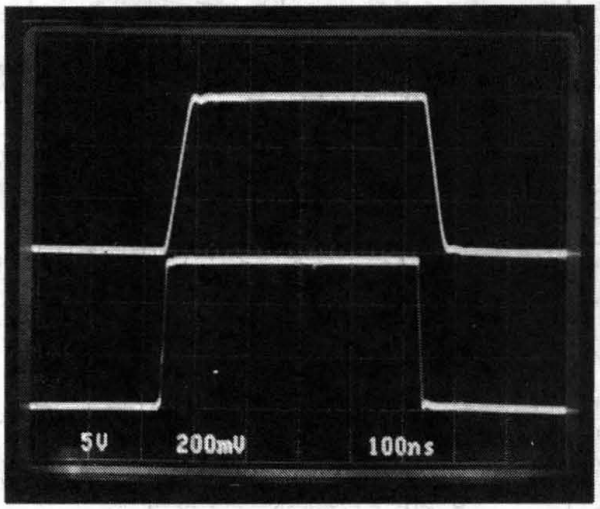
Differential Phase (Note)



TL/H/9152–7

Note: Differential gain and differential phase measured for four series LM6365 op amps configured with gain of +25 (each output attenuated by 96%), in series with an LM6321 buffer. Error added by LM6321 is negligible. Test performed using Tektronix Type 520 NTSC test system.

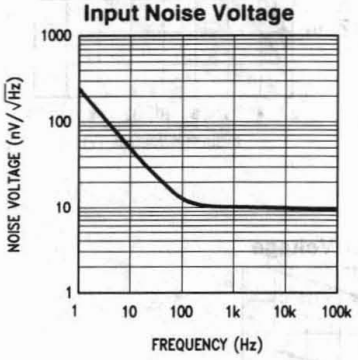
Step Response; Av = +25



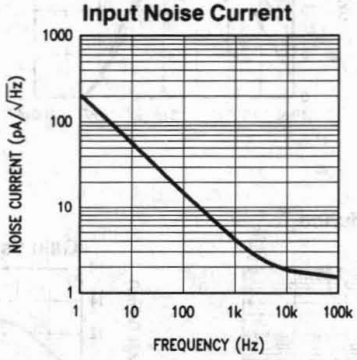
TL/H/9152–1

TIME (50 (ns/div)

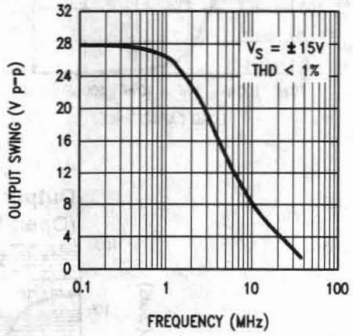
Input Noise Voltage



Input Noise Current



Power Bandwidth

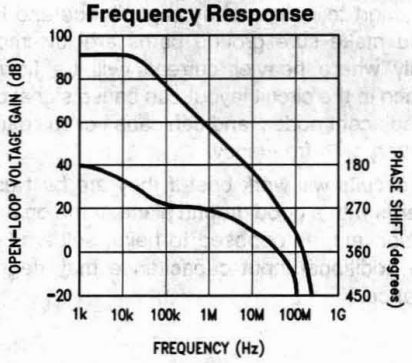


TL/H/9152–9

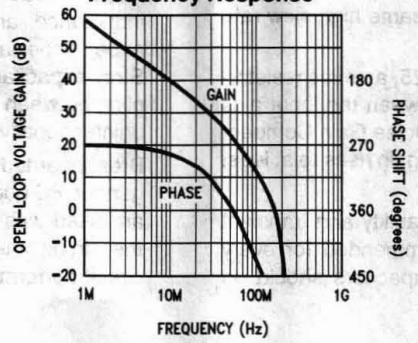
Typical Performance Characteristics (Continued)

R_L = 10 kΩ, T_A = 25°C unless otherwise specified

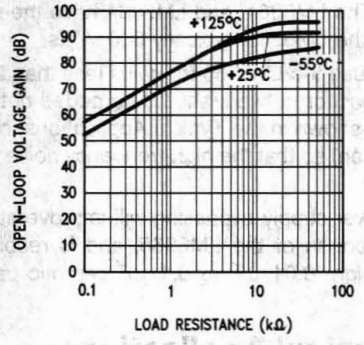
Open-Loop Frequency Response



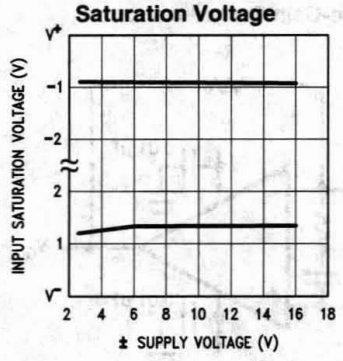
Open-Loop Frequency Response



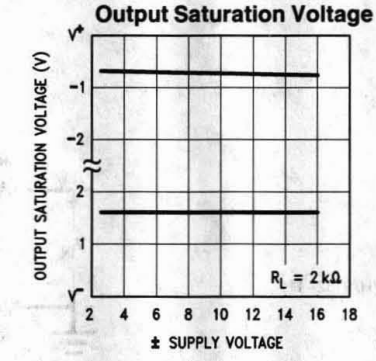
Voltage Gain vs Load Resistance



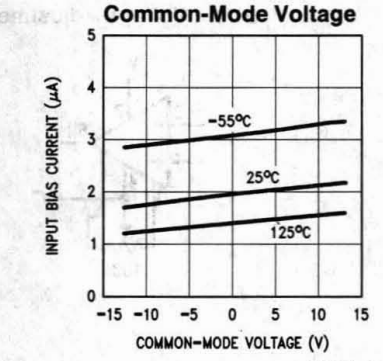
Common-Mode Input Saturation Voltage



Output Saturation Voltage

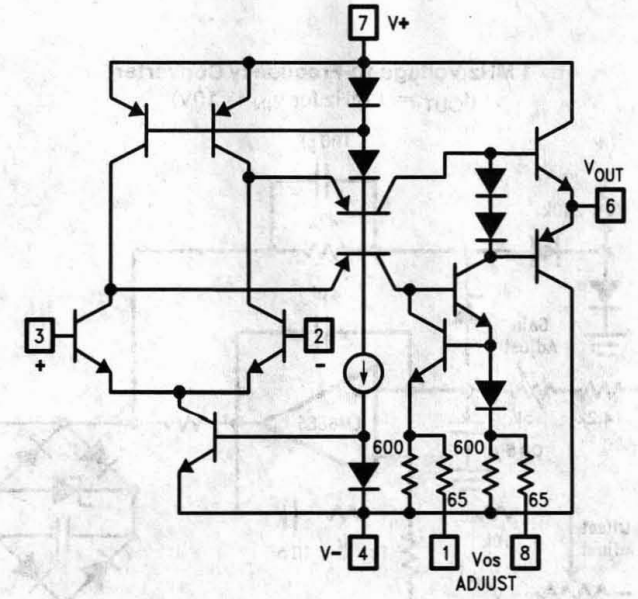


Bias Current vs Common-Mode Voltage



TL/H/9152–10

Simplified Schematic



TL/H/9152–3

Applications Tips

The LM6365 is stable for gains of 25 or greater. The LM6361 and LM6364, specified in separate datasheets, are compensated versions of the LM6365. The LM6361 is unity-gain stable, while the LM6364 is stable for gains as low as 5. The LM6361, and LM6364 have the same high slew rate as the LM6365, typically 300 V/μs.

To use the LM6365 for gains less than 25, a series resistor-capacitor network should be added between the input pins (as shown in the Typical Applications, Noise Gain Compensation) so that the high-frequency noise gain rises to at least 25.

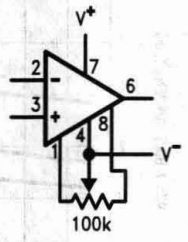
Power supply bypassing will improve stability and transient response of the LM6365, and is recommended for every design. 0.01 μF to 0.1 μF ceramic capacitors should be used (from each supply "rail" to ground); an additional 2.2 μF to 10 μF (tantalum) may be required for extra noise reduction.

Keep all leads short to reduce stray capacitance and lead inductance, and make sure ground paths are low-impedance, especially where heavier currents will be flowing. Stray capacitance in the circuit layout can cause signal coupling between adjacent nodes, and can cause circuit gain to unintentionally vary with frequency.

Breadboarded circuits will work best if they are built using generic PC boards with a good ground plane. If the op amps are used with sockets, as opposed to being soldered into the circuit, the additional input capacitance may degrade circuit performance.

Typical Applications

Offset Voltage Adjustment



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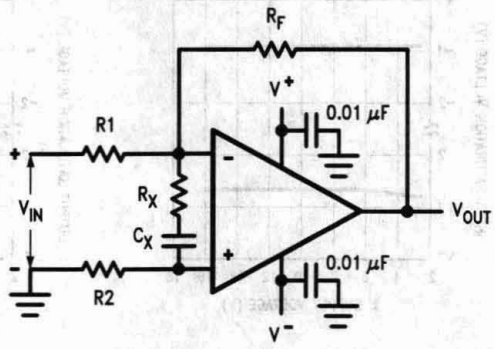
Noise-Gain Compensation



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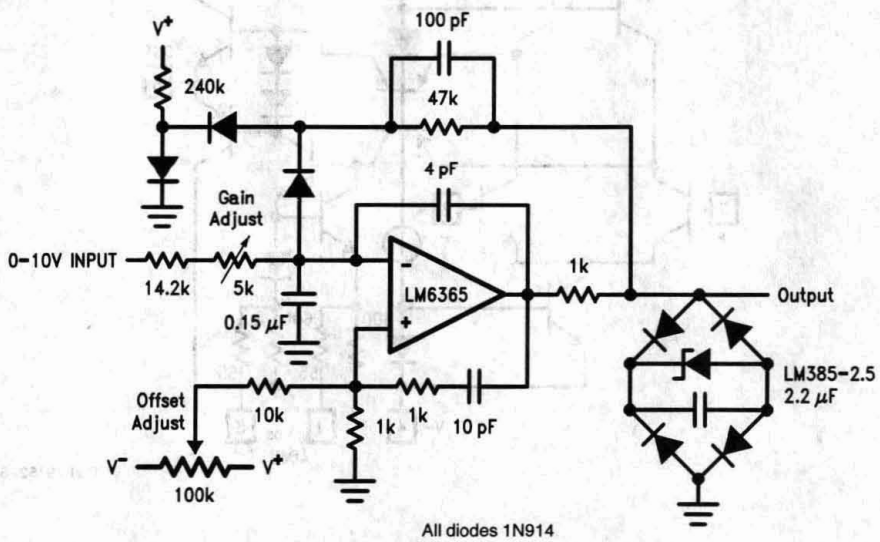
$R_X C_X \geq 1/(2\pi \bullet 25\ \text{MHz})$

$[R1 + R_F (1 + R1/R2)] = 25\, R_X$

1 MHz Voltage-to-Frequency Converter

(f_{OUT} = 1 MHz for V_{IN} = 10V)



All diodes 1N914

TL/H/9152–13

National Semiconductor

LM6171 High Speed Low Power Low Distortion Voltage Feedback Amplifier

General Description

The LM6171 is a high speed unity-gain stable voltage feedback amplifier. It offers a high slew rate of 3600V/μs and a unity-gain bandwidth of 100 MHz while consuming only 2.5 mA of supply current. The LM6171 has very impressive AC and DC performance which is a great benefit for high speed signal processing and video applications.

The ±15V power supplies allow for large signal swings and give greater dynamic range and signal-to-noise ratio. The LM6171 has high output current drive, low SFDR and THD, ideal for ADC/DAC systems. The LM6171 is specified for ±5V operation for portable applications.

The LM6171 is built on National's advanced VIP™ III (Vertically Integrated PNP) complementary bipolar process.

Features (Typical Unless Otherwise Noted)

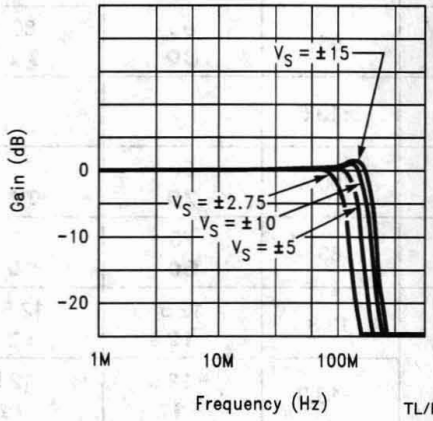
- Easy-To-Use Voltage Feedback Topology
- Very High Slew Rate 3600V/μs
- Wide Unity-Gain-Bandwidth Product 100 MHz
- −3 dB Frequency @ $A_V = +2$ 62 MHz
- Low Supply Current 2.5 mA
- High CMRR 110 dB
- High Open Loop Gain 90 dB
- Specified for ±15V and ±5V Operation

Applications

- Multimedia Broadcast Systems
- Line Drivers, Switchers
- Video Amplifiers
- NTSC, PAL® and SECAM Systems
- ADC/DAC Buffers
- HDTV Amplifiers
- Pulse Amplifiers and Peak Detectors
- Instrumentation Amplifier
- Active Filters

Typical Performance Characteristics

Closed Loop Frequency Response vs Supply Voltage ($A_V = +1$)



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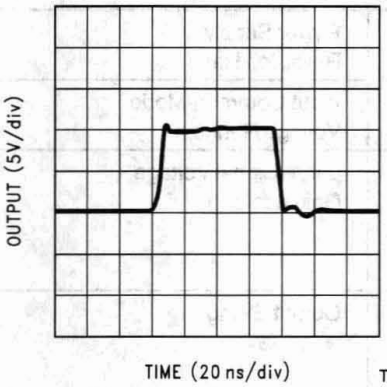
Large Signal Pulse Response $A_V = +1, V_S = \pm 15$



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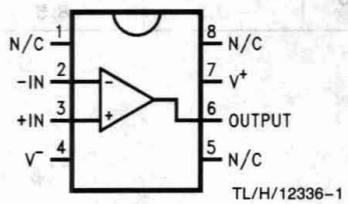
Connection Diagram

8-Pin DIP/SO



TL/H/12336-1

Top View

Ordering Information

Package	Temperature Range: Industrial −40°C to +85°C	Transport Media	NSC Drawing
8-Pin Molded DIP	LM6171AIN LM6171BIN	Rails	N08E
8-Pin Small Outline	LM6171AIM, LM6171BIM	Rails	M08A
	LM6171AIMX, LM6171BIMX	Tape and Reel	

2

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

ESD Tolerance (Note 2)	2.5 kV
Supply Voltage ($V^+ - V^-$)	36V
Differential Input Voltage (Note 11)	±10V
Common-Mode Voltage Range	$V^+ - 1.4V$ to $V^- + 1.4V$
Output Short Circuit to Ground (Note 3)	Continuous
Storage Temperature Range	−65°C to +150°C
Maximum Junction Temperature (Note 4)	150°C

Operating Ratings (Note 1)

Supply Voltage	$2.75V \le V^+ \le 18V$
Junction Temperature Range	
LM6171AI, LM6171BI	$-40°C \le T_J \le +85°C$
Thermal Resistance (θ_{JA})	
N Package, 8-Pin Molded DIP	108°C/W
M Package, 8-Pin Surface Mount	172°C/W

±15V DC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for T_J = 25°C, V^+ = +15V, V^- = −15V, V_{CM} = 0V, and R_L = 1 kΩ. **Boldface** limits apply at the temperature extremes

Symbol	Parameter	Conditions	Typ (Note 5)	LM6171AI Limit (Note 6)	LM6171BI Limit (Note 6)	Units
V_{OS}	Input Offset Voltage		1.5	3 **5**	6 **8**	mV max
TC V_{OS}	Input Offset Voltage Average Drift		6			µV/°C
I_B	Input Bias Current		1	3 **4**	3 **4**	µA max
I_{OS}	Input Offset Current		0.03	2 **3**	2 **3**	µA max
R_{IN}	Input Resistance	Common Mode	40			MΩ
		Differential Mode	4.9			
R_O	Open Loop Output Resistance		14			Ω
CMRR	Common Mode Rejection Ratio	V_{CM} = ±10V	110	80 **75**	75 **70**	dB min
PSRR	Power Supply Rejection Ratio	V_S = ±15V−±5V	95	85 **80**	80 **75**	dB min
V_{CM}	Input Common-Mode Voltage Range	CMRR ≥ 60 dB	±13.5			V
A_V	Large Signal Voltage Gain (Note 7)	R_L = 1 kΩ	90	80 **70**	80 **70**	dB min
		R_L = 100Ω	83	70 **60**	70 **60**	dB min
V_O	Output Swing	R_L = 1 kΩ	13.3	12.5 **12**	12.5 **12**	V min
			−13.3	−12.5 **−12**	−12.5 **−12**	V max
		R_L = 100Ω	11.6	9 **8.5**	9 **8.5**	V min
			−10.5	−9 **−8.5**	−9 **−8.5**	V max

±15V DC Electrical Characteristics (Continued) Unless otherwise specified, all limits guaranteed for T_J = 25°C, V^+ = +15V, V^- = −15V, V_{CM} = 0V, and R_L = 1 kΩ. **Boldface** limits apply at the temperature extremes

Symbol	Parameter	Conditions	Typ (Note 5)	LM6171AI Limit (Note 6)	LM6171BI Limit (Note 6)	Units
	Continuous Output Current (Open Loop) (Note 8)	Sourcing, R_L = 100Ω	116	90 **85**	90 **85**	mA min
		Sinking, R_L = 100Ω	105	90 **85**	90 **85**	mA max
	Continuous Output Current (in Linear Region)	Sourcing, R_L = 10Ω	100			mA
		Sinking, R_L = 10Ω	80			mA
I_{SC}	Output Short Circuit Current	Sourcing	135			mA
		Sinking	135			mA
I_S	Supply Current		2.5	4 **4.5**	4 **4.5**	mA max

±15V AC Electrical Characteristics Unless otherwise specified, all limits guaranteed for T_J = 25°C, V^+ = +15V, V^- = −15V, V_{CM} = 0V, and R_L = 1 kΩ. **Boldface** limits apply at the temperature extremes

Symbol	Parameter	Conditions	Typ (Note 5)	LM6171AI Limit (Note 6)	LM6171BI Limit (Note 6)	Units
SR	Slew Rate (Note 9)	A_V = +2, V_{IN} = 13 V_{PP}	3600			V/μs
		A_V = +2, V_{IN} = 10 V_{PP}	3000			
GBW	Unity Gain-Bandwidth Product		100			MHz
	−3 dB Frequency	A_V = +1	160			MHz
		A_V = +2	62			MHz
ϕ_m	Phase Margin		40			deg
t_s	Settling Time (0.1%)	A_V = −1, V_{OUT} = ±5V R_L = 500Ω	35			ns
	Propagation Delay	V_{IN} = ±5V, R_L = 500Ω, A_V = −2	6			ns
A_D	Differential Gain (Note 10)		0.03			%
ϕ_D	Differential Phase (Note 10)		0.5			deg
e_n	Input-Referred Voltage Noise	f = 1 kHz	12			$\frac{nV}{\sqrt{Hz}}$
i_n	Input-Referred Current Noise	f = 1 kHz	1			$\frac{pA}{\sqrt{Hz}}$

±5V DC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for T_J = 25°C, V^+ = +5V, V^- = −5V, V_{CM} = 0V, and R_L = 1 kΩ. **Boldface** limits apply at the temperature extremes

Symbol	Parameter	Conditions	Typ (Note 5)	LM6171AI Limit (Note 6)	LM6171BI Limit (Note 6)	Units
V_{OS}	Input Offset Voltage		1.2	3 **5**	6 **8**	mV max
TC V_{OS}	Input Offset Voltage Average Drift		4			μV/°C
I_B	Input Bias Current		1	2.5 **3.5**	2.5 **3.5**	μA max
I_{OS}	Input Offset Current		0.03	1.5 **2.2**	1.5 **2.2**	μA max
R_{IN}	Input Resistance	Common Mode	40			MΩ
		Differential Mode	4.9			
R_O	Open Loop Output Resistance		14			Ω
CMRR	Common Mode Rejection Ratio	V_{CM} = ±2.5V	105	80 **75**	75 **70**	dB min
PSRR	Power Supply Rejection Ratio	V_S = ±15V to ±5V	95	85 **80**	80 **75**	dB min
V_{CM}	Input Common-Mode Voltage Range	CMRR ≥ 60 dB	±3.7			V
A_V	Large Signal Voltage Gain (Note 7)	R_L = 1 kΩ	84	75 **65**	75 **65**	dB min
		R_L = 100Ω	80	70 **60**	70 **60**	dB min
V_O	Output Swing	R_L = 1 kΩ	3.5	3.2 **3**	3.2 **3**	V min
			−3.4	−3.2 **−3**	−3.2 **−3**	V max
		R_L = 100Ω	3.2	2.8 **2.5**	2.8 **2.5**	V min
			−3.0	−2.8 **−2.5**	−2.8 **−2.5**	V max
	Continuous Output Current (Open Loop) (Note 8)	Sourcing, R_L = 100Ω	32	28 **25**	28 **25**	mA min
		Sinking, R_L = 100Ω	30	28 **25**	28 **25**	mA max
I_{SC}	Output Short Circuit Current	Sourcing	130			mA
		Sinking	100			mA
I_S	Supply Current		2.3	3 **3.5**	3 **3.5**	mA max

±5V AC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for T_J = 25°C, V^+ = +5V, V^- = −5V, V_{CM} = 0V, and R_L = 1 kΩ. **Boldface** limits apply at the temperature extremes

Symbol	Parameter	Conditions	Typ (Note 5)	LM6171AI Limit (Note 6)	LM6171BI Limit (Note 6)	Units
SR	Slew Rate (Note 9)	A_V = +2, V_{IN} = 3.5 V_{PP}	750			V/μs
GBW	Unity Gain-Bandwidth Product		70			MHz
	−3 dB Frequency	A_V = +1	130			MHz
		A_V = +2	45			
φm	Phase Margin		57			deg
t_s	Settling Time (0.1%)	A_V = −1, V_{OUT} = +1V, R_L = 500Ω	48			ns
	Propagation Delay	V_{IN} = ±1V, R_L = 500Ω, A_V = −2	8			ns
A_D	Differential Gain (Note 10)		0.04			%
ϕ_D	Differential Phase (Note 10)		0.7			deg
e_n	Input-Referred Voltage Noise	f = 1 kHz	11			$\frac{nV}{\sqrt{Hz}}$
i_n	Input-Referred Current Noise	f = 1 kHz	1			$\frac{pA}{\sqrt{Hz}}$

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not guaranteed. For guaranteed specifications and the test conditions, see the Electrical Characteristics.

Note 2: Human body model, 1.5 kΩ in series with 100 pF.

Note 3: Continuous short circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 150°C.

Note 4: The maximum power dissipation is a function of $T_{J(max)}$, θ_{JA}, and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(max)} - T_A)/\theta_{JA}$. All numbers apply for packages soldered directly into a PC board.

Note 5: Typical Values represent the most likely parametric norm.

Note 6: All limits are guaranteed by testing or statistical analysis.

Note 7: Large signal voltage gain is the total output swing divided by the input signal required to produce that swing. For V_S = ±15V, V_{OUT} = ±5V. For V_S = +5V, V_{OUT} = ±1V.

Note 8: The open loop output current is the output swing with the 100Ω load resistor divided by that resistor.

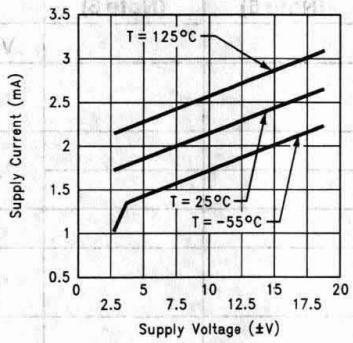
Note 9: Slew rate is the average of the rising and falling slew rates.

Note 10: Differential gain and phase are measured with A_V = +2, V_{IN} = 1 V_{PP} at 3.58 MHz and both input and output 75Ω terminated.

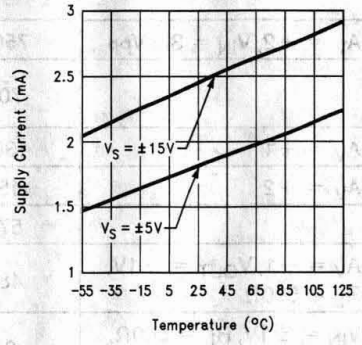
Note 11: Differential input voltage is measured at V_S = ±15V.

Typical Performance Characteristics Unless otherwise noted, $T_A = 25°C$

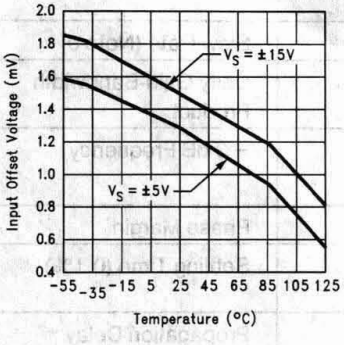
Supply Current vs Supply Voltage



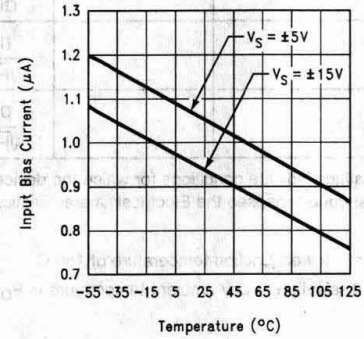
Supply Current vs Temperature



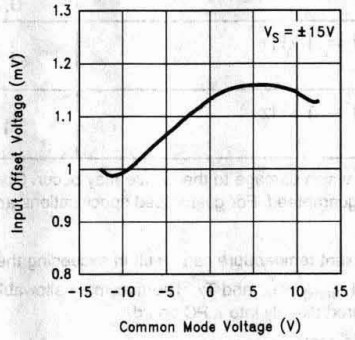
Input Offset Voltage vs Temperature



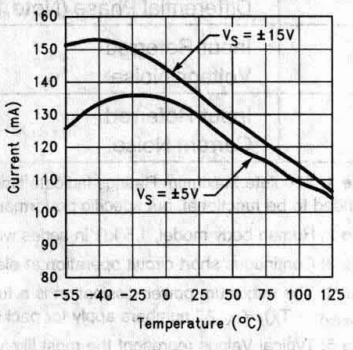
Input Bias Current vs Temperature



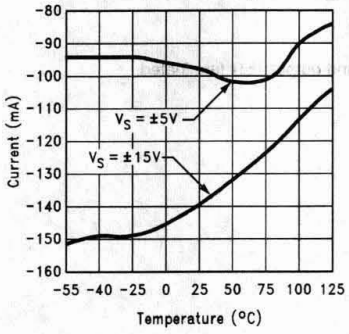
Input Offset Voltage vs Common Mode Voltage



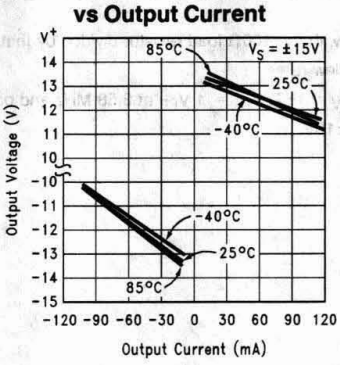
Short Circuit Current vs Temperature (Sourcing)



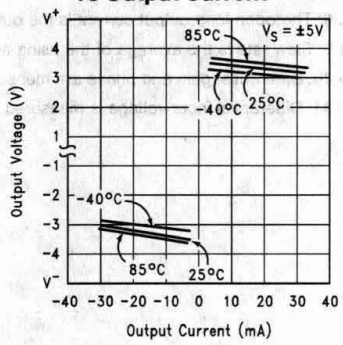
Short Circuit Current vs Temperature (Sinking)



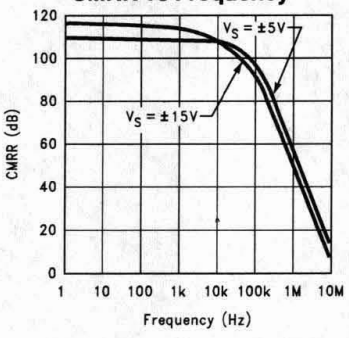
Output Voltage vs Output Current



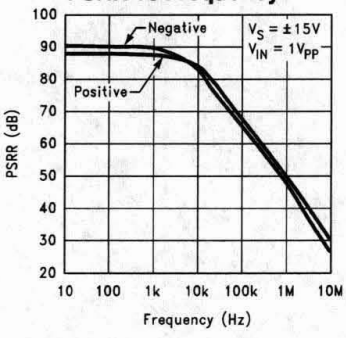
Output Voltage vs Output Current



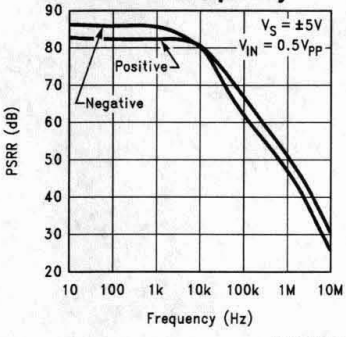
CMRR vs Frequency



PSRR vs Frequency



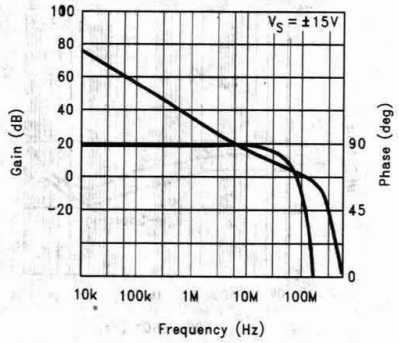
PSRR vs Frequency



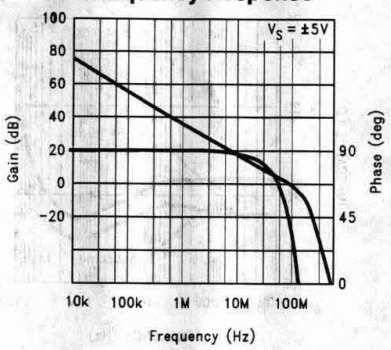
TL/H/12336–3

Typical Performance Characteristics Unless otherwise noted, T_A = 25°C (Continued)

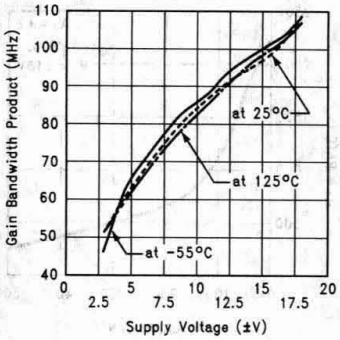
Open Loop Frequency Response



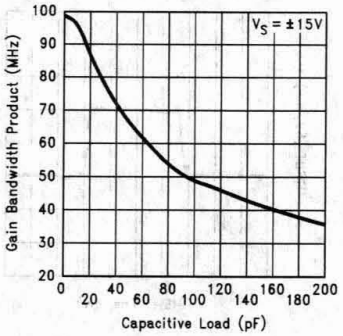
Open Loop Frequency Response



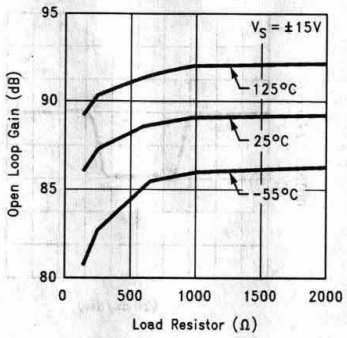
Gain Bandwidth Product vs Supply Voltage



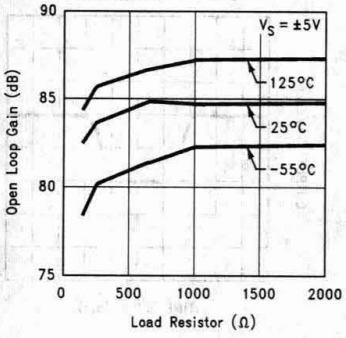
Gain Bandwidth Product vs Load Capacitance



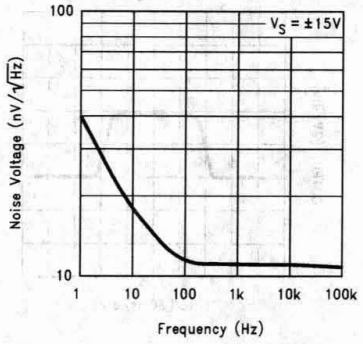
Large Signal Voltage Gain vs Load



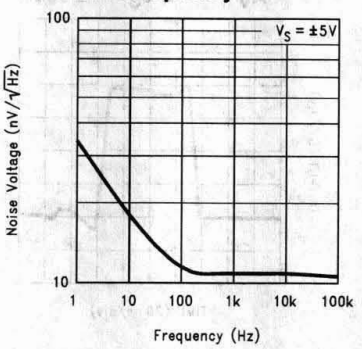
Large Signal Voltage Gain vs Load



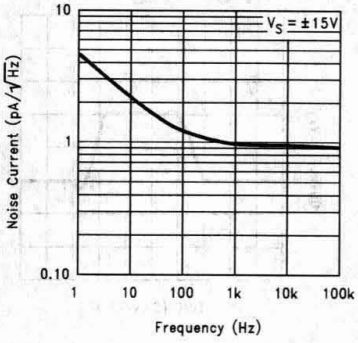
Input Voltage Noise vs Frequency



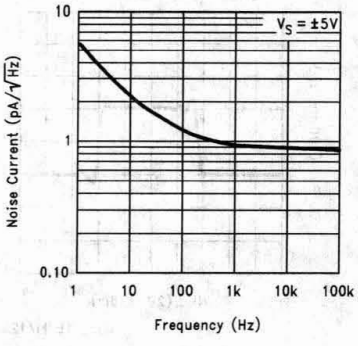
Input Voltage Noise vs Frequency



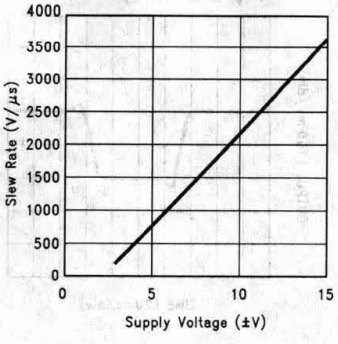
Input Current Noise vs Frequency



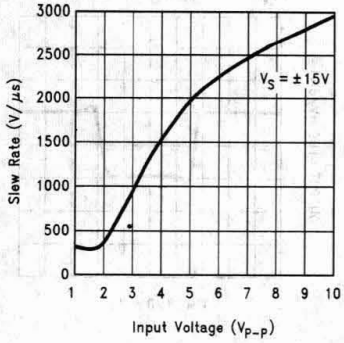
Input Current Noise vs Frequency



Slew Rate vs Supply Voltage



Slew Rate vs Input Voltage



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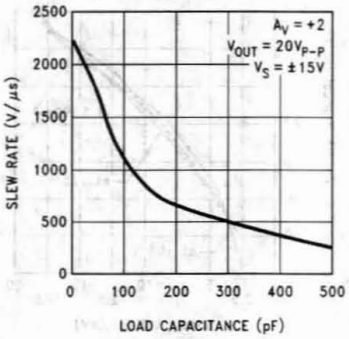
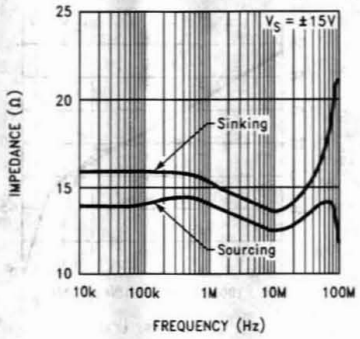
Typical Performance Characteristics Unless otherwise noted, T_A = 25°C (Continued)

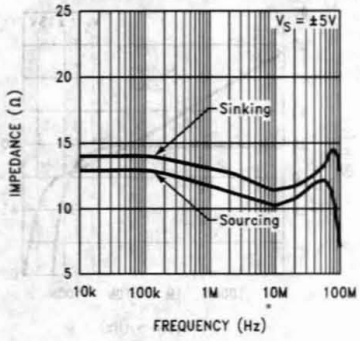
Slew Rate vs Load Capacitance



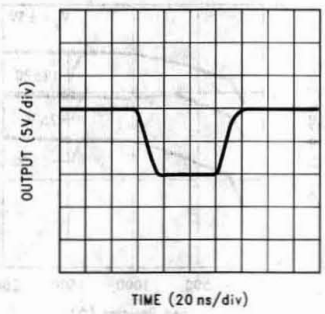
Open Loop Output Impedance vs Frequency



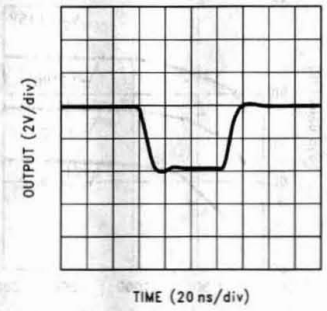
Open Loop Output Impedance vs Frequency



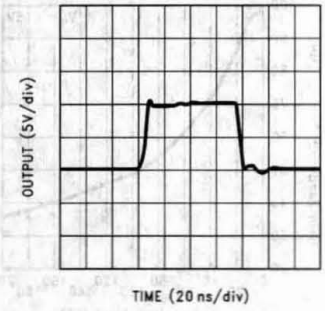
Large Signal Pulse Response $A_V = -1, V_S = \pm 15V$



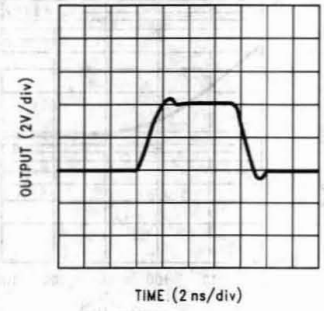
Large Signal Pulse Response $A_V = -1, V_S = \pm 5V$



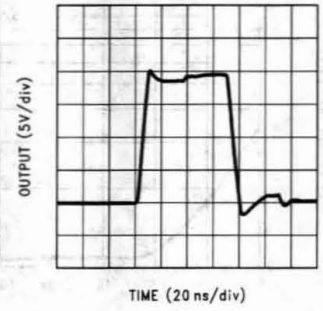
Large Signal Pulse Response $A_V = +1, V_S = \pm 15V$



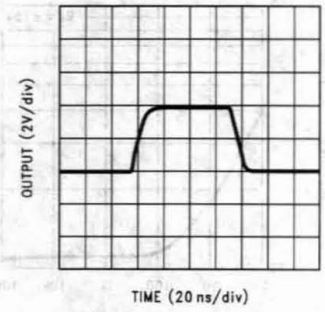
Large Signal Pulse Response $A_V = +1, V_S = \pm 5V$



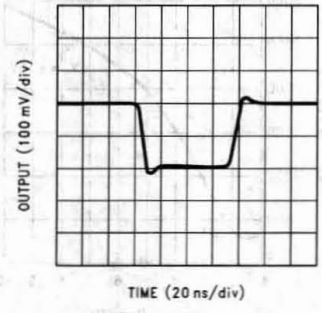
Large Signal Pulse Response $A_V = +2, V_S = \pm 15V$



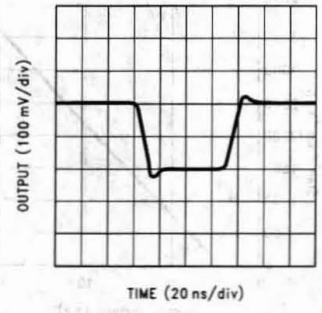
Large Signal Pulse Response $A_V = +2, V_S = \pm 5V$



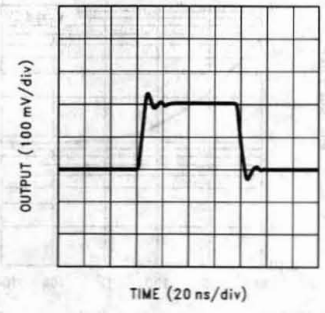
Small Signal Pulse Response $A_V = -1, V_S = \pm 15V$



Small Signal Pulse Response $A_V = -1, V_S = \pm 5V$



Small Signal Pulse Response $A_V = +1, V_S = \pm 15V$



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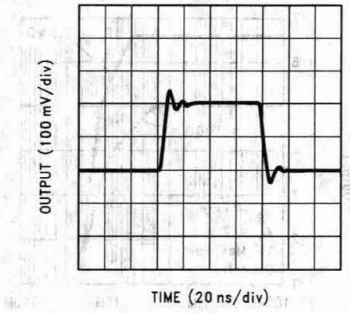
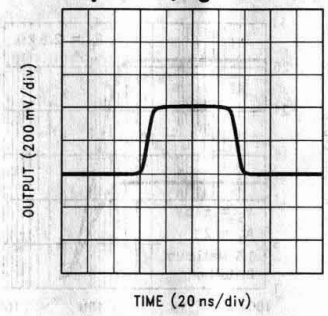
Typical Performance Characteristics Unless otherwise noted, $T_A = 25°C$ (Continued)

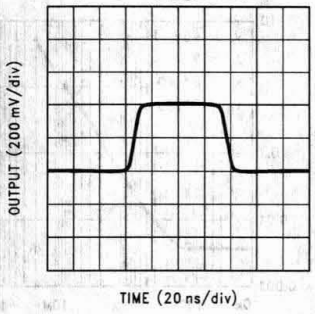
Small Signal Pulse Response $A_V = +1, V_S = \pm 5V$



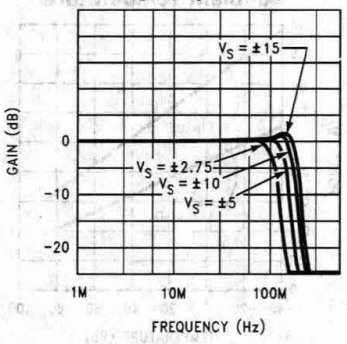
Small Signal Pulse Response $A_V = +2, V_S = \pm 15V$



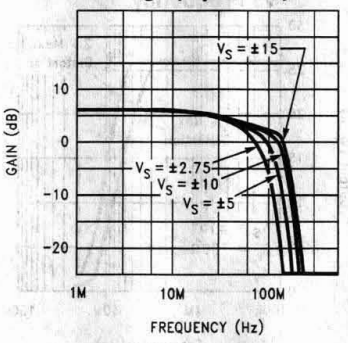
Small Signal Pulse Response $A_V = +2, V_S = \pm 5V$



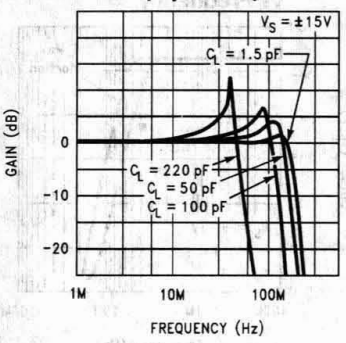
Closed Loop Frequency Response vs Supply Voltage ($A_V = +1$)



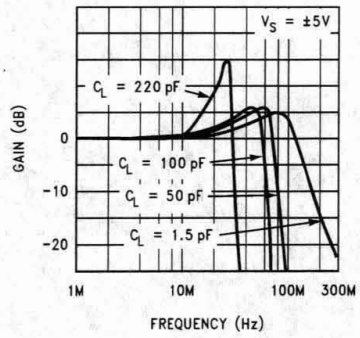
Closed Loop Frequency Response vs Supply Voltage ($A_V = +2$)



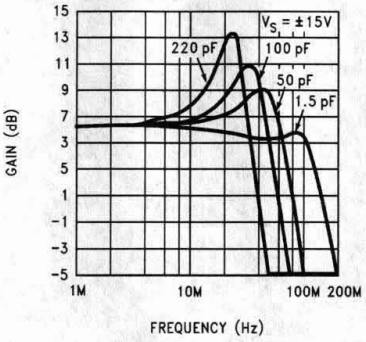
Closed Loop Frequency Response vs Capacitive Load ($A_V = +1$)



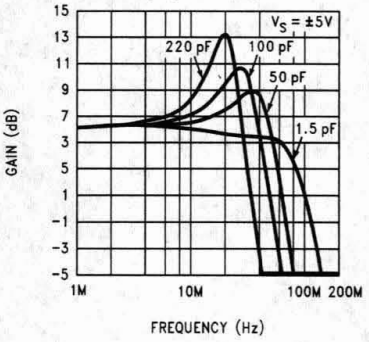
Closed Loop Frequency Response vs Capacitive Load ($A_V = +1$)



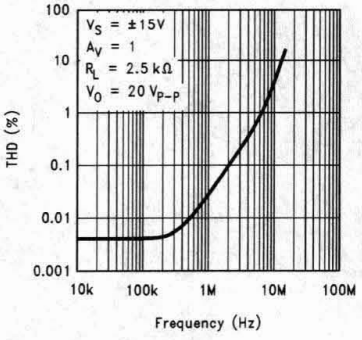
Closed Loop Frequency Response vs Capacitive Load ($A_V = +2$)



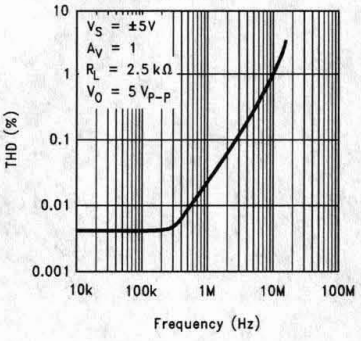
Closed Loop Frequency Response vs Capacitive Load ($A_V = +2$)



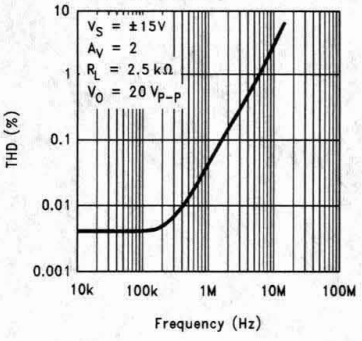
Total Harmonic Distortion vs Frequency



Total Harmonic Distortion vs Frequency



Total Harmonic Distortion vs Frequency



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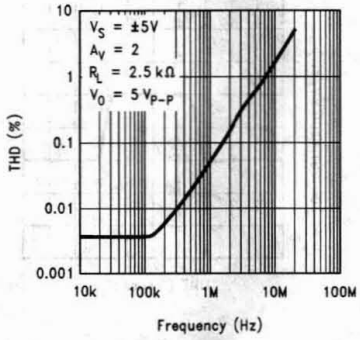
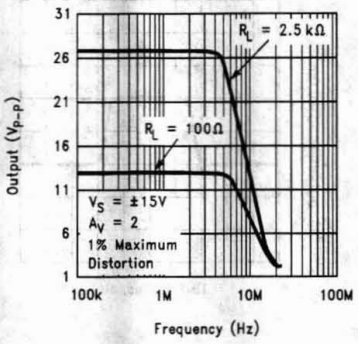
Typical Performance Characteristics Unless otherwise noted, T_A = 25°C (Continued)

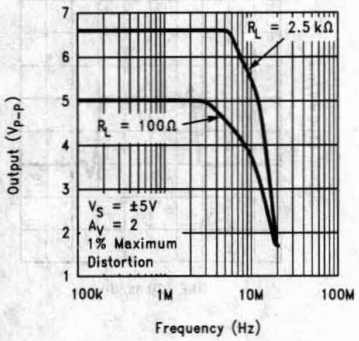
Total Harmonic Distortion vs Frequency



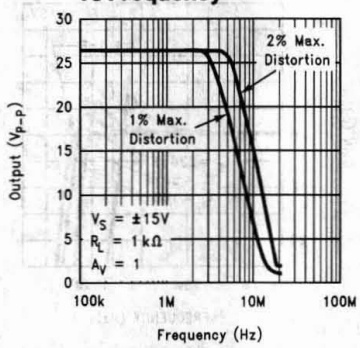
Undistorted Output Swing vs Frequency



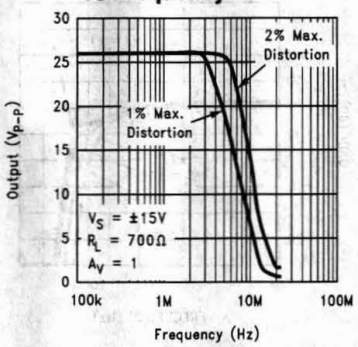
Undistorted Output Swing vs Frequency



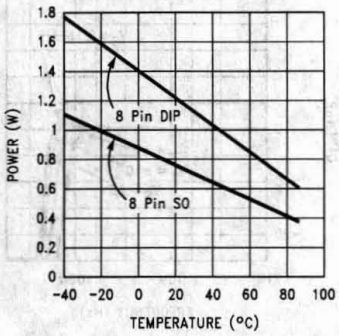
Undistorted Output Swing vs Frequency



Undistorted Output Swing vs Frequency



Total Power Dissipation vs Ambient Temperature



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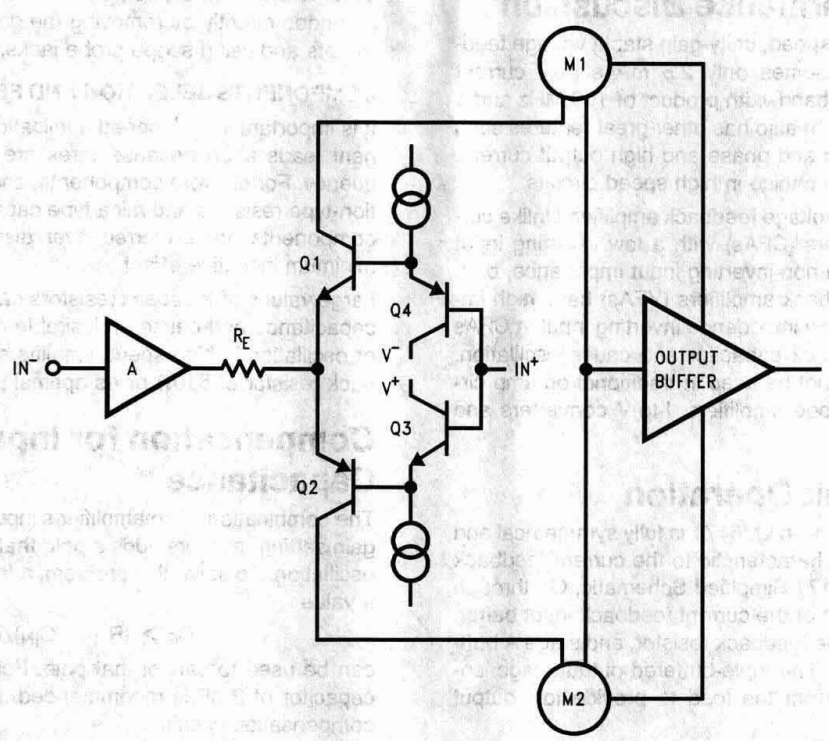
LM6171 Simplified Schematic



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Application Information

LM6171 Performance Discussion

The LM6171 is a high speed, unity-gain stable voltage feedback amplifier. It consumes only 2.5 mA supply current while providing a gain-bandwidth product of 100 MHz and a slew rate of 3600V/μs. It also has other great features such as low differential gain and phase and high output current. The LM6171 is a good choice in high speed circuits.

The LM6171 is a true voltage feedback amplifier. Unlike current feedback amplifiers (CFAs) with a low inverting input impedance and a high non-inverting input impedance, both inputs of voltage feedback amplifiers (VFAs) have high impedance nodes. The low impedance inverting input in CFAs will couple with feedback capacitor and cause oscillation. As a result, CFAs cannot be used in traditional op amp circuits such as photodiode amplifiers, I-to-V converters and integrators.

LM6171 Circuit Operation

The class AB input stage in LM6171 is fully symmetrical and has a similar slewing characteristic to the current feedback amplifiers. In the LM6171 Simplfied Schematic, Q1 through Q4 form the equivalent of the current feedback input buffer, R_E the equivalent of the feedback resistor, and stage A buffers the inverting input. The triple-buffered output stage isolates the gain stage from the load to provide low output impedance.

LM6171 Slew Rate Characteristic

The slew rate of LM6171 is determined by the current available to charge and discharge an internal high impedance node capacitor. The current is the differential input voltage divided by the total degeneration resistor R_E. Therefore, the slew rate is proportional to the input voltage level, and the higher slew rates are achievable in the lower gain configurations.

When a very fast large signal pulse is applied to the input of an amplifier, some overshoot or undershoot occurs. By placing an external series resistor such as 1 kΩ to the input of LM6171, the bandwidth is reduced to help lower the overshoot.

Layout Consideration

PRINTED CIRCUIT BOARDS AND HIGH SPEED OP AMPS

There are many things to consider when designing PC boards for high speed op amps. Without proper caution, it is very easy and frustrating to have excessive ringing, oscillation and other degraded AC performance in high speed circuits. As a rule, the signal traces should be short and wide to provide low inductance and low impedance paths. Any unused board space needs to be grounded to reduce stray signal pickup. Critical components should also be grounded at a common point to eliminate voltage drop. Sockets add capacitance to the board and can affect frequency performance. It is better to solder the amplifier directly into the PC board without using any socket.

USING PROBES

Active (FET) probes are ideal for taking high frequency measurements because they have wide bandwidth, high input impedance and low input capacitance. However, the probe ground leads provide a long ground loop that will produce errors in measurement. Instead, the probes can be grounded directly by removing the ground leads and probe jackets and using scope probe jacks.

COMPONENTS SELECTION AND FEEDBACK RESISTOR

It is important in high speed applications to keep all component leads short because wires are inductive at high frequency. For discrete components, choose carbon composition-type resistors and mica-type capacitors. Surface mount components are preferred over discrete components for minimum inductive effect.

Large values of feedback resistors can couple with parasitic capacitance and cause undesirable effects such as ringing or oscillation in high speed amplifiers. For LM6171, a feedback resistor of 510Ω gives optimal performance.

Compensation for Input Capacitance

The combination of an amplifier's input capacitance with the gain setting resistors adds a pole that can cause peaking or oscillation. To solve this problem, a feedback capacitor with a value

$$C_F > (R_G \times C_{IN})/R_F$$

can be used to cancel that pole. For LM6171, a feedback capacitor of 2 pF is recommended. *Figure 1* illustrates the compensation circuit.

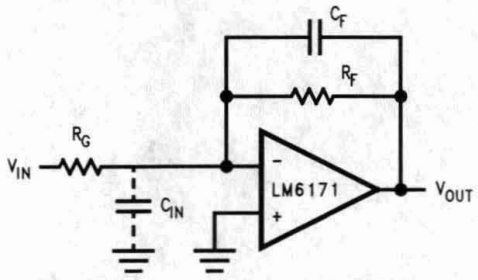

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FIGURE 1. Compensating for Input Capacitance

Power Supply Bypassing

Bypassing the power supply is necessary to maintain low power supply impedance across frequency. Both positive and negative power supplies should be bypassed individually by placing 0.01 μF ceramic capacitors directly to power supply pins and 2.2 μF tantalum capacitors close to the power supply pins.

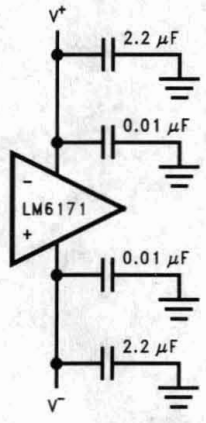

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FIGURE 2. Power Supply Bypassing

Application Information (Continued)

Termination

In high frequency applications, reflections occur if signals are not properly terminated. *Figure 3* shows a properly terminated signal while *Figure 4* shows an improperly terminated signal.

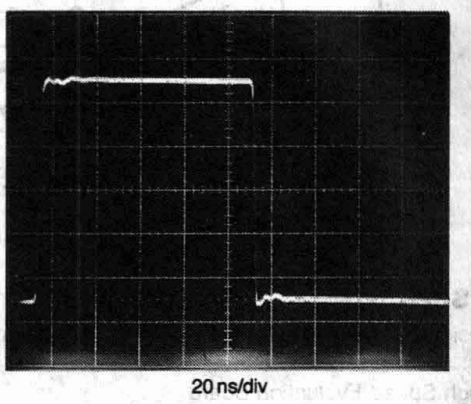

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FIGURE 3. Properly Terminated Signal

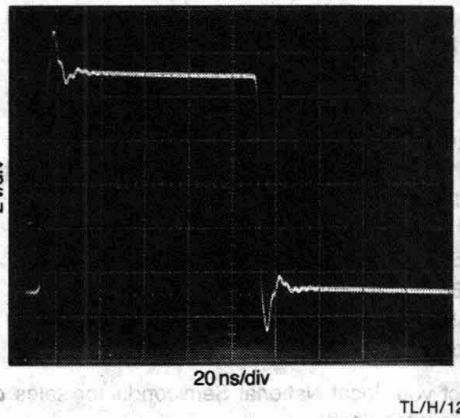

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FIGURE 4. Improperly Terminated Signal

To minimize reflection, coaxial cable with matching characteristic impedance to the signal source should be used. The other end of the cable should be terminated with the same value terminator or resistor. For the commonly used cables, RG59 has 75Ω characteristic impedance, and RG58 has 50Ω characteristic impedance.

Driving Capacitive Loads

Amplifiers driving capacitive loads can oscillate or have ringing at the output. To eliminate oscillation or reduce ringing, an isolation resistor can be placed as shown below in *Figure 5*. The combination of the isolation resistor and the load capacitor forms a pole to increase stablility by adding more phase margin to the overall system. The desired performance depends on the value of the isolation resistor; the bigger the isolation resistor, the more damped the pulse response becomes. For LM6171, a 50Ω isolation resistor is recommended for initial evaluation. *Figure 6* shows the LM6171 driving a 200 pF load with the 50Ω isolation resistor.

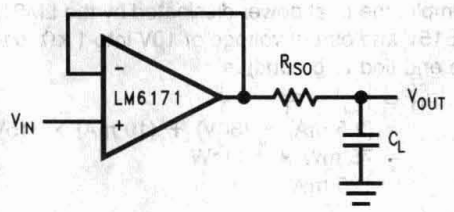

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FIGURE 5. Isolation Resistor Used to Drive Capacitive Load

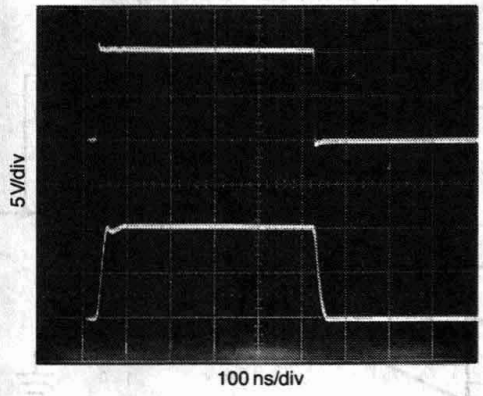

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FIGURE 6. The LM6171 Driving a 200 pF Load with a 50Ω Isolation Resistor

Power Dissipation

The maximum power allowed to dissipate in a device is defined as:

$$P_D = (T_{J(max)} - T_A)/\theta_{JA}$$

Where P_D is the power dissipation in a device
$T_{J(max)}$ is the maximum junction temperature
T_A is the ambient temperature
θ_{JA} is the thermal resistance of a particular package

For example, for the LM6171 in a SO-8 package, the maximum power dissipation at 25°C ambient temperature is 730 mW.

Thermal resistance, θ_{JA}, depends on parameters such as die size, package size and package material. The smaller the die size and package, the higher θ_{JA} becomes. The 8-pin DIP package has a lower thermal resistance (108°C/W) than that of 8-pin SO (172°C/W). Therefore, for higher dissipation capability, use an 8-pin DIP package.

The total power dissipated in a device can be calculated as:

$$P_D = P_Q + P_L$$

P_Q is the quiescent power dissipated in a device with no load connected at the output. P_L is the power dissipated in the device with a load connected at the output; it is not the power dissipated by the load.

Furthermore,

P_Q = supply current × total supply voltage with no load

P_L = output current × (voltage difference between supply voltage and output voltage of the same supply)

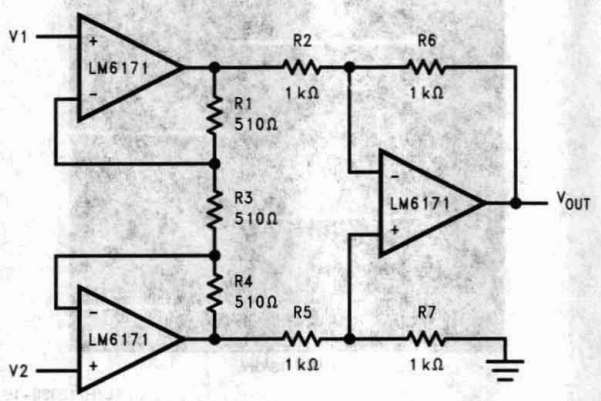
Application Information (Continued)

For example, the total power dissipated by the LM6171 with $V_S = \pm 15V$ and output voltage of 10V into 1 kΩ load resistor (one end tied to ground) is

$$P_D = P_Q + P_L$$
$$= (2.5\ mA) \times (30V) + (10\ mA) \times (15V - 10V)$$
$$= 75\ mW + 50\ mW$$
$$= 125\ mW$$

Application Circuits

Fast Instrumentation Amplifier



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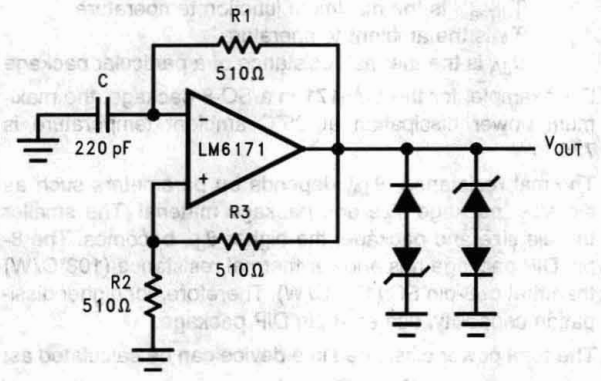
$V_{IN} = V2 - V1$

if R6 = R2, R7 = R5 and R1 = R4

$$\frac{V_{OUT}}{V_{IN}} = \frac{R6}{R2}\left(1 + 2\frac{R1}{R3}\right) = 3$$

Multivibrator



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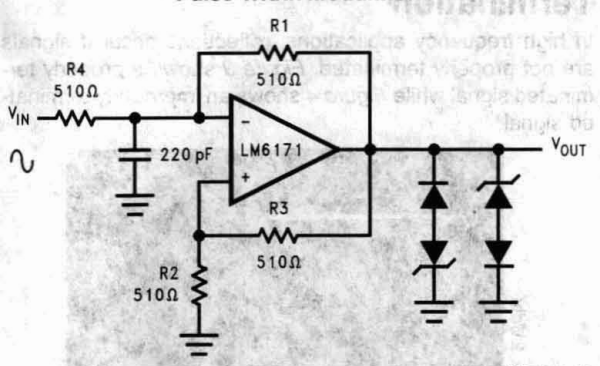
$$f = \frac{1}{2\left(R1C\ln\left(1 + 2\frac{R2}{R3}\right)\right)}$$

f = 4 MHz

Pulse Width Modulator



TL/H/12336–19

Design Kit

A design kit is available for the LM6171. The design kit contains:

- High Speed Evaluation Board
- LM6171 in 8-pin DIP Package
- LM6171 Datasheet
- Pspice Macromodel Diskette With the LM6171 Macromodel
- An Amplifier Selection Guide

Pitch Pack

A pitch pack is available for the LM6171. The pitch pack contains:

- High Speed Evaluation Board
- LM6171 in 8-pin DIP Package
- LM6171 Datasheet
- Pspice Macromodel Diskette With the LM6171 Macromodel

Contact your local National Semiconductor sales office to obtain a pitch pack.

National Semiconductor

LM6181 100 mA, 100 MHz Current Feedback Amplifier

General Description

The LM6181 current-feedback amplifier offers an unparalleled combination of bandwidth, slew-rate, and output current. The amplifier can directly drive up to 100 pF capacitive loads without oscillating and a 10V signal into a 50Ω or 75Ω back-terminated coax cable system over the full industrial temperature range. This represents a radical enhancement in output drive capability for an 8-pin DIP high-speed amplifier making it ideal for video applications.

Built on National's advanced high-speed VIP™ II (Vertically Integrated PNP) process, the LM6181 employs current-feedback providing bandwidth that does not vary dramatically with gain; 100 MHz at $A_V = -1$, 60 MHz at $A_V = -10$. With a slew rate of 2000V/μs, 2nd harmonic distortion of −50 dBc at 10 MHz and settling time of 50 ns (0.1%) the LM6181 dynamic performance makes it ideal for data acquisition, high speed ATE, and precision pulse amplifier applications.

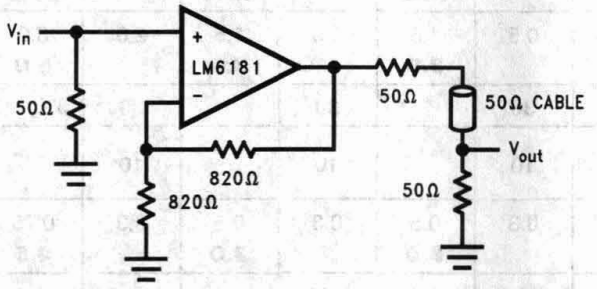
Features (Typical unless otherwise noted)

- Slew rate 2000 V/μs
- Settling time (0.1%) 50 ns
- Characterized for supply ranges ±5V and ±15V
- Low differential gain and phase error 0.05%, 0.04°
- High output drive ±10V into 100Ω
- Guaranteed bandwidth and slew rate
- Improved performance over EL2020, OP160, AD844, LT1223 and HA5004

Applications

- Coax cable driver
- Video amplifier
- Flash ADC buffer
- High frequency filter
- Scanner and Imaging systems

Typical Application



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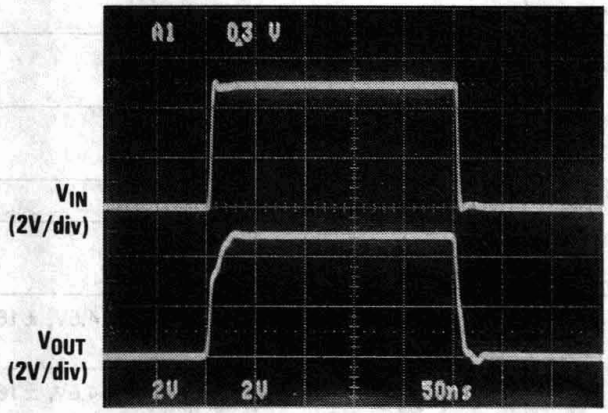
Cable Driver



TIME (50ns/div)

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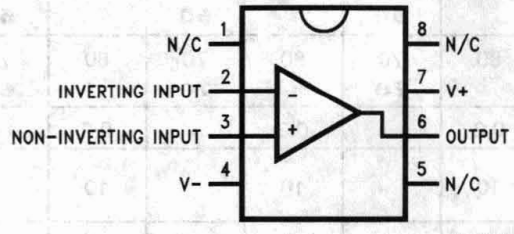
Connection Diagrams (For Ordering Information See Back Page)

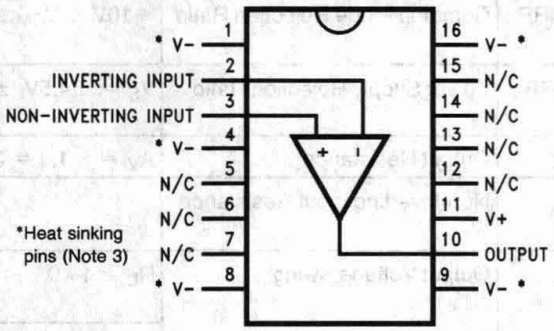
8-Pin Dual-In-Line Package (N)/ Small Outline (M-8)



TL/H/11328–3

Order Number LM6181IN, LM6181AIN, LM6181AMN, LM6181AIM-8, LM6181IM-8 or LM6181AMJ/883
See NS Package Number J08A, M08A or N08E

16-Pin Small Outline Package (M)



TL/H/11328–4

Order Number LM6181IM or LM6181AIM
See NS Package Number M16A

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	±18V
Differential Input Voltage	±6V
Input Voltage	±Supply Voltage
Inverting Input Current	15 mA
Soldering Information	
Dual-In-Line Package (N) Soldering (10 sec)	260°C
Small Outline Package (M)	
Vapor Phase (60 seconds)	215°C
Infrared (15 seconds)	220°C
Output Short Circuit	(Note 7)
Storage Temperature Range	$-65°C \le T_J \le +150°C$
Maximum Junction Temperature	150°C
ESD Rating (Note 2)	±3000V

Operating Ratings

Supply Voltage Range	7V to 32V
Junction Temperature Range (Note 3)	
LM6181AM	$-55°C \le T_J \le +125°C$
LM6181AI, LM6181I	$-40°C \le T_J \le +85°C$
Thermal Resistance (θ_{JA}, θ_{JC})	
8-pin DIP (N)	102°C/W, 42°C/W
8-pin SO (M-8)	153°C/W, 42°C/W
16-pin SO (M)	70°C/W, 38°C/W

±15V DC Electrical Characteristics

The following specifications apply for Supply Voltage = ±15V, R_F = 820Ω, and R_L = 1 kΩ unless otherwise noted. **Boldface** limits apply at the temperature extremes; all other limits T_J = 25°C.

Symbol	Parameter	Conditions	LM6181AM		LM6181AI		LM6181I		Units
			Typical (Note 4)	Limit (Note 5)	Typical (Note 4)	Limit (Note 5)	Typical (Note 4)	Limit (Note 5)	
V_{OS}	Input Offset Voltage		2.0	3.0 **4.0**	2.0	3.0 **3.5**	3.5	5.0 **5.5**	mV max
TC V_{OS}	Input Offset Voltage Drift		5.0		5.0		5.0		µV/°C
I_B	Inverting Input Bias Current		2.0	5.0 **12.0**	2.0	5.0 **12.0**	5.0	10 **17.0**	µA max
	Non-Inverting Input Bias Current		0.5	1.5 **3.0**	0.5	1.5 **3.0**	2.0	3.0 **5.0**	
TC I_B	Inverting Input Bias Current Drift		30		30		30		nA/°C
	Non-Inverting Input Bias Current Drift		10		10		10		
I_B PSR	Inverting Input Bias Current Power Supply Rejection	V_S = ±4.5V, ±16V	0.3	0.5 **3.0**	0.3	0.5 **3.0**	0.3	0.75 **4.5**	µA/V max
	Non-Inverting Input Bias Current Power Supply Rejection	V_S = ±4.5V, ±16V	0.05	0.5 **1.5**	0.05	0.5 **1.5**	0.05	0.5 **3.0**	
I_B CMR	Inverting Input Bias Current Common Mode Rejection	$-10V \le V_{CM} \le +10V$	0.3	0.5 **0.75**	0.3	0.5 **0.75**	0.3	0.75 **1.0**	
	Non-Inverting Input Bias Current Common Mode Rejection	$-10V \le V_{CM} \le +10V$	0.1	0.5 **0.5**	0.1	0.5 **0.5**	0.1	0.5 **0.5**	
CMRR	Common Mode Rejection Ratio	$-10V \le V_{CM} \le +10V$	60	50 **50**	60	50 **50**	60	50 **50**	dB min
PSRR	Power Supply Rejection Ratio	V_S = ±4.5V, ±16V	80	70 **70**	80	70 **70**	80	70 **65**	dB min
R_O	Output Resistance	A_V = −1, f = 300 kHz	0.2		0.2		0.2		Ω
R_{IN}	Non-Inverting Input Resistance		10		10		10		MΩ min
V_O	Output Voltage Swing	R_L = 1 kΩ	12	11 **11**	12	11 **11**	12	11 **11**	V min
		R_L = 100Ω	11	10 **7.5**	11	10 **8.0**	11	10 **8.0**	
I_{SC}	Output Short Circuit Current		130	100 **75**	130	100 **85**	130	100 **85**	mA min

±15V DC Electrical Characteristics (Continued)

The following specifications apply for Supply Voltage = ±15V, R_F = 820Ω, and R_L = 1 kΩ unless otherwise noted. **Boldface** limits apply at the temperature extremes; all other limits T_J = 25°C.

Symbol	Parameter	Conditions	LM6181AM		LM6181AI		LM6181I		Units
			Typical (Note 4)	Limit (Note 5)	Typical (Note 4)	Limit (Note 5)	Typical (Note 4)	Limit (Note 5)	
Z_T	Transimpedance	R_L = 1 kΩ	1.8	1.0 **0.5**	1.8	1.0 **0.5**	1.8	0.8 **0.4**	MΩ min
		R_L = 100Ω	1.4	0.8 **0.4**	1.4	0.8 **0.4**	1.4	0.7 **0.35**	
I_S	Supply Current	No Load, V_O = 0V	7.5	10 **10**	7.5	10 **10**	7.5	10 **10**	mA max
V_{CM}	Input Common Mode Voltage Range		V^+ − 1.7V V^- + 1.7V		V^+ − 1.7V V^- + 1.7V		V^+ − 1.7V V^- + 1.7V		V

±15V AC Electrical Characteristics

The following specifications apply for Supply Voltage = ±15V, R_F = 820Ω, R_L = 1 kΩ unless otherwise noted. **Boldface** limits apply at the temperature extremes; all other limits T_J = 25°C.

Symbol	Parameter	Conditions	LM6181AM		LM6181AI		LM6181I		Units
			Typical (Note 4)	Limit (Note 5)	Typical (Note 4)	Limit (Note 5)	Typical (Note 4)	Limit (Note 5)	
BW	Closed Loop Bandwidth −3 dB	A_V = +2	100		100		100		MHz min
		A_V = +10	80		80		80		
		A_V = −1	100	80	100	80	100	80	
		A_V = −10	60		60		60		
PBW	Power Bandwidth	A_V = −1, V_O = 5 V_{PP}	60		60		60		
SR	Slew Rate	Overdriven	2000		2000		2000		V/μs min
		A_V = −1, V_O = ±10V, R_L = 150Ω (Note 6)	1400	1000	1400	1000	1400	1000	
t_s	Settling Time (0.1%)	A_V = −1, V_O = ±5V R_L = 150Ω	50		50		50		ns
t_r, t_f	Rise and Fall Time	V_O = 1 V_{PP}	5		5		5		
t_p	Propagation Delay Time	V_O = 1 V_{PP}	6		6		6		
$i_{n(+)}$	Non-Inverting Input Noise Current Density	f = 1 kHz	3		3		3		pA/√Hz
$i_{n(-)}$	Inverting Input Noise Current Density	f = 1 kHz	16		16		16		pA/√Hz
e_n	Input Noise Voltage Density	f = 1 kHz	4		4		4		nV/√Hz
	Second Harmonic Distortion	2 V_{PP}, 10 MHz	−50		−50		−50		dBc
	Third Harmonic Distortion	2 V_{PP}, 10 MHz	−55		−55		−50		
	Differential Gain	R_L = 150Ω A_V = +2 NTSC	0.05		0.05		0.05		%
	Differential Phase	R_L = 150Ω A_V = +2 NTSC	0.04		0.04		0.04		Deg

±5V DC Electrical Characteristics

The following specifications apply for Supply Voltage = ±5V, R_F = 820Ω, and R_L = 1 kΩ unless otherwise noted. **Boldface** limits apply at the temperature extremes; all other limits T_J = 25°C.

Symbol	Parameter	Conditions	LM6181AM		LM6181AI		LM6181I		Units
			Typical (Note 4)	Limit (Note 5)	Typical (Note 4)	Limit (Note 5)	Typical (Note 4)	Limit (Note 5)	
V_{OS}	Input Offset Voltage		1.0	2.0 **3.0**	1.0	2.0 **2.5**	1.0	3.0 **3.5**	mV max
TC V_{OS}	Input Offset Voltage Drift		2.5		2.5		2.5		µV/°C
I_B	Inverting Input Bias Current		5.0	10 **22**	5.0	10 **22**	5.0	17.5 **27.0**	µA max
	Non-Inverting Input Bias Current		0.25	1.5 **1.5**	0.25	1.5 **1.5**	0.25	3.0 **5.0**	
TC I_B	Inverting Input Bias Current Drift		50		50		50		nA/°C
	Non-Inverting Input Bias Current Drift		3.0		3.0		3.0		
I_B PSR	Inverting Input Bias Current Power Supply Rejection	V_S = ±4.0V, ±6.0V	0.3	0.5 **0.5**	0.3	0.5 **0.5**	0.3	1.0 **1.0**	µA/V max
	Non-Inverting Input Bias Current Power Supply Rejection	V_S = ±4.0V, ±6.0V	0.05	0.5 **0.5**	0.05	0.5 **0.5**	0.05	0.5 **0.5**	
I_B CMR	Inverting Input Bias Current Common Mode Rejection	−2.5V ≤ V_{CM} ≤ +2.5V	0.3	0.5 **1.0**	0.3	0.5 **1.0**	0.3	1.0 **1.5**	
	Non-Inverting Input Bias Current Common Mode Rejection	−2.5V ≤ V_{CM} ≤ +2.5V	0.12	0.5 **1.0**	0.12	0.5 **0.5**	0.12	0.5 **0.5**	
CMRR	Common Mode Rejection Ratio	−2.5V ≤ V_{CM} ≤ +2.5V	57	50 **47**	57	50 **47**	57	50 **47**	dB min
PSRR	Power Supply Rejection Ratio	V_S = ±4.0V, ±6.0V	80	70 **70**	80	70 **70**	80	64 **64**	
R_O	Output Resistance	A_V = −1, f = 300 kHz	0.25		0.25		0.25		Ω
R_{IN}	Non-Inverting Input Resistance		8		8		8		MΩ min
V_O	Output Voltage Swing	R_L = 1 kΩ	2.6	2.25 **2.2**	2.6	2.25 **2.25**	2.6	2.25 **2.25**	V min
		R_L = 100Ω	2.2	2.0 **2.0**	2.2	2.0 **2.0**	2.2	2.0 **2.0**	
I_{SC}	Output Short Circuit Current		100	75 **70**	100	75 **70**	100	75 **70**	mA min
Z_T	Transimpedance	R_L = 1 kΩ	1.4	0.75 **0.35**	1.4	0.75 **0.4**	1.0	0.6 **0.3**	MΩ min
		R_L = 100Ω	1.0	0.5 **0.25**	1.0	0.5 **0.25**	1.0	0.4 **0.2**	
I_S	Supply Current	No Load, V_O = 0V	6.5	8.5 **8.5**	6.5	8.5 **8.5**	6.5	8.5 **8.5**	mA max
V_{CM}	Input Common Mode Voltage Range		V^+ − 1.7V V^- + 1.7V		V^+ − 1.7V V^- + 1.7V		V^+ − 1.7V V^- + 1.7V		V

±5V AC Electrical Characteristics

The following specifications apply for Supply Voltage = ±5V, R_F = 820Ω, and R_L = 1 kΩ unless otherwise noted. **Boldface** limits apply at the temperature extremes; all other limits T_J = 25°C.

Symbol	Parameter	Conditions	LM6181AM		LM6181AI		LM6181I		Units
			Typical (Note 4)	Limit (Note 5)	Typical (Note 4)	Limit (Note 5)	Typical (Note 4)	Limit (Note 5)	
BW	Closed Loop Bandwidth −3 dB	A_V = +2	50		50		50		MHZ min
		A_V = +10	40		40		40		
		A_V = −1	55	35	55	35	55	35	
		A_V = −10	35		35		35		
PBW	Power Bandwidth	A_V = −1, V_O = 4 V_{PP}	40		40		40		
SR	Slew Rate	A_V = −1, V_O = ±2V, R_L = 150Ω (Note 6)	500	375	500	375	500	375	V/μs min
t_s	Settling Time (0.1%)	A_V = −1, V_O = ±2V R_L = 150Ω	50		50		50		ns
t_r, t_f	Rise and Fall Time	V_O = 1 V_{PP}	8.5		8.5		8.5		
t_p	Propagation Delay Time	V_O = 1 V_{PP}	8		8		8		
$i_{n(+)}$	Non-Inverting Input Noise Current Density	f = 1 kHz	3		3		3		pA/√Hz
$i_{n(-)}$	Inverting Input Noise Current Density	f = 1 kHz	16		16		16		pA/√Hz
e_n	Input Noise Voltage Density	f = 1 kHz	4		4		4		nV/√Hz
	Second Harmonic Distortion	2 V_{PP}, 10 MHz	−45		−45		−45		dBc
	Third Harmonic Distortion	2 V_{PP}, 10 MHz	−55		−55		−55		
	Differential Gain	R_L = 150Ω A_V = +2 NTSC	0.063		0.063		0.063		%
	Differential Phase	R_L = 150Ω A_V = +2 NTSC	0.16		0.16		0.16		Deg

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating ratings indicate conditions the device is intended to be functional, but device parameter specifications may not be guaranteed under these conditions. For guaranteed specifications and test conditions, see the Electrical Characteristics.

Note 2: Human body model 100 pF and 1.5 kΩ.

Note 3: The typical junction-to-ambient thermal resistance of the molded plastic DIP(N) package soldered directly into a PC board is 102°C/W. The junction-to-ambient thermal resistance of the S.O. surface mount (M) package mounted flush to the PC board is 70°C/W when pins 1, 4, 8, 9 and 16 are soldered to a total 2 in^2 1 oz. copper trace. The 16-pin S.O. (M) package must have pin 4 and at least one of pins 1, 8, 9, or 16 connected to V^- for proper operation. The typical junction-to-ambient thermal resistance of the S.O. (M-8) package soldered directly into a PC board is 153°C/W.

Note 4: Typical values represent the most likely parametric norm.

Note 5: All limits guaranteed at room temperature (standard type face) or at operating temperature extremes (**bold face type**).

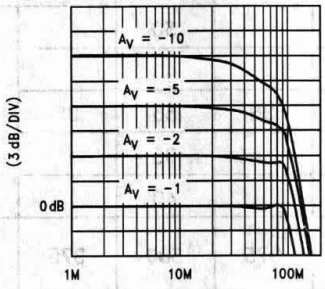
Note 6: Measured from +25% to +75% of output waveform.

Note 7: Continuous short circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 150°C. Output currents in excess of ±130 mA over a long term basis may adversely affect reliability.

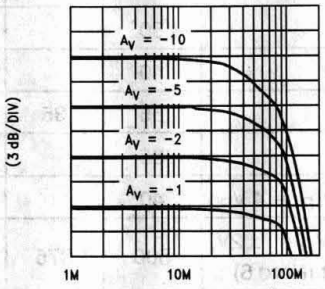
Note 8: For guaranteed Military Temperature Range parameters see RETS6181X.

Typical Performance Characteristics T_A = 25°C unless otherwise noted

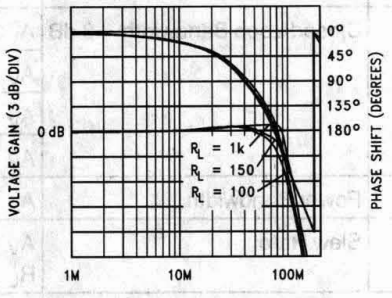
CLOSED-LOOP FREQUENCY RESPONSE
$V_S = \pm 15V$; $R_f = 820\Omega$; $R_L = 1\,k\Omega$



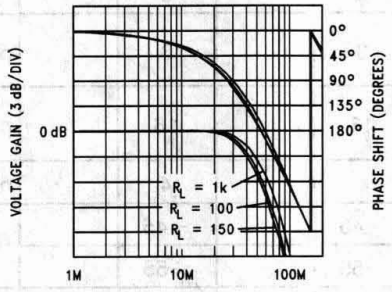
CLOSED-LOOP FREQUENCY RESPONSE
$V_S = \pm 15V$; $R_f = 820\Omega$; $R_L = 150\Omega$



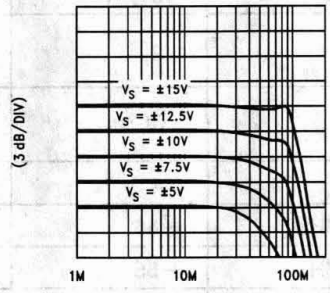
UNITY GAIN FREQUENCY RESPONSE
$V_S = \pm 15V$; $A_V = +1$; $R_f = 820\Omega$



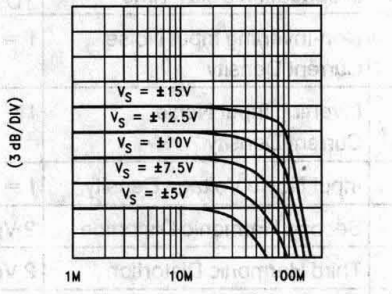
UNIT GAIN FREQUENCY RESPONSE
$V_S = \pm 5V$; $A_V = +1$; $R_f = 820\Omega$



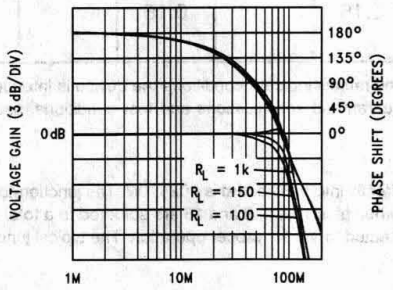
FREQUENCY RESPONSE vs SUPPLY VOLTAGE
$A_V = -1$; $R_f = 820\Omega$; $R_L = 1\,k\Omega$



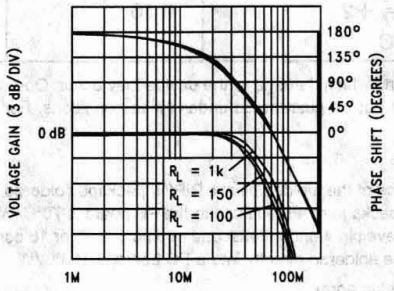
FREQUENCY RESPONSE vs SUPPLY VOLTAGE
$A_V = -1$; $R_f = 820\Omega$; $R_L = 150\Omega$



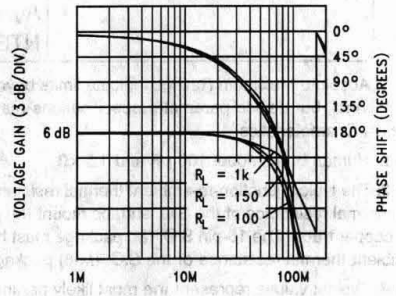
INVERTING GAIN FREQUENCY RESPONSE
$V_S = \pm 15V$; $A_V = -1$; $R_f = 820\Omega$



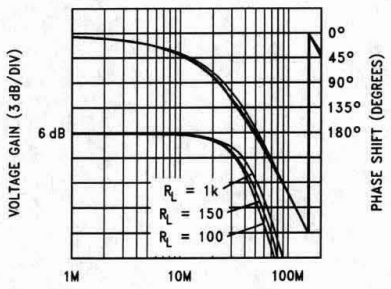
INVERTING GAIN FREQUENCY RESPONSE
$V_S = \pm 5V$; $A_V = -1$; $R_f = 820\Omega$



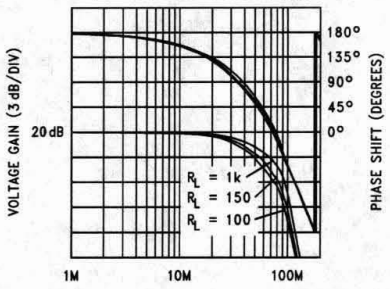
NON-INVERTING GAIN FREQUENCY RESPONSE
$V_S = \pm 15V$; $A_V = +2$; $R_f = 820\Omega$



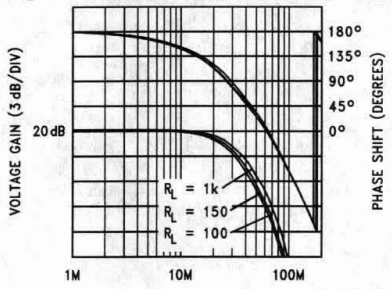
NON-INVERTING GAIN FREQUENCY RESPONSE
$V_S = \pm 5V$; $A_V = +2$; $R_f = 820\Omega$



INVERTING GAIN FREQUENCY RESPONSE
$V_S = \pm 15V$; $A_V = -10$; $R_f = 820\Omega$



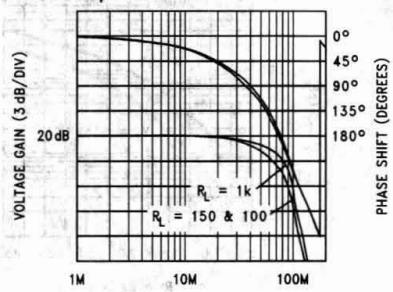
INVERTING GAIN FREQUENCY RESPONSE
$V_S = \pm 5V$; $A_V = -10$; $R_f = 820\Omega$



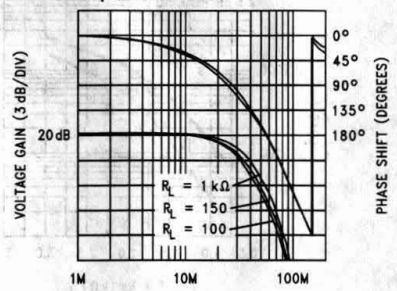
TL/H/11328–5

Typical Performance Characteristics $T_A = 25°C$ unless otherwise noted (Continued)

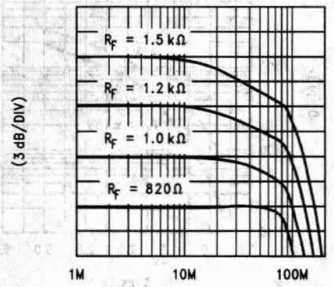
NON-INVERTING GAIN FREQUENCY RESPONSE
$V_S = \pm 15V$; $A_V = +10$;
$R_f = 820\Omega$



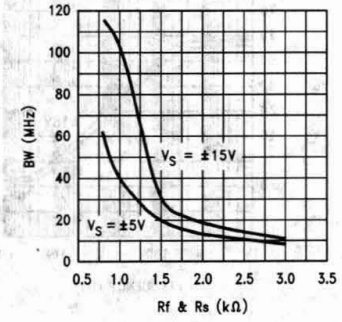
NON-INVERTING GAIN FREQUENCY RESPONSE
$V_S = \pm 5V$; $A_V = +10$;
$R_f = 820\Omega$



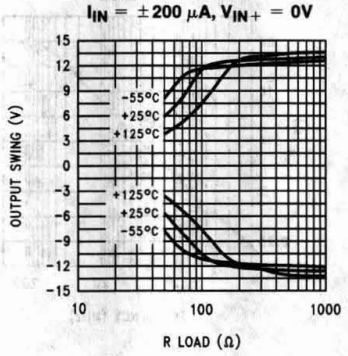
NON-INVERTING GAIN FREQUENCY COMPENSATION
$V_S = \pm 15V$; $A_V = +2$;
$R_L = 150\Omega$



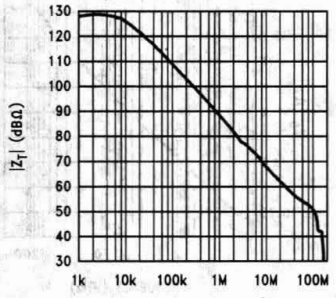
BANDWIDTH vs R_f & R_S
$A_V = -1$, $R_L = 1\ k\Omega$



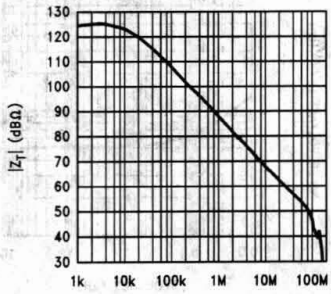
OUTPUT SWING vs R_{LOAD} PULSED, $V_S = \pm 15V$, $I_{IN} = \pm 200\ \mu A$, $V_{IN+} = 0V$



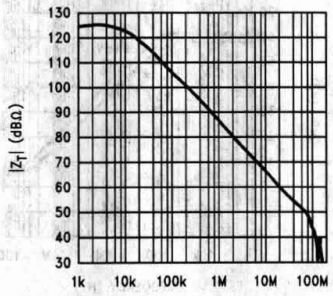
TRANSIMPEDANCE vs FREQUENCY
$V_S = \pm 15V$
$R_L = 1\ k\Omega$



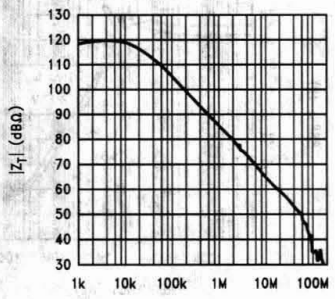
TRANSIMPEDANCE vs FREQUENCY
$V_S = \pm 15V$
$R_L = 100\Omega$



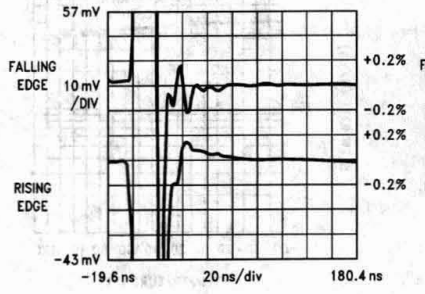
TRANSIMPEDANCE vs FREQUENCY
$V_S = \pm 5V$
$R_L = 1\ k\Omega$



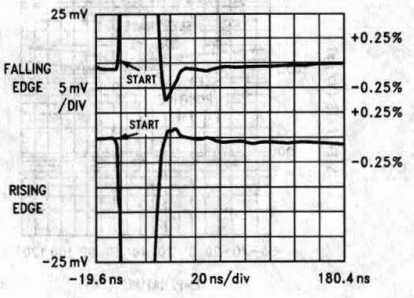
TRANSIMPEDANCE vs FREQUENCY
$V_S = \pm 5V$
$R_L = 100\Omega$



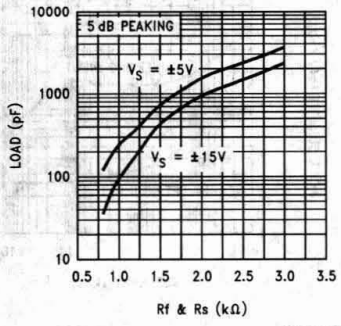
SETTLING RESPONSE
$V_S = \pm 15V$; $R_L = 150\Omega$;
$V_O = \pm 5V$; $A_V = -1$



SETTLING RESPONSE
$V_S = \pm 5V$; $R_L = 150\Omega$;
$V_O = \pm 2V$; $A_V = -1$



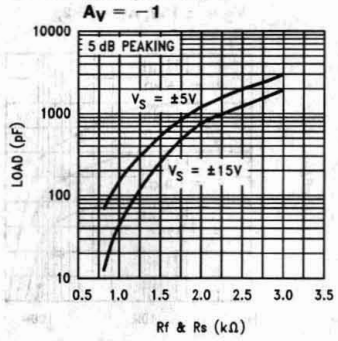
SUGGESTED R_f and R_S for C_L
$A_V = -1$; $R_L = 150\Omega$



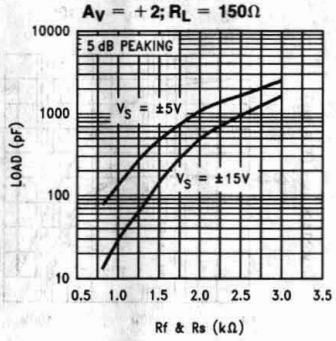
TL/H/11328–6

Typical Performance Characteristics $T_A = 25°C$ unless otherwise noted (Continued)

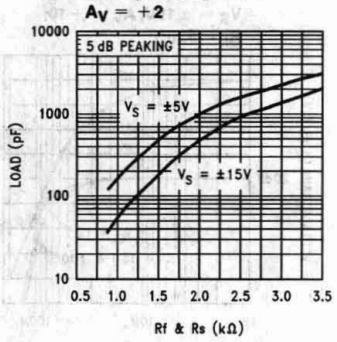
SUGGESTED R_f and R_S FOR C_L
$A_V = -1$



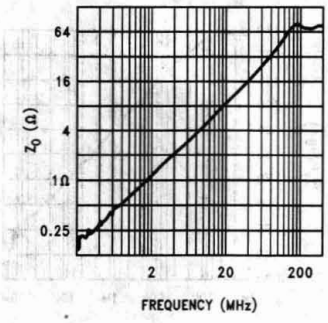
SUGGESTED R_f and R_S FOR C_L
$A_V = +2$; $R_L = 150\Omega$



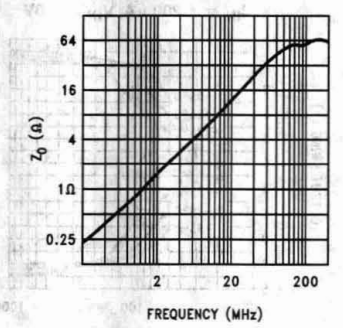
SUGGESTED R_f and R_S FOR C_L
$A_V = +2$



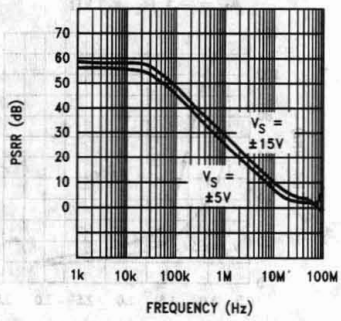
OUTPUT IMPEDANCE vs FREQ
$V_S = \pm 15V$; $A_V = -1$
$R_f = 820\Omega$



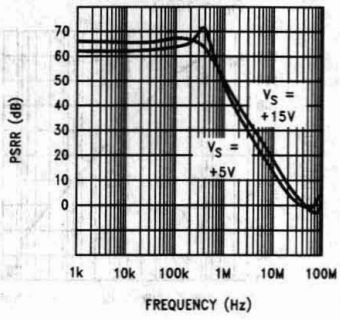
OUTPUT IMPEDANCE vs FREQ
$V_S = \pm 5V$; $A_V = -1$
$R_f = 820\Omega$



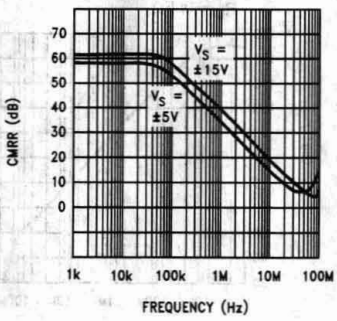
PSRR (V_S^+) vs FREQUENCY



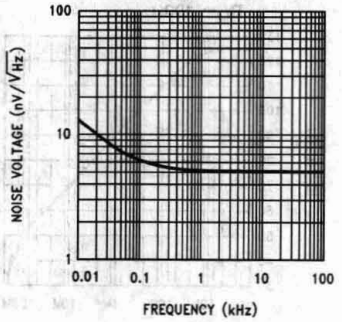
PSRR (V_S^-) vs FREQUENCY



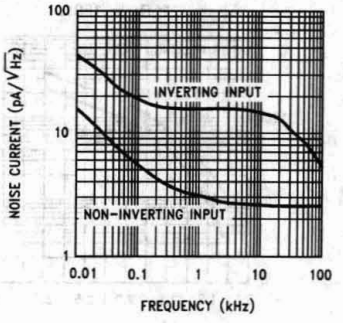
CMRR vs FREQUENCY



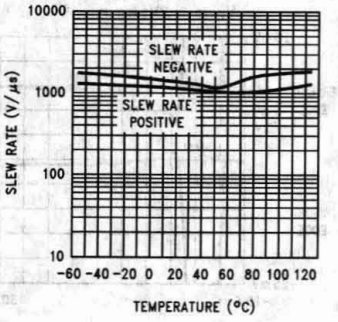
INPUT VOLTAGE NOISE vs FREQUENCY



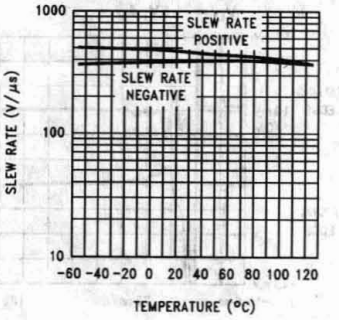
INPUT CURRENT NOISE vs FREQUENCY



SLEW RATE vs TEMPERATURE $A_V = -1$; $R_L = 150\Omega$, $V_S = \pm 15V$



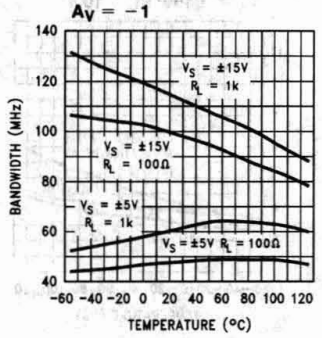
SLEW RATE vs TEMPERATURE $A_V = -1$; $R_L = 150\Omega$, $V_S = \pm 5V$



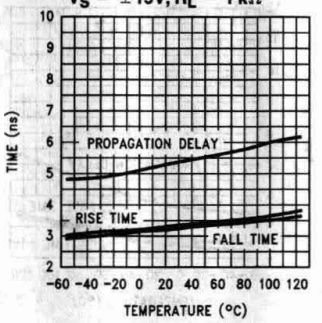
TL/H/11328–7

Typical Performance Characteristics $T_A = 25°C$ unless otherwise noted (Continued)

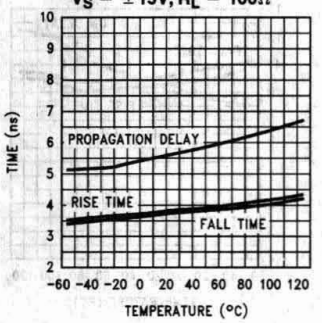
−3 dB BANDWIDTH vs TEMPERATURE $A_V = -1$



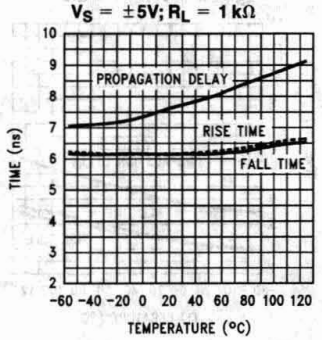
SMALL SIGNAL PULSE RESPONSE vs TEMP, $A_V = +1$ $V_S = \pm15V$; $R_L = 1\,k\Omega$



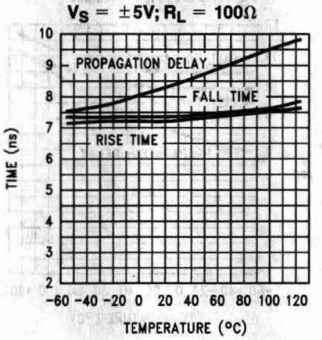
SMALL SIGNAL PULSE RESPONSE vs TEMP, $A_V = +1$ $V_S = \pm15V$; $R_L = 100\Omega$



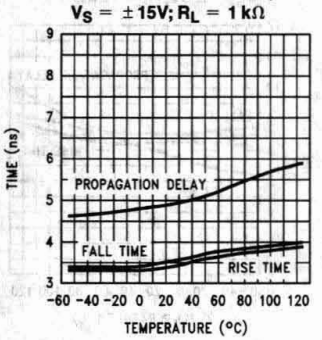
SMALL SIGNAL PULSE RESPONSE vs TEMP, $A_V = +1$ $V_S = \pm5V$; $R_L = 1\,k\Omega$



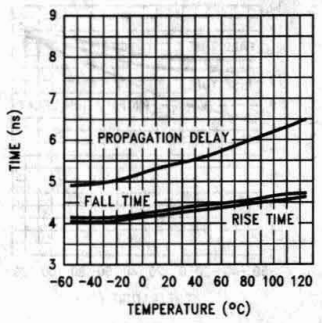
SMALL SIGNAL PULSE RESPONSE vs TEMP, $A_V = +1$ $V_S = \pm5V$; $R_L = 100\Omega$



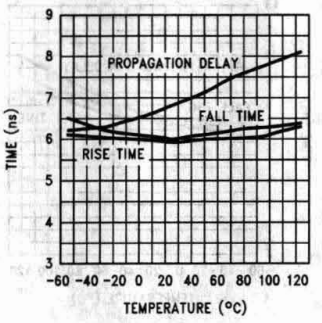
SMALL SIGNAL PULSE RESPONSE vs TEMP, $A_V = -1$ $V_S = \pm15V$; $R_L = 1\,k\Omega$



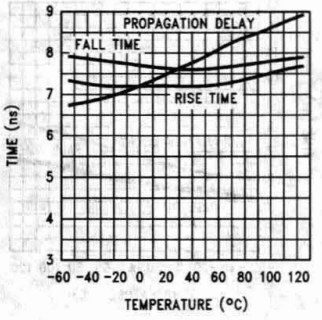
SMALL SIGNAL PULSE RESPONSE vs TEMP, $A_V = -1$ $V_S = \pm15V$; $R_L = 100\Omega$



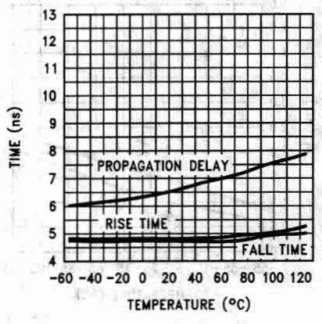
SMALL SIGNAL PULSE RESPONSE vs TEMP, $A_V = -1$ $V_S = \pm5V$; $R_L = 1\,k\Omega$



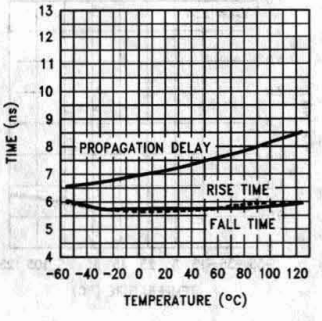
SMALL SIGNAL PULSE RESPONSE vs TEMP, $A_V = -1$ $V_S = \pm5V$; $R_L = 100\Omega$



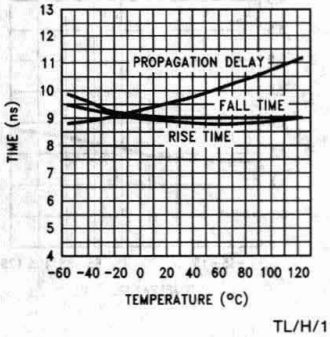
SMALL SIGNAL PULSE RESPONSE vs TEMP, $A_V = +2$ $V_S = \pm15V$; $R_L = 1\,k\Omega$



SMALL SIGNAL PULSE RESPONSE vs TEMP, $A_V = +2$ $V_S = \pm15V$; $R_L = 100\Omega$



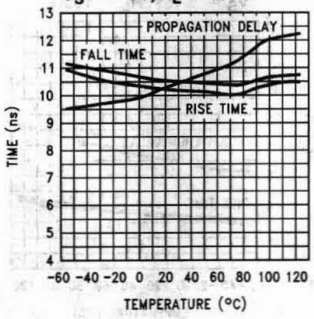
SMALL SIGNAL PULSE RESPONSE vs TEMP, $A_V = +2$ $V_S = \pm5V$; $R_L = 1\,k\Omega$



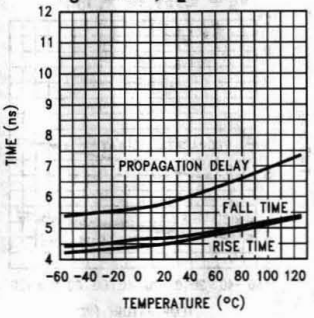
TL/H/11328–29

Typical Performance Characteristics T_A = 25°C unless otherwise noted (Continued)

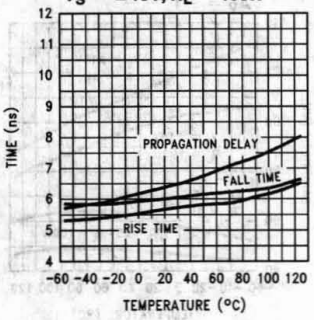
SMALL SIGNAL PULSE RESPONSE vs TEMP, A_V = +2
V_S = ±5V; R_L = 100Ω



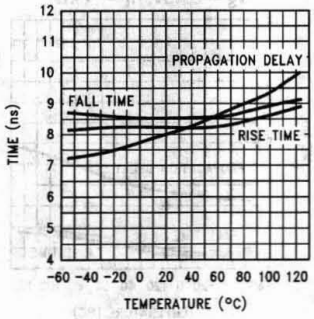
SMALL SIGNAL PULSE RESPONSE vs TEMP, A_V = −10
V_S = ±15V; R_L = 1 kΩ



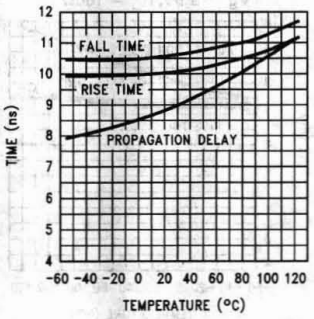
SMALL SIGNAL PULSE RESPONSE vs TEMP, A_V = −10
V_S = ±15V; R_L = 100Ω



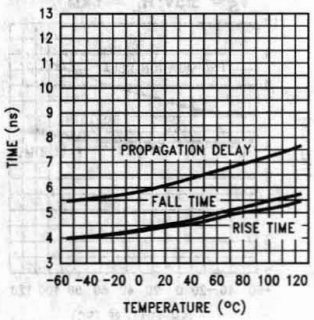
SMALL SIGNAL PULSE RESPONSE vs TEMP, A_V = −10
V_S = ±5V; R_L = 1 kΩ



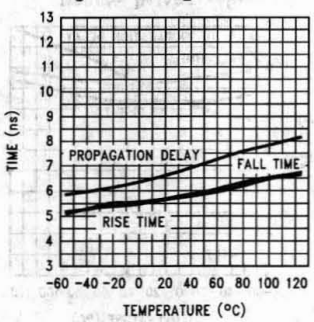
SMALL SIGNAL PULSE RESPONSE vs TEMP, A_V = −10
V_S = ±5V; R_L = 100Ω



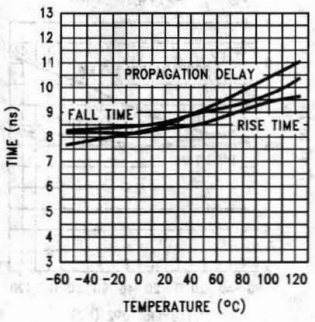
SMALL SIGNAL PULSE RESPONSE vs TEMP, A_V = +10
V_S = ±15V; R_L = 1 kΩ



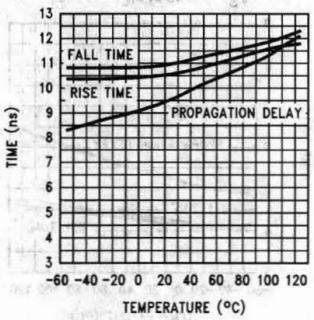
SMALL SIGNAL PULSE RESPONSE vs TEMP, A_V = +10
V_S = ±15V; R_L = 100Ω



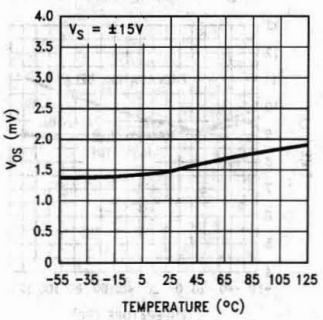
SMALL SIGNAL PULSE RESPONSE vs TEMP, A_V = +10
V_S = ±5V; R_L = 1 kΩ



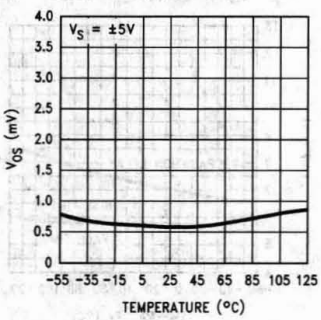
SMALL SIGNAL PULSE RESPONSE vs TEMP, A_V = +10
V_S = ±5V; R_L = 100Ω



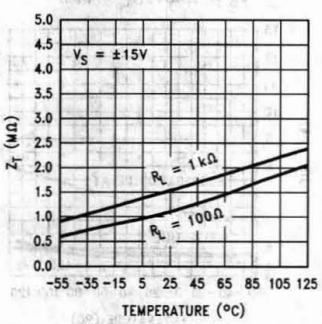
OFFSET VOLTAGE vs TEMPERATURE



OFFSET VOLTAGE vs TEMPERATURE



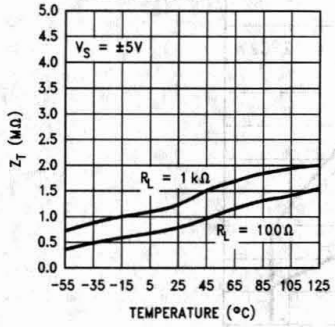
TRANSIMPEDANCE vs TEMPERATURE



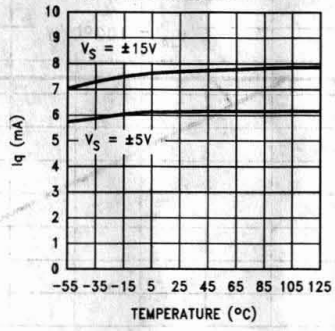
TL/H/11328–8

Typical Performance Characteristics $T_A = 25°C$ unless otherwise noted (Continued)

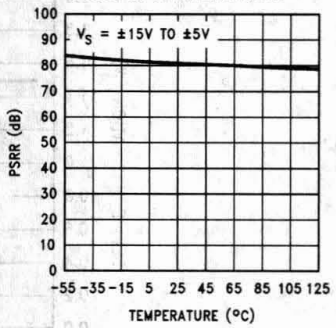
TRANSIMPEDANCE vs TEMPERATURE



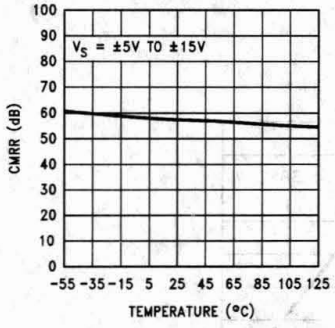
QUIESCENT CURRENT vs TEMPERATURE



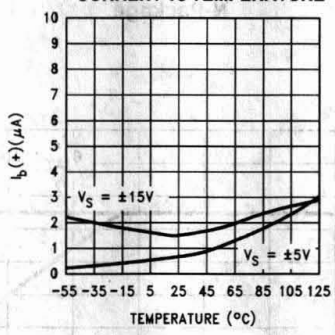
PSRR vs TEMPERATURE



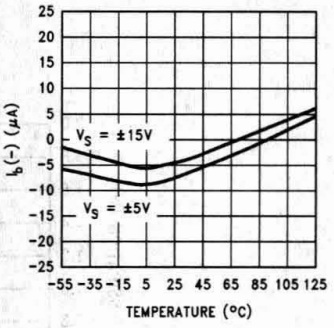
CMRR vs TEMPERATURE



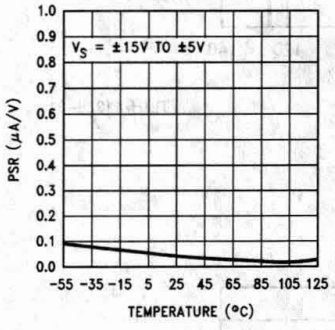
NON-INVERTING BIAS CURRENT vs TEMPERATURE



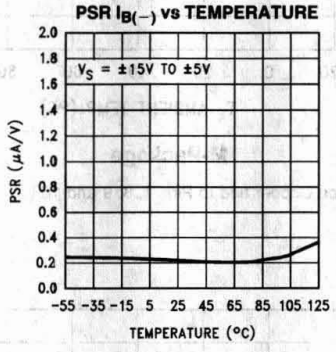
INVERTING BIAS CURRENT vs TEMPERATURE



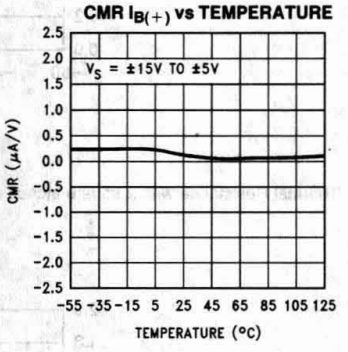
PSR $I_{B(+)}$ vs TEMPERATURE



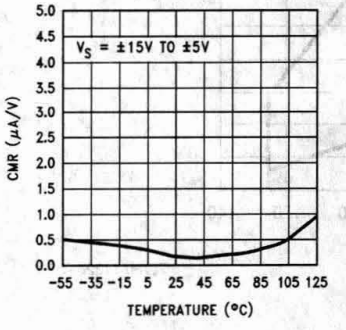
PSR $I_{B(-)}$ vs TEMPERATURE



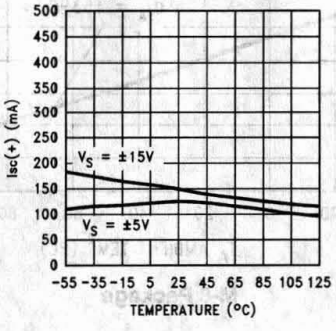
CMR $I_{B(+)}$ vs TEMPERATURE



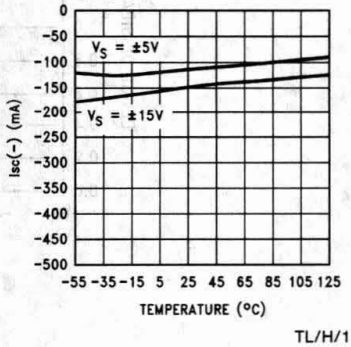
CMR $I_{B(-)}$ vs TEMPERATURE



$I_{SC(+)}$ vs TEMPERATURE



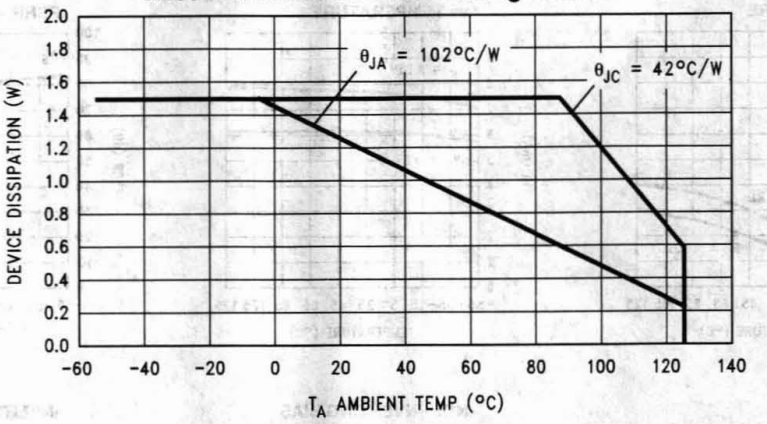
$I_{SC(-)}$ vs TEMPERATURE



TL/H/11328–9

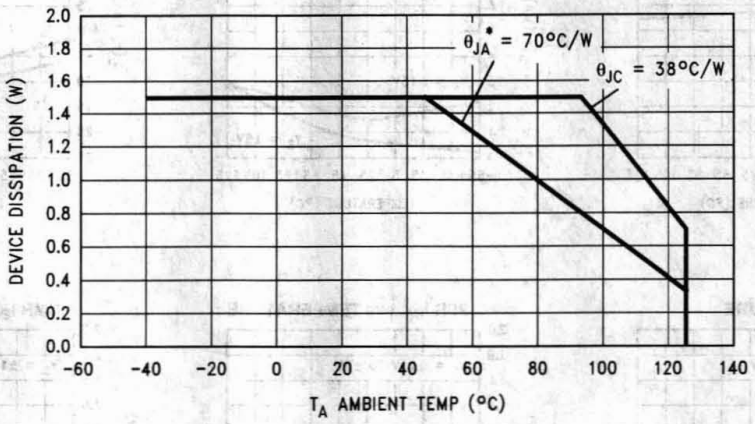
Typical Performance Characteristics

Absolute Maximum Power Derating Curves



TL/H/11328-30

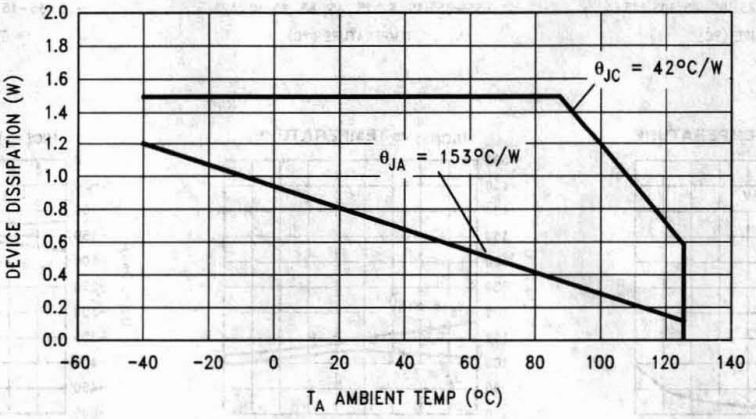
N-Package



TL/H/11328-31

M-Package

*θ_{JA} = Thermal Resistance with 2 square inches of 1 ounce Copper tied to Pins 1, 8, 9 and 16.

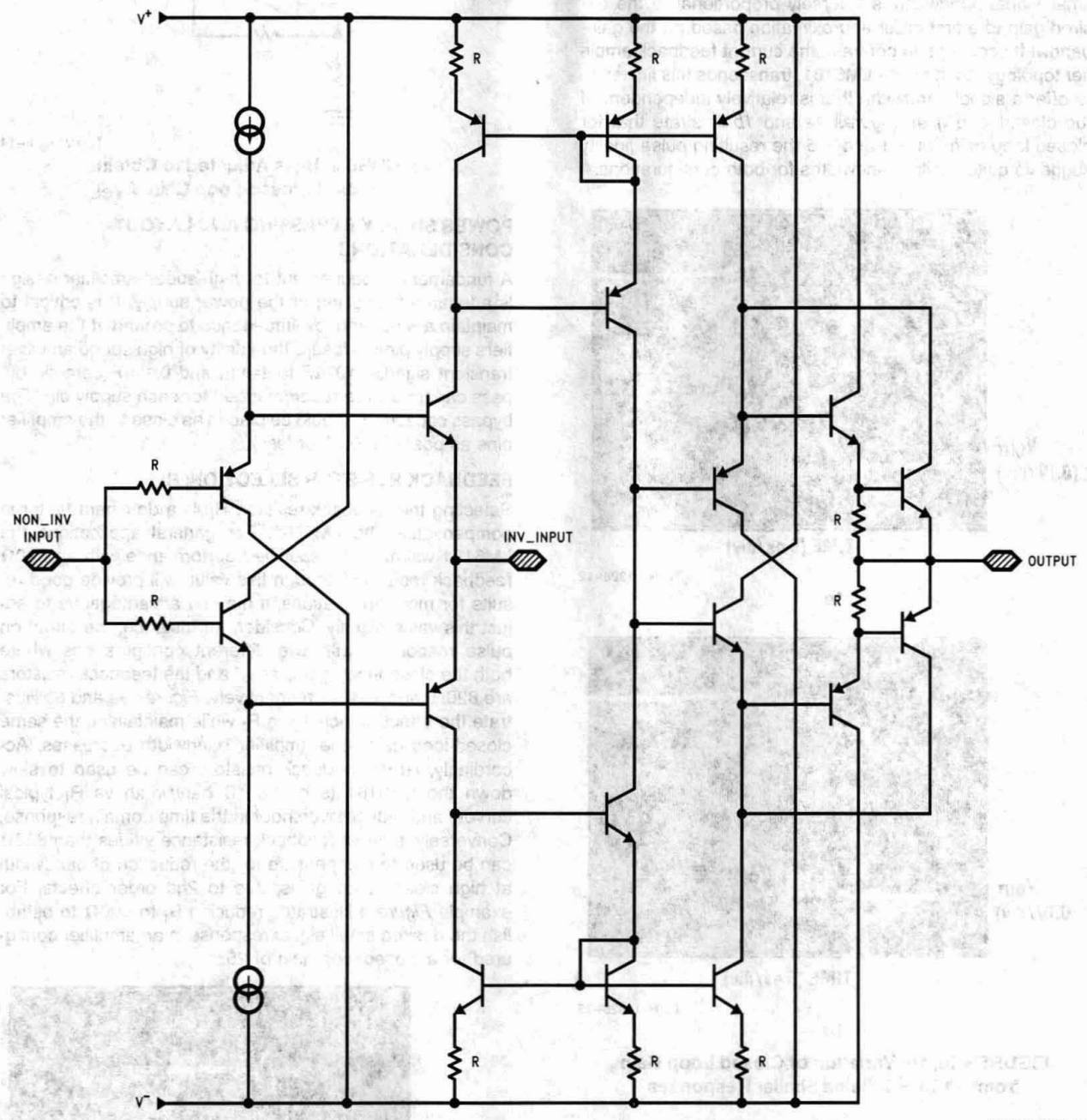


TL/H/11328-33

M-8 Package

Typical Performance Characteristics (Continued)

Simplified Schematic



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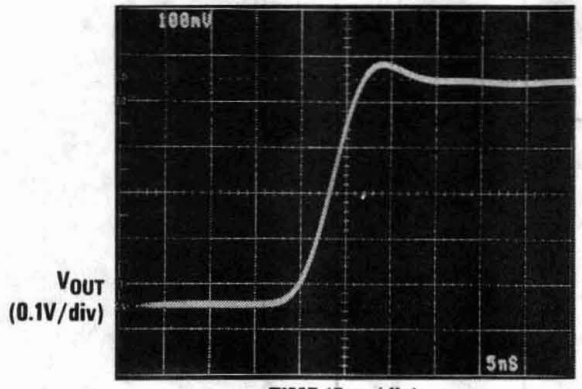
Typical Applications

CURRENT FEEDBACK TOPOLOGY

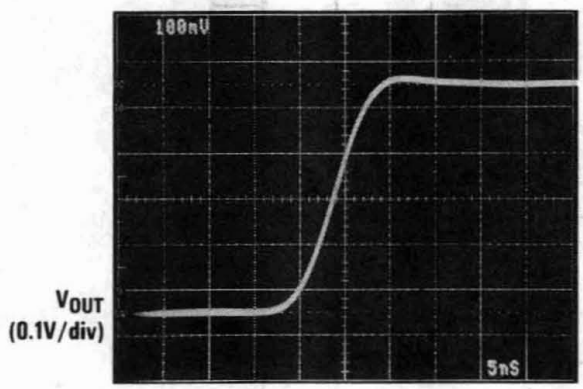
For a conventional voltage feedback amplifier the resulting small-signal bandwidth is inversely proportional to the desired gain to a first order approximation based on the gain-bandwidth concept. In contrast, the current feedback amplifier topology, such as the LM6181, transcends this limitation to offer a signal bandwidth that is relatively independent of the closed-loop gain. *Figures 1a* and *1b* illustrate that for closed loop gains of −1 and −5 the resulting pulse fidelity suggests quite similar bandwidths for both configurations.



TIME (5 ns/div)

TL/H/11328–12

1a



TIME (5 ns/div)

TL/H/11328–13

1b

FIGURES 1a, 1b: Variation of Closed Loop Gain from −1 to −5 Yields Similar Responses

The closed-loop bandwidth of the LM6181 depends on the feedback resistance, R_f. Therefore, R_S and not R_f, must be varied to adjust for the desired closed-loop gain as in *Figure 2*.

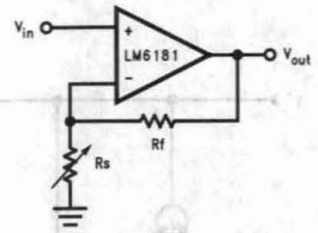


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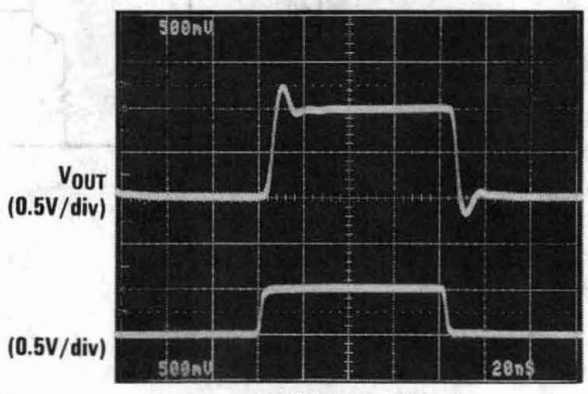
FIGURE 2. R_S Is Adjusted to Obtain the Desired Closed Loop Gain, A_{VCL}

POWER SUPPLY BYPASSING AND LAYOUT CONSIDERATIONS

A fundamental requirement for high-speed amplifier design is adequate bypassing of the power supply. It is critical to maintain a wideband low-impedance to ground at the amplifiers supply pins to insure the fidelity of high speed amplifier transient signals. 10 μF tantalum and 0.1 μF ceramic bypass capacitors are recommended for each supply pin. The bypass capacitors should be placed as close to the amplifier pins as possible (0.5″ or less).

FEEDBACK RESISTOR SELECTION: R_f

Selecting the feedback resistor, R_f, is a dominant factor in compensating the LM6181. For general applications the LM6181 will maintain specified performance with an 820Ω feedback resistor. Although this value will provide good results for most applications, it may be advantageous to adjust this value slightly. Consider, for instance, the effect on pulse responses with two different configurations where both the closed-loop gains are 2 and the feedback resistors are 820Ω, and 1640Ω, respectively. *Figures 3a* and *3b* illustrate the effect of increasing R_f while maintaining the same closed-loop gain—the amplifier bandwidth decreases. Accordingly, larger feedback resistors can be used to slow down the LM6181 (see −3 dB bandwidth vs R_f typical curves) and reduce overshoot in the time domain response. Conversely, smaller feedback resistance values than 820Ω can be used to compensate for the reduction of bandwidth at high closed loop gains, due to 2nd order effects. For example *Figure 4* illustrates reducing R_f to 500Ω to establish the desired small signal response in an amplifier configured for a closed loop gain of 25.

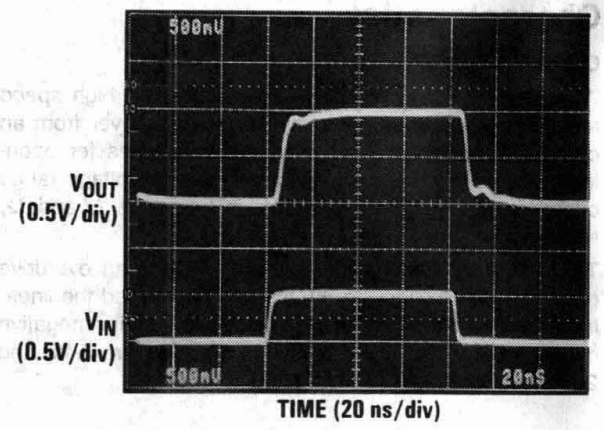


TIME (20 ns/div)

TL/H/11328–15

3a: R_f = 820Ω

Typical Applications (Continued)



TL/H/11328–16

3b: $R_f = 1640\Omega$

FIGURES 3a, b: Increasing Compensation with Increasing R_f

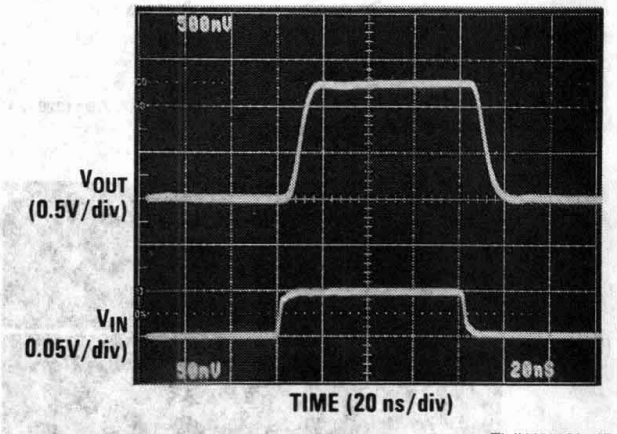


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FIGURE 4: Reducing R_f for Large Closed Loop Gains, $R_f = 500\Omega$

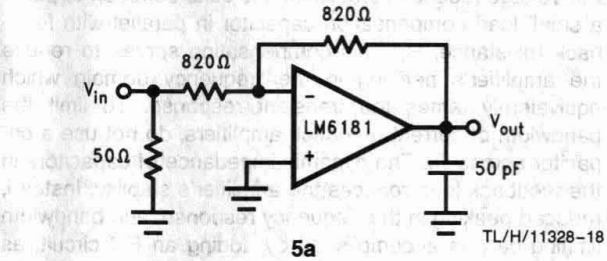
SLEW RATE CONSIDERATIONS

The slew rate characteristics of current feedback amplifiers are different than traditional voltage feedback amplifiers. In voltage feedback amplifiers slew rate limiting or non-linear amplifier behavior is dominated by the finite availability of the 1st stage tail current charging the compensation capacitor. The slew rate of current feedback amplifiers, in contrast, is not constant. Transient current at the inverting input determines slew rate for both inverting and non-inverting gains. The non-inverting configuration slew rate is also determined by input stage limitations. Accordingly, variations of slew rates occur for different circuit topologies.

DRIVING CAPACITIVE LOADS

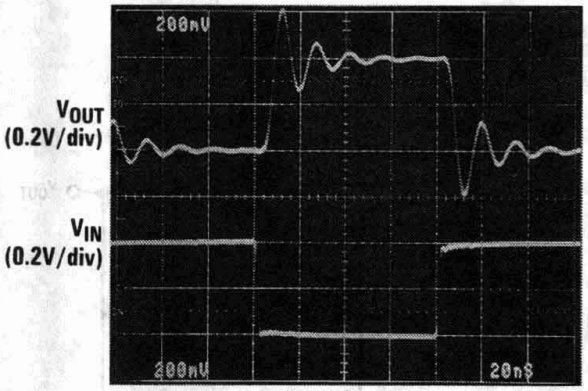
The LM6181 can drive significantly larger capacitive loads than many current feedback amplifiers. Although the LM6181 can directly drive as much as 100 pF without oscillating, the resulting response will be a function of the feedback resistor value. *Figure 5* illustrates the small-signal pulse response of the LM6181 while driving a 50 pF load. Ringing persists for approximately 70 ns. To achieve pulse responses with less ringing either the feedback resistor can be increased (see typical curves Suggested R_f and R_S for C_L), or resistive isolation can be used (10Ω–51Ω typically works well). Either technique, however, results in lowering the system bandwidth.

Figure 6 illustrates the improvement obtained with using a 47Ω isolation resistor.



5a

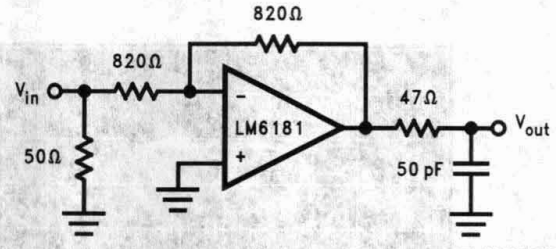
TL/H/11328–18



5b

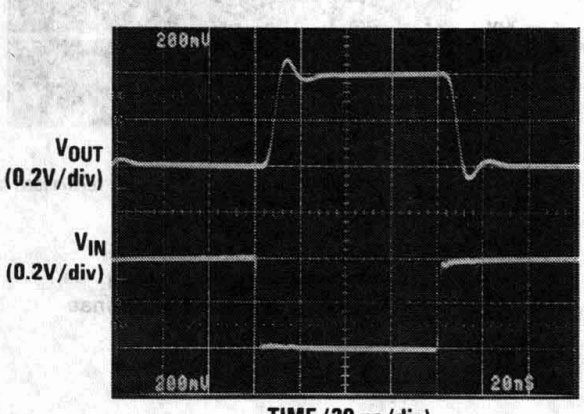
TL/H/11328–19

FIGURES 5a, b: $A_V = -1$, LM6181 Can Directly Drive 50 pF of Load Capacitance with 70 ns of Ringing Resulting in Pulse Response



6a

TL/H/11328–20



6b

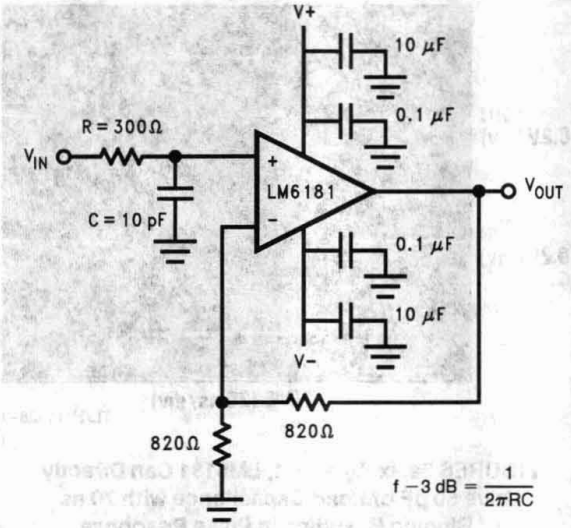
TL/H/11328–21

FIGURES 6a, b: Resistive Isolation of C_L Provides Higher Fidelity Pulse Response. R_f and R_S Could Be Increased to Maintain $A_V = -1$ and Improve Pulse Response Characteristics.

Typical Applications (Continued)

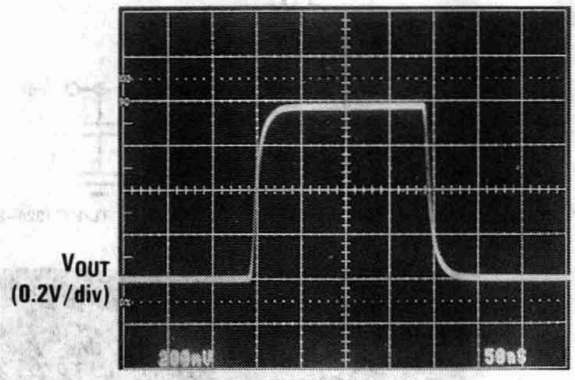
CAPACITIVE FEEDBACK

For voltage feedback amplifiers it is quite common to place a small lead compensation capacitor in parallel with feedback resistance, R_f. This compensation serves to reduce the amplifier's peaking in the frequency domain which equivalently tames the transient response. To limit the bandwidth of current feedback amplifiers, do not use a capacitor across R_f. The dynamic impedance of capacitors in the feedback loop reduces the amplifier's stability. Instead, reduced peaking in the frequency response, and bandwidth limiting can be accomplished by adding an RC circuit, as illustrated in *Figure 7b.*



TL/H/11328–22

7a



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7b

FIGURES 7a, b: RC Limits Amplifier Bandwidth to 50 MHz, Eliminating Peaking in the Resulting Pulse Response

Typical Performance Characteristics

OVERDRIVE RECOVERY

When the output or input voltage range of a high speed amplifier is exceeded, the amplifier must recover from an overdrive condition. The typical recovery times for open-loop, closed-loop, and input common-mode voltage range overdrive conditions are illustrated in *Figures 9, 11* and *12,* respectively.

The open-loop circuit of *Figure 8* generates an overdrive response by allowing the ±0.5V input to exceed the linear input range of the amplifier. Typical positive and negative overdrive recovery times shown in *Figure 9* are 5 ns and 25 ns, respectively.

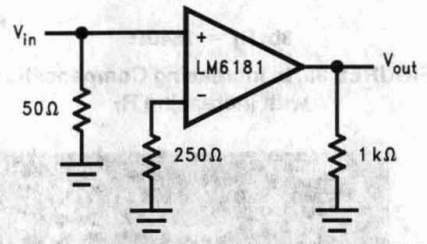

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FIGURE 8

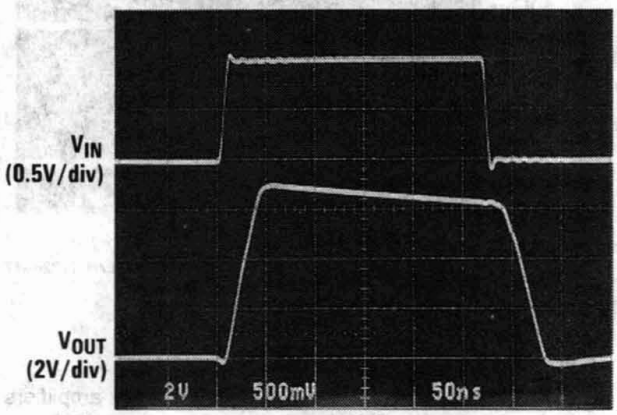

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FIGURE 9. Open-Loop Overdrive Recovery Time of 5 ns, and 25 ns from Test Circuit in *Figure 8*

Typical Performance Characteristics (Continued)

The large closed-loop gain configuration in *Figure 10* forces the amplifier output into overdrive. *Figure 11* displays the typical 30 ns recovery time to a linear output value.

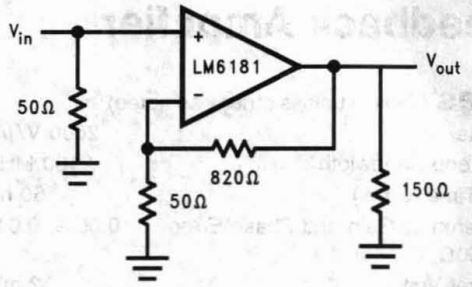

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FIGURE 10

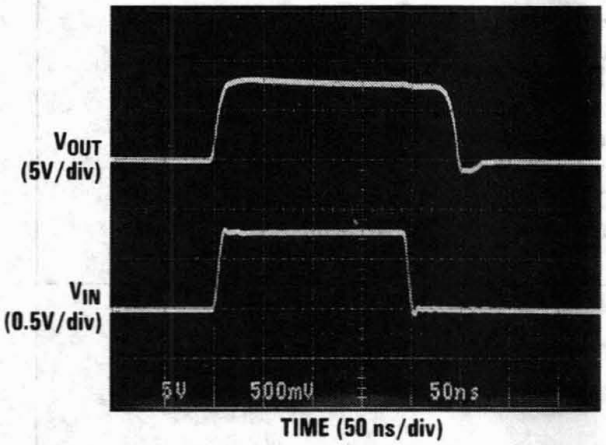

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FIGURE 11. Closed-Loop Overdrive Recovery Time of 30 ns from Exceeding Output Voltage Range from Circuit in *Figure 10*

The common-mode input of the circuit in *Figure 10* is exceeded by a 5V pulse resulting in a typical recovery time of 310 ns shown in *Figure 12*. The LM6181 supply voltage is ±5V.

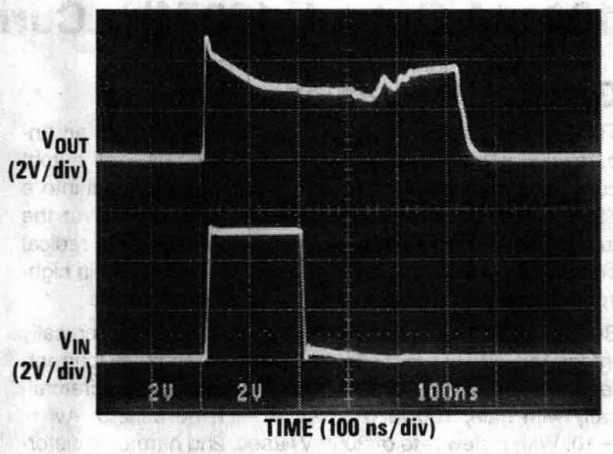

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FIGURE 12. Exceptional Output Recovery from an Input that Exceeds the Common-Mode Range

Ordering Information

Package	Temperature Range		NSC Drawing
	Military −55°C to +125°C	Industrial −40°C to +85°C	
8-Pin Molded DIP	LM6181AMN	LM6181AIN LM6181IN	N08E
8-Pin Small Outline Molded Package		LM6181AIM-8 LM6181IM-8	M08A
16-Pin Small Outline		LM6181AIM LM6181IM	M16A
8-Pin Ceramic DIP	LM6181AMJ/883		J08A

National Semiconductor

LM6182 Dual
100 mA Output, 100 MHz Current Feedback Amplifier

General Description

The LM6182 dual current feedback amplifier offers an unparalleled combination of bandwidth, slew-rate, and output current. Each amplifier can directly drive a 2V signal into a 50Ω or 75Ω back-terminated coax cable system over the full industrial temperature range. This represents a radical enhancement in output drive capability for a dual 8-pin high-speed amplifier making it ideal for video applications.

Built on National's advanced high-speed VIP II™ (Vertically Integrated PNP) process, the LM6182 employs current-feedback providing bandwidth that does not vary dramatically with gain; 100 MHz at Av = −1, 60 MHz at Av = −10. With a slew rate of 2000 V/μsec, 2nd harmonic distortion of −50 dBc at 10 MHz and settling time of 50 ns (0.1%), the two independent amplifiers of the LM6182 offer performance that is ideal for data acquisition, high-speed ATE, and precision pulse amplifier applications.

See the LM6181 data sheet for a single amplifier with these same features.

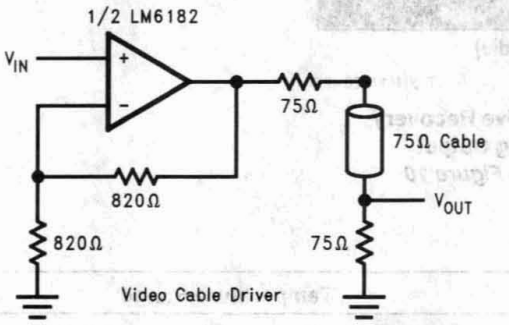
Features (Typical unless otherwise noted)

- Slew Rate 2000 V/μs
- Closed Loop Bandwidth 100 MHz
- Settling Time (0.1%) 50 ns
- Low Differential Gain and Phase Error 0.05%, 0.04°
  R_L = 150Ω
- Low Offset Voltage 2 mV
- High Output Drive ±10V into 150Ω
- Characterized for Supply Ranges ±5V and ±15V
- Improved Performance over OP260 and LT1229

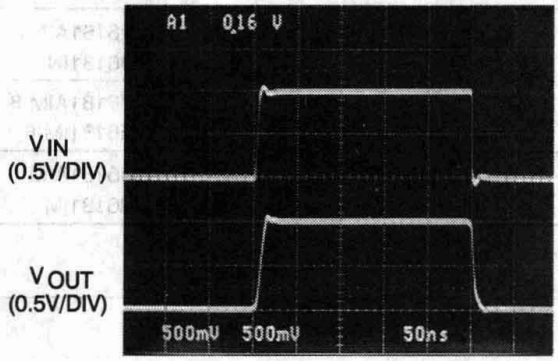
Applications

- Coax Cable Driver
- Professional Studio Video Equipment
- Flash ADC Buffer
- PC and Workstation Video Boards
- Facsimile and Imaging Systems

Typical Application



TL/H/11926–1



TIME (50ns/DIV)

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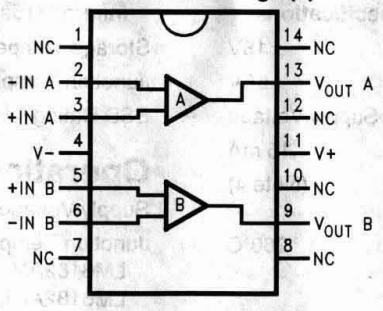
Connection Diagrams

Dual-In-Line Package (J)



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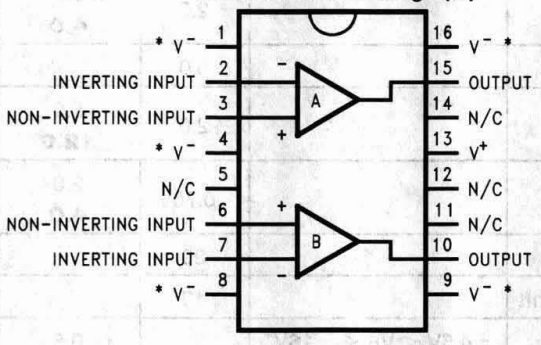
Order Number LM6182AMJ/883
See NS Package Number J14A

Small Outline Package (M)



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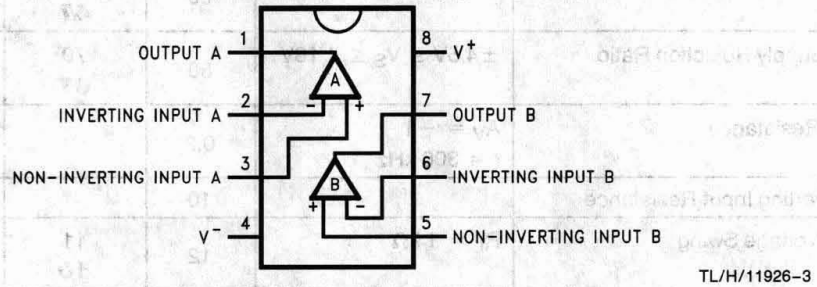
*Heat Sinking Pins (Note 3)

Order Number LM6182IM or LM6182AIM
See NS Package Number M16A

Dual-In-Line Package (N)



TL/H/11926–3

Order Number LM6182IN, LM6182AIN or LM6182AMN
See NS Package Number N08E

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	±18V
Differential Input Voltage	±6V
Input Voltage	±Supply Voltage
Inverting Input Current	15 mA
Output Short Circuit	(Note 4)
Soldering Information	
Dual-In-Line Package (N) Soldering (10s)	260°C
Small Outline Package (M)	
Vapor Phase (60s)	215°C
Infrared (15s)	220°C
Storage Temperature Range	$-65°C \le T_J \le +150°C$
Junction Temperature	150°C
ESD Rating (Note 2)	±2000V

Operating Ratings

Supply Voltage Range	7V to 32V
Junction Temperature Range (Note 3)	
LM6182AM	$-55°C \le T_J \le +125°C$
LM6182AI, LM6182I	$-40°C \le T_J \le +85°C$

±15V DC Electrical Characteristics

The following specifications apply for supply voltage = ±15V, Vcm = V_O = 0V, R_f = 820Ω, and R_L = 1 kΩ unless otherwise noted. **Boldface** limits apply at the temperature extremes; all other limits T_J = 25°C.

Symbol	Parameter	Conditions	Typical (Note 5)	LM6182AM Limit (Note 6)	LM6182AI Limit (Note 6)	LM6182I Limit (Note 6)	Units
V_{OS}	Input Offset Voltage		2.0	3.0 **4.0**	3.0 **3.5**	5.0 **5.5**	mV max
TCV_{OS}	Input Offset Voltage Drift		5.0				µV/°C
I_B	Inverting Input Bias Current		2.0	5.0 **12.0**	5.0 **12.0**	10.0 **17.0**	µA max
	Non-Inverting Input Bias Current		0.75	2.0 **4.0**	2.0 **4.0**	3.0 **5.0**	
TCI_B	Inverting Input Bias Current Drift		30				nA/°C
	Non-Inverting Input Bias Current Drift		10				
I_B PSR	Inverting Input Bias Current Power Supply Rejection	$\pm 4.5V \le V_S \le \pm 16V$	0.1	0.5 **3.0**	0.5 **3.0**	0.75 **4.5**	µA/V max
	Non-Inverting Input Bias Current Power Supply Rejection	$\pm 4.5V \le V_S \le \pm 16V$	0.05	0.5 **1.5**	0.5 **1.5**	0.5 **3.0**	
I_B CMR	Inverting Input Bias Current Common Mode Rejection	$-10V \le V_{CM} \le +10V$	0.15	0.5 **1.0**	0.5 **1.0**	0.75 **1.5**	
	Non-Inverting Input Bias Current Common Mode Rejection	$-10V \le V_{CM} \le +10V$	0.1	0.5 **1.0**	0.5 **1.0**	0.5 **1.5**	
CMRR	Common Mode Rejection Ratio	$-10V \le V_{CM} \le +10V$	60	50 **47**	50 **47**	50 **47**	dB min
PSRR	Power Supply Rejection Ratio	$\pm 4.5V \le V_S \le \pm 16V$	80	70 **67**	70 **67**	70 **65**	dB min
R_O	Output Resistance	$A_V = -1$ f = 300 kHz	0.2				Ω
R_{IN}	Non-Inverting Input Resistance		10				MΩ
V_O	Output Voltage Swing	R_L = 1 kΩ	12	11 **10**	11 **10**	11 **10**	V min
		R_L = 150Ω	11	9.5 **5.6**	9.5 **6.0**	9.5 **6.0**	

±15V DC Electrical Characteristics (Continued) The following specifications apply for supply voltage = ±15V, Vcm = V_O = 0V, R_f = 820Ω, and R_L = 1 kΩ unless otherwise noted. **Boldface** limits apply at the temperature extremes; all other limits T_J = 25°C.

Symbol	Parameter	Conditions	Typical (Note 5)	LM6182AM Limit (Note 6)	LM6182AI Limit (Note 6)	LM6182I Limit (Note 6)	Units
I_{SC}	Output Short Circuit Current		100	70 **37.5**	70 **40**	70 **40**	mA min
Z_T	Transimpedance	R_L = 1 kΩ	1.8	1.0 **0.4**	1.0 **0.5**	0.8 **0.4**	MΩ min
		R_L = 150Ω	1.4	0.8 **0.3**	0.8 **0.35**	0.7 **0.3**	
I_S	Supply Current	No Load, V_{IN} = 0V Both Amplifiers	15	20 **22**	20 **22**	20 **22**	mA max
V_{CM}	Input Common Mode Voltage Range		$V^+ - 1.7V$ $V^- + 1.7V$				V

±15V AC Electrical Characteristics The following specifications apply for supply voltage = ±15V, Vcm = V_O = 0V, R_f = 820Ω, and R_L = 1 kΩ unless otherwise noted. **Boldface** limits apply at the temperature extremes; all other limits T_J = 25°C.

Symbol	Parameter	Conditions	Typical (Note 5)	LM6182AM Limit (Note 6)	LM6182AI Limit (Note 6)	LM6182I Limit (Note 6)	Units
Xt	Crosstalk Rejection	(Note 7)	93				dB
BW	Closed Loop Bandwidth −3 dB	A_V = +2	100				MHz
		A_V = +10	75				
		A_V = −1	100				
		A_V = −10	60				
	Closed Loop Bandwidth 0.1 dB Flat, R_{SOURCE} = 200Ω	A_V = +2, R_L = 150Ω	35				
PBW	Power Bandwidth	A_V = −1, V_O = 5 V_{PP}	60				
SR	Slew Rate	Overdriven	2000				V/μs min
		A_V = −1, V_O = ±10V R_L = 150Ω, (Note 8)	1400	1000	1000	1000	
t_s	Settling Time (0.1%)	A_V = −1, V_O = ±5V R_L = 150Ω	50				ns
t_r, t_f	Rise and Fall Time	V_O = 1 V_{PP}	5				
t_p	Propagation Delay Time	V_O = 1 V_{PP}	6				
in(+)	Non-Inverting Input Noise Current Density	f = 1 kHz	3				pA/√Hz
in(−)	Inverting Input Noise Current Density	f = 1 kHz	16				pA/√Hz
e_n	Input Noise Voltage Density	f = 1 kHz	4				nV/√Hz
	Second Harmonic Distortion	V_O = 2 V_{PP}, f = 10 MHz A_V = +2	-50				dBc
	Third Harmonic Distortion	V_O = 2 V_{PP}, f = 10 MHz A_V = +2	-55				
	Differential Gain	R_L = 150Ω A_V = +2, NTSC	0.05				%
	Differential Phase	R_L = 150Ω A_V = +2, NTSC	0.04				Deg
THD	Total Harmonic Distortion	V_O = 2 V_{PP}, A_V = +2, f = 10 MHz, R_L = 150Ω	0.58				%

±5V DC Electrical Characteristics

The following specifications apply for supply voltage = ±5V, Vcm = V_O = 0V, R_f = 820Ω, and R_L = 1 kΩ unless otherwise noted. **Boldface** limits apply at the temperature extremes; all other limits T_J = 25°C.

Symbol	Parameter	Conditions	Typical (Note 5)	LM6182AM Limit (Note 6)	LM6182AI Limit (Note 6)	LM6182I Limit (Note 6)	Units
V_{OS}	Input Offset Voltage		1.0	2.0 **3.0**	2.0 **2.5**	3.0 **3.5**	mV max
TCV_{OS}	Input Offset Voltage Drift		2.5				µV/°C
I_B	Inverting Input Bias Current		5.0	10 **22**	10 **22**	17.5 **27.0**	µA max
	Non-Inverting Input Bias Current		0.25	1.5 **3.0**	1.5 **3.0**	3.0 **5.0**	
TCI_B	Inverting Input Bias Current Drift		50				nA/°C
	Non-Inverting Input Bias Current Drift		3.0				
I_B PSR	Inverting Input Bias Current Power Supply Rejection	±4V ≤ V_S ≤ ±6V	0.3	0.5 **1.0**	0.5 **1.0**	0.75 **1.5**	µA/V max
	Non-Inverting Input Bias Current Power Supply Rejection	±4V ≤ V_S ≤ ±6V	0.05	0.5 **1.0**	0.5 **1.0**	0.5 **1.5**	
I_B CMR	Inverting Input Bias Current Common Mode Rejection	−2.5V ≤ V_{CM} ≤ +2.5V	0.3	0.5 **1.0**	0.5 **1.0**	1.0 **1.5**	
	Non-Inverting Input Bias Current Common Mode Rejection	−2.5V ≤ V_{CM} ≤ +2.5V	0.12	0.5 **1.0**	0.5 **1.0**	0.5 **1.5**	
CMRR	Common Mode Rejection Ratio	−2.5V ≤ V_{CM} ≤ +2.5V	57	50 **47**	50 **47**	50 **47**	dB min
PSRR	Power Supply Rejection Ratio	±4V ≤ V_S ≤ ±6V	80	70 **67**	70 **67**	64 **60**	
R_O	Output Resistance	A_V = −1 f = 300 kHz	0.25				Ω
R_{IN}	Non-Inverting Input Resistance		8				MΩ
V_O	Output Voltage Swing	R_L = 1 kΩ	2.6	2.25 **2.0**	2.25 **2.0**	2.25 **2.0**	V min
		R_L = 150Ω	2.2	2.0 **1.8**	2.0 **1.8**	2.0 **1.8**	
I_{SC}	Output Short Circuit Current		100	65 **35**	65 **40**	65 **40**	mA min
Z_T	Transimpedance	R_L = 1 kΩ	1.4	0.75 **0.3**	0.75 **0.35**	0.6 **0.3**	MΩ min
		R_L = 150Ω	1.0	0.5 **0.2**	0.5 **0.25**	0.4 **0.2**	
I_S	Supply Current	No Load, V_{IN} = 0V Both Amplifiers	13	17 **18.5**	17 **18.5**	17 **18.5**	mA max
V_{CM}	Input Common Mode Voltage Range		V^+ − 1.7V V^- + 1.7V				V

±5V AC Electrical Characteristics

The following specifications apply for supply voltage = ±5V, Vcm = V_O = 0V, R_f = 820Ω, and R_L = 1 kΩ unless otherwise noted. **Boldface** limits apply at the temperature extremes; all other limits T_J = 25°C.

Symbol	Parameter	Conditions	Typical (Note 5)	LM6182AM Limit (Note 6)	LM6182AI Limit (Note 6)	LM6182I Limit (Note 6)	Units
Xt	Crosstalk Rejection	(Note 7)	92				dB
BW	Closed Loop Bandwidth −3 dB	A_V = +2	50				MHz
		A_V = +10	40				
		A_V = −1	55				
		A_V = −10	35				
	Closed Loop Bandwidth 0.1 dB Flat, R_{SOURCE} = 200Ω	A_V = +2, R_L = 150Ω	15				
PBW	Power Bandwidth	A_V = −1, V_O = 4 V_{PP}	40				
SR	Slew Rate	A_V = −1, V_O = ±2V R_L = 150Ω, (Note 8)	500	375	375	375	V/μs min
t_s	Settling Time (0.1%)	A_V = −1, V_O = ±2V R_L = 150Ω	50				ns
t_r, t_f	Rise and Fall Time	V_O = 1 V_{PP}	8.5				
t_p	Propagation Delay Time	V_O = 1 V_{PP}	8				
in(+)	Non-Inverting Input Noise Current Density	f = 1 kHz	3				pA/√Hz
in(−)	Inverting Input Noise Current Density	f = 1 kHz	16				pA/√Hz
e_n	Input Noise Voltage Density	f = 1 kHz	4				nV/√Hz
	Second Harmonic Distortion	V_O = 2 V_{PP}, f = 10 MHz A_V = +2	-45				dBc
	Third Harmonic Distortion	V_O = 2 V_{PP}, f = 10 MHz A_V = +2	-55				
	Differential Gain	R_L = 150Ω A_V = +2, NTSC	0.06				%
	Differential Phase	R_L = 150Ω A_V = +2, NTSC	0.16				Deg
THD	Total Harmonic Distortion	V_O = 2 V_{PP}, A_V = +2, f = 5 MHz, R_L = 150Ω	0.36				%

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating ratings indicate conditions for which the device is intended to be functional, but device parameter specifications may not be guaranteed under these conditions. For guaranteed specifications and test conditions, see the Electrical Characteristics.

Note 2: Human body model 100 pF and 1.5 kΩ.

Note 3: The typical junction-to-ambient thermal resistance of the molded plastic DIP(N) soldered directly into a PC board is 95°C/W. The junction-to-ambient thermal resistance of the S.O. surface mount (M) package mounted flush to the PC board is 70°C/W when pins 1,4,8,9 and 16 are soldered to a total of 2 in^2 1 oz copper trace. The S.O. (M) package must have pin 4 and at least one of pins 1,8,9, or 16 connected to V− for proper operation.

Note 4: Continuous short circuit operation at elevated ambient temperature can result in exceeding the maximum allowable junction temperature of 150°C. Each amplifier of the LM6182 is short circuit current limited to 100 mA typical.

Note 5: Typical values represent the most likely parametric norm.

Note 6: All limits are guaranteed at room temperature (standard type face) or at operating temperature extremes (**boldface type**).

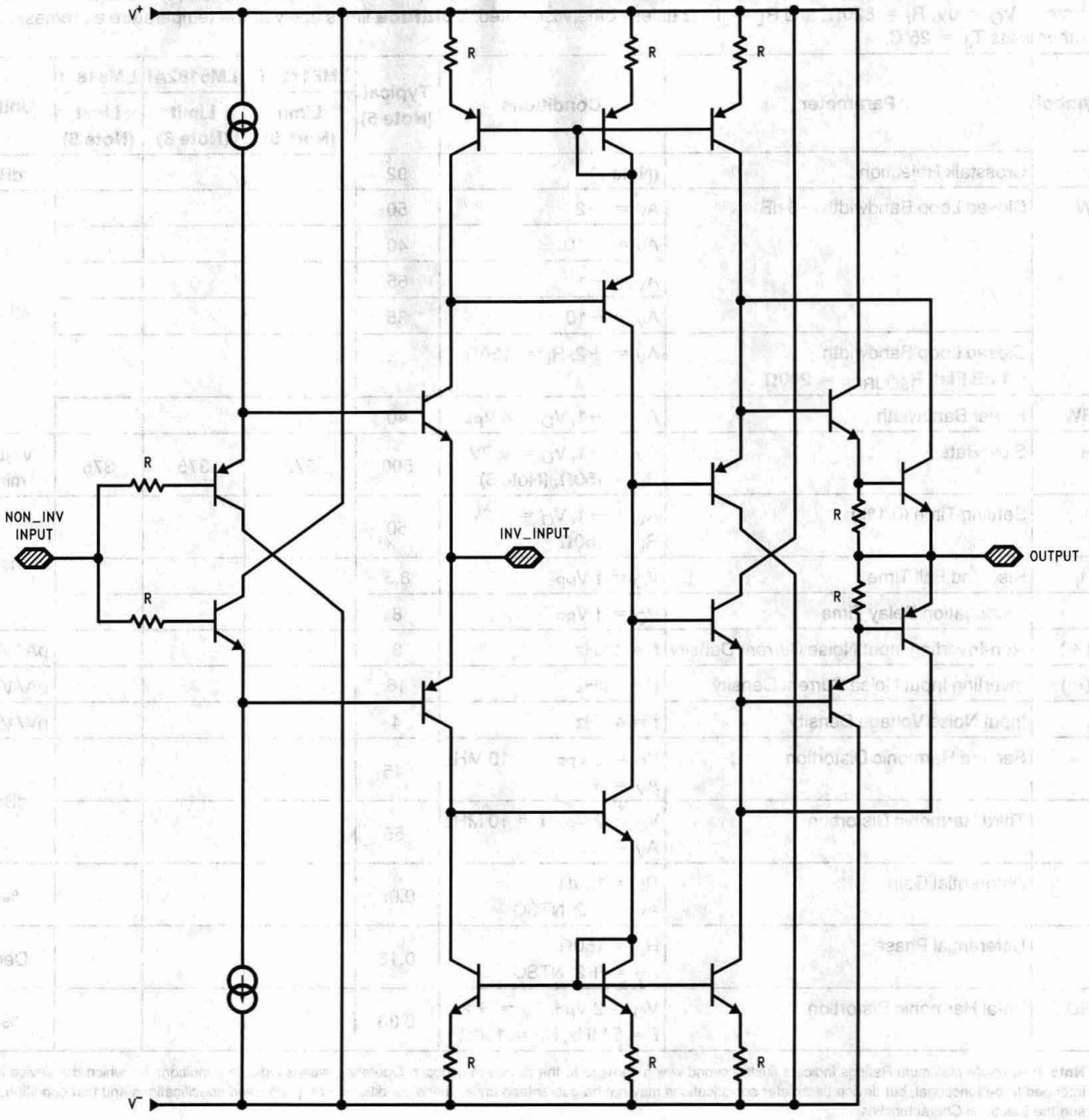
Note 7: Each amp excited in turn with 100 kHz to produce Vo = 2 Vpp. Results are input referred.

Note 8: Measured from +25% to +75% of output waveform.

Note 9: Also available per the Standard Military Drawing, 5962-9460301MCA.

Note 10: For guaranteed military specifications see military datasheet MNLM6182AM-X.

Simplified Schematic 1/2 LM6182

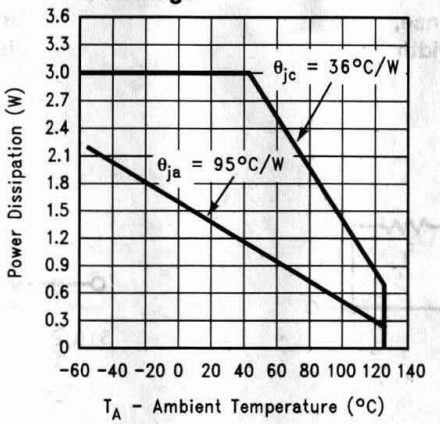


TL/H/11926–6

Typical Performance Characteristics

MAXIMUM POWER DERATING CURVES

N-Package



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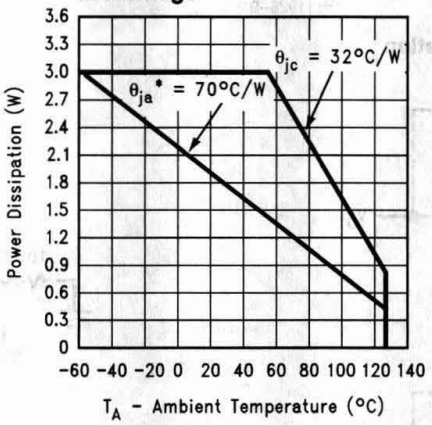
M-Package



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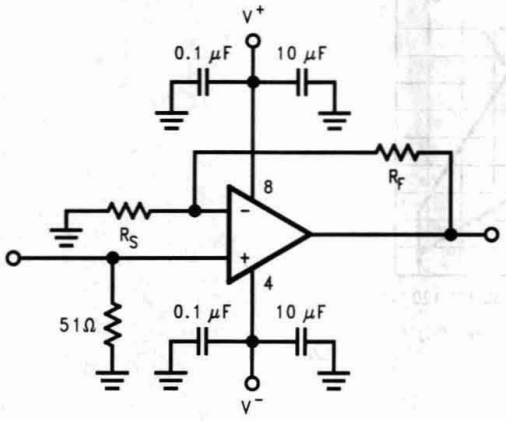
*θ_{ja} = Thermal Resistance with 2 square inches of 1 ounce copper tied to pins 1, 8, 9 and 16

2

Typical Performance Characteristics (Continued)

TYPICAL PERFORMANCE TEST CIRCUITS

Non-Inverting:
Small Signal Pulse Response,
Slew Rate, −3 dB Bandwidth



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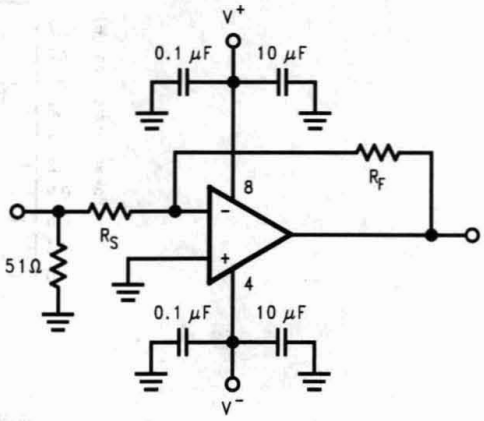
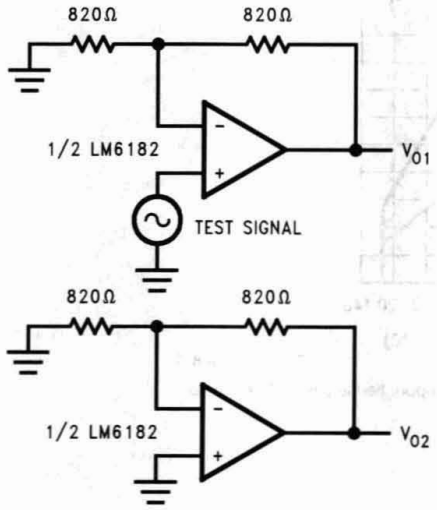
Inverting:
Small Signal Pulse Response,
Slew Rate, −3 dB Bandwidth



TL/H/11926–10

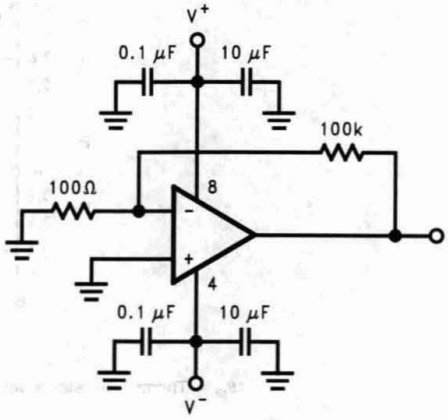
Amplifier-to-Amplifier Isolation



TL/H/11926–11

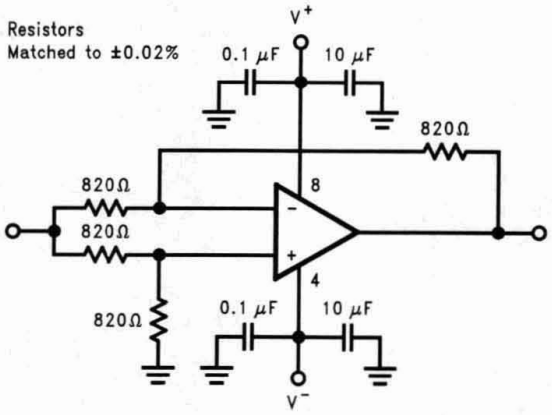
X_T (Crosstalk Rejection) $= \frac{V_{01}}{V_{02}}$

Input Voltage Noise



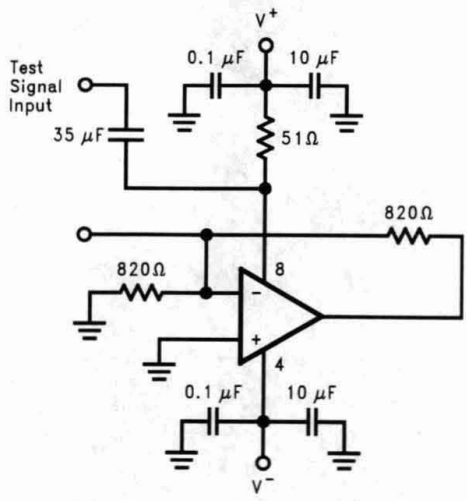
TL/H/11926–12

CMRR



TL/H/11926–13

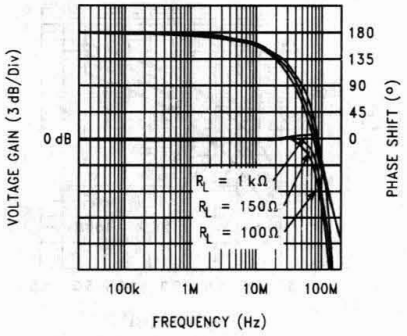
PSRR (V_{S+})



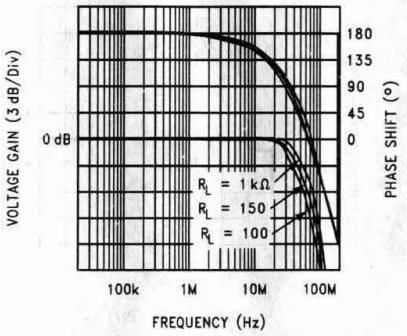
TL/H/11926–14

Typical Performance Characteristics (Continued) $V_S = \pm 15V$ and $T_A = 25°C$ unless otherwise noted.

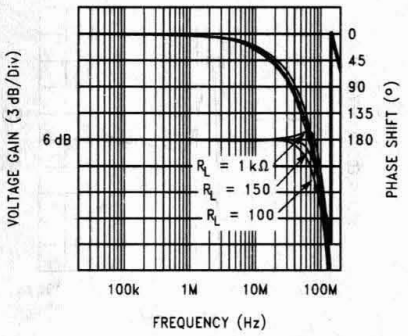
Inverting Gain Frequency Response
$V_S = \pm 15V$, $A_V = -1$, $R_f = 820\Omega$



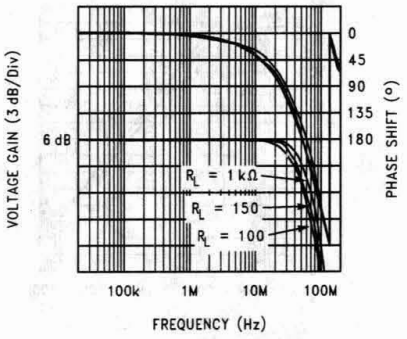
Inverting Gain Frequency Response
$V_S = \pm 5V$, $A_V = -1$, $R_f = 820\Omega$



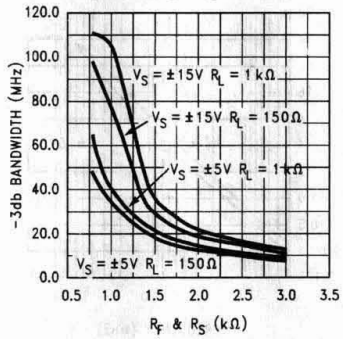
Non-Inverting Gain Frequency Response
$V_S = \pm 15V$, $A_V = +2$, $R_f = 820\Omega$



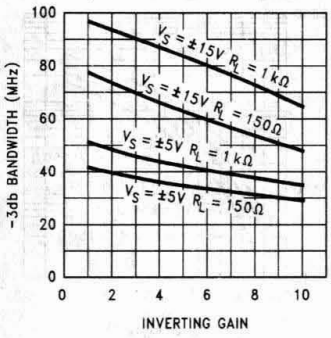
Non-Inverting Gain Frequency Response
$V_S = \pm 5V$, $A_V = +2$, $R_f = 820\Omega$



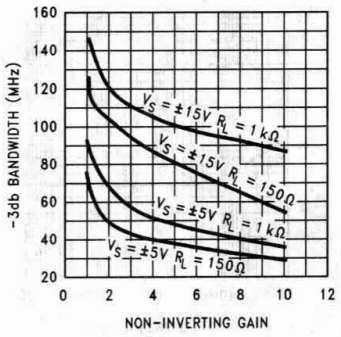
−3 dB Bandwidth vs R_f and R_s, $A_V = +2$



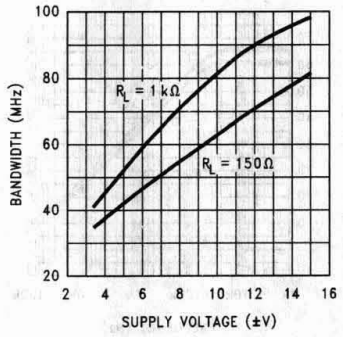
Inverting Gain vs −3 dB Bandwidth
$R_f = 820\Omega$



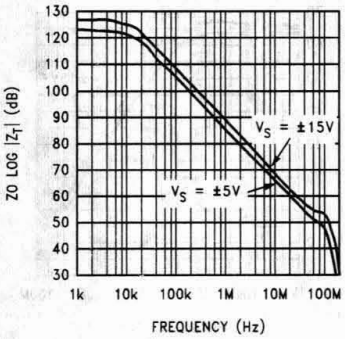
Non-Inverting Gain vs −3 dB Bandwidth
$R_f = 820\Omega$



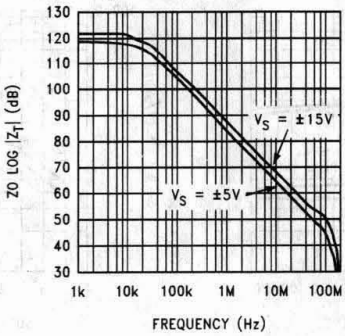
−3 dB Bandwidth vs Supply Voltage
$A_V = -1$



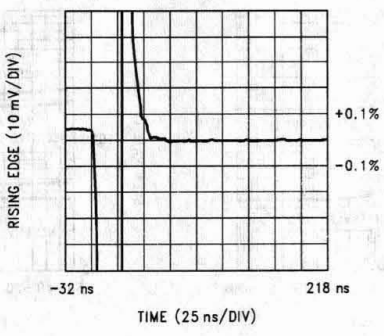
Transimpedance vs Frequency
$R_L = 1\,k\Omega$



Transimpedance vs Frequency
$R_L = 150\Omega$



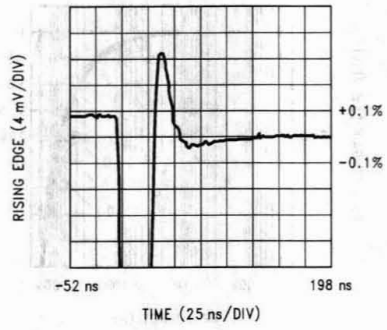
Settling Response
$V_S = \pm 15V$, $R_L = 150\Omega$
$A_V = -1$, $V_O = \pm 5V$



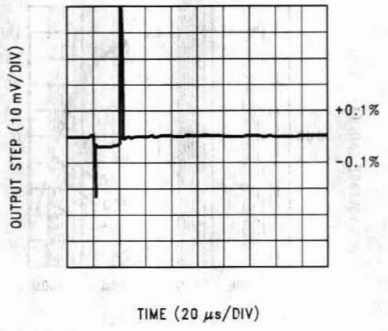
TL/H/11926–15

Typical Performance Characteristics (Continued) $V_S = \pm 15V$ and $T_A = 25°C$ unless otherwise noted.

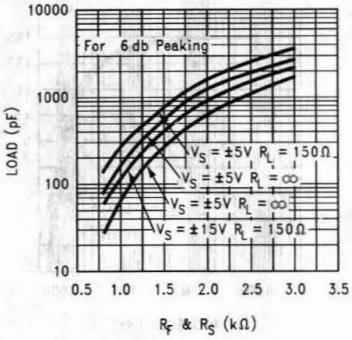
Settling Response
$V_S = \pm 5V$, $R_L = 150\Omega$
$A_V = -1$, $V_O = \pm 2V$



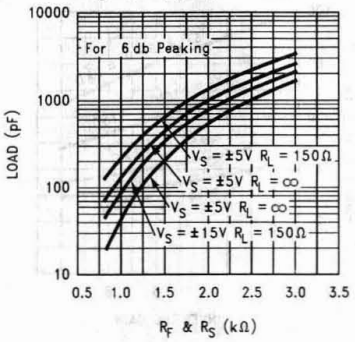
Long Term Settling Time Response $V_S = \pm 15V$, $R_L = 150\Omega$, $A_V = -1$, $V_O = \pm 5V$



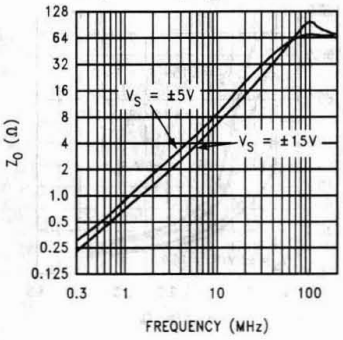
Suggested R_f and R_s for C_L, $A_V = -1$



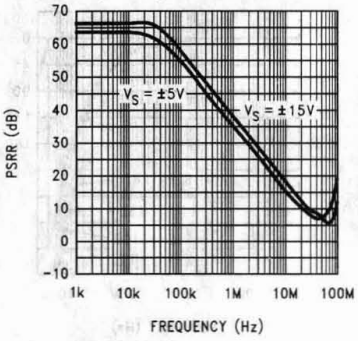
Suggested R_f and R_s for C_L, $A_V = +2$



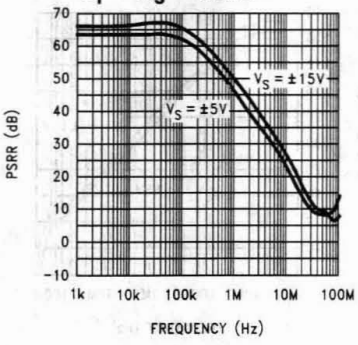
Output Impedance vs Frequency
$A_V = -1$, $R_L = 820\Omega$



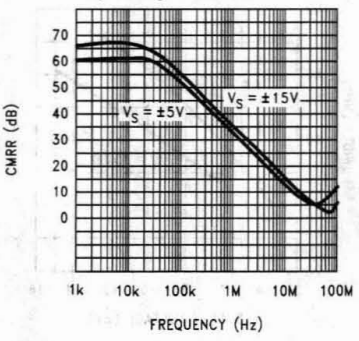
PSRR (V_{S+}) vs Frequency, $A_V = 2$, $R_f = R_s = 820\Omega$



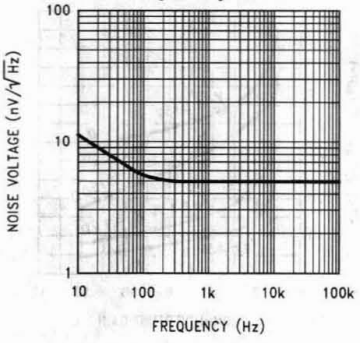
PSRR (V_{S-}) vs Frequency, $A_V = 2$, $R_f = R_s = 820\Omega$



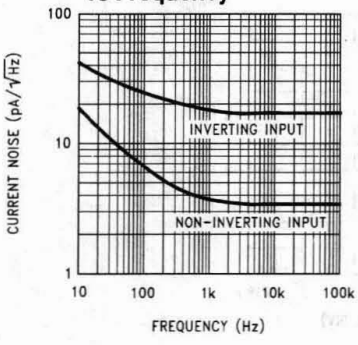
CMRR vs Frequency
$R_f = R_s = 820\Omega$



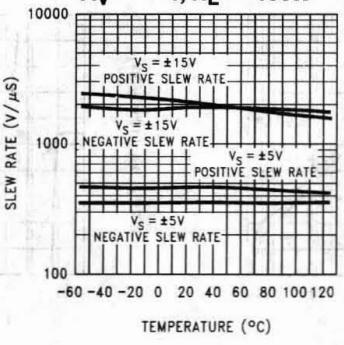
Input Voltage Noise vs Frequency



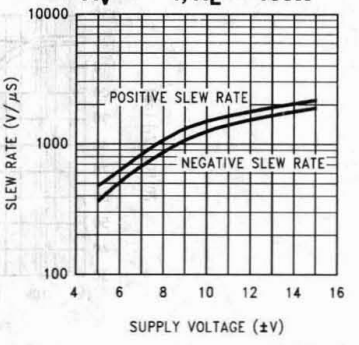
Input Current Noise vs Frequency



Slew Rate vs Temperature
$A_V = -1$, $R_L = 150\Omega$


SLEW RATE (V/μS)
$V_S = \pm 15V$ POSITIVE SLEW RATE
$V_S = \pm 15V$ NEGATIVE SLEW RATE
$V_S = \pm 5V$ POSITIVE SLEW RATE
$V_S = \pm 5V$ NEGATIVE SLEW RATE
TEMPERATURE (°C)

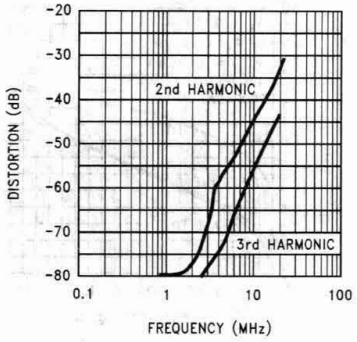
Slew Rate vs Supply Voltage
$A_V = -1$, $R_L = 150\Omega$



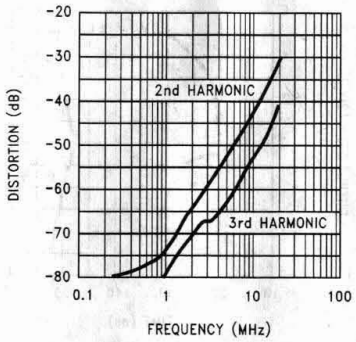
TL/H/11926–16

Typical Performance Characteristics (Continued) $V_S = \pm 15V$ and $T_A = 25°C$ unless otherwise noted.

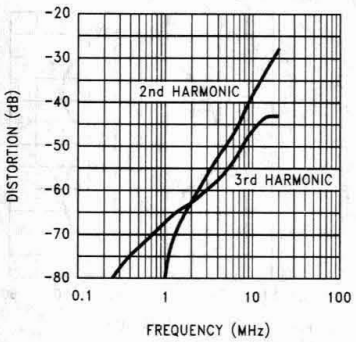
Distortion vs Frequency
$V_S = \pm 15V$, $A_V = +2$,
$R_L = 150\Omega$, $V_O = 2Vp\text{-}p$



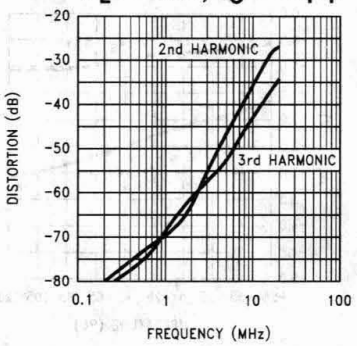
Distortion vs Frequency
$V_S = \pm 15V$, $A_V = -1$,
$R_L = 150\Omega$, $V_O = 2Vp\text{-}p$



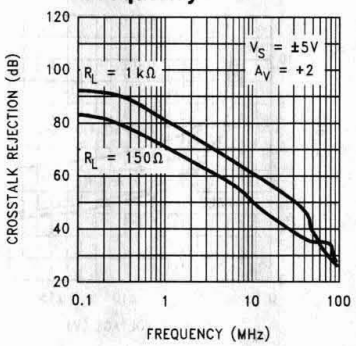
Distortion vs Frequency
$V_S = \pm 5V$, $A_V = +2$,
$R_L = 150\Omega$, $V_O = 2Vp\text{-}p$



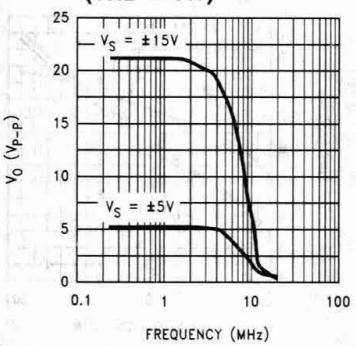
Distortion vs Frequency
$V_S = \pm 5V$, $A_V = -1$,
$R_L = 150\Omega$, $V_O = 2Vp\text{-}p$



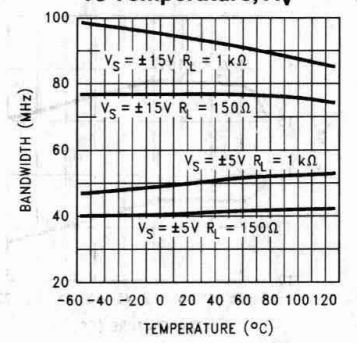
Crosstalk Rejection vs Frequency



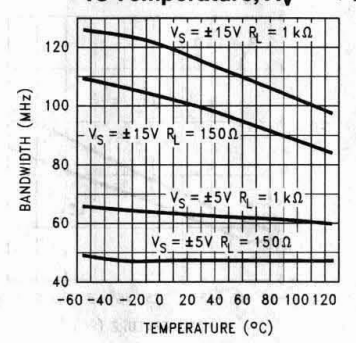
Maximum Output Voltage Swing vs Frequency (THD ≤ 1%)



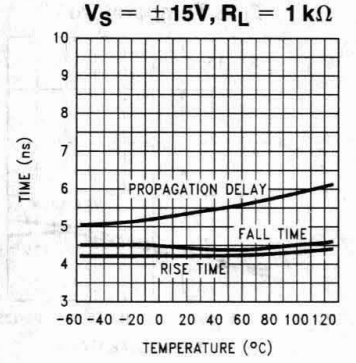
−3 dB Bandwidth vs Temperature, $A_V = -1$



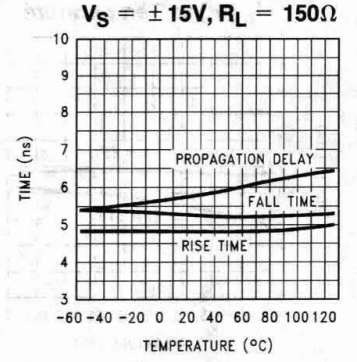
−3 dB Bandwidth vs Temperature, $A_V = +2$



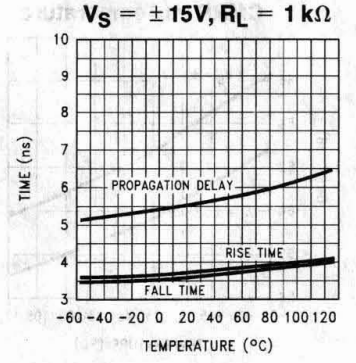
Small Signal Pulse Response vs Temperature, $A_V = -1$, $V_S = \pm 15V$, $R_L = 1\,k\Omega$



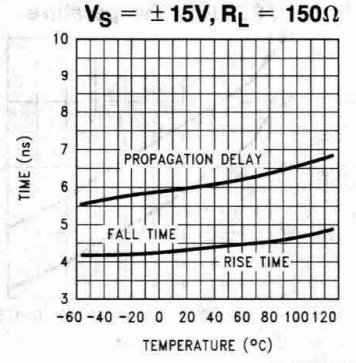
Small Signal Pulse Response vs Temperature, $A_V = -1$, $V_S = \pm 15V$, $R_L = 150\Omega$



Small Signal Pulse Response vs Temperature, $A_V = +2$, $V_S = \pm 15V$, $R_L = 1\,k\Omega$



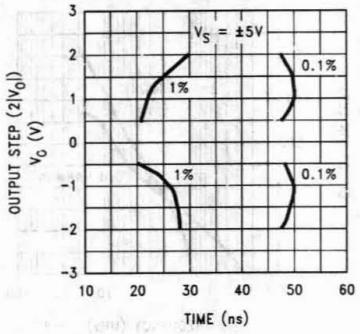
Small Signal Pulse Response vs Temperature, $A_V = +2$, $V_S = \pm 15V$, $R_L = 150\Omega$



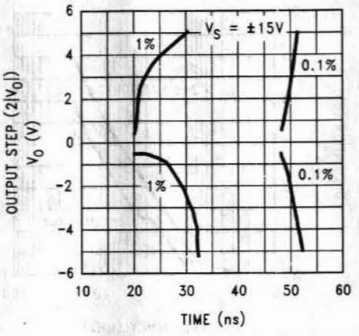
TL/H/11926–17

Typical Performance Characteristics (Continued) $V_S = \pm 15V$ and $T_A = 25°C$ unless otherwise noted.

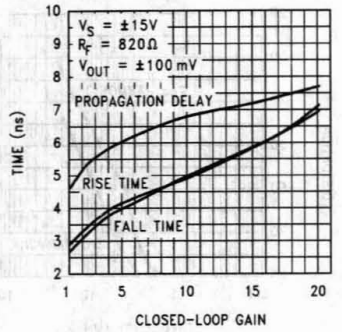
Settling Time vs Output Step, $R_F = 820\Omega$ $R_L = 150\Omega$, $A_V = -1$



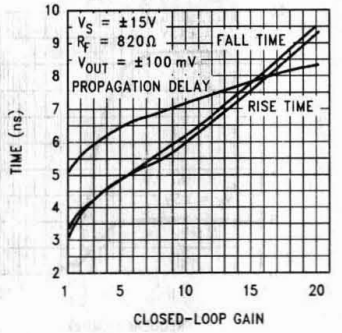
Settling Time vs Output Step, $R_F = 820\Omega$ $R_L = 150\Omega$, $A_V = -1$



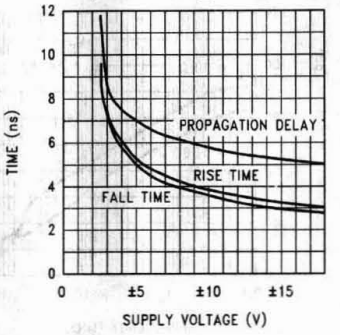
Small Signal Pulse Response vs Closed-Loop Gain $R_L = 1k$



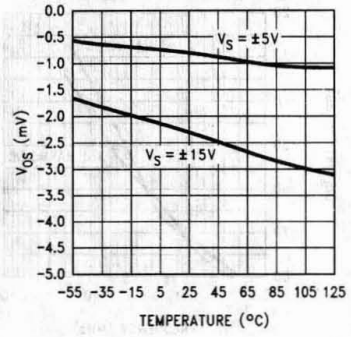
Small Signal Pulse Response vs Closed-Loop Gain $R_L = 150\Omega$



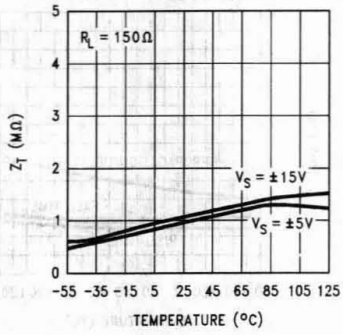
Small Signal Pulse Response vs Supply Voltage $A_V = +2$, $R_L = 1k$



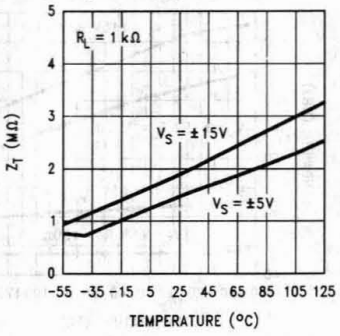
V_{OS} vs Temperature



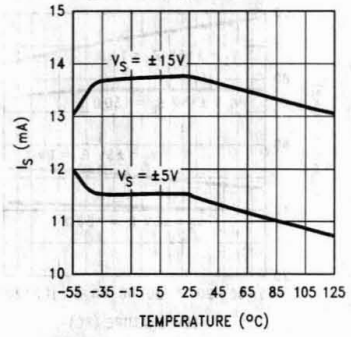
Z_t vs Temperature



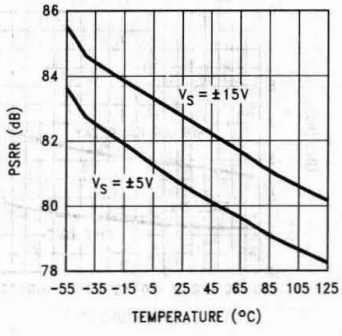
Z_t vs Temperature



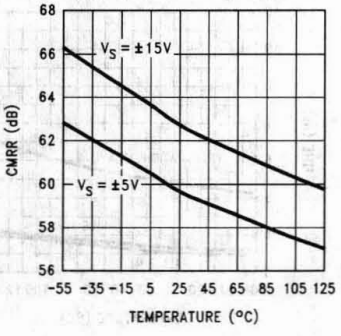
I_S vs Temperature



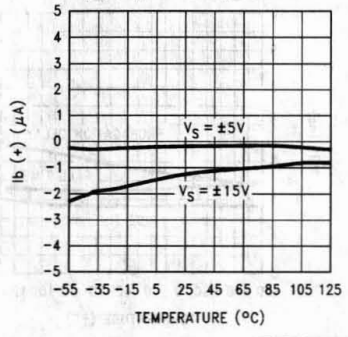
PSRR vs Temperature



CMRR vs Temperature



I_b (+) vs Temperature

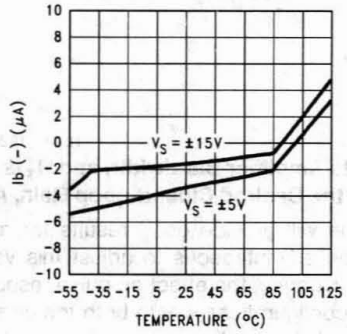


TL/H/11926–18

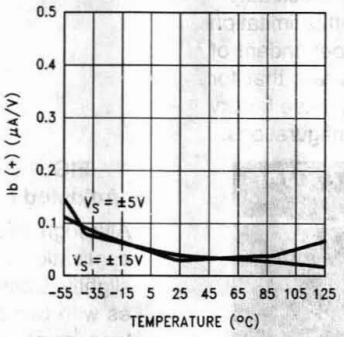
Typical Performance Characteristics

V_S = ±15V and T_A = 25°C unless otherwise noted. (Continued)

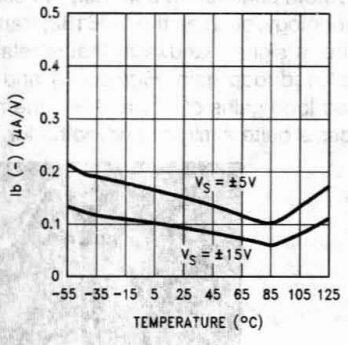
I_b (−) vs Temperature



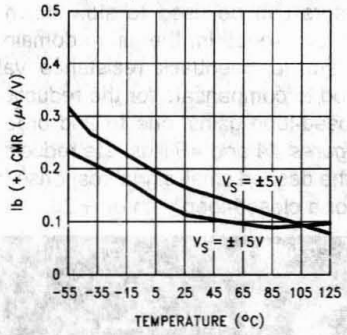
I_b (+) PSR vs Temperature



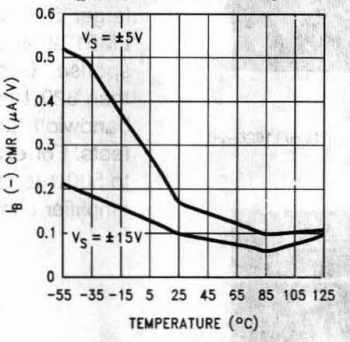
I_b (−) PSR vs Temperature



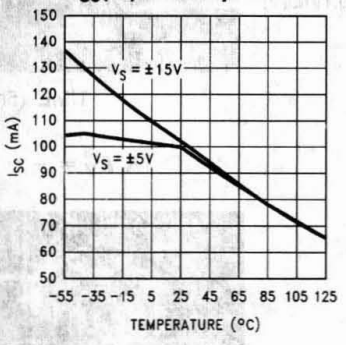
I_b (+) CMR vs Temperature



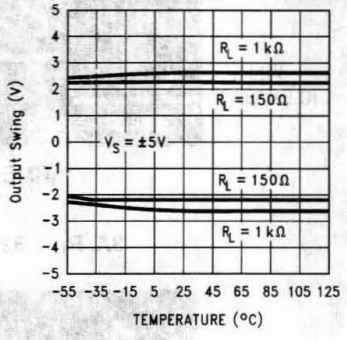
I_b (−) CMR vs Temperature



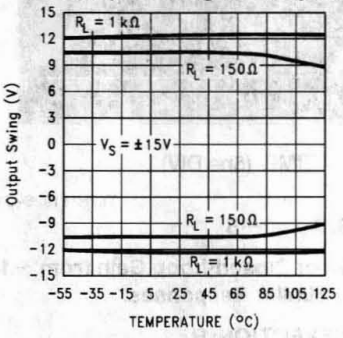
I_{sc}(±) vs Temperature



Output Swing vs Temperature



Output Swing vs Temperature



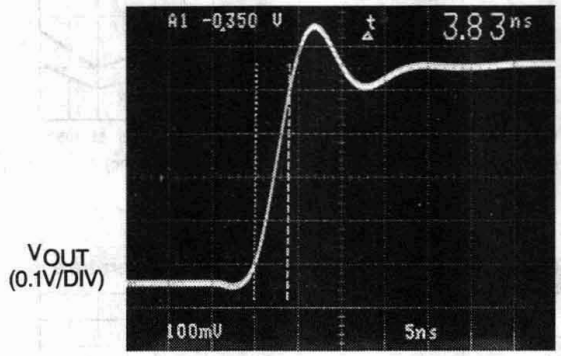
TL/H/11926–19

2

Typical Applications

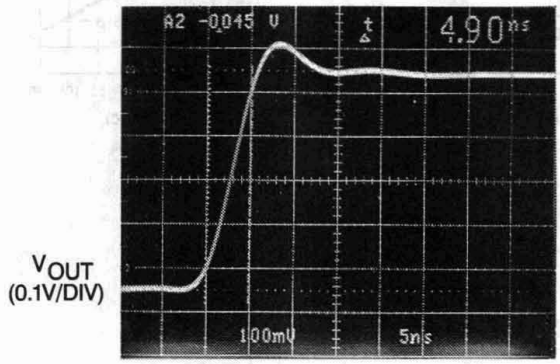
CURRENT FEEDBACK TOPOLOGY

For a conventional voltage feedback amplifier the resulting small-signal bandwidth is inversely proportional to the desired gain to a first order approximation based on the gain-bandwidth concept. In contrast, the current feedback amplifier topology, such as the LM6182, transcends this limitation to offer a signal bandwidth that is relatively independent of the closed loop gain. *Figures 1A* and *1B* illustrate that for closed loop gains of −1 and −5 the resulting pulse fidelity suggests quite similiar bandwidths for both configurations.



TL/H/11926–20

1A. $A_V = -1$



TL/H/11926–21

1B. $A_V = -5$

FIGURE 1A, 1B. Variation of Closed-Loop Gain from −1 to −5 Yields Similar Responses.

FEEDBACK RESISTOR SELECTION: R_f

Selecting the feedback resistor, R_f, is a dominant factor in compensating the LM6182. For general applications the LM6182 will maintain specified performance with an 820Ω feedback resistor. The closed-loop bandwidth of the LM6182 depends on the feedback resistance, R_f. Therefore, Rs, and not R_f, is varied to adjust for the desired closed-loop gain as demonstrated in *Figure 2*.

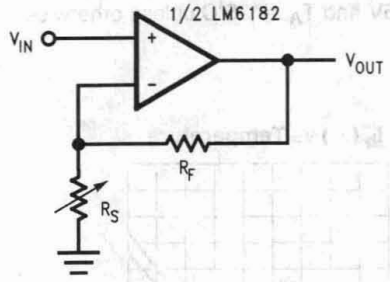


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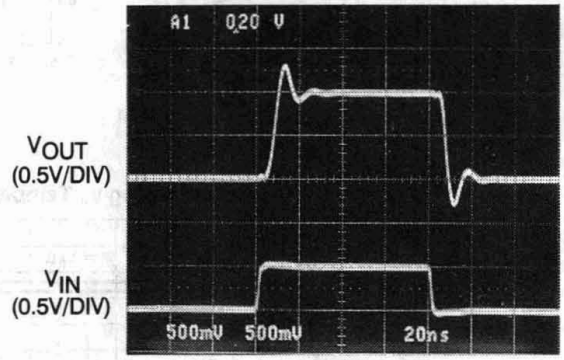
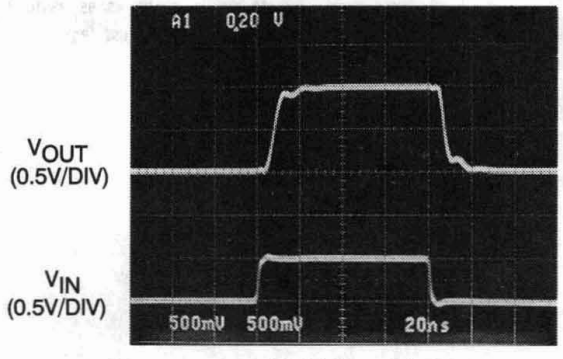
FIGURE 2. R_f Sets Amplifier Bandwidth and R_s is Adjusted to Obtain the Desired Closed-Loop Gain, A_V.

Although this R_f value will provide good results for most applications, it may be advantageous to adjust this value slightly. Consider, for instance, the effect on pulse responses with two different configurations where both the closed-loop gains are +2 and the feedback resistors are 820Ω, and 1640Ω, respectively. *Figures 3A* and *3B* illustrate the effect of increasing R_f while maintaining the same closed-loop gain – the amplifier bandwidth decreases. Accordingly, larger feedback resistors can be used to slow down the LM6182 and reduce overshoot in the time domain response. Conversely, smaller feedback resistance values than 820Ω can be used to compensate for the reduction of bandwidth at high closed-loop gains, due to 2nd order effects. For example *Figures 4A* and *4B* illustrate reducing R_f to 500Ω to establish the desired small signal response in an amplifier configured for a closed-loop gain of +25.



TL/H/11926–23

3A. $R_f = 820\Omega$

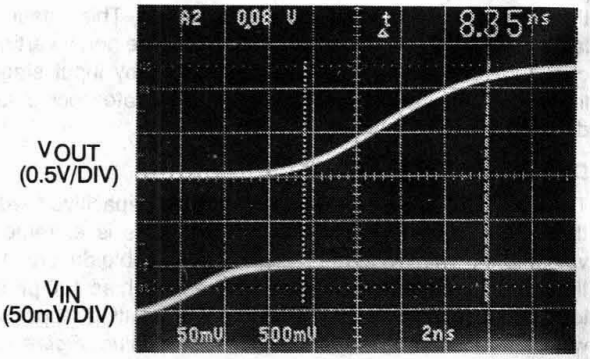


TL/H/11926–24

3B. $R_f = 1640\Omega$

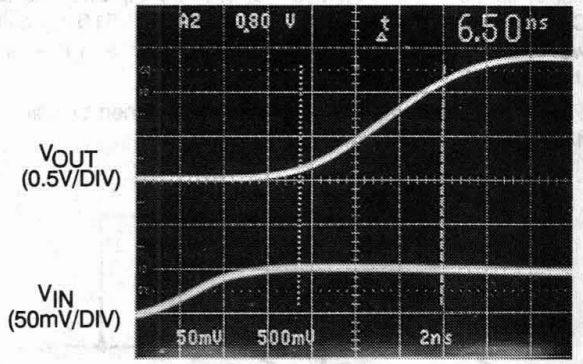
FIGURE 3A, 3B. Increase Compensation by Increasing R_f, $A_V = +2$

Typical Applications (Continued)



TL/H/11926–25

4A. $R_f = 820\Omega$



TL/H/11926–26

4B. $R_f = 500\Omega$

FIGURE 4A, 4B. Reducing R_f to Increase Bandwidth for Large Closed-Loop Gains, $A_V = +25$

The extent of the amplifier's dependence on R_f is displayed in Figure 5 for one particular closed-loop gain.

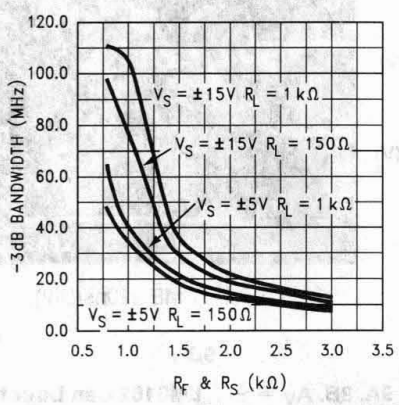


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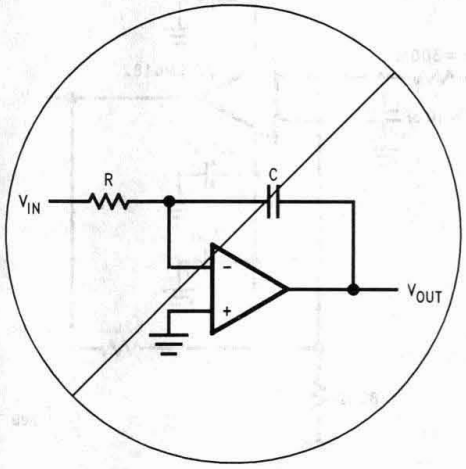
FIGURE 5. −3 dB Bandwidth Is Determined By Selecting R_f.

CAPACITIVE FEEDBACK

Current feedback amplifiers rely on feedback impedance for proper compensation. Even in unity gain current feedback amplifiers require a feedback resistor. LM6182 performance is specified for a feedback resistance of 820Ω. Decreasing the feedback impedance below 820Ω extends the amplifier's bandwidth leading to possible instability. Capacitive feedback should therefore not be used because the impedance of a capacitor decreases with increasing frequency.



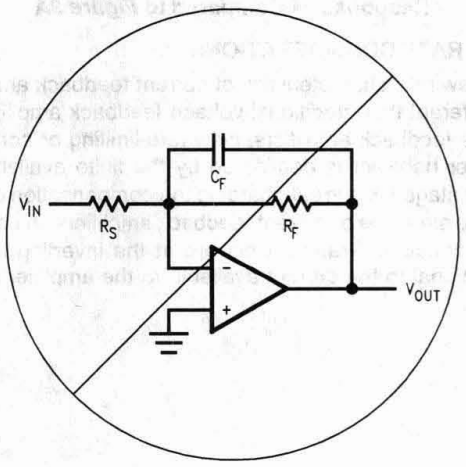
TL/H/11926–28

FIGURE 6. Current Feedback Amplifiers are Unstable with Capacitive Feedback

For voltage feedback amplifiers it is quite common to place a small lead compensation capacitor in parallel with feedback resistance, R_f. This compensation serves to reduce the amplifier's peaking. One application of the lead compensation capacitor is to counteract the effects of stray capacitance from the inverting input to ground in circuit board layouts. The LM6182 current feedback amplifier does not require this lead compensation capacitor and has an even simpler, more elegant solution.

To limit the bandwidth and peaking of the LM6182 current feedback amplifier, do not use a capacitor across R_f as in *Figure 7*. This actually has the opposite effect and extends the bandwidth of the amplifier leading to possible instability. Instead, simply increase the value of the feedback resistor as shown in *Figure 3*.

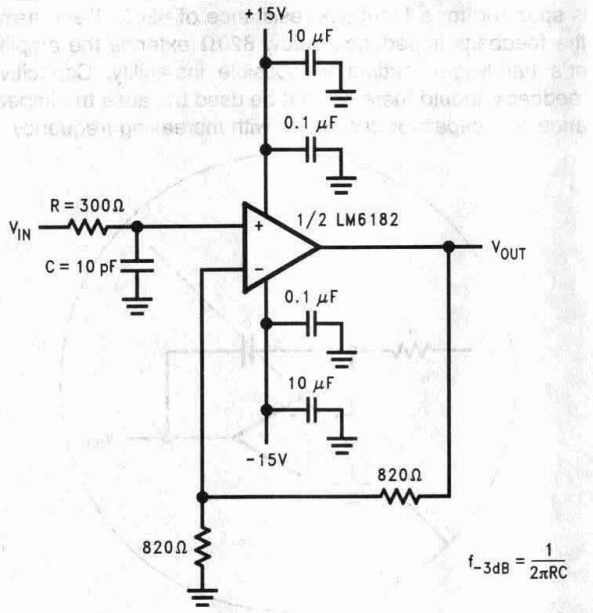
Non-inverting applications can also reduce peaking and limit bandwidth by adding an RC circuit as illustrated in *Figure 8*.



TL/H/11926–29

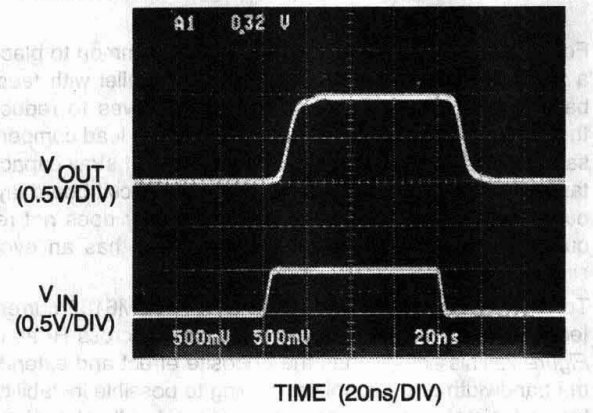
FIGURE 7. Compensation Capacitors Are Not Used with the LM6182, Instead Simply Increase R_f to Compensate

Typical Applications (Continued)



TL/H/11926–30

8A



TIME (20ns/DIV)

TL/H/11926–31

8B

FIGURE 8A, 8B. RC Limits Amplifier Bandwidth to 50 MHz, Eliminating Peaking in the Resulting Pulse Response as Compared to *Figure 3A*

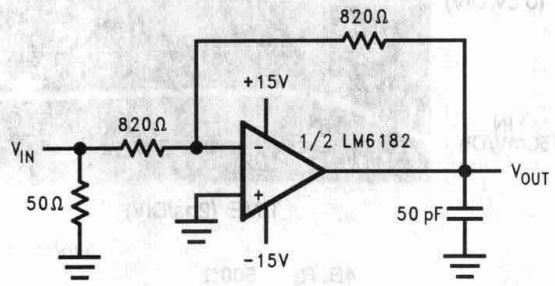
SLEW RATE CONSIDERATIONS

The slew rate characteristics of current feedback amplifiers are different than traditional voltage feedback amplifiers. In voltage feedback amplifiers, slew rate limiting or non-linear amplifier behavior is dominated by the finite availability of the 1st stage tail current charging the compensation capacitor. The slew rate of current feedback amplifiers, in contrast, is not constant. Transient current at the inverting input is proportional to the current available to the amplifier's compensation capacitor. The current feedback amplifier is therefore not traditionally slew rate limited. This enables large slew rates responses of 2000 V/μs. The non-inverting configuration slew rate is also determined by input stage limitations. Accordingly, variations of slew rates occur for different circuit topologies.

DRIVING CAPACITIVE LOADS

The LM6182 can drive significantly larger capacitive loads than many current feedback amplifiers. This is extremely valuable for simplifying the design of coax-cable drivers. Although the LM6182 can directly drive as much as 100 pF of load capacitance without oscillating, the resulting response will be a function of the feedback resistor value. *Figure 9B* illustrates the small-signal pulse response of the LM6182 while driving a 50 pF load. Ringing persists for approximately 100 ns. To achieve pulse responses with less ringing either the feedback resistor can be increased (see Typical Performance Characteristics "Suggested R_f and Rs for C_L"), or resistive isolation can be used (10Ω–51Ω typically works well). Either technique, however, results in lowering the system bandwidth.

Figure 10B illustrates the improvement obtained by using a 47Ω isolation resistor.



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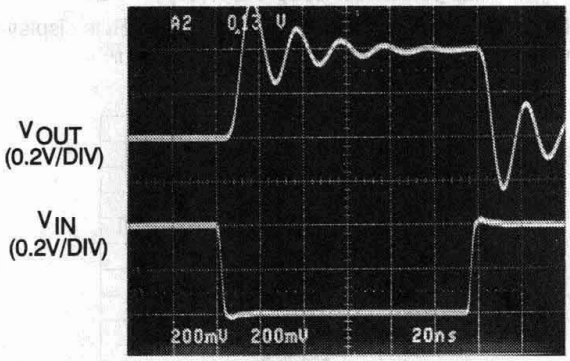
9A



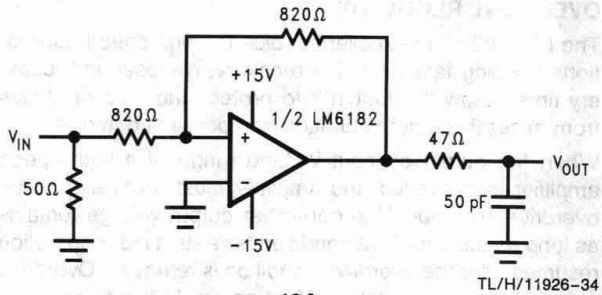
TIME (20ns/DIV)

TL/H/11926–33

9B

FIGURE 9A, 9B. $A_V = -1$, LM6182 Can Directly Drive 50 pF of Load Capacitance with 100 ns of Ringing Resulting in Pulse Response

Typical Applications (Continued)



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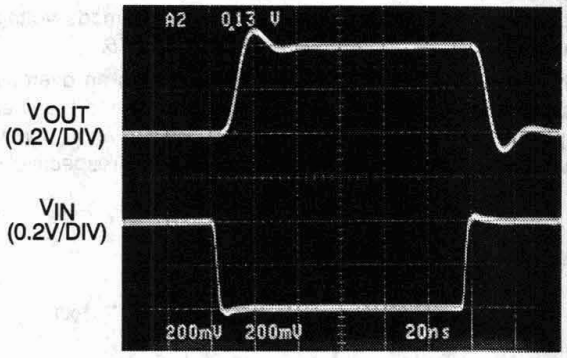
10A



TIME (20ns/DIV)

TL/H/11926–35

10B

FIGURE 10A, 10B. Resistive Isolation of C_L Provides Higher Fidelity Pulse Response. R_f and Rs Could Also Be Increased to Maintain $A_V = -1$ and Improve Pulse Response Characteristics.

POWER SUPPLY BYPASSING AND LAYOUT CONSIDERATIONS

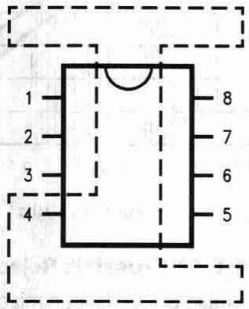
A fundamental requirement for high-speed amplifier design is adequate bypassing of the power supply. It is critical to maintain a wideband low-impedance to ground at the amplifiers supply pins to insure the fidelity of high speed amplifier transient signals. 0.1 μF ceramic bypass capacitors at each supply pin are sufficient for many applications. Typically 10 μF tantalum capacitors are also required if large current transients are delivered to the load. The bypass capacitors should be placed as close to the amplifier pins as possible, such as 0.5″ or less.

Applications requiring high output power, cable drivers for example, cause increased internal power dissipation. Internal power dissipation can be minimized by operating at reduced power supply voltages, such as ±5V.

Optimum heat dissipation is achieved by using wide circuit board traces and soldering the part directly onto the board. Large power supply and ground planes will improve power dissipation. Safe Operating Area (S.O.A.) is determined using the Maximum Power Derating Curves.

The 16-pin small outline package (M) has 5 V− heat sinking pins that enable a junction-to-ambient thermal resistance of 70°C/W when soldered to 2 in^2 1 oz. copper trace. A V− heat sinking pin is located on each corner of the package for ease of layout. This allows high output power and/or operation at elevated ambient temperatures without the additional cost of an integrated circuit heat sink. If the heat sinking capabilities of the S.O. package are not needed, pin 4 and at least one of pins 1,8,9, or 16 must be connected to V− for proper operation.

Figure 11 shows recommended copper patterns used to dissipate heat from the LM6182.



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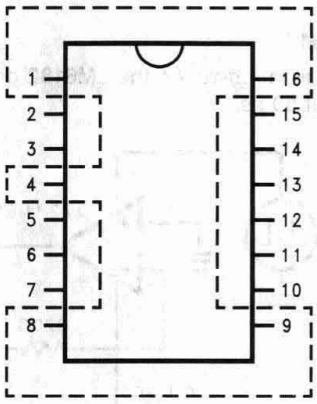
8-pin DIP (N)



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16-pin S.O. (M)

FIGURE 11. Copper Heatsink Layouts

2

Typical Applications (Continued)

CROSSTALK REJECTION

The LM6182 has an excellant crosstalk rejection value of 62 dB at 10 MHz. This value is made possible because the LM6182 amplifiers share no common circuitry other than the supply. High frequency crosstalk that does appear is primarily caused by the magnetic and capacitive coupling of the internal bond wires. Bond wires connect the die to the package lead frame. The amount of current flowing through the bond wires is proportional to the amount of crosstalk. Therefore, crosstalk rejection ratings will degrade when driving heavy loads. *Figure 12* and shows a 10 dB difference for two different loads.

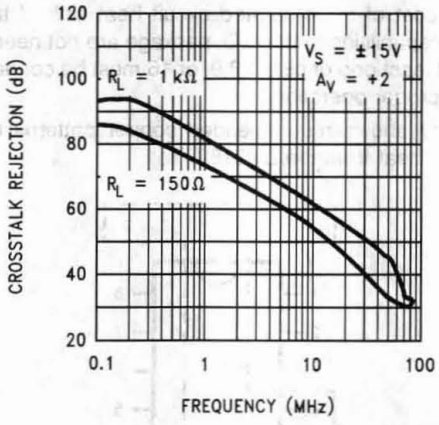

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FIGURE 12. Crosstalk Rejection

The LM6182 crosstalk effect is minimized in applications that cascade the amplifiers by preceding amplifier A with amplifier B.

START-UP TIME

Using the circuit in *Figure 13*, the LM6182 demonstrated a start-up time of 50 ns.

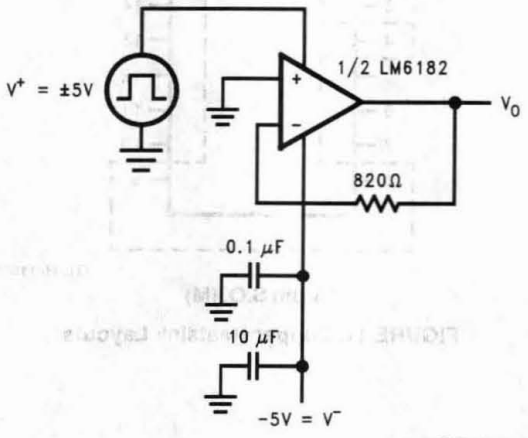

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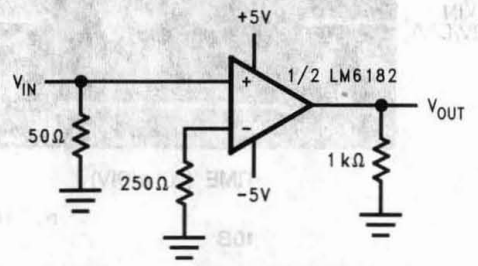
FIGURE 13. Start-Up Test Circuit

OVERDRIVE RECOVERY

The LM6182 is an excellent choice for high speed applications needing fast overdrive recovery. Nanosecond recovery times allow the LM6182 to protect subsequent stages from excessive input saturation and possible damage.

When the output or input voltage range of a high speed amplifier is exceeded, the amplifier must recover from an overdrive condition. The non-linear output voltage remains as long as the overdrive condition persists. Linear operation resumes after the overdrive condition is removed. Overdrive recovery time is the delay before an amplifier returns to linear operation. The typical recovery times for exceeding open loop, closed loop, and input commom-mode voltage ranges are illustrated in *Figures 14, 15,* and *16*.

The open-loop circuit of *Figure 14* generates an overdrive response by allowing the ±0.5V input to exceed the linear input range of the amplifier. Typical positive and negative overdrive recovery times are 5 ns and 30 ns, respectively.



TL/H/11926–41

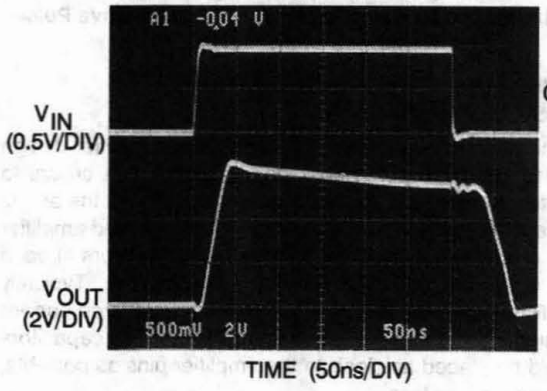


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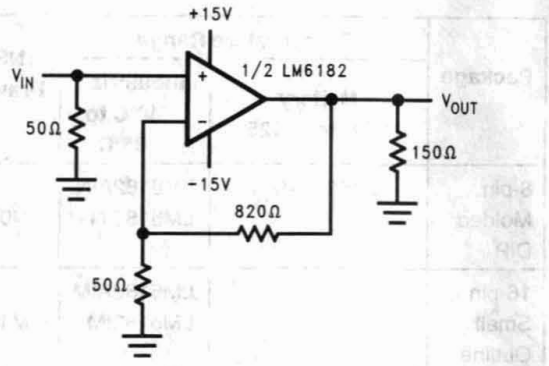
FIGURE 14. Open Loop Overdrive Recovery Times of 5 ns and 30 ns

The large closed-loop gain configuration in *Figure 15* forces the amplifier output into overdrive. The typical recovery time to a linear output value is 15 ns.

Typical Applications (Continued)



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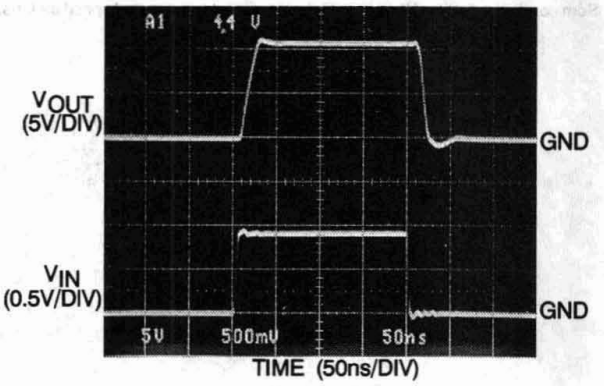
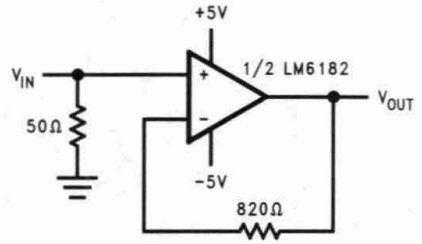


TL/H/11926–44

FIGURE 15. 15 ns Closed Loop Output Overdrive Recovery Time Generated by Saturating the Output Stage of the LM6182

The common-mode input range of a unity-gain circuit is exceeded by a 4V pulse resulting in a typical recovery time of 20 ns shown in *Figure 16*.



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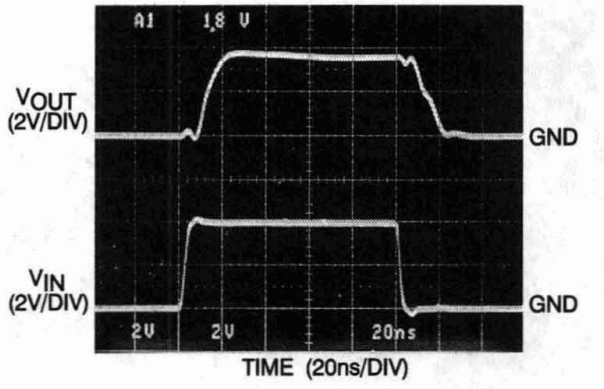

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FIGURE 16. Output Recovery from an Input that Exceeds the Common-Mode Range

SPICE MACROMODEL

A spice macromodel is available for the LM6182. Contact your local National Semiconductor sales office to obtain an operational amplifier spice model library disk.

Typical Application Circuits

UNITY GAIN AMPLIFIER

The LM6182 current feedback amplifier is unity gain stable. The feedback resistor, R_f, is required to maintain the LM6182's dynamic performance.

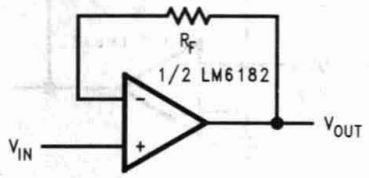

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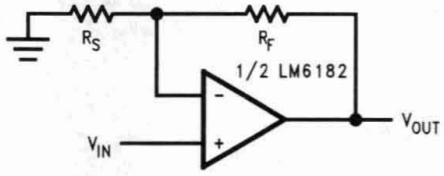
FIGURE 17. LM6182 Is Unity Gain Stable

NON-INVERTING GAIN AMPLIFIER

Current feedback amplifiers can be used in non-inverting gain and level shifting functions. The same basic closed-loop gain equation used for voltage feedback amplifiers applies to current feedback amplifiers: $1 + R_f/Rs$.



TL/H/11926–48

FIGURE 18. Non-Inverting Closed Loop Gain is Determined with the Same Equation Voltage Feedback Amplifiers Use: $1 + R_f/Rs$

INVERTING GAIN AMPLIFIER

The inverting closed loop gain equation used with voltage feedback amplifiers also applies to current feedback amplifiers.

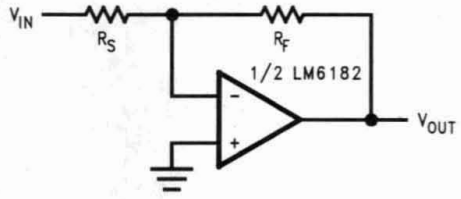


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FIGURE 19. Current Feedback Amplifiers Can Be Used for Inverting Gains, Just Like a Voltage Feedback Amplifier: $-R_f/Rs$

Typical Application Circuits (Continued)

SUMMING AMPLIFIER

The current feedback topology of the LM6182 provides significant performance advantages over a conventional voltage feedback amplifier used in a standard summing circuit. Using a voltage feedback amplifier, the bandwidth of the summing circuit in *Figure 20* is limited by the highest gain needed for either signal V1 or V2. If the LM6182 amplifier is used instead, wide circuit bandwidth can be maintained relatively independent of gain requirements.

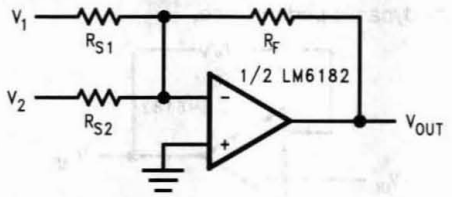

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FIGURE 20. LM6182 Allows the Summing Circuit to Meet the Requirements of Wide Bandwidth Systems Independent of Signal Gain

Ordering Information

Package	Temperature Range		NSC Drawing
	Military −55°C to +125°C	Industrial −40°C to +85°C	
8-pin Molded DIP	LM6182AMN	LM6182AIN LM6182IN	N08E
16-pin Small Outline		LM6182AIM LM6182IM	M16A

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office or Distributors for availability and specifications.

National Semiconductor

LM7131
Tiny High Speed Single Supply Operational Amplifier

General Description

The LM7131 is a high speed bipolar operational amplifier available in a tiny SOT23-5 package. This makes the LM7131 ideal for space and weight critical designs. Single supply voltages of 3V and 5V provides good video performance, wide bandwidth, low distortion, and high PSRR and CMRR. This makes the amplifier an excellent choice for desktop and portable video and computing applications. The amplifier is supplied in DIPs, surface mount 8-pin packages, and tiny SOT23-5 packages.

Tiny amplifiers are so small they can be placed anywhere on a board close to the signal source or next to an A-to-D input. Good high speed performance at low voltage makes the LM7131 a preferred part for battery powered designs.

Features

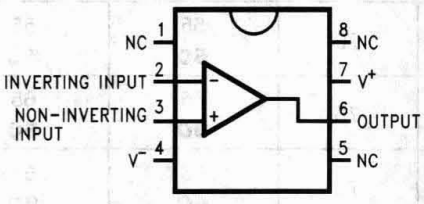
- Tiny SOT23-5 package saves space-typical circuit layouts take half the space of SO-8 designs.
- Guaranteed specs at 3V, 5V, and ±5V supplies
- Typical supply current 7.0 mA at 5V, 6.5 mA at 3V
- 4V output swing with +5V single supply
- Typical total harmonic distortion of 0.1% at 4 MHz
- 70 MHz Gain-Bandwidth Product
- 90 MHz −3 dB bandwidth at 3V and 5V, Gain = +1
- Designed to drive popular video A/D converters
- 40 mA output can drive 50Ω loads
- Differential gain and phase 0.25% and 0.75° at A_V = +2

Applications

- Driving video A/D converters
- Video output for portable computers and PDAs
- Desktop teleconferencing
- High fidelity digital audio
- Video cards

Connection Diagrams

8-Pin DIP/SO-8



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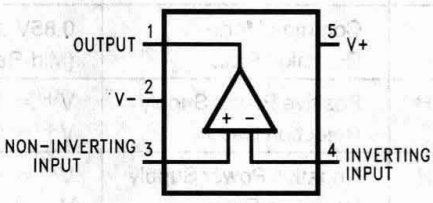
Top View

5-Pin SOT23-5



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Top View

Package	Ordering Information	NSC Drawing Number	Package Marking	Supplied as
8-Pin DIP	LM7131ACN	N08E	LM7131ACN	rails
8-Pin DIP	LM7131BCN	N08E	LM7131BCN	rails
8-Pin SO-8	LM7131ACM	M08A	LM7131ACM	rails
8-Pin SO-8	LM7131BCM	M08A	LM7131BCM	rails
8-Pin SO-8	LM7131ACMX	M08A	LM7131ACM	2.5k units tape and reel
8-Pin SO-8	LM7131BCMX	M08A	LM7131BCM	2.5k units tape and reel
5-Pin SOT 23-5	LM7131ACM5	MA05A	A02A	250 units on tape and reel
5-Pin SOT 23-5	LM7131BCM5	MA05A	A02B	250 units on tape and reel
5-Pin SOT 23-5	LM7131ACM5X	MA05A	A02A	3k units tape and reel
5-Pin SOT 23-5	LM7131BCM5X	MA05A	A02B	3k units tape and reel

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

ESD Tolerance (Note 2)	2000V
Differential Input Voltage	±2.0
Voltage at Input/Output Pin	$(V^+)+0.1V$, $(V^-)-0.3V$
Supply Voltage $(V^+ - V^-)$	12V
Current at Input Pin	±5 mA
Current at Output Pin (Note 3)	±80 mA
Current at Power Supply Pin	±80 mA
Lead Temperature (soldering, 10 sec)	260°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature (Note 4)	150°C

Operating Ratings

Supply Voltage $(V^+ - V^-)$	$2.7V \le V \le 12V$
Junction Temperature Range	
LM7131AC, LM7131BC	$0°C \le T_J \le +70°C$
Thermal Resistance (θ_{JA})	
N Package, 8-Pin Molded DIP	115°C/W
SO-8 Package, 8-Pin Surface Mount	165°C/W
M05A Package, 5-Pin Surface Mount	325°C/W

3V DC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for $T_J = 25°C$, $V^+ = 3V$, $V^- = 0V$, $V_{CM} = V_O = V^+/2$ and $R_L = 150\Omega$. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Typ (Note 5)	LM7131AC Limit (Note 6)	LM7131BC Limit (Note 6)	Units
V_{OS}	Input Offset Voltage		0.02	2 **4**	7 **10**	mV max
TCV_{OS}	Input Offset Voltage Average Drift		10			µV/°C
I_B	Input Bias Current		20	30 **40**	30 **40**	µA max
I_{OS}	Input Offset Current		0.35	3.5 **5**	3.5 **5**	µA max
CMRR	Common Mode Rejection Ratio	$0V \le V_{CM} \le 0.85V$ (Video Levels)	75	60 **55**	60 **55**	dB min
CMRR	Common Mode Rejection Ratio	$0.85V \le V_{CM} \le 1.7V$ (Mid-Range)	70	55 **50**	55 **50**	dB min
+PSRR	Positive Power Supply Rejection Ratio	$V^+ = 3V$, $V^- = 0V$ $V^+ = 3V$ to 6.5V	75	65 **60**	65 **60**	dB min
−PSRR	Negative Power Supply Rejection Ratio	$V^- = -3V$, $V^+ = 0V$ $V^- = -3V$ to $-6.5V$	75	65 **60**	65 **60**	dB min
V_{CM}	Input Common-Mode Voltage Range	$V^+ = 3V$ For CMRR ≥ 50 dB	0.0	0.0 **0.00**	0.0 **0.00**	V min
			2.0	1.70 **1.60**	1.70 **1.60**	V max
A_{VOL}	Voltage Gain	$R_L = 150\Omega$, $V_O = 0.250V$ to 1.250V	60	55 **50**	55 **50**	dB
C_{IN}	Common-Mode Input Capacitance		2			pF

3V DC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for T_J = 25°C, V^+ = 3V, V^- = 0V, V_{CM} = V_O = $V^+/2$ and R_L = 150Ω. **Boldface** limits apply at the temperature extremes. (Continued)

Symbol	Parameter	Conditions	Typ (Note 5)	LM7131AC Limit (Note 6)	LM7131BC Limit (Note 6)	Units
V_O	Output Swing High	V^+ = 3V, R_L = 150Ω terminated at 0V	2.6	2.3 **2.0**	2.3 **2.0**	V min
	Low	V^+ = 3V, R_L = 150Ω terminated at 0V	0.05	0.15 **0.20**	0.15 **0.20**	V max
	High	V^+ = 3V, R_L = 150Ω terminated at 1.5V	2.6	2.3 **2.0**	2.3 **2.0**	V min
	Low	V^+ = 3V, R_L = 150Ω terminated at 1.5V	0.5	0.8 **1.0**	0.8 **1.0**	V max
V_O	Output Swing High	V^+ = 3V, R_L = 600Ω terminated at 0V	2.73			V max
V_O	Output Swing Low	V^+ = 3V, R_L = 600Ω terminated at 0V	0.06			V max
I_{SC}	Output Short Circuit Current	Sourcing, V_O = 0V	65	45 **40**	45 **40**	mA min
		Sinking, V_O = 3V	40	25 **20**	25 **20**	mA min
I_S	Supply Current	V^+ = + 3V	6.5	8.0 **8.5**	8.0 **8.5**	mA max

3V AC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for T_J = 25°C, V^+ = 3V, V^- = 0V, V_{CM} = V_O = $V^+/2$ and R_L = 150Ω. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Typ (Note 5)	LM7131AC Limit (Note 6)	LM7131BC Limit (Note 6)	Units
T.H.D.	Total Harmonic Distortion	F = 4 MHz, A_V = + 2 R_L = 150Ω, V_O = 1.0V_{PP}	0.1			%
	Differential Gain	(Note 10)	0.45			%
	Differential Phase	(Note 10)	0.6			°
SR	Slew Rate	R_L = 150Ω, C_L = 5 pF (Note 7)	120			V/μS
SR	Slew Rate	R_L = 150Ω, C_L = 20 pF (Note 7)	100			V/μS
GBW	Gain-Bandwidth Product		70			MHz
	Closed-Loop − 3 dB Bandwidth		90			MHz

5V DC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for T_J = 25°C, V^+ = 5V, V^- = 0V, V_{CM} = V_O = $V^+/2$ and R_L = 150Ω. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Typ (Note 5)	LM7131AC Limit (Note 6)	LM7131BC Limit (Note 6)	Units
V_{OS}	Input Offset Voltage		0.02	2 **4**	7 **10**	mV max
TCV_{OS}	Input Offset Voltage Average Drift		10			μV/°C
I_B	Input Bias Current		20	30 **40**	30 **40**	μA max
I_{OS}	Input Offset Current		0.35	3.5 **5**	3.5 **5**	μA max
CMRR	Common Mode Rejection Ratio	0V ≤ V_{CM} ≤ 1.85V (Video Levels)	75	65 **60**	65 **60**	dB min
CMRR	Common Mode Rejection Ratio	1.85V ≤ V_{CM} ≤ 3.7V (Mid-Range)	70	55 **50**	55 **50**	dB min
+ PSRR	Positive Power Supply Rejection Ratio	V^+ = 5V, V^- = 0V V^+ = 5V to 10V	75	65 **60**	65 **60**	dB min
− PSRR	Negative Power Supply Rejection Ratio	V^- = − 5V, V^+ = 0V V^- = − 5V to −10V	75	65 **60**	65 **60**	dB min
V_{CM}	Input Common-Mode Voltage Range	V^+ = 5V For CMRR ≥ 50 dB	0.0	− 0.0 **0.00**	− 0.0 **0.00**	V min
			4.0	3.70 **3.60**	3.70 **3.60**	V max
A_{VOL}	Voltage Gain	R_L = 150Ω, V_O = 0.250V to 2.250V	70	60 **55**	60 **55**	dB min
C_{IN}	Common-Mode Input Capacitance		2			pF
V_O	Output Swing High	V^+ = 5V, R_L = 150Ω terminated at 0V	4.5	4.3 **4.0**	4.3 **4.0**	V min
	Low	V^+ = 5V, R_L = 150Ω terminated at 0V	0.08	0.15 **0.20**	0.15 **0.20**	V max
	High	V^+ = 5V, R_L = 150Ω terminated at 2.5V	4.5	4.3 **4.0**	4.3 **4.0**	V min
	Low	V^+ = 5V, R_L = 150Ω terminated at 2.5V	0.5	0.8 **1.0**	0.8 **1.0**	V max
V_O	Output Swing High	V^+ = 5V, R_L = 600Ω terminated at 0V	4.70			V max
V_O	Ouptut Swing Low	V^+ = 5V, R_L = 600Ω terminated at 0V	0.07			V max
I_{SC}	Output Short Circuit Current	Sourcing, V_O = 0V	65	45 **40**	45 **40**	mA min
		Sinking, V_O = 5V	40	25 **20**	25 **20**	mA min
I_S	Supply Current	V^+ = +5V	7.0	8.5 **9.0**	8.5 **9.0**	mA max

5V AC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for $T_J = 25°C$, $V^+ = 5V$, $V^- = 0V$, $V_{CM} = V_O = V^+/2$ and $R_L = 150\Omega$. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Typ (Note 5)	LM7131AC Limit (Note 6)	LM7131BC Limit (Note 6)	Units
T.H.D.	Total Harmonic Distortion	$F = 4$ MHz, $A_V = +2$ $R_L = 150\Omega$, $V_O = 2.0V_{PP}$	0.1			%
	Differential Gain	(Note 10)	0.25			%
	Differential Phase	(Note 10)	0.75			°
SR	Slew Rate	$R_L = 150\Omega$, $C_L = 5$ pF (Note 8)	150			V/μs
SR	Slew Rate	$R_L = 150\Omega$, $C_L = 20$ pF (Note 8)	130			V/μs
GBW	Gain-Bandwidth Product		70			MHz
	Closed-Loop −3 dB Bandwidth		90			MHz
e_n	Input-Referred Voltage Noise	f = 1 kHz	11			$\frac{nV}{\sqrt{Hz}}$
i_n	Input-Referred Current Noise	f = 1 kHz	3.3			$\frac{pA}{\sqrt{Hz}}$

±5V DC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for $T_J = 25°C$, $V^+ = 5V$, $V^- = 5V$, $V_{CM} = V_O = 0V$ and $R_L = 150\Omega$. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Typ (Note 5)	LM7131AC Limit (Note 6)	LM7131BC Limit (Note 6)	Units
V_{OS}	Input Offset Voltage		0.02	2 **4**	7 **10**	mV max
TCV_{OS}	Input Offset Voltage Average Drift		10			μV/°C
I_B	Input Bias Current		20	30 **40**	30 **40**	μA max
I_{OS}	Input Offset Current		0.35	3.5 **5**	3.5 **5**	μA max
CMRR	Common Mode Rejection Ratio	$-5V \le V_{CM} \le 3.7V$	75	65 **60**	65 **60**	dB min
+PSRR	Positive Power Supply Rejection Ratio	$V^+ = 5V$, $V^- = 0V$ $V^+ = 5V$ to 10V	75	65 **60**	65 **60**	dB min
−PSRR	Negative Power Supply Rejection Ratio	$V^- = -5V$, $V^+ = 0V$ $V^- = -5V$ to $-10V$	75	65 **60**	65 **60**	dB min
V_{CM}	Input Common-Mode Voltage Range	$V^+ = 5V$, $V^- = -5V$ For CMRR ≥ 60 dB	−5.0	−5.0 **−5.0**	−5.0 **−5.0**	V min
			4.0	3.70 **3.60**	3.70 **3.60**	V max
A_{VOL}	Voltage Gain	$R_L = 150\Omega$, $V_O = -2.0$ to $+2.0$	70	55 **50**	55 **50**	dB

±5V DC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for T_J = 25°C, V^+ = 5V, V^- = 5V, V_{CM} = V_O = 0V and R_L = 150Ω. **Boldface** limits apply at the temperature extremes. (Continued)

Symbol	Parameter	Conditions	Typ (Note 5)	LM7131AC Limit (Note 6)	LM7131BC Limit (Note 6)	Units
C_{IN}	Common-Mode Input Capacitance		2			pF
V_O	Output Swing High	V^+ = 5V, V^- = −5V R_L = 150Ω terminated at 0V	4.5	4.3 **4.0**	4.3 **4.0**	V min
	Low		−4.5	−3.5 **−2.5**	−3.5 **−2.5**	V max
I_{SC}	Output Short Circuit Current	Sourcing, V_O = −5V	65	45 **40**	45 **40**	mA min
		Sinking, V_O = 5V	40	25 **20**	25 **20**	mA min
I_S	Supply Current	V^+ = +5V, V^- = −5V	7.5	9 **10**	9 **10**	mA max

±5V AC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for T_J = 25°C, V^+ = 5V, V^- = 5V, V_{CM} = V_O = 0V and R_L = 150Ω. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Typ (Note 5)	LM7131AC Limit (Note 6)	LM7131BC Limit (Note 6)	Units
T.H.D.	Total Harmonic Distortion	F = 4 MHz, A_V = −2 R_L = 150Ω, V_O = 4.0V_{PP}	1.5			%
	Differential Gain	(Note 10)	0.25			%
	Differential Phase	(Note 10)	1.0			°
SR	Slew Rate	R_L = 150Ω, C_L = 5 pF (Note 9)	150			V/μs
SR	Slew Rate	R_L = 150Ω, C_L = 20 pF (Note 9)	130			V/μs
GBW	Gain-Bandwidth Product		70			MHz
	Closed-Loop −3 dB Bandwidth		90			MHz

Note 1: Absolute maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not guaranteed. For guaranteed specifications and the test conditions, see the Electrical characteristics.

Note 2: Human body model, 1.5 kΩ in series with 100 pF.

Note 3: Applies to both single-supply and split-supply operation. Continuous short circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 150°C.

Note 4: The maximum power dissipation is a function of $T_{J(max)}$, θ_{JA}, and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(max)} - T_A)/\theta_{JA}$. All numbers apply for packages soldered directly into a PC board.

Note 5: Typical values represent the most likely parametric norm.

Note 6: All limits are guaranteed by testing or statistical analysis.

Note 7: Connected as voltage follower with 1.5V step input. Number specified is the slower of the positive and negative slew rates. V^+ = 3V and R_L = 150Ω connected to 1.5V. Amp excited with 1 kHz to produce V_O = 1.5 V_{PP}.

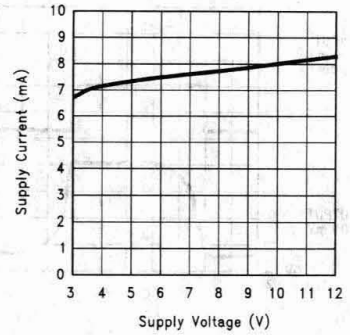
Note 8: Connected as Voltage Follower with 4.0V step input. Number specified is the slower of the positive and negative slew rates. V^+ = 5V and R_L = 150Ω connected to 2.5V. Amp excited with 1 kHz to produce V_O = 4 V_{PP}.

Note 9: Connected as Voltage Follower with 4.0V step input. Number specified is the slower of the positive and negative slew rates. V^+ = 5V, V^- = −5V and R_L = 150Ω connected to 0V. Amp excited with 1 kHz to produce V_O = 4 V_{PP}.

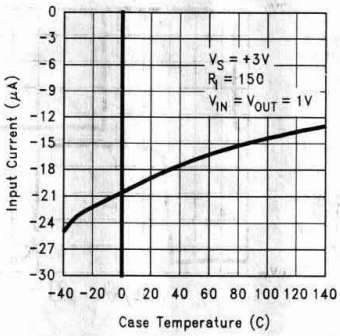
Note 10: Differential gain and phase measured with a 4.5 MHz signal into a 150Ω load, Gain = +2.0, between 0.6V and 2.0V output.

Typical Performance Characteristics

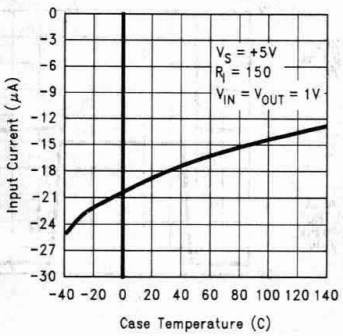
LM7131 Supply Current vs Supply Voltage



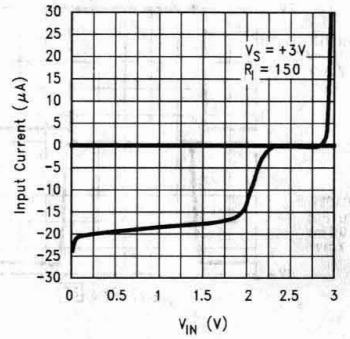
LM7131 Input Current vs Temperature @ 3V



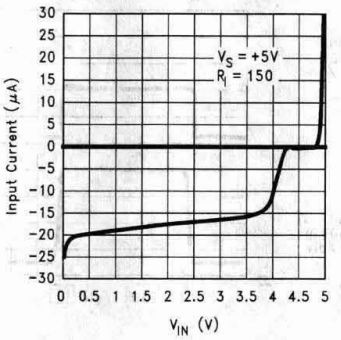
LM7131 Input Current vs Temperature @ 5V



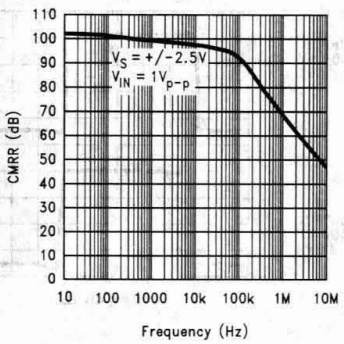
LM7131 Input Current vs Input Voltage @ 3V



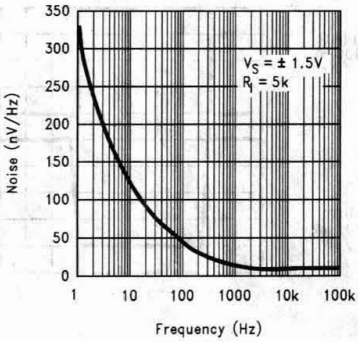
LM7131 Input Current vs Input Voltage @ 5V



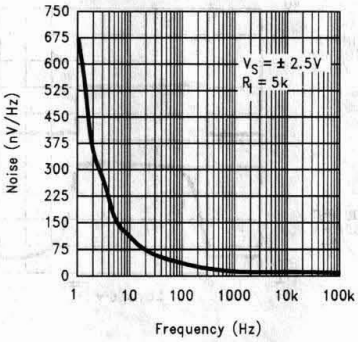
LM7131 CMRR vs Frequency @ 5V



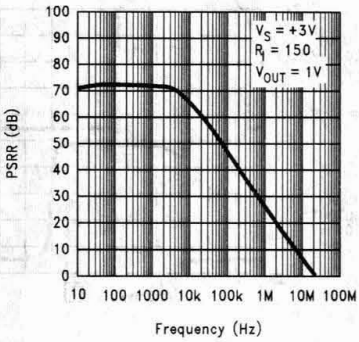
LM7131 Voltage Noise vs Frequency @ 3V



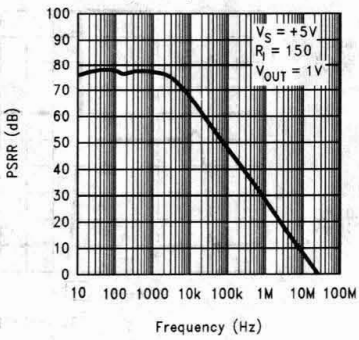
LM7131 Voltage Noise vs Frequency @ 5V



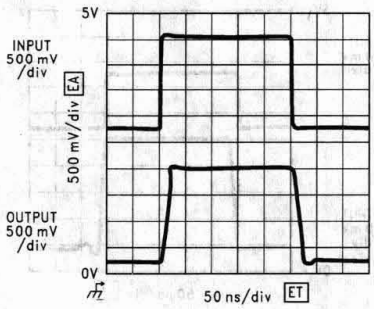
LM7131 PSRR vs Frequency @ 3V



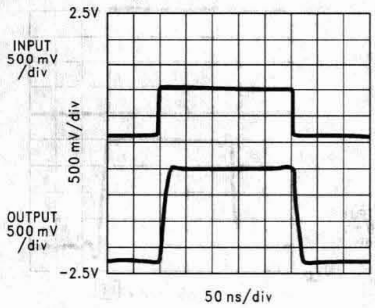
LM7131 PSRR vs Frequency @ 5V



LM7131 Cable Driver A_V = +1 @ +3V



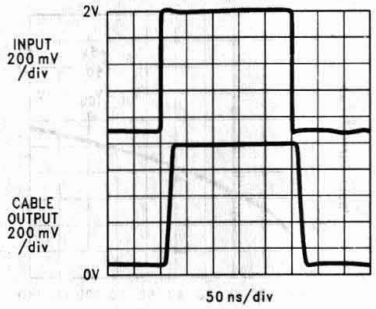
LM7131 Cable Driver A_V = +2 @ +3V



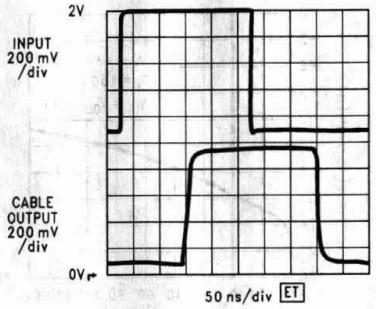
TL/H/12313–3

Typical Performance Characteristics (Continued)

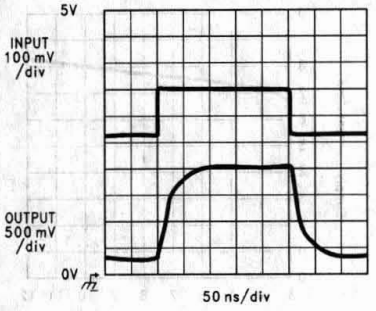
LM7131 Driving 5′ RG-59 $A_V = +2$ @ $+3V$



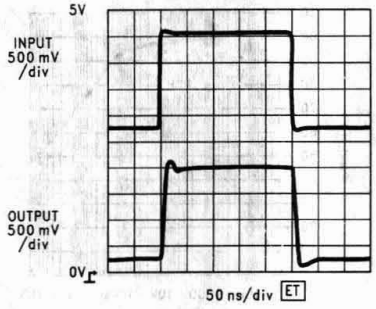
LM7131 Driving 75′ RG-59 $A_V = +2$ @ $+3V$



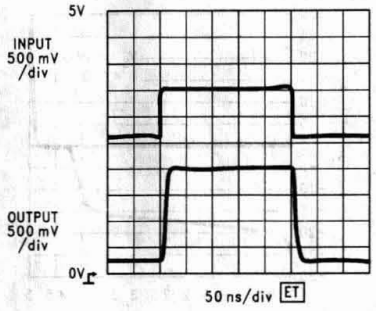
LM7131 Cable Driver $A_V = +10$ @ $+3V$



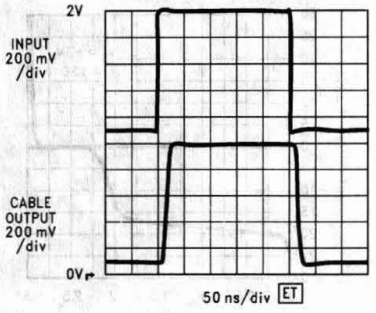
LM7131 Cable Driver $A_V = +1$ @ $+5V$



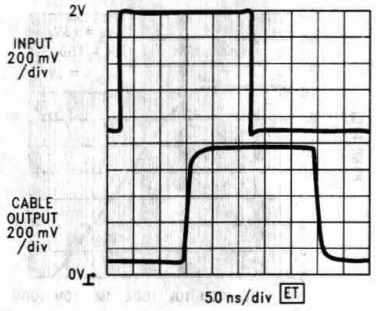
LM7131 Cable Driver $A_V = +2$ @ $+5V$



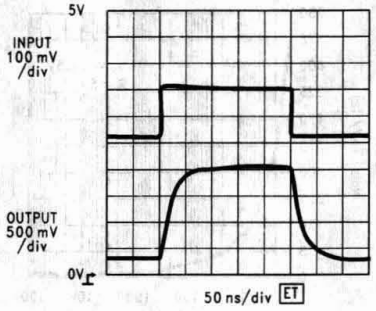
LM7131 Driving 5′ RG-59 $A_V = +2$ @ $+5V$



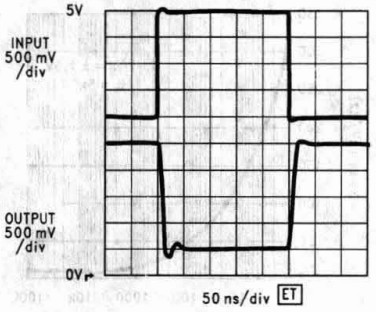
LM7131 Driving 75′ RG-59 $A_V = +2$ @ $+5V$



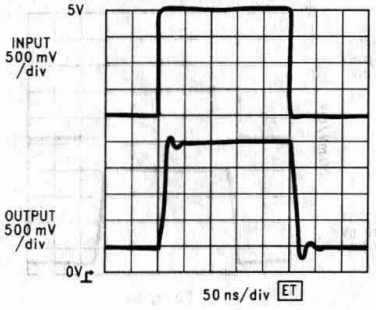
LM7131 Cable Driver $A_V = +10$ @ $+5V$



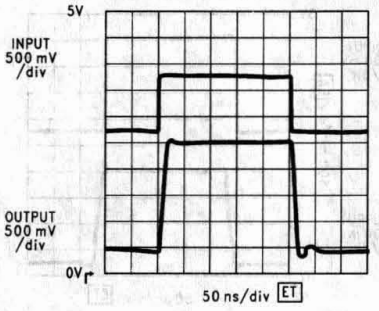
LM7131 Driving Flash A/D Load $A_V = -1$ @ $+5V$



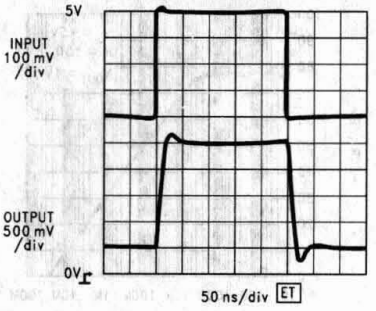
LM7131 Driving Flash A/D Load $A_V = +1$ @ $+5V$



LM7131 Driving Flash A/D Load $A_V = +2$ @ $+5V$



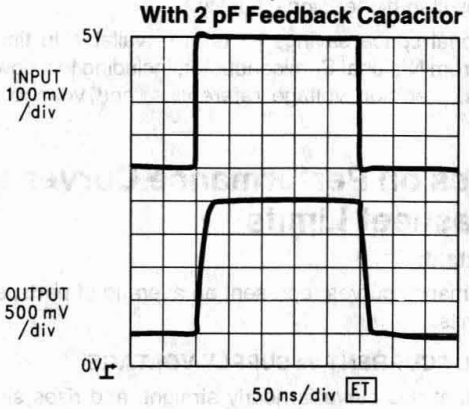
LM7131 Driving Flash A/D Load $A_V = +5$ @ $+5V$



TL/H/12313–4

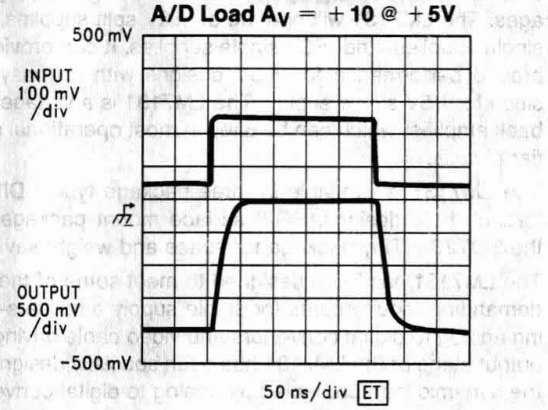
Typical Performance Characteristics (Continued)

LM7131 Driving Flash
A/D Load $A_V = +5$ @ $+5V$
With 2 pF Feedback Capacitor



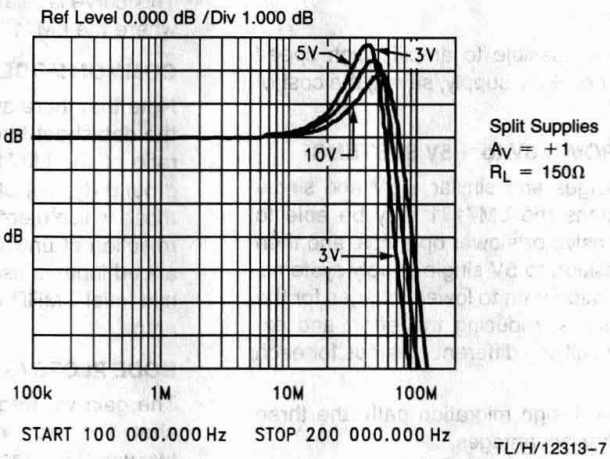
TL/H/12313–5

LM7131 Driving Flash
A/D Load $A_V = +10$ @ $+5V$



TL/H/12313–6

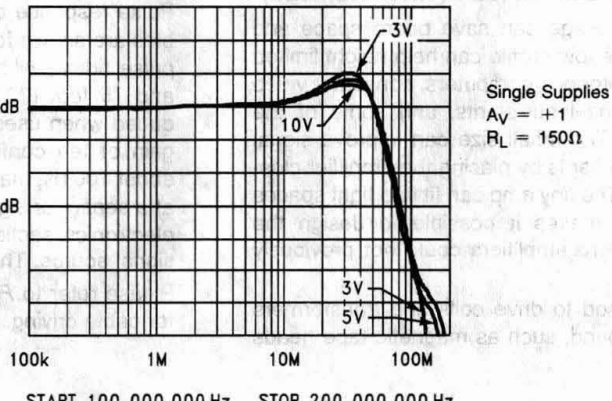
LM7131 Bode Plot
@ 3V, 5V and 10V



Split Supplies
$A_V = +1$
$R_L = 150\Omega$

TL/H/12313–7

LM7131 Single Supply
Bode Plot @ 3V, 5V and 10V



Single Supplies
$A_V = +1$
$R_L = 150\Omega$

TL/H/12313–8

2

Application Information

GENERAL INFORMATION

The LM7131 is a high speed complementary bipolar amplifier which provides high performance at single supply voltages. The LM7131 will operate at ±5V split supplies, +5V single supplies, and +3V single supplies. It can provide improved performance for ±5V designs with an easy transition to +5V single supply. The LM7131 is a voltage feedback amplifier which can be used in most operational amplifier circuits.

The LM7131 is available in three package types: DIPs for through hole designs, SO-8 surface mount packages and the SOT23-5 Tiny package for space and weight savings.

The LM7131 has been designed to meet some of the most demanding requirements for single supply amplifiers—driving analog to digital converters and video cable driving. The output stage of the LM7131 has been specially designed for the dynamic load presented by analog to digital converters. The LM7131 is capable of a 4V output range with a +5V single supply. The LM7131's drive capability and good differential gain and phase make quality video possible from a small package with only a +5V supply.

BENEFITS OF THE LM7131

The LM7131 can make it possible to amplify high speed signals with a single +5V or +3V supply, saving the cost of split power supplies.

EASY DESIGN PATH FROM ±5V to +5V SYSTEMS

The DIP and SO-8 packages and similar ±5V and single supply specifications means the LM7131 may be able to replace many more expensive or slower op amps, and then be used for an easy transition to 5V single supply systems. This could provide a migration path to lower voltages for the amplifiers in system designs, reducing the effort and expense of testing and re-qualifying different op amps for each new design.

In addition to providing a design migration path, the three packages types have other advantages.

The DIPs can be used for easy prototyping and through hole boards. The SO-8 for surface mount board designs, and using the SOT23-5 for a smaller surface mount package can save valuable board space.

SPECIFIC ADVANTAGES OF SOT23-5 (TINY PACKAGE)

The SOT23-5 (Tiny) package can save board space and allow tighter layouts. The low profile can help height limited designs, such as sub-notebook computers, consumer video equipment, personal digital assistants, and some of the thicker PCMCIA cards. The small size can improve signal integrity in noisy environments by placing the amplifier closer to the signal source. The tiny amp can fit into tight spaces and weighs little. This makes it possible to design the LM7131 into places where amplifiers could not previously fit.

The LM7131 can be used to drive coils and transformers referenced to virtual ground, such as magnetic tape heads and disk drive write heads. The small size of the SOT23-5 package can allow it to be placed with a pre-amp inside of some rotating helical scan video head (VCR) assemblies. This avoids long cable runs for low level video signals, and can result in higher signal fidelity.

Additional space savings parts are available in tiny packages from National Semiconductor, including low power amplifiers, precision voltage references, and voltage regulators.

Notes on Performance Curves and Datasheet Limits

Important:

Performance curves represent an average of parts, and are not limits.

SUPPLY CURRENT vs SUPPLY VOLTAGE

Note that this curve is nearly straight, and rises slowly as the supply voltage increases.

INPUT CURRENT vs INPUT VOLTAGE

This curve is relatively flat in the 200 mV to 4V input range, where the LM7131 also has good common mode rejection.

COMMON MODE VOLTAGE REJECTION

Note that there are two parts to the CMRR specification of the datasheet for 3V and 5V. The common mode rejection ratio of the LM7131 has been maximized for signals near ground (typical of the active part of video signals, such as those which meet the RS-170 levels). This can help provide rejection of unwanted noise pick-up by cables when a balanced input is used with good input resistor matching. The mid-level CMRR is similar to that of other single supply op amps.

BODE PLOTS (GAIN vs FREQUENCY FOR $A_V = +1$)

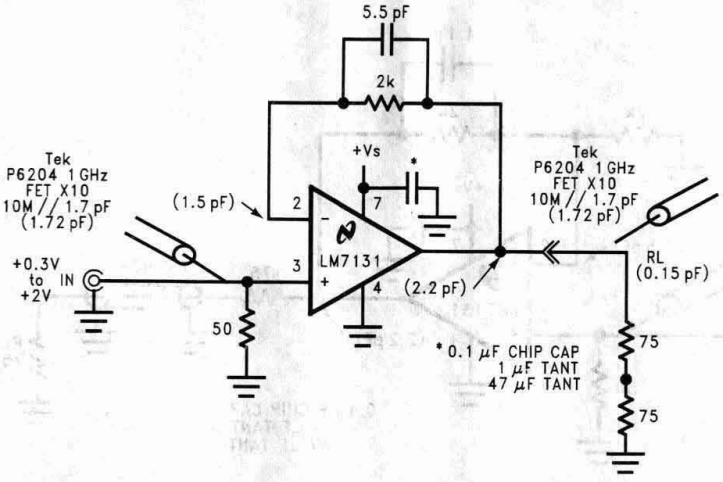
The gain vs. frequency plots for a non-inverting gain of 1 show the three voltages with the 150Ω load connected in two ways. For the single supply graphs, the load is connected to the most negative rail, which is ground. For the split supply graphs, the load is connected to a voltage halfway between the two supply rails.

DRIVING CABLES

Pulse response curves for driving 75Ω back terminate cables are shown for both 3V and 5V supplies. Note the good pulse fidelity with straight 150 loads, five foot (1.5 meter) and 75 foot (22 meter) cable runs. The bandwidth is reduced when used in a gain of ten ($A_V = +10$). Even in a gain of ten configuration, the output settles to < 1% in about 100 ns, making this useful for amplifying small signals at a sensor or signal source and driving a cable to the main electronics section which may be located away from the signal source. This will reduce noise pickup.

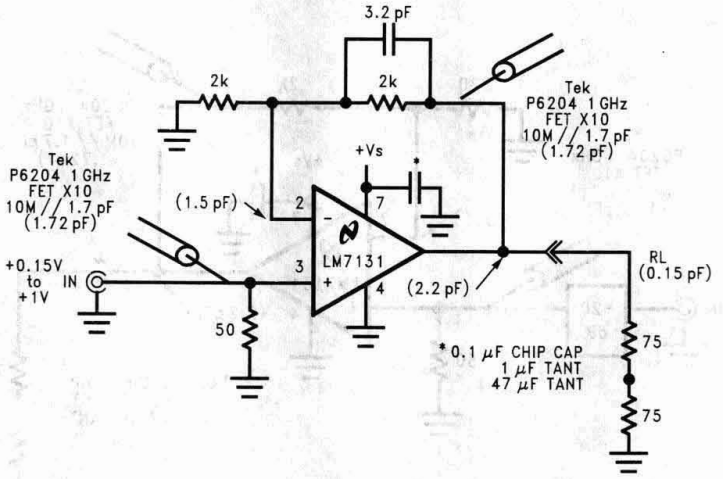
Please refer to *Figures 1–5* for schematics of test setups for cable driving.

Application Information (Continued)



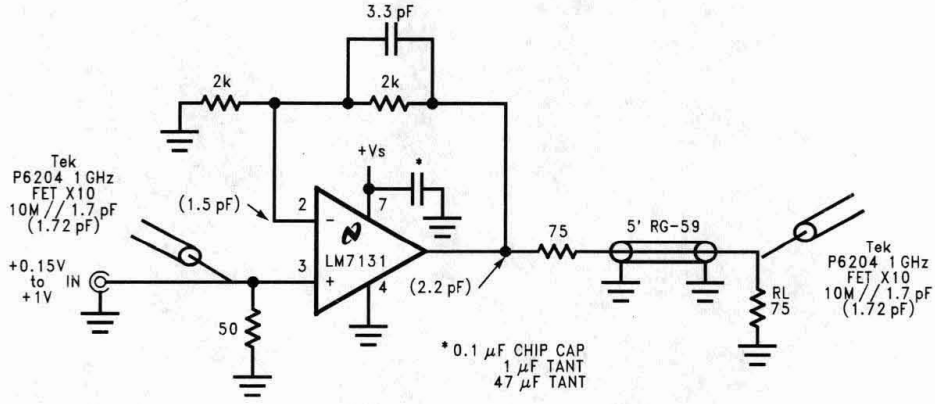
Numbers in parentheses are measured fixture capacitances w/o DUT and load.

FIGURE 1. Cable Driver $A_V = +1$



Numbers in parentheses are measured fixture capacitances w/o DUT and load.

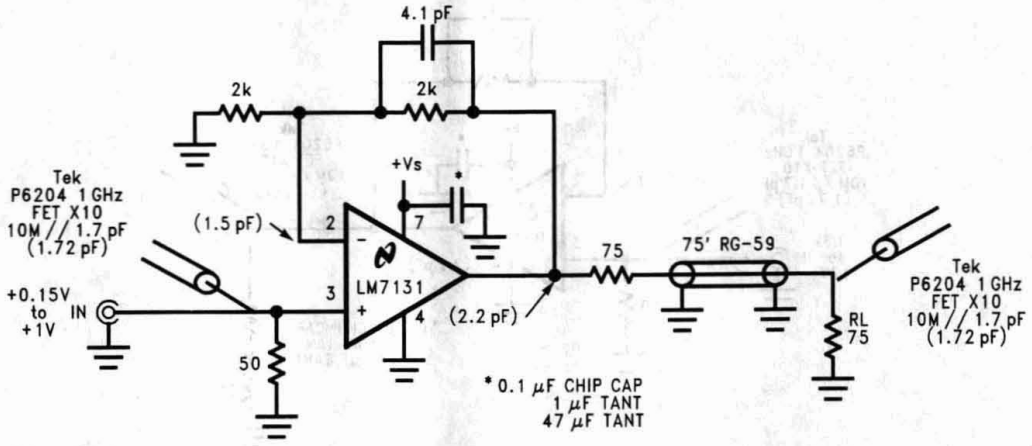
FIGURE 2. Cable Driver $A_V = +2$



Numbers in parentheses are measured fixture capacitances w/o DUT and load.

FIGURE 3. Cable Driver 5' RG-59

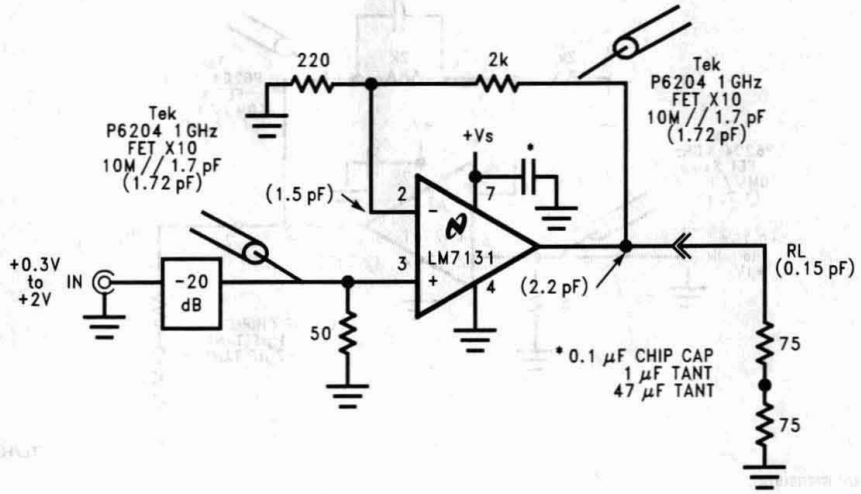
Application Information (Continued)



TL/H/12313–12

Numbers in parentheses are measured fixture capacitances w/o DUT and load.

FIGURE 4. Cable Driver 75' RG-59



TL/H/12313–13

Numbers in parentheses are measured fixture capacitances w/o DUT and load.

FIGURE 5. Cable Driver Gain of 10 $A_V = +10$

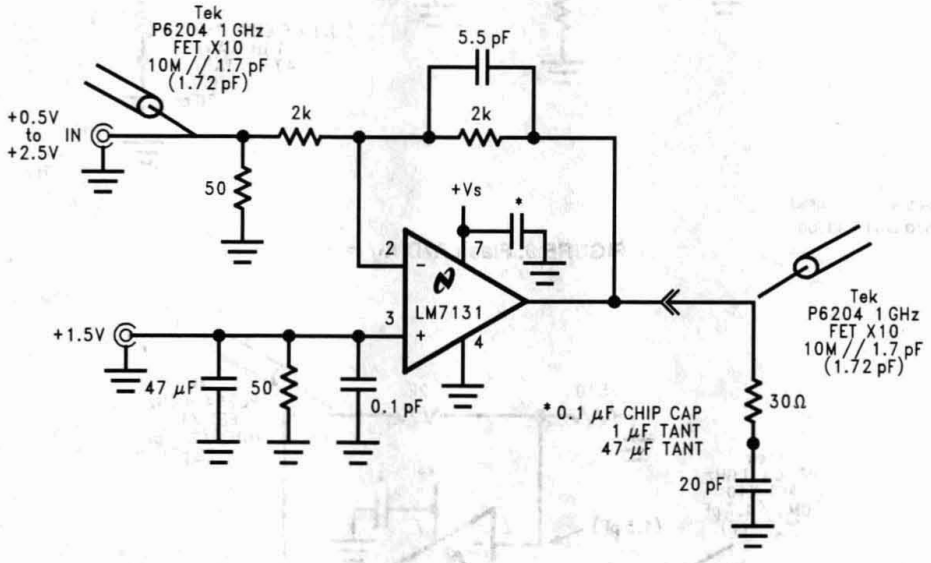
Application Information (Continued)

DRIVING TYPE 1175 FLASH A/D LOADS

The circuits in *Figures 6–11* show a LM7131 in a voltage follower configuration driving the passive equivalent of a typical flash A/D input. Note that there is a slight ringing on the output, which can affect accurate analog-to-digital conversion. In these graphs, we have adjusted the ringing to be a little larger than desirable in order to better show the settling time. Most settling times at low gain are about 75 ns to < 1% of final voltage. The ringing can be reduced by adding a low value (approximately 500Ω) feedback resistor from the output to the inverting input and placing a small (picofarad range) capacitor across the feedback resistor. See *Figures 9* and *10* for schematics and respective performance curves for flash A/D driving at $A_V = +5$ with and without a 2 pF feedback capacitor.

See section on feedback compensation. Ringing can also be reduced by placing an isolation resistor between the output and the analog-to-digital converter input—see sections on driving capacitive loads and analog-to-digital converters.

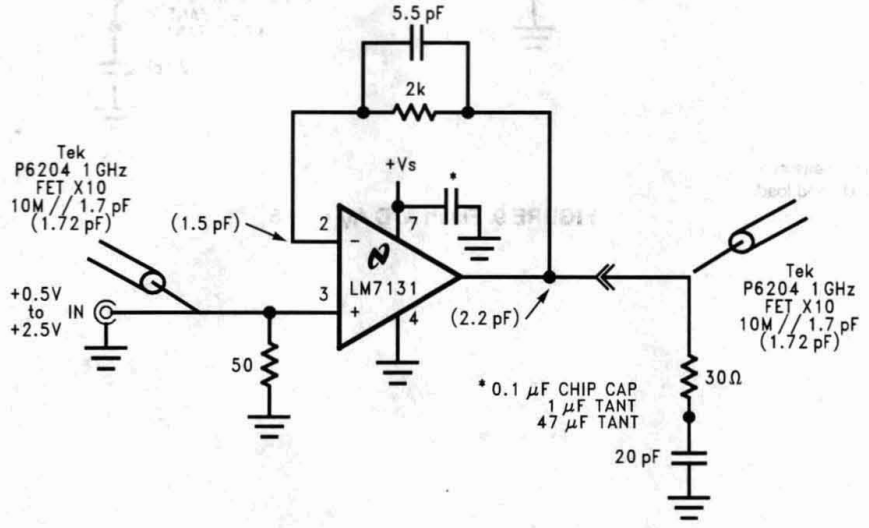
Please refer to *Figures 6–11* for schematics of test setups for driving flash A/D converters.



TL/H/12313–14

Numbers in parentheses are measured fixture capacitances w/o DUT and load.

FIGURE 6. Flash A/D $A_V = -1$

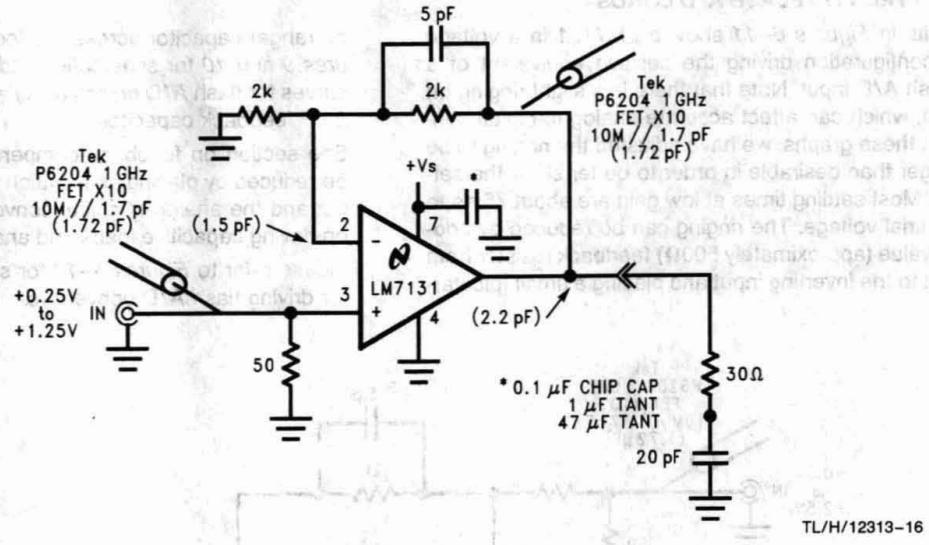


TL/H/12313–15

Numbers in parentheses are measured fixture capacitances w/o DUT and load.

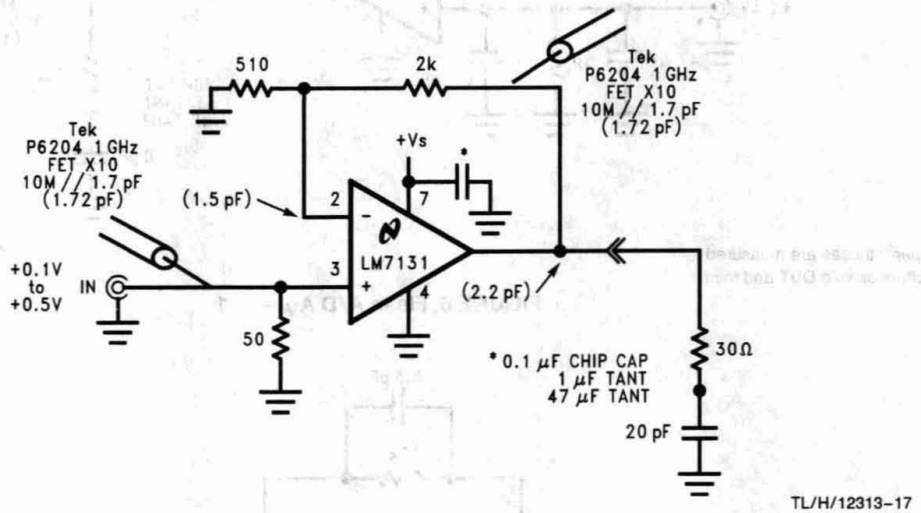
FIGURE 7. Flash A/D $A_V = +1$

Application Information (Continued)



Numbers in parentheses are measured fixture capacitances w/o DUT and load.

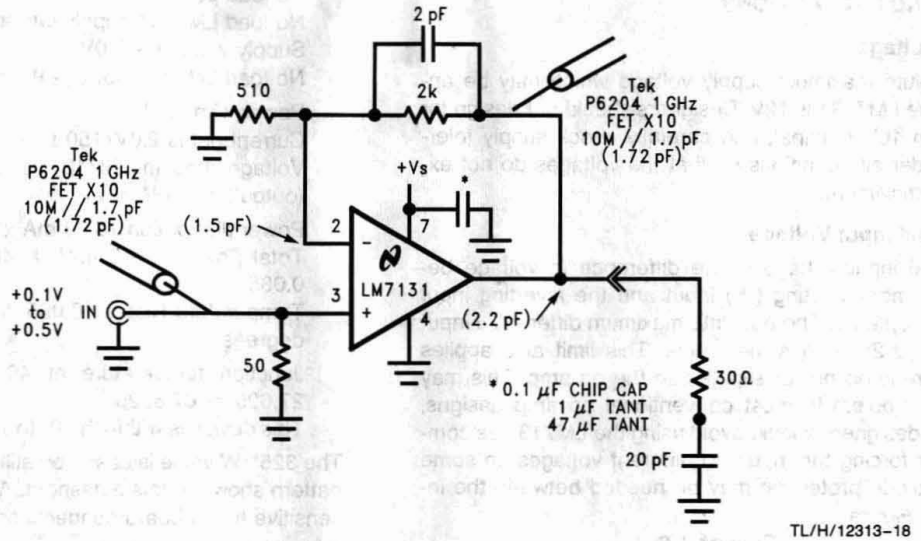
FIGURE 8. Flash A/D $A_V = +2$



Numbers in parentheses are measured fixture capacitances w/o DUT and load.

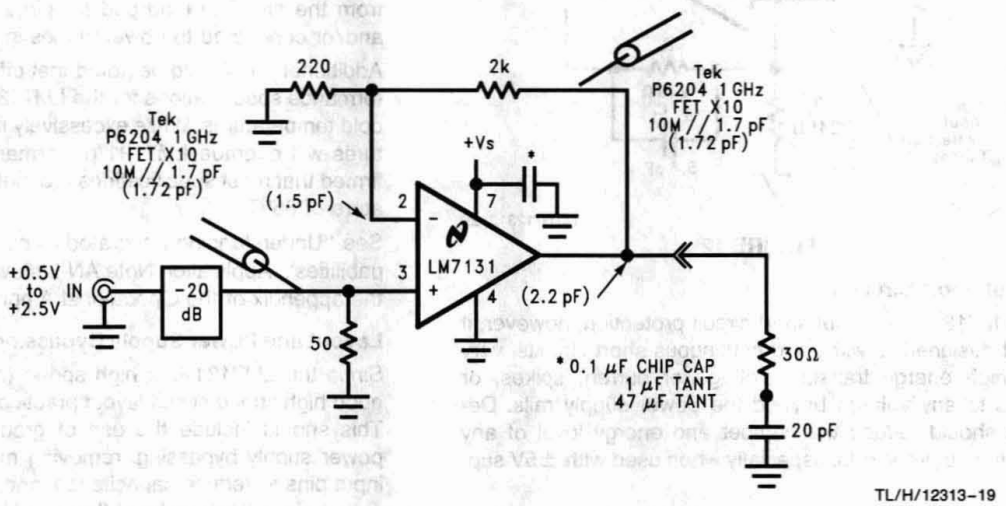
FIGURE 9. Flash A/D $A_V = +5$

Application Information (Continued)



Numbers in parentheses are measured fixture capacitances w/o DUT and load.

FIGURE 10. Flash A/D $A_V = +5$ with Feedback Capacitor



Numbers in parentheses are measured fixture capacitances w/o DUT and load.

FIGURE 11. Flash A/D $A_V = +10$

Using the LM7131

LIMITS AND PRECAUTIONS

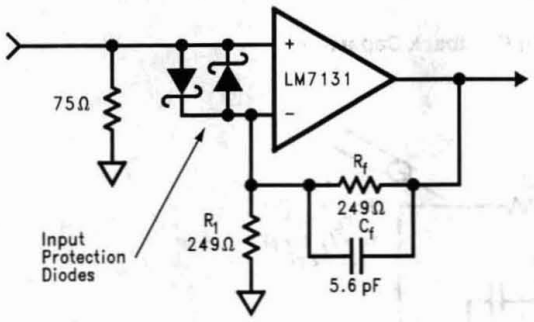
Supply Voltage

The absolute maximum supply voltage which may be applied to the LM7131 is 12V. Designers should not design for more than 10V nominal, and carefully check supply tolerances under all conditions so that the voltages do not exceed the maximum.

Differential Input Voltage

Differential input voltage is the difference in voltage between the non-inverting (+) input and the inverting input (−) of the op amp. The absolute maximum differential input voltage is ±2V across the inputs. This limit also applies when there is no power supplied to the op amp. This may not be a problem in most conventional op amp designs, however, designers should avoid using the LM7131 as comparator or forcing the inputs to different voltages. In some designs, diode protection may be needed between the inputs. See *Figure 12*.

Gain of +2



TL/H/12313–20

FIGURE 12

Output Short Circuits

The LM7131 has output short circuit protection, however, it is not designed to withstand continuous short circuits, very fast high energy transient voltage or current spikes, or shorts to any voltage beyond the power supply rails. Designs should reduce the number and energy level of any possible output shorts, especially when used with ±5V supplies.

A resistor in series with the output, such as the 75Ω resistor used to back terminate 75Ω cables, will reduce the effects of shorts. For outputs which will send signals off the PC board additional protection devices, such as diodes to the power rails, zener-type surge suppressors, and varistors may be useful.

Thermal Management

Note that the SOT23-5 (Tiny) package has less power dissipation capability (325°/W) than the S0-8 and DIP packages (115°/W). This may cause overheating with ±5 supplies and heavy loads at high ambient temps. This is less of a problem when using +5V single supplies.

Example:
Driving a 150Ω load to 2.0V at a 40°C (104 °F) ambient temperature. (This is common external maximum temperature for office environments. Temperatures inside equipment may be higher.)

No load power-
No load LM7131 supply current - 9.0 mA
Supply voltage is 5.0V
No load LM7131 power - 9.0 mA x 5.0V = 45 mW

Power with load-
Current out is 2.0V/150 Ω = 13.33 mA
Voltage drop in LM7131 is 5.0V (supply) − 2.0V (output) = 3.0V

Power dissipation 13.33 mA x 3.0V = 40 mW
Total Power = 45 mW + 40 mW = 85 mW = 0.085
Temperature Rise = 0.085 W x 325°/W = 27.625 degrees

Junction temperature at 40° ambient = 40 + 27.625 = 67.6225°.
This device is within the 0° to 70° specification limits.

The 325°/W value is based on still air and the pc board land pattern shown in this datasheet. Actual power dissipation is sensitive to PC board connections and airflow.

SOT23-5 power dissipation may be increased by airflow or by increasing the metal connected to the pads, especially the center pin (pin number 2, V−) on the left side of the SOT23-5. This pin forms the mounting paddle for the die inside the SOT23-5, and can be used to conduct heat away from the die. The land pad for pin 2 can be made larger and/or connected to power planes in a multilayer board.

Additionally, it should be noted that difficulty in meeting performance specifications for the LM7131 is most common at cold temperatures. While excessively high junction temperatures will degrade LM7131 performance, testing has confirmed that most specifications are met at a junction temperature of 85°C.

See "Understanding Integrated Circuit Package Power Capabilities", Application Note AN-336, which may be found in the appendix of the Operational Amplifier Databook.

Layout and Power Supply Bypassing

Since the LM7131 is a high speed (over 50 MHz) device, good high speed circuit layout practices should be followed. This should include the use of ground planes, adequate power supply bypassing, removing metal from around the input pins to reduce capacitance, and careful routing of the output signal lines to keep them away from the input pins.

The power supply pins should be bypassed on both the negative and positive supply inputs with capacitors placed close to the pins. Surface mount capacitors should be used for best performance, and should be placed as close to the pins as possible. It is generally advisable to use two capacitors at each supply voltage pin. A small surface mount capacitor with a value of around 0.01 microfarad (10 nF), usually a ceramic type with good RF performance, should be placed closest to the pin. A larger capacitor, in usually in the range of 1.0 μF to 4.7 μF, should also be placed near the pin. The larger capacitor should be a device with good RF characteristics and low ESR (equivalent series resistance) for best results. Ceramic and tantalum capacitors generally work well as the larger capacitor.

For single supply operation, if continuous low impedance ground planes are available, it may be possible to use bypass capacitors between the +5V supply and ground only, and reduce or eliminate the bypass capacitors on the V− pin.

Using the LM7131 (Continued)

Capacitive Load Driving

The phase margin of the LM7131 is reduced by driving large capacitive loads. This can result in ringing and slower settling of pulse signals. This ringing can be reduced by placing a small value resistor (typically in the range of 22Ω–100Ω) between the LM7131 output and the load. This resistor should be placed as close as practical to the LM7131 output. When driving cables, a resistor with the same value as the characteristic impedance of the cable may be used to isolate the cable capacitance from the output. This resistor will reduce reflections on the cable.

Input Current

The LM7131 has typical input bias currents in the 15 μA to 25 μA range. This will not present a problem with the low input impedances frequently used in high frequency and video circuits. For a typical 75Ω input termination, 20 μA of input current will produce a voltage across the termination resistor of only 1.5 mV. An input impedance of 10 kΩ, however, would produce a voltage of 200 mV, which may be large compared to the signal of interest. Using lower input impedances is recommended to reduce this error source.

Feedback Resistor Values and Feedback Compensation

Using large values of feedback resistances (roughly 2k) with low gains (such gains of 2) will result in degraded pulse response and ringing. The large resistance will form a pole with the input capacitance of the inverting input, delaying feedback to the amplifier. This will produce overshoot and ringing. To avoid this, the gain setting resistors should be scaled to lower values (below 1k) At higher gains (> 5) larger values of feedback resistors can be used.

Overshoot and ringing of the LM7131 can be reduced by adding a small compensation capacitor across the feed back resistor. For the LM7131 values in pF to tens of pF range are useful initial values. Too large a value will reduce the circuit bandwidth and degrade pulse response.

Since the small stray capacitance from the circuit layout, other components, and specific circuit bandwidth requirements will vary, it is often useful to select final values based on prototypes which are similar in layout to the production circuit boards.

Reflections

The output slew rate of the LM7131 is fast enough to produce reflected signals in many cables and long circuit traces. For best pulse performance, it may be necessary to terminate cables and long circuit traces with their characteristic impedance to reduce reflected signals.

Reflections should not be confused with overshoot. Reflections will depend on cable length, while overshoot will depend on load and feedback resistance and capacitance. When determining the type of problem, often removing or drastically shortening the cable will reduce or eliminate reflections. Overshoot can exist without a cable attached to the op amp output.

Driving Flash A/D Converters (Video Converters)

The LM7131 has been optimized to drive flash analog to digital converters in a +5V only system. Different flash A/D converters have different voltage input ranges. The LM7131 has enough gain-bandwidth product to amplify standard video level signals to voltages which match the optimum input range of many types of A/D converters.

For example, the popular 1175 type 8-bit flash A/D converter has a preferred input range from 0.6V to 2.6V. If the input signal has an active video range (excluding sync levels) of approximately 700 mV, a circuit like the one in *Figure 13* can be used to amplify and drive an A/D. The 10 μF capacitor blocks the DC components, and allows the + input of the LM7131 to be biased through R clamp so that the minimum output is equal to V_{RB} of the A/D converter. The gain of the circuit is determined as follows:

Output Signal Range = 2.6V (V top) = 0.6V (V bottom) = 2.0V

Gain = Output Signal Range/Input Signal = 2.857 = 2.00/0.700

Gain = $(R_f/R_1) + 1$ = (249Ω/133Ω) +1

R isolation and C_f will be determined by the designer based on the A/D input capacitance and the desired pulse response of the system. The nominal values of 33Ω and 5.6 pF shown in the schematic may be a useful starting point, however, signal levels, A/D converters, and system performance requirements will require modification of these values.

The isolation resistor, R isolation should be placed close to the output of the LM7131, which should be close to the A/D input for best results.

R clamp is connected to a voltage level which will result in the bottom of the video signal matching the Vrb level of the A/D converter. This level will need to be set by clamping the black level of the video signal. The clamp voltage will depend on the level and polarity of the video signal. Detecting the sync signal can be done by a circuit such as the LM1881 Video Sync Separator.

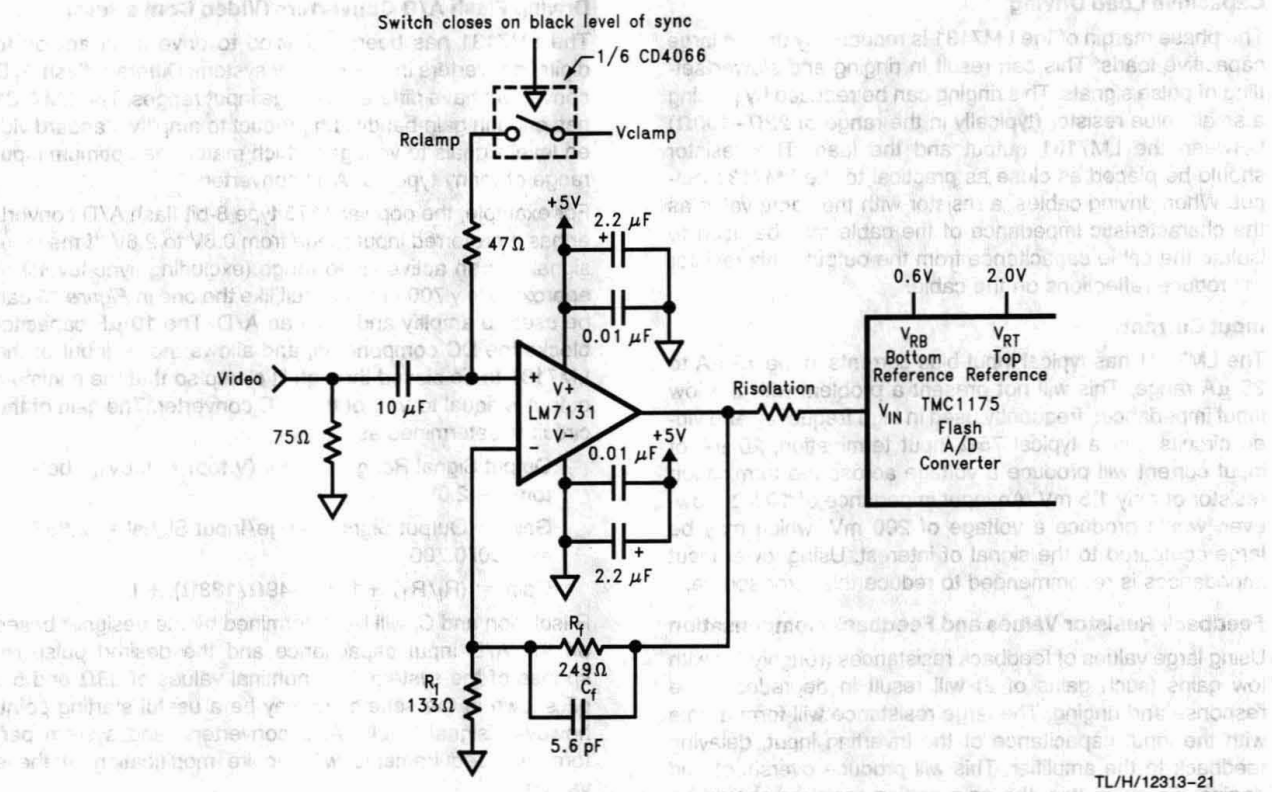
Important Note: This is an illustration of a conceptual use of the LM7131, not a complete design. The circuit designer will need to modify this for input protection, sync, and possibly some type of gain control for varying signal levels.

Some A/D converters have wide input ranges where the lower reference level can be adjusted. With these converters, best distortion results are obtained if the lower end of the output range is about 250 mV or more above the V− input of the LM7131 more. The upper limit can be as high as 4.0V with good results.

Driving the ADC12062 +5V 12-BIT A/D Converter

Figure 14 shows the LM7131 driving a National ADC12062 12 bit analog to digital converter. Both devices can be powered from a single +5V supply, lowering system complexity and cost. With the lowest signal voltage limited to 300 mV and a 3.8V peak-to-peak 100 KHz signal, bench tests have shown distortion less than −75 db, signal to noise ratios greater than 66 db, and SINAD (signal to noise + distortion) values greater than 65 db. For information on the latest single supply analog-to-digital converters, please contact your National Semiconductor representative.

Using the LM7131 (Continued)



TL/H/12313–21

FIGURE 13

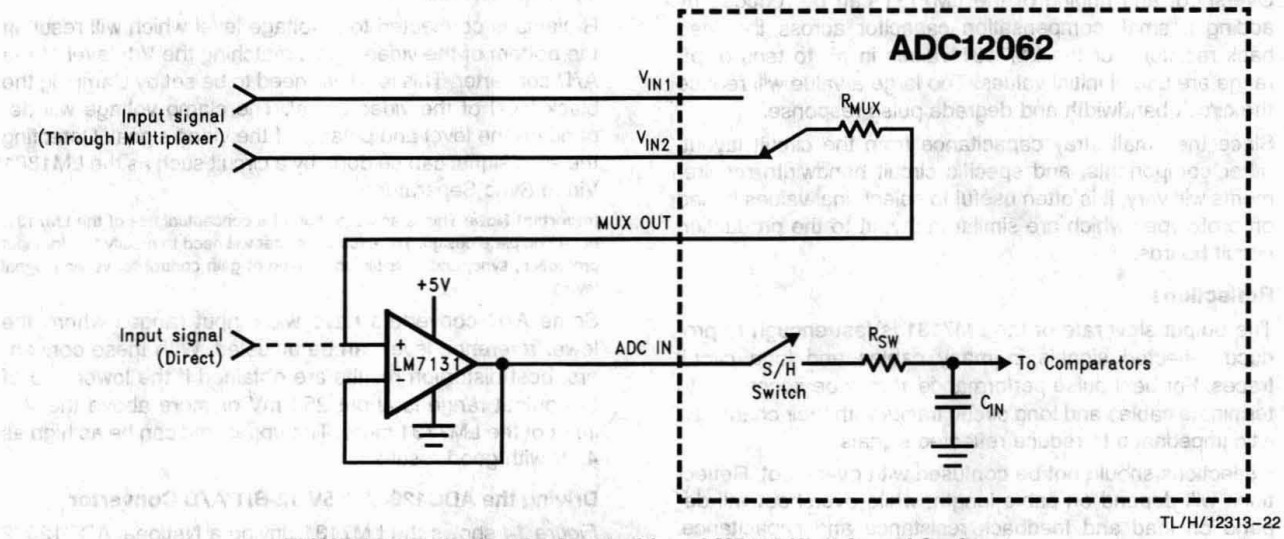


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FIGURE 14. Buffering the Input with an LM7131 High Speed Op Amp

Using the LM7131 (Continued)

CCD Amplifiers

The LM7131 has enough gain bandwidth to amplify low level signals from a CCD or similar image sensor and drive a flash analog-to-digital converter with one amplifier stage.

Signals from CCDs, which are used in scanners, copiers, and digital cameras, often have an output signal in the 100 mV–300 mV range. See *Figure 15* for a conceptual diagram. With a gain of 6 the output to the flash analog-to-digital converter is 1.8V, matching 90% of the converter's 2V input range. With a −3db bandwidth of 70 MHz for a gain of +1, the bandwidth at a gain of 6 will be 11.6 MHz. This 11.6 MHz bandwidth will result in a time constant of about 13.6 ns. This will allow the output to settle to 7 bits of accuracy within 4.9 time constants, or about 66 ns. Slewing time for a 1.8V step will be about 12 ns. The total slewing and settling time will be about 78 ns of the 150 ns pixel valid time. This will leave about 72 ns total for the flash converter signal acquisition time and tolerance for timing signals.

For scanners and copiers with moving scan bars, the SOT23-5 package is small enough to be placed next to the light sensor. The LM7131 can drive a cable to the main electronics section from the scan bar. This can reduce noise pickup by amplifying the signal before sending on the cable.

A/D Reference Drivers

The LM7131's output and drive capability make it a good choice for driving analog-to-digital references which have suddenly changing loads. The small size of the SOT23-5 package allow the LM7131 to be placed very close to the A/D reference pin, maximizing response. The small size avoids the penalty of increased board space. Often the SOT23-5 package is small enough that it can fit in space used by the large capacitors previously attached to the A/D reference. By acting as a buffer for a reference voltage, noise pickup can be reduced and the accuracy may be increased.

For additional space savings, the LM4040 precision voltage reference is available in a tiny SOT23-3 package.

Video Gain of +2

The design of the LM7131 has been optimized for gain of +2 video applications. Typical values for differential gain and phase are 0.25% differential gain and 0.75 degree differential phase. See *Figure 12*.

Improving Video Performance

Differential gain and phase performance can be improved by keeping the active video portion of the signal above 300 mV. The sync signal can go below 300 mV without affecting the video quality. If it is possible to AC couple the signal and shift the output voltage slightly higher, much better video performance is possible. For a +5V single supply, an output range between 2.0V and 3.0V can have a differential gain of 0.07% and differential phase of 0.3 degree when driving a 150Ω load. For a +3V single supply, the output should be between 1.0V and 2.0V.

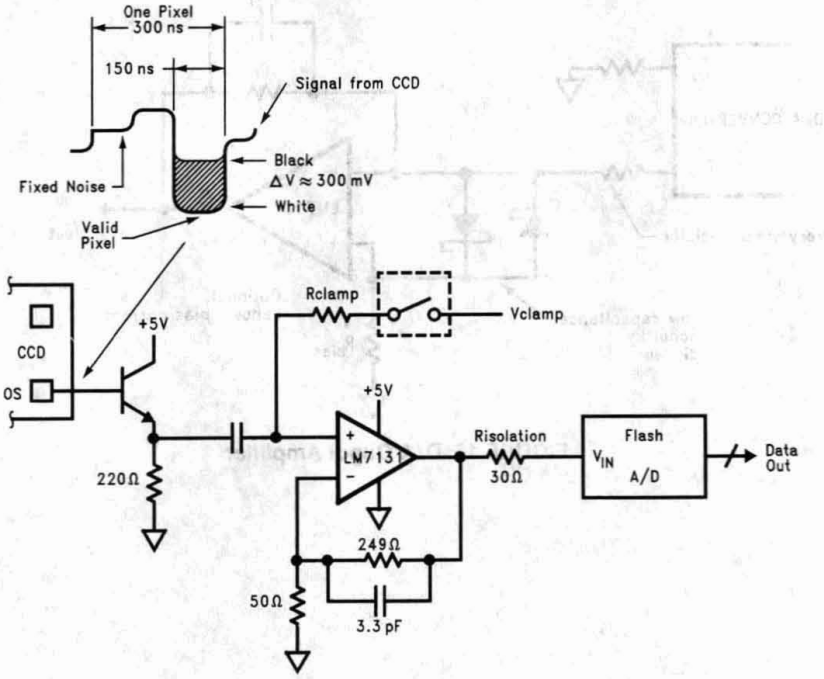
Cable Driving with +5V Supplies

The LM7131 can easily drive a back-terminated 75Ω video cable (150Ω load) when powered by a +5V supply. See *Figures 2*, *3* and *4*. This makes it a good choice for video output for portable equipment, personal digital devices, and desktop video applications.

The LM7131 can also supply +2.00V to a 50Ω load to ground, making it useful as driver in 50Ω systems such as portable test equipment.

Cable Driving with +3V Supplies

The LM7131 can drive 150Ω to 2.00V when supplied by a 3V supply. This 3V performance means that the LM7131 is useful in battery powered video applications, such as camcorders, portable video mixers, still video cameras, and portable scanners.



TL/H/12313–23

FIGURE 15. CCD Amplifier

Using the LM7131 (Continued)

Audio and High Frequency Signal Processing

The LM7131 is useful for high fidelity audio and signal processing. A typical LM7131 is capable of driving 2V across 150Ω (referenced to ground) at less than 0.1% distortion at 4 MHz when powered by a single 5V supply.

Use with 2.5V Virtual Ground Systems with +5V Single Supply Power

Many analog systems which must work on a single +5V supply use a 'virtual ground' - a reference voltage for the signal processing which is usually between +5V and 0V. This virtual ground is usually halfway between the top and bottom supply rails. This is usually +2.5V for +5V systems and +1.5V for +3V systems.

The LM7131 can be used in single supply/virtual ground systems driving loads referenced to 2.5V. The output swing specifications in the data sheet show the tested voltage limits for driving a 150Ω load to a virtual ground supply for +3V and +5V. A look at the output swing specifications shows that for heavy loads like 150 ohms, the output will swing as close as one diode drop (roughly, 0.7V) to the supply rail. This leaves a relatively wide range for +5V systems and a somewhat narrow range for +3V systems. One way to increase this output range is to have the output load referenced to ground—this will allow the output to swing lower. Another is to use higher load impedances. The output swing specifications show typical numbers for swing with loads of 600Ω to ground. Note that these typical numbers are similar to those for a 150Ω load. These typical numbers are an indication of the maximum DC performance of the LM7131.

The sinking output of the LM7131 is somewhat lower than the amplifier's sourcing capability. This means that the LM7131 will not drive as much current into a load tied to 2.5 V as it will drive into a load tied to 0V.

Good AC performance will require keeping the output further away from the supply rails. For a +5V supply and relatively high impedance load (analog-to-digital converter input) the following are suggested as an initial starting range for achieving high (> 60 dB) AC accuracy

Upper output level—
Approximately 0.8V to 1V below the positive (V+) rail.
Lower output level—
Approximately 200 mV–300 mV above the negative rail.

The LM7131 very useful in virtual ground systems as an output device for output loads which are referenced to 0V or the lower rail. It is also useful as a driver for capacitive loads, such as sample and hold circuits, and audio analog to digital converters. If fast amplifiers with rail-to-rail output ranges are needed, please see the National Semiconductor LM6142 datasheet.

D/A Output Amplifier

The LM7131 can be used as an output amplifier for fast digital-to-analog converters. When using the LM7131 with converters with an output voltage range which may exceed the differential input voltage limit of ±2V, it may be necessary to add protection diodes to the inputs. See *Figure 16*. For high speed applications, it may be useful to consider low capacitance schottky diodes. Additional feedback capacitance may be needed to control ringing due to the additional input capacitance from the D/A and protection diodes. When used with current output D/As, the input bias currents may produce a DC offset in the output. This offset may be canceled by a resistor between the positive input and ground.

Spice Macromodel

A SPICE macromodel of the LM7131 and many other National Semiconductor op amps is available at no charge from your National Semiconductor representative.

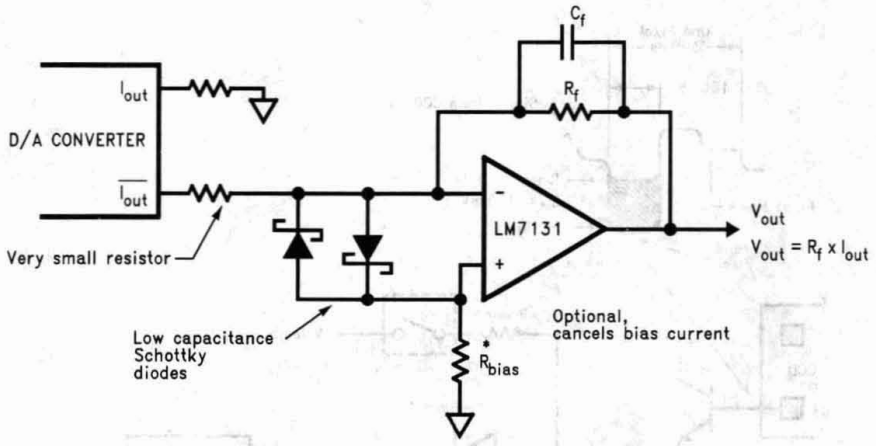


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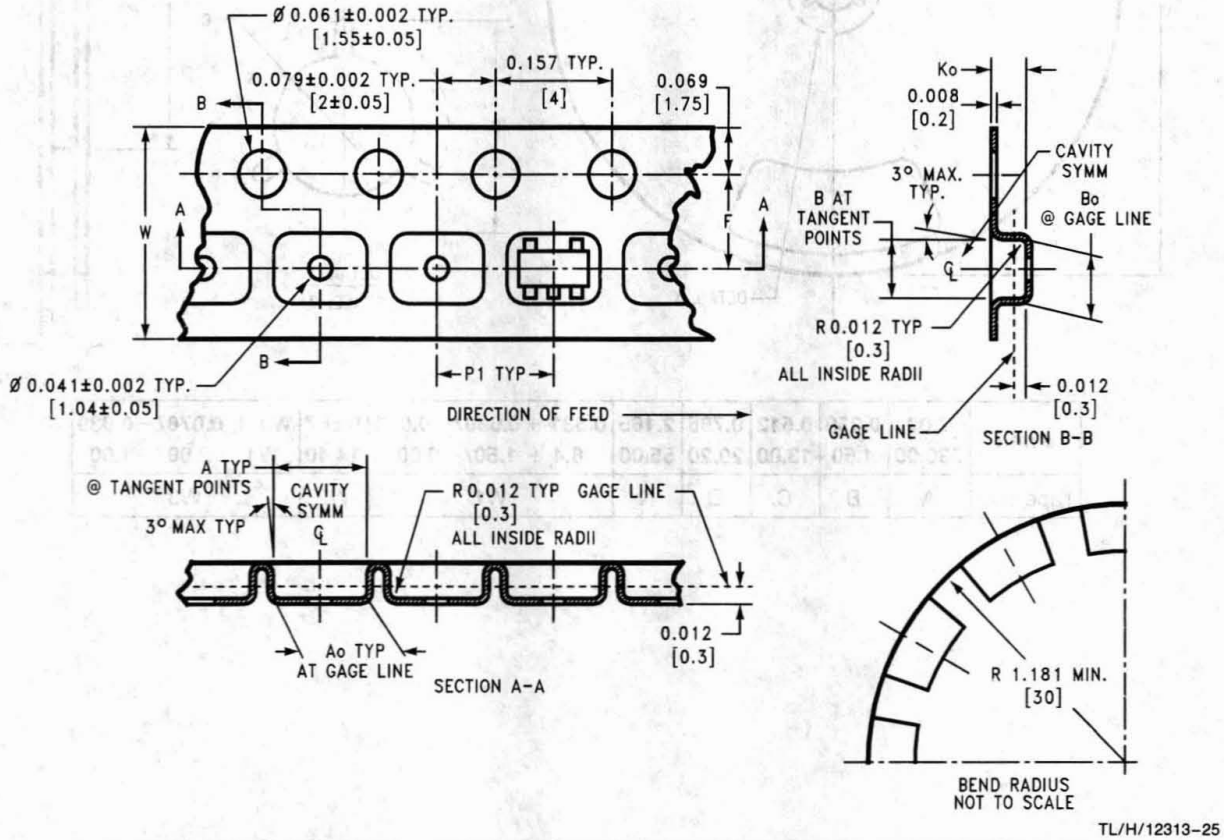
FIGURE 16. D/A Ouput Amplifier

SOT-23-5 Tape and Reel Specification

TAPE FORMAT

Tape Section	# Cavaties	Cavity Status	Cover Tape Status
Leader (Start End)	0 (min)	Empty	Sealed
	75 (min)	Empty	Sealed
Carrier	3000	Filled	Sealed
	250	Filled	Sealed
Trailer (Hub End)	125 (min)	Empty	Sealed
	0 (min)	Empty	Sealed

TAPE DIMENSIONS



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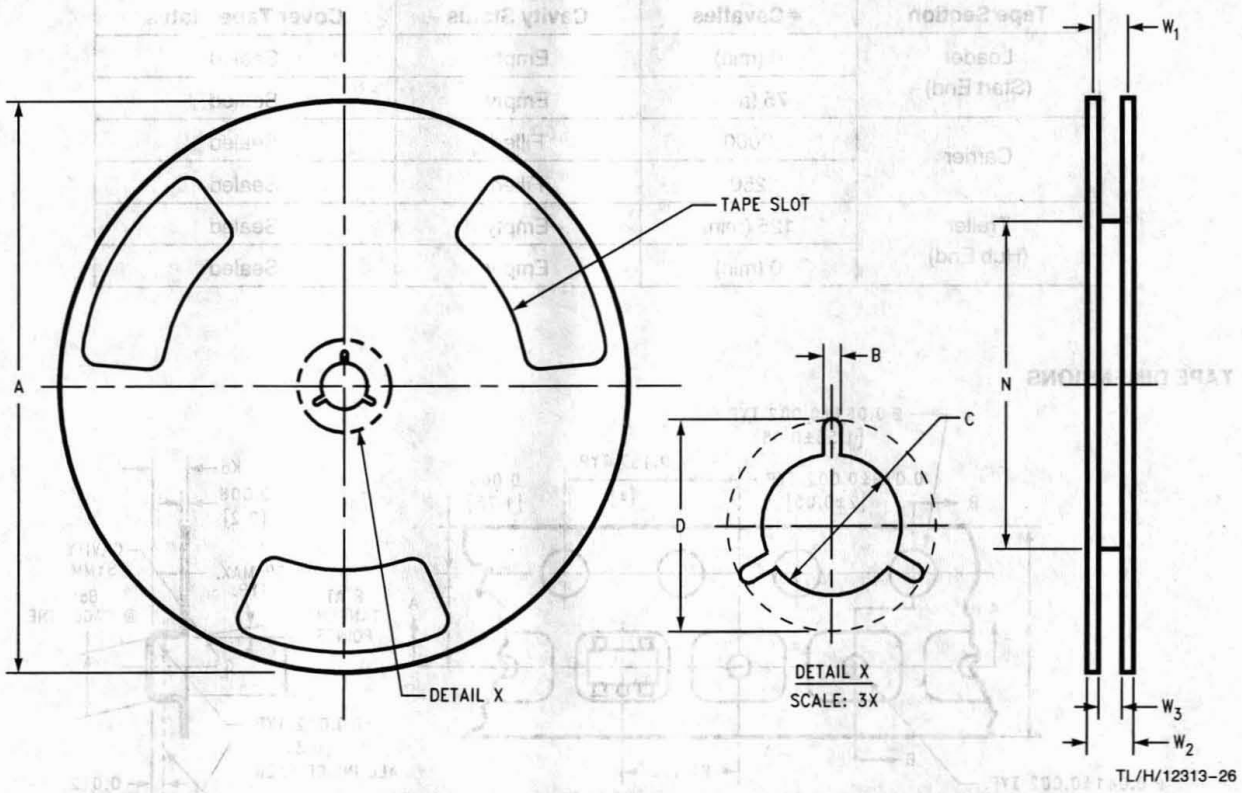
8 mm	0.130 (3.3)	0.124 (3.15)	0.130 (3.3)	0.126 (3.2)	0.138 ±0.002 (3.5 ±0.05)	0.055 ±0.004 (1.4 ±0.11)	0.157 (4)	0.315 ±0.012 (8 ±0.3)
Tape Size	DIM A	DIM Ao	DIM B	DIM Bo	DIM F	DIM Ko	DIM P1	DIM W

SOT-23-5 Tape and Reel Specification (Continued)

REEL DIMENSIONS



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8 mm	7.00 330.00	0.059 1.50	0.512 13.00	0.795 20.20	2.165 55.00	0.331 +0.059/−0.000 8.4 + 1.50/−0.00	0.567 14.40	W1 + 0.078/−0.039 W1 + 2.00/−1.00
Tape Size	A	B	C	D	N	W1	W2	W3

National Semiconductor

ADVANCE INFORMATION

LM7171 Very High Speed High Output Current Voltage Feedback Amplifier

General Description

The LM7171 is a voltage feedback amplifier optimally designed for $A_V > 1$ operation. It provides a very high slew rate at 4100V/μs and a wide gain-bandwidth product bandwidth of 200 MHz while consuming only 6.5 mA of supply current. It is ideal for video and high speed signal processing applications such as ultrasound and pulse amplifiers. With 100 mA output current, the LM7171 can be used for video distribution, transformer driver and laser diode driver.

The ±15V power supplies allow for large signal swings and give greater dynamic range and signal-to-noise ratio. The LM7171 offers low SFDR and THD, ideal for ADC/DAC systems. In addition, the LM7171 is specified for ±5V operation for portable applications.

The LM7171 is built on Nationals advanced VIP™ III (Vertically integrated PNP) complementary bipolar process.

Features (Typical Unless Otherwise Noted)

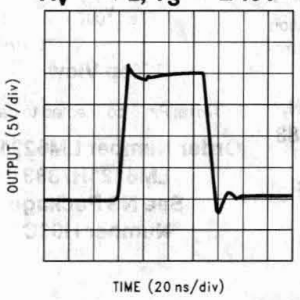
- Easy-To-Use Voltage Feedback Topology
- Very High Slew Rate 4100V/μs
- Wide Gain-Bandwidth Product 200 MHz
- −3 dB Frequency @ $A_V = +2$ 220 MHz
- Low Supply Current 6.5 mA
- High Open Loop Gain 85 dB
- High Output Current 100 mA
- Differential Gain and Phase 0.01%, 0.02°
- Specified for ±15V and ±5V Operation

Applications

- HDSL and ADSL Drivers
- Multimedia Broadcast Systems
- Professional Video Cameras
- Video Amplifiers
- Copiers/Scanners/Fax
- HDTV Amplifiers
- Pulse Amplifiers and Peak Detectors
- CATV/Fiber Optics Signal Processing

Typical Performance

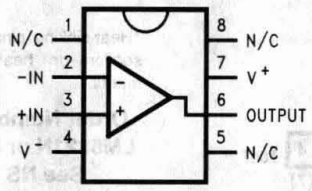
Large Signal Pulse Response
$A_V = +2$, $V_S = \pm 15V$



TL/H/12351–7

Connection Diagrams

8-Pin DIP/SO



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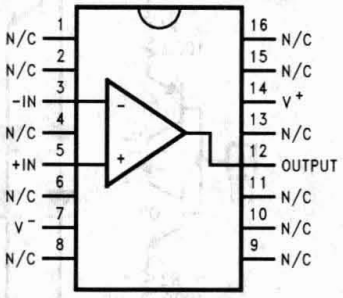
Top View

16-Pin Wide Body SO



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Top View

Ordering Information

Package	Temperature Range		Transport Media	NSC Drawing
	Industrial −40°C to +85°C	Military −55°C to +125°C		
8-Pin DIP	LM7171AIN, LM7171BIN		Rails	N08E
8-Pin CDIP		5962-9553601QPA*	Rails	J08A
8-Pin Small Outline	LM7171AIM, LM7171BIM		Rails	M08A
	LM7171AIMX, LM7171BIMX		Tape and Reel	
16-Pin Small Outline	LM7171AIWM, LM7171BIWM		Rails	M16B
	LM7171AWMX, LM7171BWMX		Tape and Reel	

*For the military temperature grade, please refer to the Military Datasheet: MNLM7171AMJ/883

2

National Semiconductor

LM6121/LM6221/LM6321 High Speed Buffer

General Description

These high speed unity gain buffers slew at 800 V/μs and have a small signal bandwidth of 50 MHz while driving a 50Ω load. They can drive ±300 mA peak and do not oscillate while driving large capacitive loads. The LM6121 family are monolithic ICs which offer performance similar to the LH0002 with the additional features of current limit and thermal shutdown.

These buffers are built with National's VIP™ (Vertically Integrated PNP) process which provides fast PNP transistors that are true complements to the already fast NPN devices. This advanced junction-isolated process delivers high speed performance without the need for complex and expensive dielectric isolation.

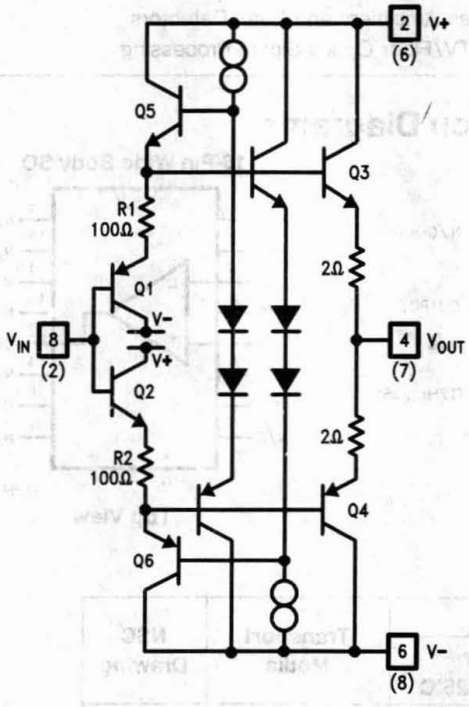
Features

- High slew rate — 800 V/μs
- Wide bandwidth — 50 MHz
- Slew rate and bandwidth 100% tested
- Peak output current — ±300 mA
- High input impedance — 5 MΩ
- LH0002H pin compatible
- No oscillations with capacitive loads
- 5V to ±15V operation guaranteed
- Current and thermal limiting
- Fully specified to drive 50Ω lines

Applications

- Line Driving
- Radar
- Sonar

Simplified Schematic



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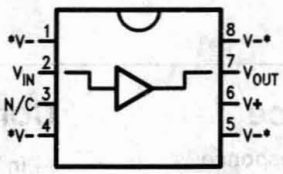
Numbers in ( ) are for 8-pin N DIP.

Connection Diagrams

Plastic DIP



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*Heat-sinking pins. See Application section on heat sinking requirements.

Order Number LM6221N, LM6321N or LM6121J/883
See NS Package Number J08A or N08E

Metal Can

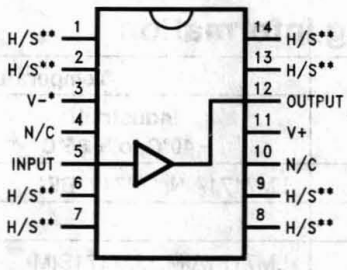
TL/H/9223–3

Top View

Note: Pin 6 connected to case.

Order Number LM6221H or LM6121H/883
See NS Package Number H08C

Plastic SO



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*Pin 3 must be connected to the negative supply.

**Heat-sinking pins. See Application section on heat-sinking requirements. These pins are at V^- potential.

Order Number LM6321M
See NS Package Number M14A

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	36V (±18)
Input to Output Voltage (Note 2)	±7V
Input Voltage	±Vsupply
Output Short-Circuit to GND (Note 3)	Continuous
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	260°C
Power Dissipation	(Note 10)
ESD Tolerance (Note 8)	±2000V
Junction Temperature ($T_{J(max)}$)	150°C

Operating Ratings

Operating Temperature Range	
LM6121H/883	−55°C to +125°C
LM6221	−40°C to +85°C
LM6321	0°C to +70°C
Operating Supply Range	4.75 to ±16V
Thermal Resistance (θ_{JA}), (Note 4)	
H Package	150°C/W
N Package	47°C/W
M Package	69°C/W
Thermal Resistance (θ_{JC}), H Package	17°C/W

DC Electrical Characteristics

The following specifications apply for Supply Voltage = ±15V, V_{CM} = 0, $R_L \geq 100\ k\Omega$ and $R_S = 50\Omega$ unless otherwise noted. **Boldface** limits apply for $T_A = T_J = T_{MIN}$ to T_{MAX}; all other limits $T_A = T_J = 25°C$.

Symbol	Parameter	Conditions	Typ	LM6121 Limit (Notes 5, 9)	LM6221 Limit (Note 5)	LM6321 Limit (Note 5)	Units
A_{V1}	Voltage Gain 1	$R_L = 1\ k\Omega$, $V_{IN} = \pm 10V$	0.990	0.980 **0.970**	0.980 **0.950**	0.970 **0.950**	V/V Min
A_{V2}	Voltage Gain 2	$R_L = 50\Omega$, $V_{IN} = \pm 10V$	0.900	0.860 **0.800**	0.860 **0.820**	0.850 **0.820**	
A_{V3}	Voltage Gain 3 (Note 6)	$R_L = 50\Omega$, $V^+ = 5V$ $V_{IN} = 2\ V_{pp}$ **(1.5 V_{pp})**	0.840	0.780 **0.750**	0.780 **0.700**	0.750 **0.700**	
V_{OS}	Offset Voltage	$R_L = 1\ k\Omega$	15	30 **50**	30 **60**	50 **100**	mV Max
I_B	Input Bias Current	$R_L = 1\ k\Omega$, $R_S = 10\ k\Omega$	1	4 **7**	4 **7**	5 **7**	μA Max
R_{IN}	Input Resistance	$R_L = 50\Omega$	5				MΩ
C_{IN}	Input Capacitance		3.5				pF
R_O	Output Resistance	$I_{OUT} = \pm 10\ mA$	3	5 **10**	5 **10**	5 **6**	Ω Max
I_{S1}	Supply Current 1	$R_L = \infty$	15	18 **20**	18 **20**	20 **22**	mA Max
I_{S2}	Supply Current 2	$R_L = \infty$, $V^+ = 5V$	14	16 **18**	16 **18**	18 **20**	
V_{O1}	Output Swing 1	$R_L = 1k$	13.5	13.3 **13**	13.3 **13**	13.2 **13**	±V Min
V_{O2}	Output Swing 2	$R_L = 100\Omega$	12.7	11.5 **10**	11.5 **10**	11 **10**	
V_{O3}	Output Swing 3	$R_L = 50\Omega$	12	11 **9**	11 **9**	10 **9**	
V_{O4}	Output Swing 4	$R_L = 50\Omega$, $V^+ = 5V$ (Note 6)	1.8	1.6 **1.3**	1.6 **1.4**	1.6 **1.5**	V_{PP} Min
PSSR	Power Supply Rejection Ratio	$V^{\pm} = \pm 5V$ to ±15V	70	60 **55**	60 **50**	60 **50**	dB Min

AC Electrical Characteristics

The following specifications apply for Supply Voltage = ±15V, V_{CM} = 0, $R_L \geq 100\ k\Omega$ and $R_S = 50\Omega$ unless otherwise noted. **Boldface** limits apply for $T_A = T_J = T_{MIN}$ to T_{MAX}; all other limits $T_A = T_J = 25°C$.

Symbol	Parameter	Conditions	Typ	LM6121 Limit (Note 5)	LM6221 Limit (Note 5)	LM6321 Limit (Note 5)	Units
SR_1	Slew Rate 1	$V_{IN} = \pm 11V$, $R_L = 1\ k\Omega$	1200	550	550	550	V/μs Min
SR_2	Slew Rate 2	$V_{IN} = \pm 11V$, $R_L = 50\Omega$ (Note 7)	800	550	550	550	
SR_3	Slew Rate 3	$V_{IN} = 2\ V_{PP}$, $R_L = 50\Omega$ $V^+ = 5V$ (Note 6)	50	550	550	550	
BW	−3 dB Bandwidth	$V_{IN} = \pm 100\ mV_{PP}$, $R_L = 50\Omega$ $C_L \leq 10\ pF$	50	30	30	30	MHz Min
t_r, t_f	Rise Time Fall Time	$R_L = 50\Omega$, $C_L \leq 10\ pF$ $V_O = 100\ mV_{PP}$	7.0				ns
t_{pd}	Propagation Delay Time	$R_L = 50\Omega$, $C_L \leq 10\ pF$ $V_O = 100\ mV_{PP}$	4.0				ns
O_S	Overshoot	$R_L = 50\Omega$, $C_L \leq 10\ pF$ $V_O = 100\ mV_{PP}$	10				%

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications do not apply when operating the device beyond its rated operating conditions.

Note 2: During current limit or thermal limit, the input current will increase if the input to output differential voltage exceeds 8V. For input to output differential voltages in excess of 8V the input current should be limited to ±20 mA.

Note 3: The LM6121 series buffers contain current limit and thermal shutdown to protect against fault conditions.

Note 4: The thermal resistance θ_{JA} of the device in the N package is measured when soldered directly to a printed circuit board, and the heat-sinking pins (pins 1, 4, 5 and 8) are connected to 2 square inches of 2 oz. copper. When installed in a socket, the thermal resistance θ_{JA} of the N package is 84°C/W. The thermal resistance θ_{JA} of the device in the M package is measured when soldered directly to a printed circuit board, and the heat-sinking pins (pins 1, 2, 6, 7, 8, 9, 13, 14) are connected to 1 square inch of 2 oz. copper.

Note 5: Limits are guaranteed by testing or correlation.

Note 6: The input is biased to 2.5V and V_{IN} swings V_{pp} about this value. The input swing is 2 V_{pp} at all temperatures except for the A_V3 test at −55°C where it is reduced to 1.5 V_{pp}.

Note 7: Slew rate is measured with a ±11V input pulse and 50Ω source impedance at 25°C. Since voltage gain is typically 0.9 driving a 50Ω load, the output swing will be approximately ±10V. Slew rate is calculated for transitions between ±5V levels on both rising and falling edges. A high speed measurement is done to minimize device heating. For slew rate versus junction temperature see typical performance curves. The input pulse amplitude should be reduced to ±10V for measurements at temperature extremes. For accurate measurements, the input slew rate should be at least 1700 V/μs.

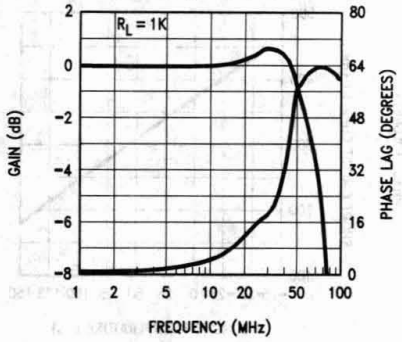
Note 8: The test circuit consists of the human body model of 120 pF in series with 1500Ω.

Note 9: For specification limits over the full Military Temperature Range, see RETS6121X.

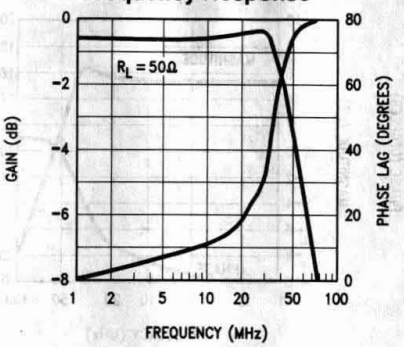
Note 10: The maximum power dissipation is a function of $T_{J(max)}$, θ_{JA}, and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(max)} - T_A)/\theta_{JA}$.

Typical Performance Characteristics T_J = 25°C, unless otherwise specified

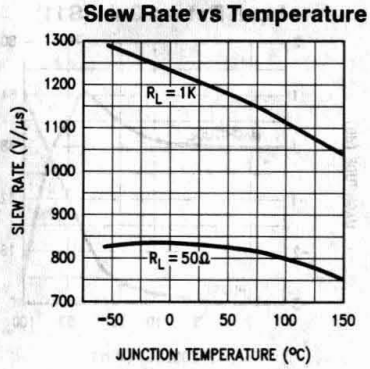
Frequency Response



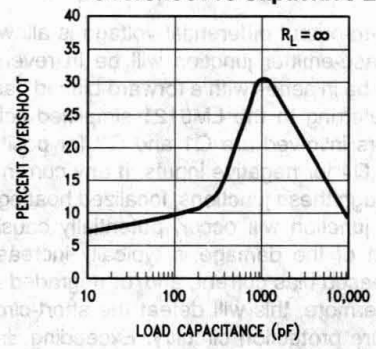
Frequency Response



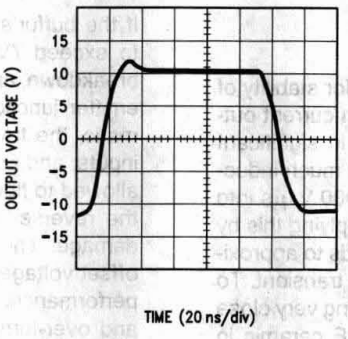
Slew Rate vs Temperature



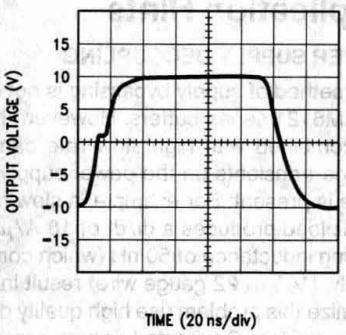
Overshoot vs Capacitive Load



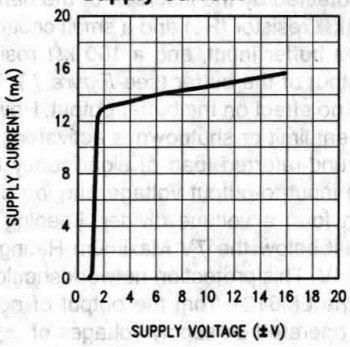
Large Signal Response
R_L = 1 kΩ



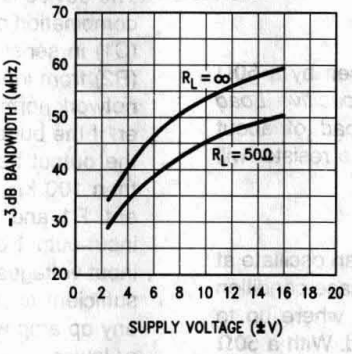
Large Signal Response
R_L = 50Ω



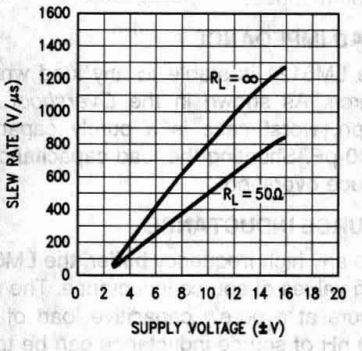
Supply Current



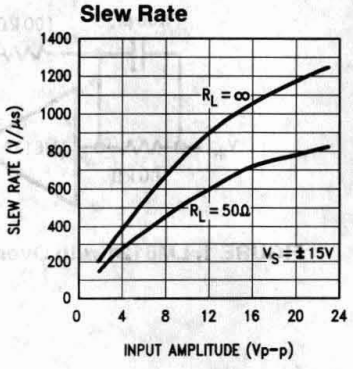
−3 dB Bandwidth



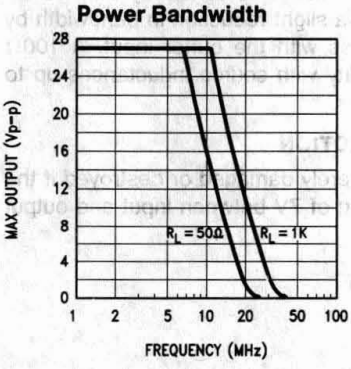
Slew Rate



Slew Rate



Power Bandwidth



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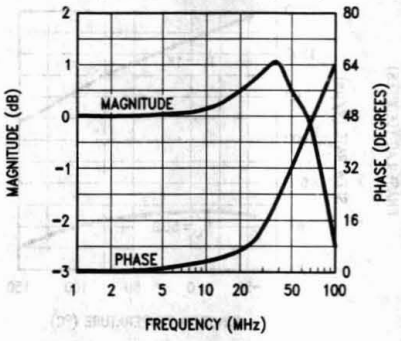
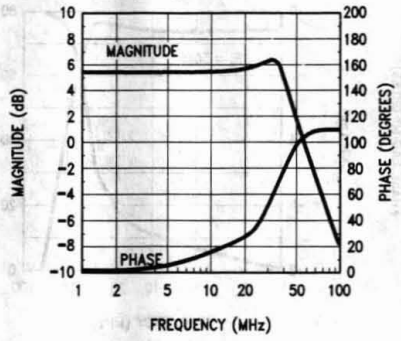
2

Typical Performance Characteristics T_J = 25°C, unless otherwise specified (Continued)

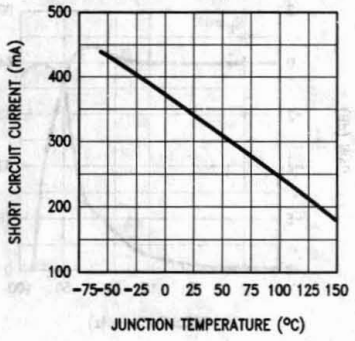
Input Return Gain (S11)



Forward Transmission Gain (S12)



Current Limit



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Application Hints

POWER SUPPLY DECOUPLING

The method of supply bypassing is not critical for stability of the LM6121 series buffers. However, their high current output combined with high slew rate can result in significant voltage transients on the power supply lines if much inductance is present. For example, a slew rate of 900 V/μs into a 50Ω load produces a di/dt of 18 A/μs. Multiplying this by a wiring inductance of 50 nH (which corresponds to approximately 1½" of 22 gauge wire) result in a 0.9V transient. To minimize this problem use high quality decoupling very close to the device. Suggested values are a 0.1 μF ceramic in parallel with one or two 2.2 μF tantalums. A ground plane is recommended.

LOAD IMPEDANCE

The LM6121 is stable to any load when driven by a 50Ω source. As shown in the *Overshoot vs Capacitive Load* graph, worst case is a purely capacitive load of about 1000 pF. Shunting the load capacitance with a resistor will reduce overshoot.

SOURCE INDUCTANCE

Like any high frequency buffer, the LM6121 can oscillate at high values of source inductance. The worst case condition occurs at a purely capacitive load of 50 pF where up to 100 nH of source inductance can be tolerated. With a 50Ω load, this goes up to 200 nH. This sensitivity may be reduced at the expense of a slight reduction in bandwidth by adding a resistor in series with the buffer input. A 100Ω resistor will ensure stability with source inductances up to 400 nH with any load.

OVERVOLTAGE PROTECTION

The LM6121 may be severely damaged or destroyed if the Absolute Maximum Rating of 7V between input and output pins is exceeded.

If the buffer's input-to-output differential voltage is allowed to exceed 7V, a base-emitter junction will be in reverse-breakdown, and will be in series with a forward-biased base-emitter junction. Referring to the LM6121 simplified schematic, the transistors involved are Q1 and Q3 for positive inputs, and Q2 and Q4 for negative inputs. If any current is allowed to flow through these junctions, localized heating of the reverse-biased junction will occur, potentially causing damage. The effect of the damage is typically increased offset voltage, increased bias current, and/or degraded AC performance. Furthermore, this will defeat the short-circuit and over-temperature protection circuitry. Exceeding ±7V input with a shorted output will destroy the device.

The device is best protected by the insertion of the parallel combination of a 100 kΩ resistor (R1) and a small capacitor (C1) in series with the buffer input, and a 100 kΩ resistor (R2) from input to output of the buffer (see *Figure 1*). This network normally has no effect on the buffer output. However, if the buffer's current limit or shutdown is activated, and the output has a ground-referred load of significantly less than 100 kΩ, a large input-to-output voltage may be present. R1 and R2 then form a voltage divider, keeping the input-output differential below the 7V Maximum Rating for input voltages up to 14V. This protection network should be sufficient to protect the LM6121 from the output of nearly any op amp which is operated on supply voltages of ±15V or lower.

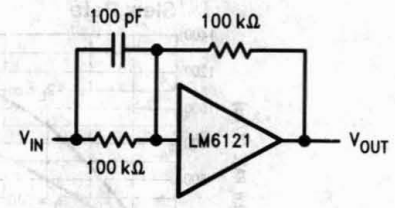

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FIGURE 1. LM6121 with Overvoltage Protection

Application Hints

HEATSINK REQUIREMENTS

A heatsink may be required with the LM6321 depending on the maximum power dissipation and maximum ambient temperature of the application. Under all possible operating conditions, the junction temperature must be within the range specified under Absolute Maximum Ratings.

To determine if a heatsink is required, the maximum power dissipated by the buffer, P(max), must be calculated. The formula for calculating the maximum allowable power dissipation in any application is $P_D = (T_J(max) - T_A)/\theta_{JA}$. For the simple case of a buffer driving a resistive load as in *Figure 2*, the maximum DC power dissipation occurs when the output is at half the supply. Assuming equal supplies, the formula is $P_D = I_S (2V^+) + V^{+2}/2\ R_L$.

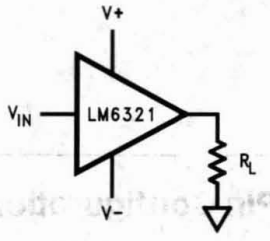

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FIGURE 2

The next parameter which must be calculated is the maximum allowable temperature rise, $T_R(max)$. This is calculated by using the formula:

$$T_R(max) = T_J(max) - T_A(max)$$

where: $T_J(max)$ is the maximum allowable junction temperature

$T_A(max)$ is the maximum ambient temperature

Using the calculated values for $T_R(max)$ and P(max), the required value for junction-to-ambient thermal resistance, $\theta_{(J-A)}$, can now be found:

$$\theta_{(J-A)} = T_R(max)/P(max)$$

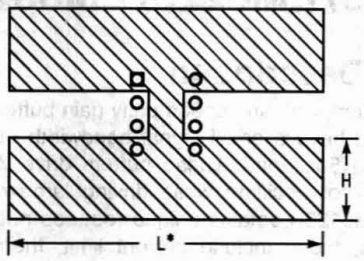
The heatsink for the LM6321 is made using the PC board copper. The heat is conducted from the die, through the lead frame (inside the part), and out the pins which are soldered to the PC board. The pins used for heat conduction are:

TABLE I

Part	Package	Pins
LM6321N	8-Pin DIP	1, 4, 5, 8
LM6321M	14-Pin SO	1, 2, 3, 6, 7, 8, 9, 13, 14

Figure 3 shows copper patterns which may be used to dissipate heat from the LM6321.

8-Pin DIP



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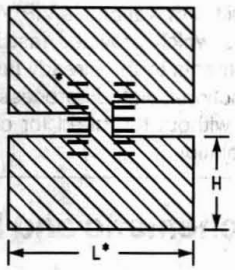
14-Pin SO



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*For best results, use L = 2H

FIGURE 3. Copper Heatsink Patterns

Table II shows some values of junction-to-ambient thermal resistance (θ_{J-A}) for values of L and W for 2 oz. copper:

TABLE II

Package	L (in.)	H (in.)	θ_{J-A} (°C/W)
8-Pin DIP	2	0.5	47
14-Pin SO	1	0.5	69
	2	1	57

2

National Semiconductor

LM6125/LM6225/LM6325 High Speed Buffer

General Description

The LM6125 family of high speed unity gain buffers slew at 800 V/μs and have a small signal bandwidth of 50 MHz while driving a 50Ω load. These buffers drive ±300 mA peak and do not oscillate while driving large capacitive loads. The LM6125 contains unique features not found in power buffers; these include current limit, thermal shutdown, electronic shutdown, and an error flag that warns of fault conditions.

These buffers are built with National's VIP™ (Vertically Integrated PNP) process which provides fast PNP transistors that are true complements to the already fast NPN devices. This advanced junction-isolated process delivers high speed performance without the need for complex and expensive dielectric isolation.

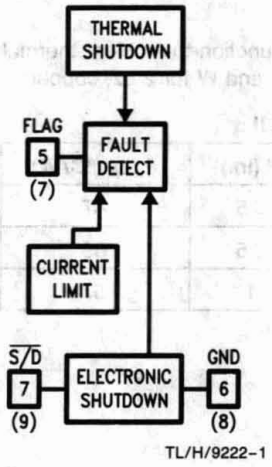
Features

- High slew rate — 800 V/μs
- High output current — ±300 mA
- Stable with large capacitive loads
- Current and thermal limiting
- Electronic shutdown
- 5V to ±15V operation guaranteed
- Fully specified to drive 50Ω lines

Applications

- Line Driving
- Radar
- Sonar

Simplified Schematic and Block Diagram



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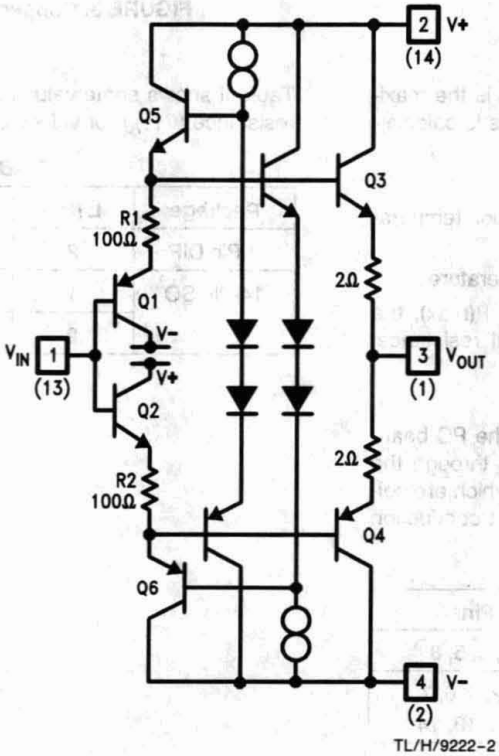

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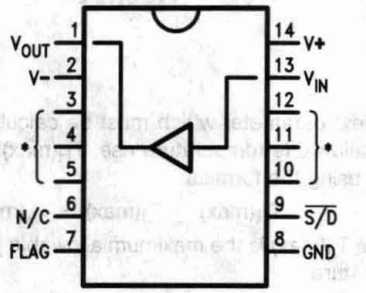
Numbers in ( ) are for 14-pin N DIP.

Pin Configurations



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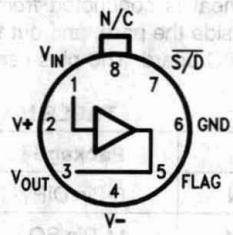
*Heat sinking pins.
Internally connected to V−.

Order Number LM6225N or LM6325N
See NS Package Number N14A



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Top View

Note: Pin 4 connected to case

Order Number LM6125H/883* or LM6125H
See NS Package Number H08C

*Available per 5962-9081501

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	36V (±18V)
Input to Output Voltage (Note 2)	±7V
Input Voltage	±Vsupply
Output Short-Circuit to GND (Note 3)	Continuous
Flag Output Voltage	GND ≤ Vflag ≤ +Vsupply
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	260°C
ESD Tolerance (Note 9)	±1500V
θ_{JA} (Note 4)	
H Package	150°C/W
N Package	40°C/W
Maximum Junction Temperature (T_J)	150°C
Operating Temperature Range	
LM6125	−55°C to +125°C
LM6225	−40°C to +85°C
LM6325	0°C to +70°C
Operating Supply Voltage Range	4.75V to ±16V

DC Electrical Characteristics

The following specifications apply for Supply Voltage = ±15V, V_{CM} = 0, $R_L \geq 100\ k\Omega$ and $R_S = 50\Omega$ unless otherwise noted. **Boldface** limits apply for $T_A = T_J = T_{MIN}$ to T_{MAX}; all other limits $T_A = T_J = 25°C$.

Symbol	Parameter	Conditions	Typ	LM6125 Limit (Notes 5, 10)	LM6225 Limit (Note 5)	LM6325 Limit (Note 5)	Units
A_{V1}	Voltage Gain 1	$R_L = 1k\Omega$, $V_{IN} = \pm 10V$	0.990	0.980 **0.970**	0.980 **0.950**	0.970 **0.950**	
A_{V2}	Voltage Gain 2	$R_L = 50\Omega$, $V_{IN} = \pm 10V$	0.900	0.860 **0.800**	0.860 **0.820**	0.850 **0.820**	V/V Min
A_{V3}	Voltage Gain 3 (Note 6)	$R_L = 50\Omega$, $V^+ = 5V$ $V_{IN} = 2\ V_{PP}$ **(1.5 V_{PP})**	0.840	0.780 **0.750**	0.780 **0.700**	0.750 **0.700**	
V_{OS}	Offset Voltage	$R_L = 1\ k\Omega$	15	30 **50**	30 **60**	50 **100**	mV Max
I_B	Input Bias Current	$R_L = 1\ k\Omega$, $R_S = 10\ k\Omega$	1	4 **7**	4 **7**	5 **7**	μA Max
R_{IN}	Input Resistance	$R_L = 50\Omega$	5				MΩ
C_{IN}	Input Capacitance		3.5				pF
R_O	Output Resistance	$I_{OUT} = \pm 10$ mA	3	5 **10**	5 **10**	5 **6**	Ω Max
I_{S1}	Supply Current 1	$R_L = \infty$	15	18 **20**	18 **20**	20 **22**	
I_{S2}	Supply Current 2	$R_L = \infty$, $V^+ = 5V$	14	16 **18**	16 **18**	18 **20**	mA Max
$I_{S/D}$	Supply Current in Shutdown	$R_L = \infty$, $V^{\pm} = \pm 15V$	1.1	1.5 **2.0**	1.5 **2.0**	1.5 **2.0**	
V_{O1}	Output Swing 1	$R_L = 1\ k\Omega$	13.5	13.3 **13**	13.3 **13**	13.2 **13**	
V_{O2}	Output Swing 2	$R_L = 100\Omega$	12.7	11.5 **10**	11.5 **10**	11 **10**	±V Min
V_{O3}	Output Swing 3	$R_L = 50\Omega$	12	11 **9**	11 **9**	10 **9**	
V_{O4}	Output Swing 4	$R_L = 50\Omega$	1.8	1.6 **1.3**	1.6 **1.4**	1.6 **1.5**	V_{PP} Min
PSRR	Power Supply Rejection Ratio	$V^+ = 5V$ (Note 6)	70	60 **55**	60 **50**	60 **50**	dB Min
V_{OL}	Flag Pin Output Low Voltage	$V^{\pm} = \pm 5V$ to $\pm 15V$ $V_{S/D} = 0V$		300 **400**	300 **400**	340 **400**	mV Max
I_{OH}	Flag Pin Output High Current	V_{OH} Flag Pin = 15V (Note 7)	0.01	10 **20**	10 **20**	10 **20**	μA Max

2

DC Electrical Characteristics (Continued)

The following specifications apply for Supply Voltage = ±15V, V_{CM} = 0, $R_L \geq 100\ k\Omega$ and $R_S = 50\Omega$ unless otherwise noted. **Boldface** limits apply for $T_A = T_J = T_{MIN}$ to T_{MAX}; all other limits $T_A = T_J = 25°C$.

Symbol	Parameter	Conditions	Typ	LM6125 Limit (Notes 5, 10)	LM6225 Limit (Note 5)	LM6325 Limit (Note 5)	Units
V_{TH}	Shutdown Threshold		1.4				V
V_{IH}	Shutdown Pin Trip Point High			2.0 **2.0**	2.0 **2.0**	2.0 **2.0**	V Min
V_{IL}	Shutdown Pin Trip Point Low			0.8 **0.8**	0.8 **0.8**	0.8 **0.8**	V Max
I_{IL}	Shutdown Pin Input Low Current	$V_{S/D}$ = 0V	−0.07	−10 **−20**	−10 **−20**	−10 **−20**	μA Max
I_{IH}	Shutdown Pin Input High Current	$V_{S/D}$ = 5V	−0.05	−10 **−20**	−10 **−20**	−10 **−20**	μA Max
I_O	Bi-State Output Current	Shutdown Pin = 0V V_{OUT} = +5V or −5V	1	50 **2000**	50 **100**	100 **200**	μA

AC Electrical Characteristics

The following specifications apply for Supply Voltage = ±15V, V_{CM} = 0, $R_L \geq 100\ k\Omega$ and $R_S = 50\Omega$ unless otherwise noted. **Boldface** limits apply for $T_A = T_J = T_{MIN}$ to T_{MAX}; all other limits $T_A = T_J = 25°C$.

Symbol	Parameter	Conditions	Typ	LM6125 Limit (Note 5)	LM6225 Limit (Note 5)	LM6325 Limit (Note 5)	Units
SR_1	Slew Rate 1	V_{IN} = ±11V, R_L = 1 kΩ	1200				
SR_2	Slew Rate 2	V_{IN} = ±11V, R_L = 50Ω (Note 8)	800	550	550	550	V/μs Min
SR_3	Slew Rate 3	V_{IN} = 2 V_{PP}, R_L = 50Ω V^+ = 5V (Note 6)	50				
BW	−3 dB Bandwidth	V_{IN} = 100 mV_{PP} R_L = 50Ω, $C_L \leq$ 10 pF	50	30	30	30	MHz Min
t_r, t_f	Rise Time Fall Time	R_L = 50Ω, $C_L \leq$ 10 pF V_O = 100 mV_{PP}	8.0				ns
t_{PD}	Propagation Delay Time	R_L = 50Ω, $C_L \leq$ 10 pF V_O = 100 mV_{PP}	4.0				ns
O_S	Overshoot	R_L = 50Ω, $C_L \leq$ 10 pF V_O = 100 mV_{PP}	10				%
V_{FT}	V_{IN}, V_{OUT} Feedthrough in Shutdown	Shutdown Pin = 0V V_{IN} = 4 V_{PP}, 1 MHz R_L = 50Ω	−50				dB
C_{OUT}	Output Capacitance in Shutdown	Shutdown Pin = 0V	30				pF
t_{SD}	Shutdown Response Time		700				ns

Electrical Characteristics (Continued)

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications do not apply when operating the device beyond its rated operating conditions.

Note 2: During current limit, thermal limit, or electronic shutdown the input current will increase if the input to output differential voltage exceeds 8V. See Overvoltage Protection in Application Hints.

Note 3: The LM6125 series buffers contain current limit and thermal shutdown to protect against fault conditions.

Note 4: For operation at elevated temperature, these devices must be derated based on a thermal resistance of θ_{JA} and T_J max, $T_J = T_A + \theta_{JA} P_D$. θ_{JC} for the LM6125H and LM6225H is 17°C/W. The thermal impedance θ_{JA} of the device in the N package is 40°C/W when soldered directly to a printed circuit board, and the heat-sinking pins (pins 3, 4, 5, 10, 11, and 12) are connected to 2 square inches of 2 oz. copper. When installed in a socket, the thermal impedance θ_{JA} of the N package is 60°C/W.

Note 5: Limits are guaranteed by testing or correlation.

Note 6: The input is biased to +2.5V, and V_{IN} swings V_{PP} about this value. The input swing is 2 V_{PP} at all temperatures except for the A_V3 test at −55°C where it is reduced to 1.5 V_{PP}.

Note 7: The Error Flag is set (low) during current limit or thermal fault detection in addition to being set by the Shutdown pin. It is an open-collector output which requires an external pullup resistor.

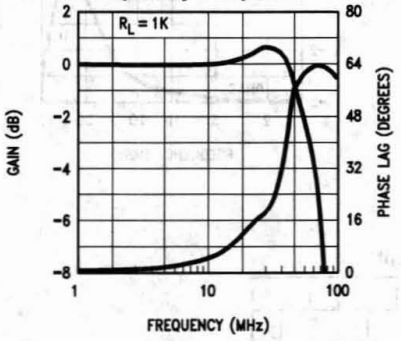
Note 8: Slew rate is measured with a ±11V input pulse and 50Ω source impedance at 25°C. Since voltage gain is typically 0.9 driving a 50Ω load, the output swing will be approximately ±10V. Slew rate is calculated for transitions between ±5V levels on both rising and falling edges. A high speed measurement is done to minimize device heating. For slew rate versus junction temperature see typical performance curves. The input pulse amplitude should be reduced to ±10V for measurements at temperature extremes. For accurate measurements, the input slew rate should be at least 1700 V/μs.

Note 9: The test circuit consists of the human body model of 120 pF in series with 1500Ω.

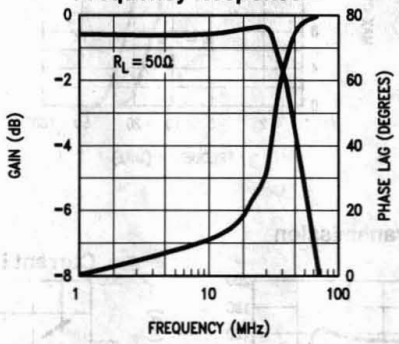
Note 10: A military RETS specification is available on request. At the time of printing, the LM6125H/883 RETS spec complied with the **Boldface** limits in this column. The LM6125H/883 may also be procured as Standard Military Drawing specification #5962-9081501MXX.

Typical Performance Characteristics T_A = 25°C, V_S = ±15V, unless otherwise specified

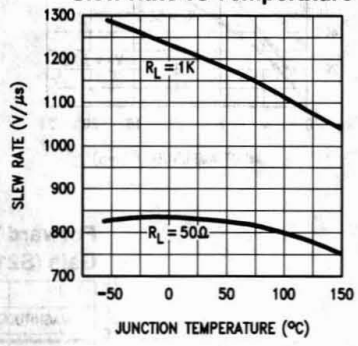
Frequency Response



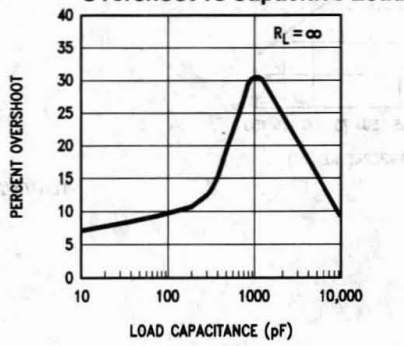
Frequency Response



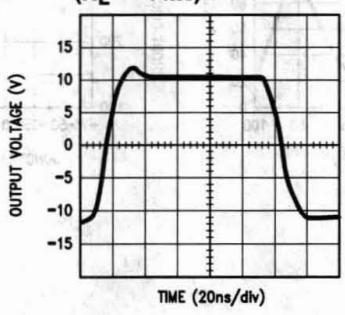
Slew Rate vs Temperature



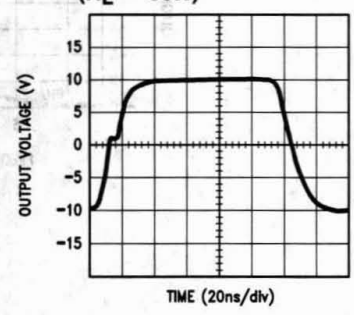
Overshoot vs Capacitive Load



Large Signal Response (R_L = 1 kΩ)



Large Signal Response (R_L = 50Ω)



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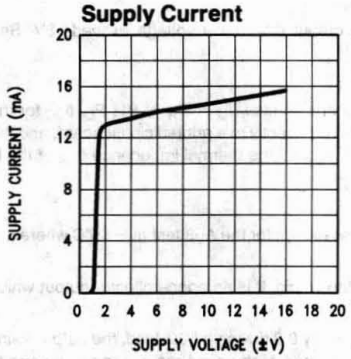
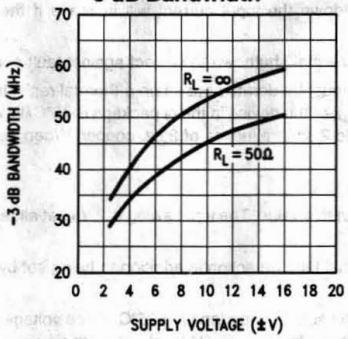
2

Typical Performance Characteristics $T_A = 25°C$, $V_S = \pm 15V$, unless otherwise specified (Continued)

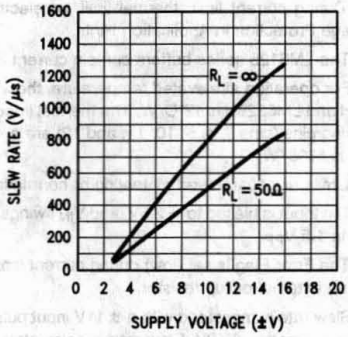
Supply Current



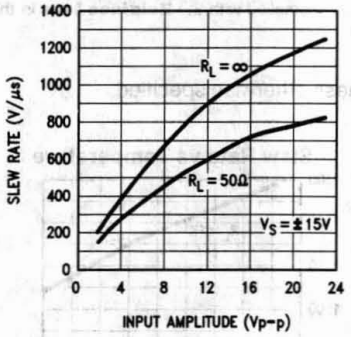
−3 dB Bandwidth



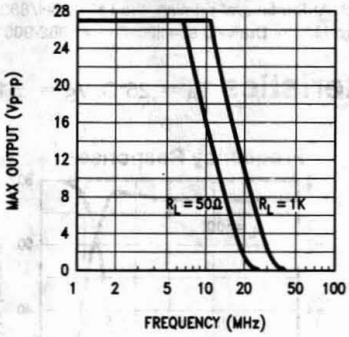
Slew Rate



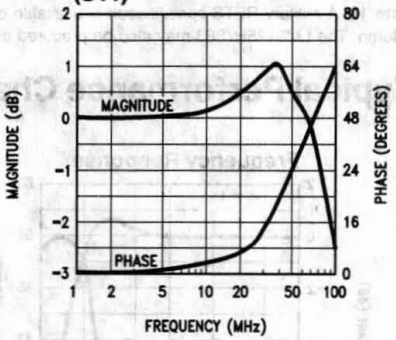
Slew Rate



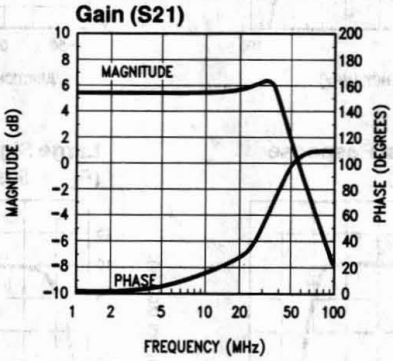
Power Bandwidth



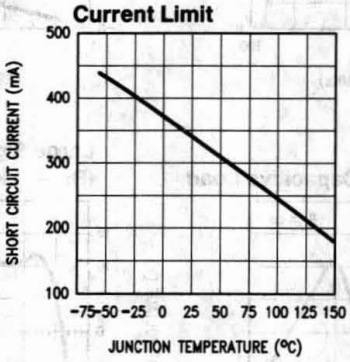
Input Return Gain (S11)



Forward Transmission Gain (S21)



Current Limit



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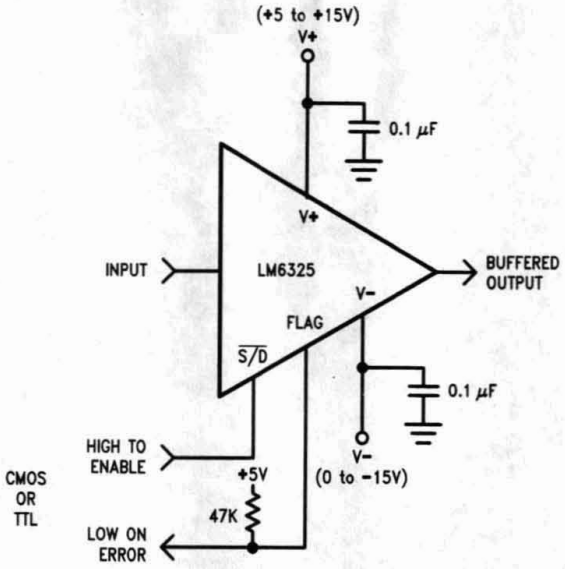
Typical Connection Diagram



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Application Hints

POWER SUPPLY DECOUPLING

The method of supply bypassing is not critical for stability of the LM6125 series buffers. However, their high current output combined with high slew rate can result in significant voltage transients on the power supply lines if much inductance is present. For example, a slew rate of 900 V/μs into a 50Ω load produces a di/dt of 18 A/μs. Multiplying this by a wiring inductance of 50 nH results in a 0.9V transient. To minimize this problem use high quality decoupling very close to the device. Suggested values are a 0.1 μF ceramic in parallel with one or two 2.2 μF tantalums. A ground plane is recommended.

LOAD IMPEDANCE

The LM6125 is stable into any load when driven by a 50Ω source. As shown in the *Overshoot vs Capacitive Load* graph, worst case is a purely capacitive load of about 1000 pF. Shunting the load capacitance with a resistor will reduce overshoot.

SOURCE INDUCTANCE

Like any high-frequency buffer, the LM6125 can oscillate at high values of source inductance. The worst case condition occurs at a purely capacitive load of 50 pF where up to 100 nH of source inductance can be tolerated. With a 50Ω load, this goes up to 200 nH. This sensitivity may be reduced at the expense of a slight reduction in bandwidth by adding a resistor in series with the buffer input. A 100Ω resistor will ensure stability with source inductances up to 400 nH with any load.

ERROR FLAG LOGIC

The Error Flag pin is an open-collector output which requires an external pull-up resistor. Flag voltage is HIGH during operation, and is LOW during a fault condition. A fault condition occurs if either the internal current limit or the thermal shutdown is activated, or the shutdown (S/D) pin is driven low by external logic. Flag voltage returns to its HIGH state when normal operation resumes.

If the S/D pin is not to be used, it should be connected to V^+.

OVERVOLTAGE PROTECTION

The LM6125 may be severely damaged or destroyed if the Absolute Maximum Rating of 7V between input and output pins is exceeded.

If the buffer's input-to-output differential voltage is allowed to exceed 7V, a base-emitter junction will be in reverse-breakdown, and will be in series with a forward-biased base-emitter junction. Referring to the LM6125 simplified schematic, the transistors involved are Q1 and Q3 for positive inputs, and Q2 and Q4 for negative inputs. If any current is allowed to flow through these junctions, localized heating of the reverse-biased junction will occur, potentially causing damage. The effect of the damage is typically increased offset voltage, increased bias current, and/or degraded AC performance. The damage is cumulative, and may eventually result in complete device failure.

The device is best protected by the insertion of the parallel combination of a 100 kΩ resistor (R1) and a small capacitor (C1) in series with the buffer input, and a 100 kΩ resistor (R2) from input to output of the buffer (see *Figure 1*). This network normally has no effect on the buffer output. However, if the buffer's current limit or shutdown is activated, and the output has a ground-referred load of significantly less than 100 kΩ, a large input-to-output voltage may be present. R1 and R2 then form a voltage divider, keeping the input-output differential below the 7V Maximum Rating for input voltages up to 14V. This protection network should be sufficient to protect the LM6125 from the output of nearly any op amp which is operated on supply voltages of ±15V or lower.

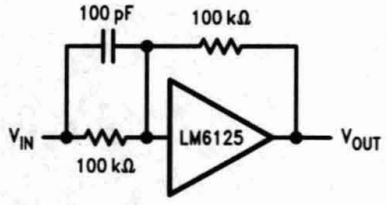

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FIGURE 1. LM6125 with Overvoltage Protection

Section 3
Automotive

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Peripheral Drivers

Peripheral drivers is a broad definition given to interface power devices. The devices generally have open-collector output transistors that can switch hundreds of milliamps at high voltage and are driven by standard logic gates. They serve many applications including relay drivers, printer hammer drivers, lamp drivers, bus drivers, core memory drivers, voltage level translators, stepper motor drivers and solenoid drivers.

Unlike standard logic devices, peripheral drivers have many varied load situations depending on the application. This requires the design engineer to interpret device specifications in greater detail. Designers at National Semiconductor have incorporated many technically advanced and useful features into their broad line of peripheral driver devices.

Some of these features include:

- Short circuit protection at individual outputs
- Glitch-free power up/down
- Fail-safe operation
- Inductive fly-back protection
- Negative transient protection
- High input impedance for CMOS/NMOS compatibility

For further information on National Semiconductor's broad line of peripheral drivers, refer to the selection guide to follow and application note AN-213 in Appendix H.

PERIPHERAL DRIVERS SELECTION GUIDE

Device Number and Temperature Range		Drivers/ Package	Logic Function (Driver On)	Input Compatibility (Logic)	Output High Voltage (V)	Latch-Up Voltage (Note 1) (V)	Output Low Voltage (V)	Output Low Current (mA)	Propagation Delay Typ (ns)	On Power Supply Current (mA)	Page No.
0°C to +70°C	−55°C to +125°C										
DP8310	DP7310	8	(Note 2)	TTL	30		0.5	100	40	152	3-6
DP8311	DP7311	8	(Note 3)	TTL	30		0.5	100	40	125	3-6
DS2003C	DS2003M	7	NAND	TTL/CMOS	50		1.6	350	5000		3-18
DS9667C	DS9667M										3-18
DS2004C	DS2004M	7	NAND	CMOS/PMOS	50		1.6	350	5000		3-18
DS3631	DS1631	2	AND	CMOS	56	40	1.4	300	150	8	3-13
DS3632	DS1632	2	NAND	CMOS	56	40	1.4	300	150	8	3-13
DS3633	DS1633	2	OR	CMOS	56	40	1.4	300	150	8	3-13
DS3634	DS1634	2	NOR	CMOS	56	40	1.4	300	150	8	3-13
DS3658		4	NAND	TTL/LS	70	35	0.7	600	2430	65	3-23
DS3668		4	NAND	TTL/LS	70	(Note 4)	1.5	600	2000	80	3-26
DS3680		4	(Note 5)	TTL/CMOS	−2.1	−60	−60	−50	10,000	4.4	3-29
DS75451	DS55451	2	AND	TTL	30	20	0.7	300	31	55	3-32
DS75452	DS55452	2	NAND	TTL	30	20	0.7	300	31	55	3-32
DS75453	DS55453	2	OR	TTL	30	20	0.7	300	31	55	3-32
DS75454	DS55454	2	NOR	TTL	30	20	0.7	300	31	55	3-32

Note 1: Latch-up voltage is the maximum voltage the output can sustain when switching an inductive load.

Note 2: DS8310 inverting, positive edge latching.

Note 3: DS8311 inverting, fall through latch.

Note 4: DS3668 35V, latch-up with output fault protection.

Note 5: DS3680 has a differential input circuit.

HIGH CURRENT SWITCH SELECTION GUIDE

Device	Drivers/ Package	Continuous Current	Peak Current	Input Voltage Range	Diagnostics
LM1921*	1	1.0A	2.0A	4.5V to 26V	none
LM1950*	1	750 mA	1.4A	4.75V to 26V	none
LM1951*	1	1.0A	2.5A	4.5V to 26V	Error Flag
LMD18400*	4	1.0A	3.0A	6V to 28V	Error Flag Thermal Shutdown Flag Data Output provides switch status feedback, output load fault conditions and thermal and overvoltage shut-down status.

*All incorporate Automotive transient protection.

High Current Switch Selection Guide

Device	Drivers/ Package	Continuous Current	Peak Current	Input Voltage Range*	Diagnostics	Page No.
LM1921	1	1.0A	2.0A	4.5V to 26V	None	3-44
LM1950	1	750 mA	1.4A	4.75V to 26V	None	3-49
LM1951	1	1.0A	2.5A	4.5V to 26V	Error Flag	3-54
LMD18400	4	1.0A	3.0A	6V to 26V	Error Flag Thermal Shutdown Flag Data Output provides switch status feedback, output load fault conditions and thermal and overvoltage shutdown status.	3-74

*All devices incorporate Automotive transient protection.

National Semiconductor

DP7310/DP8310/DP7311/DP8311 Octal Latched Peripheral Drivers

General Description

The DP7310/8310, DP7311/8311 Octal Latched Peripheral Drivers provide the function of latching eight bits of data with open collector outputs, each driving up to 100 mA DC with an operating voltage range of 30V. Both devices are designed for low input currents, high input/output voltages, and feature a power up clear (outputs off) function.

The DP7310/8310 are positive edge latching. Two active low write/enable inputs are available for convenient data bussing without external gating.

The DP7311/8311 are positive edge latches. The active low strobe input latches data or allows fall through operation when held at logic "0". The latches are cleared (outputs off) with a logic "0" on the clear pin.

Features

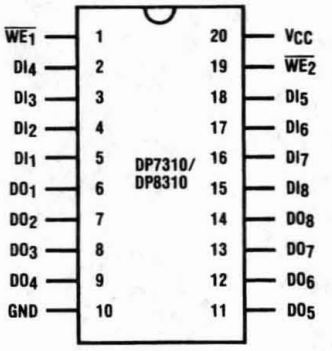
- High current, high voltage open collector outputs
- Low current, high voltage inputs
- All outputs simultaneously sink rated current "DC" with no thermal derating at maximum rated temperature
- Parallel latching or buffering
- Separate active low enables for easy data bussing
- Internal "glitch free" power up clear
- 10% V_{CC} tolerance

Applications

- High current high voltage drivers
- Relay drivers
- Lamp drivers
- LED drivers
- TRIAC drivers
- Solenoid drivers
- Stepper motor drivers
- Level translators
- Fiber-optic LED drivers

Connection Diagrams

Dual-In-Line Package



TL/F/5246–1

Top View

Dual-In-Line Package

TL/F/5246–2

Top View

Order Number DP7310J, DP7311J, DP8310N or DP8311N
See NS Package Number J20A or N20A

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7.0V
Input Voltage	35V
Output Voltage	35V
Maximum Power Dissipation* at 25°C	
Cavity Package	1821 mW
DP8310/DP8311	2005 mW
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 4 sec.)	260°C

*Derate cavity package 12.1 mW/°C above 25°C; derate molded package 16.0 mW/°C above 25°C.

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	4.5	5.5	V
Temperature			
DP7310/DP7311	−55	+125	°C
DP8310/DP8311	0	+70	°C
Input Voltage		30	V
Output Voltage		30	V

DC Electrical Characteristics DP7310/DP8310, DP7311/DP8311 (Notes 2 and 3)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{IH}	Logical "1" Input Voltage		2.0			V
V_{IL}	Logical "0" Input Voltage				0.8	V
V_{OL}	Logical "0" Output Voltage	Data outputs latched to logical "0", V_{CC} = Min.				
	DP7310/DP7311	I_{OL} = 75 mA			0.4	V
	DP8310/DP8311	I_{OL} = 100 mA		0.35	0.5	V
I_{OH}	Logical "1" Output Current	Data outputs latched to logical "1", V_{CC} = Min.				
	DP7310/DP7311	V_{OH} = 25V			500	μA
	DP8310/DP8311	V_{OH} = 30V		2.5	250	μA
I_{IH}	Logical "1" Input Current	V_{IH} = 2.7V, V_{CC} = Max		0.1	25	μA
I_I	Input Current at Maximum Input Voltage	V_{IN} = 30V, V_{CC} = Max		1	250	μA
I_{IL}	Logical "0" Input Current	V_{IN} = 0.4V, V_{CC} = Max		−215	−300	μA
V_{clamp}	Input Clamp Voltage	I_{IN} = 12 mA		−0.8	−1.5	V
I_{CC0}	Supply Current, Outputs On	Data outputs latched to a logical "0". All Inputs are at logical "1", V_{CC} = Max.				
	DP7310			100	125	mA
	DP8310			100	152	mA
	DP7311			88	117	mA
	DP8311			88	125	mA
I_{CC1}	Supply Current, Outputs Off	Data outputs latched to a logic "1". Other conditions same as I_{CC0}.				
	DP7310			40	47	mA
	DP8310			40	57	mA
	DP7311			25	34	mA
	DP8311			25	36	mA

AC Electrical Characteristics DP7310/DP8310: V_{CC} = 4.5V, T_A = −55°C to +125°C

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{pd0}	High to Low Propagation Delay Write Enable Input to Output	*(Figure 1)*		40	120	ns
t_{pd1}	Low to High Propagation Delay Write Enable Input to Output	*(Figure 1)*		70	150	ns
t_{SETUP}	Minimum Set-Up Time Data in to Write Enable Input	t_{HOLD} = 0 ns *(Figure 1)*	45	20		ns
t_{pWH}, t_{pWL}	Minimum Write Enable Pulse Width	*(Figure 1)*	60	25		ns
t_{THL}	High to Low Output Transition Time	*(Figure 1)*		16	35	ns
t_{TLH}	Low to High Output Transition Time	*(Figure 1)*		38	70	ns
C_{IN}	"N" Package (Note 4)			5	15	pF

AC Electrical Characteristics DP7311/DP8311: V_{CC} = 5V, T_A = 25°C

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{pd0}	High to Low Propagation Delay Data In to Output	*(Figure 2)*		30	60	ns
t_{pd1}	Low to High Propagation Delay Data to Output	*(Figure 2)*		70	100	ns
t_{SETUP}	Minimum Set-Up Time Data in to Strobe Input	t_{HOLD} = 0 ns *(Figure 2)*	0	−25		ns
t_{pWL}	Minimum Strobe Enable Pulse Width	*(Figure 2)*	60	35		ns
t_{pdC}	Propagation Delay Clear to Data Output	*(Figure 2)*		70	135	ns
t_{pWC}	Minimum Clear Input Pulse Width	*(Figure 2)*	60	25		ns
t_{THL}	High to Low Output Transition Time	*(Figure 2)*		20	35	ns
t_{TLH}	Low to High Output Transition Time	*(Figure 2)*		38	60	ns
C_{IN}	Input Capacitance—Any Input	(Note 4)		5	15	pF

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DP7310/DP7311 and across the 0°C to +70°C for the DP8310/DP8311. All typical values are for T_A = 25°C, V_{CC} = 5V.

Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted.

Note 4: Input capacitance is guaranteed by periodic testing. f_{TEST} = 10 kHz at 300 mV, T_A = 25°C.

Logic Table

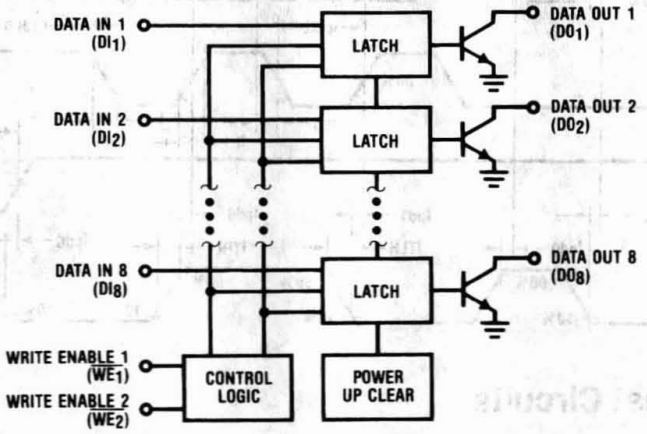
DP7310/DP8310			
Write Enable 1 $\overline{WE_1}$	Write Enable 2 $\overline{WE_2}$	Data Input DI_{1-8}	Data Output DO_{1-8}
0	0	X	Q
0	↓	0	1
0	↓	1	0
↓	0	0	1
↓	0	1	0
0	1	X	Q
1	0	X	Q
1	1	X	Q

DP7311/DP8311			
Clear $\overline{CLR}$	Strobe $\overline{STR}$	Data Input DI_{1-8}	Data Output DO_{1-8}
1	1	X	Q
1	0	0	1
1	0	1	0
0	X	X	1

X = Don't Care
1 = Outputs Off
0 = Outputs On
Q = Pre-existing Output
↓ = Positive Edge Transition

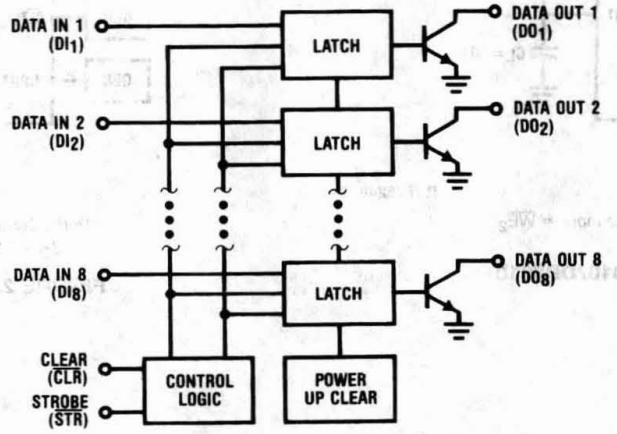
Block Diagrams

DP7310/DP8310



TL/F/5246–3

DP7311/DP8311

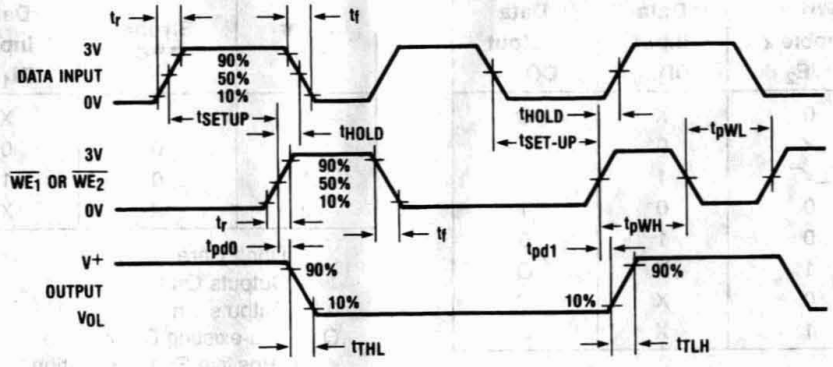


TL/F/5246–4

3

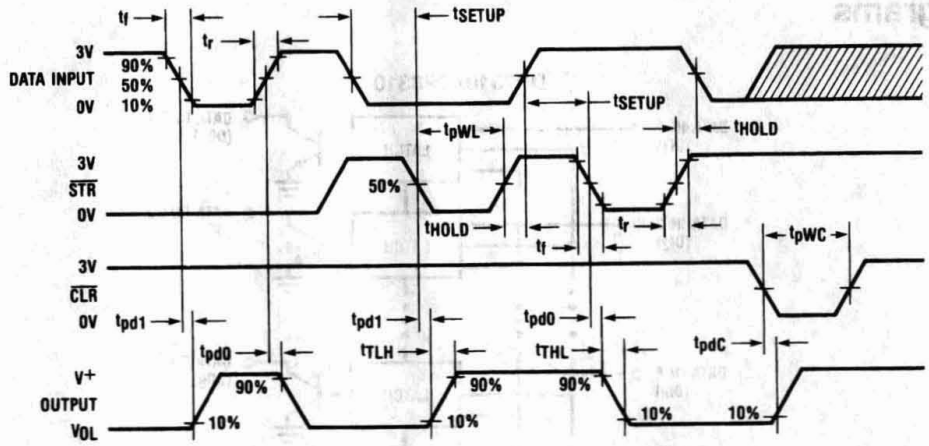
Switching Time Waveforms

DP7310/DP8310



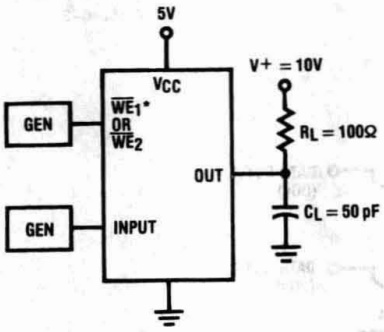
TL/F/5246–5

DP7311/DP8311



TL/F/5246–6

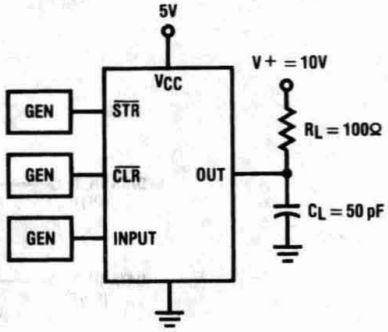
Switching Time Test Circuits



TL/F/5246–7

*$\overline{WE}_1$ = 0V When the Input = $\overline{WE}_2$

FIGURE 1. DP7310/DP8310



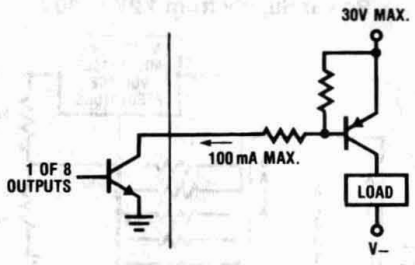
TL/F/5246–8

Pulse Generator Characteristics:
$Z_O = 50\Omega$, $t_r = t_f = 5$ ns

FIGURE 2. DP7311/DP8311

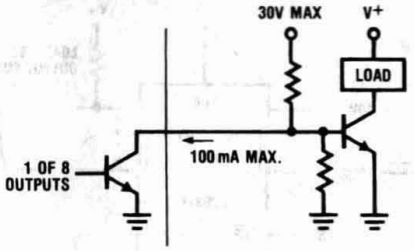
Typical Applications DP8310/11 Buffering High Current Device (Notes 1 and 2)

PNP High Current Driver



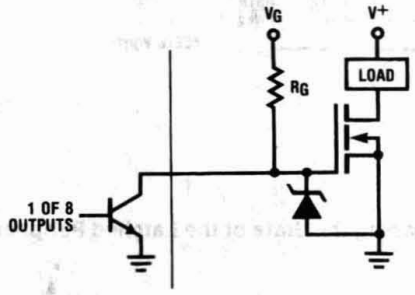
TL/F/5246–9

NPN High Current Driver



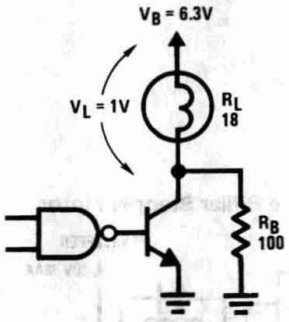
TL/F/5246–10

VMOS High Current Driver



TL/F/5246–11

Circuit Used to Reduce Peak Transient Lamp Current



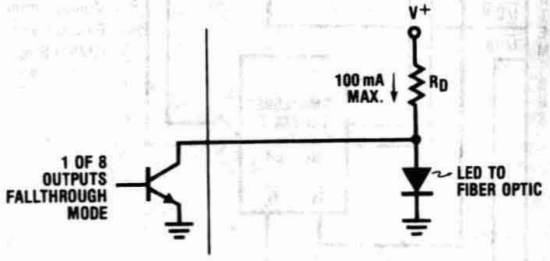
TL/F/5246–12

$$R_B = \left(\frac{V_B - V_L}{V_L}\right) R_L$$

$$R_B = \left(\frac{6.3 - 1}{1}\right) 18\Omega = 95.4 \approx 100\Omega$$

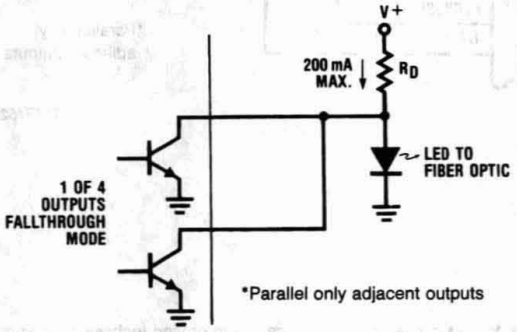
Eight Output/Four Output Fiber Optic LED Driver

DP8311 100 mA Drivers



TL/F/5246–13

DP8311 Parallel Outputs (200 mA) Drivers*

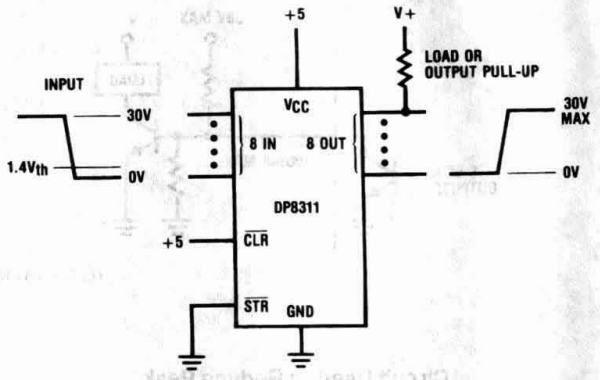


*Parallel only adjacent outputs

TL/F/5246–14

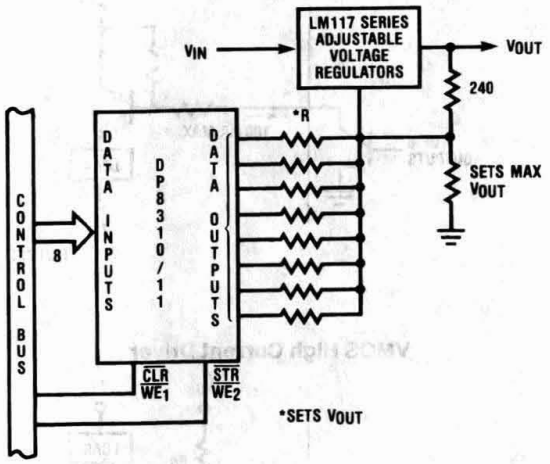
Typical Applications (Continued)

8-Bit Level Translator-Driver



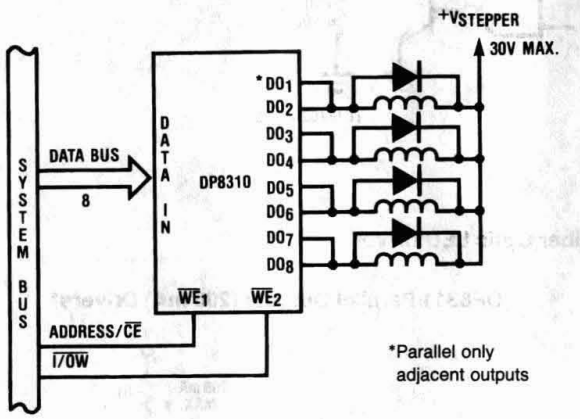
TL/F/5246–15

Digital Controlled 256 Level Power Supply from 1.2V to 30V



TL/F/5246–16

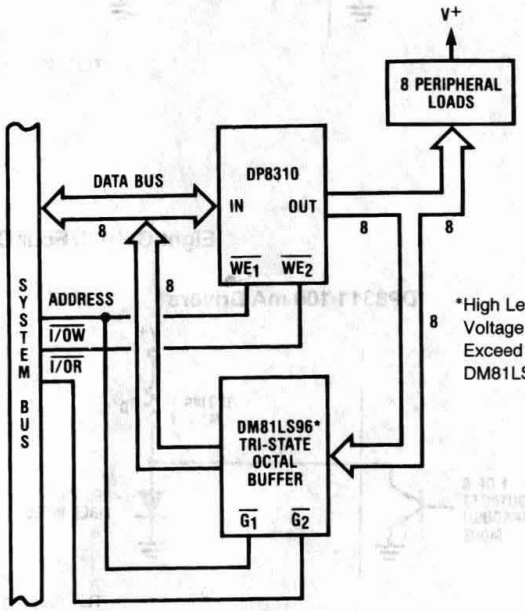
200 mA Drive for a 4 Phase Bifilar Stepper Motor



*Parallel only adjacent outputs

TL/F/5246–17

Reading the State of the Latched Peripherals



*High Level Input Voltage must not Exceed V_{CC} of the DM81LS96

TL/F/5246–18

Note 1: Always use good V_{CC} bypass and ground techniques to suppress transients caused by peripheral loads.

Note 2: Printed circuit board mounting is required if these devices are operated at maximum rated temperature and current (all outputs on DC).

National Semiconductor

DS1631/DS3631/DS1632/DS3632/DS1633/DS3633/ DS1634/DS3634 CMOS Dual Peripheral Drivers

General Description

The DS1631 series of dual peripheral drivers was designed to be a universal set of interface components for CMOS circuits.

Each circuit has CMOS compatible inputs with thresholds that track as a function of V_{CC} (approximately ½ V_{CC}). The inputs are PNPs providing the high impedance necessary for interfacing with CMOS.

Outputs have high voltage capability, minimum breakdown voltage is 56V at 250 μA.

The outputs are Darlington connected transistors. This allows high current operation (300 mA max) at low internal V_{CC} current levels since base drive for the output transistor is obtained from the load in proportion to the required loading conditions. This is essential in order to minimize loading on the CMOS logic supply.

Typical V_{CC} = 5V power is 28 mW with both outputs ON. V_{CC} operating range is 4.5V to 15V.

The circuit also features output transistor protection if the V_{CC} supply is lost by forcing the output into the high impedance OFF state with the same breakdown levels as when V_{CC} was applied.

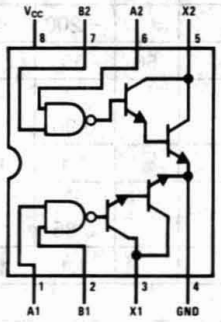
Pin-outs are the same as the respective logic functions found in the following popular series of circuits: DS75451, DS75461. This feature allows direct conversion of present systems to the MM74C CMOS family and DS1631 series circuits with great power savings.

The DS1631 series is also TTL compatible at V_{CC} = 5V.

Features

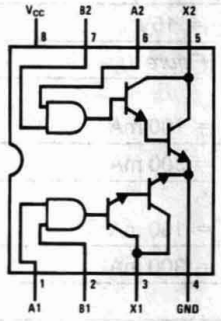
- CMOS compatible inputs
- High impedance inputs — PNP's
- High output voltage breakdown — 56V min
- High output current capability — 300 mA max
- Same pin-outs and logic functions as DS75451 and DS75461 series circuits
- Low V_{CC} power dissipation (28 mW both outputs "ON" at 5V)

Connection Diagrams (Dual-In-Line and Metal Can Packages)



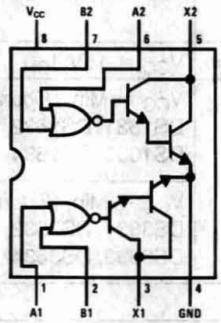
TL/F/5816–1

Top View
Order Number DS1631J-8 or DS3631N



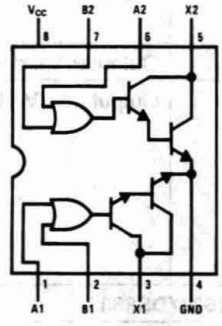
TL/F/5816–2

Top View
Order Number DS1632J-8 or DS3632N



TL/F/5816–3

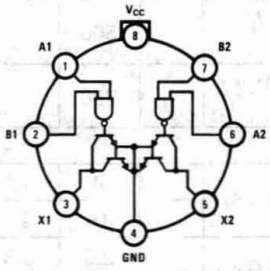
Top View
Order Number DS1633J-8 or DS3633N



TL/F/5816–4

Top View
Order Number DS1634J-8 or DS3634N

See NS Package Number J08A or N08E

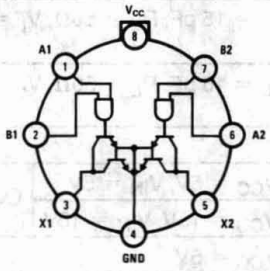


TL/F/5816–5

Top View

(Pin 4 is electrically connected to the case.)

Order Number DS1631H

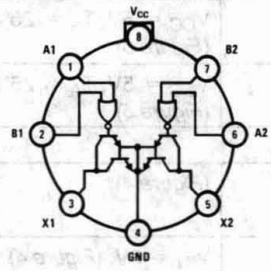


TL/F/5816–6

Top View

(Pin 4 is electrically connected to the case.)

Order Number DS1632H

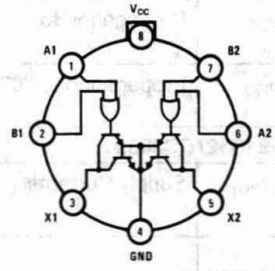


TL/F/5816–7

Top View

(Pin 4 is electrically connected to the case.)

Order Number DS1633H



TL/F/5816–8

Top View

(Pin 4 is electrically connected to the case.)

Order Number DS1634H

See NS Package Number H08C

3

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	16V
Voltage at Inputs	−0.3V to V_{CC} + 0.3V
Output Voltage	56V
Storage Temperature Range	−65°C to +150°C
Maximum Power Dissipation* at 25°C	
Cavity Package	1133 mW
Molded Package	1022 mW
TO-5 Package	787 mW
Lead Temperature (Soldering, 4 sec.)	260°C

*Derate cavity package 7.6 mW/°C above 25°C; derate molded package 8.2 mW/°C above 25°C; derate TO-5 package 5.2 mW/°C above 25°C.

Operating Conditions

	Min	Max	Units
Supply Voltage, V_{CC}			
DS1631/DS1632/ DS1633/DS1634	4.5	15	V
DS3631/DS3632/ DS3633/DS3634	4.75	15	V
Temperature, T_A			
DS1631/DS1632/ DS1633/DS1634	−55	+125	°C
DS3631/DS3632/ DS3633/DS3634	0	+70	°C

Electrical Characteristics (Notes 2 and 3)

Symbol	Parameter	Conditions			Min	Typ	Max	Units
ALL CIRCUITS								
V_{IH}	Logical "1" Input Voltage	(*Figure 1*)	V_{CC} = 5V		3.5	2.5		V
			V_{CC} = 10V		8.0	5		V
			V_{CC} = 15V		12.5	7.5		V
V_{IL}	Logical "0" Input Voltage	(*Figure 1*)	V_{CC} = 5V			2.5	1.5	V
			V_{CC} = 10V			5.5	2.0	V
			V_{CC} = 15V			7.5	2.5	V
I_{IH}	Logical "1" Input Current	V_{CC} = 15V, V_{IN} = 15V, (*Figure 2*)				0.1	10	μA
I_{IL}	Logical "0" Input Current	V_{IN} = 0.4V, (*Figure 3*)	V_{CC} = 5V			−50	−120	μA
			V_{CC} = 15V			−200	−360	μA
V_{OH}	Output Breakdown Voltage	V_{CC} = 15V, I_{OH} = 250 μA, (*Figure 1*)			56	65		V
V_{OL}	Output Low Voltage	V_{CC} = Min, (*Figure 1*), DS1631, DS1632, DS1633, DS1634	I_{OL} = 100 mA			0.85	1.1	V
			I_{OL} = 300 mA			1.1	1.4	V
		V_{CC} = Min, (*Figure 1*), DS3631, DS3632, DS3633, DS3634	I_{OL} = 100 mA			0.85	1.0	V
			I_{OL} = 300 mA			1.1	1.3	V
DS1631/DS3631								
$I_{CC(0)}$	Supply Currents	V_{IN} = 0V, (*Figure 4*)	V_{CC} = 5V	Output Low		7	11	mA
			V_{CC} = 15V	Both Drivers		14	20	mA
$I_{CC(1)}$		(*Figure 4*)	V_{CC} = 5V, V_{IN} = 5V	Output High		2	3	mA
			V_{CC} = 15V, V_{IN} = 15V	Both Drivers		7.5	10	mA
t_{PD1}	Propagation to "1"	V_{CC} = 5V, T_A = 25°C, C_L = 15 pF, R_L = 50Ω, V_L = 10V, (*Figure 5*)				500		ns
t_{PD0}	Propagation to "0"	V_{CC} = 5V, T_A = 25°C, C_L = 15 pF, R_L = 50Ω, V_L = 10V, (*Figure 5*)				750		ns
DS1632/DS3632								
$I_{CC(0)}$	Supply Currents	(*Figure 4*)	V_{CC} = 5V, V_{IN} = 5V	Output Low		8	12	mA
			V_{CC} = 15V, V_{IN} = 15V			18	23	mA
$I_{CC(1)}$		V_{IN} = 0V, (*Figure 4*)	V_{CC} = 5V	Output High		2.5	3.5	mA
			V_{CC} = 15V			9	14	mA
t_{PD1}	Propagation to "1"	V_{CC} = 5V, T_A = 25°C, C_L = 15 pF, R_L = 50Ω, V_L = 10V, (*Figure 5*)				500		ns
t_{PD0}	Propagation to "0"	V_{CC} = 5V, T_A = 25°C, C_L = 15 pF, R_L = 50Ω, V_L = 10V, (*Figure 5*)				750		ns

Electrical Characteristics (Notes 2 and 3) (Continued)

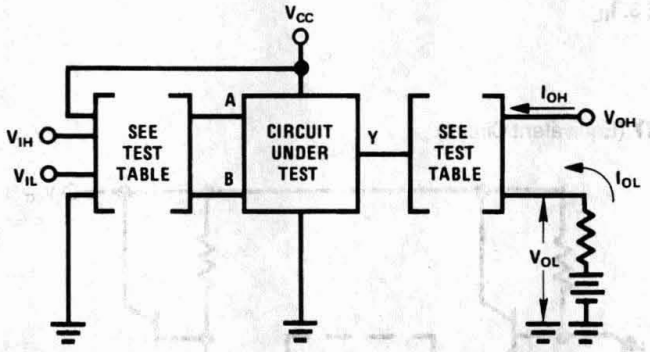
Symbol	Parameter	Conditions			Min	Typ	Max	Units
DS1633/DS3633								
$I_{CC(0)}$	Supply Currents	V_{IN} = 0V, (*Figure 4*)	V_{CC} = 5V	Output Low		7.5	12	mA
			V_{CC} = 15V			16	23	mA
$I_{CC(1)}$		(*Figure 4*)	V_{CC} = 5V, V_{IN} = 5V	Output High		2	4	mA
			V_{CC} = 15V, V_{IN} = 15V			7.2	15	mA
t_{PD1}	Propagation to "1"	V_{CC} = 5V, T_A = 25°C, C_L = 15 pF, R_L = 50Ω, V_L = 10V, (*Figure 5*)				500		ns
t_{PD0}	Propagation to "0"	V_{CC} = 5V, T_A = 25°C, C_L = 15 pF, R_L = 50Ω, V_L = 10V, (*Figure 5*)				750		ns
DS1634/DS3634								
$I_{CC(0)}$	Supply Currents	(*Figure 4*)	V_{CC} = 5V, V_{IN} = 5V	Output Low		7.5	12	mA
			V_{CC} = 15V, V_{IN} = 15V			18	23	mA
$I_{CC(1)}$		V_{IN} = 0V, (*Figure 4*)	V_{CC} = 5V	Output High		3	5	mA
			V_{CC} = 15V			11	18	mA
t_{PD1}	Propagation to "1"	V_{CC} = 5V, T_A = 25°C, C_L = 15 pF, R_L = 50Ω, V_L = 10V, (*Figure 5*)				500		ns
t_{PD0}	Propagation to "0"	V_{CC} = 5V, T_A = 25°C, C_L = 15 pF, R_L = 50Ω, V_L = 10V, (*Figure 5*)				750		ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DS1631, DS1632, DS1633 and DS1634 and across the 0°C to +70°C range for the DS3631, DS3632, DS3633 and DS3634. All typical values are for T_A = 25°C.

Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

Test Circuits



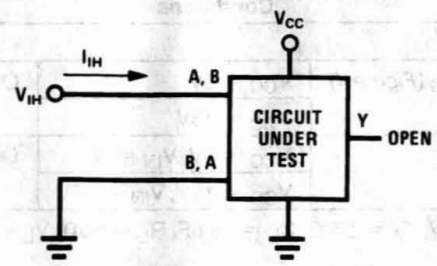
TL/F/5816–9

Circuit	Input Under Test	Other Input	Output	
			Apply	Measure
DS3631	V_{IH} V_{IL}	V_{IH} V_{CC}	I_{OH} I_{OL}	V_{OH} V_{OL}
DS3632	V_{IH} V_{IL}	V_{IH} V_{CC}	I_{OL} I_{OH}	V_{OL} V_{OH}
DS3633	V_{IH} V_{IL}	GND V_{IL}	I_{OH} I_{OL}	V_{OH} V_{OL}
DS3634	V_{IH} V_{IL}	GND V_{IL}	I_{OL} I_{OH}	V_{OL} V_{OH}

Note: Each input is tested separately.

FIGURE 1. V_{IH}, V_{IL}, V_{OH}, V_{OL}

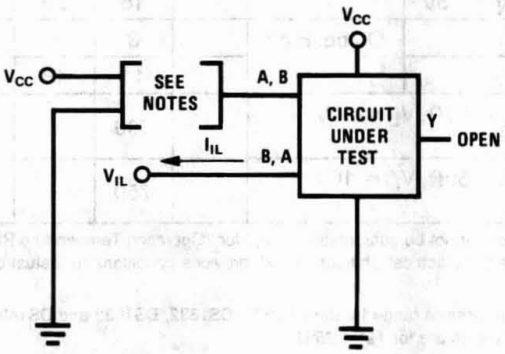
Test Circuits (Continued)



TL/F/5816–10

Each input is tested separately.

FIGURE 2. I_{IH}

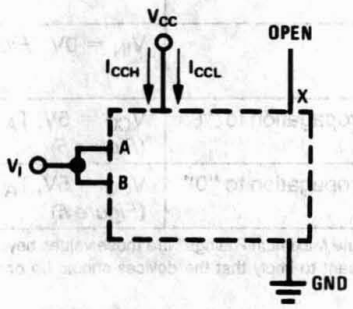


TL/F/5816–11

Note A: Each input is tested separately.

Note B: When testing DS1633 and DS1634 input not under test is grounded. For all other circuits it is at V_{CC}.

FIGURE 3. I_{IL}

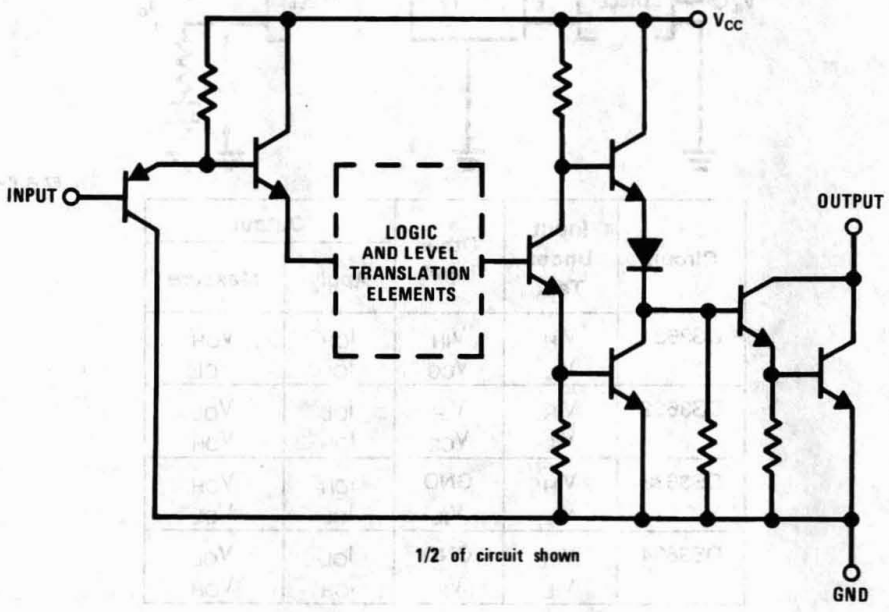


TL/F/5816–12

Both gates are tested simultaneously.

FIGURE 4. I_{CC} for AND and NAND Circuits

Schematic Diagram (Equivalent Circuit)



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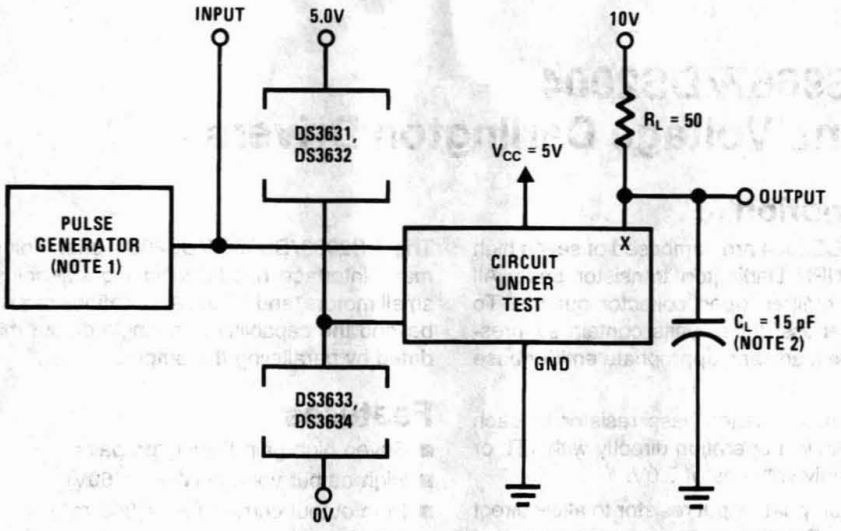
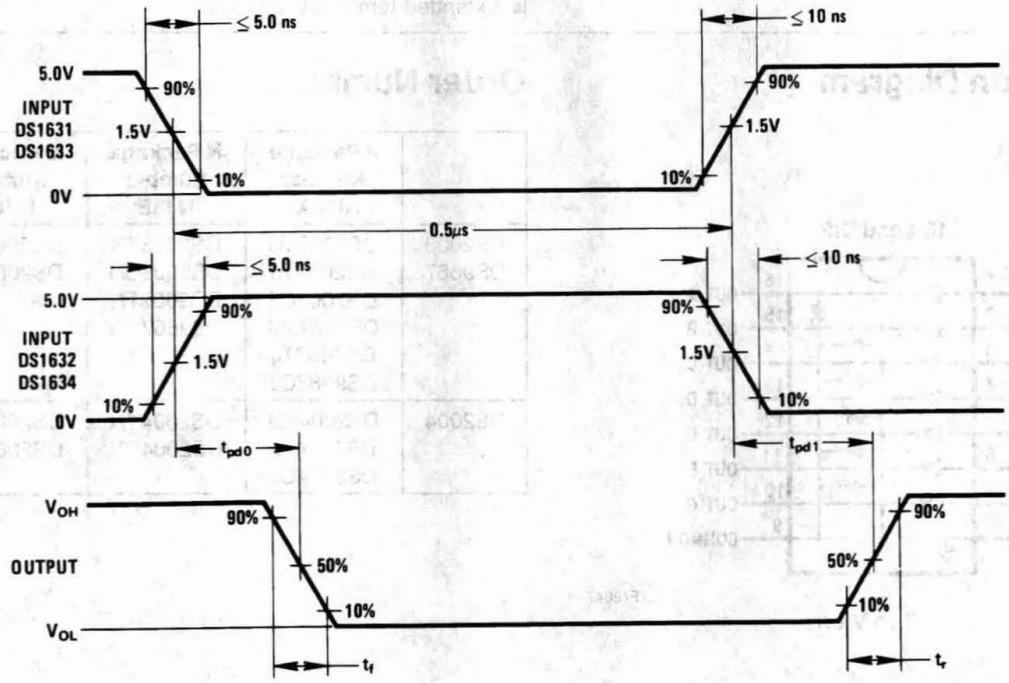
Switching Time Waveforms



TL/F/5816–13



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Note 1: The pulse generator has the following characteristics: PRR = 500 kHz, $Z_{OUT} \approx 50\Omega$

Note 2: C_L includes probe and jig capacitance

FIGURE 5. Switching Times

National Semiconductor

DS2003/DS9667/DS2004
High Current/Voltage Darlington Drivers

General Description

The DS2003/DS9667/DS2004 are comprised of seven high voltage, high current NPN Darlington transistor pairs. All units feature common emitter, open collector outputs. To maximize their effectiveness, these units contain suppression diodes for inductive loads and appropriate emitter base resistors for leakage.

The DS2003/DS9667 has a series base resistor to each Darlington pair, thus allowing operation directly with TTL or CMOS operating at supply voltages of 5.0V.

The DS2004 has an appropriate input resistor to allow direct operation from CMOS or PMOS outputs operating from supply voltages of 6.0V to 15V.

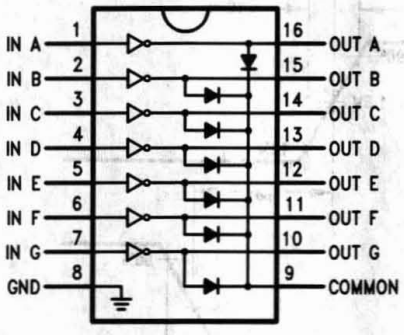
The DS2003/DS9667/DS2004 offer solutions to a great many interface needs, including solenoids, relays, lamps, small motors, and LEDs. Applications requiring sink currents beyond the capability of a single output may be accommodated by paralleling the outputs.

Features

- Seven high gain Darlington pairs
- High output voltage (V_{CE} = 50V)
- High output current (I_C = 350 mA)
- TTL, PMOS, CMOS compatible
- Suppression diodes for inductive loads
- Extended temperature range

Connection Diagram

16-Lead DIP



TL/F/9647–1

Top View

Order Numbers

	J Package Number J16A	N Package Number N16E	M Package Number M16A
DS2003 DS9667	DS2003MJ DS2003TJ DS2003CJ DS9667MJ DS9667TJ DS9667CJ	DS2003TN DS2003CN DS9667TN DS9667CN	DS2003TM DS2003CM
DS2004	DS2004MJ DS2004TJ DS2004CJ	DS2004TN DS2004CN	DS2004TM DS2004CM

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature Range
- Ceramic DIP: −65°C to +175°C
- Molded DIP: −65°C to +150°C

Operating Temperature Range
- DS2003M/DS9667M: −55°C to +125°C
- DS2004M: −55°C to +125°C
- DS2003T/DS9667T: −40°C to +105°C
- DS2004T: −40°C to +105°C
- DS2003C/DS9667C: 0°C to +85°C
- DS2004C: 0°C to +85°C

Lead Temperature
- Ceramic DIP (Soldering, 60 seconds): 300°C
- Molded DIP (Soldering, 10 seconds): 265°C

Maximum Power Dissipation* at 25°C
- Cavity Package: 2016 mW
- Molded Package: 1838 mW
- S.O. Package: 926 mW

*Derate cavity package 16.13 mW/°C above 25°C; derate molded DIP package 14.7 mW/°C above 25°C. Derate S.O. package 7.4 mW/°C.

- Input Voltage: 30V
- Output Voltage: 55V
- Emitter-Base Voltage: 6.0V
- Continuous Collector Current: 500 mA
- Continuous Base Current: 25 mA

Electrical Characteristics T_A = 25°C, unless otherwise specified (Note 2)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
I_{CEX}	Output Leakage Current	T_A = 85°C for Commercial V_{CE} = 50V *(Figure 1a)*				100	μA
		V_{CE} = 50V, V_I = 1.0V *(Figure 1b)*	DS2004			500	
$V_{CE(Sat)}$	Collector-Emitter Saturation Voltage	I_C = 350 mA, I_B = 500 μA *(Figure 2)* (Note 3)			1.25	1.6	V
		I_C = 200 mA, I_B = 350 μA *(Figure 2)*			1.1	1.3	
		I_C = 100 mA, I_B = 250 μA *(Figure 2)*			0.9	1.1	
$I_{I(ON)}$	Input Current	V_I = 3.85V *(Figure 3)*	DS2003/DS9667		0.93	1.35	mA
		V_I = 5.0V *(Figure 3)*	DS2004		0.35	0.5	
		V_I = 12V *(Figure 3)*			1.0	1.45	
$I_{I(OFF)}$	Input Current (Note 4)	T_A = 85°C for Commercial I_C = 500 μA *(Figure 4)*		50	100		μA
$V_{I(ON)}$	Input Voltage (Note 5)	V_{CE} = 2.0V, I_C = 200 mA *(Figure 5)*	DS2003/DS9667			2.4	V
		V_{CE} = 2.0V, I_C = 250 mA *(Figure 5)*				2.7	
		V_{CE} = 2.0V, I_C = 300 mA *(Figure 5)*				3.0	
		V_{CE} = 2.0V, I_C = 125 mA *(Figure 5)*	DS2004			5.0	
		V_{CE} = 2.0V, I_C = 200 mA *(Figure 5)*				6.0	
		V_{CE} = 2.0V, I_C = 275 mA *(Figure 5)*				7.0	
		V_{CE} = 2.0V, I_C = 350 mA *(Figure 5)*				8.0	
C_I	Input Capacitance				15	30	pF
t_{PLH}	Turn-On Delay	0.5 V_I to 0.5 V_O				1.0	μs
t_{PHL}	Turn-Off Delay	0.5 V_I to 0.5 V_O				1.0	μs
I_R	Clamp Diode Leakage Current	V_R = 50V *(Figure 6)*	T_A = 25°C T_A = 85°C			50 100	μA μA
V_F	Clamp Diode Forward Voltage	I_F = 350 mA *(Figure 7)*			1.7	2.0	V

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The tables of "Electrical Characteristics" provide conditions for actual device operation.

Note 2: All limits apply to the complete Darlington series except as specified for a single device type.

Note 3: Under normal operating conditions these units will sustain 350 mA per output with $V_{CE\ (Sat)}$ = 1.6V at 70°C with a pulse width of 20 ms and a duty cycle of 30%.

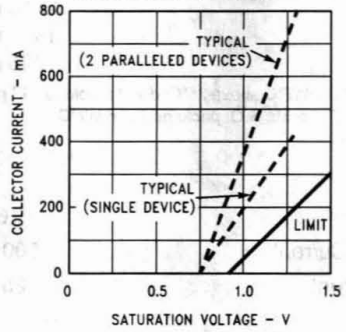
Note 4: The $I_{I(OFF)}$ current limit guaranteed against partial turn-on of the output.

Note 5: The $V_{I(ON)}$ voltage limit guarantees a minimum output sink current per the specified test conditions.

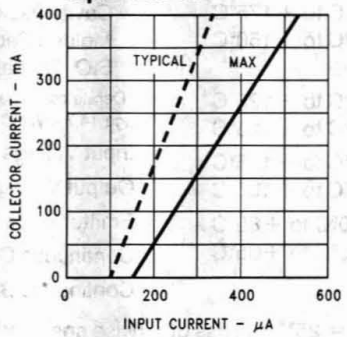
3

Typical Performance Characteristics

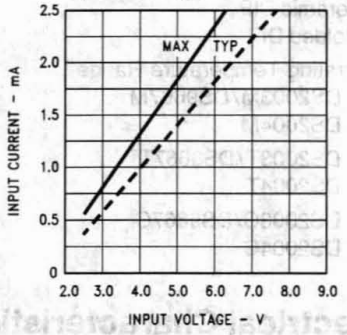
Collector Current vs Saturation Voltage



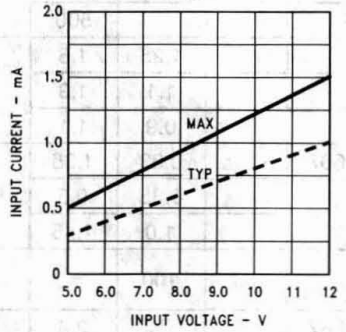
Collector Current vs Input Current



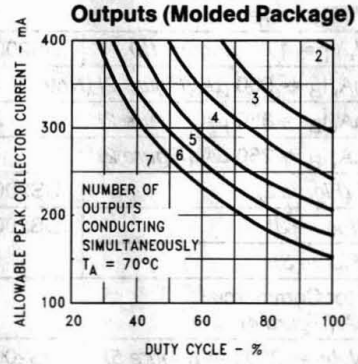
DS2003/DS9667 Input Current vs Input Voltage



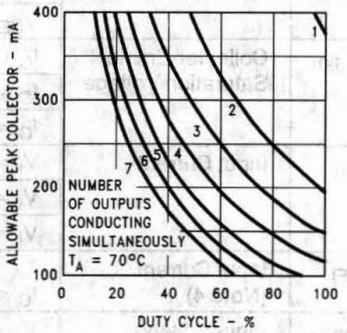
DS2004 Input Current vs Input Voltage



Peak Collector Current vs Duty Cycle and Number of Outputs (Molded Package)



Peak Collector Current vs Duty Cycle and Number of Outputs (Ceramic Package)



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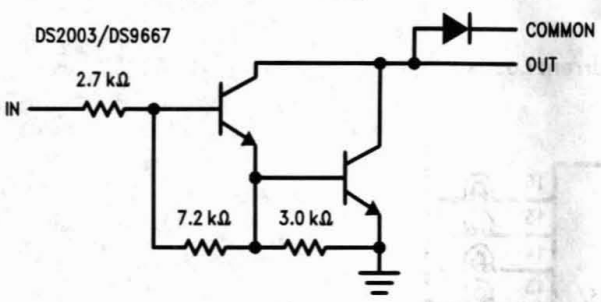
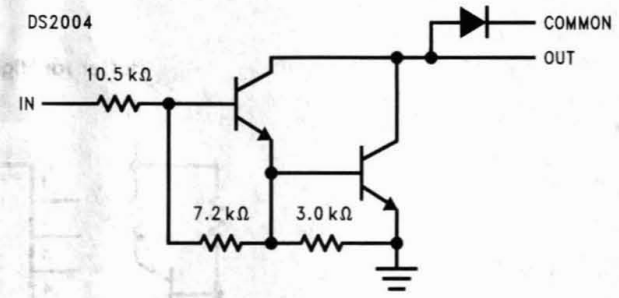
Equivalent Circuits



TL/F/9647–3



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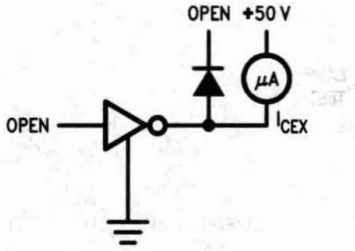
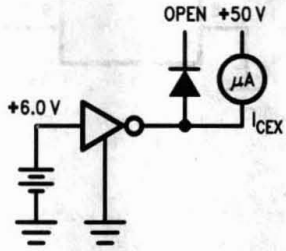
Test Circuits



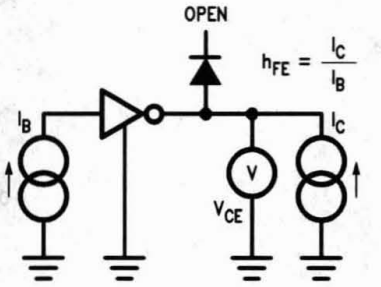
TL/F/9647–7

FIGURE 1a



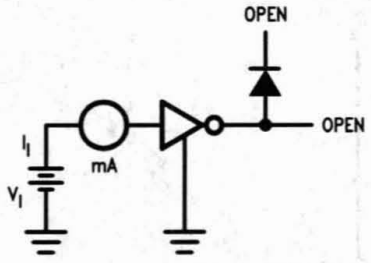
TL/F/9647–8

FIGURE 1b



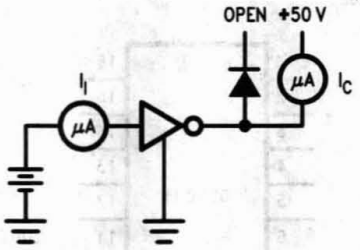
TL/F/9647–9

FIGURE 2



TL/F/9647–10

FIGURE 3



TL/F/9647–11

FIGURE 4

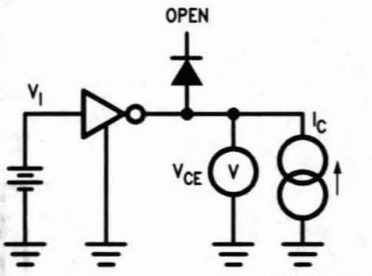


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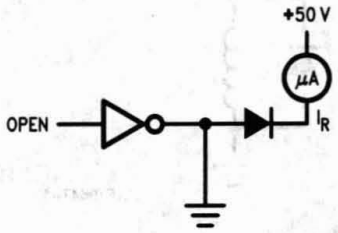
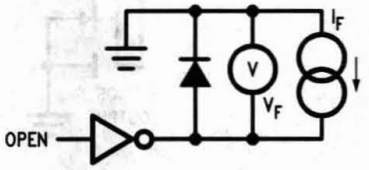
FIGURE 5



TL/F/9647–13

FIGURE 6

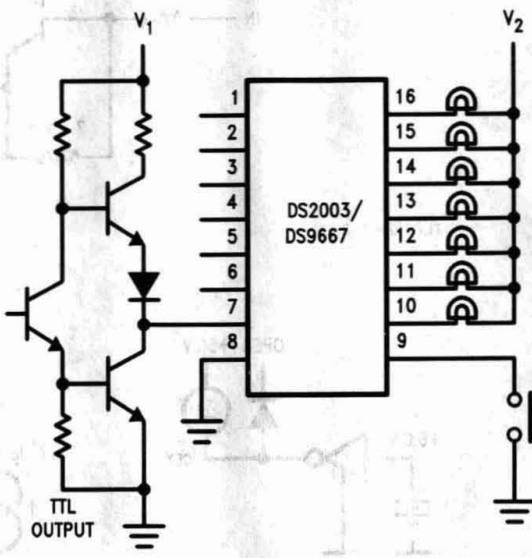


TL/F/9647–14

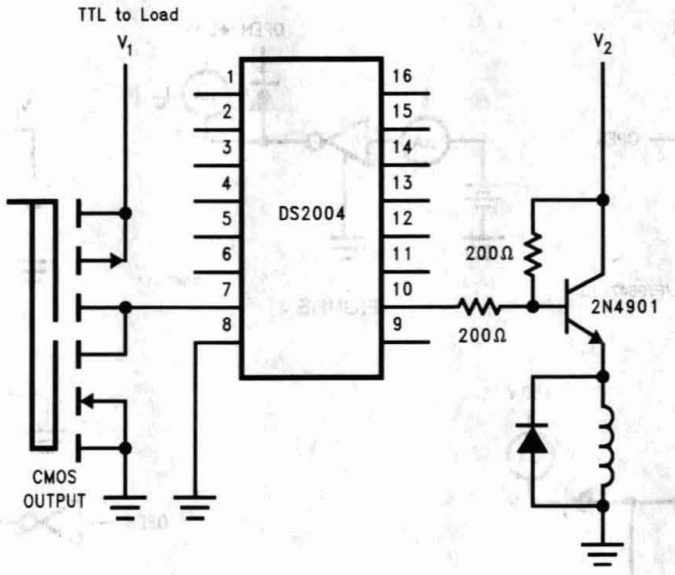
FIGURE 7

Typical Applications

Buffer for Higher Current Loads



TL/F/9647–16



TL/F/9647–17

National Semiconductor

DS3658 Quad High Current Peripheral Driver

General Description

The DS3658 quad peripheral driver is designed for those applications where low operating power, high breakdown voltage, high output current and low output ON voltage are required. A unique input circuit combines TTL compatibility with high impedance. In fact, its extreme low input current allows it to be driven directly by a CMOS device.

The outputs are capable of sinking 600 mA each and offer a 70V breakdown. However, for inductive loads the output should be clamped to 35V or less to avoid latch-up during turn off (inductive fly back protection—refer AN-213). An on-chip clamp diode capable of handling 800 mA is provided at each output for this purpose. In addition, the DS3658 incorporates circuitry that guarantees glitch-free power up or down operation and a fail-safe feature which puts the output in a high impedance state when the input is open.

The molded package is specifically constructed to allow increased power dissipation over conventional packages. The four ground pins are directly connected to the device chip with a special copper lead frame. When the quad driver is soldered into a PC board, the power rating of the device improves significantly.

Applications

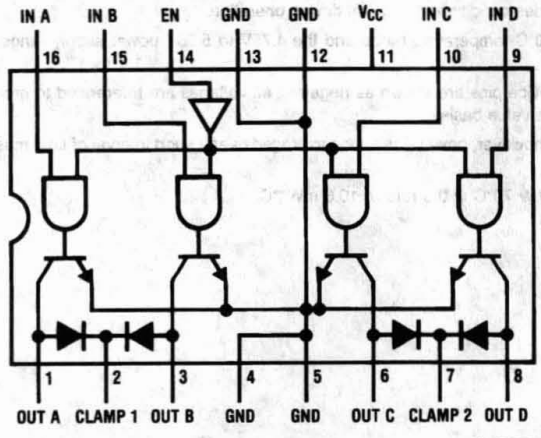
- Relay drivers
- Lamp drivers
- Solenoid drivers
- Hammer drivers
- Stepping motor drivers
- Triac drivers
- LED drivers
- High current, high voltage drivers
- Level translators
- Fiber optic LED drivers

Features

- Single saturated transistor outputs
- Low standby power, 10 mW typical
- High impedance TTL compatible inputs
- Outputs may be tied together for increased current capacity
- High output current
  600 mA per output
  2.4A per package
- No output latch-up at 35V
- Low output ON voltage (350 mV typ @ 600 mA)
- High breakdown voltage (70V)
- Open collector outputs
- Output clamp diodes for inductive fly back protection
- NPN inputs for minimal input currents (1 μA typical)
- Low operating power
- Standard 5V power supply
- Power up/down protection
- Fail safe operation
- 2W power package
- Pin-for-pin compatible with SN75437

Connection Diagram

Dual-In-Line Package



TL/F/5819–1

Top View

Order Number DS3658N
See NS Package Number N16E

Truth Table

IN	EN	OUT
H	H	L
L	H	Z
H	L	Z
L	L	Z

H = High state
L = Low state
Z = High impedance state

3

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	15V
Output Voltage	70V
Output Current	1.5A
Continuous Power Dissipation @ 25°C Free-Air (Note 5)	2075 mW
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 4 sec.)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage	4.75	5.25	V
Ambient Temperature	0	70	°C

Electrical Characteristics (Notes 2 and 3)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{IH}	Input High Voltage		2.0			V
V_{IL}	Input Low Voltage				0.8	V
I_{IH}	Input High Current	V_{IN} = 5.25V, V_{CC} = 5.25V		1.0	10	μA
I_{IL}	Input Low Current	V_{IN} = 0.4V			±10	μA
V_{IK}	Input Clamp Voltage	I_I = −12 mA		−0.8	−1.5	V
V_{OL}	Output Low Voltage	I_L = 300 mA		0.2	0.4	V
		I_L = 600 mA (Note 4)		0.35	0.7	V
I_{CEX}	Output Leakage Current	V_{CE} = 70V, V_{IN} = 0.8V			100	μA
V_F	Diode Forward Voltage	I_F = 800 mA		1.0	1.6	V
I_R	Diode Leakage Current	V_R = 70V			100	μA
I_{CC}	Supply Current	All Inputs High		60	85	mA
		All Inputs Low		2	4	mA

Switching Characteristics (Note 2)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{PHL}	Turn On Delay	R_L = 60Ω, V_L = 30V		226	500	ns
t_{PLH}	Turn Off Delay	R_L = 60Ω, V_L = 30V		2430	8000	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the device should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

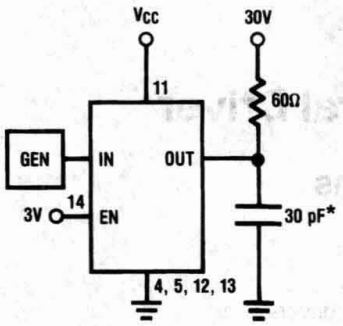
Note 2: Unless otherwise specified, min/max limits apply across the 0°C to +70°C temperature range and the 4.75V to 5.25V power supply range. All typical values are for T_A = 25°C and V_{CC} = 5.0V.

Note 3: All currents into device pins are shown as positive; all currents out of device pins are shown as negative; all voltages are referenced to ground, unless otherwise specified. All values shown as max or min are so classified on absolute value basis.

Note 4: All sections of this quad circuit may conduct rated current simultaneously; however, power dissipation averaged over a short interval of time must fall within specified continuous dissipation ratings.

Note 5: For operation over 25°C free-air temperature, derate linearly to 1328 mW @ 70°C @ the rate of 16.6 mW/°C.

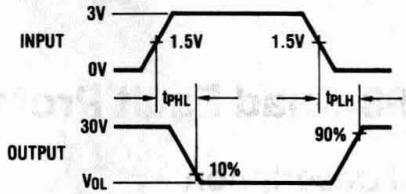
AC Test Circuit



TL/F/5819–2

*Includes probe and jig capacitance

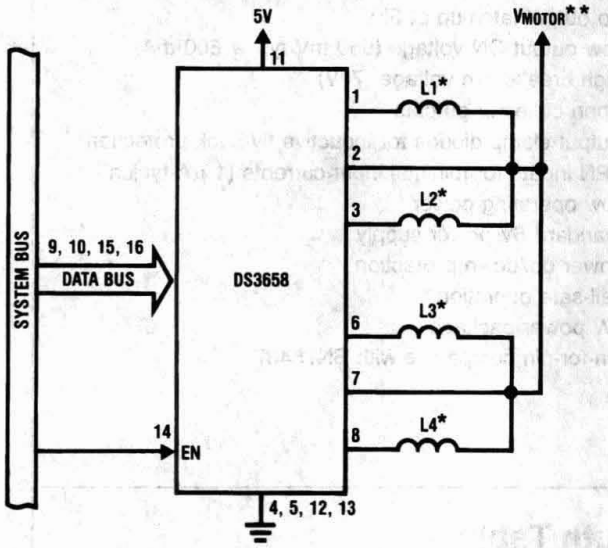
Switching Waveforms



TL/F/5819–3

Typical Applications

Stepping Motor Driver

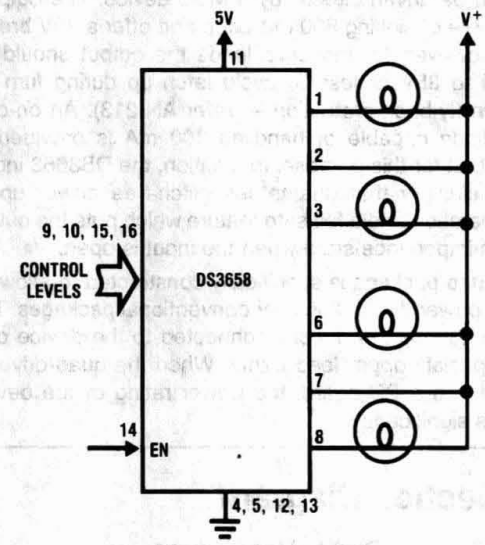


TL/F/5819–4

*L1, L2, L3, L4 are the windings of a bifilar stepping motor

**V_{MOTOR} is the supply voltage of the motor

Lamp Driver



TL/F/5819–5

National Semiconductor

DS3668 Quad Fault Protected Peripheral Driver

General Description

The DS3668 quad peripheral driver is designed for those applications where low operating power, high breakdown voltage, high output current and low output ON voltage are required. Unlike most peripheral drivers available, a unique fault protection circuit is incorporated on each output. When the load current exceeds 1.0A (approximately) on any output for more than a built-in delay time, nominally 12 μs, that output will be shut off by its protection circuitry with no effect on other outputs. This condition will prevail until that protection circuitry is reset by toggling the corresponding input or the enable pin low for at least 1.0 μs. This built-in delay is provided to ensure that the protection circuitry is not triggered by turn-on surge currents associated with certain kinds of loads.

The DS3668's inputs combine TTL compatibility with high input impedance. In fact, its extreme low input current allows it to be driven directly by a MOS device. The outputs are capable of sinking 600 mA each and offer a 70V breakdown. However, for inductive loads the output should be clamped to 35V or less to avoid latch up during turn off (inductive fly-back protection — refer AN-213). An on-chip clamp diode capable of handling 800 mA is provided at each output for this purpose. In addition, the DS3668 incorporates circuitry that guarantees glitch-free power up or down operation and a fail-safe feature which puts the output in a high impedance state when the input is open.

The molded package is specifically constructed to allow increased power dissipation over conventional packages. The four ground pins are directly connected to the device chip with a special copper lead frame. When the quad driver is soldered into a PC board, the power rating of the device improves significantly.

Applications

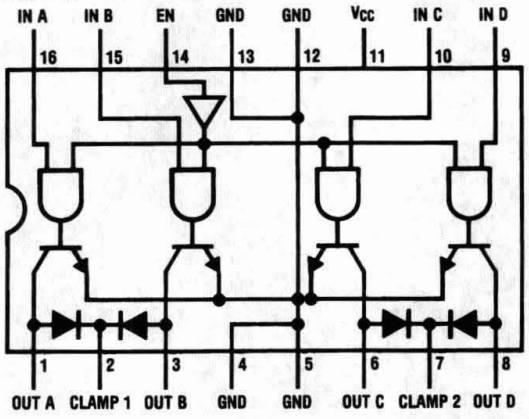
- Relay drivers
- Solenoid drivers
- Hammer drivers
- Stepping motor drivers
- Triac drivers
- LED drivers
- High current, high voltage drivers
- Level translators
- Fiber optic LED drivers

Features

- Output fault protection
- High impedance TTL compatible inputs
- High output current—600 mA per output
- No output latch-up at 35V
- Low output ON voltage (550 mV typ @ 600 mA)
- High breakdown voltage (70V)
- Open collector outputs
- Output clamp diodes for inductive fly-back protection
- NPN inputs for minimal input currents (1 μA typical)
- Low operating power
- Standard 5V power supply
- Power up/down protection
- Fail-safe operation
- 2W power package
- Pin-for-pin compatible with SN75437

Connection Diagram

Dual-In-Line Package



TL/F/5225–1

Top View

Truth Table

IN	EN	OUT
H	H	L
L	H	Z
H	L	Z
L	L	Z

H = High state

L = Low state

Z = High impedance state

Order Number DS3668N
See NS Package Number N16E

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7.0V
Input Voltage	15V
Output Voltage	70V
Continuous Power Dissipation @ 25°C Free-Air(5)	2075 mW
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 4 seconds)	260

Operating Conditions

	Min	Max	Units
Supply Voltage	4.75	5.25	V
Ambient Temperature	0	70	°C

Electrical Characteristics (Notes 2 and 3)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{IH}	Input High Voltage		2.0			V
V_{IL}	Input Low Voltage				0.8	V
I_{IH}	Input High Current	V_{IN} = 5.25V, V_{CC} = 5.25V		1.0	20	μA
I_{IL}	Input Low Current	V_{IN} = 0.4V			±10	μA
V_{IK}	Input Clamp Voltage	I_I = −12 mA		−0.8	−1.5	V
V_{OL}	Output Low Voltage	I_L = 300 mA		0.2	0.7	V
		I_L = 600 mA (Note 4)		0.55	1.5	V
I_{CEX}	Output Leakage Current	V_{CE} = 70V, V_{IN} = 0.8V			100	μA
V_F	Diode Forward Voltage	I_F = 800 mA		1.2	1.6	V
I_R	Diode Leakage Current	V_R = 70V			100	μA
I_{CC}	Supply Current	All Inputs High		62	80	mA
		All Inputs Low		20		mA
I_{TH}	Protection Circuit Threshold Current			1	1.4	A

Switching Characteristics (Note 2)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{PHL}	Turn On Delay	R_L = 60Ω, V_L = 30V		0.3	1.0	μs
t_{PLH}	Turn Off Delay	R_L = 60Ω, V_L = 30V		2	10.0	μs
t_{FZ}	Protection Enable Delay (after Detection of Fault)		6	12		μs
t_{RL}	Input Low Time for Protection Circuit Reset		1.0			μs

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the device should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

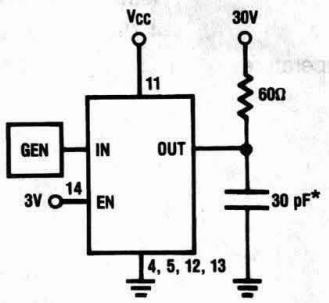
Note 2: Unless otherwise specified, min/max limits apply across the 0°C to +70°C temperature range and the 4.75V to 5.25V power supply range. All typical values are for T_A = 25°C and V_{CC} = 5.0V.

Note 3: All currents into device pins are shown as positive; all currents out of device pins are shown as negative; all voltages are referenced to ground, unless otherwise specified. All values shown as max or min are so classified on absolute value basis.

Note 4: All sections of this quad circuit may conduct rated current simultaneously; however, power dissipation averaged over a short interval of time must fall within specified continuous dissipation ratings.

Note 5: For operation over 25°C free-air temperature, derate linearly to 1328 mW @ 70°C @ the rate of 16.6 mW/°C.

AC Test Circuit



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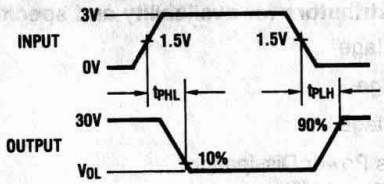
*Includes probe and jig capacitance.

Switching Waveforms



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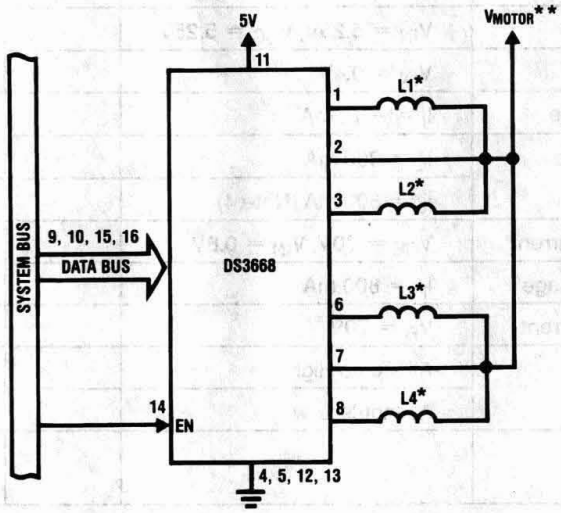
Typical Application

Stepping Motor Driver



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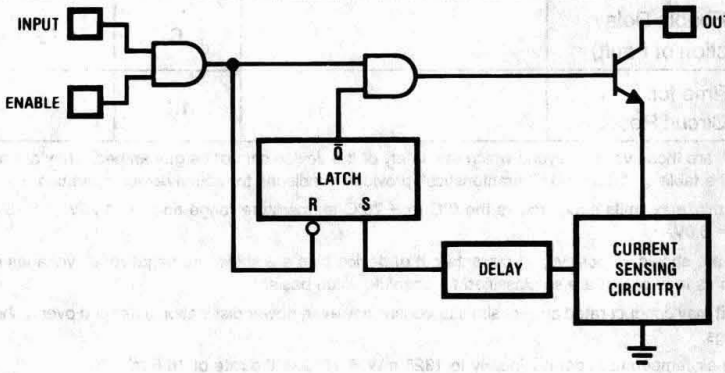
*L1, L2, L3, L4 are the windings of a bifilar stepping motor.

**V_{MOTOR} is the supply voltage of the motor.

Protection Circuit Block Diagram



TL/F/5225–5

National Semiconductor

DS3680 Quad Negative Voltage Relay Driver

General Description

The DS3680 is a quad high voltage negative relay driver designed to operate over wide ranges of supply voltage, common-mode voltage, and ambient temperature, with 50 mA sink capability. These drivers are intended for switching the ground end of loads which are directly connected to the negative supply, such as in telephone relay systems.

Since there may be considerable noise and IR drop between logic ground and negative supply ground in many applications, these drivers are designed to operate with a high common-mode range (±20V referenced to negative supply ground). Each driver has a common-mode range separate from the other drivers in the package, which pemits input signals from more than one element of the system.

With low differential input current requirements (typically 100 μA), these drivers are compatible with TTL, LS and CMOS logic. Differential inputs permit either inverting or non-inverting operation.

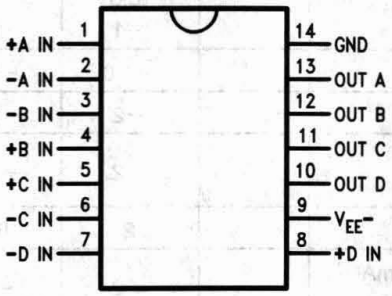
The driver outputs incorporate transient suppression clamp networks, which eliminate the need for external networks when used in applications of switching inductive loads. A fail-safe feature is incorporated to insure that, if the +IN input or both inputs are open, the driver will be OFF.

Features

- −10V to −60V operation
- Quad 50 mA sink capability
- TTL/LS/COMS or voltage comparator input
- High input common-mode voltage range
- Very low input current
- Fail-safe disconnect feature
- Built-in output clamp diode

Connection Diagram

Dual-In-Line Package

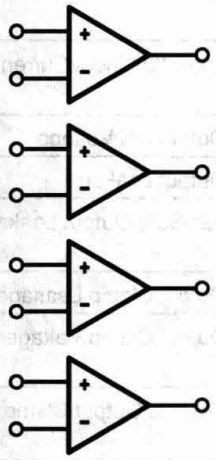


TL/F/5821–1

Top View

Order Number DS3680J, DS3680M or DS3680N
See NS Package Number J14A, M14A, N14A

Logic Diagram



TL/F/5821–2

Truth Table

Differential Inputs	Outputs
$V_{ID} \geq 2V$	On
$V_{ID} \leq 0.8V$	Off
Open	Off

3

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (GND to $V_{EE}-$, and Any Pin)	−70V
Positive Input Voltage (Input to GND)	20V
Negative Input Voltage (Input to $V_{EE}-$)	−5V
Differential Voltage (+IN to −IN)	±20V
Inductive Load	$L_L \leq 5h$
	$I_L \leq 50$ mA
Output Current	−100 mA
Storage Temperature	−65°C to +150°C
Maximum Power Dissipation* at 25°C	
Cavity Package	1433 mW
Molded Dip Package	1398 mW
SO Package	1002 mW
Lead Temperature (Soldering, 4 seconds)	260°C

* Derate cavity package 9.6 mW/°C above 25°C; derate molded dip package 11.2 mW/°C above 25°C; derate SO package 8.02 mW/°C above 25°C.

Recommended Operating Conditions

	Min	Max	Units
Supply Voltage (GND to $V_{EE}-$)	−10	−60	V
Input Voltage (Input to GND)	−20	20	V
Logic ON Voltage (+IN) Referenced to −IN	2	20	V
Logic OFF Voltage (+IN) Referenced to −IN	−20	0.8	V
Temperature Range	−25	+85	°C

Electrical Characteristics (Notes 2 and 3)

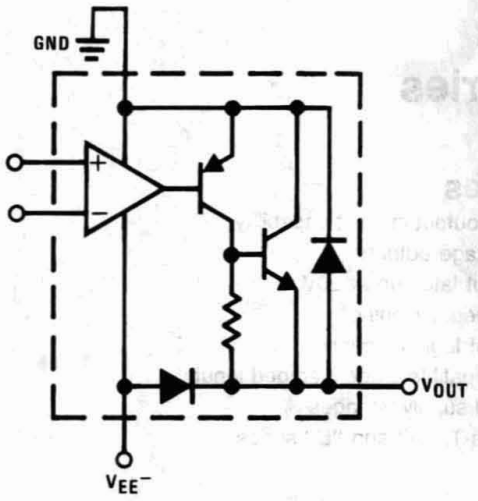
Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{IH}	Logic "1" Input Voltage		2.0	1.3		V
V_{IL}	Logic "0" Input Voltage			1.3	0.8	V
I_{INH}	Logic "1" Input Current	V_{IN} = 2V V_{IN} = 7V		40 375	100 1000	μA μA
I_{INL}	Logic "0" Input Current	V_{IN} = 0.4V V_{IN} = −7V		−0.01 −1	−5 −100	μA μA
V_{OL}	Output ON Voltage	I_{OL} = 50 mA		−1.6	−2.1	V
I_{OFF}	Output Leakage	$V_{OUT} = V_{EE}-$		−2	−100	μA
I_{FS}	Fail-Safe Output Leakage	$V_{OUT} = V_{EE}-$ (Inputs Open)		−2	−100	μA
I_{LC}	Output Clamp Leakage Current	V_{OUT} = GND		2	100	μA
V_C	Output Clamp Voltage	I_{CLAMP} = −50 mA Referenced to $V_{EE}-$		−2	−1.2	V
V_P	Positive Output Clamp Voltage	I_{CLAMP} = 50 mA Referenced to GND		0.9	1.2	V
$I_{EE(ON)}$	ON Supply Current	All Drivers ON		−2	−4.4	mA
$I_{EE(OFF)}$	OFF Supply Current	All Drivers OFF		−1	−100	μA
$t_{PD(ON)}$	Propagation Delay to Driver ON	L = 1h, R_L = 1k, V_{IN} = 3V Pulse		1	10	μs
$t_{PD(OFF)}$	Propagation Delay to Driver OFF	L = 1h, R_L = 1k, V_{IN} = 3V Pulse		1	10	μs

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range", they are not meant to imply that the device should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

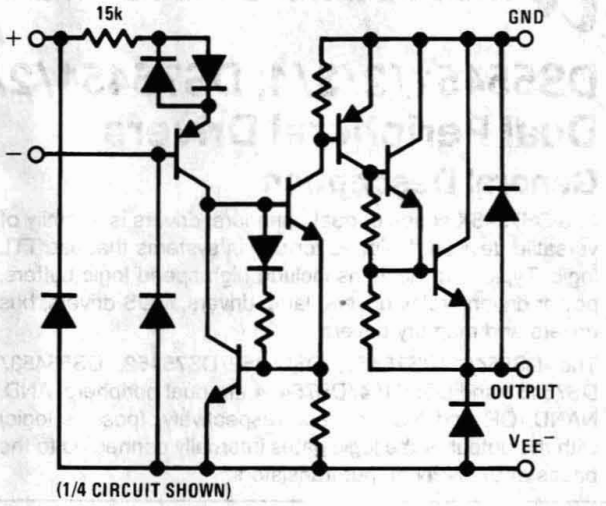
Note 2: Unless otherwise specified, the min/max limits of the table of "Electrical Characteristics" apply within the range of the table of "Operating Conditions". All typical values are given for $V_{EE}-$ = 52V, and T_A = 25°C.

Note 3: All current into device pins shown as positive, out of the device as negative. All voltages are referenced to ground unless otherwise noted.

Schematic Diagrams



TL/F/5821–3



TL/F/5821–4

National Semiconductor

DS55451/2/3/4, DS75451/2/3/4 Series Dual Peripheral Drivers

General Description

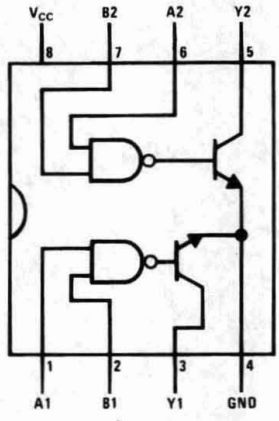
The DS7545X series of dual peripheral drivers is a family of versatile devices designed for use in systems that use TTL logic. Typical applications include high speed logic buffers, power drivers, relay drivers, lamp drivers, MOS drivers, bus drivers and memory drivers.

The DS55451/DS75451, DS55452/DS75452, DS55453/DS75453 and DS55454/DS75454 are dual peripheral AND, NAND, OR and NOR drivers, respectively, (positive logic) with the output of the logic gates internally connected to the bases of the NPN output transistors.

Features

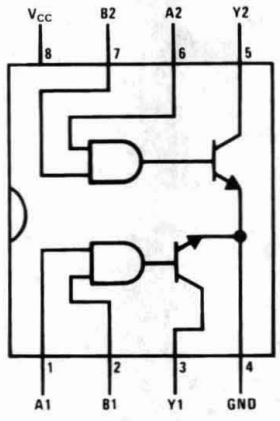
- 300 mA output current capability
- High voltage outputs
- No output latch-up at 20V
- High speed switching
- Choice of logic function
- TTL compatible diode-clamped inputs
- Standard supply voltages
- Replaces TI "A" and "B" series

Connection Diagrams (Dual-In-Line and Metal Can Packages)



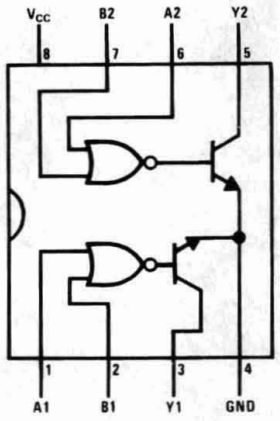
TL/F/5824–2

Top View
Order Number DS55451J-8, DS75451M or DS75451N



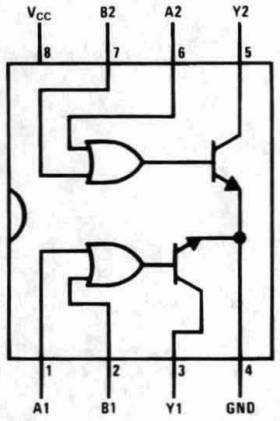
TL/F/5824–3

Top View
Order Number DS55452J-8, DS75452M or DS75452N



TL/F/5824–4

Top View
Order Number DS55453J-8, DS75453M or DS75453N

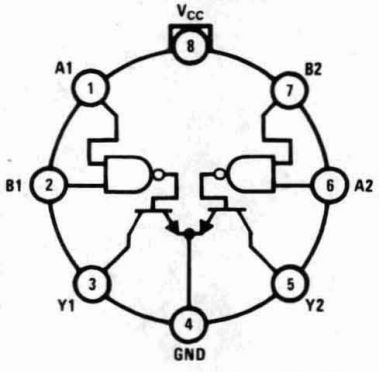


TL/F/5824–5

Top View
Order Number DS55454J-8, DS75454M or DS75454N

See NS Package Numbers J08A, M08A* or N08E

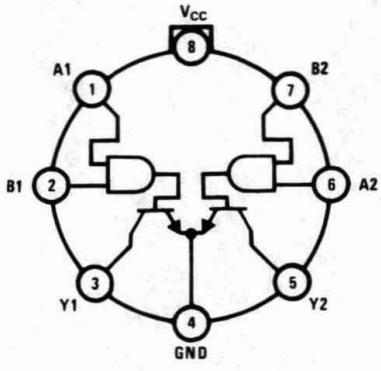
*See Note 5 and Appendix E regarding S.O. package power dissipation constraints.



TL/F/5824–6

Top View

Order Number DS55451H

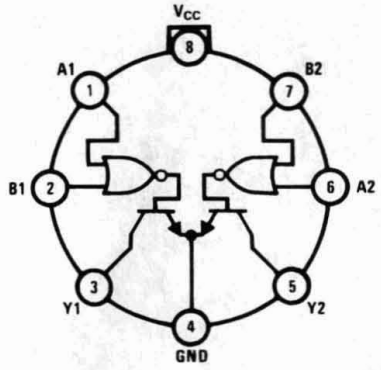


TL/F/5824–7

Top View

(Pin 4 is in Electrical Contact with the Case)

Order Number DS55452H



TL/F/5824–8

Top View

Order Number DS55453H

See NS Package Number H08C

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage, (V_{CC}) (Note 2)	7.0V
Input Voltage	5.5V
Inter-Emitter Voltage (Note 3)	5.5V
Output Voltage (Note 4)	
DS55451/DS75451, DS55452/DS75452, DS55453/DS75453, DS55454/DS75454	30V
Output Current (Note 5)	
DS55451/DS75451, DS55452/DS75452, DS55453/DS75453, DS55454/DS75454	300 mA
DS75451/2/3/4 Maximum Power (Note 5)	
Dissipation† at 25°C	
Cavity Package	1090 mW
Molded DIP Package	957 mW
TO-5 Package	760 mW
SO Package	632 mW
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 4 sec.)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage, (V_{CC})			
DS5545X	4.5	5.5	V
DS7545X	4.75	5.25	V
Temperature, (T_A)			
DS5545X	−55	+125	°C
DS7545X	0	+70	°C

† Derate cavity package 7.3 mW/°C above 25°C; derate molded package 7.7 mW/°C above 25°C; derate TO-5 package 5.1 mW/°C above 25°C; derate SO package 7.56 mW/°C above 25°C.

Electrical Characteristics

DS55451/DS75451, DS55452/DS75452, DS55453/DS75453, DS55454/DS75454 (Notes 6 and 7)

Symbol	Parameter	Conditions				Min	Typ	Max	Units
V_{IH}	High-Level Input Voltage	*(Figure 7)*				2			V
V_{IL}	Low-Level Input Voltage							0.8	V
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA						−1.5	V
V_{OL}	Low-Level Output Voltage	V_{CC} = Min, *(Figure 7)*	V_{IL} = 0.8V	I_{OL} = 100 mA	DS55451, DS55453		0.25	0.5	V
					DS75451, DS75453		0.25	0.4	V
				I_{OL} = 300 mA	DS55451, DS55453		0.5	0.8	V
					DS75451, DS75453		0.5	0.7	V
			V_{IH} = 2V	I_{OL} = 100 mA	DS55452, DS55454		0.25	0.5	V
					DS75452, DS75454		0.25	0.4	V
				I_{OL} = 300 mA	DS55452, DS55454		0.5	0.8	V
					DS75452, DS75454		0.5	0.7	V
I_{OH}	High-Level Output Current	V_{CC} = Min, *(Figure 7)*	V_{OH} = 30V	V_{IH} = 2V	DS55451, DS55453			300	μA
					DS75451, DS75453			100	μA
				V_{IL} = 0.8V	DS55452, DS55454			300	μA
					DS75452, DS75454			100	μA
I_I	Input Current at Maximum Input Voltage	V_{CC} = Max, V_I = 5.5V, *(Figure 9)*						1	mA
I_{IH}	High-Level Input Current	V_{CC} = Max, V_I = 2.4V, *(Figure 9)*						40	μA
I_{IL}	Low-Level Input Current	V_{CC} = Max, V_I = 0.4V, *(Figure 8)*					−1	−1.6	mA
I_{CCH}	Supply Current, Outputs High	V_{CC} = Max, *(Figure 10)*	V_I = 5V		DS55451/DS75451		7	11	mA
			V_I = 0V		DS55452/DS75452		11	14	mA
			V_I = 5V		DS55453/DS75453		8	11	mA
			V_I = 0V		DS55454/DS75454		13	17	mA
I_{CCL}	Supply Current, Outputs Low	V_{CC} = Max, *(Figure 10)*	V_I = 0V		DS55451/DS75451		52	65	mA
			V_I = 5V		DS55452/DS75452		56	71	mA
			V_I = 0V		DS55453/DS75453		54	68	mA
			V_I = 5V		DS55454/DS75454		61	79	mA

3

Switching Characteristics

DS55451/DS75451, DS55452/DS75452, DS55453/DS75453, DS55454/DS75454 (V_{CC} = 5V, T_A = 25°C)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	C_L = 15 pF, R_L = 50Ω, $I_O \approx$ 200 mA, *(Figure 14)*	DS55451/DS75451		18	25	ns
			DS55452/DS75452		26	35	ns
			DS55453/DS75453		18	25	ns
			DS55454/DS75454		27	35	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output	C_L = 15 pF, R_L = 50Ω, $I_O \approx$ 200 mA, *(Figure 14)*	DS55451/DS75451		18	25	ns
			DS55452/DS75452		24	35	ns
			DS55453/DS75453		16	25	ns
			DS55454/DS75454		24	35	ns
t_{TLH}	Transition Time, Low-to-High Level Output	C_L = 15 pF, R_L = 50Ω, $I_O \approx$ 200mA, *(Figure 14)*			5	8	ns
t_{THL}	Transition Time, High-to-Low Level Output	C_L = 15 pF, R_L = 50Ω, $I_O \approx$ 200 mA, *(Figure 14)*			7	12	ns
V_{OH}	High-Level Output Voltage after Switching	V_S = 20V, $I_O \approx$ 300 mA, *(Figure 15)*		V_S − 6.5			mV

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Voltage values are with respect to network ground terminal unless otherwise specified.

Note 3: The voltage between two emitters of a multiple-emitter transistor.

Note 4: The maximum voltage which should be applied to any output when it is in the "OFF" state.

Note 5: Both halves of these dual circuits may conduct rated current simultaneously; however, power dissipation averaged over a short time interval must fall within the continuous dissipation rating.

Note 6: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DS55450 series and across the 0°C to +70°C range for the DS7545X series. All typicals are given for V_{CC} = +5V and T_A = 25°C.

Note 7: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

Truth Tables (H = high level, L = low level)

DS55451/DS75451

A	B	Y
L	L	L (ON State)
L	H	L (ON State)
H	L	L (ON State)
H	H	H (OFF State)

DS55453/DS75453

A	B	Y
L	L	L (ON State)
L	H	H (OFF State)
H	L	H (OFF State)
H	H	H (OFF State)

DS55452/DS75452

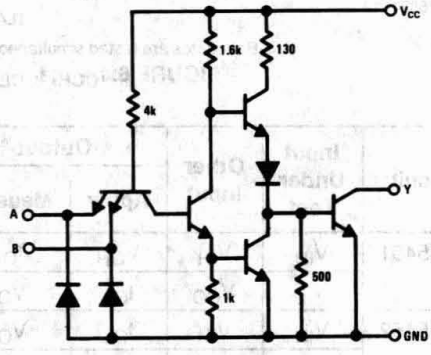
A	B	Y
L	L	H (OFF State)
L	H	H (OFF State)
H	L	H (OFF State)
H	H	L (ON State)

DS55454/DS75454

A	B	Y
L	L	H (OFF State)
L	H	L (ON State)
H	L	L (ON State)
H	H	L (ON State)

Schematic Diagrams

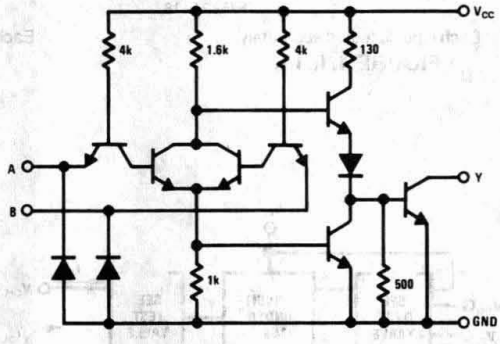
DS55451/DS75451



TL/F/5824–11

Resistor values shown are nominal.

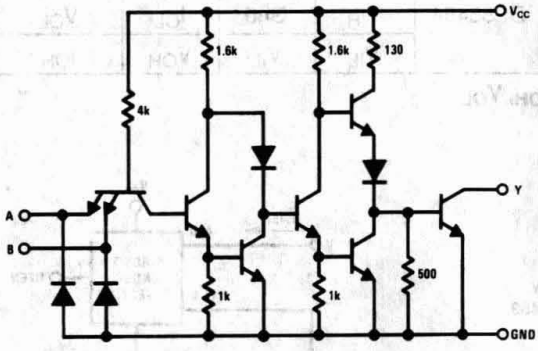
DS55453/DS75453



TL/F/5824–13

Resistor values shown are nominal.

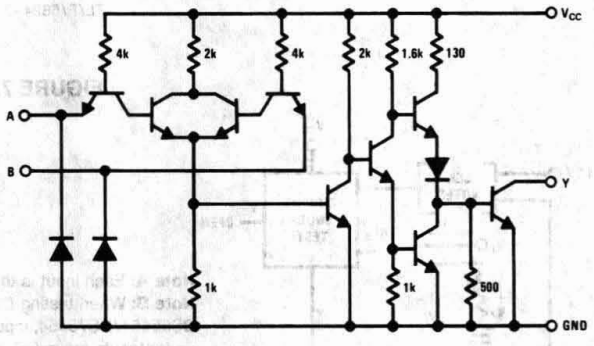
DS55452/DS75452



TL/F/5824–12

Resistor values shown are nominal.

DS55454/DS75454

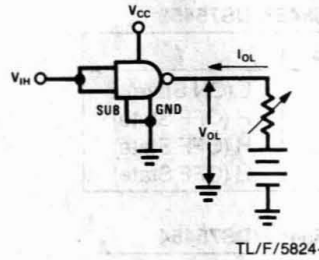


TL/F/5824–14

Resistor values shown are nominal.

3

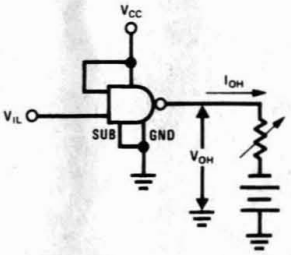
DC Test Circuits



TL/F/5824–15

Both inputs are tested simultaneously.

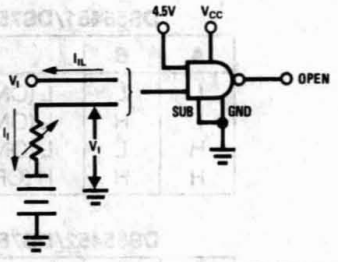
FIGURE 1. V_{IH}, V_{OL}



TL/F/5824–16

Each input is tested separately.

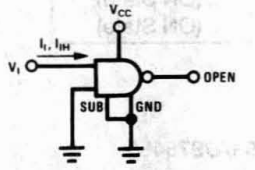
FIGURE 2. V_{IL}, V_{OH}



TL/F/5824–17

Each input is tested separately.

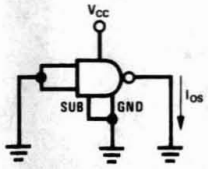
FIGURE 3. V_I, I_{IL}



TL/F/5824–18

Each input is tested separately.

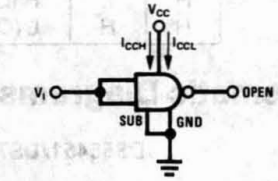
FIGURE 4. I_I, I_{IH}



TL/F/5824–19

Each input is tested separately.

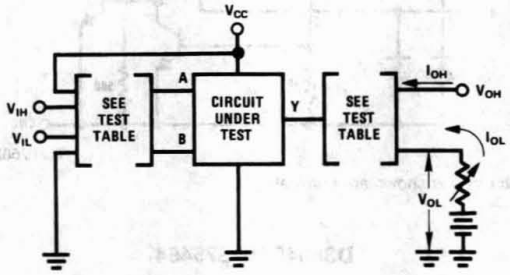
FIGURE 5. I_{OS}



TL/F/5824–20

Both gates are tested simultaneously.

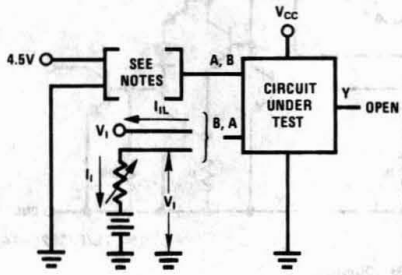
FIGURE 6. I_{CCH}, I_{CCL}



TL/F/5824–21

Circuit	Input Under Test	Other Input	Output	
			Apply	Measure
DS55451	V_{IH}	V_{IH}	V_{OH}	I_{OH}
	V_{IL}	V_{CC}	I_{OL}	V_{OL}
DS55452	V_{IH}	V_{IH}	I_{OL}	V_{OL}
	V_{IL}	V_{CC}	V_{OH}	I_{OH}
DS55453	V_{IH}	Gnd	V_{OH}	I_{OH}
	V_{IL}	V_{IL}	I_{OL}	V_{OH}
DS55454	V_{IH}	Gnd	I_{OL}	V_{OL}
	V_{IL}	V_{IL}	V_{OH}	I_{OH}

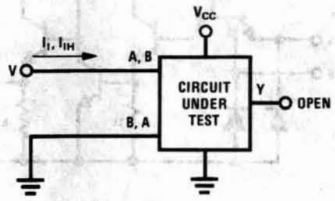
FIGURE 7. V_{IH}, V_{IL}, I_{OH}, V_{OL}



Note A: Each input is tested separately.
Note B: When testing DS55453/DS75453, DS55454/DS75454, input not under test is grounded. For all other circuits it is at 4.5V.

TL/F/5824–22

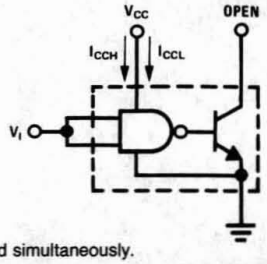
FIGURE 8. V_I, V_{IL}



Each input is tested separately.

TL/F/5824–23

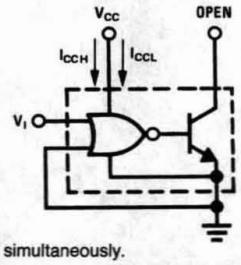
FIGURE 9. I_I, I_{IH}



Both gates are tested simultaneously.

TL/F/5824–24

FIGURE 10. I_{CCH}, I_{CCL} for AND, NAND Circuits

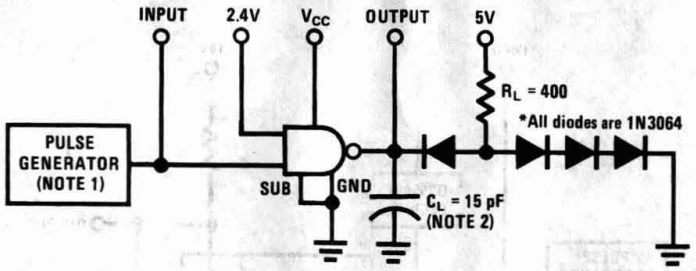


Both gates are tested simultaneously.

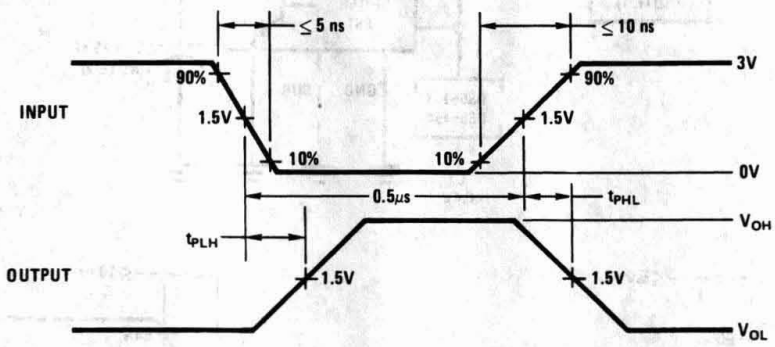
TL/F/5824–25

FIGURE 11. I_{CCH}, I_{CCL} for OR, NOR Circuits

AC Test Circuits and Switching Time Waveforms



TL/F/5824–26

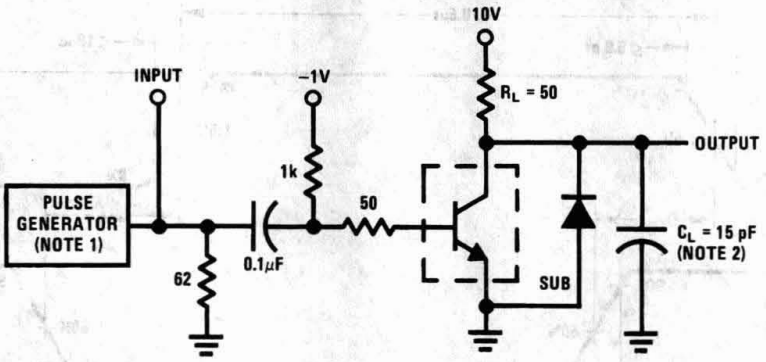


TL/F/5824–27

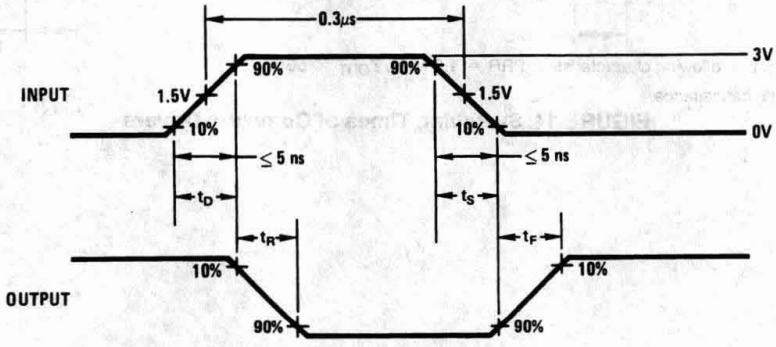
Note 1: The pulse generator has the following characteristics: PRR = 1 MHz, $Z_{OUT} \approx 50\Omega$.

Note 2: C_L includes probe and jig capacitance.

FIGURE 12. Propagation Delay Times, Each Gate



TL/F/5824–28



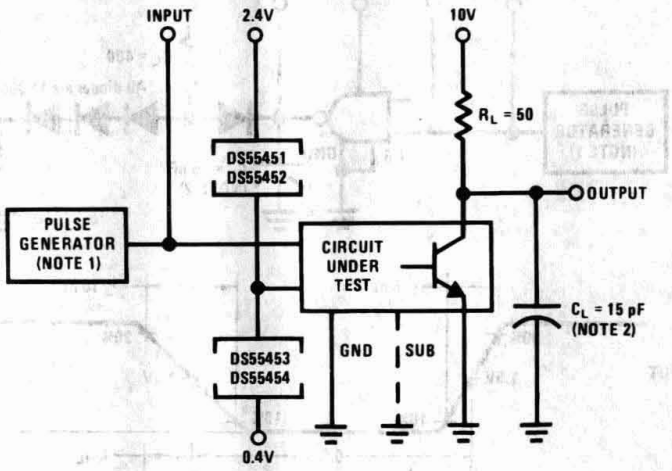
TL/F/5824–29

Note 1: The pulse generator has the following characteristics: duty cycle ≤ 1%, $Z_{OUT} \approx 50\Omega$.

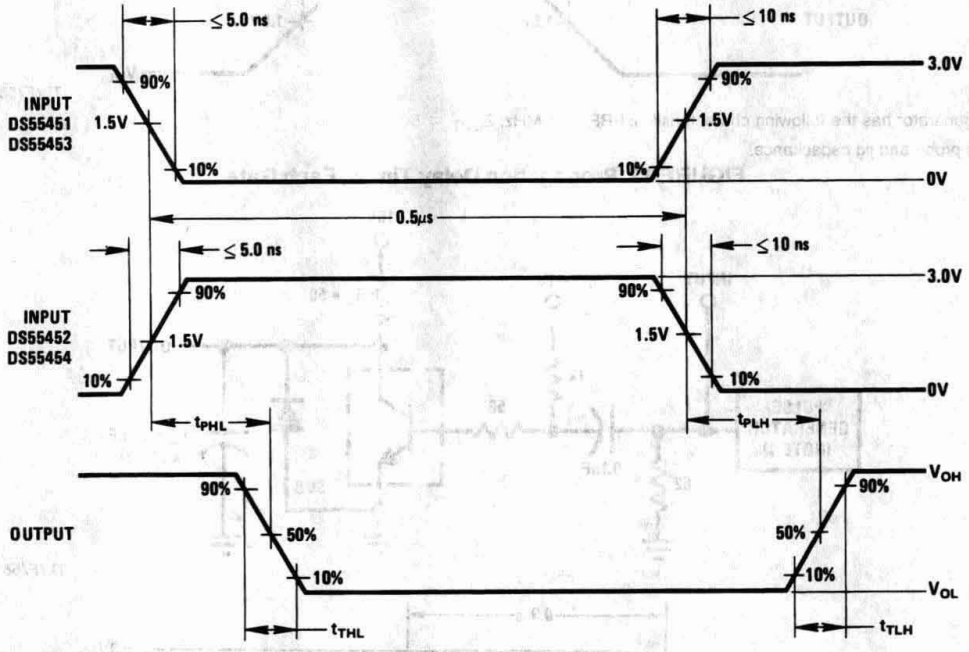
Note 2: C_L includes probe and jig capacitance.

FIGURE 13. Switching Times, Each Transistor

AC Test Circuits and Switching Time Waveforms (Continued)



TL/F/5824–30



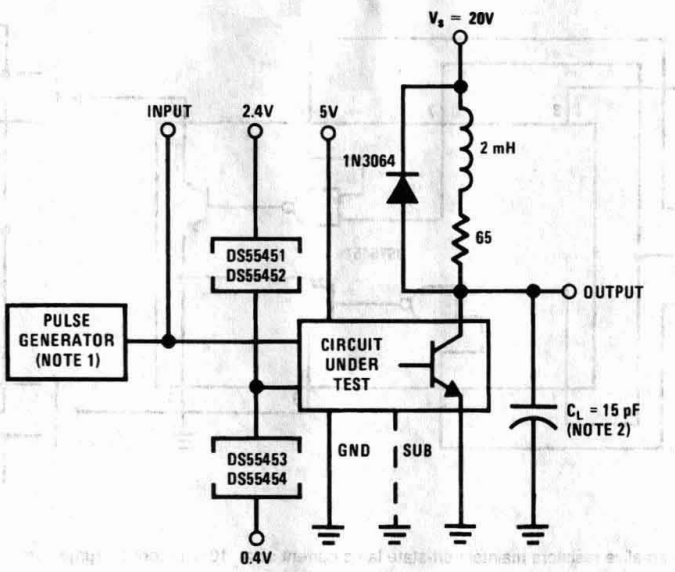
TL/F/5824–31

Note 1: The pulse generator has the following characteristics: PRR = 1.0 MHz, $Z_{OUT} \approx 50\Omega$.

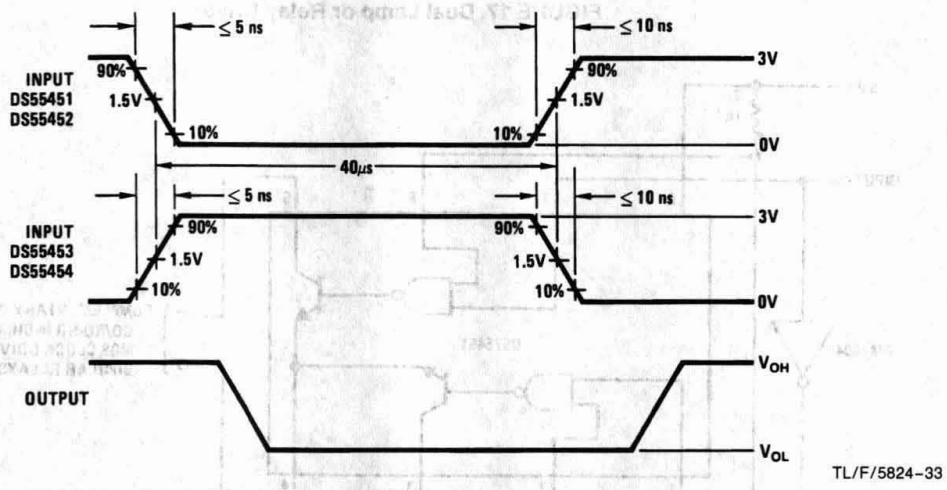
Note 2: C_L includes probe and jig capacitance.

FIGURE 14. Switching Times of Complete Drivers

AC Test Circuits and Switching Time Waveforms (Continued)



TL/F/5824–32



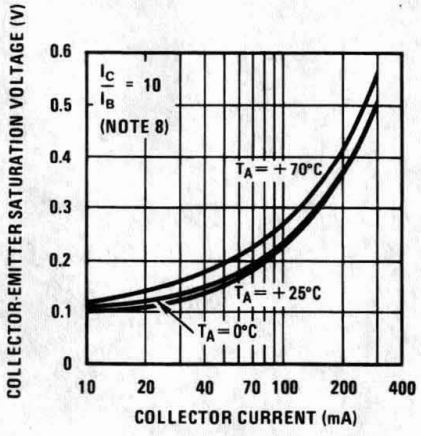
TL/F/5824–33

Note 1: The pulse generator has the following characteristics: PRR = 12.5 kHz, $Z_{OUT} \approx 50\Omega$.

Note 2: C_L includes probe and jig capacitance.

FIGURE 15. Latch-UP Test of Complete Drivers

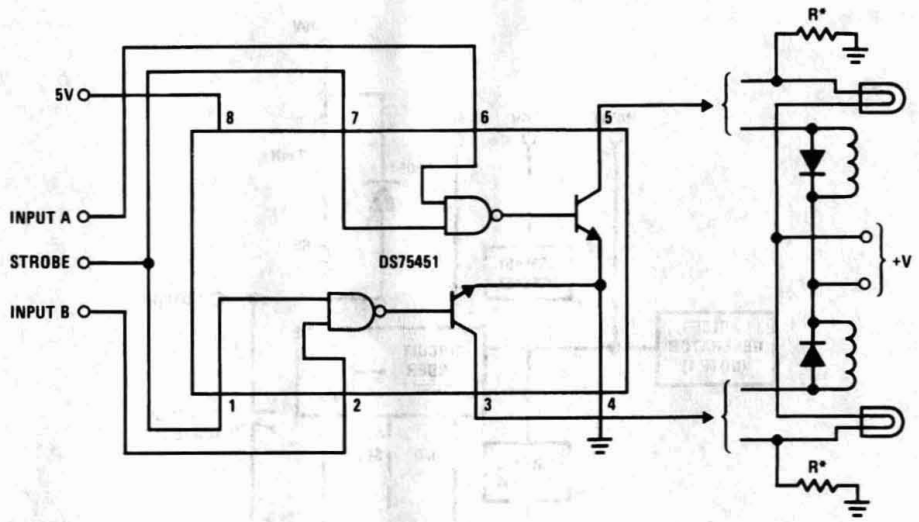
Typical Performance Characteristics



TL/F/5824–37

FIGURE 16. Transistor Collector-Emitter Saturation Voltage vs Collector Current

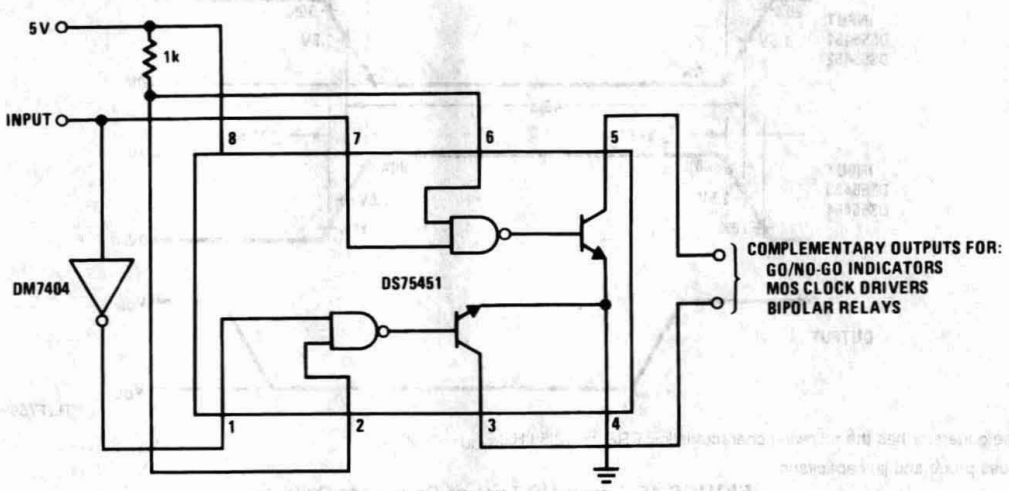
Typical Applications



TL/F/5824–46

*Optional keep-alive resistors maintain off-state lamp current at ≈ 10% to reduce surge current.

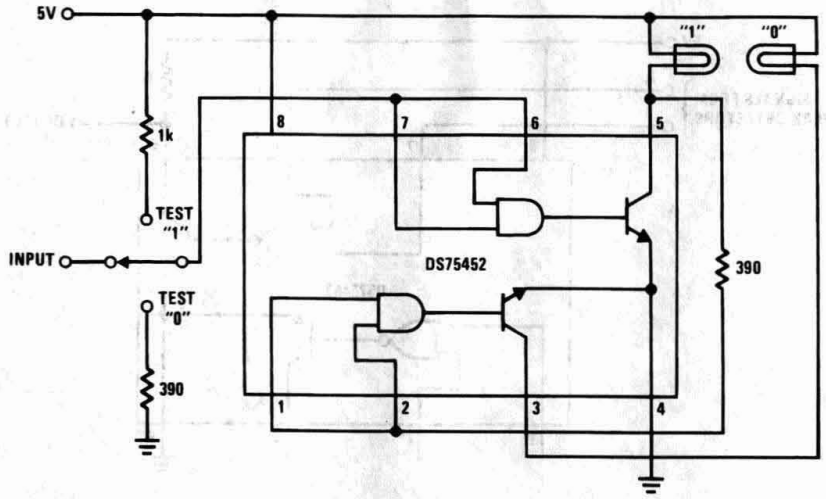
FIGURE 17. Dual Lamp or Relay Driver



TL/F/5824–47

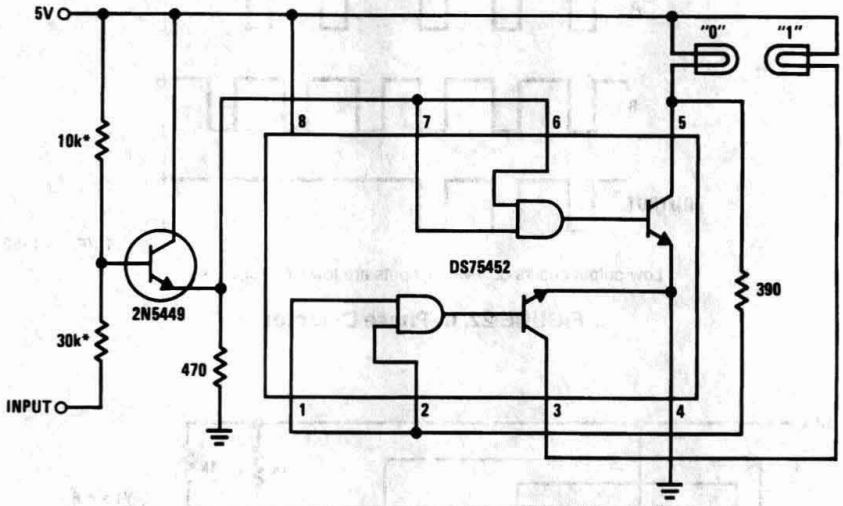
FIGURE 18. Complementary Driver

Typical Applications (Continued)



TL/F/5824–48

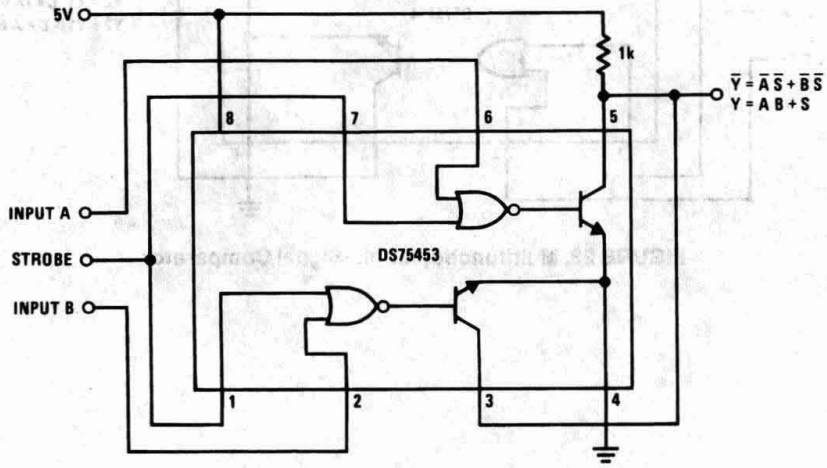
FIGURE 19. TTL or DTL Positive Logic-Level Detector



TL/F/5824–49

*The two input resistors must be adjusted for the level of MOS input.

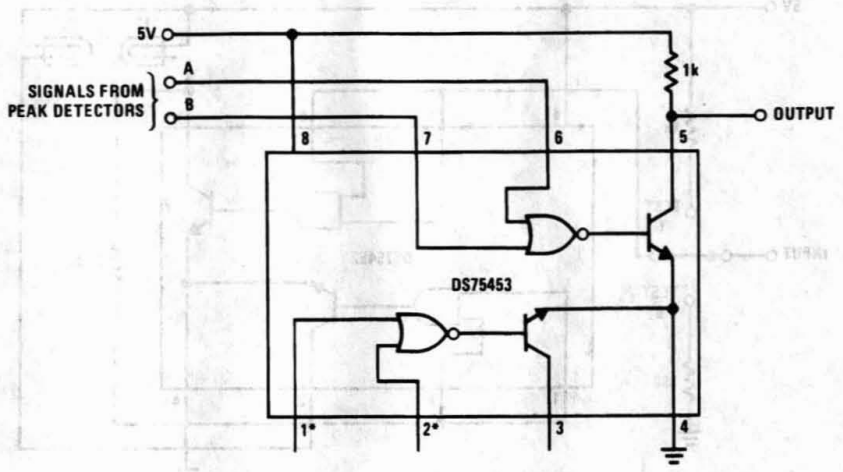
FIGURE 20. MOS Negative Logic-Level Detector



TL/F/5824–50

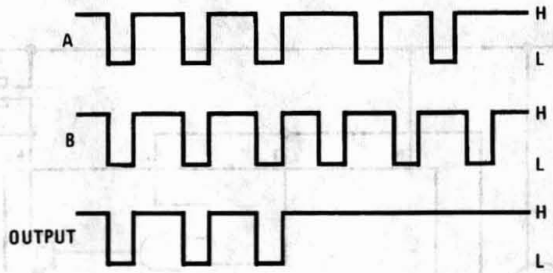
FIGURE 21. Logic Signal Comparator

Typical Applications (Continued)



TL/F/5824–51

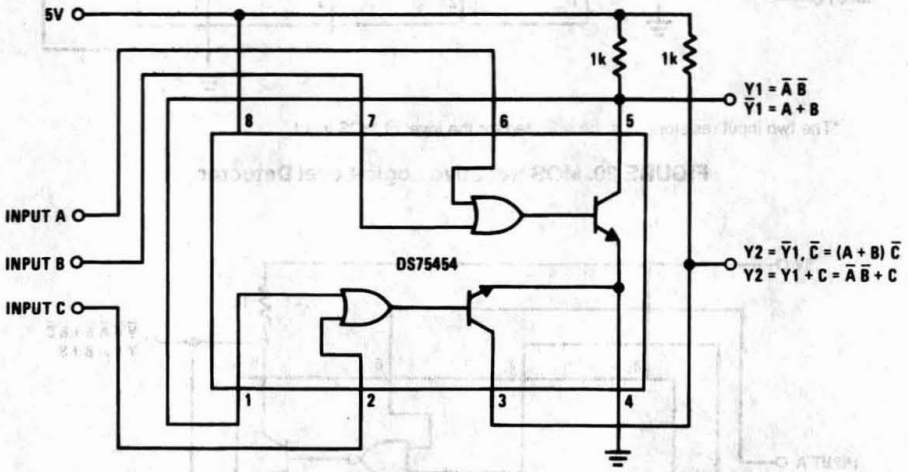
*If inputs are unused, they should be connected to +5V through a 1k resistor.



TL/F/5824–52

Low output occurs only when inputs are low simultaneously.

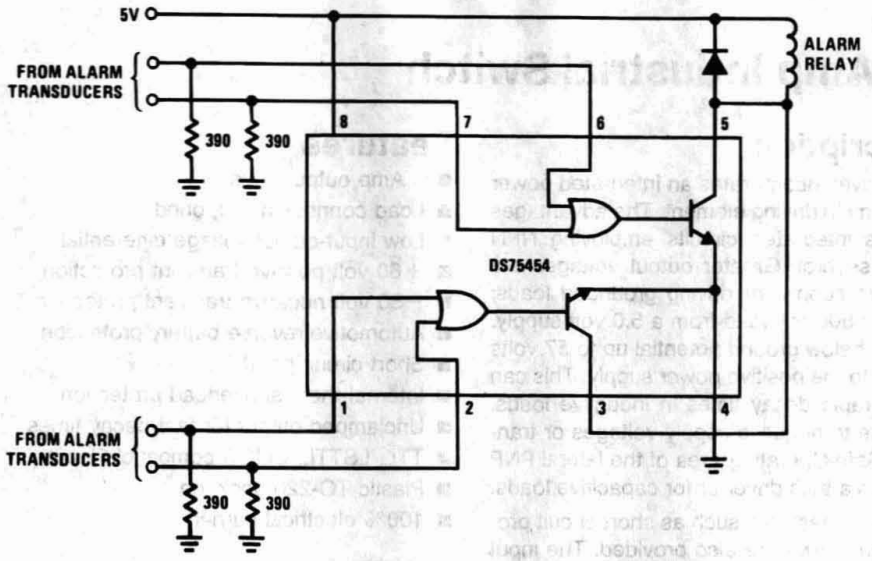
FIGURE 22. In-Phase Detector



TL/F/5824–53

FIGURE 23. Multifunction Logic-Signal Comparator

Typical Applications (Continued)



TL/F/5824–54

FIGURE 24. Alarm Detector

National Semiconductor

LM1921 1 Amp Industrial Switch

General Description

The LM1921 Relay Driver incorporates an integrated power PNP transistor as the main driving element. The advantages of this over previous integrated circuits employing NPN power elements are several. Greater output voltages are available off the same supply for driving grounded loads; typically 4.5 volts for a 500 mA load from a 5.0 volt supply. The output can swing below ground potential up to 57 volts negative with respect to the positive power supply. This can be used to facilitate rapid decay times in inductive loads. Also, the IC is immune to negative supply voltages or transients. The inherent Safe Operating Area of the lateral PNP allows use of the IC as a bulb driver or for capacitive loads.

Familiar integrated circuit features such as short circuit protection and thermal shutdown are also provided. The input voltage threshold levels are designed to be TTL, CMOS, and LSTTL compatible over the entire operating temperature range. If several drivers are used in a system, their inputs and/or outputs may be combined and wired together if their supply voltages are also common.

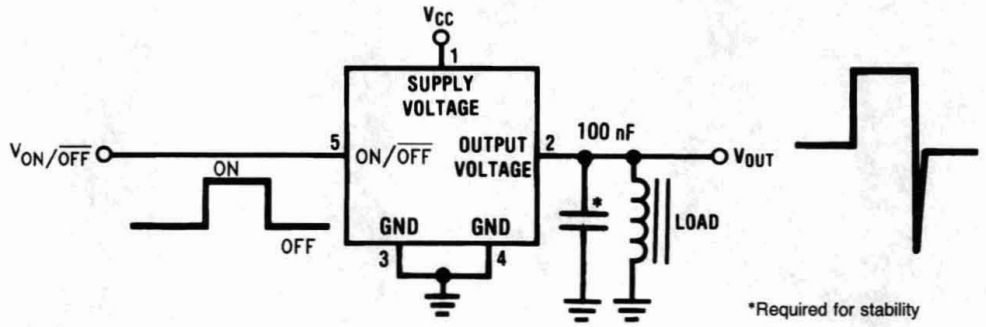
Features

- 1 Amp output drive
- Load connected to ground
- Low input-output voltage differential
- +60 volt positive transient protection
- −50 volt negative transient protection
- Automotive reverse battery protection
- Short circuit proof
- Internal thermal overload protection
- Unclamped output for fast decay times
- TTL, LSTTL, CMOS compatible input
- Plastic TO-220 package
- 100% electrical burn-in

Applications

- Relays
- Solenoids
- Valves
- Motors
- Lamps
- Heaters

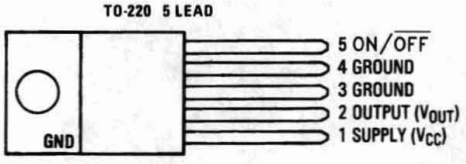
Typical Application Circuit



TL/H/5271–1

FIGURE 1. Test and Application Circuit

Connection Diagram



TL/H/5271–2

Front View
Order Number LM1921T
See NS Package Number T05A

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	
Operating Range	4.75V to 26V
Overvoltage Protection (100 ms)	−50V to +60V
Internal Power Dissipation	Internally Limited
Operating Temperature Range	−40°C to +125°C
Maximum Junction Temperature	150°C
Storage Temperature Range	−65°C to +150°C
Lead Temp. (Soldering, 10 seconds)	230°C

Electrical Characteristics (V_{CC} = 12V, I_{OUT} = 500 mA, T_J = 25°C, $V_{ON/\overline{OFF}}$ = 2V, unless otherwise specified.)

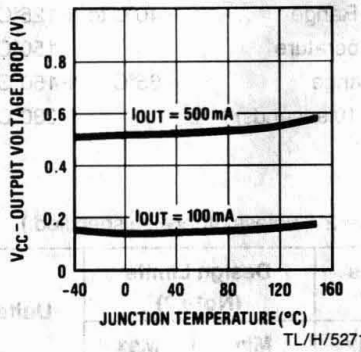
Parameter	Conditions	Typ	Tested Limits (Note 1)		Design Limits (Note 2)		Units
			Min	Max	Min	Max	
Supply Voltage							
Operational			4.75	26	6	24	V
Survival			−15	60			V_{DC}
Transient	100 ms, 1% Duty Cycle		−50				V
Supply Current							
$V_{ON/\overline{OFF}}$ = 0		0.6				1.5	mA
$V_{ON/\overline{OFF}}$ = 2V	I_{OUT} = 0 mA	6		10			mA
	I_{OUT} = 250 mA	285		350			mA
	I_{OUT} = 500 mA	575		700			mA
	I_{OUT} = 1A	1.3		1.5			A
Input to Output Voltage Drop	I_{OUT} = 500 mA	0.5		0.8			V
	I_{OUT} = 1A	1.0					V
Short Circuit Current		1.4	1.0	2.0			A
	6V ≤ V_{CC} ≤ 24V				.75	3.0	A
Output Leakage Current	$V_{ON/\overline{OFF}}$ = 0	0.1				50	μA
ON/$\overline{OFF}$ Voltage		1.3	0.8	2.0			V
Threshhold	6V ≤ V_{CC} ≤ 24V				0.8	2.0	V
ON/$\overline{OFF}$ Current		15	10	30			μA
Overvoltage Shutdown		32			26	36	V
Thermal Resistance							
junction-case	θjc	3					°C/W
case-ambient	θca	50					°C/W
Inductive Clamp							
Output Voltage	$V_{ON/\overline{OFF}}$ = 0, I_{OUT} = 100 mA	−60			−120	−45	V
Fault Conditions							
Output Current							
ON/$\overline{OFF}$ Floating	Pin 5 Open	0.1				50	μA
Ground Floating	Pin 3 & Pin 4 Open	0.1				50	μA
Reverse Voltage	V_{CC} = −15V	−0.01			−1		mA
Reverse Transient	V_{CC} = −50V	−100					mA
Overvoltage	V_{CC} = +60V	0.01				1	mA
Supply Current	Pin 1 & Pin 2 Short, No load	10				40	mA

Note 1: Guaranteed and 100% production tested.

Note 2: Guaranteed, not necessarily 100% production tested. Not used to calculate outgoing AQL. Limits are for the temperature range of −40°C ≤ T_j ≤ 150°C.

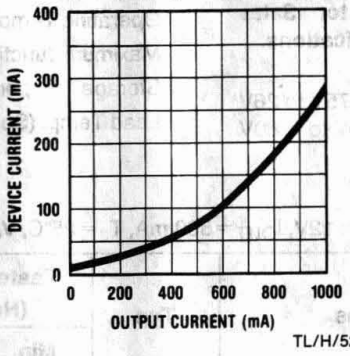
Typical Performance Characteristics

Output Voltage Drop



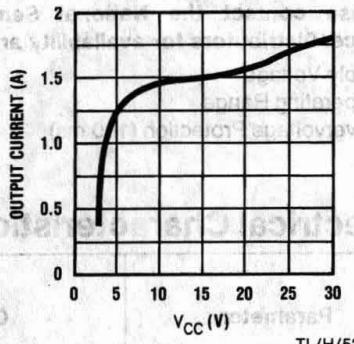
TL/H/5271–3

Device Operating Current



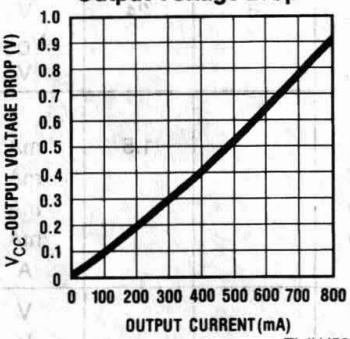
TL/H/5271–4

Peak Output Current (V_{OUT})



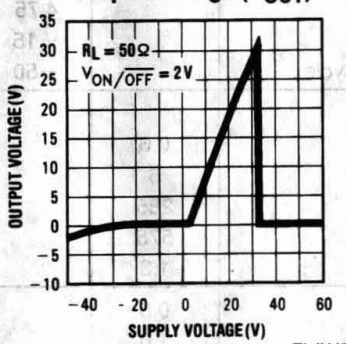
TL/H/5271–5

Output Voltage Drop



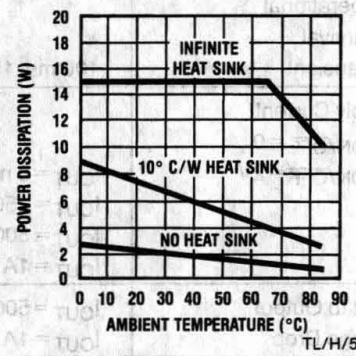
TL/H/5271–6

Output Voltage (V_{OUT})



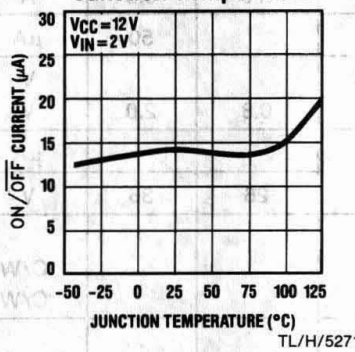
TL/H/5271–7

Maximum Power Dissipation (TO-220)



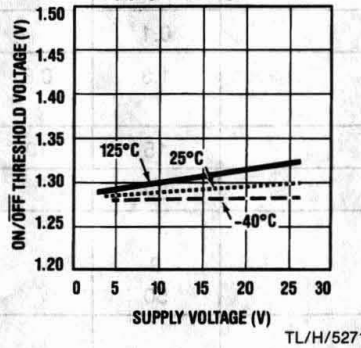
TL/H/5271–8

ON/$\overline{OFF}$ Current vs. Junction Temperature



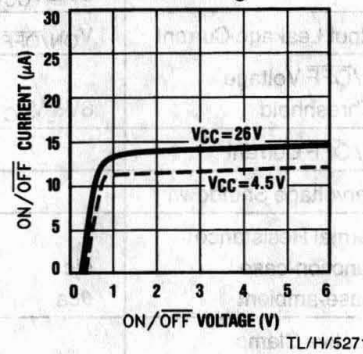
TL/H/5271–13

Threshold Voltage vs. Supply Voltage



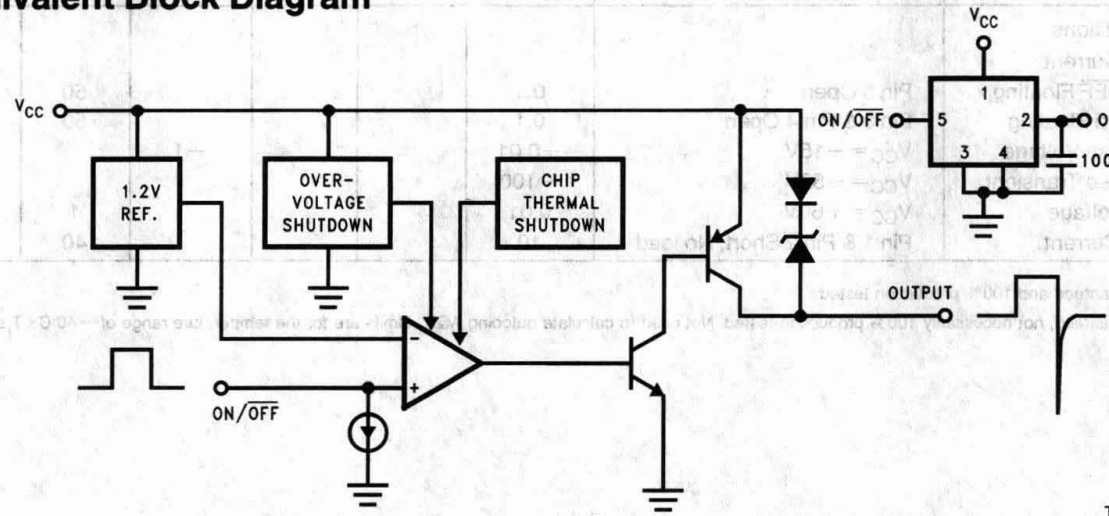
TL/H/5271–14

ON/$\overline{OFF}$ Current vs. ON/$\overline{OFF}$ Voltage



TL/H/5271–15

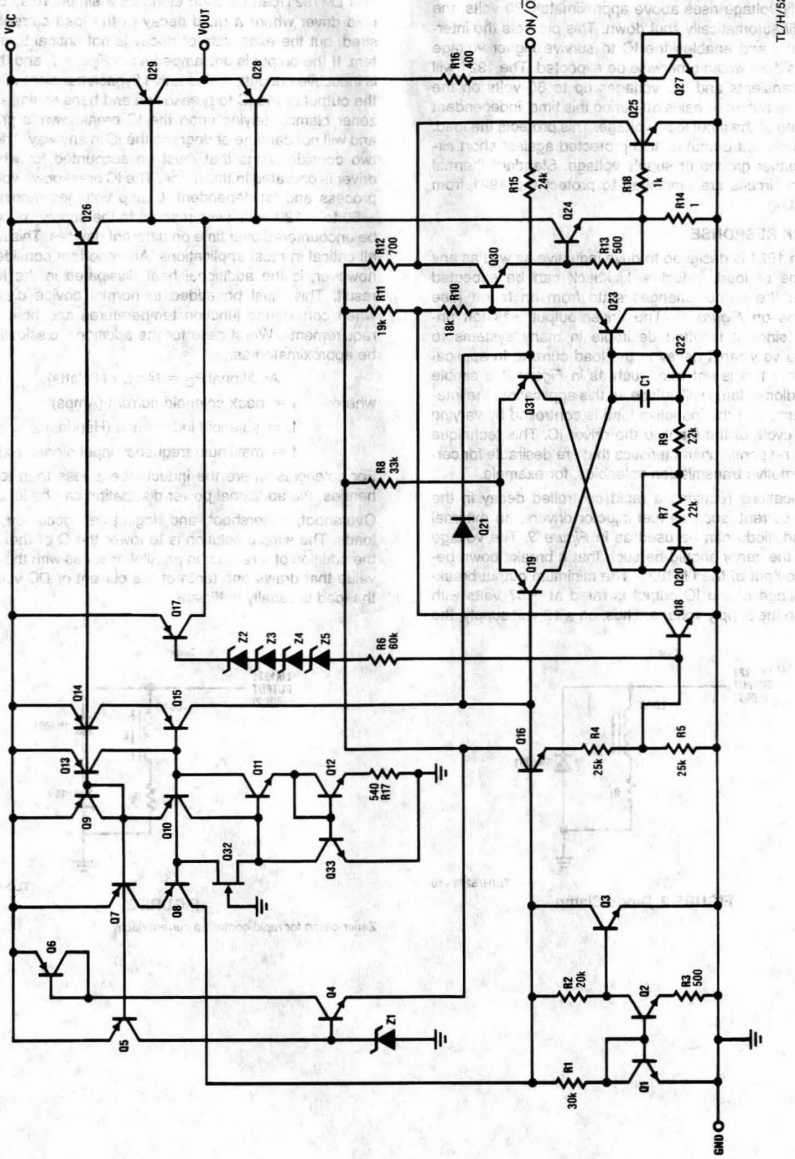
Equivalent Block Diagram



TL/H/5271–12

FIGURE 1

Circuit Schematic



TL/H/5271–9

Application Hints

HIGH CURRENT OUTPUT

The 1 Amp output is fault protected against overvoltage. If the supply voltage rises above approximately 30 volts, the output will automatically shut down. This protects the internal circuitry and enables the IC to survive higher voltage transients than would otherwise be expected. The 1921 will survive transients and DC voltages up to 60 volts on the supply. The output remains off during this time, independent of the state of the input logic voltage. This protects the load. The high current output is also protected against short circuits to either ground or supply voltage. Standard thermal shutdown circuits are employed to protect the 1921 from over heating.

FLYBACK RESPONSE

Since the 1921 is designed to drive inductive as well as any other type of load, inductive kickback can be expected whenever the output changes state from on to off (see waveforms on *Figure 1*). The driver output was left unclamped since it is often desirable in many systems to achieve a very rapid decay in the load current. In applications where this is not true, such as in *Figure 2*, a simple external diode clamp will suffice. In this application, the integrated current in the inductive load is controlled by varying the duty cycle of the input to the driver IC. This technique achieves response characteristics that are desirable for certain automotive transmission solenoids, for example.

For applications requiring a rapid controlled decay in the solenoid current, such as fuel injector drivers, an external zener and diode can be used as in *Figure 3*. The voltage rating of the zener should be such that it breaks down before the output of the LM1921. The minimum output breakdown voltage of the IC output is rated at −57 volts with respect to the supply voltage. Thus, on a 12 volt supply, the combined zener and diode breakdown should be less than 45 volts.

The LM1921 can be used alone as a simple relay or solenoid driver where a rapid decay of the load current is desired, but the exact rate of decay is not critical to the system. If the output is unclamped as in *Figure 1*, and the load is inductive enough, the negative flyback transient will cause the output of the IC to breakdown and behave similarly to a zener clamp. Relying upon the IC breakdown is practical, and will not damage or degrade the IC in any way. There are two considerations that must be accounted for when the driver is operated in this mode. The IC breakdown voltage is process and lot dependent. Clamp voltages ranging from −60 to −120 volts (with respect to the supply voltage) will be encountered over time on different devices. This is not at all critical in most applications. An important consideration, however, is the additional heat dissipated in the IC as a result. This must be added to normal device dissipation when considering junction temperatures and heat sinking requirements. Worst case for the additional dissipation can be approximated as:

$$\text{Additional } P_D = I^2 \times L \times f \text{ (Watts)}$$

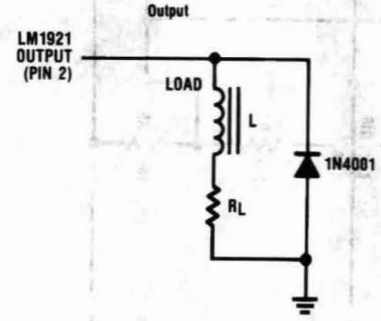
where: I = peak solenoid current (Amps)

L = solenoid inductance (Henries)

f = maximum frequency input signal (Hz)

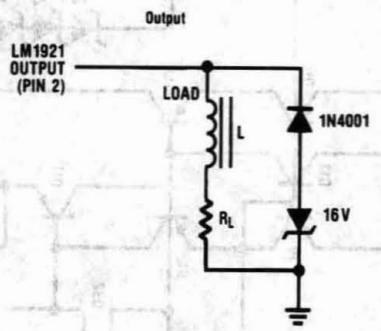
For solenoids where the inductance is less than ten millihenries, the additional power dissipation can be ignored.

Overshoot, undershoot, and ringing can occur on certain loads. The simple solution is to lower the Q of the load by the addition of a resistor in parallel or series with the load. A value that draws one tenth of the current or DC voltage of the load is usually sufficient.



TL/H/5271–10

FIGURE 2. Diode Clamp



TL/H/5271–11

FIGURE 3

Zener clamp for rapid controlled current decay

National Semiconductor

LM1950 750 mA High Side Switch

General Description

The LM1950 is a high current, high side (PNP) power switch for driving ground referenced loads. Intended for industrial and automotive applications the LM1950 is guaranteed to deliver 750 mA continuous load current (with typically 1.4 Amps peak) and can withstand supply voltage transients up to +60V and −50V. When switched OFF the quiescent current drain from the input power supply is less than 100 μA which can allow continuous connection to a battery power source.

The LM1950 will drive all types of resistive or reactive loads. To obtain a rapid decay time of the energy in inductive loads, the output is internally protected but not clamped and can swing below ground to at least 54V negative with respect to the input power supply voltage.

The ON/OFF input can be driven with standard 5V TTL or CMOS compatible logic levels independent of the V_{CC} supply voltage used. Built in protection features include short circuit protection, thermal shutdown, over-voltage shutdown to protect load circuits and protection against reverse polarity input connections. The LM1950 is available in a 5-lead power TO-220 package and specified over a wide −40°C to 125°C operating temperature range.

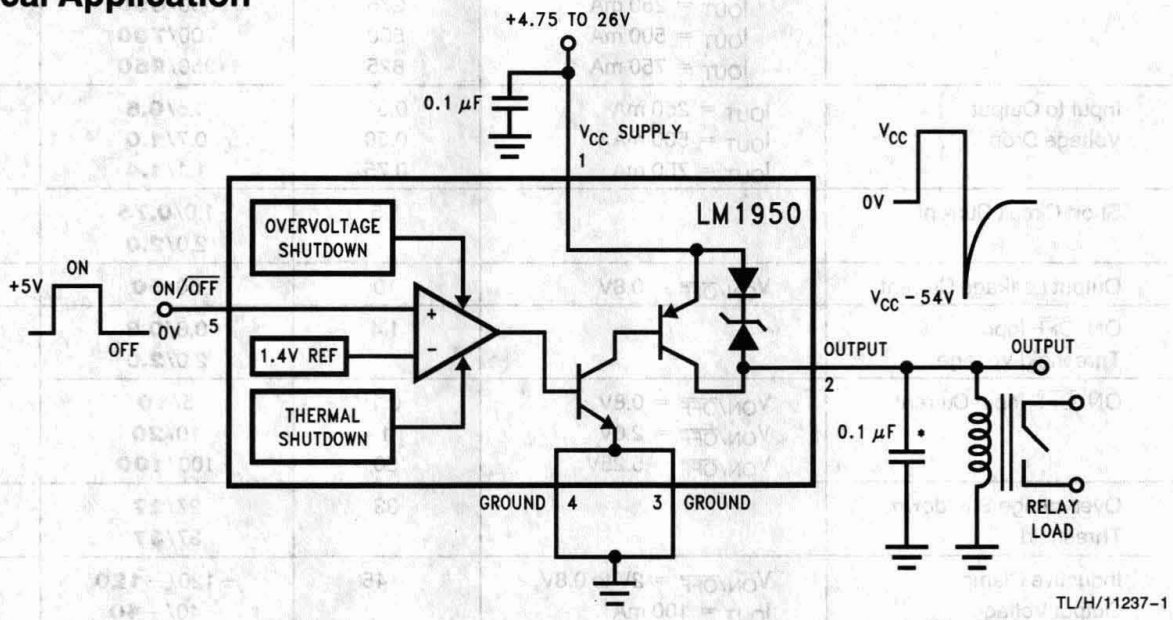
Features

- 750 mA continuous output drive current
- Less than 100 μA quiescent current in OFF state
- Low input/output voltage drop
- +60V/−50V transient protection
- Drives resistive or reactive loads
- Unclamped output for fast inductive decay tmies
- Reverse battery protected
- Short circuit proof
- Overvoltage shutdown to protect loads
- TTL/CMOS compatible control input
- Thermal overload protection

Applications

- Relay driver
- Solenoid/Valve driver
- Lamp driver
- Load circuit switching
- Motor driver

Typical Application

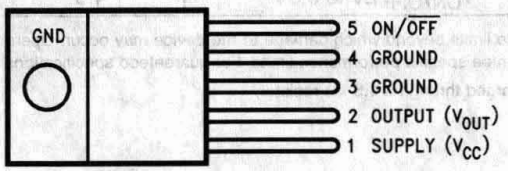


TL/H/11237–1

*Required for stability

Connection Diagram

TO 220, 5 Lead



TL/H/11237–2

Front View
Order Number LM1950T
See NS Package Number T05A

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	
Continuous	26V
Transient ($\tau \leq$ 100 ms)	−50V to +60V
Reverse Polarity (continuous)	−15V
On/$\overline{\text{Off}}$ Voltage	−0.3V to +6.0V
Power Dissipation	Internally Limited
Load Inductance	150 mH
Maximum Junction Temperature	150°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	230°C
ESD Susceptibility (Note 2)	2000V

Operating Ratings (Note 1)

Temperature Range (T_A)	−40°C to +125°C
Supply Voltage Range	4.75V to 26V
Thermal Resistances:	
Junction to Case ($\theta_{j\text{-}c}$)	3°C/W
Case to Ambient ($\theta_{c\text{-}a}$)	50°C/W

Electrical Characteristics

V_{CC} = 14V, I_{OUT} = 150 mA unless otherwise indicated. **Boldface** limits apply over the entire operating temperature range, −40°C ≤ T_A ≤ 125°C, all other specifications are for $T_A = T_J$ = 25°C

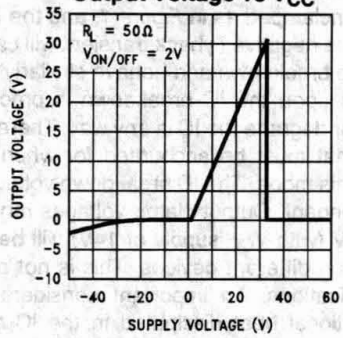
Parameter	Conditions	Typical	Limit	Units (Limit)
Supply Voltage				
Operational			4.75/**4.75**	V (Min)
			26/**26**	V (Max)
Survival			−15/−**15**	V_{DC} (Min)
Transient	t = 1 ms, τ = 100 ms, 1% dutycycle		60/**60**	V (Max)
			−50/−**50**	V (Min)
Supply Current	$V_{ON/\overline{OFF}}$ = 0.8V	20	100/**100**	μA(Max)
	$V_{ON/\overline{OFF}}$ = 2.0V			
	I_{OUT} = 0 mA	5	10/**10**	mA (Max)
	I_{OUT} = 250 mA	275	350/**350**	mA (Max)
	I_{OUT} = 500 mA	550	700/**700**	mA (Max)
	I_{OUT} = 750 mA	825	950/**950**	mA (Max)
Input to Output Voltage Drop	I_{OUT} = 250 mA	0.30	0.5/**0.6**	V (Max)
	I_{OUT} = 500 mA	0.50	0.7/**1.0**	V (Max)
	I_{OUT} = 750 mA	0.75	1.1/**1.4**	V (Max)
Short Circuit Current		1.5	1.0/**0.75**	A (Min)
			2.0/**2.0**	A (Max)
Output Leakage Current	$V_{ON/\overline{OFF}}$ = 0.8V	10	50/**50**	μA (Max)
ON/$\overline{\text{OFF}}$ Input Threshold Voltage		1.4	0.8/**0.8**	V (Min)
			2.0/**2.0**	V (Max)
ON/$\overline{\text{OFF}}$ Input Current	$V_{ON/\overline{OFF}}$ = 0.8V	0.1	5/**10**	μA (Max)
	$V_{ON/\overline{OFF}}$ = 2.0V	1	10/**20**	μA (Max)
	$V_{ON/\overline{OFF}}$ = 5.25V	50	100/**100**	μA (Max)
Overvoltage Shutdown Threshold		33	27/**27**	V (Min)
			37/**37**	V (Max)
Inductive Clamp Output Voltage	$V_{ON/\overline{OFF}}$ = 2V to 0.8V, I_{OUT} = 100 mA	−45	−120/−**120**	V (Max)
			−40/−**40**	V (Min)
Output Turn-On Delay	$V_{ON/\overline{OFF}}$ 0.8V to 2V	4.2	**20**	μs
Output Turn-Off Delay	$V_{ON/\overline{OFF}}$ 2V to 0.8V	4.5	**20**	μs

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics.

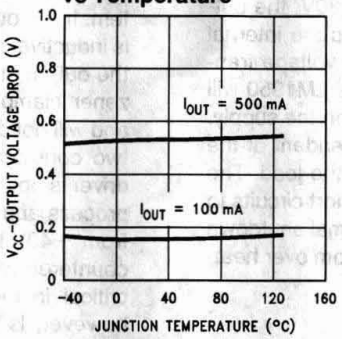
Note 2: Human body model, 100 pF discharged through a 1.5 kΩ resistor.

Typical Performance Characteristics

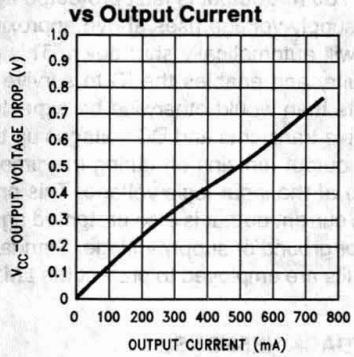
Output Voltage vs V_{CC}



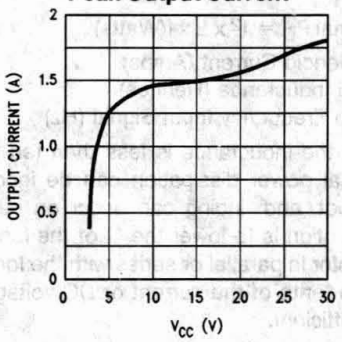
Output Voltage Drop vs Temperature



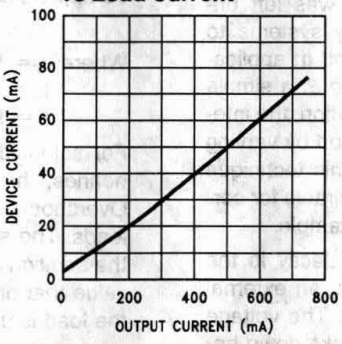
Output Voltage Drop vs Output Current



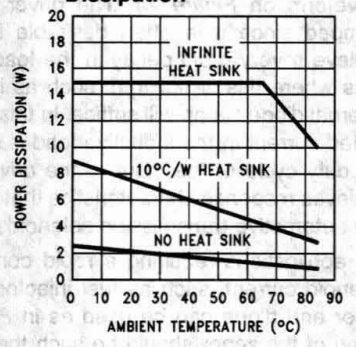
Peak Output Current



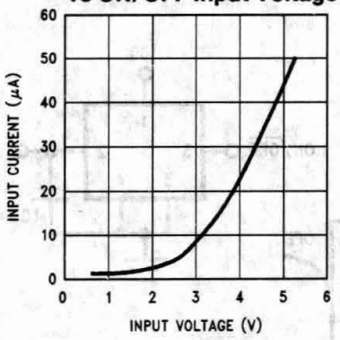
Operating Current vs Load Current



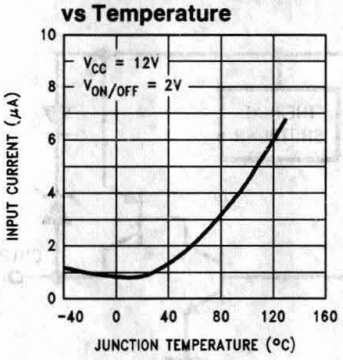
Maximum Power Dissipation



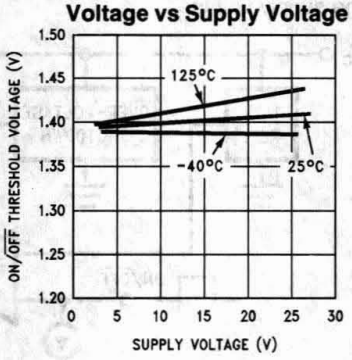
ON/$\overline{OFF}$ Input Current vs ON/$\overline{OFF}$ Input Voltage



ON/$\overline{OFF}$ Input Current vs Temperature



On/$\overline{OFF}$ Input Threshold Voltage vs Supply Voltage



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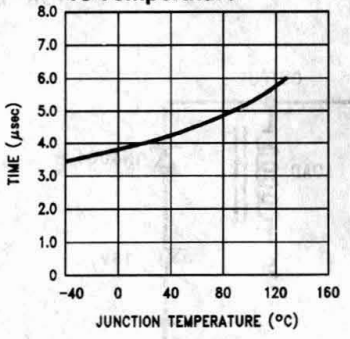
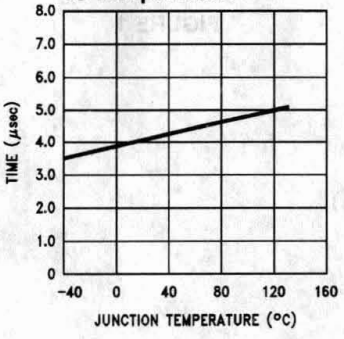
Turn-On Delay Time vs Temperature



TL/H/11237–11

Turn-Off Delay Time vs Temperature



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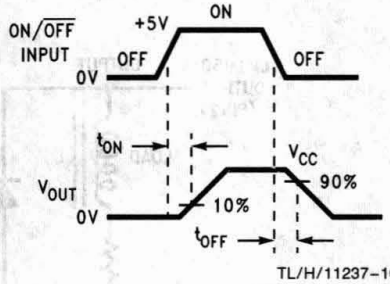
Delay Time Definitions



TL/H/11237–10

Application Hints

HIGH CURRENT OUTPUT

The 750 mA output is fault protected against overvoltage. If the supply voltage rises above approximately 30V, the output will automatically shut down. This protects the internal circuitry and enables the IC to survive higher voltage transients than would otherwise be expected. The LM1950 will survive transients and DC voltages up to 60V on the supply. The output remains off during this time, independent of the state of the input logic voltage. This protects the load. The high current output is also protected against short circuits to either ground or supply voltage. Standard thermal shutdown circuits are employed to protect the LM1950 from over heating.

FLYBACK RESPONSE

Since the LM1950 is designed to drive inductive as well as any other type of load, inductive kickback can be expected whenever the output changes state from ON to OFF (See Waveform on *Figure 1*). The driver output was left unclamped since it is often desirable in many systems to achieve a very rapid decay in the load current. In applications where this is not true, such as in *Figure 2*, a simple external diode clamp will suffice. In this application, the integrated current in the inductive load is controlled by varying the duty cycle of the input to the drive IC. This technique achieves response characteristics that are desirable for certain automotive transmission solenoids, for example.

For applications requiring a rapid controlled decay in the solenoid current, such as fuel injector drivers, an external zener and diode can be used as in *Figure 3*. The voltage rating of the zener should be such that it breaks down before the output of the LM1950. The minimum output breakdown voltage of the IC output is rated at -54V with respect to the supply voltage.

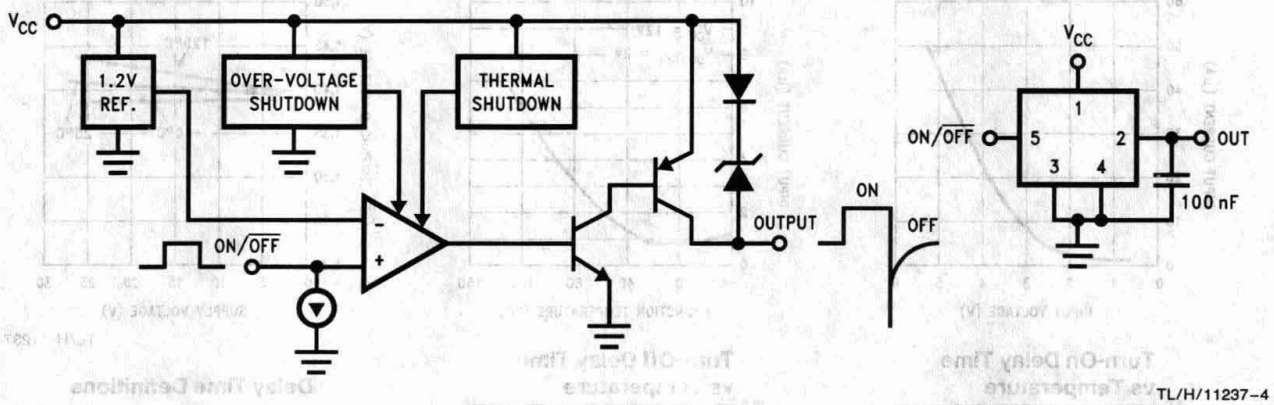
The LM1950 can be used alone as a simple relay or solenoid driver where a rapid decay of the load current is desired, but the exact rate of decay is not critical to the system. If the output is unclamped as in *Figure 1*, and the load is inductive enough, the negative flyback transient will cause the output of the IC to breakdown and behave similarly to a zener clamp. Relying upon the IC breakdown is practical and will not damage or degrade the IC in any way. There are two considerations that must be accounted for when the driver is operated in this mode. The IC breakdown voltage is process and lot dependent. Output clamp voltages ranging from -40V to -120V (with V_{CC} supply of 14V) will be encountered over time on different devices. This is not at all critical in most applications. An important consideration, however, is the additional heat dissipated in the IC as a result. This must be added to normal device dissipation when considering junction temperatures and heat sinking requirements. Worst case for the additional dissipation can be approximated as:

$$\text{Additional } P_D = I^2 \times L \times f(\text{Watts})$$

Where: I = Peak Solenoid Current (Amps)
L = Solenoid Inductance (Henries)
f = Maximum Frequency Input Signal (Hz)

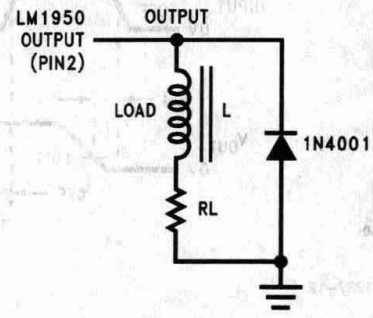
For solenoids where the inductance is less than ten millihenries, the additional power dissipation can be ignored. Overshoot, undershoot, and ringing can occur on certain loads. The simple solution is to lower the Q of the load by the addition of a resistor in parallel or series with the load. A value that draws one tenth of the current or DC voltage of the load is usually sufficient.

For frequency stability of the switch, a 0.1 μF or larger output bypass capacitor is required.



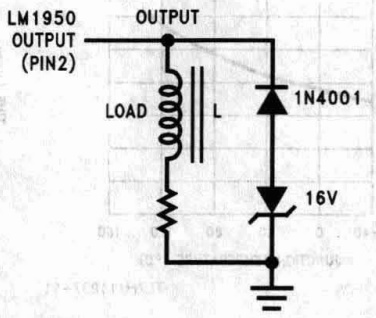
TL/H/11237–4

FIGURE 1



TL/H/11237–5

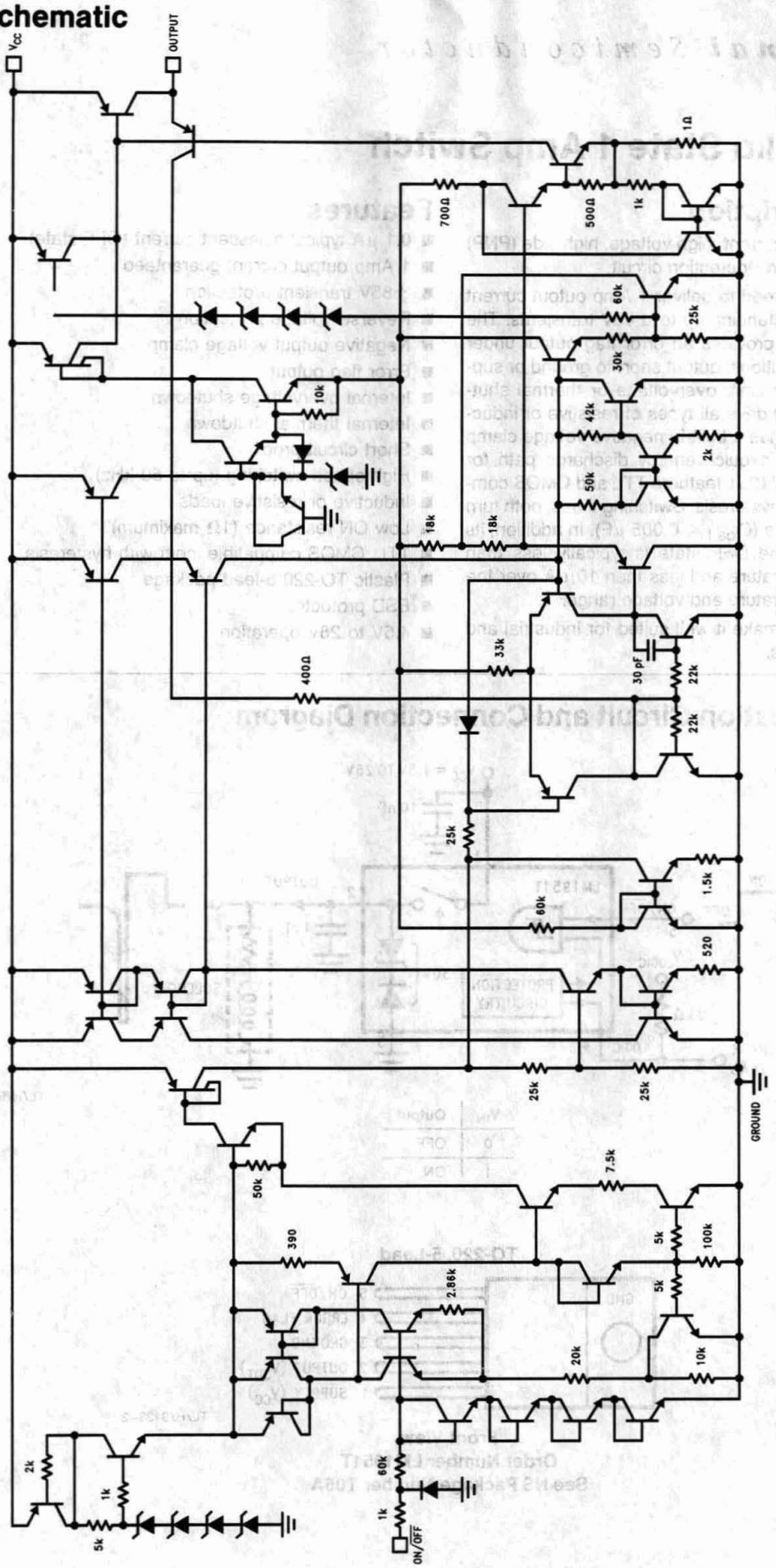
FIGURE 2. Diode Clamp



TL/H/11237–6

FIGURE 3. Zener Clamp for Rapid Controlled Current Decay

Circuit Schematic



TL/H/11237–9

National Semiconductor

LM1951 Solid State 1 Amp Switch

General Description

The LM1951 is a high current, high voltage, high side (PNP) switch with a built-in error detection circuit.

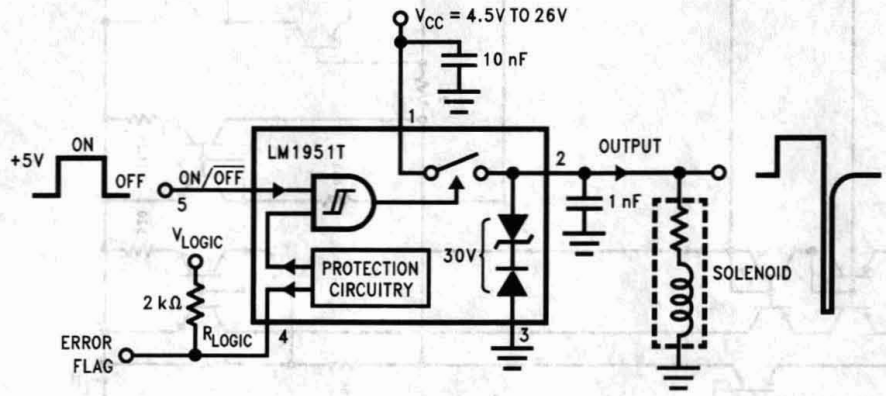
The LM1951 is guaranteed to deliver 1 Amp output current and is capable of withstanding up to ±85V transients. The built-in error detection provides an error flag output under the following fault conditions: output short to ground or supply, open load, current limit, overvoltage or thermal shutdown. The LM1951 will drive all types of resistive or inductive loads. The output has a built-in negative voltage clamp (≈ −30V) to provide a quick energy discharge path for inductive loads. The LM1951 features TTL and CMOS compatible logic input with hysteresis. Switching times, both turn on and turn off, are 2 μs (C_{load} < 0.005 μF). In addition, its quiescent current in the OFF state is typically less than 0.1 μA at room temperature and less than 10 μA over the entire operating temperature and voltage range.

The LM1951 features make it well suited for industrial and automotive applications.

Features

- 0.1 μA typical quiescent current (OFF state)
- 1 Amp output current guaranteed
- ±85V transient protection
- Reverse voltage protection
- Negative output voltage clamp
- Error flag output
- Internal overvoltage shutdown
- Internal thermal shutdown
- Short circuit proof
- High speed switching (up to 50 kHz)
- Inductive or resistive loads
- Low ON resistance (1Ω maximum)
- TTL, CMOS compatible input with hysteresis
- Plastic TO-220 5-lead package
- ESD protected
- 4.5V to 26V operation

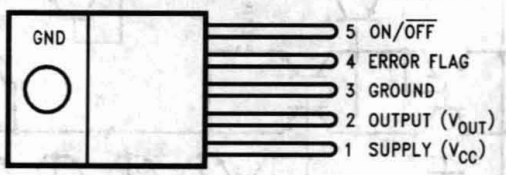
Typical Application Circuit and Connection Diagram



TL/H/9133–1

V_{IN}	Output
0	OFF
1	ON

TO-220, 5-Lead



TL/H/9133–2

Front View
Order Number LM1951T
See NS Package Number T05A

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage
- Operational Voltage: 26 V_{DC}
- Sustained Voltage: $-40\ V_{DC} \geq V_{CC} \leq 85\ V_{DC}$
- Transient Voltage Protection: ±85V
  (τ = 100 ms, 1% Duty Cycle, $R_S \geq 10\Omega$)
- Pins 4, 5: 26 V_{DC}

Power Dissipation (Note 1)	Internally Limited
Load Inductance	1H
Operating Temperature Range (T_A)	−40°C to +125°C
Maximum Junction Temperature	150°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec.)	260°C
ESD Tolerance (Note 4):	2000V

Electrical Characteristics

V_{CC} = 12V, I_{out} = 500 mA, C_{out} = 0.001 µF, T_A = 25°C unless otherwise specified

Parameter	Conditions		Typical	Tested Limit (Note 2)	Design Limit (Note 3)	Units
Supply Voltage, V_{CC}				4.5		V_{min}
Operational				26		V_{max}
Transient	τ = 100 ms, 1% Duty Cycle, $R_{CC} \geq 10\Omega$			−85		V
				85		V
Supply Current	I_{out} = 0 mA, $V_{ON/\overline{OFF}}$ = 0.8V		0.1	10	100	μA_{max}
	I_{out} = 250 mA, $V_{ON/\overline{OFF}}$ = 2.0V		260	270		mA_{max}
	I_{out} = 600 mA, $V_{ON/\overline{OFF}}$ = 2.0V		630	650		mA_{max}
	I_{out} = 1A, $V_{ON/\overline{OFF}}$ = 2.0V		1.06	1.2		A_{max}
Voltage Drop ($V_{CC} - V_{OUT}$)	I_{out} = 600 mA, $V_{ON/\overline{OFF}}$ = 2.0V		400	600		mV_{max}
	I_{out} = 1A, $V_{ON/\overline{OFF}}$ = 2.0V		0.7	1.0		V_{max}
Short Circuit Current	V_{OUT} = 0V, $V_{ON/\overline{OFF}}$ = 2V		1.3	1.0		A_{min}
				2.5		A_{max}
Input Threshold, Pin 5	4.5V ≤ V_{CC} ≤ 26V	Turn ON	1.4	2.0	2.0	V_{max}
		Turn OFF	1.2	0.8	0.8	V_{min}
Input Current, Pin 5	0.8V ≤ $V_{ON/\overline{OFF}}$ ≤ 5.5V		25	50		μA_{max}
				10		μA_{min}
Output Clamp	I_{out} ≤ 600 mA		−30	−40		V_{min}
				−24		V_{max}
Delay Time t_d, ON	R_{load} = 20Ω, C_{load} = 0.001 µF		1	3		μs_{max}
t_d, OFF			1	3		μs_{max}
Rise Time			1	3		μs_{max}
Fall Time			1	3		μs_{max}
Error Flag Characteristics:						
Output Voltage	Error Condition, Pin 4 Low, Sinking 10 mA		0.3	0.8		V_{max}
Sink Current	Error Condition, Pin 4 = 0.3V		10	3		mA_{min}
Output Leakage Current	No Error, Pin 4 = 26V		0.01	1		μA_{max}
Response Time	V_{LOGIC} = 5V, R_{LOGIC} = 2 kΩ, C_{LOGIC} = 0 µF		1			µs

Note 1: Thermal resistance junction-to-case is 3°C/W. Thermal resistance case-to-ambient is 50°C/W.

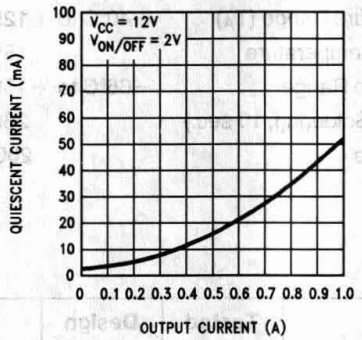
Note 2: Tested Limits are guaranteed and 100% production tested.

Note 3: Design Limits are guaranteed (but not 100% production tested) over the operating temperature and supply voltage range. These limits are not used to calculate outgoing quality levels.

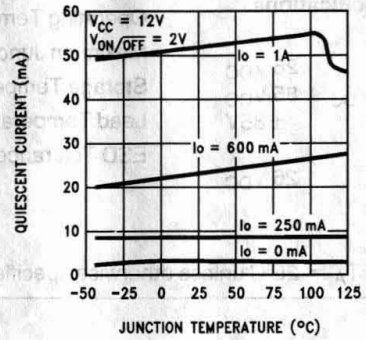
Note 4: Human body model, 100 pF discharged through a 1.5 kΩ resistor.

Typical Performance Characteristics

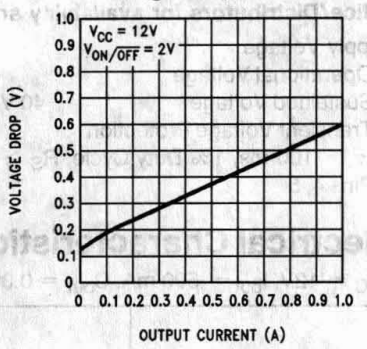
Quiescent Current



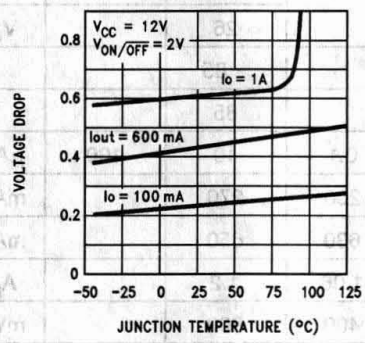
Quiescent Current



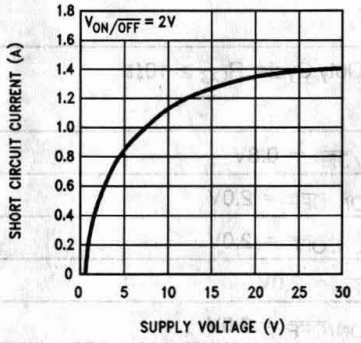
Voltage Drop



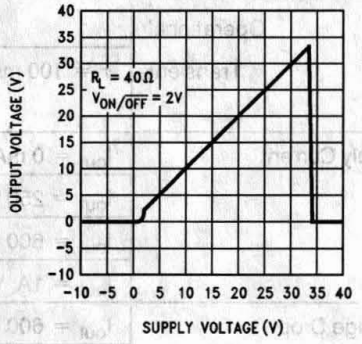
Voltage Drop



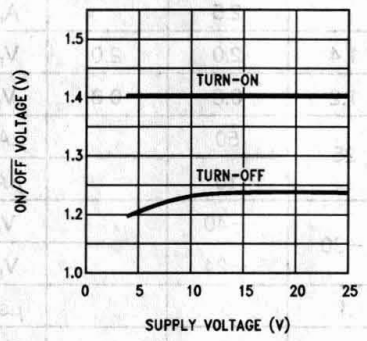
Short Circuit Current



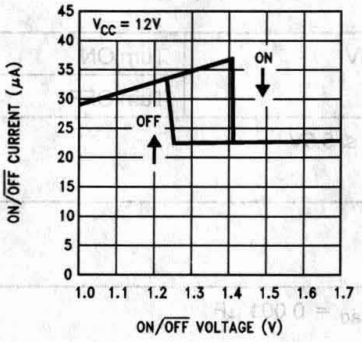
High Voltage Behavior



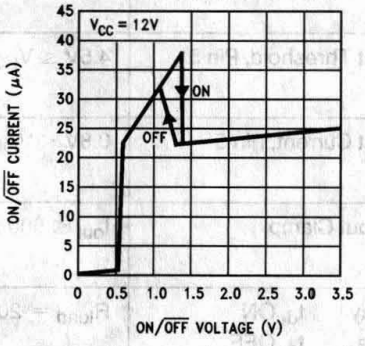
ON/$\overline{\text{OFF}}$ Threshold (Pin 5)



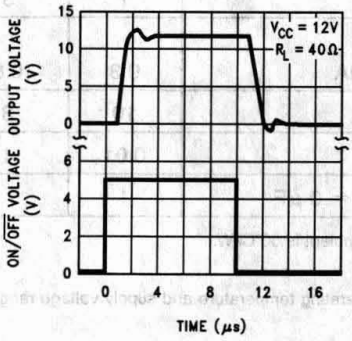
ON/$\overline{\text{OFF}}$ Current (Pin 5)



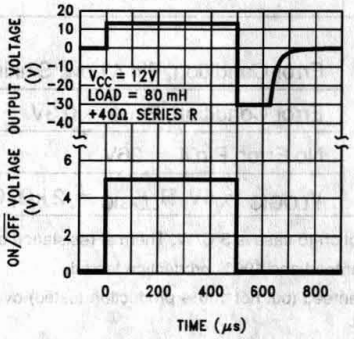
ON/$\overline{\text{OFF}}$ Current (Pin 5)



Output Voltage
Resistive Load

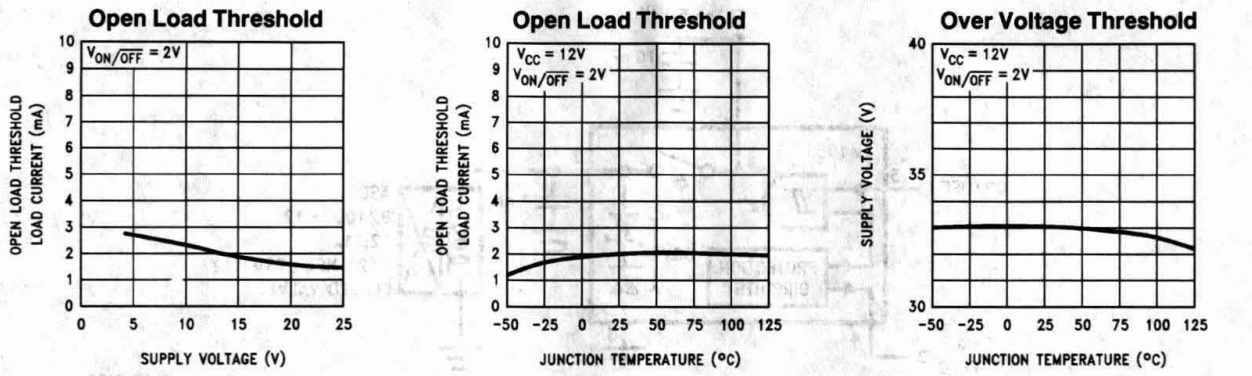


Output Voltage
Inductive Load



TL/H/9133–3

Error Flag Output Characteristics



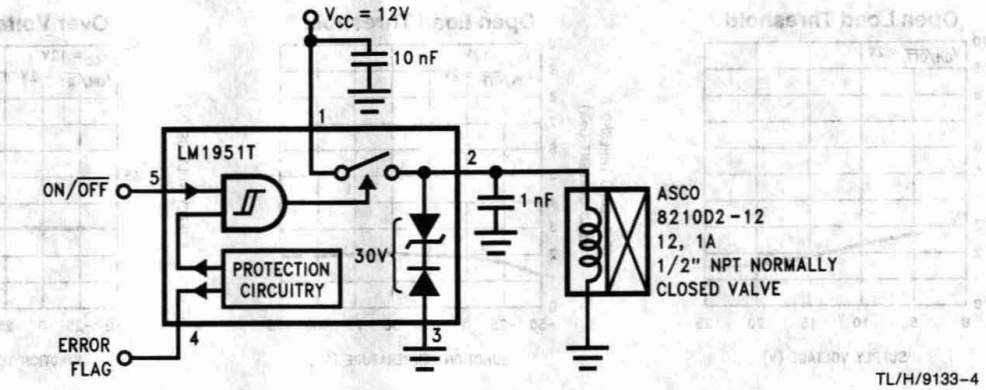
TL/H/9133–13

Truth Table

Fault Condition	$V_{ON/\overline{OFF}}$*	V_{out}	Error Flag
Normal	L	L	H
	H	H	H
Overvoltage	L	L	L
	H	L	L
Thermal Shutdown	L	L	L
	H	L	L
V_{OUT} Short to GND	L	L	H
	H	L	L
V_{OUT} Short to V_{supply}	L	H	L
	H	H	L
Open Load	L	L	H
	H	H	L
Current Limit	L	L	H
	H	H	L

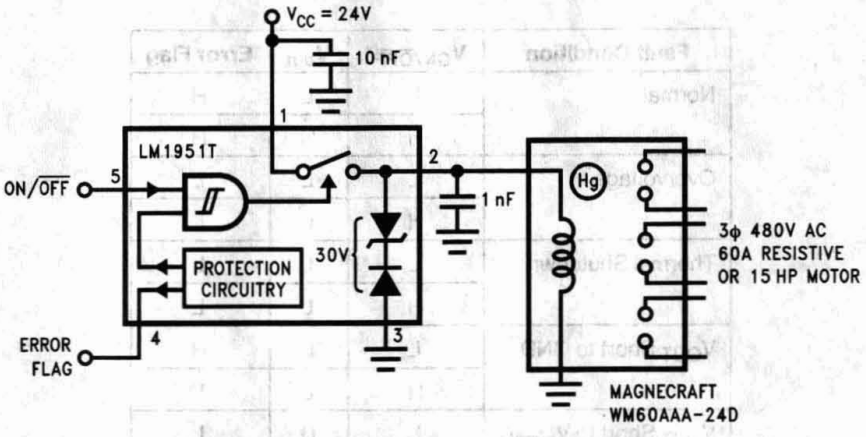
* L ≅ $0 \leq V_{ON/\overline{OFF}} \leq 0.8V$ H ≅ $2V \leq V_{ON/\overline{OFF}} \leq 26V$

Typical Applications



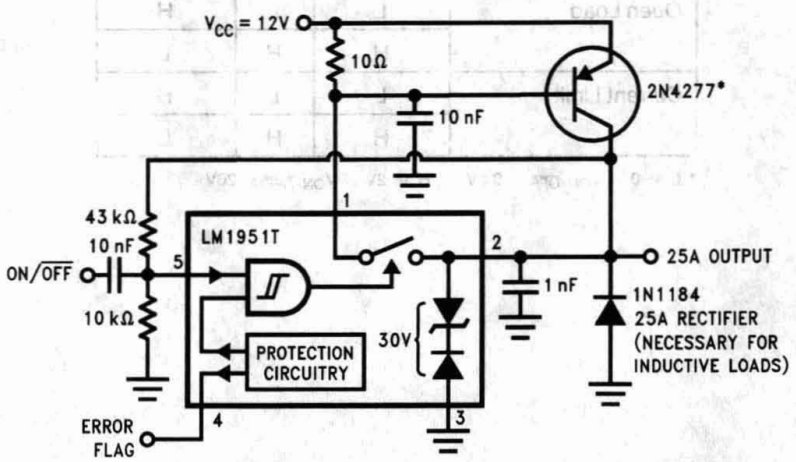
TL/H/9133–4

FIGURE 1. Solenoid Actuated Valve



TL/H/9133–5

FIGURE 2. 60A 3-Phase Mercury Displacement Relay

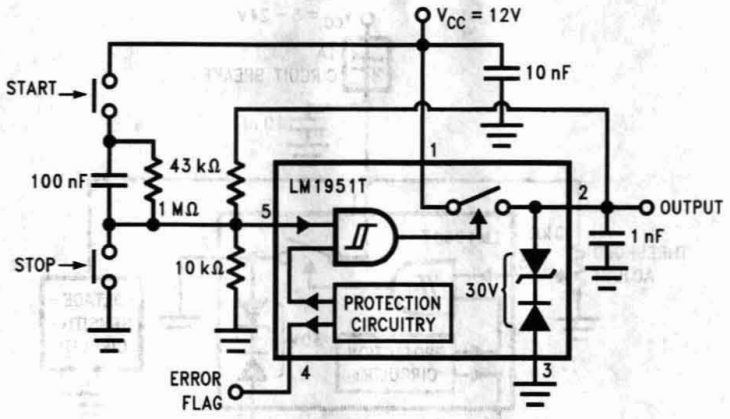


TL/H/9133–6

*Available from Germanium Power Devices, Andover, MA, Tel. (617) 475-5982

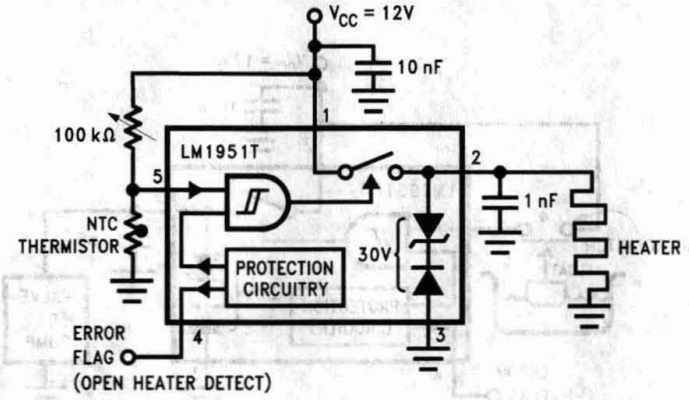
FIGURE 3. 25A Switch with Short Circuit Foldback

Typical Applications (Continued)



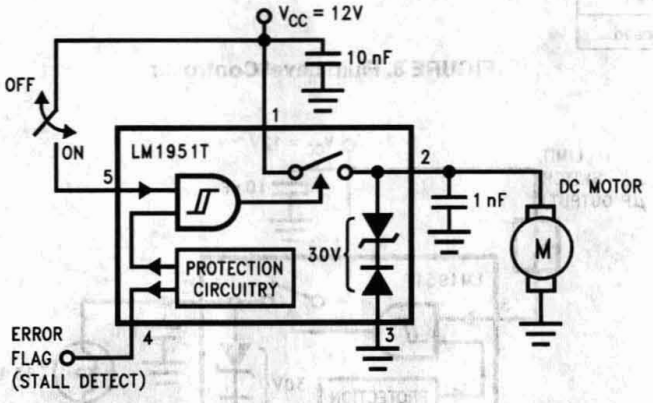
TL/H/9133–7

FIGURE 4. Latching Switch



TL/H/9133–8

FIGURE 5. Temperature Controller with Hysteresis

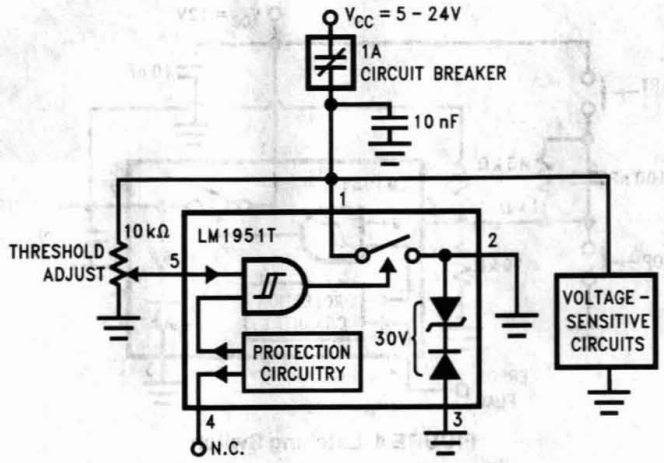


TL/H/9133–9

FIGURE 6. DC Motor Driver

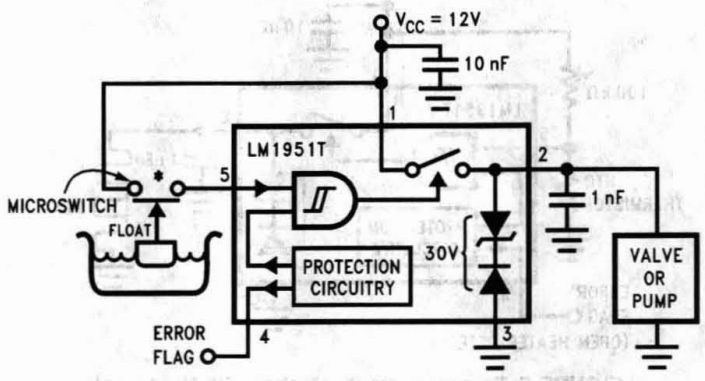
3

Typical Applications (Continued)



TL/H/9133–10

FIGURE 7. Over-Voltage Crowbar

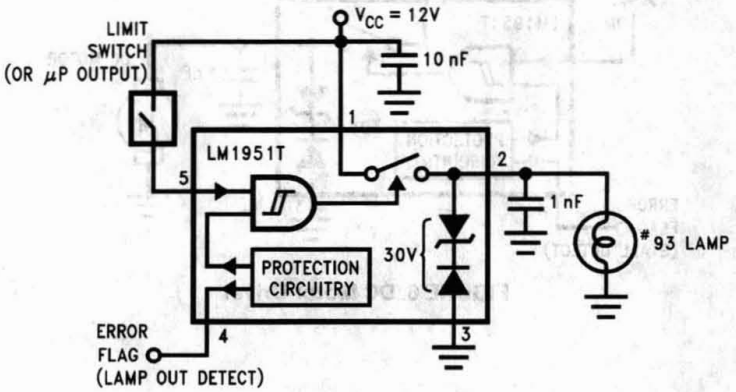


TL/H/9133–11

*

Operation	Switch Type
Empty	Normally Open
Fill	Normally Closed

FIGURE 8. Fluid Level Controller



TL/H/9133–12

FIGURE 9. Indicator Lamp Driver

Application Hints

When inductive loads are turned OFF, they produce a negative voltage spike. The LM1951 contains a voltage clamp that limits these spikes to approximately −30V, thus an external clamp is not necessary in most applications.

Loads with an inductance of greater than 1H, driven to full output current, may damage the clamp simply by exceeding the power capabilities of the LM1951. An LM1951 can dissipate 25W continuous at 25°C ambient when mounted on a large heatsink. If the load current is limited to 800 mA, the sustained spike from an infinitely large inductance can be handled. Sustained spikes produced by higher currents and high inductances will exceed the 25W limit.

For inductances above 1H, care should be taken to see that the output current does not exceed a value that could damage the clamp. While 800 mA is acceptable for the device running at 25°C ambient on a heatsink, derate this current for smaller heatsinks or higher ambient temperatures to limit the junction temperature to 150°C. Alternatively, an external clamp or resonating capacitor can be added to handle any combination of load inductance, load current, and device temperature. This is especially important if the output current is boosted, such as the application shown in *Figure 3*. A peak power of 750W could be developed in the internal clamp if an inductive load is switched without external clamping.

Another case where the clamp's power capability may be exceeded is when driving a solenoid. The inductance of a solenoid is greatest when energized, with the plunger pulled in. As the plunger is pulled out of the solenoid, the inductance goes down. Under certain conditions of high solenoid inductance and fast mechanical time constants, the current may actually **increase** when the solenoid is turned OFF. Since the energy stored in an inductor cannot change instantaneously, the current must increase to conserve energy when the inductance decreases. This condition is traced by observing the load current with a current probe and storage oscilloscope.

Load capacitances larger than 1 nF will slow rise and fall times. Inductive loads having a capacitive component larger than 1 nF will also exhibit overshoot. Furthermore, ringing may be evident in a combination inductive/capacitive load, or in an inductive load with supply decoupling capacitors in the range of 100 nF to 1 μF. For fast rise and fall times and minimum ringing with inductive loads, a supply decoupling capacitor of 10 nF and an output capacitor of 1 nF is recommended. These should be located as close to the IC pins as possible.

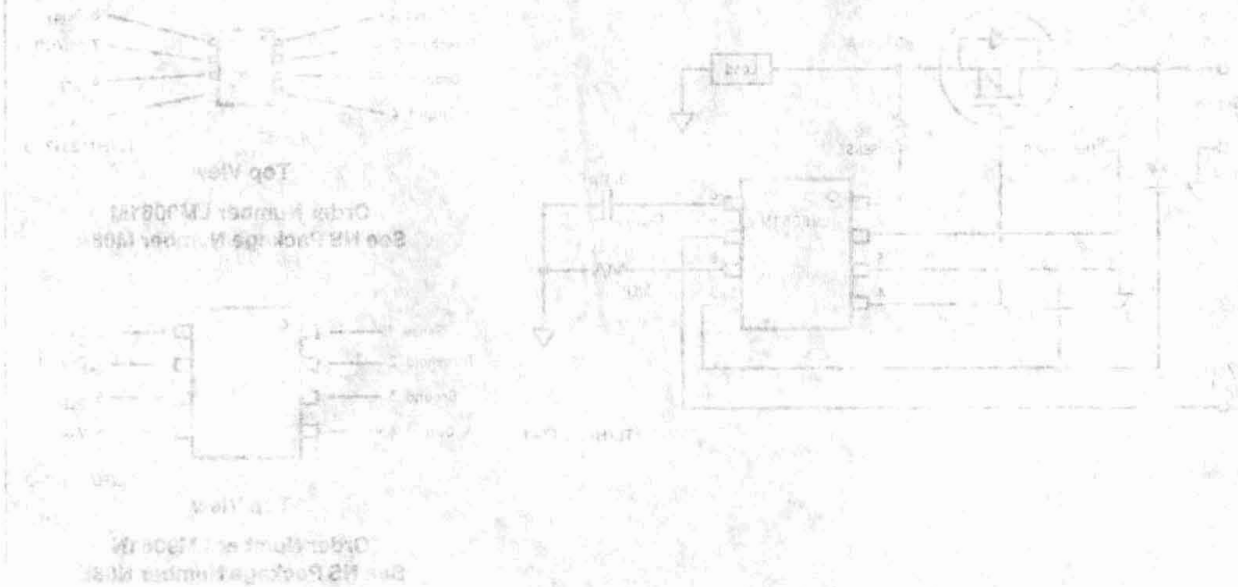
The error flag is an open collector output that pulls low under certain fault conditions. These errors include overvoltage (V_{CC} > 26V), overcurrent (I_{OUT} > 1.3A), undercurrent (I_{OUT} < 2 mA), output short circuit to ground, output short circuit to supply, and junction temperature greater than 150°C. By connecting a 2 kΩ resistor from the error flag output to a 5V supply a logic output to a microprocessor is provided.

The error flag can give seemingly false indications in a number of situations. Slewing large capacitive loads (>100 nF) can drive the LM1951 into temporary current limit, producing a momentary error indication. Incandescent lamps and DC motors require an inrush current that will also cause a temporary current limit and error indication. Large inductive loads (>50 mH) initially appear as open circuits, falsing the error flag. The error flag pulses for about 1 μs when any load is turned ON since the output is initially at ground. In microprocessor systems these false indications are easily ignored in software. In discrete logic circuits utilizing a latch at the error flag output, some filtering may be required.

An internal current sink (10 μA minimum) is connected to the input, pin 5. If this pin is left open it is guaranteed to pull low, switching the LM1951 OFF. This characteristic is important under certain fault conditions such as when the control line fails open cirucit.

Although the input threshold has hysteresis, the switch points are derived from a very stable band-gap reference. In many applications, such as *Figures 5* and *7*, the LM1951 input can replace an extenal reference and comparator.

The input (pin 5) is clamped at −0.7V and includes a series resistance of approximately 30 kΩ. This pin tolerates negative inputs of up to 1 mA without affecting the performance of the chip.



National Semiconductor

LM9061
Power MOSFET Driver with Lossless Protection

General Description

The LM9061 is a charge-pump device which provides the gate drive to any size external power MOSFET configured as a high side driver or switch. A CMOS logic compatible ON/OFF input controls the output gate drive voltage. In the ON state, the charge pump voltage, which is well above the available V_{CC} supply, is directly applied to the gate of the MOSFET. A built-in 15V zener clamps the maximum gate to source voltage of the MOSFET. When commanded OFF a 110 μA current sink discharges the gate capacitances of the MOSFET for a gradual turn-OFF characteristic to minimize the duration of inductive load transient voltages and further protect the power MOSFET.

Lossless protection of the power MOSFET is a key feature of the LM9061. The voltage drop (V_{DS}) across the power device is continually monitored and compared against an externally programmable threshold voltage. A small current sensing resistor in series with the load, which causes a loss of available energy, is not required for the protection circuitry. Should the V_{DS} voltage, due to excessive load current, exceed the threshold voltage, the output is latched OFF in a more gradual fashion (through a 10 μA output current sink) after a programmable delay time interval.

Designed for the automotive application environment the LM9061 has a wide operating temperature range of $-40°C$ to $+125°C$, remains operational with V_{CC} up to 26V, and can withstand 60V power supply transients. The LM9061 is available in an 8-pin small outline package, and an 8-pin dual in-line package.

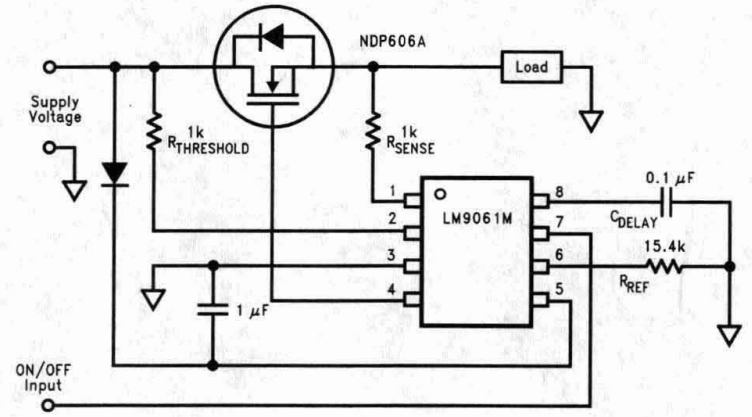
Features

- Built-in charge pump for gate overdrive of high side drive applications
- Lossless protection of the power MOSFET
- Programmable MOSFET protection voltage
- Programmable delay of protection latch-OFF
- Fast turn-ON (1.5 ms max with gate capacitance of 25000 pF)
- Undervoltage shut OFF with $V_{CC} < 7V$
- Overvoltage shut OFF with $V_{CC} > 26V$
- Withstands 60V supply transients
- CMOS logic compatible ON/OFF control input
- Surface mount and dual in-line packages available

Applications

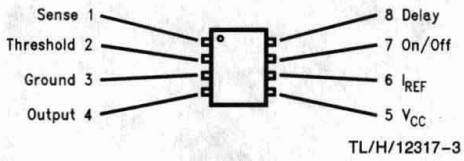
- Valve, relay and solenoid drivers
- Lamp drivers
- DC motor PWM drivers
- Logic controlled power supply distribution switch
- Electronic circuit breaker

Typical Application



TL/H/12317–1

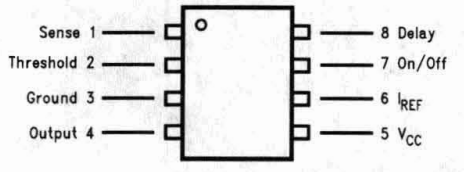
Connection Diagrams



TL/H/12317–3

Top View

Order Number LM9061M
See NS Package Number M08A



TL/H/12317–2

Top View

Order Number LM9061N
See NS Package Number N08E

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	60V
Reverse Supply Current	20 mA
Output Voltage	V_{CC} + 15V
Voltage at Sense and Threshold (through 1 kΩ)	−25V to +60V
ON/OFF Input Voltage	−0.3V to V_{CC} + 0.3V
Junction Temperature	150°C
Storage Temperature	−55°C to 150°C
Lead Temperature (Soldering, 10 seconds)	260°C

Operating Ratings (Note 2)

Supply Voltage	7V to 26V
ON/OFF Input Voltage	−0.3V to V_{CC}
Ambient Temperature Range	−40°C to 125°C
Thermal Resistance (θ_{J-A})	
LM9061M	150°C/W
LM9061N	100°C/W

DC Electrical Characteristics

7V ≤ V_{CC} ≤20V, R_{REF} = 15.4 kΩ, −40°C ≤ T_J ≤ +125°C, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Max	Units
POWER SUPPLY					
I_Q	Quiescent Supply Current	ON/OFF = "0"		5	mA
I_{CC}	Operating Supply Current	ON/OFF = "1", C_{LOAD} = 0.025 μF, Includes Turn-ON Transient Output Current		40	mA
ON/OFF CONTROL INPUT					
$V_{IN}(0)$	ON/OFF Input Logic "0"	V_{OUT} = OFF		1.5	V
$V_{IN}(1)$	ON/OFF Input Logic "1"	V_{OUT} = ON	3.5		V
V_{HYST}	ON/OFF Input Hysteresis	Peak to Peak	0.8	2	V
I_{IN}	ON/OFF Input Pull-Down Current	VON/OFF = 5V	50	250	μA
GATE DRIVE OUTPUT					
V_{OH}	Charge Pump Output Voltage	ON/OFF = "1"	V_{CC} + 7	V_{CC} + 15	V
V_{OL}	OFF Output Voltage	ON/OFF = "0", I_{SINK} = 110 μA		0.9	V
V_{CLAMP}	Sense to Output Clamp Voltage	ON/OFF = "1", V_{SENSE} = $V_{THRESHOLD}$	11	15	V
$I_{SINK(Normal-OFF)}$	Output Sink Current, Normal Operation	ON/OFF = "0", V_{DELAY} = 0V, V_{SENSE} = $V_{THRESHOLD}$	75	145	μA
$I_{SINK(Latch-OFF)}$	Output Sink Current with Protection Comparator Tripped	V_{DELAY} = 7V, V_{SENSE} < $V_{THRESHOLD}$	5	15	μA
PROTECTION CIRCUITRY					
I_{REF}	Threshold Pin Reference Current	V_{SENSE} = $V_{THRESHOLD}$	75	88	μA
V_{REF}	Reference Voltage		1.15	1.35	V
$I_{THR(LEAKAGE)}$	Threshold Pin Leakage Current	V_{CC} = Open, 7V ≤ $V_{THRESHOLD}$ ≤ 20V		10	μA
I_{SENSE}	Sense Pin Input Bias Current	V_{SENSE} = $V_{THRESHOLD}$		10	μA
DELAY TIMER					
I_{DELAY}	Delay Pin Source Current		6.74	15.44	μA
V_{TIMER}	Delay Timer Threshold Voltage		5	6.2	V
I_{DIS}	Delay Capacitor Discharge Current	V_{DELAY} = 5V	2	10	mA
V_{SAT}	Discharge Transistor Saturation Voltage	I_{DIS} = 1 mA		0.4	V

AC Timing Characteristics

$7V \le V_{CC} \le 20V$, $R_{REF} = 15.4\ k\Omega$, $-40°C \le T_J \le +125°C$, $C_{LOAD} = 0.025\ \mu F$, $C_{DELAY} = 0.022\ \mu F$, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Max	Units
T_{ON}	Output Turn-ON Time	$C_{LOAD} = 0.025\ \mu F$ $7V \le V_{CC} \le 10V$, $V_{OUT} \ge V_{CC} + 7V$ $10V \le V_{CC} \le 20V$, $V_{OUT} \ge V_{CC} + 11V$		1.5 1.5	ms ms
$T_{OFF(Normal)}$	Output Turn-OFF Time, Normal Operation (Note 4)	$C_{LOAD} = 0.025\ \mu F$ $V_{CC} = 14V$, $V_{OUT} \ge 25V$ $V_{SENSE} = V_{THRESHOLD}$	4	10	ms
$T_{OFF(Latch-OFF)}$	Output Turn-OFF Time, Protection Comparator Tripped (Note 4)	$C_{LOAD} = 0.025\ \mu F$ $V_{CC} = 14V$, $V_{OUT} \ge 25V$ $V_{SENSE} = V_{THRESHOLD}$	45	140	ms
T_{DELAY}	Delay Timer Interval	$C_{DELAY} = 0.022\ \mu F$	8	18	ms

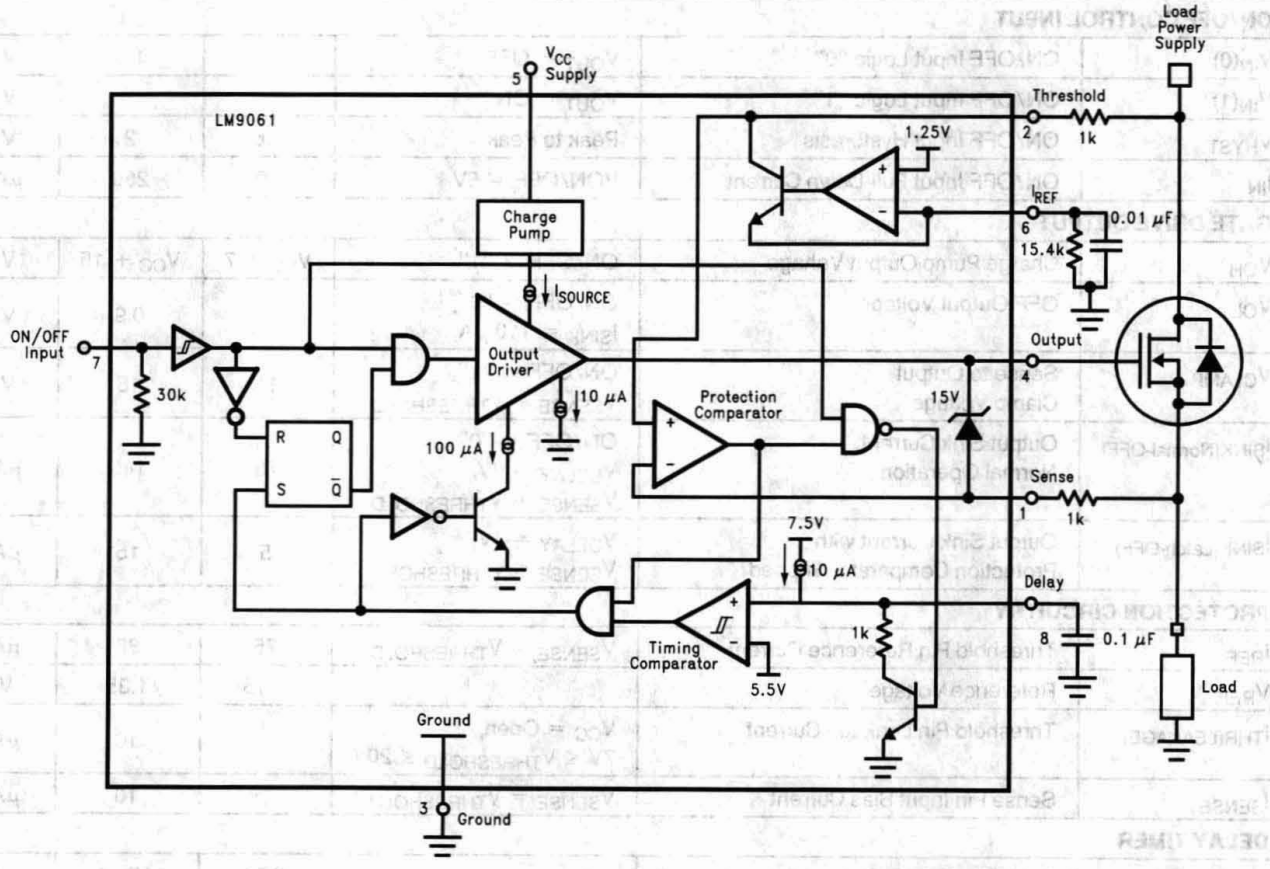
Note 1: Absolute Maximum Ratings indicate the limits beyond which damage to the device may occur.

Note 2: Operating Ratings indicate conditions for which the device is intended to be functional, but may not meet the guaranteed specific performance limits. For guaranteed specifications and test conditions see the Electrical Characteristics.

Note 3: ESD Human Body Model: 100 pF discharged through 1500Ω resistor.

Note 4: The AC Timing specifications for T_{OFF} are not production tested, and therefore are not specifically guaranteed. Limits are provided for reference purposes only. Smaller load capacitances will have proportionally faster turn-ON and turn-OFF times.

Block Diagram



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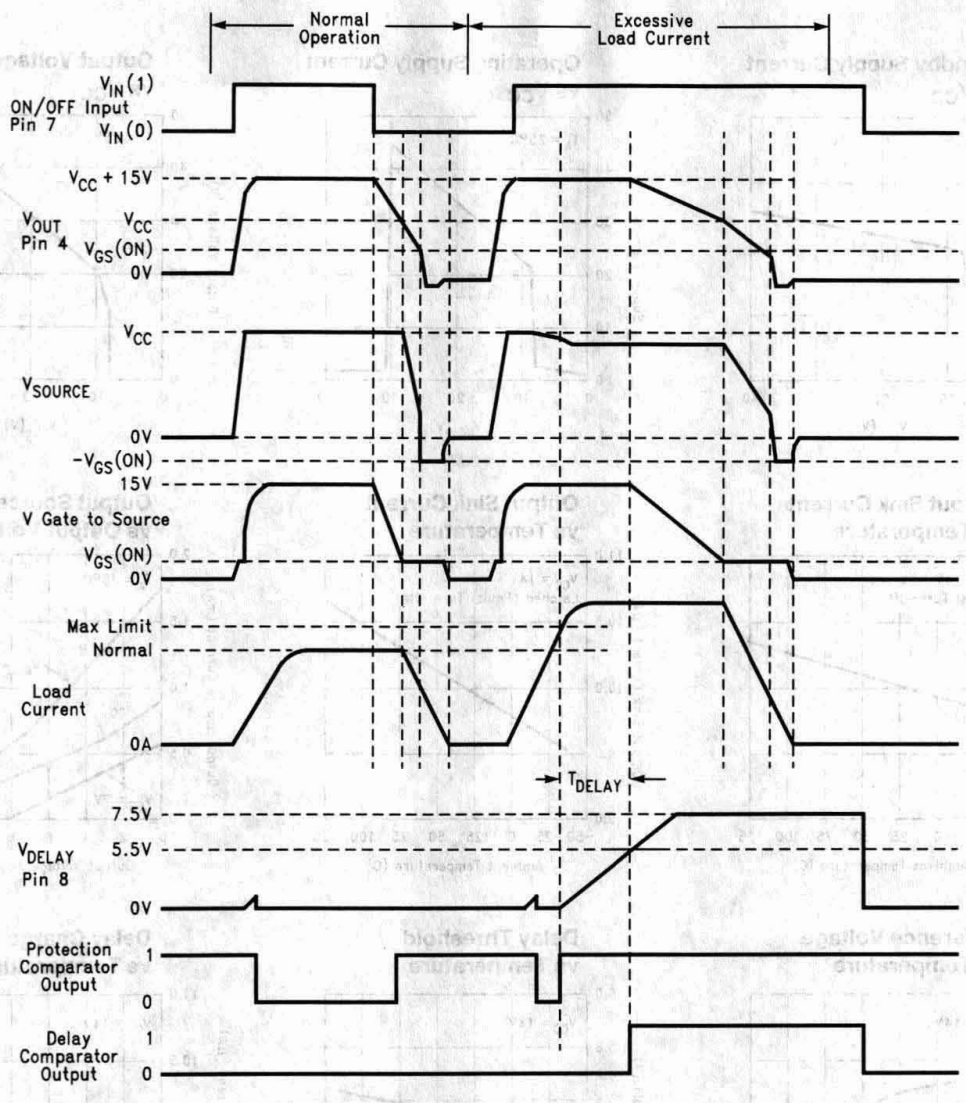
Typical Operating Waveforms



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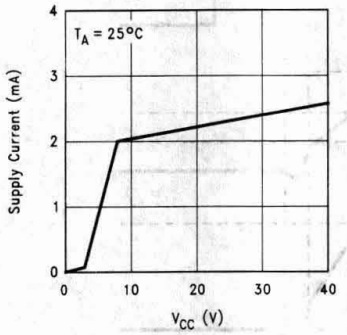
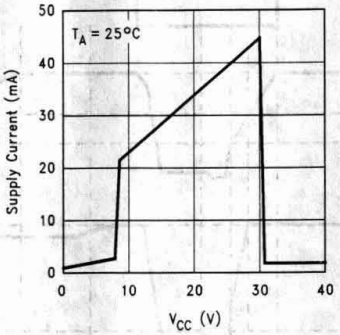
Typical Electrical Characteristics

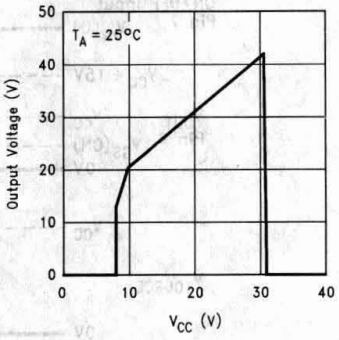
Standby Supply Current vs V_{CC}



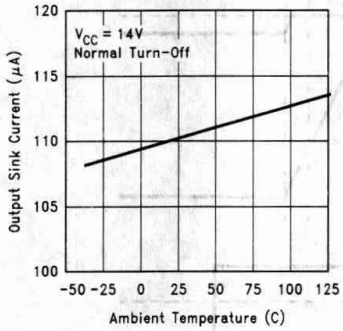
Operating Supply Current vs V_{CC}



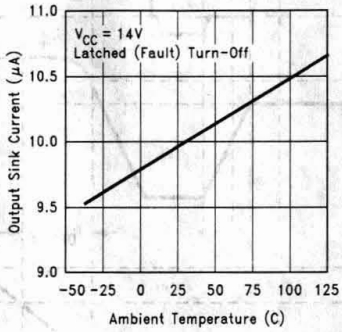
Output Voltage vs V_{CC}



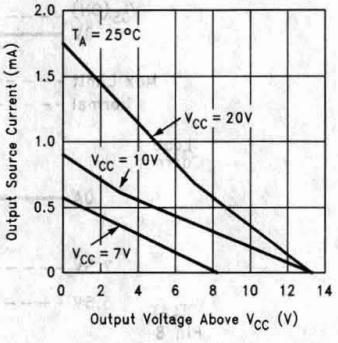
Output Sink Current vs Temperature



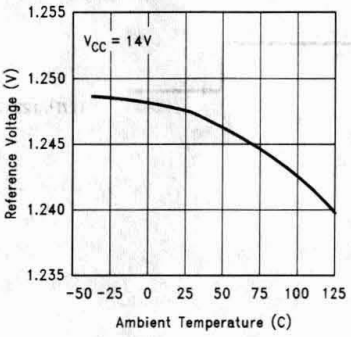
Output Sink Current vs Temperature



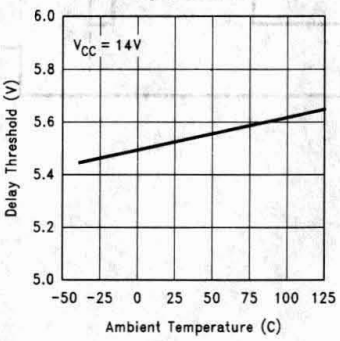
Output Source Current vs Output Voltage



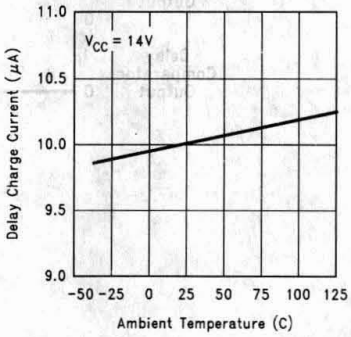
Reference Voltage vs Temperature



Delay Threshold vs Temperature



Delay Charge Current vs Temperature



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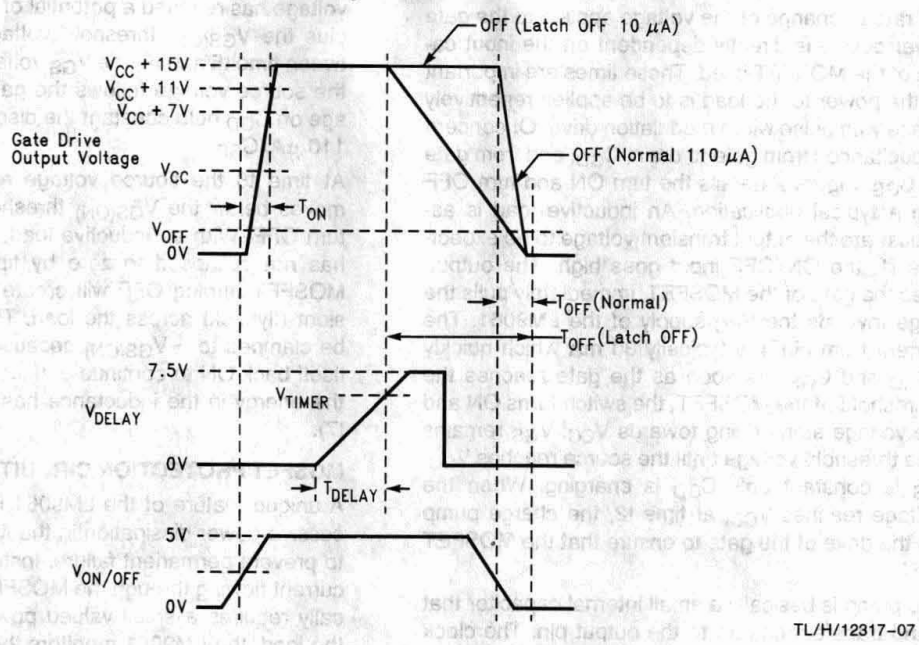
Typical Electrical Characteristics (Continued)

Timing Definitions



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Application Hints

BASIC OPERATION

The LM9061 contains a charge pump circuit that generates a voltage in excess of the applied supply voltage to provide gate drive voltage to power MOSFET transistors. Any size of N-channel power MOSFET, including multiple parallel connected MOSFETs for very high current applications, can be used to apply power to a ground referenced load circuit in what is referred to as "high side drive" applications. *Figure 1* shows the basic application of the LM9061.

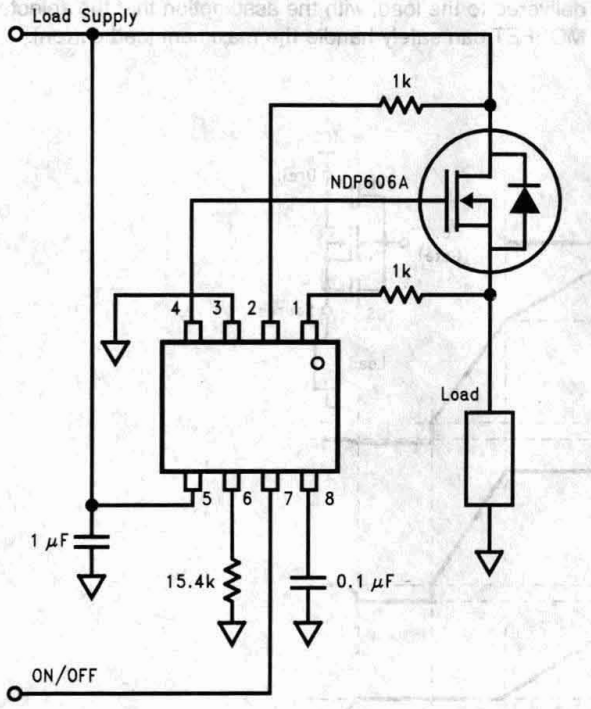

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FIGURE 1. Basic Application Circuit

When commanded ON by a logic "1" input to pin 7, the gate drive output, pin 4, rises quickly to the V_{CC} supply potential at pin 5. Once the gate voltage exceeds the gate-source threshold voltage of the MOSFET, $V_{GS(ON)}$, (the source is connected to ground through the load) the MOSFET turns ON and connects the supply voltage to the load. With the source at near the supply potential, the charge pump continues to provide a gate voltage greater than the supply to keep the MOSFET turned ON. To protect the gate of the MOSFET, the output voltage of the LM9061 is clamped to limit the maximum V_{GS} to 15V.

It is important to remember that during the Turn-ON of the MOSFET the output current to the Gate is drawn from the V_{CC} supply pin. The V_{CC} pin should be bypassed with a capacitor with a value of at least ten times the Gate capacitance, and no less than 0.1 μF. The output current into the Gate will typically be 30 mA with V_{CC} at 14V and the Gate at 0V. As the Gate voltage rises to V_{CC}, the output current will decrease. When the Gate voltage reaches V_{CC}, the output current will typically be 1 mA with V_{CC} at 14V.

A logic "0" on pin 7 turns the MOSFET OFF. When commanded OFF a 110 μA current sink is connected to the output pin. This current discharges the gate capacitances of the MOSFET linearly. When the gate voltage equals the source voltage (which is near the supply voltage) plus the $V_{GS(ON)}$ threshold of the MOSFET, the source voltage starts following the gate voltage and ramps toward ground. Eventually the source voltage equals 0V and the gate continues to ramp to zero thus turning OFF the power device. This gradual Turn-OFF characteristic, instead of an abrupt removal of the gate drive, can, in some applications, minimize the power dissipation in the MOSFET or reduce the duration of negative transients, as is the case when driving inductive loads. In the event of an overstress condition on the power device, the turn OFF characteristic is even more gradual as the output sinking current is only 10 μA (see Protection Circuitry Section).

Application Hints (Continued)

TURN ON AND TURN OFF CHARACTERISTICS

The actual rate of change of the voltage applied to the gate of the power device is directly dependent on the input capacitances of the MOSFET used. These times are important to know if the power to the load is to be applied repetitively as is the case with pulse width modulation drive. Of concern are the capacitances from gate to drain, C_{GD}, and from gate to source, C_{GS}. *Figure 2* details the turn ON and turn OFF intervals in a typical application. An inductive load is assumed to illustrate the output transient voltage to be expected. At time t1, the ON/OFF input goes high. The output, which drives the gate of the MOSFET, immediately pulls the gate voltage towards the V_{CC} supply of the LM9061. The source current from pin 4 is typically 30 mA which quickly charges C_{GD} and C_{GS}. As soon as the gate reaches the $V_{GS(ON)}$ threshold of the MOSFET, the switch turns ON and the source voltage starts rising towards V_{CC}. V_{GS} remains equal to the threshold voltage until the source reaches V_{CC}. While V_{GS} is constant only C_{GD} is charging. When the source voltage reaches V_{CC}, at time t2, the charge pump takes over the drive of the gate to ensure that the MOSFET remains ON.

The charge pump is basically a small internal capacitor that acquires and transfers charge to the output pin. The clock rate is set internally at typically 300 kHz. In effect the charge pump acts as a switched capacitor resistor (approximately 67k) connected to a voltage that is clamped at 13V above the Sense input pin of the LM9061 which is equal to the V_{CC} supply in typical applications. The gate voltage rises above V_{CC} in an exponential fashion with a time constant dependent upon the sum of C_{GD} and C_{GS}. At this time however the load is fully energized. At time t3, the charge pump reaches its maximum potential and the switch remains ON.

At time t4, the ON/OFF input goes low to turn OFF the MOSFET and remove power from the load. At this time the charge pump is disconnected and an internal 110 μA current sink begins to discharge the gate input capacitances to ground. The discharge rate ($\Delta V/\Delta T$) is equal to 110 $\mu A/(C_{GD} + C_{GS})$.

The load is still fully energized until time t5 when the gate voltage has reached a potential of the source voltage (V_{CC}) plus the $V_{GS(ON)}$ threshold voltage of the MOSFET. Between time t5 and t6, the V_{GS} voltage remains constant and the source voltage follows the gate voltage. With the voltage on C_{GD} held constant the discharge rate now becomes 110 $\mu A/C_{GD}$.

At time t6 the source voltage reaches 0V. As the gate moves below the $V_{GS(ON)}$ threshold the MOSFET tries to turn OFF. With an inductive load, if the current in the load has not collapsed to zero by time t6, the action of the MOSFET turning OFF will create a negative voltage transient (flyback) across the load. The negative transient will be clamped to $-V_{GS(ON)}$ because the MOSFET must turn itself back ON to continue conducting the load current until the energy in the inductance has been dissipated (at time t7).

MOSFET PROTECTION CIRCUITRY

A unique feature of the LM9061 is the ability to sense excessive power dissipation in the MOSFET and latch it OFF to prevent permanent failure. Instead of sensing the actual current flowing through the MOSFET to the load, which typically requires a small valued power resistor in series with the load, the LM9061 monitors the voltage drop from drain to source, V_{DS}, across the MOSFET. This "lossless" technique allows all of the energy available from the supply to be conducted to the load as required. The only power loss is that of the MOSFET itself and proper selection of a particular power device for an application will minimize this concern. Another benefit of this technique is that all applications use only standard inexpensive ¼W or less resistors.

To utilize this lossless protection technique requires knowledge of key characteristics of the power MOSFET used. In any application the emphasis for protection can be placed on either the power MOSFET or on the amount of current delivered to the load, with the assumption that the selected MOSFET can safely handle the maximum load current.

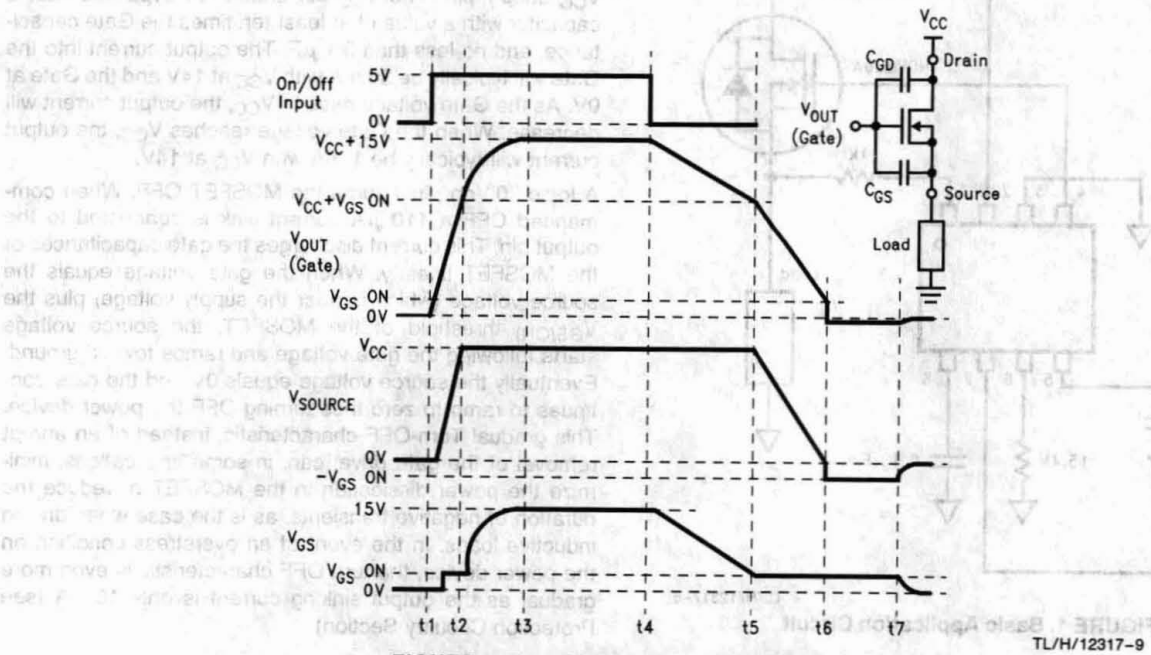

FIGURE 2. Turn ON and Turn OFF Waveforms

Application Hints (Continued)

To protect the MOSFET from exceeding its maximum junction temperature rating, the power dissipation needs to be limited. The maximum power dissipation allowed (derated for temperature) and the maximum drain to source ON resistance, $R_{DS(ON)}$, with both at the maximum operating ambient temperature, needs to be determined. When switched ON the power dissipation in the MOSFET will be:

$$P_{DISS} = \frac{V_{DS}^2}{R_{DS(ON)}}$$

The V_{DS} voltage to limit the maximum power dissipation is therefore:

$$V_{DS\,(MAX)} = \sqrt{P_{D\,(MAX)} \times R_{DS(ON)\,(MAX)}}$$

With this restriction the actual load current and power dissipation obtained will be a direct function of the actual $R_{DS(ON)}$ of the MOSFET at any particular ambient temperature but the junction temperature of the power device will never exceed its rated maximum.

To limit the maximum load current requires an estimate of the minimum $R_{DS(ON)}$ of the MOSFET (the minimum $R_{DS(ON)}$ of discrete MOSFETs is rarely specified) over the required operating temperature range.

The maximum current to the load will be:

$$I_{LOAD\,(MAX)} = \frac{V_{DS}}{R_{DS(ON)\,(MIN)}}$$

The maximum junction temperature of the MOSFET and/or the maximum current to the load can be limited by monitoring and setting a maximum operational value for the drain to source voltage drop, V_{DS}. In addition, in the event that the load is inadvertently shorted to ground, the power device will automatically be turned-OFF.

In all cases, should the MOSFET be switched OFF by the built in protection comparator, the output sink current is switched to only 10 μA to gradually turn OFF the power device.

Figure 3 illustrates how the threshold voltage for the internal protection comparator is established.

Two resistors connect the drain and source of the MOSFET to the LM9061. The Sense input, pin 1, monitors the source voltage while the Threshold input, pin 2, is connected to the drain, which is also connected to the constant load power supply. Both of these inputs are the two inputs to the protection comparator. Should the voltage at the sense input ever drop below the voltage at the threshold input, the protection comparator output goes high and initiates an automatic latch-OFF function to protect the power device. Therefore the switching threshold voltage of the comparator directly controls the maximum V_{DS} allowed across the MOSFET while conducting load current.

The threshold voltage is set by the voltage drop across resistor $R_{THRESHOLD}$. A reference current is fixed by a resistor to ground at I_{REF}, pin 6. To precisely regulate the reference current over temperature, a stable band gap reference voltage is provided to bias a constant current sink. The reference current is set by:

$$I_{REF} = \frac{V_{REF}}{R_{REF}}$$

The reference current sink output is internally connected to the threshold pin. I_{REF} then flows from the load supply through $R_{THRESHOLD}$. The fixed voltage drop across $R_{THRESHOLD}$ is approximately equal to the maximum value of V_{DS} across the MOSFET before the protection comparator trips.

It is important to note that the programmed reference current serves a multiple purpose as it is used internally for biasing and also has a direct effect on the internal charge pump switching frequency. The design of the LM9061 is optimized for a reference current of approximately 80 μA, set with a 15.4 kΩ $\pm$1% resistor for R_{REF}. To obtain the guaranteed performance characteristics it is recommended that a 15.4 kΩ resistor be used for R_{REF}.

The protection comparator is configured such that during normal operation, when the output of the comparator is low, the differential input stage of the comparator is switched in

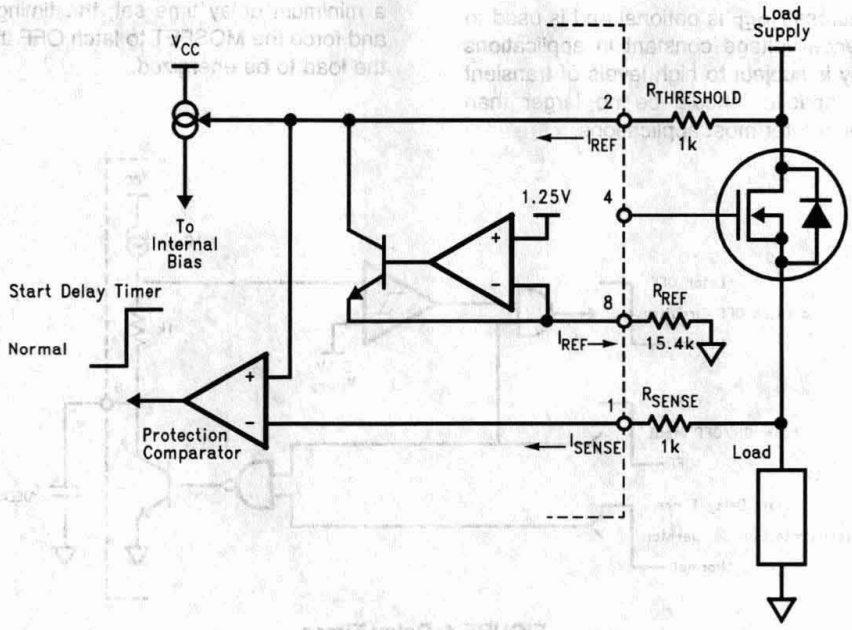

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FIGURE 3. Protection Comparator Biasing

Application Hints (Continued)

a manner that there is virtually no current flowing into the non-inverting input of the comparator. Therefore, only I_{REF} flows through resistor $R_{THRESHOLD}$. All of the input bias current, 20 μA maximum, for the comparator input stage (twice the I_{SENSE} specification of 10 μA maximum, defined for equal potentials on each of the comparator inputs) however flows into the inverting input through resistor R_{SENSE}. At the comparator threshold, the current through R_{SENSE} will be no more than the I_{SENSE} specification of 10 μA.

To tailor the $V_{DS\ (MAX)}$ threshold for any particular application, the resistor $R_{THRESHOLD}$ can be selected per the following formula:

$$V_{DS\ (MAX)} = \frac{V_{REF} \times R_{THR}}{R_{REF}} - (I_{SENSE} \times R_{SENSE}) + V_{OS}$$

where R_{REF} = 15.4 kΩ, I_{SENSE} is the input bias current to the protection comparator, R_{SENSE} is the resistor connected to pin 1 and V_{OS} is the offset voltage of the protection comparator (typically in the range of $\pm$10 mV).

The resistor R_{SENSE} is optional, but is strongly recommended to provide transient protection for the Sense pin, especially when driving inductive type loads. A minimum value of 1 kΩ will protect the pin from transients ranging from $-$25V to $+$60V. This resistor should be equal to, or less than, the resistor used for $R_{THRESHOLD}$. Never set R_{SENSE} to a value larger than $R_{THRESHOLD}$. When the protection comparator output goes high, the total bias current for the input stage transfers from the Sense pin to the Threshold pin, thereby changing the voltages present at the inputs to the comparator. For consistent switching of the comparator right at the desired threshold point, the voltage drop that occurs at the non-inverting input (Threshold) should equal, or exceed, the rise in voltage at the inverting input (Sense).

In automotive applications the load supply may be the battery of the vehicle whereas the V_{CC} supply for the LM9061 is a switched ignition supply. When the V_{CC} supply is switched OFF there is always a concern for the amount of current drained from the battery. The only current drain under this condition is a leakage current into the Threshold pin which is less than 10 μA.

A bypass capacitor across R_{REF} is optional and is used to help keep the reference voltage constant in applications where the V_{CC} supply is subject to high levels of transient noise. This bypass capacitor should be no larger than 0.1 μF, and is not needed for most applications.

DELAY TIMER

To allow the MOSFET to conduct currents beyond the protection threshold for a brief period of time, a delay timer function is provided. This timer delays the actual latching OFF of the MOSFET for a programmable interval. This feature is important to drive loads which require a surge of current in excess of the normal ON current upon start up, or at any point in time, such as lamps and motors. *Figure 4* details the delay timer circuitry. A capacitor connected from the Delay pin 8, to ground sets the delay time interval. With the MOSFET turned ON and all conditions normal, the output of the protection comparator is low and this keeps the discharge transistor ON. This transistor keeps the delay capacitor discharged. Should a surge of load current trip the protection comparator high, the discharge transistor turns OFF and an internal 10 μA current source begins linearly charging the delay capacitor.

If the surge current, with excessive V_{DS} voltage, lasts long enough for the capacitor to charge to the timing comparator threshold of typically 5.5V, the output of the comparator will go high to set a flip-flop and immediately latch the MOSFET OFF. It will not re-start until the ON/OFF Input is toggled low then high.

The delay time interval is set by the selection of C_{DELAY} and can be found from:

$$T_{DELAY} = \frac{(V_{TIMER} \times C_{DELAY})}{I_{DELAY}}$$

where typically V_{TIMER} = 5.5V and I_{DELAY} = 10μA.

Charging of the delay capacitor is clamped at approximately 7.5V which is the internal bias voltage for the 10 μA current source.

MINIMUM DELAY TIME

A minimum delay time interval is required in all applications due to the nature of the protection circuitry. At the instant the MOSFET is commanded ON, the voltage across the MOSFET, V_{DS}, is equal to the full load supply voltage because the source is held at ground by the load. This condition will immediately trip the protection comparator. Without a minimum delay time set, the timing comparator will trip and force the MOSFET to latch OFF thereby never allowing the load to be energized.

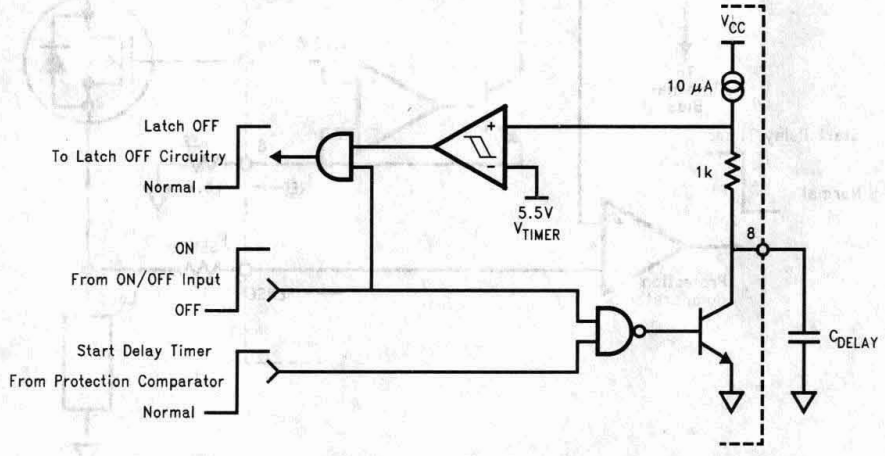

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FIGURE 4. Delay Timer

Application Hints (Continued)

To prevent this situation a delay capacitor is required at pin 8. The selection of a minimum capacitor value to ensure proper start-up depends primarily on the load characteristics and how much time is required for the MOSFET to raise the load voltage to the point where the Sense input is more positive than the Threshold input ($T_{START-UP}$). Some experimentation is required if a specific minimum delay time characteristic is desired. Therefore:

$$C_{DELAY} = \frac{(I_{DELAY} \times T_{START-UP})}{V_{TIMER}}$$

In the absence of a specific delay time requirement, a value for C_{DELAY} of 0.1 μF is recommended.

OVER VOLTAGE PROTECTION

The LM9061 will remain operational with up to +26V on V_{CC}. If V_{CC} increases to more than typically +30V the LM9061 will turn off the MOSFET to protect the load from excessive voltage. When V_{CC} has returned to the normal operating range the device will return to normal operation without requiring toggling the ON/OFF input. This feature will allow MOSFET operation to continue in applications that are subject to periodic voltage transients, such as automotive applications.

For circuits where the load is sensitive to high voltages, the circuit shown in *Figure 5* can be used. The addition of a zener on the Sense input (pin 1) will provide a maximum voltage reference for the Protection Comparator. The Sense resistor is required in this application to limit the zener current. When the device is ON, and the load supply attempts to rise higher than (V_{ZENER} + $V_{THRESHOLD}$), the Protection comparator will trip, and the Delay Timer will start. If the high supply voltage condition lasts long enough for the Delay Timer to time out, the MOSFET will be latched off. The ON/OFF input will need to be toggled to restart the MOSFET.

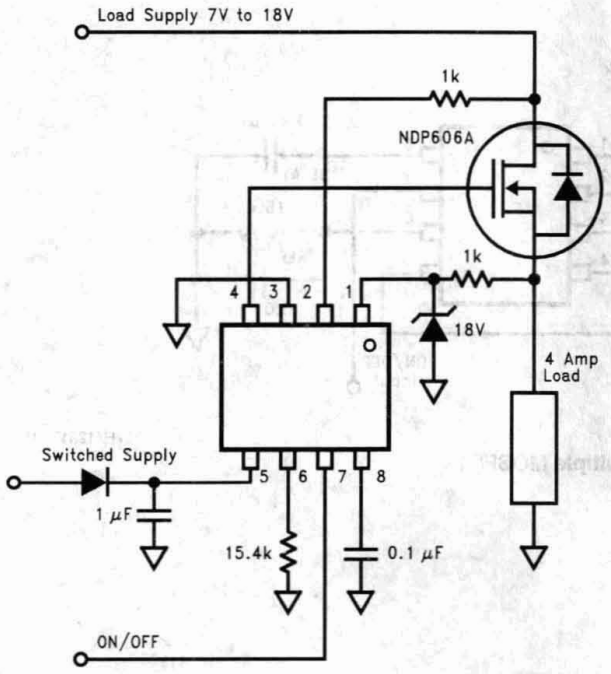

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FIGURE 5. Adding Over-Voltage Protection

REVERSE BATTERY

The LM9061 is not protected against reverse polarity supply connections. If the V_{CC} supply should be taken negative with respect to ground, the current from the V_{CC} pin should be limited to 20 mA. The addition of a diode in series with the V_{CC} input is recommended. This diode drop does not subtract significantly from the charge pump gate overdrive output voltage.

LOW BATTERY

As an additional protection feature the LM9061 incorporates an Undervoltage Shut-OFF function. If the V_{CC} supply to the package drops below 7V, where it may not be assured that the MOSFET is actually ON when it should be, circuitry will automatically turn OFF the power MOSFET.

Figure 6 shows the LM9061 used as an electronic circuit breaker. This circuit provides low voltage shutdown, overvoltage latch OFF, and overcurrent latch OFF. In the event of a latch OFF shutdown, the circuit can be reset by shutting the main supply off, then back on. An optional reset switch on the ON/OFF pin will allow a "push-button reset" of the circuit after latching OFF.

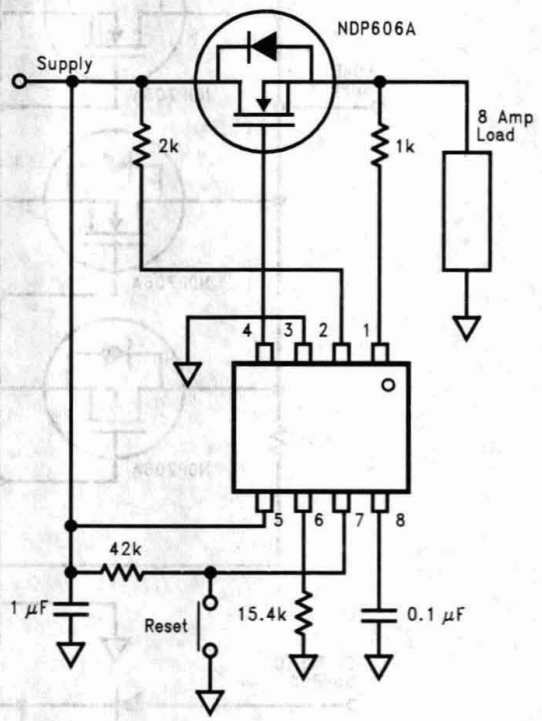

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FIGURE 6. Electronic Circuit Breaker

Scaling of the external resistor value, from V_{CC} to the ON/OFF input pin, with the internal 30k resistor can be used to increase the startup voltage. The circuit operation then becomes dependent on the resistor ratio and V_{CC} providing an ON/OFF pin voltage being above the ON threshold rather than the LM9061 low V_{CC} shutdown feature.

DRIVING MOSFET ARRAYS

The LM9061 is an ideal driver for any application that requires multiple parallel MOSFETs to provide the necessary load current. Only a few "common sense" precautions need to be observed. All MOSFETs in the array must have identical electrical and thermal characteristics. This can be solved by using the same part number from the same

Application Hints (Continued)

manufacturer for all of the MOSFETs in the array. Also, all MOSFETs should have the same style heat sink or, ideally, all mounted on the same heat sink. The electrical connection of the MOSFETs should get special attention. With typical $R_{DS(ON)}$ values in the range of tens of milli-Ohms, a poor electrical connection for one of the MOSFETs can render it useless in the circuit.

Figure 7 shows a circuit with four parallel NDP706A MOSFETs. This particular MOSFET has a typical $R_{DS(ON)}$ of 0.013Ω with a T_J of 25°C, and 0.020Ω with a T_J of +125°C.

With the V_{DS} threshold voltage being set to 500 mV, this circuit will provide a typical maximum load current of 150A at 25°C, and a typical maximum load current of 100A at 125°C. The maximum dissipation, per MOSFET, will be nearly 20W at 25°C, and 12.5W at 125°C. With up to 20W being dissipated by each of the four devices, an effective heat sink will be required to keep the T_J as low as possible when operating near the maximum load currents.

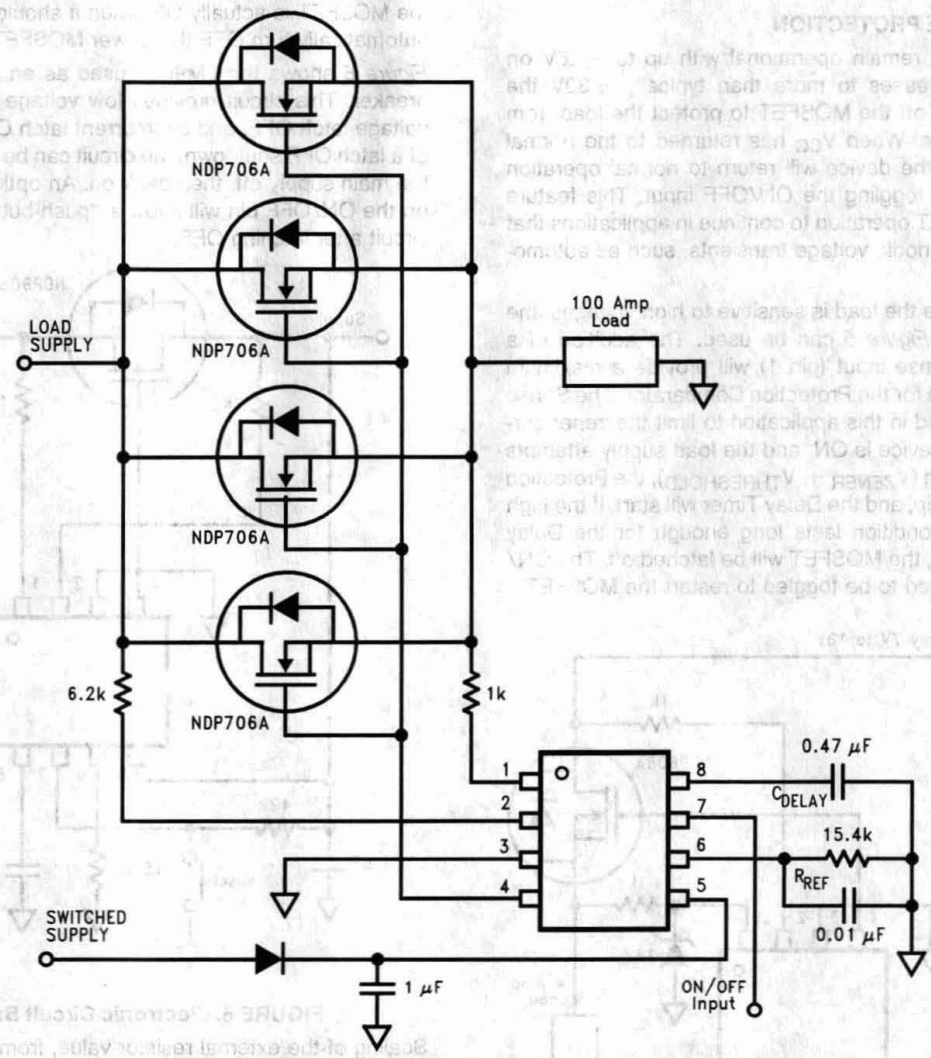

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FIGURE 7. Driving Multiple MOSFETs

Application Hints (Continued)

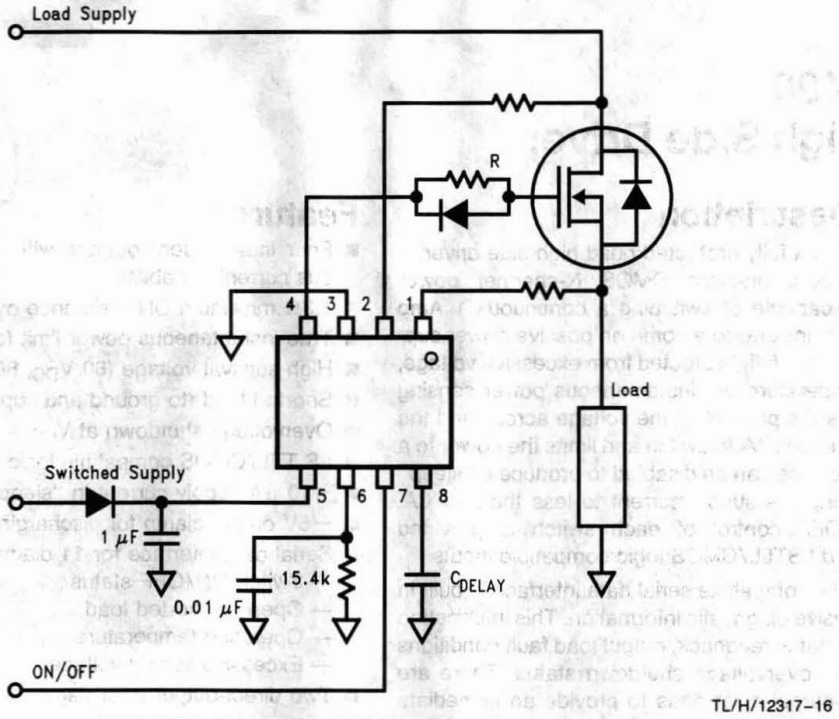

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FIGURE 8. Increasing MOSFET Turn On Time

INCREASING MOSFET TURN ON TIME

The ability of the LM9061 to quickly turn on the MOSFET is an important factor in the management of the MOSFET power dissipation. Caution should be exercised when attempting to increase the MOSFET Turn On time by limiting the Gate drive current. The MOSFET average dissipation, and the LM9061 Delay time, must be recalculated with the extended switching transition time.

Figure 8 shows a method of increasing the MOSFET Turn On time, without affecting the Turn Off time. In this method the Gate is charged at an exponential rate set by the added external Gate resistor and the MOSFET Gate capacitances.

Although the LM9061 will drive MOSFETs from any manufacturer, National Semiconductor offers a wide range of power MOSFETs. *Figure 9* shows a small sample of the devices available.

Part	I_D	V_{DSS}	$R_{DS(ON)}$	Package
NDP706A	75A	60V	0.015Ω	TO-220
NDP706B	70A	60V	0.018Ω	TO-220
NDP708A	60A	80V	0.022Ω	TO-220
NDB708A	60A	80V	0.022Ω	TO-263
NDP606A	48A	60V	0.025Ω	TO-220
NDP606B	42A	60V	0.028Ω	TO-220
NDP608A	36A	80V	0.042Ω	TO-220
NDB608A	36A	80V	0.042Ω	TO-263
NDP508A	19A	80V	0.080Ω	TO-220
NDB508A	19A	80V	0.080Ω	TO-263
NDP408A	11A	80V	0.160Ω	TO-220
NDS9410	7A	30V	0.03Ω	SO-8
NDS9936*	5A	30V	0.05Ω	SO-8
NDS9945*	3.5A	60V	0.10Ω	SO-8

* Dual

FIGURE 9. Recommended DMOS Power MOSFETs

National Semiconductor

LMD18400
Quad High Side Driver

General Description

The LMD18400 is a fully protected quad high side driver. It contains four common-drain DMOS N-channel power switches, each capable of switching a continuous 1 Amp load (>3 Amps transient) to a common positive power supply. The switches are fully protected from excessive voltage, current and temperature. An instantaneous power sensing circuit calculates the product of the voltage across and the current through each DMOS switch and limits the power to a safe level. The device can be disabled to produce a "sleep" condition reducing the supply current to less than 10 μA. Separate ON/OFF control of each switch is provided through standard LSTLL/CMOS logic compatible inputs.

A MICROWIRE™ compatible serial data interface is built in to provide extensive diagnostic information. This information includes switch status readback, output load fault conditions and thermal and overvoltage shutdown status. There are also two direct-output error flags to provide an immediate indication of a general system fault and an indication of excessive operating temperature.

The LMD18400 is packaged in a special power dissipating leadframe that reduces the junction to case thermal resistance to approximately 20°C/W.

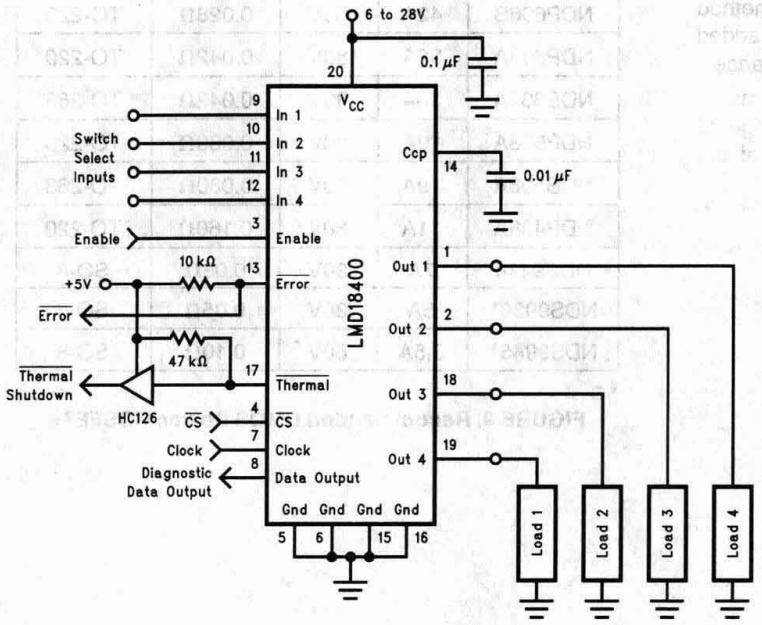
Features

- Four independent outputs with >3A peak, 1A continuous current capability
- 1.3Ω maximum ON resistance over temperature
- True instantaneous power limit for each switch
- High survival voltage (60 V_{DC}, 80V transient)
- Shorted load (to ground and supply) protection
- Overvoltage shutdown at V_{CC} > 35V
- LS TTL/CMOS compatible logic inputs and outputs
- <10 μA supply current in "sleep" mode
- −5V output clamp for discharging inductive loads
- Serial data interface for 11 diagnostic checks:
  - — Switch ON/OFF status
  - — Open or shorted load
  - — Operating temperature
  - — Excessive supply voltage
- Two direct-output error flags

Applications

- Relay and solenoid drivers
- High impedance automotive fuel injector drivers
- Lamp drivers
- Power supply switching
- Motor drivers

Typical Application



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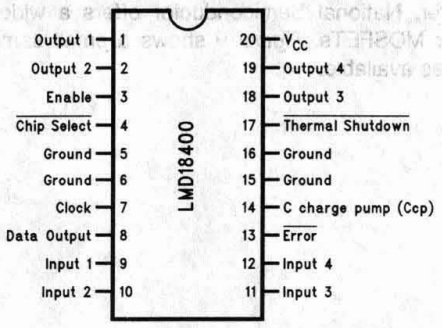
Connection Diagram



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Order Number LMD18400N
See NS Package Number N20A

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Survival Voltage (Pin 20)	
Transient (t = 10 ms)	80V
Continuous	−0.5V to +60V
Output Transient Current (Each Switch)	3.75A
Output Transient Current (Total, All Switches)	6A
Output Steady State Current (Each Switch)	1A
Logic Input Voltage (Pins 3, 9, 10, 11, 12)	−0.3V to +16V
Logic Input Voltage (Pins 4, 7)	−0.3V to +6V
Error Flag Voltage	16V
ESD Susceptibility (Note 2)	2000V
Power Dissipation (Note 3)	5W
	Internally Limited
Junction Temperature ($T_{J_{Max}}$)	150°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 Sec.)	+260°C

Operating Ratings (Note 1)

Ambient Temperature Range (T_A)	−40°C to +125°C
Supply Voltage Range	6V to 28V

Electrical Characteristics

V_{CC} = 12V, C_{CP} = 0.01 μFd, unless otherwise indicated. **Boldface** limits apply over the entire operating temperature range, −40°C ≤ T_A ≤ +125°C, all other limits are for T_A = T_J = +25°C.

Parameter	Conditions	Typical (Note 4)	Limit (Note 5)	Units (Limit)
DC CHARACTERISTICS				
Supply Current	Enable Input = 0V	0.04	10	μA (Max)
	Enable Input = 5V, Inputs = 0V	7.5	15	mA (Max)
	Enable Input = 5V, Inputs = 5V Open Loads	7.5	15	mA (Max)
Output Leakage	Enable Input = 0V, Inputs = 0V (Pins 1, 2, 18, 19)	0.01	10	μA (Max)
Rds ON	I_{OUT} = 1A, (Note 6)	0.8	**1.3**	Ω (Max)
Short Circuit Current	V_{CC} = 12V, (Note 6)	1.2	0.8	A (Min)
	V_{CC} = 6V, (Note 6)	2.4		A
	V_{CC} = 28V, (Note 6)	0.6		A
Maximum Output Current	$V_{CC} - V_O$ = 4V, (Note 6)	3.75		A
Load Error Threshold Voltage	Pins 1, 2, 18, 19	4.1		V
Open Load Detection Current	Pins 1, 2, 18, 19	150		μA
Negative Clamp Output Voltage	I_O = 1A, (Note 6)	−5		V
Overvoltage Shutdown Threshold		35	40	V (Max)
Overvoltage Shutdown Hysteresis		0.75		V
Error Output Leakage Current	$V_{Pin\ 13}$ = 12V	0.001	10	μA (Max)
Thermal Warning Temperature	$V_{Pin\ 13}$ < 0.8V	145		°C
Thermal Shutdown Temperature	$V_{Pin\ 17}$ < 0.8V	170		°C

Electrical Characteristics

V_{CC} = 12V, C_{CP} = 0.01 µF, unless otherwise indicated. **Boldface** limits apply over the entire operating temperature range, −40°C ≤ T_A ≤ +125°C, all other limits are for $T_A = T_J$ = +25°C. (Continued)

Parameter	Conditions	Typical (Note 4)	Limit (Note 5)	Units (Limit)
AC CHARACTERISTICS				
Switch Turn-On Delay ($t_{d(ON)}$)	Enable (Pin 3) = 5V, I_{OUT} = 1A	5	10	µs (Max)
Switch Turn-On Rise Time (t_{ON})	I_{OUT} = 1A	7	15	µs (Max)
Switch Turn-Off Delay (t_{dOFF})	Enable (Pin 3) = 5V, I_{OUT} = 1A	0.5	2	µs (Max)
Switch Turn-Off Fall Time (t_{OFF})	I_{OUT} = 1A	0.15	1	µs (Max)
Enable Time (t_{EN})	Measured with Switch 1, Pin 9 = 5V	30	50	µs (Max)
Error Reporting Delay (t_{Error})	Enable (Pin 3) = 5V, Switch 1 Load Opened	75	150	µs (Max)
Data Setup Time (t_{DS})	C_L = 30 pF	200	500	ns (Min)
TRI-STATE® Control (t_{1H}, t_{OH})	Pin 8, Hi-Z Enable Time	2		µs
Data Clock Frequency		3	1	MHz (Max)
DIGITAL CHARACTERISTICS				
Logic "1" Input Voltage	Pins 3, 4, 7, 9, 10, 11, 12		**2.0**	V (Min)
Logic "0" Input Voltage	Pins 3, 4, 7, 9, 10, 11, 12		**0.8**	V (Max)
Logic "1" Input Current	Pins 4, 7	0.001	**1**	µA (Max)
Logic "0" Input Current	Pins 4, 7	−0.001	**−1**	µA (Max)
TRI-STATE Output Current	Pin 8, Pin 4 = 5V Pin 8 = 0V	0.05 −0.05	10 −10	µA (Max) µA (Max)
Enable Input Current	Pin 3 = 2.4V	12	**25**	µA (Max)
Channel Input Resistance	Pins 9, 10, 11, 12	75	**25**	kΩ (Min)
Error Output Sink Current	Pin 13 = 0.8V	4	**1.6**	mA (Min)
Logic "1" Output Voltage	Pin 8 I_{OUT} = −360 µA I_{OUT} = −10 µA I_{OUT} = −10 µA	 4.4 5.1	 **2.4** **4.5** **5.5**	 V (Min) V (Min) V (Max)
Logic "0" Output Voltage	Pin 8 I_{OUT} = 100 µA		**0.4**	V (Max)
Thermal Shutdown Output Source Current	Pin 17 = 2.4V	5	3	µA (Min)
Thermal Shutdown Output Sink Current	Pin 17 = 0.8V	360	250	µA (Min)

Electrical Characteristics Notes

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics.

Note 2: Human body model; 100 pF discharge through a 1.5 kΩ resistor. All pins except pins 8 and 13 which are protected to 1000V and pins 1, 2, 18 and 19 which are protected to 500V.

Note 3: The maximum power dissipation is a function of $T_{J_{Max}}$, θ_{JA}, and T_A and is limited by thermal shutdown. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J_{Max}} - T_A)/\theta_{JA}$. If this dissipation is exceeded, the die temperature will rise above 150°C and the device will eventually go into thermal shutdown. For the LMD18400 the junction-to-ambient thermal resistance, θ_{JA}, is 60°C/W. With sufficient heatsinking the maximum continuous power dissipation for the package will be, $I_{DC_{Max}}^2 \times R_{ON(Max)} \times 4$ switches ($1A^2 \times 1.3\Omega \times 4 = 5.2W$).

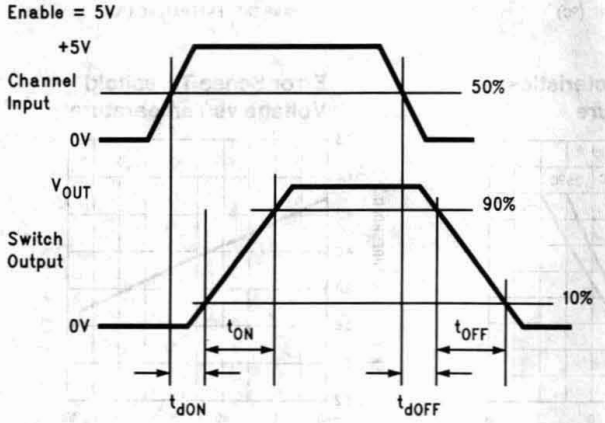
Note 4: Typical values are at $T_J = +25°C$ and represent the most likely parametric norm.

Note 5: All limits are 100% production tested at +25°C. Limits at temperature extremes are guaranteed through correlation and accepted Statistical Quality Control (SQC) methods.

Note 6: Pulse Testing techniques used. Pulse width is < 5 ms with a duty cycle < 1 %.

Timing Specification Definitions

Switching Turn ON/OFF



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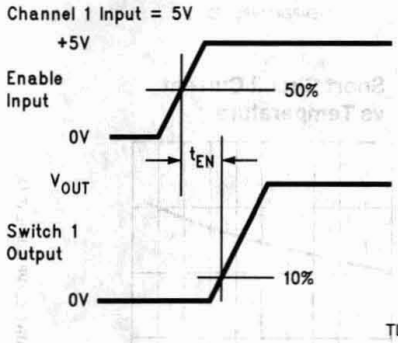
Enable Turn-ON



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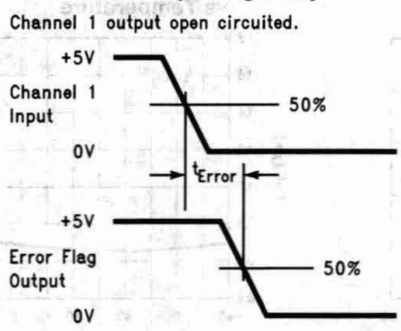
Error Reporting Delay



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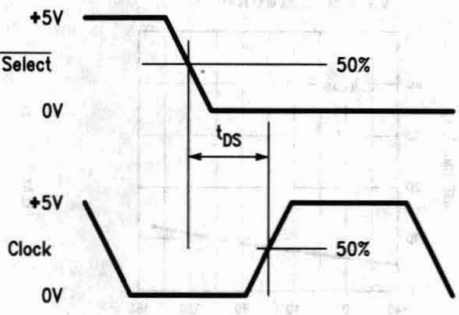
Data Setup Time



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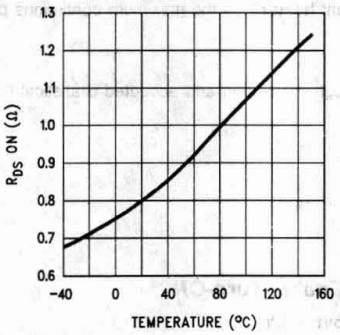
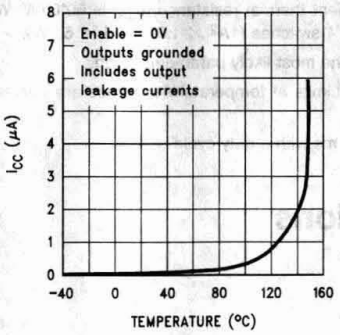
Typical Performance Characteristics

For all curves, V_{CC} = 12V, Temperature is the junction temperature unless otherwise noted.

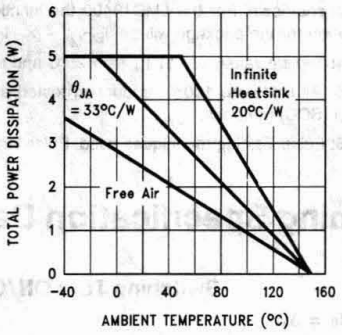
Switch ON Resistance vs Temperature



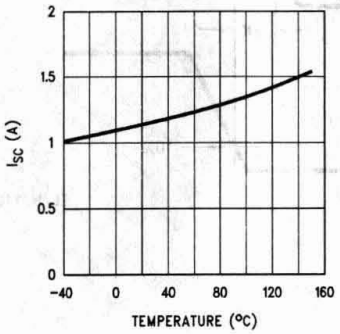
"Sleep" Mode Supply Current vs Temperature



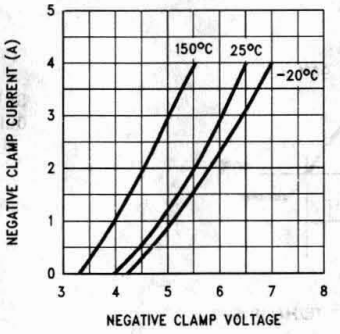
Maximum Power Dissipation vs Ambient Temperature



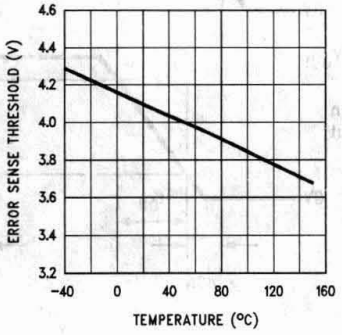
Short Circuit Current vs Temperature



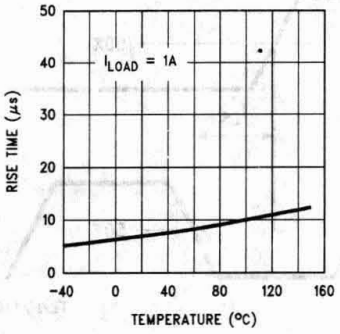
Clamp Characteristics vs Temperature



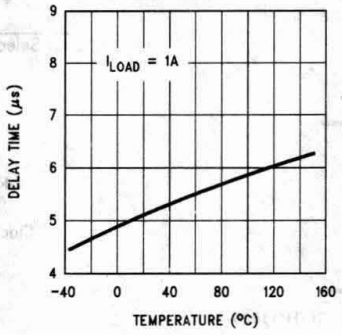
Error Sense Threshold Voltage vs Temperature



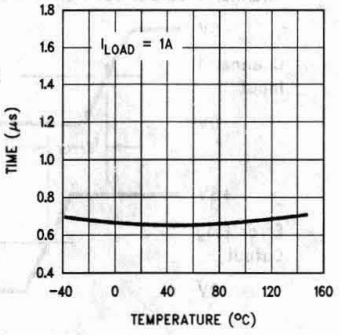
Turn ON Rise Time vs Temperature



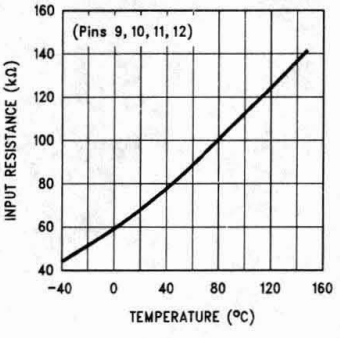
Turn ON Delay Time vs Temperature



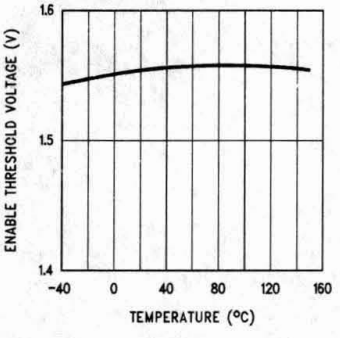
Turn OFF Time vs Temperature



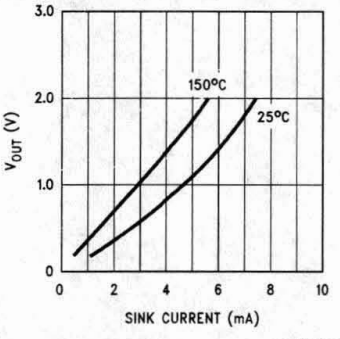
Switch Select Logic Input Resistance vs Temperature



Enable Threshold Voltage vs Temperature



Error Output Voltage vs Sink Current



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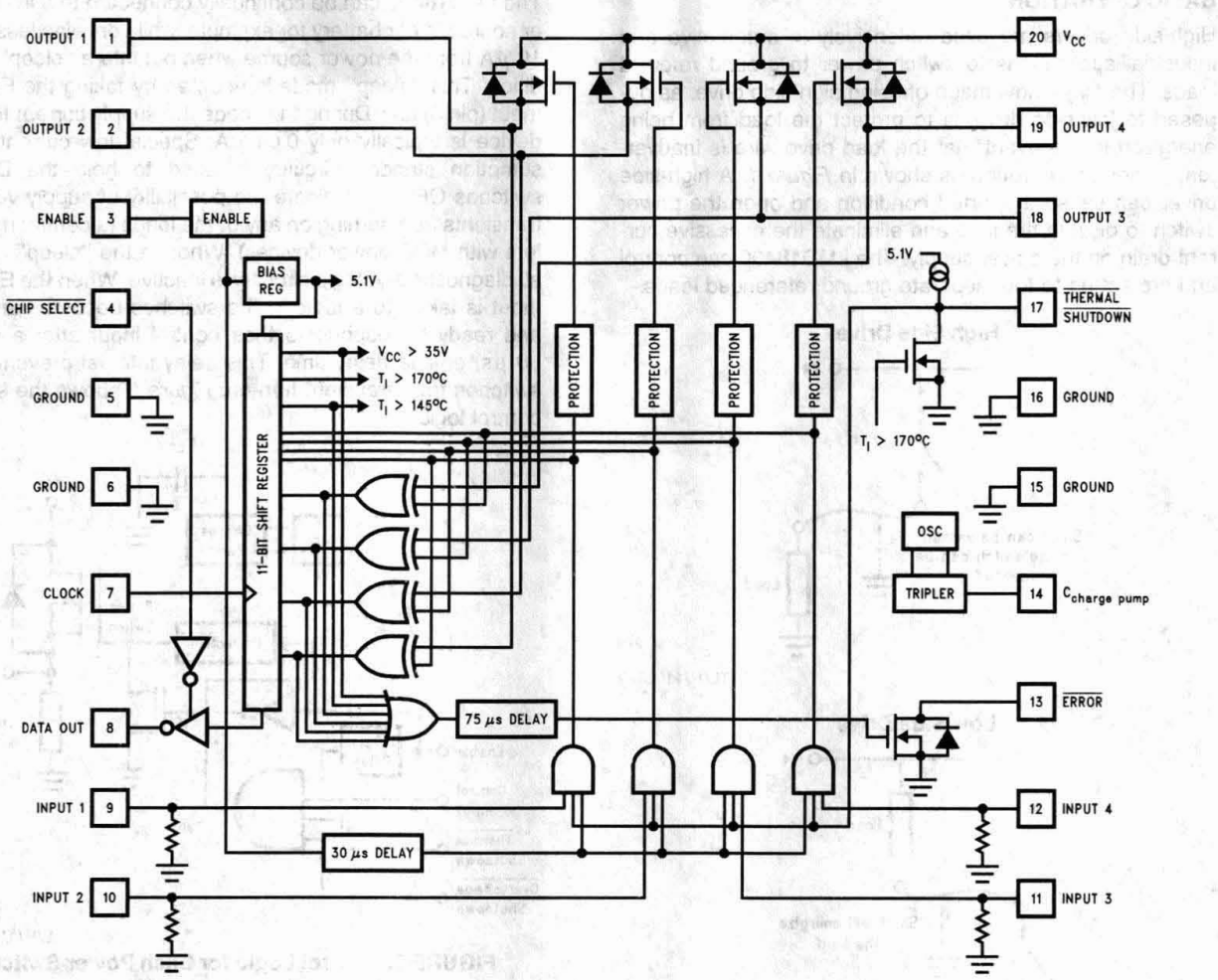
Functional Block Diagram



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Truth Table

Enable Input (Pin 3)	Chip Select Input (Pin 4)	Switch Control Input (Pins 8, 9, 10, 11)	Error Output (Pin 13)	Thermal SD Output (Pin 17)	Conditions
0	X	X	0	0	"Sleep" Mode, $I_{Supply} < 10\ \mu A$
1	X	0	1	1	Selected Switch is OFF
1	X	1	1	1	Selected Switch is ON, Normal Operation
1	X	0	0	1	Switch is OFF but: a. Load is Open Circuited, or b. Load is Shorted to V_{CC}, or c. $T_J > +145°C$, or d. $V_{CC} > +35V$
1	X	1	0	1	Switch is ON, but; a. Load is Shorted to Ground, or b. Switch is in Power Limit, or c. $T_J > +145°C$, or d. $V_{CC} > +35V$ and Switch is Actually OFF
1	X	1	0	0	$T_J > +170°C$, All Switches are OFF
1	1	X	X	X	Data Output Pin is TRI-STATE
1	0	X	X	X	Data Output Pin is Enabled and Ready to Output Diagnostic Information

3

Applications Information

BASIC OPERATION

High-side drivers are used extensively in automotive and industrial applications to switch power to ground referred loads. The major advantage of using high-side drive, as opposed to low-side drive, is to protect the load from being energized in the event that the load drive wire is inadvertently shorted to ground as shown in *Figure 1*. A high-side driver can sense a shorted condition and open the power switch to disable the load and eliminate the excessive current drain on the power supply. The LMD18400 can control and protect up to four separate ground referenced loads.

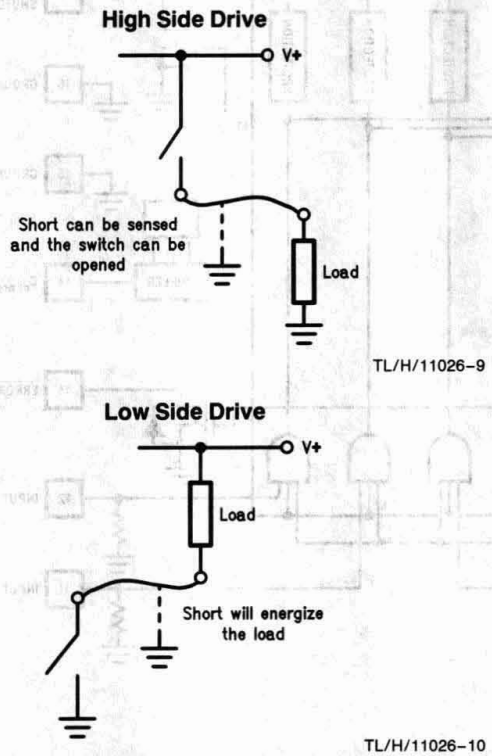


FIGURE 1. High-Side vs Low-Side Drive

The LMD18400 combines low voltage CMOS logic control circuitry with a high voltage DMOS process. Each DMOS power switch has an individual ON/OFF control input. When commanded ON, the output of the switch will connect the load to the V_{CC} supply through a maximum resistance of 1.3Ω (the ON resistance of the DMOS switch). The voltage applied to the load will depend upon the load current and the designed current capability of the LMD18400. When a switch is commanded OFF, the load will be disconnected from the supply except for a small leakage current of typically less than 0.01 μA.

The LMD18400 can be continually connected to a live power source, a car battery for example, while drawing less than 10 μA from the power source when put into a "sleep" condition. This "sleep" mode is enacted by taking the Enable Input (pin 3) low. During this mode the supply current for the device is typically only 0.04 μA. Special low current consumption standby circuitry is used to hold the DMOS switches OFF to eliminate the possibility of supply voltage transients from turning on any of the loads (a common problem with MOS power devices). When in the "sleep" mode, all diagnostic and logic circuitry is inactive. When the Enable Input is taken to a logic 1, the switches become "armed" and ready to respond to their control input after a short, 30 μs, enable delay time. This delay interval prevents the switches from transient turn-on. *Figure 2* shows the switch control logic.

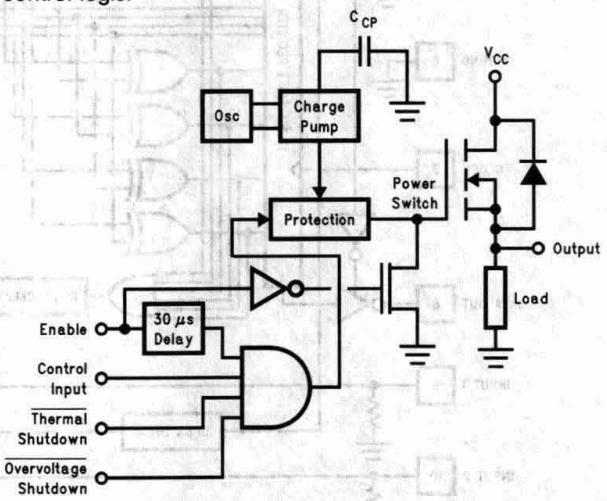


FIGURE 2. Control Logic for Each Power Switch

Each DMOS switch is turned ON when its gate is driven approximately 3.5V more positive than its source voltage. Because the source of the switch is the output terminal to the load it can be taken to a voltage very near the V_{CC} supply potential. To ensure that there is sufficient voltage available to drive the gates of the DMOS device a charge pump circuit is built in. This circuit is controlled by an internal 300 kHz oscillator and using an external 10 nF capacitor connected from pin 14 to ground generates a voltage that is approximately 20V greater than the V_{CC} supply voltage. This provides sufficient gate voltage drive for each of the switches which is applied under command of standard 5V logic input levels.

The turn-on time for each switch is approximately 12 μs when driving a 1A load current. This relatively slow switching time is beneficial in minimizing electromagnetic interference (EMI) related problems created from switching high current levels.

Applications Information (Continued)

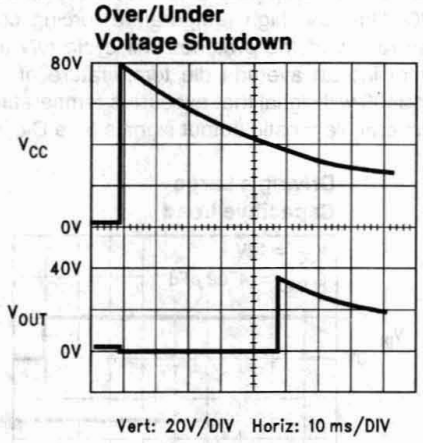
PROTECTION CIRCUITRY

The LMD18400 has extensive protection circuitry built in. With any power device, protection against excessive voltage, current and temperature conditions is essential. To achieve a "fail-safe" system implementation, the loads are deactivated automatically by the LMD18400 in the event of any detected overvoltage or over-temperature fault conditions.

Voltage Protection

The V_{CC} supply can range from $-0.5V$ to $+60$ V_{DC} without any damage to the LMD18400. The CMOS logic circuitry is biased from an internal 5.1V regulator which protects these lower voltage transistors from the higher V_{CC} potentials. In order to protect the loads connected to the switch outputs however, an overvoltage shutdown circuit is employed. Should the V_{CC} potential exceed 35V all of the switches are turned OFF thereby disconnecting the loads. This 35V threshold has 750 mV of hysteresis to prevent potential oscillations.

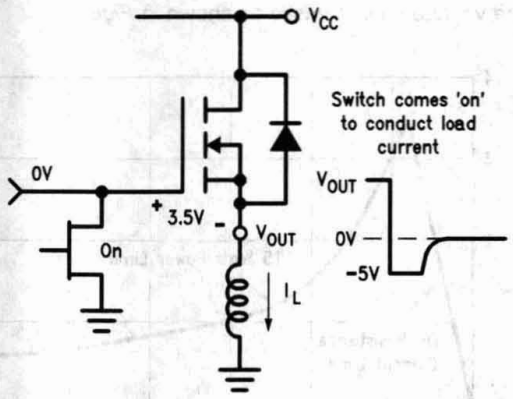
Additionally, there is an undervoltage lockout feature built in. With V_{CC} less than 5V it becomes uncertain whether the logic circuitry can hold the switches in their commanded state. To avoid this uncertainty, all of the switches are turned OFF when V_{CC} drops below approximately 5V. *Figure 3* illustrates the shutoff of an output during a 0V to 80V V_{CC} supply transient.



TL/H/11026–12

FIGURE 3. Overvoltage/Undervoltage Shutdown

The LMD18400 has been designed to drive all types of loads. When driving a ground referenced inductive load such as a relay or solenoid, the voltage across the load will reverse in polarity as the field in the inductor collapses when the power switch is turned OFF. This will pull the output pin of the LMD18400 below ground. This negative transient voltage is clamped at approximately $-5V$ to protect the IC. This clamping action is not done with diodes but rather the power DMOS switch turning back on momentarily to conduct the inductor current as it de-energizes as shown in *Figure 4*.



TL/H/11026–13

FIGURE 4. Turn-OFF Conditions with an Inductive Load

When the output inductance produces a negative voltage, the gate of the DMOS transistor is clamped at 0V. At $-3.5V$, the source of the power device is less than the gate by enough to cause the switch to turn ON again. During this negative transient condition the power limiting circuitry to protect the switch is disabled due to the gate being held at 0V. The maximum current during this clamping interval, which is equal to the steady state ON current through the inductor, should be kept less than 1A. Another concern during this interval has to do with the size of an inductive load and the amount of time required to de-energize it. With larger inductors it may be possible for the additional power dissipation to cause the die temperaure to exceed the thermal shutdown limit. If this occurs all of the other switches will turn OFF momentarily (see section on Thermal Management).

Power Limiting

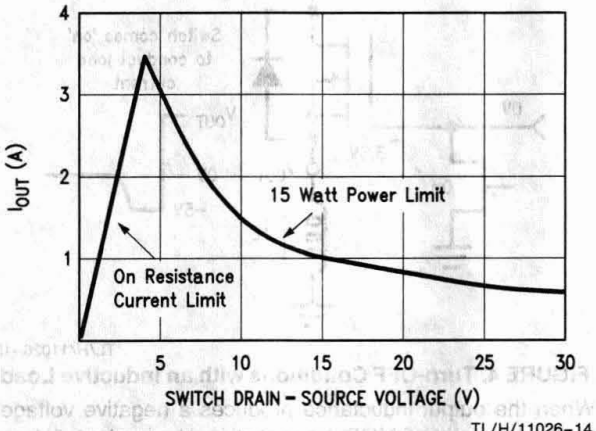
The LMD18400 utilizes a true instantaneous power limit circuit rather than simple current limiting to protect each switch. This provides a higher transient current capability while still maintaining a safe power dissipation level. The power dissipation in each switch (the product of the Drain-to Source voltage and the output current, $V_{ds} \times I_{OUT}$) is con-

Applications Information (Continued)

tinually monitored and limited to 15W by varying the gate voltage and therefore the ON resistance of the switch. Basically the ON resistance will be as low as possible until 15W is being dissipated. To maintain 15W, the ON resistance increases to reduce the load current. This results in a decrease of the output voltage. For resistive loads, the output voltage when in power limit will be:

$$V_{OUT}\ (\text{in Power Limit}) = \frac{V_{CC} - \sqrt{V_{CC}^2 - 60\,R_L}}{2}$$

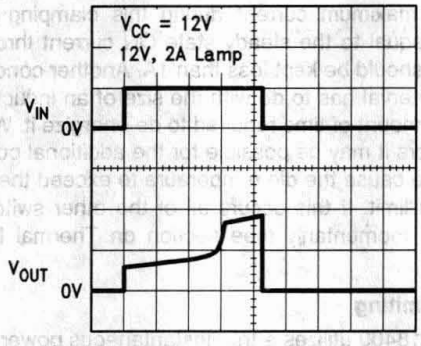
This provides a maximum transient current and drain-to-source voltage characteristic as shown in *Figure 5*.



TL/H/11026–14

FIGURE 5. Maximum Output Current with Instantaneous Power Limiting

Driving a Lamp



TL/H/11026–15

FIGURE 6. Soft Turn-On of a Lamp Load

The steady state current to the load is limited by the package power dissipation, ambient temperature and the ON resistance of the switch which has a positive temperature coefficient as shown in the Typical Performance Characteristics.

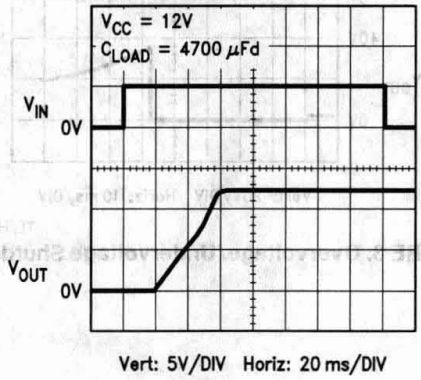
This dynamic current limiting of the switches is beneficial when driving lamp and large capacitive loads. Lamps require a large inrush current, on the order of 10 times the normal operating current, when first switched on with a cold filament. The LMD18400 will limit this initial current to the level where 15W is dissipated in the switch. As the filament warms up the voltage across the lamp increases thereby decreasing the voltage across the switch which permits more current to fully light the lamp. With limited inrush current the lifetime of a lamp load is increased significantly. *Figure 6* illustrates the soft turn-on of a lamp load.

The same principle of increasing output current as the voltage across the load increases allows large capacitive loads to be charged more quickly by an LMD18400 driver than as opposed to a driver with a fixed 1A current limit protection scheme. *Figure 7* shows the output response while driving a large capacitive load.

Thermal Protection

The die temperature of the LMD18400 is continually monitored. Should any conditions cause the die temperature to rise to +170°C, all of the power switches are turned OFF automatically to reduce the power dissipation. It is important to realize that the thermal shutdown affects all four of the switches together. That is, if just one switch load is enough to heat the die to the thermal shutdown threshold, all of the other switches, regardless of their power dissipation conditions, will be switched OFF. All of the switches will be re-enabled when the die temperature has cooled to approximately +160°C. Until the high temperature forcing conditions have been removed the switches will cycle ON and OFF thus maintaining an average die temperature of +165°C. The LMD18400 will signal that excessive temperatures exist through several diagnostic output signals (see Diagnostics).

Driving a Large Capacitive Load



TL/H/11026–16

FIGURE 7. Driving a Large Capacitive Load

Applications Information (Continued)

DIAGNOSTICS

The LMD18400 has extensive circuit diagnostic information reporting capability. Use of this information can produce systems with intelligent feedback of switch status as well as load fault conditions for troubelshooting purposes. All of the diagnostic information is contained in an 11-bit word. This data can be clocked out of the LMD18400 in a serial fashion as shown in *Figure 8*. The shift register is parallel loaded with the diagnostic data whenever the Chip Select Input is at a Logic 1 and changes to the serial shift mode when Chip Select is taken to a Logic 0. The Data Output line (pin 8) is biased internally from a 5.1V regulator which sets the Logic 1 output voltage. This pin has low current sourcing capability so any load on this pin will reduce the Logic 1 output level which is guaranteed to be at least 2.4V with a 360 μA load.

The data interface is MICROWIRE compatible in that data is clocked out of the LMD18400 on the falling edge of the clock, to be clocked into the controlling microprocessor on the rising edge. Any number of devices can share a common data output line because the data output pin is held in a high impedance (TRI-STATE) condition until the device is selected by taking its Chip Select Input low. Following Chip Select going low there is a short data setup time interval (500 ns Min) required. This is necessary to allow the first data bit of information to be established on the data output line prior to the first rising clock edge which will input the data bit into the controller. When all 11 bits of diagnostic data have been shifted out the data output goes to a Logic 1 level until the Chip Select line is returned high.

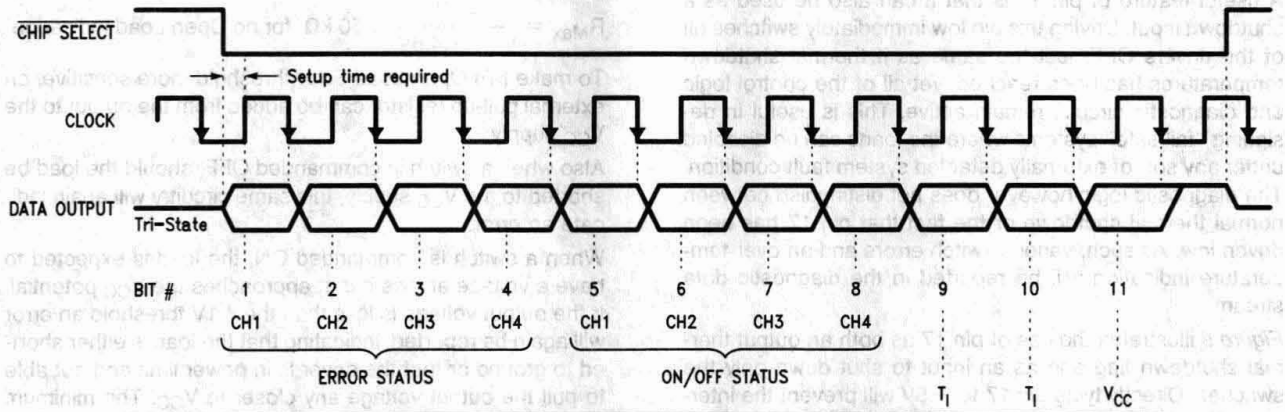
Figure 8 also indicates the significance of the diagnostic data bits. The first 4 bits indicate an output load error condition, one for each channel in succession (see Load Error Detection).

Bits 5 through 8 provide a readback of the commanded ON/OFF status of each switch.

A unique feature of the LMD18400 is that it provides an early warning of excessive operating temperature. Should the die temperature exceed +145°C, bit 9 will be set to a Logic 0. Acting on this information a system can be programmed to take corrective action, shutting OFF specific loads perhaps, while the LMD18400 is still operating normally (not yet in thermal shutdown). If this early warning is ignored and the device continues to rise in temperature, the thermal shutdown circuitry will come into action at a die temperature of +170°C. Should this occur bit 10 of the diagnostic data stream will be set to a Logic 0 indicating that the device is in thermal shutdown and all of the outputs have been shut OFF.

The final data bit, bit 11, indicates an overvoltage condition on the V_{CC} supply (V_{CC} is greater than 35V) and again indicates that all of the drivers are OFF.

The diagnostic data can be read periodically by a controller or only in the event of a general system error indication to determine the cause of any system problem. This general indication of a fault is provided by an Error Flag output (pin 13). This pin goes low whenever any type of error is detected. There is a built-in delay of approximately 75 μs from the time an error is detected until pin 13 is taken low. This is to help mask short duration error conditions such as may be caused by driving highly capacitive loads (>2 μF). A lamp load may generate a shorted load error for several hundred milliseconds as it turns on which should be ignored.



LOGIC 1	LOAD OK	SWITCH OFF	<145°C	<170°C	<35V
LOGIC 0	LOAD ERROR	SWITCH ON	>145°C	>170°C	>35V

TL/H/11026–17

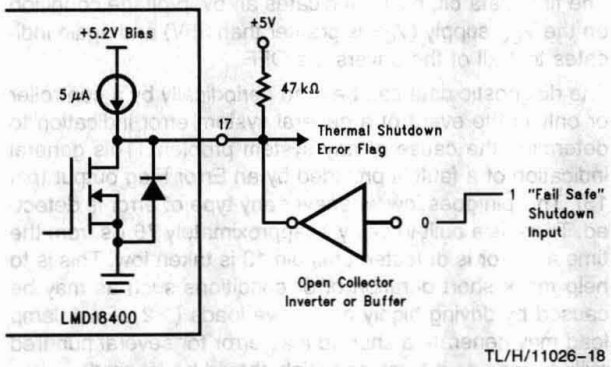
FIGURE 8. Serial Diagnostic Data Assignments

3

Applications Information (Continued)

The Error Flag output pin is an open drain transistor which requires a pull-up resistor to a positive voltage of up to 16V. Typically this pull-up is to the same 5V supply which is biasing the Enable input and any other external logic circuitry. The Error Flag pins of several LMD18400 packages can be connected together with just one pull-up resistor to provide an all-encompassing general system error indication. Upon detection of an error, each device could then be polled for diagnostic information to determine the source of the fault condition.

A second direct output error flag is for an indication of Thermal Shutdown (pin 17). This active low flag provides an immediate indication that the die temperature has reached +170°C and that the drive to all four switches has been removed. This output is pulled up to the internal 5.1V logic regulator through a small (5 μA) current source so use of a buffer on this pin is recommended.



TL/H/11026–18

FIGURE 9. Thermal Shutdown Flag and Shutdown Input

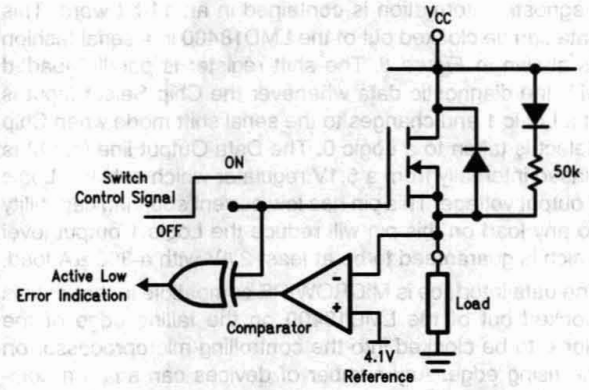
A useful feature of pin 17 is that it can also be used as a shutdown input. Driving this pin low immediately switches all of the drivers OFF, just the same as if thermal shutdown temperatures has been reached, yet all of the control logic and diagnostic circuits remain active. This is useful in designing "fail-safe" systems where the loads can be disabled under any sort of externally detected system fault condition. The diagnostic logic however does not distinguish between normal thermal shutdown or the fact that pin 17 has been driven low. As such, various switch errors and an over-temperature indication will be reported in the diagnostic data stream.

Figure 9 illustrates the use of pin 17 as both an output thermal shutdown flag and as an input to shut down only the switches. Directly tying pin 17 to +5V will prevent the internal thermal shutdown circuitry from disabling the switches. For reliability purposes however this is not recommended as there will then be no limit to the maximum die temperature.

Refer to the Truth Table for a summary of the action of these direct-output error flags.

LOAD ERROR DETECTION

An important feature of the LMD18400 is the ability to detect open or shorted load connections. *Figure 10* illustrates the detection circuit used with each of the drivers.



TL/H/11026–19

FIGURE 10. Detection Circuitry for Open/Shorted Loads

A voltage comparator monitors the voltage to the load and compares it to a fixed 4.1V reference level. When a switch is OFF, the ground referenced load should have no voltage across it. Under this condition, an internal 50 kΩ resistor connected to V_{CC} will provide a small amount of current to the load. If the load resistance is large enough to create a voltage greater than 4.1V an Open Load Error will be indicated for that switch. The maximum load resistance that will not generate an Open Load Error when a switch is OFF can be found by:

$$R_{Max} = \frac{4.1V}{V_{CC} - 4.6V} \times 50\ k\Omega;\ \text{for no Open Load Indication}$$

To make this Open Load Error threshold more sensitive, an external pull-up resistor can be added from the output to the V_{CC} supply.

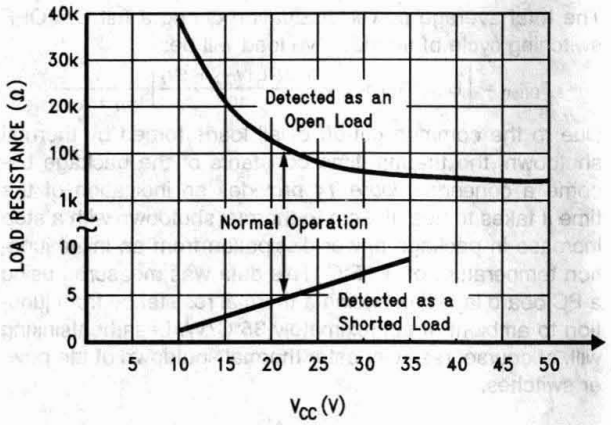
Also when a switch is commanded OFF, should the load be shorted to the V_{CC} supply, this same circuitry will again indicate an error.

When a switch is commanded ON, the load is expected to have a voltage across it that approaches the V_{CC} potential. If the output voltage is less than the 4.1V threshold an error will again be reported, indicating that the load is either shorted to ground or that the driver is in power limit and not able to pull the output voltage any closer to V_{CC}. The minimum load resistance that will not generate a Shorted Load Error when a switch is ON can be found by:

$$R_{Min} = \frac{4.1V\ (V_{CC} - 4.1V)}{15W};\ \text{for no Shorted Load Error}$$

Applications Information (Continued)

Figure 11 indicates the range of load resistance for normal operation, open load, and shorted load or power limit indication.



TL/H/11026–20

FIGURE 11. Load Resistance Detected as Errors

THERMAL MANAGEMENT

It is particularly important to consider the total amount of power being dissipated by all four switches in the LMD18400 at all times. Any combination of the switches driving loads will cause an increase in the die temperature. Should the die temperature reach the thermal shutdown threshold of +170°C, all of the switches will be disabled. Careful calculation of the worst case total power dissipation required at any point in time, together with providing sufficient heatsinking will prevent this from occurring.

The LMD18400 is packaged with a special leadframe that helps dissipate heat through the two ground pins on each side of the package. The thermal resistance from junction-to-case (θ_{JC}) for this package is approximately 20°C/W. The thermal resistance from junction-to-ambient (θ_{JA}), without any heatsinking, is approximately 60°C/W. *Figure 12* illustrates how the copper foil of a printed circuit board can be designed to provide heatsinking and reduce the overall junction-to-ambient thermal resistance.

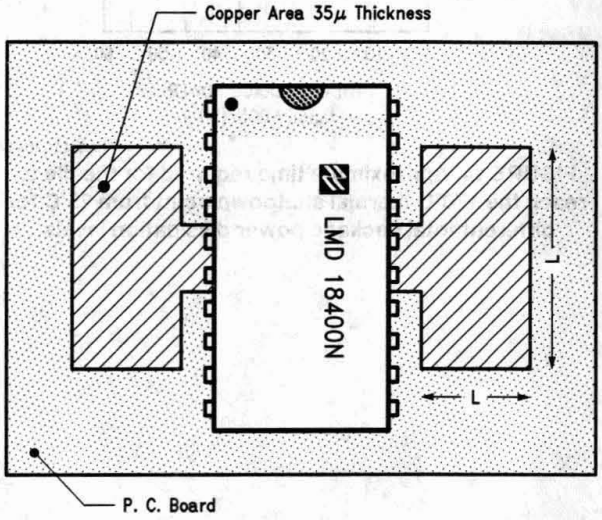
The power dissipation in each switch is equal to:

$$P_{D\ (Each\ Switch)} = I_{Load}^2 \times R_{ON} \quad or \quad \frac{(V_{CC} - V_{OUT})^2}{R_{ON}}$$

where R_{ON} is the ON resistance of the switch (1.3Ω maximum). These equations hold true until the power dissipation reaches the maximum limit of 15W. With resistive loads, the 15W power limit threshold will be reached when:

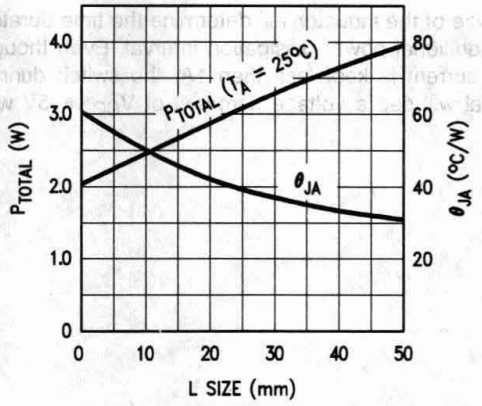
$$R_L \leq \frac{V_{CC}^2}{60W}$$

Inductive loads will create additional power dissipation when switched OFF. *Figure 13* shows the idealized voltage and current waveforms for an inductive load.



TL/H/11026–21

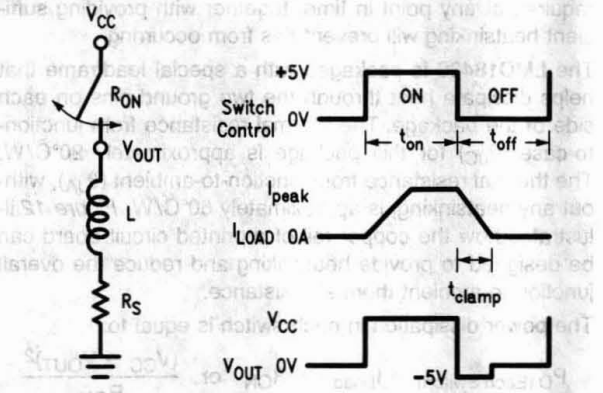
Maximum Power Dissipated and Junction to Ambient Thermal Resistance vs Size



TL/H/11026–22

FIGURE 12. Recommended PC Board Layout to Reduce the Thermal Resistance from Junction-to-Ambient

Applications Information (Continued)



TL/H/11026–23

FIGURE 13. Switching an Inductive Load

When switched ON, the worst case power dissipation is:

$$P_{D(ON)} = I_{Peak}^2 \times R_{ON}; \text{ where } I_{Peak} = \frac{V_{CC}}{R_{ON} + R_S}$$

The steady-state ON current of the inductor should be kept less than 1A per power switch.

The additional power dissipation during turn-off, as the inductor is de-energized and the voltage across the inductor is clamped to −5V, can be found by:

$$P_{D(OFF)} = \frac{(V_{CC} + 5V) \times I_{Peak}}{2}$$

for the time interval, t_{Clamp}, which is the time required for the inductor current to fall to zero;

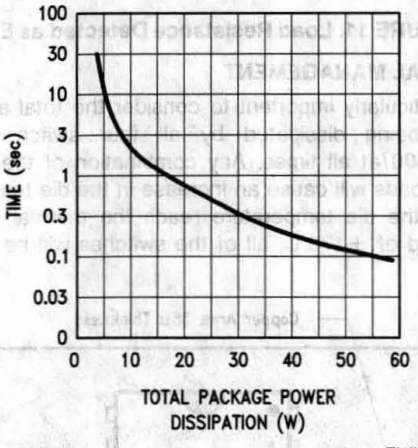
$$t_{Clamp} = \frac{I_{Peak} \times L}{5V}$$

The size of the inductor will determine the time duration for this additional power dissipation interval. Even though the peak current is kept less than 1A, the switch during this interval will see a voltage across it of V_{CC} + 5V with no power limit protection. If the inductor is too large, the time interval may be long enough to heat the die temperature to +170°C thereby shutting OFF all other loads on the package.

The total average power dissipation during a full ON/OFF switching cycle of an inductive load will be:

$$P_{D(tot)} = \left[I_{Peak}^2 R_{ON} t_{ON} + \frac{I_{Peak}^2 L (V_{CC} + 5V)}{10} \right] \frac{1}{t_{ON} + t_{OFF}}$$

Due to the common cut-off of all loads forced by thermal shutdown, the thermal time constants of the package become a concern. *Figure 14* provides an indication of the time it takes to heat the die to thermal shutdown with a step increase in package power dissipation from an initial junction temperature of +25°C. This data was measured using a PC board layout providing a thermal resistance from junction to ambient of approximately 35°C/W. Less heatsinking will, of course, result in faster thermal shutdown of the power switches.

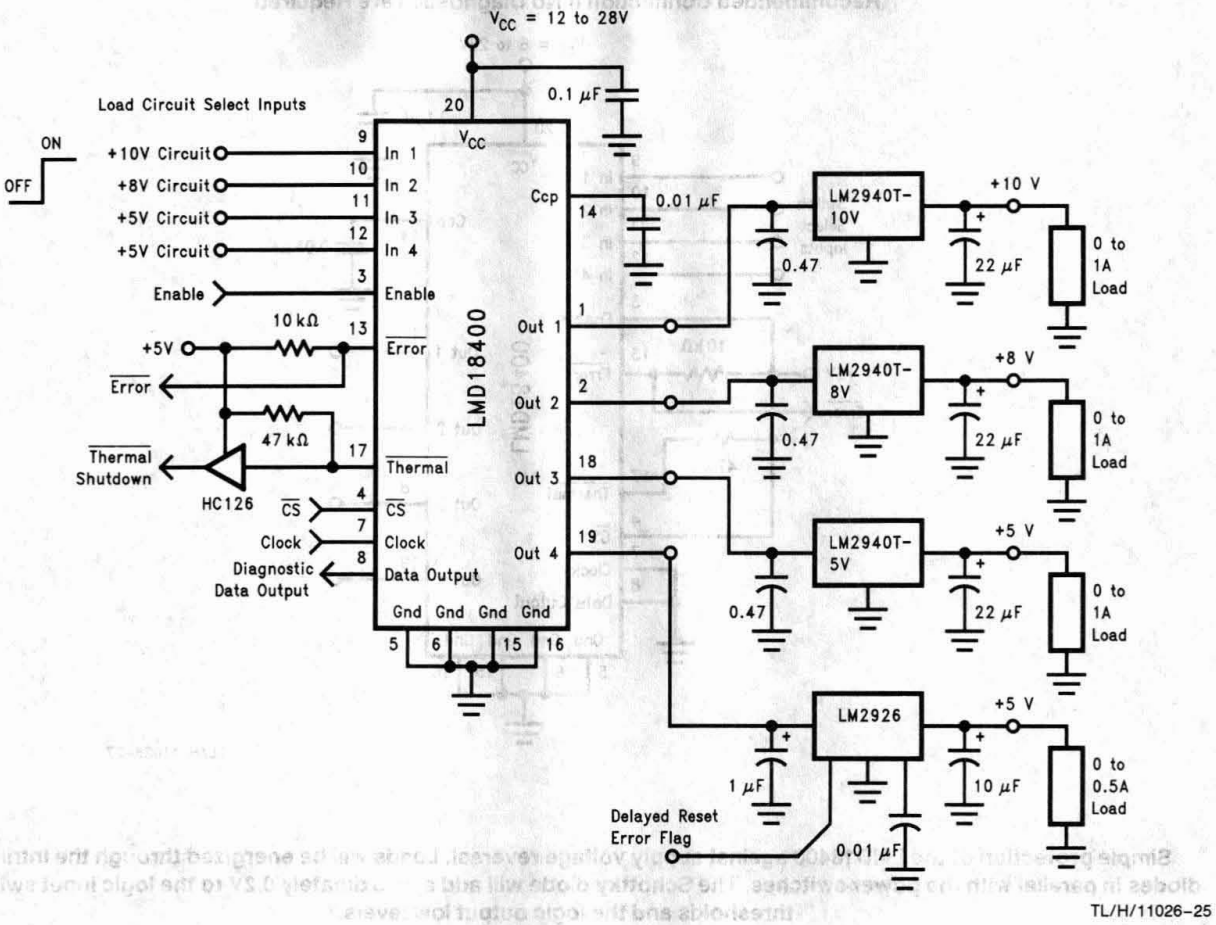


TL/H/11026–24

FIGURE 14. Approximate time required for the die to reach the 170°C thermal shutdown point from 25°C for different total package power dissipation levels.

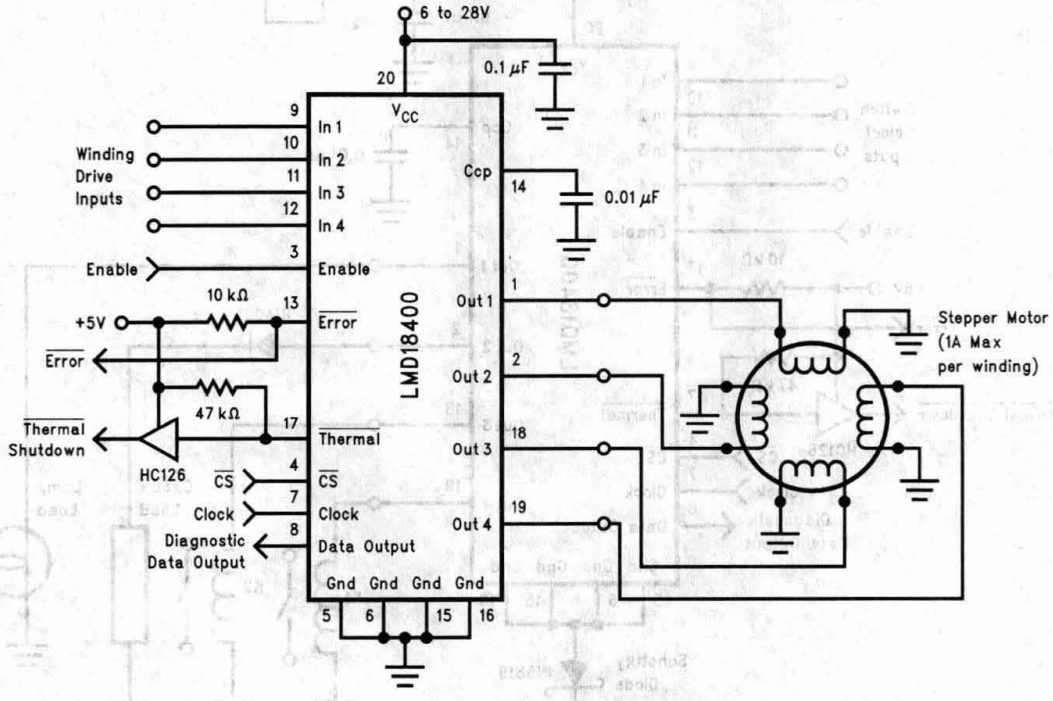
Applications

ON/OFF Switching of multiple voltage regulated circuit loads.



TL/H/11026–25

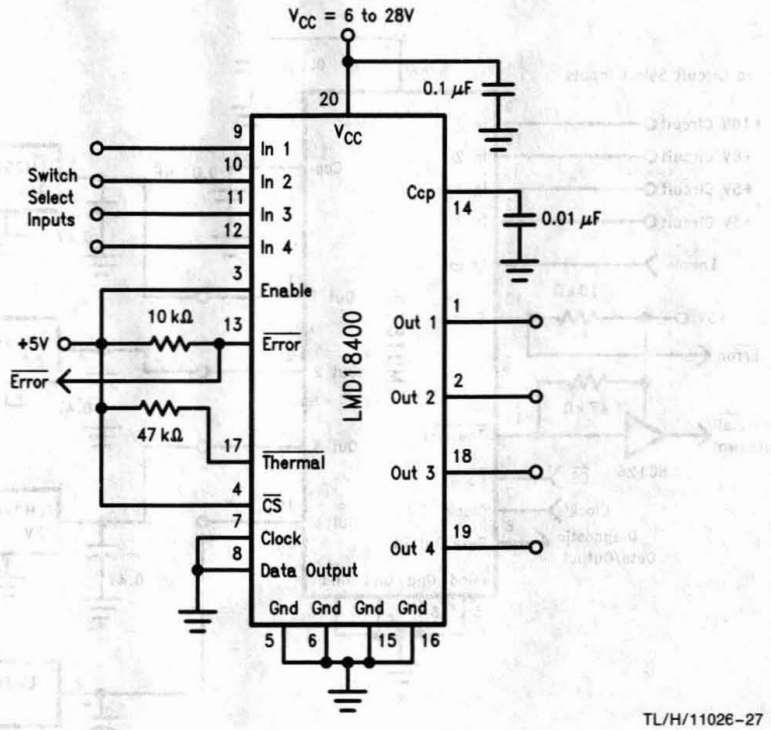
Unipolar Drive for a 4-Phase Stepper Motor



TL/H/11026–26

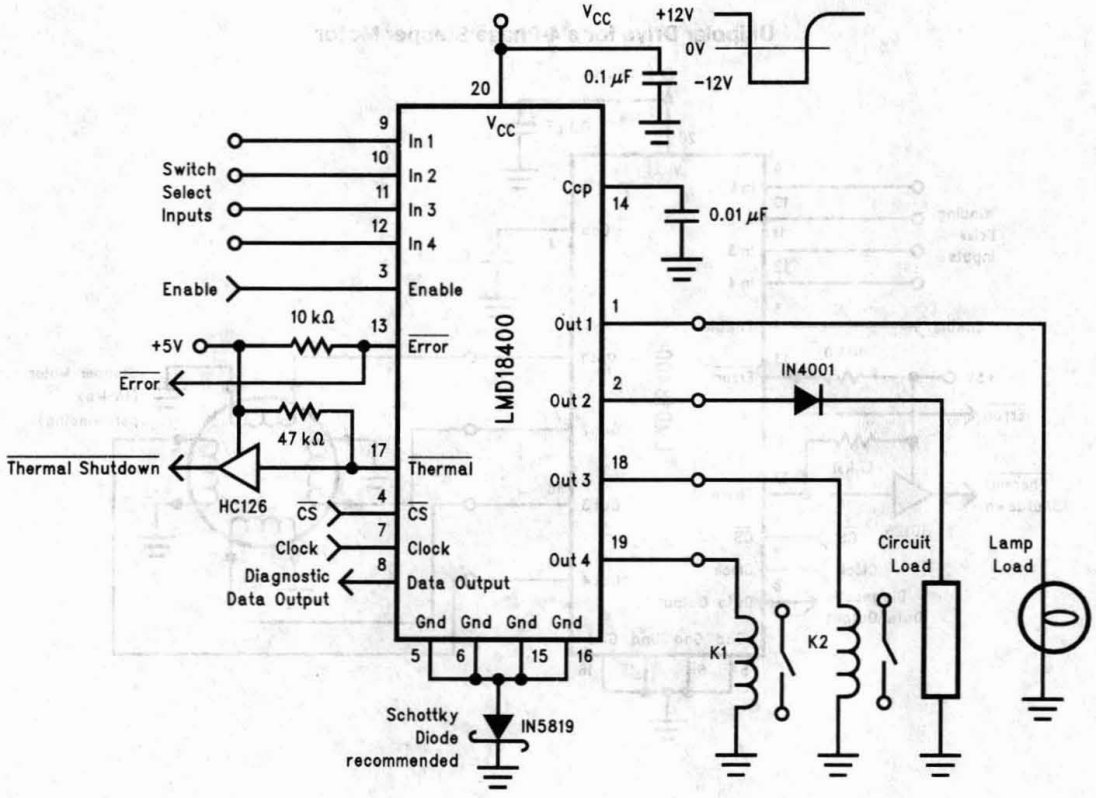
Applications (Continued)

Recommended Connection if No Diagnostics are Required



TL/H/11026–27

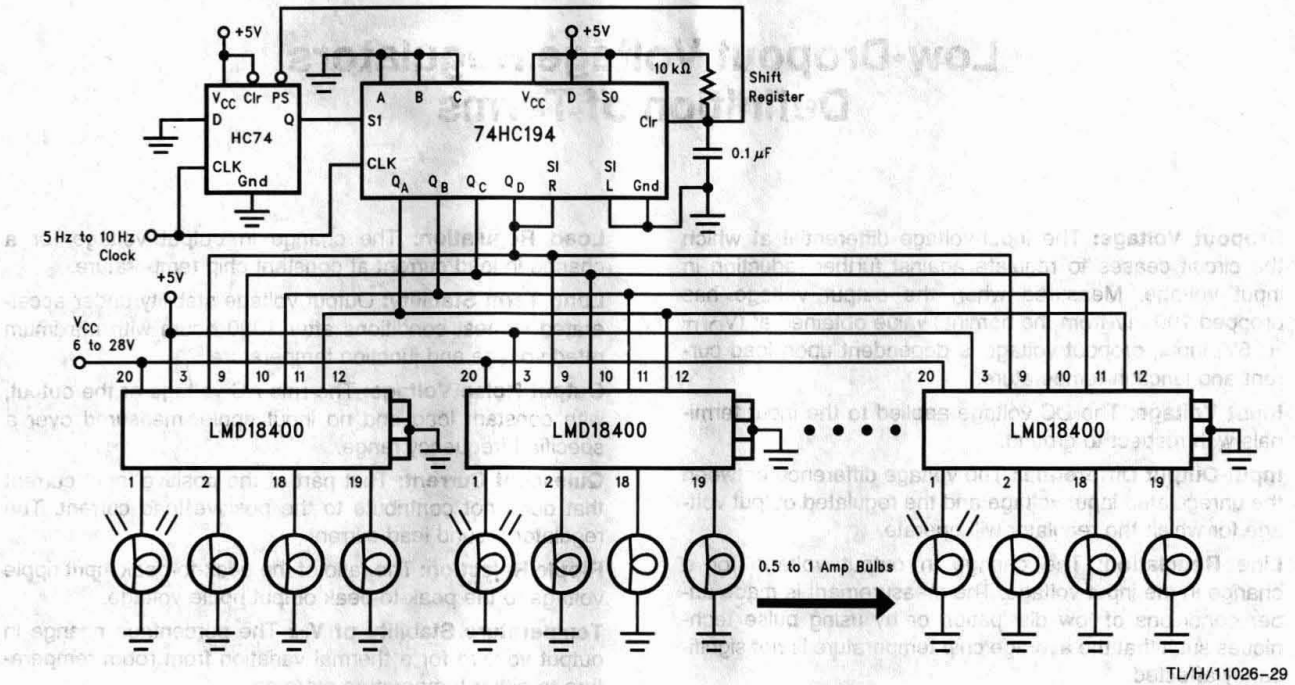
Simple protection of the LMD18400 against supply voltage reversal. Loads will be energized through the intrinsic diodes in parallel with the power switches. The Schottky diode will add approximately 0.2V to the logic input switching thresholds and the logic output low levels.



TL/H/11026–28

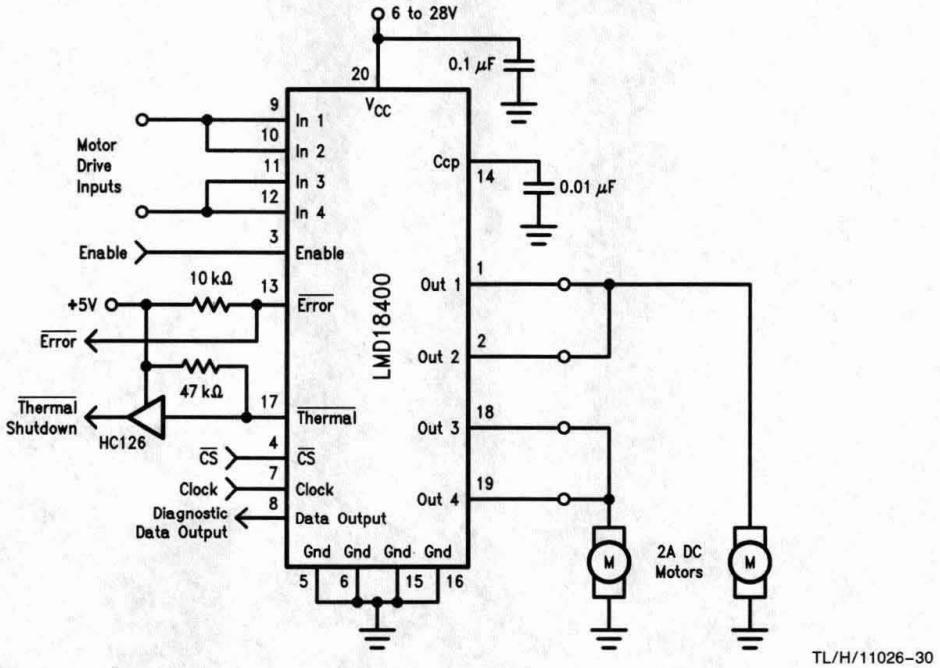
Applications (Continued)

Simple Light "Chaser"



TL/H/11026–29

Parallelling switches for higher current capability. Positive temperature coefficient of the switch ON resistance provides ballasting to evenly share the load current between the switches. Any combination of switches can be paralleled. Required peak load current will depend upon the motor load. Motor speed control can be provided by a PWM signal of up to 20 kHz applied to the motor drive input lines.



TL/H/11026–30

National Semiconductor

Low-Dropout Voltage Regulators Definition of Terms

Dropout Voltage: The input-voltage differential at which the circuit ceases to regulate against further reduction in input voltage. Measured when the output voltage has dropped 100 mV from the nominal value obtained at (V_{OUT} + 5V) input, dropout voltage is dependent upon load current and junction temperature.

Input Voltage: The DC voltage applied to the input terminals with respect to ground.

Input-Output Differential: The voltage difference between the unregulated input voltage and the regulated output voltage for which the regulator will operate.

Line Regulation: The change in output voltage for a change in the input voltage. The measurement is made under conditions of low dissipation or by using pulse techniques such that the average chip temperature is not significantly affected.

Load Regulation: The change in output voltage for a change in load current at constant chip temperature.

Long Term Stability: Output voltage stability under accelerated life-test conditions after 1000 hours with maximum rated voltage and junction temperature.

Output Noise Voltage: The rms AC voltage at the output, with constant load and no input ripple, measured over a specified frequency range.

Quiescent Current: That part of the positive input current that does not contribute to the positive load current. The regulator ground lead current.

Ripple Rejection: The ratio of the peak-to-peak input ripple voltage to the peak-to-peak output ripple voltage.

Temperature Stability of V_O: The percentage change in output voltage for a thermal variation from room temperature to either temperature extreme.

National Semiconductor

Low Dropout Regulators Selection Guide

Output Current (A)	Device	Output Voltage (V)	Typical Dropout Voltage (V)*	Maximum Input Voltage (V)	Typical Quiescent Current (mA)	Reverse Polarity Protection (V)	Transient Protection (V)	Operating Temperature (Tj °C)	Page No.
1.0	LM2940	5, 8, 12, 15	0.50	26	10	−15	+60**/−50	−55 to +150	3-154
	LM2940C	5, 9, 12, 15	0.50	26	10	−15	+45/−45	0 to +150	3-154
0.75	LM2925	5	0.82	26	3	−15	+60**/−50	−40 to +150	3-114
	LM2935	Two 5V Outputs	0.82	26	3	−15	+60**/−50	−40 to +150	3-136
0.5	LM2926	5	0.35	26	2	−18	+80**/−50	−40 to +125	3-120
	LM2927	5	0.35	26	2	−18	+80**/−50	−40 to +125	3-120
	LM2937	5, 8, 10, 12, 15	0.50	26	2	−15	+60**/−50	−40 to +125	3-149
	LM2984	Three 5V Outputs	0.53	26	14	−15	+60**/−35	−40 to +150	3-179
0.1	LM2931	5	0.30	24	0.400	−15	+60**/−50	−40 to +125	3-128
	LM2931C	Adj. (3 to 29)	0.30	24	0.400	−15	+60**/−50	−40 to +125	3-128
	LP2950C	5	0.38	30	0.075			−40 to +125	3-164
	LP2950AC	5	0.38	30	0.075			−40 to +125	3-164
	LP2951	5, Adj. (1.24V to 29)	0.38	30	0.075			−55 to +150	3-164
	LP2951C	3.0, 3.3, 5, Adj. (1.24V to 29)	0.38	30	0.075			−40 to +125	3-164
	LP2951AC	3.0, 3.3, 5, Adj. (1.24V to 29)	0.38	30	0.075			−40 to +125	3-164
0.05	LM2936	5	0.4	40	0.009	−15	+60/−50	−40 to +125	3-144

*Guaranteed maximum dropout voltage at full load over temperature.

**Positive transient protection value also indicates the regulator's load dump capability.

National Semiconductor

LM1577/LM2577 Series
SIMPLE SWITCHER® Step-Up Voltage Regulator

General Description

The LM1577/LM2577 are monolithic integrated circuits that provide all of the power and control functions for step-up (boost), flyback, and forward converter switching regulators. The device is available in three different output voltage versions: 12V, 15V, and adjustable.

Requiring a minimum number of external components, these regulators are cost effective, and simple to use. Listed in this data sheet are a family of standard inductors and flyback transformers designed to work with these switching regulators.

Included on the chip is a 3.0A NPN switch and its associated protection circuitry, consisting of current and thermal limiting, and undervoltage lockout. Other features include a 52 kHz fixed-frequency oscillator that requires no external components, a soft start mode to reduce in-rush current during start-up, and current mode control for improved rejection of input voltage and output load transients.

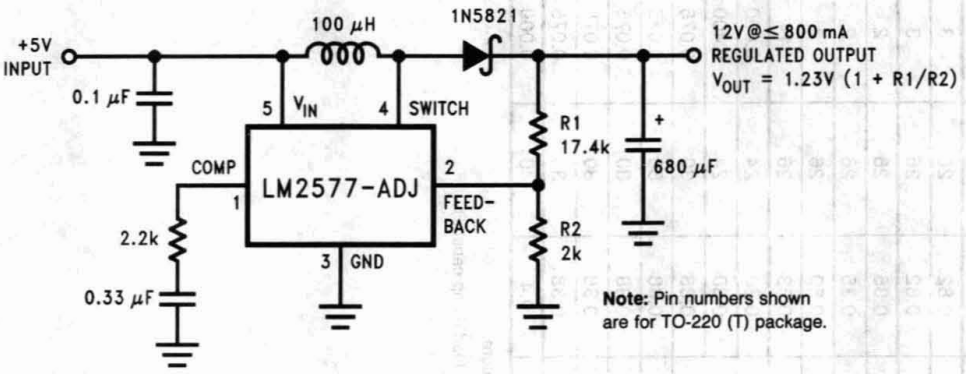
Features

- Requires few external components
- NPN output switches 3.0A, can stand off 65V
- Wide input voltage range: 3.5V to 40V
- Current-mode operation for improved transient response, line regulation, and current limit
- 52 kHz internal oscillator
- Soft-start function reduces in-rush current during start-up
- Output switch protected by current limit, under-voltage lockout, and thermal shutdown

Typical Applications

- Simple boost regulator
- Flyback and forward regulators
- Multiple-output regulator

Typical Application



TL/H/11468–1

Ordering Information

Temperature Range	Package Type	Output Voltage			NSC Package Drawing	Package
		12V	15V	ADJ		
−40°C ≤ T_A ≤ +125°C	24-Pin Surface Mount	LM2577M-12	LM2577M-15	LM2577M-ADJ	M24B	SO
	16-Pin Molded DIP	LM2577N-12	LM2577N-15	LM2577N-ADJ	N16A	N
	5-Lead Surface Mount	LM2577S-12	LM2577S-15	LM2577S-ADJ	TS5B	TO-263
	5-Straight Leads	LM2577T-12	LM2577T-15	LM2577T-ADJ	T05A	TO-220
	5-Bent Staggered Leads	LM2577T-12	LM2577T-15	LM2577T-ADJ	T05D	TO-220
		Flow LB03	Flow LB03	Flow LB03		
−55°C ≤ T_A ≤ +150°C	4-Pin TO-3	LM1577K-12/883	LM1577K-15/883	LM1577K-ADJ/883	K04A	TO-3

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	45V
Output Switch Voltage	65V
Output Switch Current (Note 2)	6.0A
Power Dissipation	Internally Limited
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec.)	260°C
Maximum Junction Temperature	150°C
Minimum ESD Rating (C = 100 pF, R = 1.5 kΩ)	2 kV

Operating Ratings

Supply Voltage	$3.5V \le V_{IN} \le 40V$
Output Switch Voltage	$0V \le V_{SWITCH} \le 60V$
Output Switch Current	$I_{SWITCH} \le 3.0A$
Junction Temperature Range	
LM1577	$-55°C \le T_J \le +150°C$
LM2577	$-40°C \le T_J \le +125°C$

Electrical Characteristics—LM1577-12, LM2577-12

Specifications with standard type face are for T_J = 25°C, and those in **bold type face** apply over full **Operating Temperature Range**. Unless otherwise specified, V_{IN} = 5V, and I_{SWITCH} = 0.

Symbol	Parameter	Conditions	Typical	LM1577-12 Limit (Notes 3, 4)	LM2577-12 Limit (Note 5)	Units (Limits)
SYSTEM PARAMETERS Circuit of *Figure 1* (Note 6)						
V_{OUT}	Output Voltage	V_{IN} = 5V to 10V I_{LOAD} = 100 mA to 800 mA (Note 3)	12.0	 11.60/**11.40** 12.40/**12.60**	 11.60/**11.40** 12.40/**12.60**	V V(min) V(max)
$\frac{\Delta V_{OUT}}{\Delta V_{IN}}$	Line Regulation	V_{IN} = 3.5V to 10V I_{LOAD} = 300 mA	20	 50/**100**	 50/**100**	mV mV(max)
$\frac{\Delta V_{OUT}}{\Delta_{LOAD}}$	Load Regulation	V_{IN} = 5V I_{LOAD} = 100 mA to 800 mA	20	 50/**100**	 50/**100**	mV mV(max)
η	Efficiency	V_{IN} = 5V, I_{LOAD} = 800 mA	80			%
DEVICE PARAMETERS						
I_S	Input Supply Current	$V_{FEEDBACK}$ = 14V (Switch Off)	7.5	 10.0/**14.0**	 10.0/**14.0**	mA mA(max)
		I_{SWITCH} = 2.0A V_{COMP} = 2.0V (Max Duty Cycle)	25	 50/**85**	 50/**85**	mA mA(max)
V_{UV}	Input Supply Undervoltage Lockout	I_{SWITCH} = 100 mA	2.90	 2.70/**2.65** 3.10/**3.15**	 2.70/**2.65** 3.10/**3.15**	V V(min) V(max)
f_O	Oscillator Frequency	Measured at Switch Pin I_{SWITCH} = 100 mA	52	 48/**42** 56/**62**	 48/**42** 56/**62**	kHz kHz(min) kHz(max)
V_{REF}	Output Reference Voltage	Measured at Feedback Pin V_{IN} = 3.5V to 40V V_{COMP} = 1.0V	12	 11.76/**11.64** 12.24/**12.36**	 11.76/**11.64** 12.24/**12.36**	V V(min) V(max)
$\frac{\Delta V_{REF}}{\Delta V_{IN}}$	Output Reference Voltage Line Regulator	V_{IN} = 3.5V to 40V	7			mV
R_{FB}	Feedback Pin Input Resistance		9.7			kΩ
G_M	Error Amp Transconductance	I_{COMP} = −30 μA to +30 μA V_{COMP} = 1.0V	370	 225/**145** 515/**615**	 225/**145** 515/**615**	μmho μmho(min) μmho(max)
A_{VOL}	Error Amp Voltage Gain	V_{COMP} = 1.1V to 1.9V R_{COMP} = 1.0 MΩ (Note 7)	80	 50/**25**	 50/**25**	V/V V/V(min)

Electrical Characteristics—LM1577-12, LM2577-12 (Continued)

Specifications with standard type face are for T_J = 25°C, and those in **bold type face** apply over full **Operating Temperature Range**. Unless otherwise specified, V_{IN} = 5V, and I_{SWITCH} = 0.

Symbol	Parameter	Conditions	Typical	LM1577-12 Limit (Notes 3, 4)	LM2577-12 Limit (Note 5)	Units (Limits)
DEVICE PARAMETERS (Continued)						
	Error Amplifier Output Swing	Upper Limit $V_{FEEDBACK}$ = 10.0V	2.4	2.2/**2.0**	2.2/**2.0**	V V(min)
		Lower Limit $V_{FEEDBACK}$ = 15.0V	0.3	0.40/**0.55**	0.40/**0.55**	V V(max)
	Error Amplifier Output Current	$V_{FEEDBACK}$ = 10.0V to 15.0V V_{COMP} = 1.0V	±200	±130/±**90** ±300/±**400**	±130/±**90** ±300/±**400**	µA µA(min) µA(max)
I_{SS}	Soft Start Current	$V_{FEEDBACK}$ = 10.0V V_{COMP} = 0V	5.0	2.5/**1.5** 7.5/**9.5**	2.5/**1.5** 7.5/**9.5**	µA µA(min) µA(max)
D	Maximum Duty Cycle	V_{COMP} = 1.5V I_{SWITCH} = 100 mA	95	93/**90**	93/**90**	% %(min)
$\frac{\Delta I_{SWITCH}}{\Delta V_{COMP}}$	Switch Transconductance		12.5			A/V
I_L	Switch Leakage Current	V_{SWITCH} = 65V $V_{FEEDBACK}$ = 15V (Switch Off)	10	300/**600**	300/**600**	µA µA(max)
V_{SAT}	Switch Saturation Voltage	I_{SWITCH} = 2.0A V_{COMP} = 2.0V (Max Duty Cycle)	0.5	0.7/**0.9**	0.7/**0.9**	V V(max)
	NPN Switch Current Limit		4.5	3.7/**3.0** 5.3/**6.0**	3.7/**3.0** 5.3/**6.0**	A A(min) A(max)

Electrical Characteristics—LM1577-15, LM2577-15

Specifications with standard type face are for T_J = 25°C, and those in **bold type face** apply over full **Operating Temperature Range**. Unless otherwise specified, V_{IN} = 5V, and I_{SWITCH} = 0.

Symbol	Parameter	Conditions	Typical	LM1577-15 Limit (Notes 3, 4)	LM2577-15 Limit (Note 5)	Units (Limits)
SYSTEM PARAMETERS Circuit of *Figure 2* (Note 6)						
V_{OUT}	Output Voltage	V_{IN} = 5V to 12V I_{LOAD} = 100 mA to 600 mA (Note 3)	15.0	 14.50/**14.25** 15.50/**15.75**	 14.50/**14.25** 15.50/**15.75**	V V(min) V(max)
$\frac{\Delta V_{OUT}}{V_{IN}}$	Line Regulation	V_{IN} = 3.5V to 12V I_{LOAD} = 300 mA	20	 50/**100**	 50/**100**	mV mV(max)
$\frac{\Delta V_{OUT}}{\Delta I_{LOAD}}$	Load Regulation	V_{IN} = 5V I_{LOAD} = 100 mA to 600 mA	20	 50/**100**	 50/**100**	mV mV(max)
η	Efficiency	V_{IN} = 5V, I_{LOAD} = 600 mA	80			%
DEVICE PARAMETERS						
I_S	Input Supply Current	$V_{FEEDBACK}$ = 18.0V (Switch Off)	7.5	 10.0/**14.0**	 10.0/**14.0**	mA mA(max)
		I_{SWITCH} = 2.0A V_{COMP} = 2.0V (Max Duty Cycle)	25	 50/**85**	 50/**85**	mA mA(max)
V_{UV}	Input Supply Undervoltage Lockout	I_{SWITCH} = 100 mA	2.90	 2.70/**2.65** 3.10/**3.15**	 2.70/**2.65** 3.10/**3.15**	V V(min) V(max)
f_O	Oscillator Frequency	Measured at Switch Pin I_{SWITCH} = 100 mA	52	 48/**42** 56/**62**	 48/**42** 56/**62**	kHz kHz(min) kHz(max)
V_{REF}	Output Reference Voltage	Measured at Feedback Pin V_{IN} = 3.5V to 40V V_{COMP} = 1.0V	15	 14.70/**14.55** 15.30/**15.45**	 14.70/**14.55** 15.30/**15.45**	V V(min) V(max)
$\frac{\Delta V_{REF}}{\Delta V_{IN}}$	Output Reference Voltage Line Regulation	V_{IN} = 3.5V to 40V	10			mV
R_{FB}	Feedback Pin Input Voltage Line Regulator		12.2			kΩ
G_M	Error Amp Transconductance	I_{COMP} = −30 μA to +30 μA V_{COMP} = 1.0V	300	 170/**110** 420/**500**	 170/**110** 420/**500**	μmho μmho(min) μmho(max)
A_{VOL}	Error Amp Voltage Gain	V_{COMP} = 1.1V to 1.9V R_{COMP} = 1.0 MΩ (Note 7)	65	 40/**20**	 40/**20**	V/V V/V(min)

3

Electrical Characteristics—LM1577-15, LM2577-15 (Continued)

Specifications with standard type face are for T_J = 25°C, and those in **bold type face** apply over full **Operating Temperature Range**. Unless otherwise specified, V_{IN} = 5V, and I_{SWITCH} = 0.

Symbol	Parameter	Conditions	Typical	LM1577-15 Limit (Notes 3, 4)	LM2577-15 Limit (Note 5)	Units (Limits)
DEVICE PARAMETERS (Continued)						
	Error Amplifier Output Swing	Upper Limit $V_{FEEDBACK}$ = 12.0V	2.4	2.2/**2.0**	2.2/**2.0**	V V(min)
		Lower Limit $V_{FEEDBACK}$ = 18.0V	0.3	0.4/**0.55**	0.40/**0.55**	V V(max)
	Error Amp Output Current	$V_{FEEDBACK}$ = 12.0V to 18.0V V_{COMP} = 1.0V	±200	±130/±**90** ±300/±**400**	±130/±**90** ±300/±**400**	µA µA(min) µA(max)
I_{SS}	Soft Start Current	$V_{FEEDBACK}$ = 12.0V V_{COMP} = 0V	5.0	2.5/**1.5** 7.5/**9.5**	2.5/**1.5** 7.5/**9.5**	µA µA(min) µA(max)
D	Maximum Duty Cycle	V_{COMP} = 1.5V I_{SWITCH} = 100 mA	95	93/**90**	93/**90**	% %(min)
$\frac{\Delta I_{SWITCH}}{\Delta V_{COMP}}$	Switch Transconductance		12.5			A/V
I_L	Switch Leakage Current	V_{SWITCH} = 65V $V_{FEEDBACK}$ = 18.0V (Switch Off)	10	300/**600**	300/**600**	µA µA(max)
V_{SAT}	Switch Saturation Voltage	I_{SWITCH} = 2.0A V_{COMP} = 2.0V (Max Duty Cycle)	0.5	0.7/**0.9**	0.7/**0.9**	V V(max)
	NPN Switch Current Limit	V_{COMP} = 2.0V	4.3	3.7/**3.0** 5.3/**6.0**	3.7/**3.0** 5.3/**6.0**	A A(min) A(max)

Electrical Characteristics—LM1577-ADJ, LM2577-ADJ

Specifications with standard type face are for T_J = 25°C, and those in **bold type face** apply over full **Operating Temperature Range**. Unless otherwise specified, V_{IN} = 5V, $V_{FEEDBACK}$ = V_{REF}, and I_{SWITCH} = 0.

Symbol	Parameter	Conditions	Typical	LM1577-ADJ Limit (Notes 3, 4)	LM2577-ADJ Limit (Note 5)	Units (Limits)
SYSTEM PARAMETERS Circuit of *Figure 3* (Note 6)						
V_{OUT}	Output Voltage	V_{IN} = 5V to 10V I_{LOAD} = 100 mA to 800 mA (Note 3)	12.0	11.60/**11.40** 12.40/**12.60**	11.60/**11.40** 12.40/**12.60**	V V(min) V(max)
$\Delta V_{OUT}/\Delta V_{IN}$	Line Regulation	V_{IN} = 3.5V to 10V I_{LOAD} = 300 mA	20	50/**100**	50/**100**	mV mV(max)
$\Delta V_{OUT}/\Delta I_{LOAD}$	Load Regulation	V_{IN} = 5V I_{LOAD} = 100 mA to 800 mA	20	50/**100**	50/**100**	mV mV(max)
η	Efficiency	V_{IN} = 5V, I_{LOAD} = 800 mA	80			%
DEVICE PARAMETERS						
I_S	Input Supply Current	$V_{FEEDBACK}$ = 1.5V (Switch Off)	7.5	10.0/**14.0**	10.0/**14.0**	mA mA(max)
		I_{SWITCH} = 2.0A V_{COMP} = 2.0V (Max Duty Cycle)	25	50/**85**	50/**85**	mA mA(max)
V_{UV}	Input Supply Undervoltage Lockout	I_{SWITCH} = 100 mA	2.90	2.70/**2.65** 3.10/**3.15**	2.70/**2.65** 3.10/**3.15**	V V(min) V(max)
f_O	Oscillator Frequency	Measured at Switch Pin I_{SWITCH} = 100 mA	52	48/**42** 56/**62**	48/**42** 56/**62**	kHz kHz(min) kHz(max)
V_{REF}	Reference Voltage	Measured at Feedback Pin V_{IN} = 3.5V to 40V V_{COMP} = 1.0V	1.230	1.214/**1.206** 1.246/**1.254**	1.214/**1.206** 1.246/**1.254**	V V(min) V(max)
$\Delta V_{REF}/\Delta V_{IN}$	Reference Voltage Line Regulation	V_{IN} = 3.5V to 40V	0.5			mV
I_B	Error Amp Input Bias Current	V_{COMP} = 1.0V	100	300/**800**	300/**800**	nA nA(max)
G_M	Error Amp Transconductance	I_{COMP} = −30 μA to +30 μA V_{COMP} = 1.0V	3700	2400/**1600** 4800/**5800**	2400/**1600** 4800/**5800**	μmho μmho(min) μmho(max)
A_{VOL}	Error Amp Voltage Gain	V_{COMP} = 1.1V to 1.9V R_{COMP} = 1.0 MΩ (Note 7)	800	500/**250**	500/**250**	V/V V/V(min)
	Error Amplifier Output Swing	Upper Limit $V_{FEEDBACK}$ = 1.0V	2.4	2.2/**2.0**	2.2/**2.0**	V V(min)
		Lower Limit $V_{FEEDBACK}$ = 1.5V	0.3	0.40/**0.55**	0.40/**0.55**	V V(max)

Electrical Characteristics—LM1577-ADJ, LM2577-ADJ (Continued)

Specifications with standard type face are for T_J = 25°C, and those in **bold type face** apply over full **Operating Temperature Range**. Unless otherwise specified, V_{IN} = 5V, $V_{FEEDBACK}$ = V_{REF}, and I_{SWITCH} = 0.

Symbol	Parameter	Conditions	Typical	LM1577-ADJ Limit (Notes 3, 4)	LM2577-ADJ Limit (Note 5)	Units (Limits)
DEVICE PARAMETERS (Continued)						
	Error Amp Output Current	$V_{FEEDBACK}$ = 1.0V to 1.5V V_{COMP} = 1.0V	±200	±130/±**90** ±300/±**400**	±130/±**90** ±300/±**400**	µA µA(min) µA(max)
I_{SS}	Soft Start Current	$V_{FEEDBACK}$ = 1.0V V_{COMP} = 0V	5.0	2.5/**1.5** 7.5/**9.5**	2.5/**1.5** 7.5/**9.5**	µA µA(min) µA(max)
D	Maximum Duty Cycle	V_{COMP} = 1.5V I_{SWITCH} = 100 mA	95	93/**90**	93/**90**	% %(min)
$\Delta I_{SWITCH}/\Delta V_{COMP}$	Switch Transconductance		12.5			A/V
I_L	Switch Leakage Current	V_{SWITCH} = 65V $V_{FEEDBACK}$ = 1.5V (Switch Off)	10	300/**600**	300/**600**	µA µA(max)
V_{SAT}	Switch Saturation Voltage	I_{SWITCH} = 2.0A V_{COMP} = 2.0V (Max Duty Cycle)	0.5	0.7/**0.9**	0.7/**0.9**	V V(max)
	NPN Switch Current Limit	V_{COMP} = 2.0V	4.3	3.7/**3.0** 5.3/**6.0**	3.7/**3.0** 5.3/**6.0**	A A(min) A(max)
THERMAL PARAMETERS (All Versions)						
θ_{JA} θ_{JC}	Thermal Resistance	K Package, Junction to Ambient K Package, Junction to Case	35 1.5			°C/W
θ_{JA} θ_{JC}		T Package, Junction to Ambient T Package, Junction to Case	65 2			
θ_{JA}		N Package, Junction to Ambient (Note 8)	85			
θ_{JA}		M Package, Junction to Ambient (Note 8)	100			
θ_{JA}		S Package, Junction to Ambient (Note 9)	37			

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating ratings indicate conditions the device is intended to be functional, but device parameter specifications may not be guaranteed under these conditions. For guaranteed specifications and test conditions, see the Electrical Characteristics.

Note 2: Due to timing considerations of the LM1577/LM2577 current limit circuit, output current cannot be internally limited when the LM1577/LM2577 is used as a step-up regulator. To prevent damage to the switch, its current must be externally limited to 6.0A. However, output current is internally limited when the LM1577/LM2577 is used as a flyback or forward converter regulator in accordance to the Application Hints.

Note 3: All limits guaranteed at room temperature (standard type face) and at temperature extremes (**boldface type**). All limits are used to calculate Outgoing Quality Level, and are 100% production tested.

Note 4: A military RETS electrical test specification is available on request. At the time of printing, the LM1577K-12/883, LM1577K-15/883, and LM1577K-ADJ/883 RETS specifications complied fully with the **boldface** limits in these columns. The LM1577K-12/883, LM1577K-15/883, and LM1577K-ADJ/883 may also be procured to Standard Military Drawing specifications.

Note 5: All limits guaranteed at room temperature (standard type face) and at temperature extremes (**boldface type**). All room temperature limits are 100% production tested. All limits at temperature extremes are guaranteed via correlation using standard Statistical Quality Control (SQC) methods.

Note 6: External components such as the diode, inductor, input and output capacitors can affect switching regulator performance. When the LM1577/LM2577 is used as shown in the Test Circuit, system performance will be as specified by the system parameters.

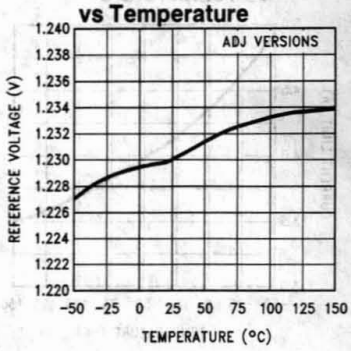
Note 7: A 1.0 MΩ resistor is connected to the compensation pin (which is the error amplifier's output) to ensure accuracy in measuring A_{VOL}. In actual applications, this pin's load resistance should be ≥10 MΩ, resulting in A_{VOL} that is typically twice the guaranteed minimum limit.

Note 8: Junction to ambient thermal resistance with approximately 1 square inch of pc board copper surrounding the leads. Additional copper area will lower thermal resistance further. See thermal model in "Switchers Made Simple" software.

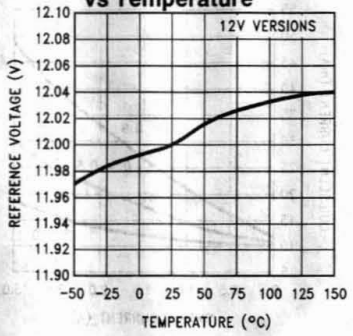
Note 9: If the TO-263 package is used, the thermal resistance can be reduced by increasing the PC board copper area thermally connected to the package. Using 0.5 square inches of copper area, θ_{JA} is 50°C/W; with 1 square inch of copper area, θ_{JA} is 37°C/W; and with 1.6 or more square inches of copper area, θ_{JA} is 32°C/W.

Typical Performance Characteristics

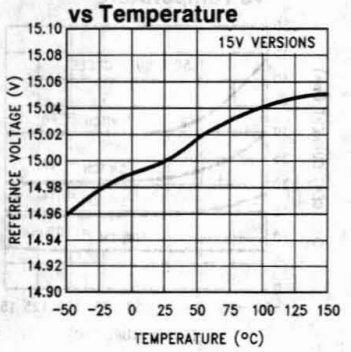
Reference Voltage vs Temperature



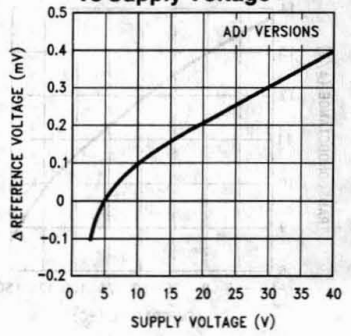
Reference Voltage vs Temperature



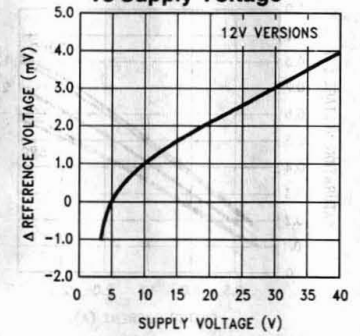
Reference Voltage vs Temperature



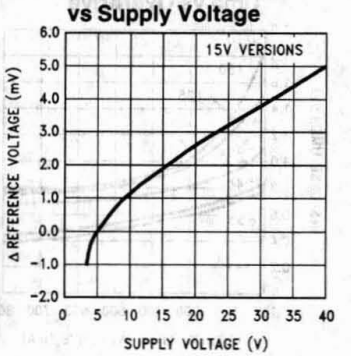
Δ Reference Voltage vs Supply Voltage



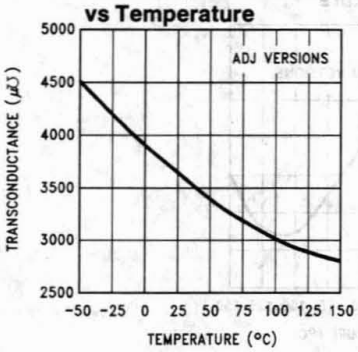
Δ Reference Voltage vs Supply Voltage



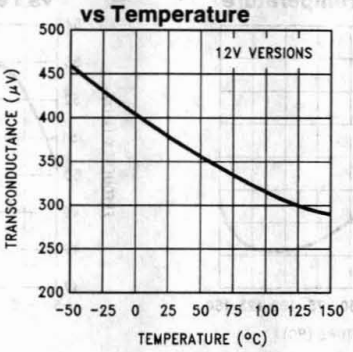
Δ Reference Voltage vs Supply Voltage



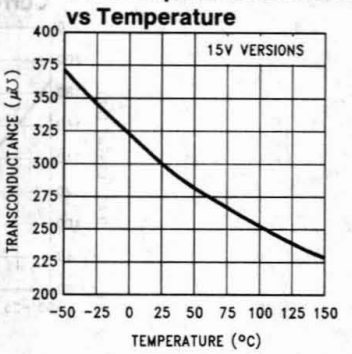
Error Amp Transconductance vs Temperature



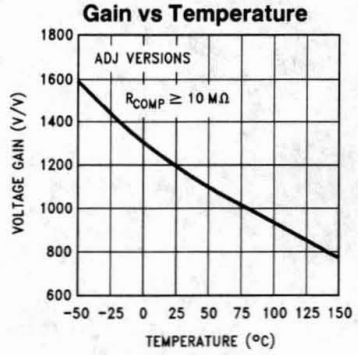
Error Amp Transconductance vs Temperature



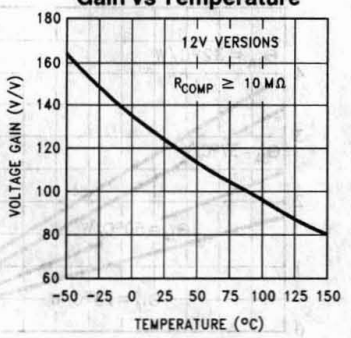
Error Amp Transconductance vs Temperature



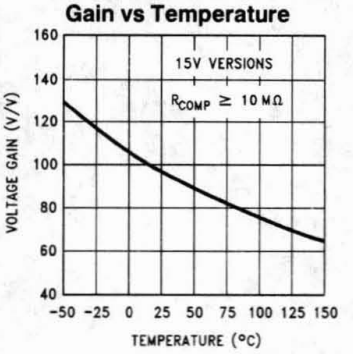
Error Amp Voltage Gain vs Temperature



Error Amp Voltage Gain vs Temperature



Error Amp Voltage Gain vs Temperature

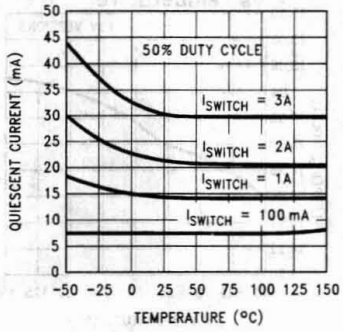


TL/H/11468–2

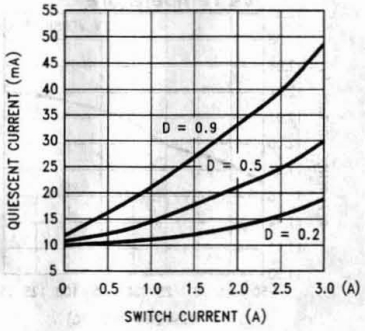
3

Typical Performance Characteristics (Continued)

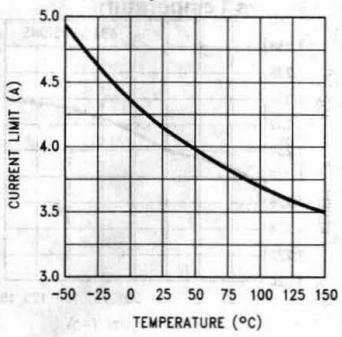
Quiescent Current vs Temperature



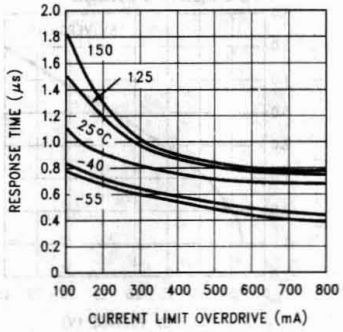
Quiescent Current vs Switch Current



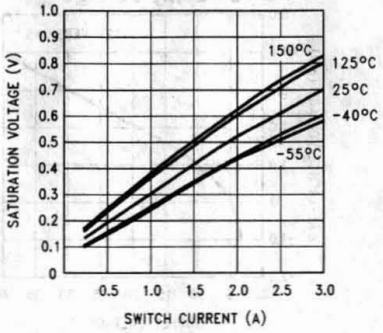
Current Limit vs Temperature



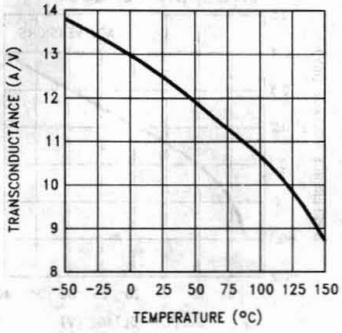
Current Limit Response Time vs Overdrive



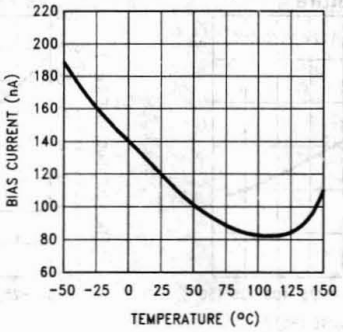
Switch Saturation Voltage vs Switch Current



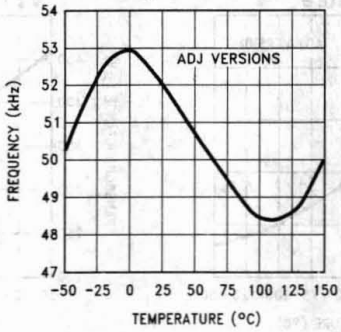
Switch Transconductance vs Temperature



Feedback Pin Bias Current vs Temperature

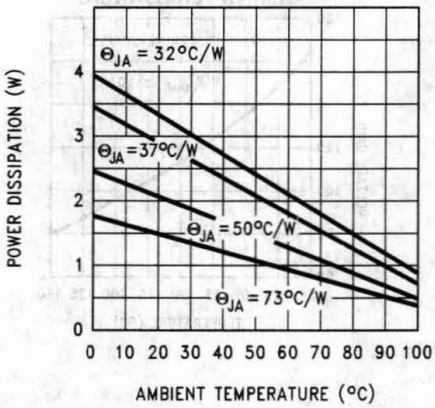


Oscillator Frequency vs Temperature



TL/H/11468–3

Maximum Power Dissipation (TO-263) (See Note 9)



TL/H/11468–31

Connection Diagrams

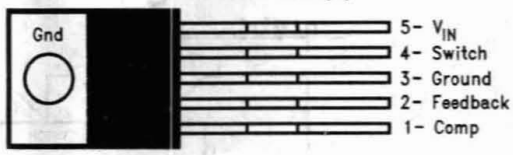
Straight Leads
5-Lead TO-220 (T)

TL/H/11468–4

Top View

Order Number LM2577T-12, LM2577T-15, or LM2577T-ADJ
See NS Package Number T05A

Bent, Staggered Leads
5-Lead TO-220 (T)

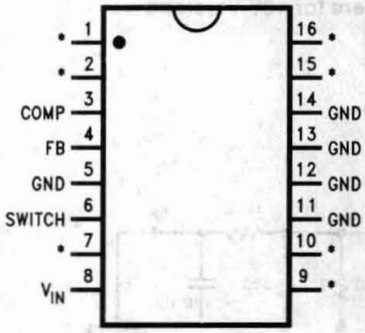


TL/H/11468–5

Top View

Order Number LM2577T-12 Flow LB03, LM2577T-15 Flow LB03, or LM2577T-ADJ Flow LB03
See NS Package Number T05D

16-Lead DIP (N)

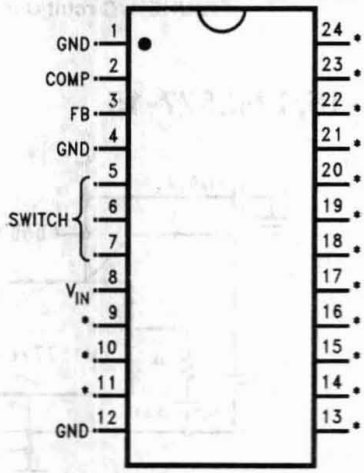


TL/H/11468–6

Top View

Order Number LM2577N-12, LM2577N-15, or LM2577N-ADJ
See NS Package Number N16A

24-Lead Surface Mount (M)

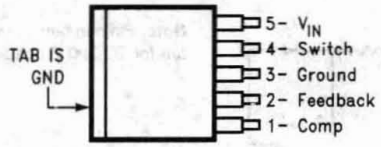


TL/H/11468–7

Top View

Order Number LM2577M-12, LM2577M-15, or LM2577M-ADJ
See NS Package Number M24B

TO-263 (S)
5-Lead Surface-Mount Package



TL/H/11468-32

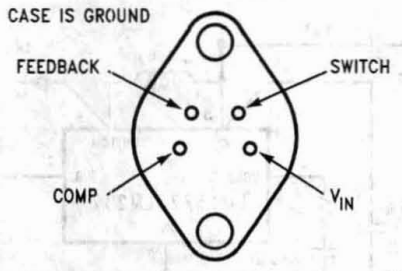
Top View

TL/H/11468-33

Side View

Order Number LM2577S-12, LM2577S-15, or LM2577S-ADJ
See NS Package Number TS5B

4-Lead TO-3 (K)



TL/H/11468–8

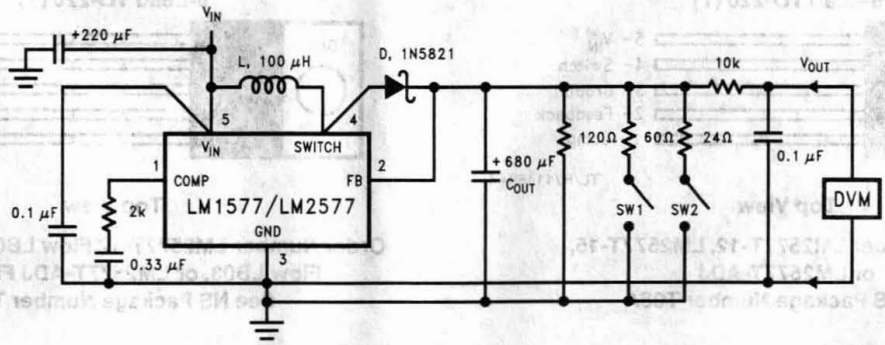
Bottom View

Order Number LM1577K-12/883, LM1577K-15/883, or LM1577K-ADJ/883
See NS Package Number K04A

3

Test Circuits

LM1577-12, LM2577-12



TL/H/11468–30

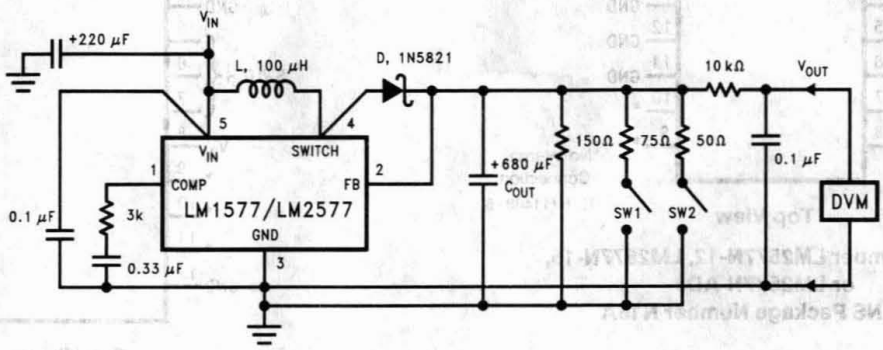
L = 415-0930 (AIE)
D = any manufacturer

C_{OUT} = Sprague Type 673D Electrolytic 680 µF, 20V

Note: Pin numbers shown are for TO-220 (T) package

FIGURE 1. Circuit Used to Specify System Parameters for 12V Versions

LM1577-15, LM2577-15



TL/H/11468–26

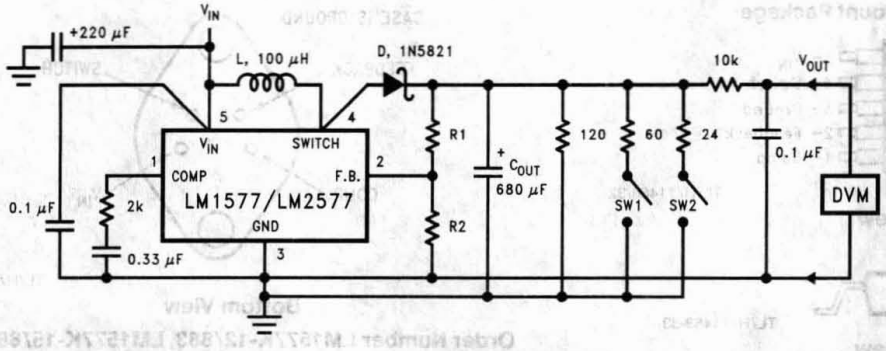
L = 415-0930 (AIE)
D = any manufacturer

C_{OUT} = Sprague Type 673D Electrolytic 680 µF, 20V

Note: Pin numbers shown are for TO-220 (T) package

FIGURE 2. Circuit Used to Specify System Parameters for 15V Versions

LM1577-ADJ, LM2577-ADJ



Note: Pin numbers shown are for TO-220 (T) package

TL/H/11468–9

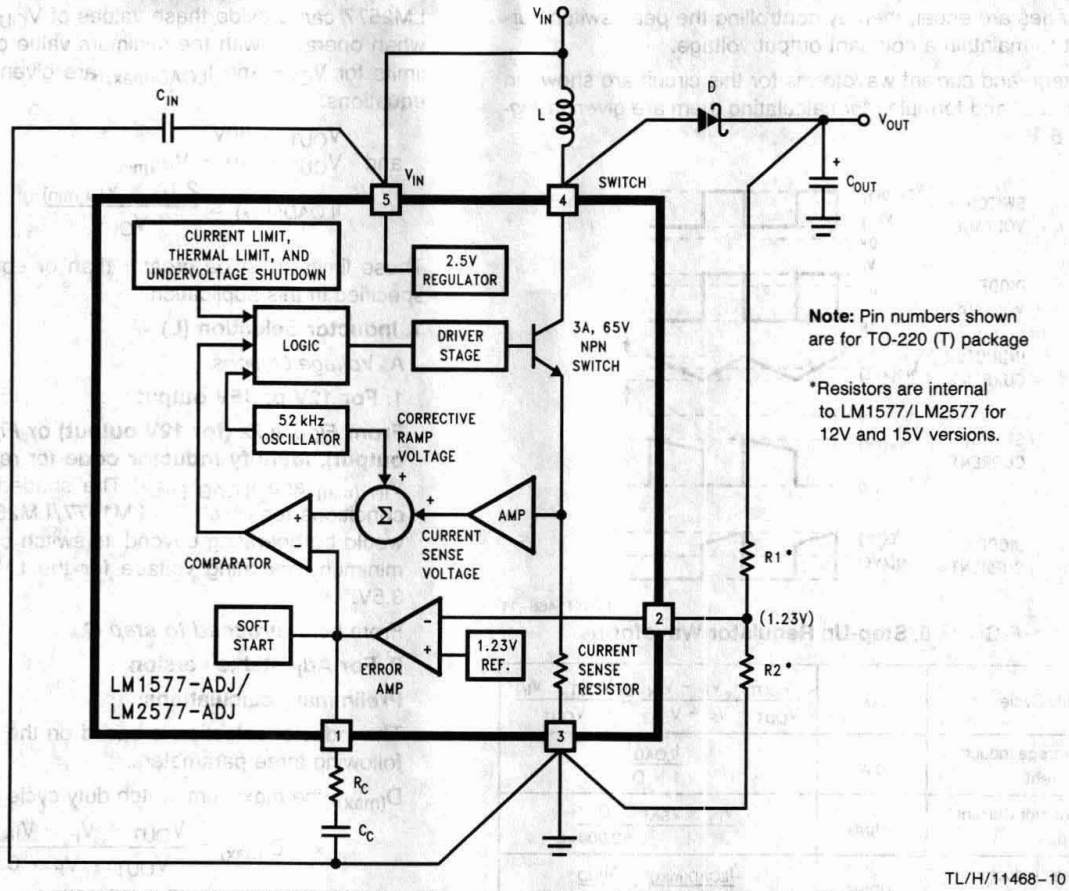
L = 415-0930 (AIE)
D = any manufacturer

C_{OUT} = Sprague Type 673D Electrolytic 680 µF, 20V

R1 = 48.7k in series with 511Ω (1%)
R2 = 5.62k (1%)

FIGURE 3. Circuit Used to Specify System Parameters for ADJ Versions

Application Hints



TL/H/11468–10

FIGURE 4. LM1577/LM2577 Block Diagram and Boost Regulator Application

STEP-UP (BOOST) REGULATOR

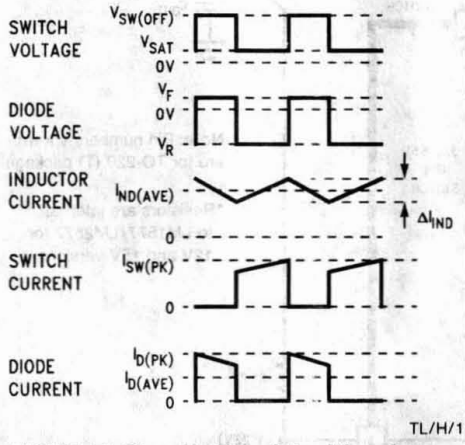
Figure 4 shows the LM1577-ADJ/LM2577-ADJ used as a Step-Up Regulator. This is a switching regulator used for producing an output voltage greater than the input supply voltage. The LM1577-12/LM2577-12 and LM1577-15/LM2577-15 can also be used for step-up regulators with 12V or 15V outputs (respectively), by tying the feedback pin directly to the regulator output.

A basic explanation of how it works is as follows. The LM1577/LM2577 turns its output switch on and off at a frequency of 52 kHz, and this creates energy in the inductor (L). When the NPN switch turns on, the inductor current charges up at a rate of V_{IN}/L, storing current in the inductor. When the switch turns off, the lower end of the inductor flies above V_{IN}, discharging its current through diode (D) into the output capacitor (C_{OUT}) at a rate of $(V_{OUT} - V_{IN})/L$. Thus, energy stored in the inductor during the switch on time is transferred to the output during the switch off time. The output voltage is controlled by the amount of energy transferred which, in turn, is controlled by modulating the peak inductor current. This is done by feeding back a portion of the output voltage to the error amp, which amplifies the difference between the feedback voltage and a 1.230V reference. The error amp output voltage is compared to a voltage proportional to the switch current (i.e., inductor current during the switch on time).

Application Hints (Continued)

The comparator terminates the switch on time when the two voltages are equal, thereby controlling the peak switch current to maintain a constant output voltage.

Voltage and current waveforms for this circuit are shown in *Figure 5*, and formulas for calculating them are given in *Figure 6*.



TL/H/11468–11

FIGURE 5. Step-Up Regulator Waveforms

Duty Cycle	D	$\frac{V_{OUT} + V_F - V_{IN}}{V_{OUT} + V_F - V_{SAT}} \approx \frac{V_{OUT} - V_{IN}}{V_{OUT}}$
Average Inductor Current	$I_{IND(AVE)}$	$\frac{I_{LOAD}}{1 - D}$
Inductor Current Ripple	ΔI_{IND}	$\frac{V_{IN} - V_{SAT}}{L} \frac{D}{52{,}000}$
Peak Inductor Current	$I_{IND(PK)}$	$\frac{I_{LOAD(max)}}{1 - D_{(max)}} + \frac{\Delta I_{IND}}{2}$
Peak Switch Current	$I_{SW(PK)}$	$\frac{I_{LOAD(max)}}{1 - D_{(max)}} + \frac{\Delta I_{IND}}{2}$
Switch Voltage When Off	$V_{SW(OFF)}$	$V_{OUT} + V_F$
Diode Reverse Voltage	V_R	$V_{OUT} - V_{SAT}$
Average Diode Current	$I_{D(AVE)}$	I_{LOAD}
Peak Diode Current	$I_{D(PK)}$	$\frac{I_{LOAD}}{1 - D_{(max)}} + \frac{\Delta I_{IND}}{2}$
Power Dissipation of LM1577/2577	P_D	$0.25\Omega \left(\frac{I_{LOAD}}{1 - D}\right)^2 D + \frac{I_{LOAD}\, D\, V_{IN}}{50\,(1 - D)}$

V_F = Forward Biased Diode Voltage
I_{LOAD} = Output Load Current

FIGURE 6. Step-Up Regulator Formulas

STEP-UP REGULATOR DESIGN PROCEDURE

The following design procedure can be used to select the appropriate external components for the circuit in *Figure 4*, based on these system requirements.

Given:

$V_{IN\ (min)}$ = Minimum input supply voltage
V_{OUT} = Regulated output voltage
$I_{LOAD(max)}$ = Maximum output load current

Before proceeding any further, determine if the LM1577/LM2577 can provide these values of V_{OUT} and $I_{LOAD(max)}$ when operating with the minimum value of V_{IN}. The upper limits for V_{OUT} and $I_{LOAD(max)}$ are given by the following equations.

$$V_{OUT} \leq 60V$$

and $V_{OUT} \leq 10 \times V_{IN(min)}$

$$I_{LOAD(max)} \leq \frac{2.1A \times V_{IN(min)}}{V_{OUT}}$$

These limits must be greater than or equal to the values specified in this application.

1. Inductor Selection (L)

A. *Voltage Options:*

1. **For 12V or 15V output**

From *Figure 7a* (for 12V output) or *Figure 7b* (for 15V output), identify inductor code for region indicated by $V_{IN\ (min)}$ and $I_{LOAD\ (max)}$. The shaded region indicates conditions for which the LM1577/LM2577 output switch would be operating beyond its switch current rating. The minimum operating voltage for the LM1577/LM2577 is 3.5V.

From here, ***proceed to step C***.

2. **For Adjustable version**

Preliminary calculations:

The inductor selection is based on the calculation of the following three parameters:

$D_{(max)}$, the maximum switch duty cycle ($0 \leq D \leq 0.9$):

$$D_{(max)} = \frac{V_{OUT} + V_F - V_{IN(min)}}{V_{OUT} + V_F - 0.6V}$$

where V_F = 0.5V for Schottky diodes and 0.8V for fast recovery diodes (typically);

E•T, the product of volts × time that charges the inductor:

$$E \bullet T = \frac{D_{(max)}\,(V_{IN(min)} - 0.6V)10^6}{52{,}000\ Hz} \quad (V \bullet \mu s)$$

$I_{IND,DC}$, the average inductor current under full load;

$$I_{IND,DC} = \frac{1.05 \times I_{LOAD(max)}}{1 - D_{(max)}}$$

B. *Identify Inductor Value:*

1. From *Figure 7c*, identify the inductor code for the region indicated by the intersection of E•T and $I_{IND,DC}$. This code gives the inductor value in microhenries. The L or H prefix signifies whether the inductor is rated for a maximum E•T of 90 V•μs (L) or 250 V•μs (H).

2. If $D < 0.85$, go on to step C. If $D \geq 0.85$, then calculate the minimum inductance needed to ensure the switching regulator's stability:

$$L_{MIN} = \frac{6.4\,(V_{IN(min)} - 0.6V)\,(2D_{(max)} - 1)}{1 - D_{(max)}} \quad (\mu H)$$

If L_{MIN} is smaller than the inductor value found in step B1, go on to step C. Otherwise, the inductor value found in step B1 is too low; an appropriate inductor code should be obtained from the graph as follows:

1. Find the lowest value inductor that is greater than L_{MIN}.
2. Find where E•T intersects this inductor value to determine if it has an L or H prefix. If E•T intersects both the L and H regions, select the inductor with an H prefix.

Application Hints (Continued)

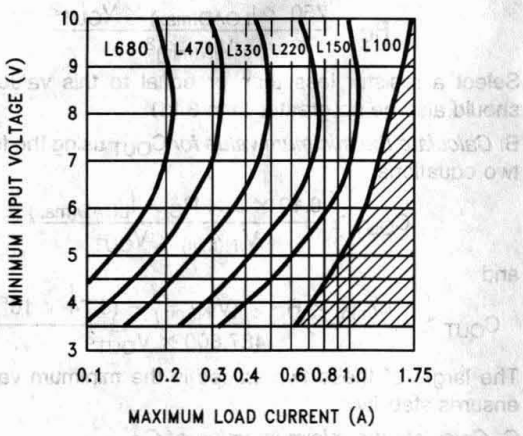


FIGURE 7a. LM2577-12 Inductor Selection Guide

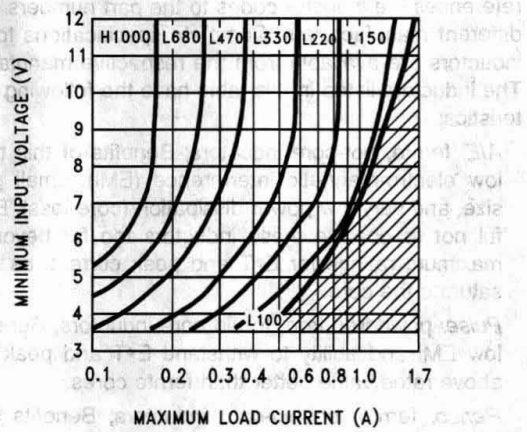


FIGURE 7b. LM2577-15 Inductor Selection Guide

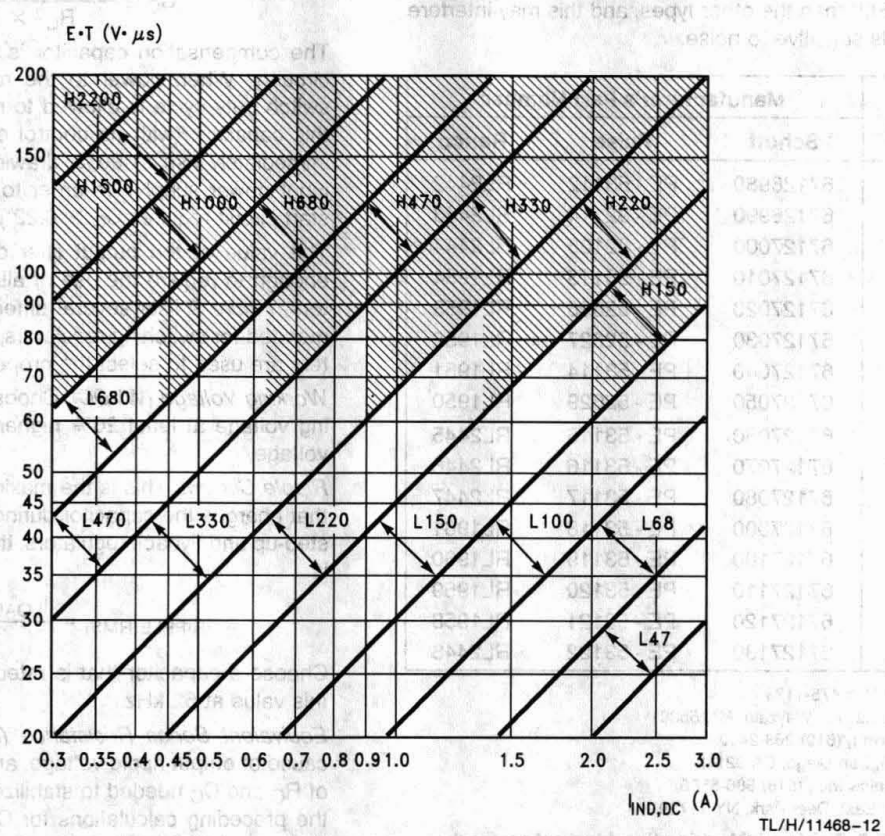


FIGURE 7c. LM1577-ADJ/LM2577-ADJ Inductor Selection Graph

Note:

These charts assume that the inductor ripple current inductor is approximately 20% to 30% of the average inductor current (when the regulator is under full load). Greater ripple current causes higher peak switch currents and greater output ripple voltage; lower ripple current is achieved with larger-value inductors. The factor of 20 to 30% is chosen as a convenient balance between the two extremes.

Application Hints (Continued)

C. *Select an inductor* from the table of *Figure 8* which cross-references the inductor codes to the part numbers of three different manufacturers. Complete specifications for these inductors are available from the respective manufacturers. The inductors listed in this table have the following characteristics:

AIE: ferrite, pot-core inductors; Benefits of this type are low electro-magnetic interference (EMI), small physical size, and very low power dissipation (core loss). Be careful not to operate these inductors too far beyond their maximum ratings for E•T and peak current, as this will saturate the core.

Pulse: powdered iron, toroid core inductors; Benefits are low EMI and ability to withstand E•T and peak current above rated value better than ferrite cores.

Renco: ferrite, bobbin-core inductors; Benefits are low cost and best ability to withstand E•T and peak current above rated value. Be aware that these inductors generate more EMI than the other types, and this may interfere with signals sensitive to noise.

Inductor Code	Manufacturer's Part Number		
	Schott	Pulse	Renco
L47	67126980	PE - 53112	RL2442
L68	67126990	PE - 92114	RL2443
L100	67127000	PE - 92108	RL2444
L150	67127010	PE - 53113	RL1954
L220	67127020	PE - 52626	RL1953
L330	67127030	PE - 52627	RL1952
L470	67127040	PE - 53114	RL1951
L680	67127050	PE - 52629	RL1950
H150	67127060	PE - 53115	RL2445
H220	67127070	PE - 53116	RL2446
H330	67127080	PE - 53117	RL2447
H470	67127090	PE - 53118	RL1961
H680	67127100	PE - 53119	RL1960
H1000	67127110	PE - 53120	RL1959
H1500	67127120	PE - 53121	RL1958
H2200	67127130	PE - 53122	RL2448

Schott Corp., (612) 475-1173
1000 Parkers Lake Rd., Wayzata, MN 55391
Pulse Engineering, (619) 268-2400
P.O. Box 12235, San Diego, CA 92112
Renco Electronics Inc., (516) 586-5566
60 Jeffryn Blvd. East, Deer Park, NY 11729

FIGURE 8. Table of Standardized Inductors and Manufacturer's Part Numbers

2. Compensation Network (R_C, C_C) and Output Capacitor (C_{OUT}) Selection

R_C and C_C form a pole-zero compensation network that stabilizes the regulator. The values of R_C and C_C are mainly dependant on the regulator voltage gain, $I_{LOAD(max)}$, L and C_{OUT}. The following procedure calculates values for R_C, C_C, and C_{OUT} that ensure regulator stability. Be aware that this procedure doesn't necessarily result in R_C and C_C that provide optimum compensation. In order to guarantee optimum compensation, one of the standard procedures for testing loop stability must be used, such as measuring V_{OUT} transient response when pulsing I_{LOAD} (see *Figure 13*).

A. *First, calculate the maximum value for* R_C

$$R_C \le \frac{750 \times I_{LOAD(max)} \times V_{OUT}^2}{V_{IN(min)}^2}$$

Select a resistor less than or equal to this value, and it should also be no greater than 3 kΩ.

B. *Calculate the minimum value for* C_{OUT} using the following two equations.

$$C_{OUT} \ge \frac{0.19 \times L \times R_C \times I_{LOAD(max)}}{V_{IN(min)} \times V_{OUT}}$$

and

$$C_{OUT} \ge \frac{V_{IN(min)} \times R_C \times (V_{IN(min)} + (3.74 \times 10^5 \times L))}{487{,}800 \times V_{OUT}^3}$$

The larger of these two values is the minimum value that ensures stability.

C. *Calculate the minimum value of* C_C.

$$C_C \ge \frac{58.5 \times V_{OUT}^2 \times C_{OUT}}{R_C^2 \times V_{IN(min)}}$$

The compensation capacitor is also part of the soft start circuitry. When power to the regulator is turned on, the switch duty cycle is allowed to rise at a rate controlled by this capacitor (with no control on the duty cycle, it would immediately rise to 90%, drawing huge currents from the input power supply). In order to operate properly, the soft start circuit requires $C_C \ge 0.22\ \mu F$.

The value of the output filter capacitor is normally large enough to require the use of aluminum electrolytic capacitors. *Figure 9* lists several different types that are recommended for switching regulators, and the following parameters are used to select the proper capacitor.

Working Voltage (WVDC): Choose a capacitor with a working voltage at least 20% higher than the regulator output voltage.

Ripple Current: This is the maximum RMS value of current that charges the capacitor during each switching cycle. For step-up and flyback regulators, the formula for ripple current is

$$I_{RIPPLE(RMS)} = \frac{I_{LOAD(max)} \times D_{(max)}}{1 - D_{(max)}}$$

Choose a capacitor that is rated at least 50% higher than this value at 52 kHz.

Equivalent Series Resistance (ESR): This is the primary cause of output ripple voltage, and it also affects the values of R_C and C_C needed to stabilize the regulator. As a result, the preceding calculations for C_C and R_C are only valid if ESR doesn't exceed the maximum value specified by the following equations.

$$ESR \le \frac{0.01 \times V_{OUT}}{I_{RIPPLE(P-P)}} \text{ and } \le \frac{8.7 \times (10) - 3 \times V_{IN}}{I_{LOAD(max)}}$$

where

$$I_{RIPPLE(P-P)} = \frac{1.15 \times I_{LOAD(max)}}{1 - D_{(max)}}$$

Select a capacitor with ESR, at 52 kHz, that is less than or equal to the lower value calculated. Most electrolytic capacitors specify ESR at 120 Hz which is 15% to 30% higher than at 52 kHz. Also, be aware that ESR increases by a factor of 2 when operating at −20°C.

Application Hints (Continued)

In general, low values of ESR are achieved by using large value capacitors (C ≥ 470 μF), and capacitors with high WVDC, or by paralleling smaller-value capacitors.

3. Output Voltage Selection (R1 and R2)

This section is for applications using the LM1577-ADJ/LM2577-ADJ. Skip this section if the LM1577-12/LM2577-12 or LM1577-15/LM2577-15 is being used.

With the LM1577-ADJ/LM2577-ADJ, the output voltage is given by

$$V_{OUT} = 1.23V\,(1 + R1/R2)$$

Resistors R1 and R2 divide the output down so it can be compared with the LM1577-ADJ/LM2577-ADJ internal 1.23V reference. For a given desired output voltage V_{OUT}, select R1 and R2 so that

$$\frac{R1}{R2} = \frac{V_{OUT}}{1.23V} - 1$$

4. Input Capacitor Selection (C_{IN})

The switching action in the step-up regulator causes a triangular ripple current to be drawn from the supply source. This in turn causes noise to appear on the supply voltage. For proper operation of the LM1577, the input voltage should be decoupled. Bypassing the Input Voltage pin directly to ground with a good quality, low ESR, 0.1 μF capacitor (leads as short as possible) is normally sufficient.

If the LM1577 is located far from the supply source filter capacitors, an additional large electrolytic capacitor (e.g. 47 μF) is often required.

5. Diode Selection (D)

The switching diode used in the boost regulator must withstand a reverse voltage equal to the circuit output voltage, and must conduct the peak output current of the LM2577. A suitable diode must have a minimum reverse breakdown voltage greater than the circuit output voltage, and should be rated for average and peak current greater than $I_{LOAD(max)}$ and $I_{D(PK)}$. Schottky barrier diodes are often favored for use in switching regulators. Their low forward voltage drop allows higher regulator efficiency than if a (less expensive) fast recovery diode was used. See *Figure 10* for recommended part numbers and voltage ratings of 1A and 3A diodes.

Cornell Dublier—Types 239, 250, 251, UFT, 300, or 350
P.O. Box 128, Pickens, SC 29671
(803) 878-6311

Nichicon—Types PF, PX, or PZ
927 East Parkway, Schaumburg, IL 60173
(708) 843-7500

Sprague—Types 672D, 673D, or 674D
Box 1, Sprague Road, Lansing, NC 28643
(919) 384-2551

United Chemi-Con—Types LX, SXF, or SXJ
9801 West Higgins Road, Rosemont, IL 60018
(708) 696-2000

FIGURE 9. Aluminum Electrolytic Capacitors Recommended for Switching Regulators

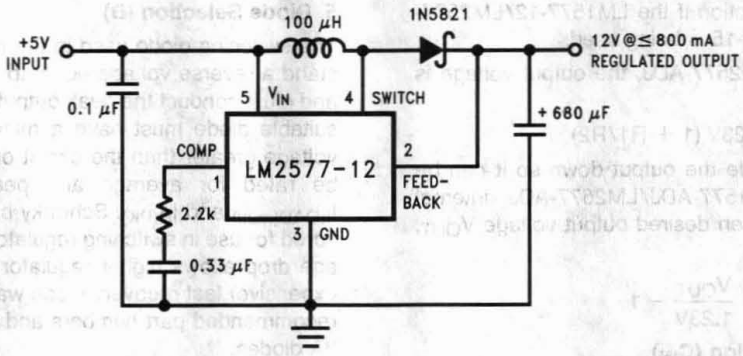
V_{OUT} (max)	Schottky		Fast Recovery	
	1A	3A	1A	3A
20V	1N5817 MBR120P	1N5820 MBR320P		
30V	1N5818 MBR130P 11DQ03	1N5821 MBR330P 31DQ03		
40V	1N5819 MBR140P 11DQ04	1N5822 MBR340P 31DQ04		
50V	MBR150 11DQ05	MBR350 31DQ05	1N4933 MUR105	
100V			1N4934 HER102 MUR110 10DL1	MR851 30DL1 MR831 HER302

FIGURE 10. Diode Selection Chart

Application Hints (Continued)

BOOST REGULATOR CIRCUIT EXAMPLE

By adding a few external components (as shown in *Figure 11*), the LM2577 can be used to produce a regulated output voltage that is greater than the applied input voltage. Typical performance of this regulator is shown in *Figures 12* and *13*. The switching waveforms observed during the operation of this circuit are shown in *Figure 14*.



TL/H/11468–13

Note: Pin numbers shown are for TO-220 (T) package.

FIGURE 11. Step-up Regulator Delivers 12V from a 5V Input

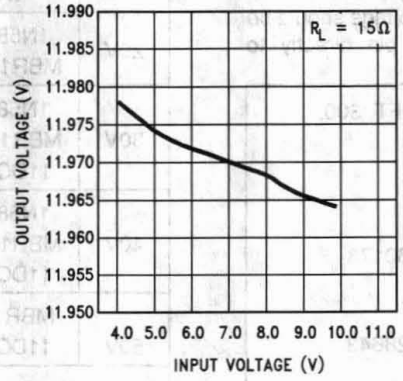


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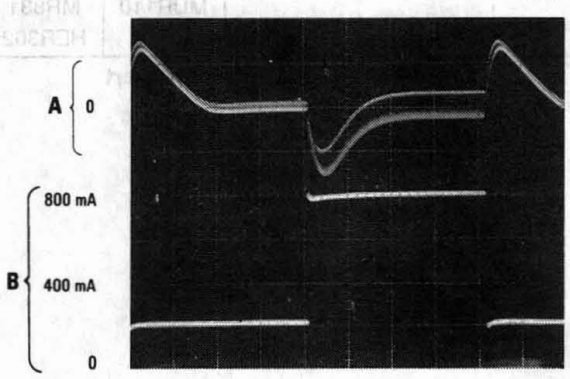
FIGURE 12. Line Regulation (Typical) of Step-Up Regulator of *Figure 11*



TL/H/11468–15

FIGURE 13. Load Transient Response of Step-Up Regulator of *Figure 11*

A: Output Voltage Change, 100 mV/div. (AC-coupled)
B: Load current, 0.2 A/div
Horizontal: 5 ms/div

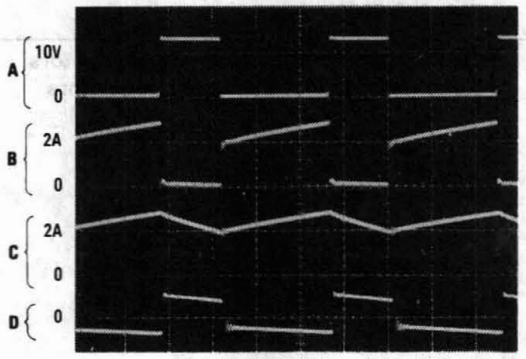


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FIGURE 14. Switching Waveforms of Step-Up Regulator of *Figure 11*

A: Switch pin voltage, 10 V/div
B: Switch pin current, 2 A/div
C: Inductor current, 2 A/div
D: Output ripple voltage, 100 mV/div (AC-coupled)
Horizontal: 5 μs/div

Application Hints (Continued)

FLYBACK REGULATOR

A Flyback regulator can produce single or multiple output voltages that are lower or greater than the input supply voltage. *Figure 15* shows the LM1577/LM2577 used as a flyback regulator with positive and negative regulated outputs. Its operation is similar to a step-up regulator, except the output switch contols the primary current of a flyback transformer. Note that the primary and secondary windings are out of phase, so no current flows through secondary when current flows through the primary. This allows the primary to charge up the transformer core when the switch is on. When the switch turns off, the core discharges by sending current through the secondary, and this produces voltage at the outputs. The output voltages are controlled by adjusting the peak primary current, as described in the step-up regulator section.

Voltage and current waveforms for this circuit are shown in *Figure 16*, and formulas for calculating them are given in *Figure 17*.

FLYBACK REGULATOR DESIGN PROCEDURE

1. Transformer Selection

A family of standardized flyback transformers is available for creating flyback regulators that produce dual output voltages, from ±10V to ±15V, as shown in *Figure 15*. *Figure 18* lists these transformers with the input voltage, output voltages and maximum load current they are designed for.

2. Compensation Network (C_C, R_C) and Output Capacitor (C_{OUT}) Selection

As explained in the Step-Up Regulator Design Procedure, C_C, R_C and C_{OUT} must be selected as a group. The following procedure is for a dual output flyback regulator with equal turns ratios for each secondary (i.e., both output voltages have the same magnitude). The equations can be used for a single output regulator by changing $\Sigma I_{LOAD(max)}$ to $I_{LOAD(max)}$ in the following equations.

A. **First, calculate the maximum value for R_C.**

$$R_C \leq \frac{750 \times \Sigma I_{LOAD(max)} \times (15V + V_{IN(min)}N)^2}{V_{IN(min)}^2}$$

Where $\Sigma I_{LOAD(max)}$ is the sum of the load current (magnitude) required from both outputs. Select a resistor less than or equal to this value, and no greater than 3 kΩ.

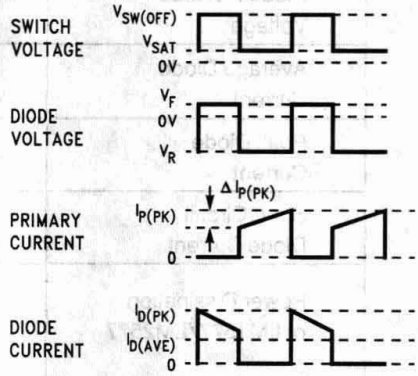
B. **Calculate the minimum value for ΣC_{OUT}** (sum of C_{OUT} at both outputs) using the following two equations.

$$C_{OUT} \geq \frac{0.19 \times R_C \times L_P \times \Sigma I_{LOAD(max)}}{15V \times V_{IN(min)}}$$

and

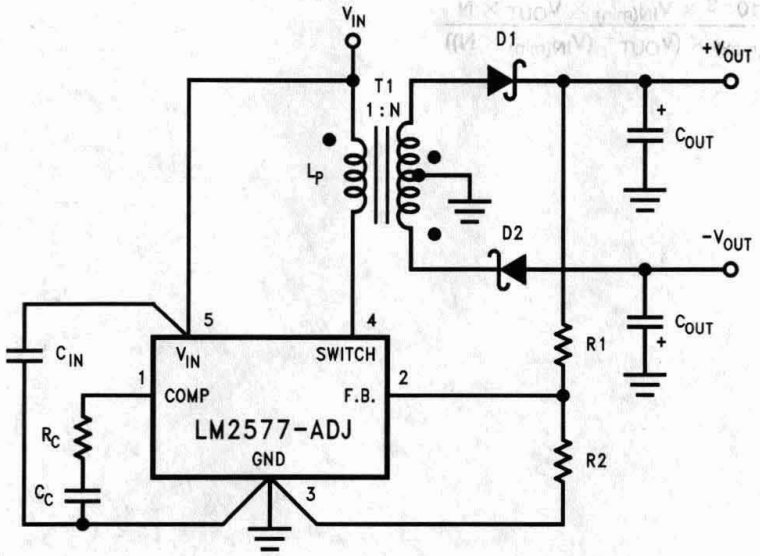
$$C_{OUT} \geq \frac{V_{IN(min)} \times R_C \times N^2 \times (V_{IN(min)} + (3.74 \times 10^5 \times L_P))}{487{,}800 \times (15V)^2 \times (15V + V_{IN(min)} \times N)}$$

The larger of these two values must be used to ensure regulator stability.



TL/H/11468–17

FIGURE 16. Flyback Regulator Waveforms



TL/H/11468–18

T1 = Pulse Engineering, PE-65300

D1, D2 = 1N5821

FIGURE 15. LM1577-ADJ/LM2577-ADJ Flyback Regulator with ± Outputs

Application Hints (Continued)

Duty Cycle	D	$\frac{V_{OUT} + V_F}{N(V_{IN} - V_{SAT}) + V_{OUT} + V_F} \approx \frac{V_{OUT}}{N(V_{IN}) + V_{OUT}}$
Primary Current Variation	ΔI_P	$\frac{D(V_{IN} - V_{SAT})}{L_P \times 52{,}000}$
Peak Primary Current	$I_{P(PK)}$	$\frac{N}{\eta} \times \frac{\Sigma I_{LOAD}}{1 - D} + \frac{\Delta I_{PK}}{2}$
Switch Voltage when Off	$V_{SW(OFF)}$	$V_{IN} + \frac{V_{OUT} + V_F}{N}$
Diode Reverse Voltage	V_R	$V_{OUT} + N(V_{IN} - V_{SAT})$
Average Diode Current	$I_{D(AVE)}$	I_{LOAD}
Peak Diode Current	$I_{D(PK)}$	$\frac{I_{LOAD}}{1 - D} + \frac{\Delta I_{IND}}{2}$
Short Circuit Diode Current		$\approx \frac{6A}{N}$
Power Dissipation of LM1577/LM2577	P_D	$0.25\Omega \left(\frac{N \Sigma I_{LOAD}}{1 - D}\right)^2 + \frac{N I_{LOAD} D}{50(1 - D)} V_{IN}$

N = Transformer Turns Ratio = $\frac{\text{number of secondary turns}}{\text{number of primary turns}}$

η = Transformer Efficiency *(typically 0.95)*

$\Sigma I_{LOAD} = |+I_{LOAD}| + |-I_{LOAD}|$

FIGURE 17. Flyback Regulator Formulas

C. *Calculate the minimum value of* C_C

$$C_C \geq \frac{58.5 \times C_{OUT} \times V_{OUT} \times (V_{OUT} + (V_{IN(min)} \times N))}{R_C^2 \times V_{IN(min)} \times N}$$

D. *Calculate the maximum ESR* of the $+V_{OUT}$ and $-V_{OUT}$ output capacitors in parallel.

$$ESR_+ \| ESR_- \leq \frac{8.7 \times 10^{-3} \times V_{IN(min)} \times V_{OUT} \times N}{\Sigma I_{LOAD(max)} \times (V_{OUT} + (V_{IN(min)} \times N))}$$

This formula can also be used to calculate the maximum ESR of a single output regulator.

At this point, refer to this same section in the **Step-Up Regulator Design Procedure** for more information regarding the selection of C_{OUT}.

Application Hints (Continued)

3. Output Voltage Selection

This section is for applications using the LM1577-ADJ/LM2577-ADJ. Skip this section if the LM1577-12/LM2577-12 or LM1577-15/LM2577-15 is being used.

With the LM1577-ADJ/LM2577-ADJ, the output voltage is given by

$$V_{OUT} = 1.23V\,(1 + R1/R2)$$

Resistors R1 and R2 divide the output voltage down so it can be compared with the LM1577-ADJ/LM2577-ADJ internal 1.23V reference. For a desired output voltage V_{OUT}, select R1 and R2 so that

$$\frac{R1}{R2} = \frac{V_{OUT}}{1.23V} - 1$$

4. Diode Selection

The switching diode in a flyback converter must withstand the reverse voltage specified by the following equation.

$$V_R = V_{OUT} + \frac{V_{IN}}{N}$$

A suitable diode must have a reverse voltage rating greater than this. In addition it must be rated for more than the average and peak diode currents listed in *Figure 17*.

5. Input Capacitor Selection

The primary of a flyback transformer draws discontinuous pulses of current from the input supply. As a result, a flyback regulator generates more noise at the input supply than a step-up regulator, and this requires a larger bypass capacitor to decouple the LM1577/LM2577 V_{IN} pin from this noise. For most applications, a low ESR, 1.0 μF cap will be sufficient, if it is connected very close to the V_{IN} and Ground pins.

In addition to this bypass cap, a larger capacitor ($\geq$ 47 μF) should be used where the flyback transformer connects to the input supply. This will attenuate noise which may interfere with other circuits connected to the same input supply voltage.

Transformer Type		Input Voltage	Dual Output Voltage	Maximum Output Current
1	L_P = 100 μH, N = 1	5V	±10V	325 mA
		5V	±12V	275 mA
		5V	±15V	225 mA
2	L_P = 200 μH, N = 0.5	10V	±10V	700 mA
		10V	±12V	575 mA
		10V	±15V	500 mA
		12V	±10V	800 mA
		12V	±12V	700 mA
		12V	±15V	575 mA
3	L_P = 250 μH, N = 0.5	15V	±10V	900 mA
		15V	±12V	825 mA
		15V	±15V	700 mA

Transformer Type	Manufacturers' Part Numbers		
	AIE	Pulse	Renco
1	326-0637	PE-65300	RL-2580
2	330-0202	PE-65301	RL-2581
3	330-0203	PE-65302	RL-2582

FIGURE 18. Flyback Transformer Selection Guide

6. Snubber Circuit

A "snubber" circuit is required when operating from input voltages greater than 10V, or when using a transformer with $L_P \geq 200$ μH. This circuit clamps a voltage spike from the transformer primary that occurs immediately after the output switch turns off. Without it, the switch voltage may exceed the 65V maximum rating. As shown in *Figure 19*, the snubber consists of a fast recovery diode, and a parallel RC. The RC values are selected for switch clamp voltage (V_{CLAMP}) that is 5V to 10V greater than $V_{SW(OFF)}$. Use the following equations to calculate R and C;

$$C \geq \frac{0.02 \times L_P \times I_{P(PK)}^2}{(V_{CLAMP})^2 - (VSW_{(OFF)})^2}$$

$$R \leq \left(\frac{V_{CLAMP} + V_{SW(OFF)} - V_{IN}}{2}\right)^2 \times \left(\frac{19.2 \times 10^{-4}}{L_P \times I_{P(PK)}^2}\right)$$

Power dissipation (and power rating) of the resistor is;

$$P = \left(\frac{V_{CLAMP} + V_{SW(OFF)} - V_{IN}}{2}\right)^2 / R$$

The fast recovery diode must have a reverse voltage rating greater than V_{CLAMP}.

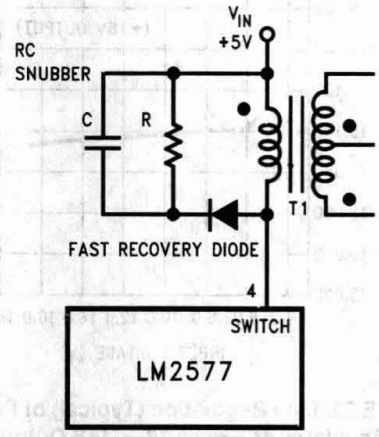


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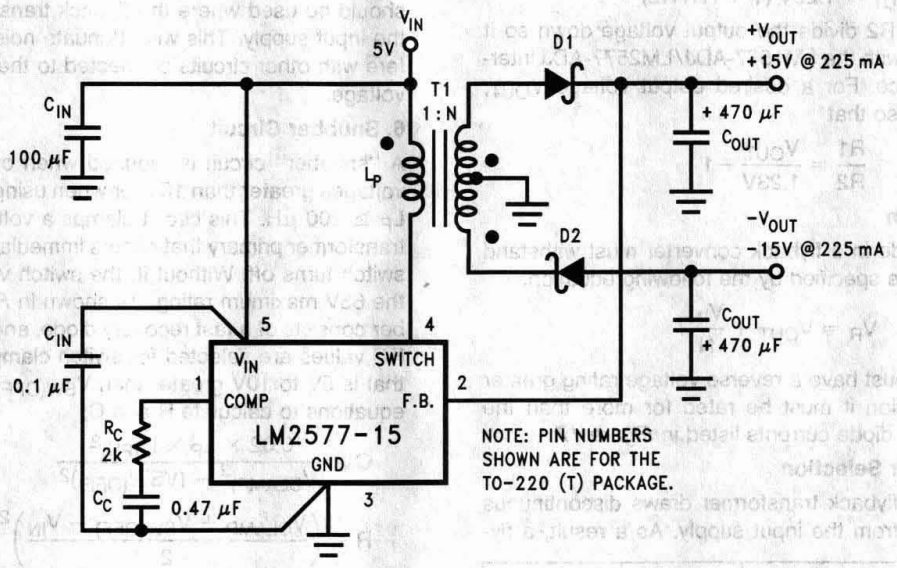
FIGURE 19. Snubber Circuit

Application Hints (Continued)

FLYBACK REGULATOR CIRCUIT EXAMPLE

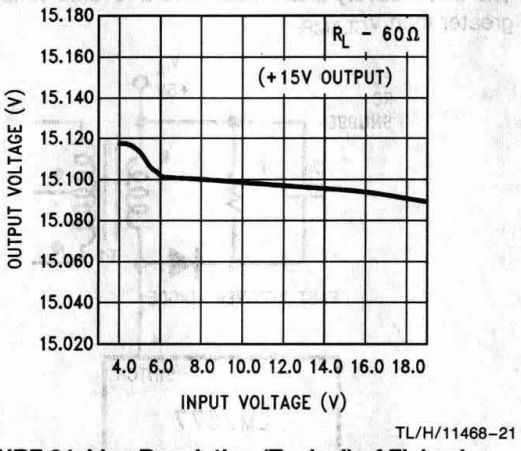
The circuit of *Figure 20* produces ±15V (at 225 mA each) from a single 5V input. The output regulation of this circuit is shown in *Figures 21* and *22*, while the load transient response is shown in *Figures 23* and *24*. Switching waveforms seen in this circuit are shown in *Figure 25*.



TL/H/11468–20

T1 = Pulse Engineering, PE-65300
D1, D2 = 1N5821

FIGURE 20. Flyback Regulator Easily Provides Dual Outputs



TL/H/11468–21

FIGURE 21. Line Regulation (Typical) of Flyback Regulator of *Figure 20*, +15V Output

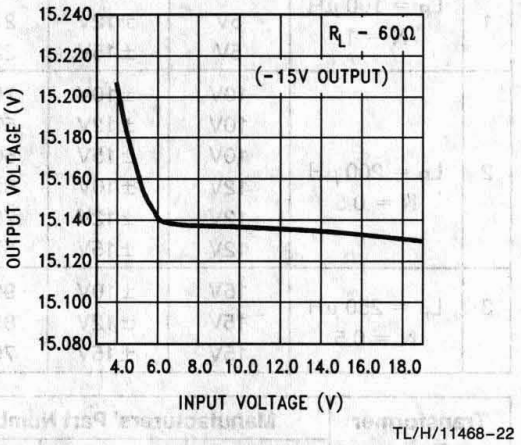


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FIGURE 22. Line Regulation (Typical) of Flyback Regulator of *Figure 20*, −15V Output

Application Hints (Continued)

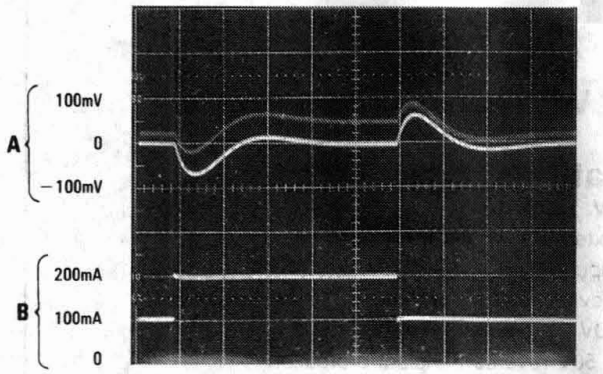

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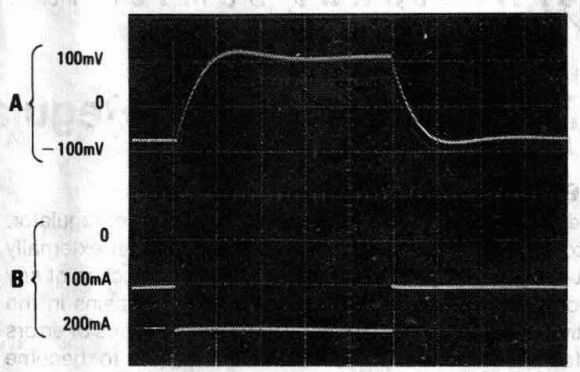
FIGURE 23. Load Transient Response of Flyback Regulator of *Figure 20*, +15V Output

A: Output Voltage Change, 100 mV/div
B: Output Current, 100 mA/div
Horizontal: 10 ms/div



TL/H/11468–24

FIGURE 24. Load Transient Response of Flyback Regulator of *Figure 20*, −15V Output

A: Output Voltage Change, 100 mV/div
B: Output Current, 100 mA/div
Horizontal: 10 ms/div

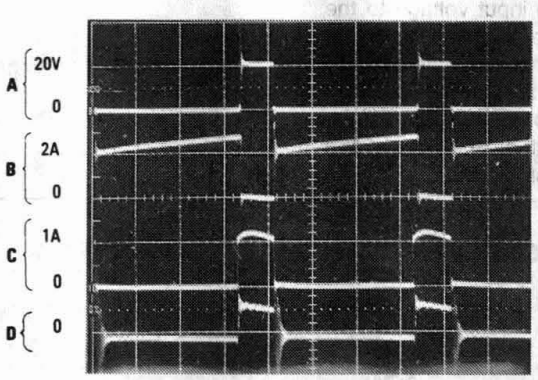


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FIGURE 25. Switching Waveforms of Flyback Regulator of *Figure 20*, Each Output Loaded with 60Ω

A: Switch pin voltage, 20 V/div
B: Primary current, 2 A/div
C: +15V Secondary current, 1 A/div
D: +15V Output ripple voltage, 100 mV/div
Horizontal: 5 μs/div

National Semiconductor

LM2925 Low Dropout Regulator with Delayed Reset

General Description

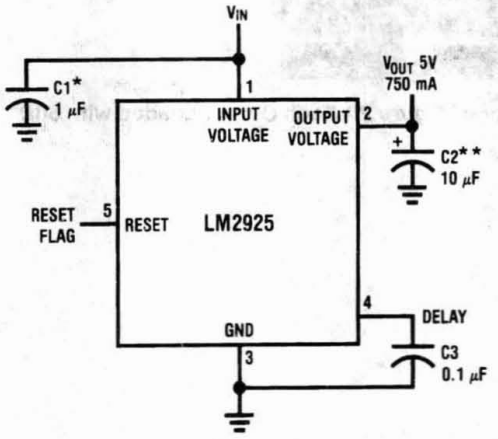
The LM2925 features a low dropout, high current regulator. Also included on-chip is a reset function with an externally set delay time. Upon power up, or after the detection of any error in the regulated output, the reset pin remains in the active low state for the duration of the delay. Types of errors detected include any that cause the output to become unregulated: low input voltage, thermal shutdown, short circuit, input transients, etc. No external pull-up resistor is necessary. The current charging the delay capacitor is very low, allowing long delay times.

Designed primarily for automotive applications, the LM2925 and all regulated circuitry are protected from reverse battery installations or two-battery jumps. During line transients, such as a load dump (60V) when the input voltage to the regulator can momentarily exceed the specified maximum operating voltage, the 0.75A regulator will automatically shut down to protect both internal circuits and the load. The LM2925 cannot be harmed by temporary mirror-image insertion. Familiar regulator features such as short circuit and thermal overload protection are also provided.

Features

- 5V, 750 mA output
- Externally set delay for reset
- Input-output differential less than 0.6V at 0.5A
- Reverse battery protection
- 60V load dump protection
- −50V reverse transient protection
- Short circuit protection
- Internal thermal overload protection
- Available in plastic TO-220
- Long delay times available
- P+ Product Enhancement tested

Typical Application Circuit



*Required if regulator is located far from power supply filter.

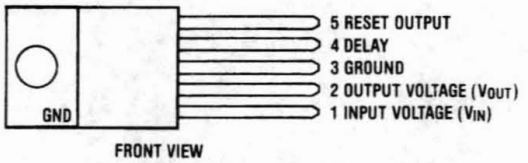
**C_{OUT} must be at least 10 μF to maintain stability. May be increased without bound to maintain regulation during transients. Locate as close as possible to the regulator. This capacitor must be rated over the same operating temperature range as the regulator. The equivalent series resistance (ESR) of this capacitor is critical; see curve.

TL/H/5268–1

FIGURE 1. Test and Application Circuit

Connection Diagram

TO-220 5-Lead



FRONT VIEW

TL/H/5268–2

Order Number LM2925T
See NS Package Number T05A

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Input Voltage	
Operating Range	26V
Overvoltage Protection	60V
Internal Power Dissipation (Note 1)	Internally Limited
Operating Temperature Range	−40°C to + 125°C
Maximum Junction Temperature	150°C
Storage Temperature Range	−65°C to + 150°C
Lead Temperature (Soldering, 10 seconds)	260°C

ESD rating is to be determined

Electrical Characteristics for V_{OUT}

V_{IN} = 14V, C2 = 10 μf, I_O = 500 mA, T_J = 25°C (Note 3) (unless otherwise specified)

Parameter	Conditions	Min	Typ	Max	Units
			Note 2		
Output Voltage	6V ≤ V_{IN} ≤ 26V, I_O ≤ 500 mA, −40°C ≤ T_J ≤ +125°C	4.75	5.00	5.25	V
Line Regulation	9V ≤ V_{IN} ≤ 16V, I_O = 5 mA 6V ≤ V_{IN} ≤ 26V, I_O = 5 mA		4 10	25 50	mV mV
Load Regulation	5 mA ≤ I_O ≤ 500 mA		10	50	mV
Output Impedance	500 mA_{DC} and 10 mArms, 100 Hz-10 kHz		200		mΩ
Quiescent Current	I_O ≤ 10 mA I_O = 500 mA I_O = 750 mA		3 40 90	 100	mA mA mA
Output Noise Voltage	10 Hz-100 kHz		100		μVrms
Long Term Stability			20		mV/1000 hr
Ripple Rejection	f_o = 120 Hz		66		dB
Dropout Voltage	I_O = 500 mA I_O = 750 mA		0.45 0.82	0.6	V V
Current Limit		0.75	1.2		A
Maximum Operational Input Voltage		26	31		V
Maximum Line Transient	V_O ≤ 5.5V	60	70		V
Reverse Polarity Input Voltage, DC	V_O ≥ − 0.6V, 10Ω Load	−15	−30		V
Reverse Polarity Input Voltage, Transient	1% Duty Cycle, τ ≤ 100 ms, 10Ω Load	−50	−80		V

Electrical Characteristics for Reset Output

V_{IN} = 14V, C3 = 0.1 μF, T_A = 25°C (Note 3) (unless otherwise specified)

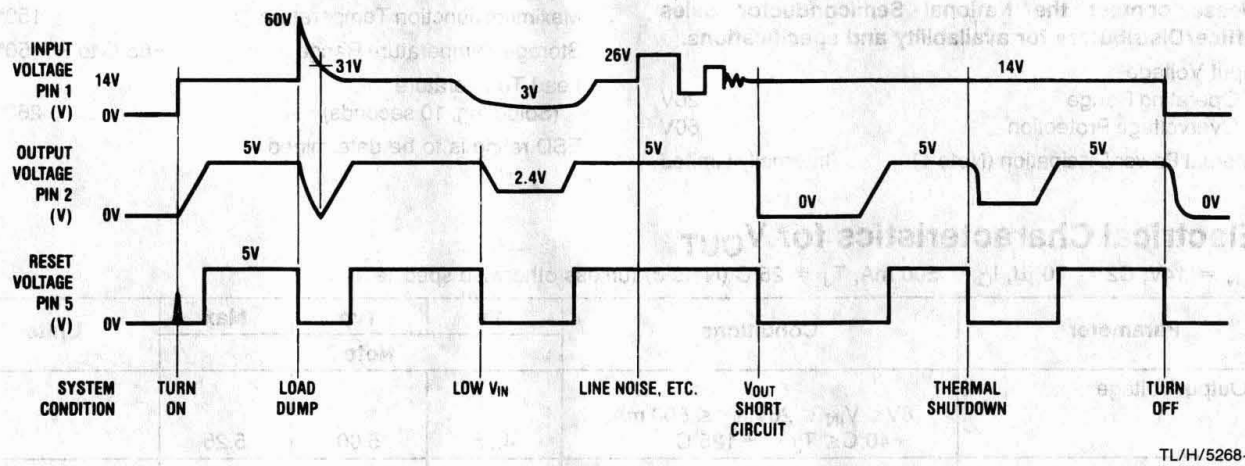
Parameter	Conditions	Min	Typ	Max	Units
			Note 2		
Reset Voltage Output Low Output High	 I_{SINK} = 1.6 mA, V_{IN} = 35V I_{SOURCE} = 0	 4.5	 0.3 5.0	 0.6 5.5	 V V
Reset Internal Pull-up Resistor			30		kΩ
Reset Output Current Limit	V_{RESET} = 1.2 V		5		mA
V_{OUT} Threshold			4.5		V
Delay Time	C_3 = .005 μF C_3 = 0.1 μF C_3 = 4.7 μF tantalum	 150	12 250 12	 300	ms ms s
Delay Current	Pin 4	1.2	1.95	2.5	μA

Note 1: Thermal resistance without a heat sink for junction to case temperature is 3°C/W (TO-220). Thermal resistance for TO-220 case to ambient temperature is 50°C/W.

Note 2: These parameters are guaranteed and 100% production tested.

Note 3: To ensure constant junction temperature, low duty cycle pulse testing is used.

Typical Circuit Waveforms

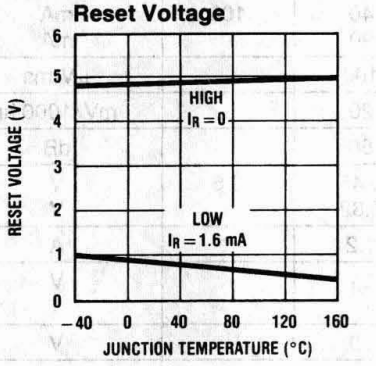


TL/H/5268–3

FIGURE 2

Typical Performance Characteristics

Reset Voltage



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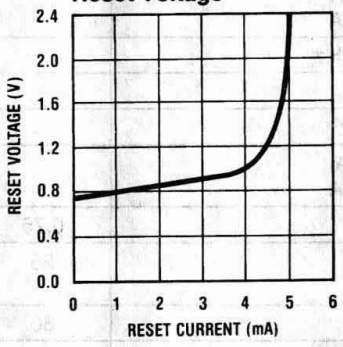
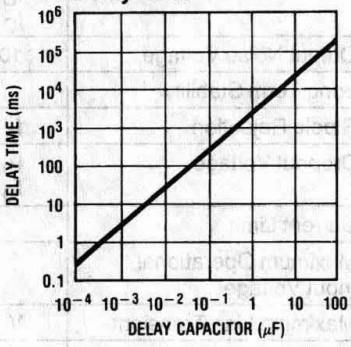
Reset Voltage



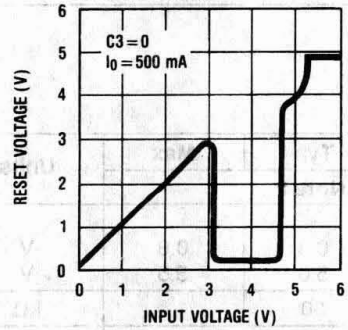
TL/H/5268–5

Delay Time



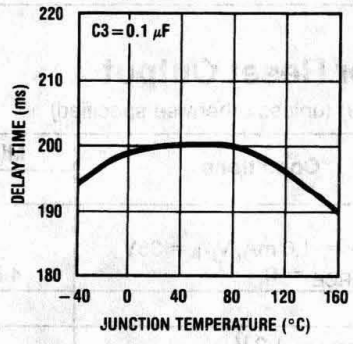
TL/H/5268–6

Reset Voltage on Power-up



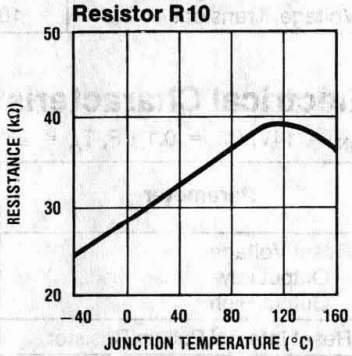
TL/H/5268–7

Delay Time



TL/H/5268–8

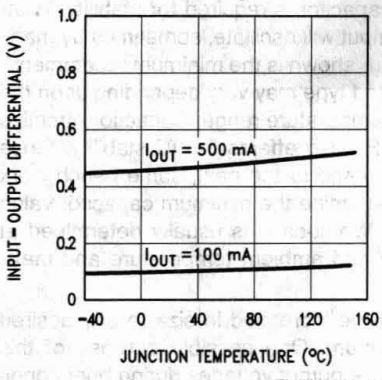
Reset Pull-up Resistor R10



TL/H/5268–9

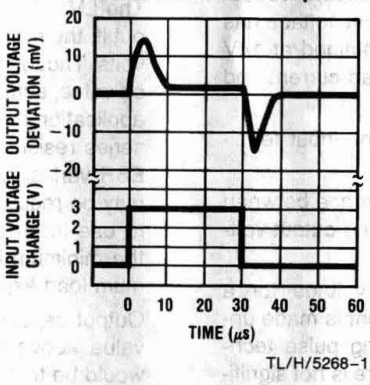
Typical Performance Characteristics (Continued)

Dropout Voltage



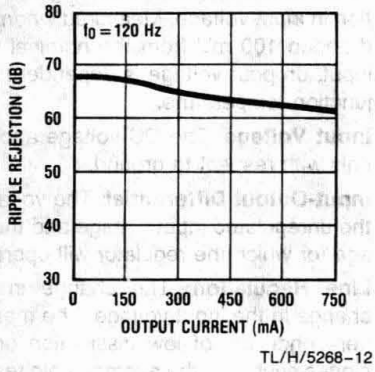
TL/H/5268–10

Line Transient Response



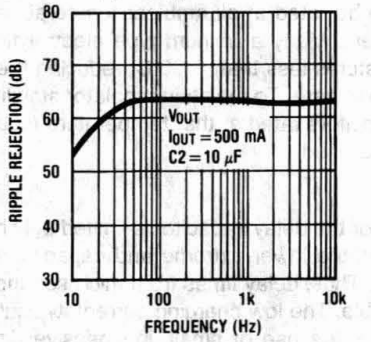
TL/H/5268–11

Ripple Rejection



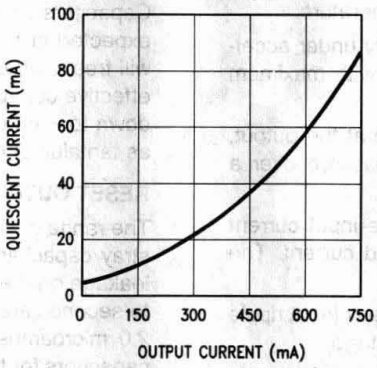
TL/H/5268–12

Ripple Rejection



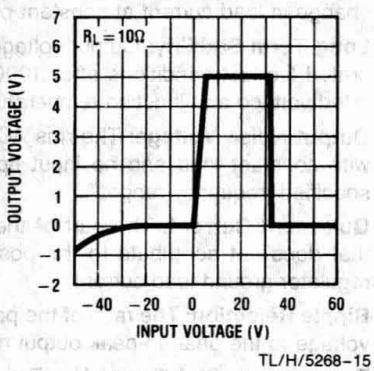
TL/H/5268–13

Quiescent Current



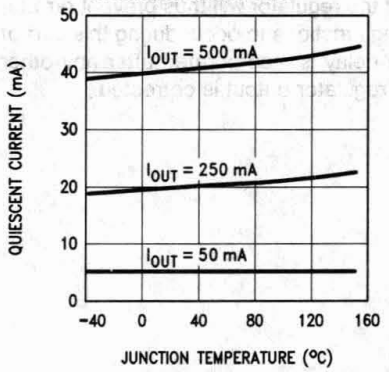
TL/H/5268–14

Output Voltage



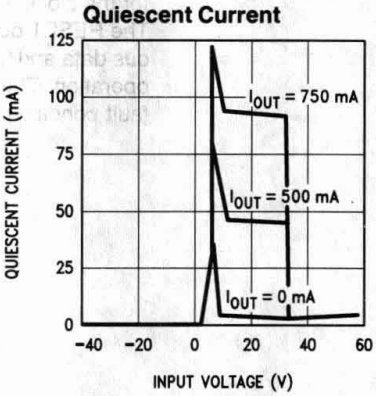
TL/H/5268–15

Quiescent Current



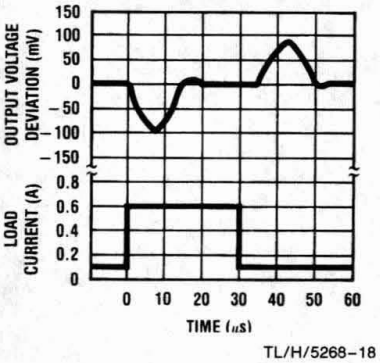
TL/H/5268–19

Quiescent Current



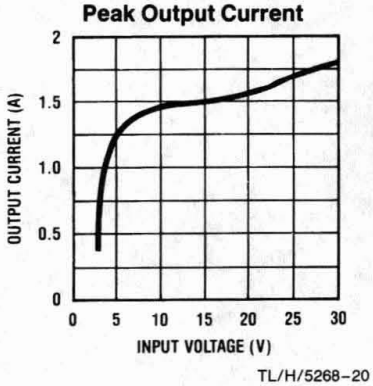
TL/H/5268–17

Load Transient Response



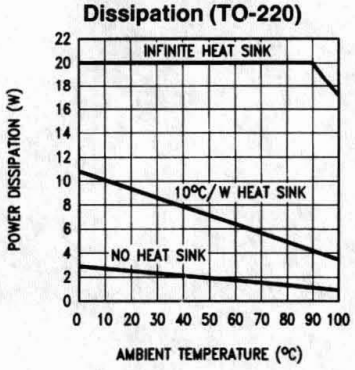
TL/H/5268–18

Peak Output Current



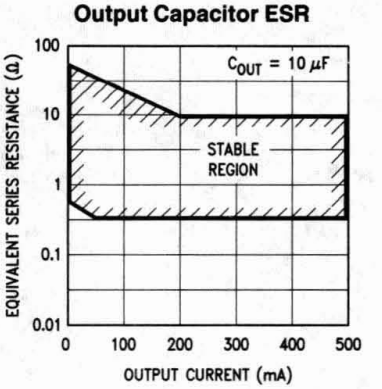
TL/H/5268–20

Maximum Power Dissipation (TO-220)



TL/H/5268–21

Output Capacitor ESR



TL/H/5268–22

3

Definition of Terms

Dropout Voltage: The input-output voltage differential at which the circuit ceases to regulate against further reduction in input voltage. Measured when the output voltage has dropped 100 mV from the nominal value obtained at 14V input, dropout voltage is dependent upon load current and junction temperature.

Input Voltage: The DC voltage applied to the input terminals with respect to ground.

Input-Output Differential: The voltage difference between the unregulated input voltage and the regulated output voltage for which the regulator will operate.

Line Regulation: The change in output voltage for a change in the input voltage. The measurement is made under conditions of low dissipation or by using pulse techniques such that the average chip temperature is not significantly affected.

Load Regulation: The change in output voltage for a change in load current at constant chip temperature.

Long Term Stability: Output voltage stability under accelerated life-test conditions after 1000 hours with maximum rated voltage and junction temperature.

Output Noise Voltage: The rms AC voltage at the output, with constant load and no input ripple, measured over a specified frequency range.

Quiescent Current: The part of the positive input current that does not contribute to the positive load current. The regulator ground lead current.

Ripple Rejection: The ratio of the peak-to-peak input ripple voltage to the peak-to-peak output ripple voltage.

Temperature Stability of V_O: The percentage change in ouput voltage for a thermal variation from room temperature to either temperature extreme.

Application Hints

EXTERNAL CAPACITORS

The LM2925 output capacitor is required for stability. Without it, the regulator output will oscillate, sometimes by many volts. Though the 10 μF shown is the minimum recommended value, actual size and type may vary depending upon the application load and temperature range. Capacitor effective series resistance (ESR) also effects the IC stability. Since ESR varies from one brand to the next, some bench work may be required to determine the minimum capacitor value to use in production. Worst-case is usually determined at the minimum junction and ambient temperature and maximum load expected.

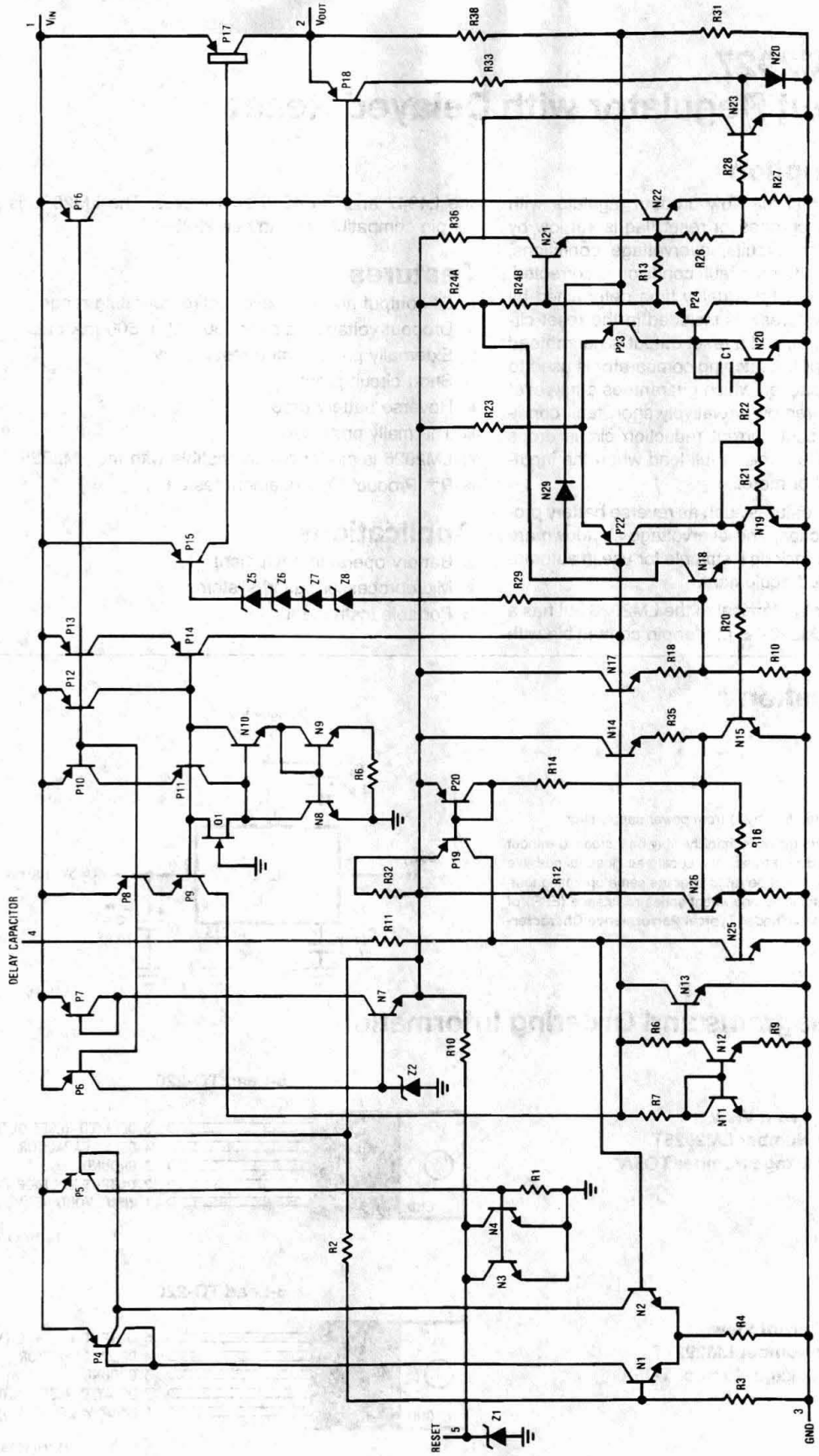
Output capacitors can be increased in size to any desired value above the minimum. One possible purpose of this would be to maintain the output voltages during brief conditions of negative input transients that might be characteristic of a particular system.

Capacitors must also be rated at all ambient temperatures expected in the system. Many aluminum type electrolytics will freeze at temperatures less than −30°C, reducing their effective capacitance to zero. To maintain regulator stability down to −40°C, capacitors rated at that temperature (such as tantalums) must be used.

RESET OUTPUT

The range of values for the delay capacitor is limited only by stray capacitances on the lower extreme and capacitance leakage on the other. Thus, delay times from microseconds to seconds are possible. The low charging current, typically 2.0 microamps, allows the use of small, inexpensive disc capacitors for the nominal range of 100 to 500 milliseconds. This is the time required in many microprocessor systems for the clock oscillator to stabilize when initially powered up. The RESET output of the regulator will thus prevent erroneous data and/or timing functions to occur during this part of operation. The same delay is incorporated after any other fault condition in the regulator output is corrected.

Circuit Schematic



TL/H/5268–23

FIGURE 3

National Semiconductor

LM2926/LM2927
Low Dropout Regulator with Delayed Reset

General Description

The LM2926 is a 5V, 500 mA, low dropout regulator with delayed reset. The microprocessor reset flag is set low by thermal shutdown, short circuits, overvoltage conditions, dropout, and power-up. After the fault condition is corrected, the reset flag remains low for a delay time determined by the delay capacitor. Hysteresis is included in the reset circuit to prevent oscillations, and a reset output is guaranteed down to 3.2V supply input. A latching comparator is used to discharge the delay capacitor, which guarantees a full reset pulse even when triggered by a relatively short fault condition. A patented quiescent current reduction circuit drops the ground pin current to 8 mA at full load when the input-output differential is 3V or more.

Familiar PNP regulator features such as reverse battery protection, transient protection, and overvoltage shutdown are included in the LM2926 making it suitable for use in automotive and battery operated equipment.

The LM2927 is electrically identical to the LM2926 but has a different pin-out. The LM2927 is pin-for-pin compatible with the L4947 and TLE4260 alternatives. The LM2926 is pin-for-pin compatible with the LM2925.

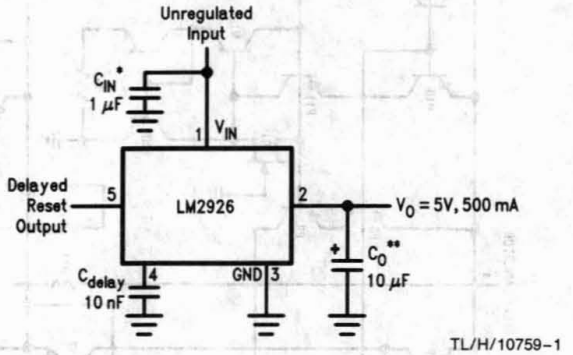
Features

- 5% output accuracy over entire operating range
- Dropout voltage typically 350 mV at 500 mA output
- Externally programmed reset delay
- Short circuit proof
- Reverse battery proof
- Thermally protected
- LM2926 is pin-for-pin compatible with the LM2925
- P+ Product Enhancement tested

Applications

- Battery operated equipment
- Microprocessor-based systems
- Portable instruments

Typical Application



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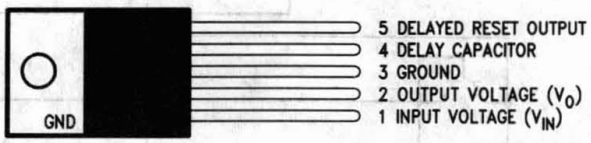
*Required if regulator is located far (>2") from power supply filter.

C_O must be at least 10 μF to maintain stability. May be increased without bound to maintain regulation during transients. Locate as close as possible to the regulator. This capacitor msut be rated over the same operating temperature range as the regulator. The equivalent series resistance (ESR) of this capacitor is critical; see curve under **Typical Performance Characteristics.

Connection Diagrams and Ordering Information

5-Lead TO-220

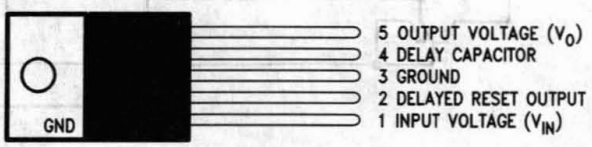
Front View
Order Number LM2926T
See NS Package Number TO5A



TL/H/10759–2

5-Lead TO-220

Front View
Order Number LM2927T
See NS Package Number TO5A



TL/H/10759–14

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Input Voltage	
Survival	
t = 100 ms	80V
t = 1 ms	−50V
Continuous	−18V to +26V
Reset Output Sink Current	10 mA
ESD Susceptibility (Note 2)	2 kV
Power Dissipation (Note 3)	Internally Limited
Junction Temperature (T_{JMAX})	150°C
Storage Temperature Range	−40°C to +150°C
Lead Temperature (Soldering, 10 sec.)	260°C

Operating Ratings (Note 1)

Junction Temperature Range (T_J)	−40°C to +125°C
Maximum Input Voltage	26V

Electrical Characteristics V_{IN} = 14.4V, C_O = 10 µF, −40°C ≤ T_J ≤ 125°C, unless otherwise specified.

Parameter	Conditions	Typ (Note 4)	Limit (Note 5)	Units (Limit)
REGULATOR OUTPUT				
Output Voltage	5 mA ≤ I_O ≤ 500 mA, T_J = 25°C	5	4.85 5.15	V (min) V (max)
	5 mA ≤ I_O ≤ 500 mA	5	4.75 5.25	V (min) V (max)
Line Regulation	I_O = 5 mA, 9V ≤ V_{IN} ≤ 16V	1	25	mV mV (max)
	I_O = 5 mA, 7V ≤ V_{IN} ≤ 26V	3	50	mV mV (max)
Load Regulation	5 mA ≤ I_O ≤ 500 mA	5	60	mV mV (max)
Quiescent Current	I_O = 5 mA	2	3	mA mA (max)
	I_O = 500 mA	8	30	mA mA (max)
Quiescent Current at Low V_{IN}	I_O = 5 mA, V_{IN} = 5V	3	10	mA mA (max)
	I_O = 500 mA, V_{IN} = 6V	25	60	mA mA (max)
Dropout Voltage (Note 6)	I_O = 5 mA, T_J = 25°C	60	200	mV mV (max)
	I_O = 5 mA		300	mV (max)
	I_O = 500 mA, T_J = 25°C	350	600	mV mV (max)
	I_O = 500 mA		700	mV (max)
Short Circuit Current	V_{IN} = 8V, R_L = 1Ω	2	800 3	mA (min) A A (max)
Ripple Rejection	f_{RIPPLE} = 120 Hz, V_{RIPPLE} = 1 Vrms, I_O = 50 mA		60	dB (min)
Output Impedance	I_O = 50 mAdc and 10 mArms @ 1 kHz	100		mΩ
Output Noise	10 Hz to 100 kHz, I_O = 50 mA	1		mVrms
Long Term Stability		20		mV/1000 Hr
Maximum Operational Input Voltage	Continuous		26	V (min)

3

Electrical Characteristics

V_{IN} = 14.4V, C_O = 10 μF, −40°C ≤ T_J ≤ 125°C, unless otherwise specified (Continued)

Parameter	Conditions	Typ (Note 4)	Limit (Note 5)	Units (Limit)
REGULATOR OUTPUT (Continued)				
Peak Transient Input Voltage	$V_O \leq 7V$, $R_L = 100\Omega$, $t_f = 100$ ms		80	V (min)
Reverse DC Input Voltage	$V_O \geq -0.6V$, $R_L = 100\Omega$		−18	V (min)
Reverse Transient Input Voltage	$t_r = 1$ ms, $R_L = 100\Omega$		−50	V (min)
RESET OUTPUT				
Threshold	ΔV_O Required for Reset Condition (Note 7)		−80	mV (min)
		−250		mV
			−400	mV (max)
Output Low Voltage	$I_{SINK} = 1.6$ mA, $V_{IN} = 3.2V$	0.15		
			0.4	V (max)
Internal Pull-Up Resistance		30		kΩ
Delay Time	$C_{DELAY} = 10$ nF (See Timing Curve)	19		ms
Minimum Operational V_{IN} on Power Up	Delayed Reset Output ≤ 0.8V,	2.2		V
	$I_{SINK} = 1.6$ mA, $R_L = 100\Omega$		3.2	V (min)
Minimum Operational V_O on Power Down	Delay Reset Output ≤ 0.8V,	0.7		V
	$I_{SINK} = 10$ μA, $V_{IN} = 0V$			
DELAY CAPACITOR PIN				
Threshold Difference (ΔV_{DELAY})	Change in Delay Capacitor Voltage Required for Reset Output to Return High		3.5	V (min)
		3.75		V
			4.1	V (max)
Charging Current (I_{DELAY})			1.0	μA (min)
		2.0		μA
			3.0	μA (max)

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. **Operating Ratings** indicate conditions for which the device is intended to be functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the **Electrical Characteristics.**

Note 2: Human body model; 100 pF discharged through a 1.5 kΩ resistor.

Note 3: The maximum power dissipation is a function of T_{JMAX}, and θ_{JA}, and T_A, and is limited by thermal shutdown. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{JMAX}-T_A)/\theta_{JA}$. If this dissipation is exceeded, the die temperature will rise above 150°C and the device will go into thermal shutdown. For the LM2926 and LM2927, the junction-to-ambient thermal resistance is 53°C/W, and the junction-to-case thermal resistance is 3°C/W.

Note 4: Typicals are at T_J = 25°C and represent the most likely parametric norm.

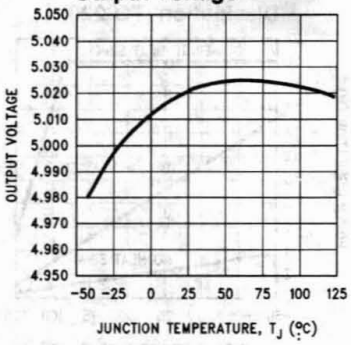
Note 5: Limits are 100% guaranteed by production testing.

Note 6: Dropout voltage is the input-output differential at which the circuit ceases to regulate against any further reduction in input voltage. Dropout voltage is measured when the output voltage (V_O) has dropped 100 mV from the nominal value measured at V_{IN} = 14.4V.

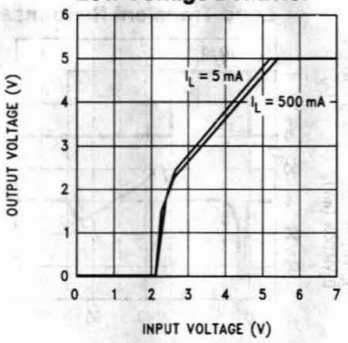
Note 7: The reset flag is set LOW when the output voltage has dropped an amount, ΔV_O, from the nominal value measured at V_{IN} = 14.4V.

Typical Performance Characteristics

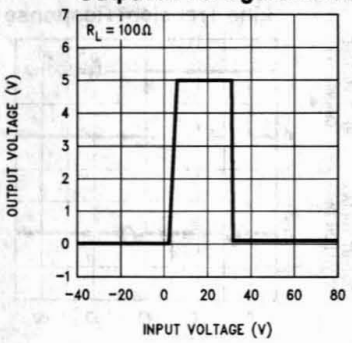
Output Voltage



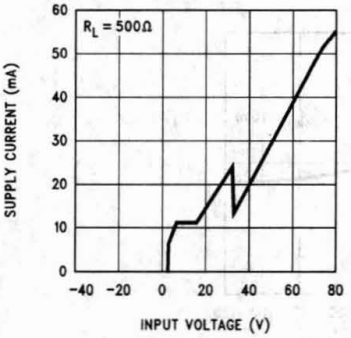
Low Voltage Behavior



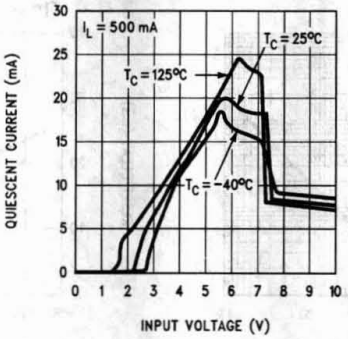
Output at Voltage Extremes



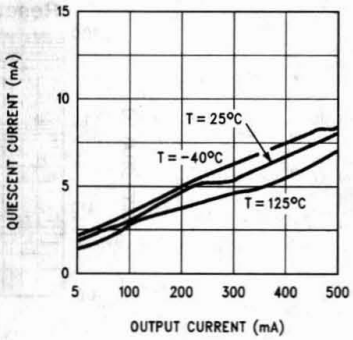
Supply Current



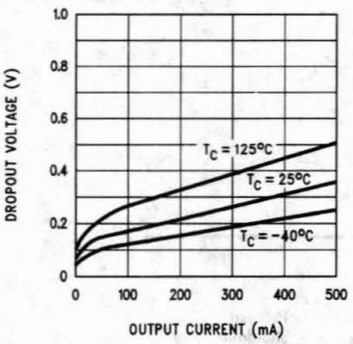
Quiescent Current



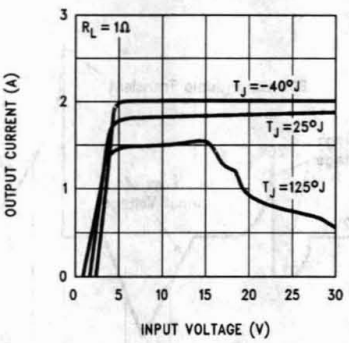
Quiescent Current



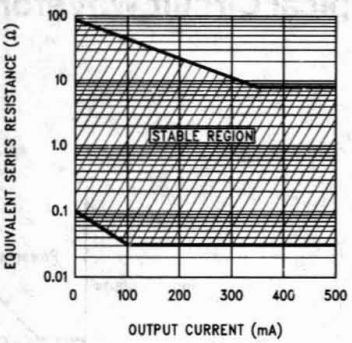
Dropout Voltage



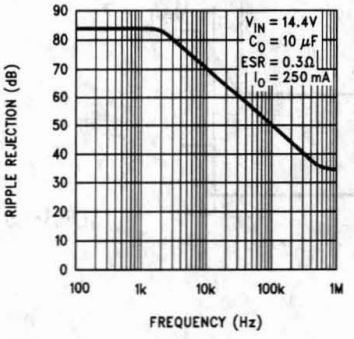
Output Current Limit



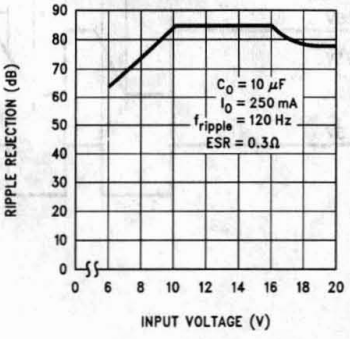
Output Capacitor ESR



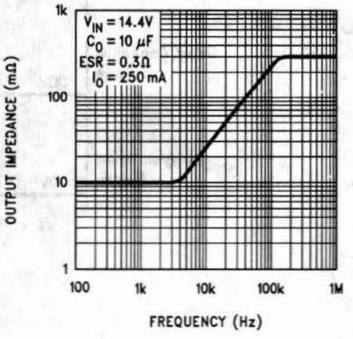
Ripple Rejection



Ripple Rejection



Output Impedance



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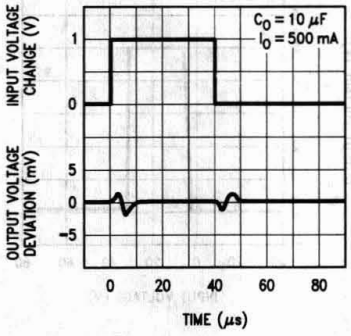
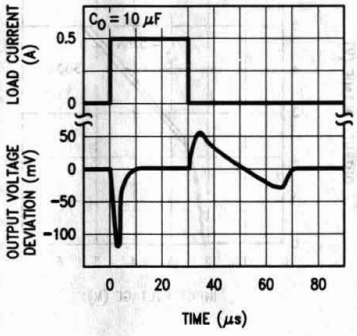
Typical Performance Characteristics (Continued)

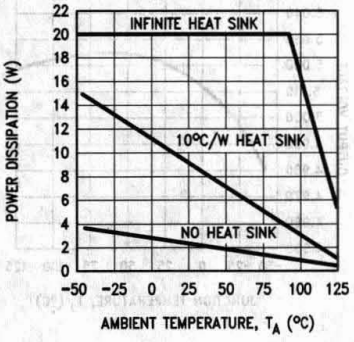
Line Transient Response



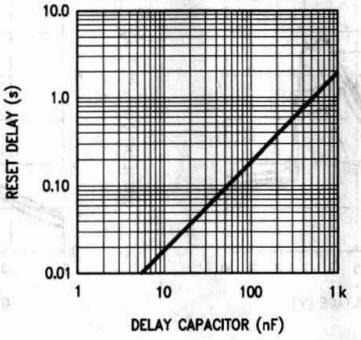
Load Transient Response



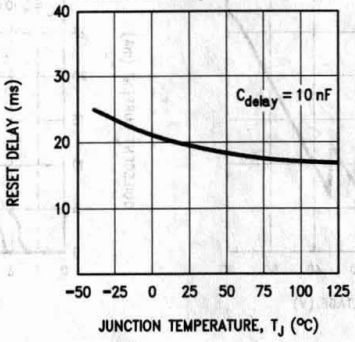
Maximum Power Dissipation (TO-220)



Reset Delay

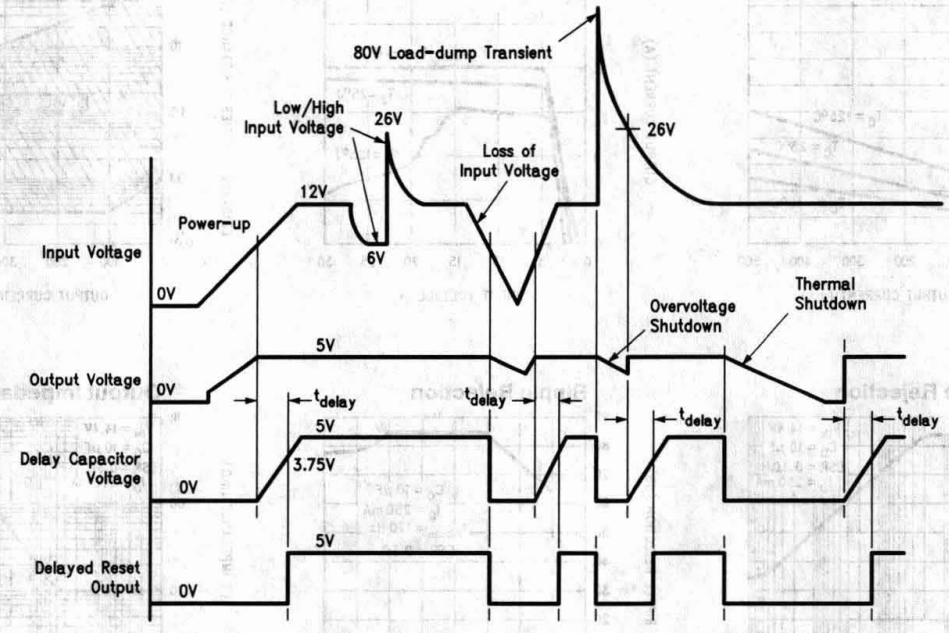


Reset Delay



TL/H/10759–4

Typical Circuit Waveforms



TL/H/10759–5

Applications Information

EXTERNAL CAPACITORS

The LM2926/7 output capacitor is required for stability. Without it, the regulator output will oscillate at amplitudes as high as several volts peak-to-peak at frequencies up to 500 kHz. Although 10 μF is the minimum recommended value, the actual size and type may vary depending upon the application load and temperature range. Capacitor equivalent series resistance (ESR) also affects stability. The region of stable operation is shown in the **Typical Performance Characteristics** (Output Capacitor ESR curve).

Output capacitors can be increased in size to any desired value above 10 μF. One possible purpose of this would be to maintain the output voltage during brief conditions of input transients that might be characteristic of a particular system.

Capacitors must also be rated at all ambient temperatures expected in the system. Many aluminum electrolytics freeze at temperatures below −30°C, reducing their effective capacitance to zero. To maintain regulator stability down to −40°C, capacitors rated at that temperature (such as tantalums) must be used.

DELAYED RESET

The delayed reset output is designed to hold a microprocessor in a reset state on system power-up for a programmable time interval to allow the system clock and other powered circuitry to stabilize. A full reset interval is also generated whenever the output voltage falls out of regulation. The circuit is tripped whenever the output voltage of the regulator is out of regulation by the Reset Threshold value. This can be caused by low input voltages, over current conditions, over-voltage shutdown, thermal shutdown, and by both power-up and power-down sequences. When the reset circuit detects one of these conditions, the delay capacitor is discharged by an SCR and held in a discharged state by a saturated NPN switch. As long as the delay capacitor is held low, the reset output is also held low. Because of the action of the SCR, the reset output cannot glitch on noise or transient fault conditions. A full reset pulse is obtained for any fault condition that trips the reset circuit.

When the output regains regulation, the SCR is switched off and a small current (I_{DELAY} = 2 μA) begins charging the delay capacitor. When the capacitor voltage increases 3.75V (ΔV_{DELAY}) from its discharged value, the reset output is again set HIGH. The delay time is calculated by:

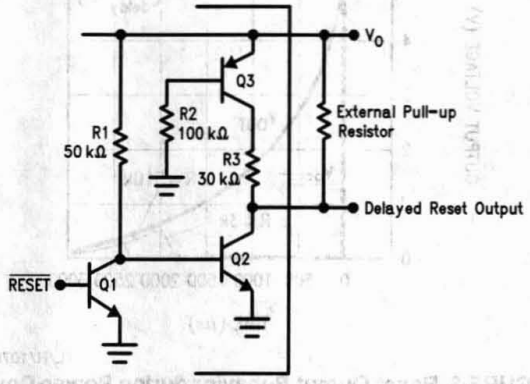
$$\text{delay time} = \frac{C_{DELAY}\,\Delta V_{DELAY}}{I_{DELAY}} \qquad (1)$$

or

$$\text{delay time} \approx 1.9 \times 10^6\, C_{DELAY} \qquad (2)$$

The constant, 1.9×10^6, has a ±20% tolerance from device to device. The total delay time error budget is the sum of the 20% device tolerance and the tolerance of the external capacitor. For a 20% timing capacitor tolerance, the worst case total timing variation would amount to ±40%, or a ratio of 2.33:1. In most applications the minimum expected reset pulse is of interest. This occurs with minimum C_{DELAY}, minimum ΔV_{DELAY}, and maximum I_{DELAY}. ΔV_{DELAY} and I_{DELAY} are fully specified in the **Electrical Characteristics.** Graphs showing the relationship between delay time and both temperature and C_{DELAY} are shown in the **Typical Performance Characteristics.**

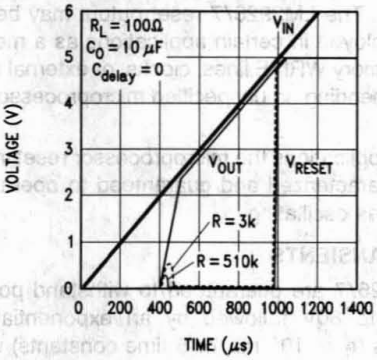
As shown in *Figure 1,* the delayed reset output is pulled low by an NPN transistor (Q2), and pulled high to V_O by an internal 30 kΩ resistor (R3) and PNP transistor (Q3). The reset output will operate when V_O is sufficient to bias Q2 (0.7V or more). At lower voltages the reset output will be in a high impedance condition. Because of differences in the V_{BE} of Q2 and Q3 and the values of R1 and R2, Q2 is guaranteed by design to bias *before* Q3, providing a smooth transition from the high impedance state when V_O < 0.7V, to the active low state when V_O > 0.7V.



TL/H/10759–6

FIGURE 1. Delay Reset Output

The static reset characteristics are shown in *Figure 2.* This shows the relationship between the input voltage, the regultor output and reset output. Plots are shown for various external pull-up resistors ranging in value from 3 kΩ to an open circuit. Any external pull-up resistance causes the reset output to follow the regulator output until Q2 is biased ON. C_{DELAY} has no effect on this characteristic.



TL/H/10759–7

FIGURE 2. Reset Output Behavior during Power-Up

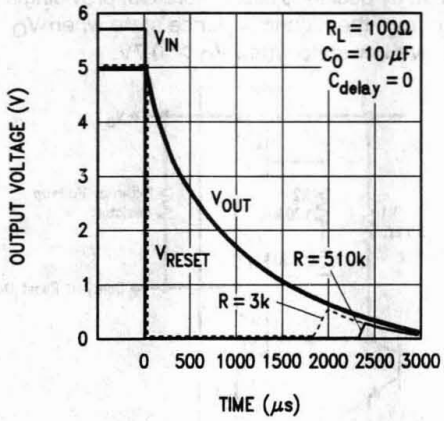
Figure 2 is useful for determing reset performance at any particular input voltage. Dynamic performance at power-up will closely follow the characteristics illustrated in *Figure 2,* except for the delay added by C_{DELAY} when V_O reaches 5V.

The dynamic reset characteristics at power-down are illustrated by the curve shown in *Figure 3.* At time t = 0 the input voltage is instantaneously brought to 0V, leaving the output powered by C_O. As the voltage on C_O decays (discharged by a 100Ω load resistor), the reset output is held low. As V_O drops below 0.7V, the reset rises up slightly should there be any external pull-up resistance. With no external resistance, the reset line stays low throughout the entire power down cycle. If the input voltage does not fall instantaneously, the reset signal will tend to follow the performance characteristics shown in *Figure 2.*

Applications Information (Continued)

SYSTEM DESIGN CONSIDERATIONS

Many microprocessors are specified for operation at 5V ±10%, although they often continue operating well outside this range. Others, such as certain members of the COPS family of microcontrollers, are specified for operation as low as 2.4V.



TL/H/10759–8

FIGURE 3. Reset Output Behavior during Power-Down

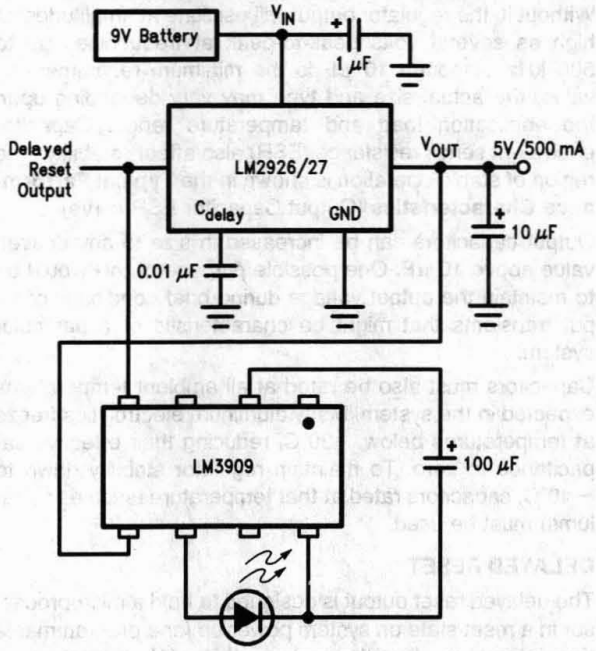
Of particular concern is low voltage operation, which occurs in battery operated systems when the battery reaches the end of its discharge cycle. Under this condition, when the supply voltage is outside the guaranteed operating range, the clock may continue to run and the microprocessor will attempt to execute instructions. If the supply voltage is outside the guaranteed operating range, the instructions may not execute properly and a hardware reset such as is supplied by the LM 2926/7 may fail to bring the processor under control. The LM2926/7 reset output may be more efficiently employed in certain applications as a means of defeating memory WRITE lines, clocks, or external loads, rather than depending on unspecified microprocessor operating conditions.

In critical applications the microprocessor reset input should be fully characterized and guaranteed to operate until the clock ceases oscillating.

INPUT TRANSIENTS

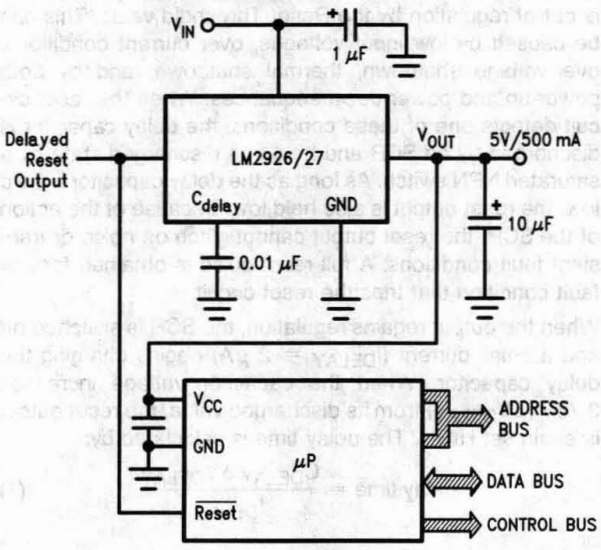
The LM2926/7 are guaranteed to withstand positive input transients to 80V followed by an exponential decay of τ = 20 ms (t_f = 100 ms, or 5 time constants) while maintaining an output of less than 7V. The regulator remains operational to 26 V_{DC}, and shuts down if this value is exceeded.

Battery Powered Regulator with Flashing LED for Low Battery Indication



TL/H/10759–9

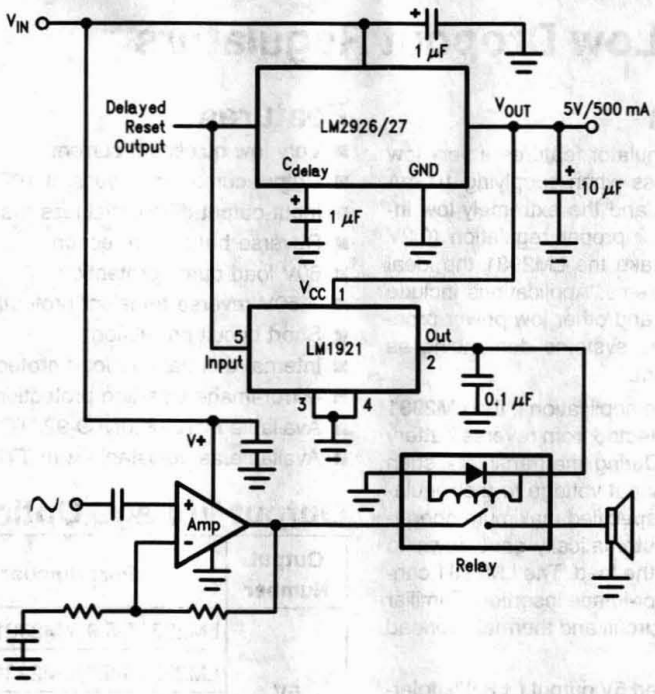
General Microprocessor Configuration



TL/H/10759–10

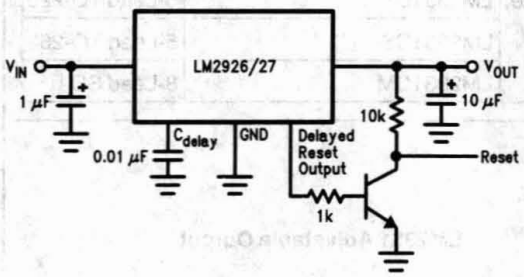
Applications Information (Continued)

Using the Reset to De-Activate Power Loads. The LM1921 is a Fully Protected 1 Amp High-Side Driver.



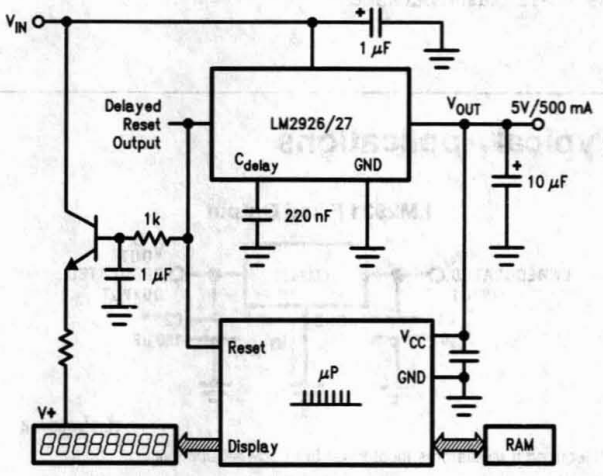
TL/H/10759–11

Generating an Active High Reset Signal



TL/H/10759–12

Using the Reset to Ensure an Accurate Display on Power-Up or Power-Down



TL/H/10759–13

3

National Semiconductor

LM2931 Series Low Dropout Regulators

General Description

The LM2931 positive voltage regulator features a very low quiescent current of 1 mA or less when supplying 10 mA loads. This unique characteristic and the extremely low input-output differential required for proper regulation (0.2V for output currents of 10 mA) make the LM2931 the ideal regulator for standby power systems. Applications include memory standby circuits, CMOS and other low power processor power supplies as well as systems demanding as much as 100 mA of output current.

Designed originally for automotive applications, the LM2931 and all regulated circuitry are protected from reverse battery installations or 2 battery jumps. During line transients, such as a load dump (60V) when the input voltage to the regulator can momentarily exceed the specified maximum operating voltage, the regulator will automatically shut down to protect both internal circuits and the load. The LM2931 cannot be harmed by temporary mirror-image insertion. Familiar regulator features such as short circuit and thermal overload protection are also provided.

The LM2931 family includes a fixed 5V output (±3.8% tolerance for A grade) or an adjustable output with ON/OFF pin. Both versions are available in a TO-220 power package, TO-263 surface mount package, and an 8-lead surface mount package. The fixed output version is also available in the TO-92 plastic package.

Features

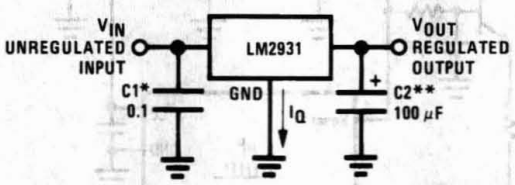
- Very low quiescent current
- Output current in excess of 100 mA
- Input-output differential less than 0.6V
- Reverse battery protection
- 60V load dump protection
- −50V reverse transient protection
- Short circuit protection
- Internal thermal overload protection
- Mirror-image insertion protection
- Available in TO-220, TO-92, TO-263 or SO-8 packages
- Available as adjustable with TTL compatible switch

Output Voltage Options

Output Number	Part Number	Package Type
5V	LM2931T-5.0, LM2931AT-5.0	3-Lead TO-220
	LM2931S-5.0, LM2931AS-5.0	3-Lead TO-263
	LM2931Z-5.0, LM2931AZ-5.0	TO-92
	LM2931M-5.0, LM2931AM-5.0	8-Lead SO
Adjustable, 3V to 24V	LM2931CT	5-Lead TO-220
	LM2931CS	5-Lead TO-263
	LM2931CM	8-Lead SO

Typical Applications

LM2931 Fixed Output

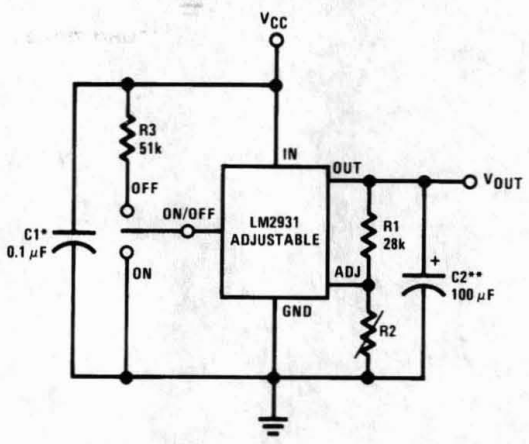


TL/H/5254–4

*Required if regulator is located far from power supply filter.

**C2 must be at least 100 µF to maintain stability. May be increased without bound to maintain regulation during transients. Locate as close as possible to the regulator. This capacitor must be rated over the same operating temperature range as the regulator. The equivalent series resistance (ESR) of this capacitor is critical; see curve.

LM2931 Adjustable Output



TL/H/5254–5

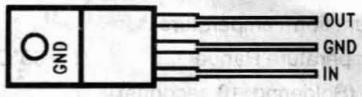
$$V_{OUT} = \text{Reference Voltage} \times \frac{R1 + R2}{R1}$$

Note: Using 27k for R1 will automatically compensate for errors in V_{OUT} due to the input bias current of the ADJ pin (approximately 1 µA).

Connection Diagrams and Ordering Information

FIXED 5V OUTPUT

TO-220 3-Lead Power Package

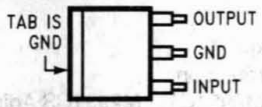


TL/H/5254–6

Front View

Order Number LM2931T-5.0 or LM2931AT-5.0
See NS Package Number T03B

TO-263 Surface-Mount Package



TL/H/5254–11

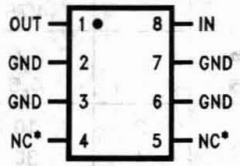
Top View

TL/H/5254–12

Side View

Order Number LM2931S-5.0 or LM2931AS-5.0
See NS Package Number TS3B

8-Pin Surface Mount



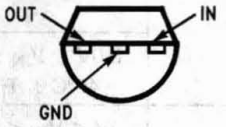
TL/H/5254–7

*NC = Not internally connected

Top View

Order Number LM2931M-5.0 or LM2931AM-5.0
See NS Package Number M08A

TO-92 Plastic Package



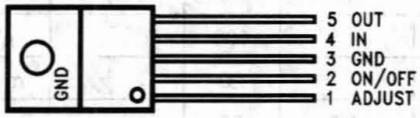
TL/H/5254–8

Bottom View

Order Number LM2931Z-5.0 or LM2931AZ-5.0
See NS Package Number Z03A

ADJUSTABLE OUTPUT VOLTAGE

TO-220 5-Lead Power Package

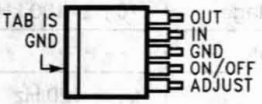


TL/H/5254–9

Front View

Order Number LM2931CT
See NS Package Number T05A

TO-263
5-Lead Surface-Mount Package



TL/H/5254–13

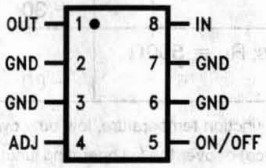
Top View

TL/H/5254–14

Side View

Order Number LM2931CS
See NS Package Number TS5B

8-Pin Surface Mount



TL/H/5254–10

Top View

Order Number LM2931CM
See NS Package Number M08A

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Input Voltage	
Operating Range	26V
Overvoltage Protection	
LM2931A, LM2931CT, LM2931CS Adjustable	60V
LM2931	50V
Internal Power Dissipation (Notes 1 and 3)	Internally Limited
Operating Ambient Temperature Range	−40°C to +85°C
Maximum Junction Temperature	125°C
Storage Temperature Range	−65°C to +150°C
Lead Temp. (Soldering, 10 seconds)	230°C
ESD Tolerance (Note 4)	2000V

Electrical Characteristics for Fixed 5V Version

V_{IN} = 14V, I_O = 10 mA, T_J = 25°C, C2 = 100 μF (unless otherwise specified) (Note 1)

Parameter	Conditions	LM2931A-5.0		LM2931-5.0		Units Limit
		Typ	Limit (Note 2)	Typ	Limit (Note 2)	
Output Voltage		5	5.19 4.81		5.25 4.75	V_{MAX} V_{MIN}
	6.0V ≤ V_{IN} ≤ 26V, I_O = 100 mA −40°C ≤ T_j ≤ 125°C		**5.25** **4.75**		**5.5** **4.5**	V_{MAX} V_{MIN}
Line Regulation	9V ≤ V_{IN} ≤ 16V 6V ≤ V_{IN} ≤ 26V	2 4	10 30	2 4	10 30	mV_{MAX} mV_{MAX}
Load Regulation	5 mA ≤ I_O ≤ 100 mA	14	50	14	50	mV_{MAX}
Output Impedance	100 mA_{DC} and 10 mA_{rms}, 100 Hz–10 kHz	200		200		$m\Omega_{MAX}$
Quiescent Current	I_O ≤ 10 mA, 6V ≤ V_{IN} ≤ 26V −40°C ≤ T_j ≤ 125°C	0.4	**1.0**	0.4	**1.0**	mA_{MAX}
	I_O = 100 mA, V_{IN} = 14V, T_j = 25°C	15	30 5	15		mA_{MAX} mA_{MIN}
Output Noise Voltage	10 Hz–100 kHz, C_{OUT} = 100 μF	500		500		$\mu V_{rms_{MAX}}$
Long Term Stability		20		20		mV/1000 hr
Ripple Rejection	f_O = 120 Hz	80	**55**	80		dB_{MIN}
Dropout Voltage	I_O = 10 mA I_O = 100 mA	0.05 0.3	0.2 0.6	0.05 0.3	0.2 0.6	V_{MAX} V_{MAX}
Maximum Operational Input Voltage		33	 26	33	 26	V_{MAX} V_{MIN}
Maximum Line Transient	R_L = 500Ω, V_O ≤ 5.5V, T = 1 ms, τ ≤ 100 ms	70	60	70	50	V_{MIN}
Reverse Polarity Input Voltage, DC	V_O ≥ −0.3V, R_L = 500Ω	−30	−15	−30	−15	V_{MIN}
Reverse Polarity Input Voltage, Transient	T = 1 ms, τ ≤ 100 ms, R_L = 500Ω	−80	−50	−80	−50	V_{MIN}

Note 1: See circuit in Typical Applications. To ensure constant junction temperature, low duty cycle pulse testing is used.

Note 2: All limits are guaranteed for T_J = 25°C (standard type face) or over the full operating junction temperature range of −40°C to +125°C **(bold type face).**

Note 3: The maximum power dissipation is a function of maximum junction temperature T_{Jmax}, total thermal resistance θ_{JA}, and ambient temperature T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{Jmax} - T_A)/\theta_{JA}$. If this dissipation is exceeded, the die temperature will rise above 150°C and the LM2931 will go into thermal shutdown. For the LM2931 in the TO-92 package, θ_{JA} is 195°C/W; in the SO-8 package, θ_{JA} is 160°C/W, and in the TO-220 package, θ_{JA} is 50°C/W; and in the TO-263 package, θ_{JA} is 73°C/W. If the TO-220 package is used with a heat sink, θ_{JA} is the sum of the package thermal resistance junction-to-case of 3°C/W and the thermal resistance added by the heat sink and thermal interface.

If the TO-263 package is used, the thermal resistance can be reduced by increasing the P.C. board copper area thermally connected to the package: Using 0.5 square inches of copper area, θ_{JA} is 50°C/W; with 1 square inch of copper area, θ_{JA} is 37°C/W; and with 1.6 or more square inches of copper area, θ_{JA} is 32°C/W.

Note 4: Human body model, 100 pF discharged through 1.5 kΩ.

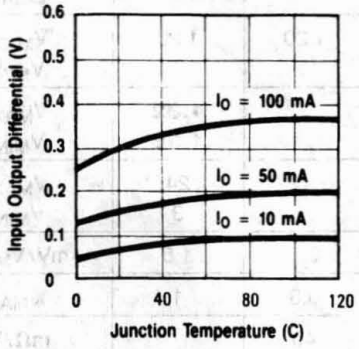
Electrical Characteristics for Adjustable Version

V_{IN} = 14V, V_{OUT} = 3V, I_O = 10 mA, T_J = 25°C, R1 = 27k, C2 = 100 μF (unless otherwise specified) (Note 1)

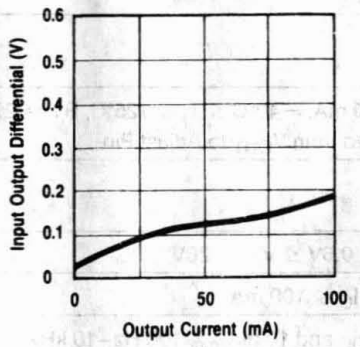
Parameter	Conditions	Typ	Limit	Units Limit
Reference Voltage		1.20	1.26 1.14	V_{MAX} V_{MIN}
	$I_O \leq 100$ mA, $-40°C \leq T_j \leq 125°C$, R1 = 27k Measured from V_{OUT} to Adjust Pin		**1.32** **1.08**	V_{MAX} V_{MIN}
Output Voltage Range			24 3	V_{MAX} V_{MIN}
Line Regulation	$V_{OUT} + 0.6V \leq V_{IN} \leq 26V$	0.2	1.5	mV/V_{MAX}
Load Regulation	5 mA $\leq I_O \leq$ 100 mA	0.3	1	$\%_{MAX}$
Output Impedance	100 mA_{DC} and 10 mA_{rms}, 100 Hz–10 kHz	40		mΩ/V
Quiescent Current	I_O = 10 mA I_O = 100 mA During Shutdown R_L = 500Ω	0.4 15 0.8	1 1	mA_{MAX} mA mA_{MAX}
Output Noise Voltage	10 Hz–100 kHz	100		$\mu V_{rms}/V$
Long Term Stability		0.4		%/1000 hr
Ripple Rejection	f_O = 120 Hz	0.02		%/V
Dropout Voltage	$I_O \leq$ 10 mA I_O = 100 mA	0.05 0.3	0.2 0.6	V_{MAX} V_{MAX}
Maximum Operational Input Voltage		33	26	V_{MIN}
Maximum Line Transient	I_O = 10 mA, Reference Voltage ≤ 1.5V T = 1 ms, $\tau \leq$ 100 ms	70	60	V_{MIN}
Reverse Polarity Input Voltage, DC	$V_O \geq -0.3V$, R_L = 500Ω	−30	−15	V_{MIN}
Reverse Polarity Input Voltage, Transient	T = 1 ms, $\tau \leq$ 100 ms, R_L = 500Ω	−80	−50	V_{MIN}
On/Off Threshold Voltage On Off	V_O=3V	 2.0 2.2	 1.2 3.25	 V_{MAX} V_{MIN}
On/Off Threshold Current		20	50	μA_{MAX}

Typical Performance Characteristics

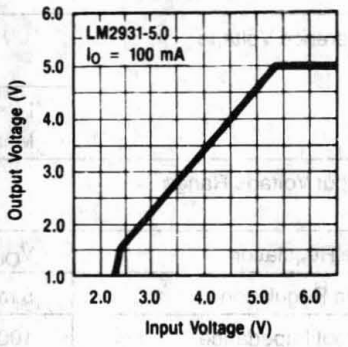
Dropout Voltage



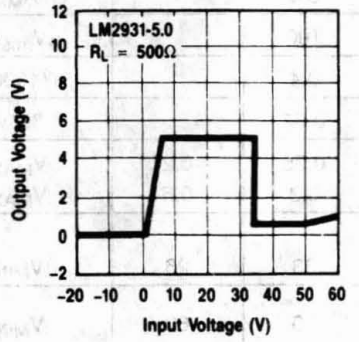
Dropout Voltage



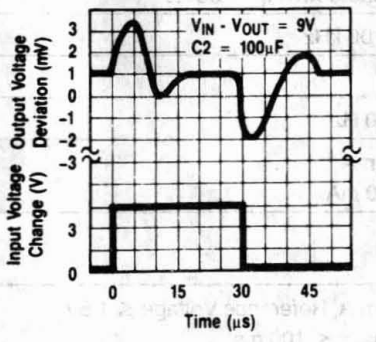
Low Voltage Behavior



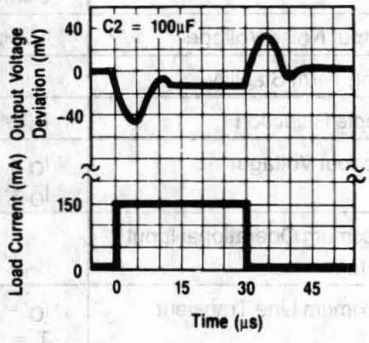
Output at Voltage Extremes



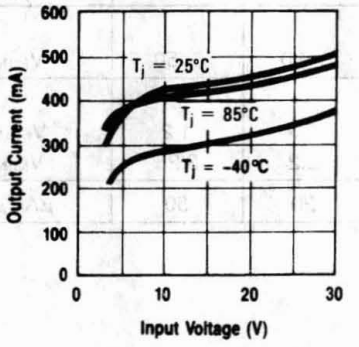
Line Transient Response



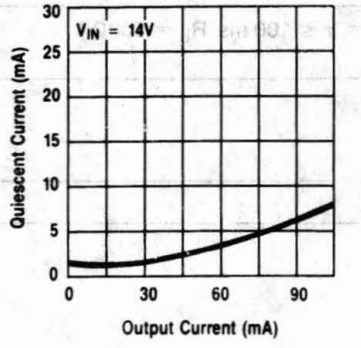
Load Transient Response



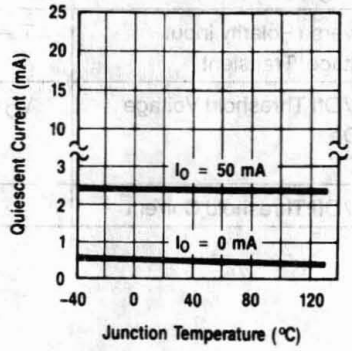
Peak Output Current



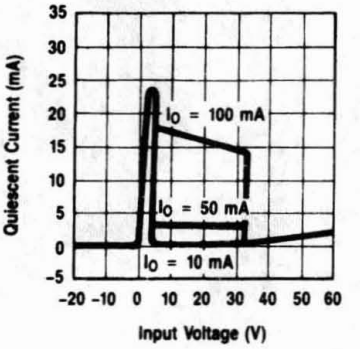
Quiescent Current



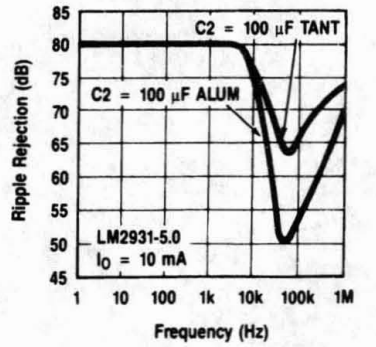
Quiescent Current



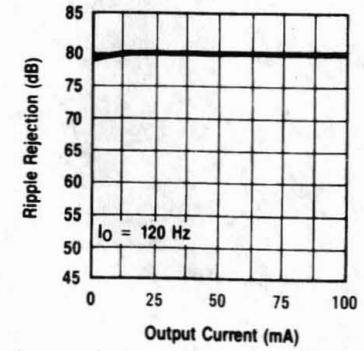
Quiescent Current



Ripple Rejection



Ripple Rejection



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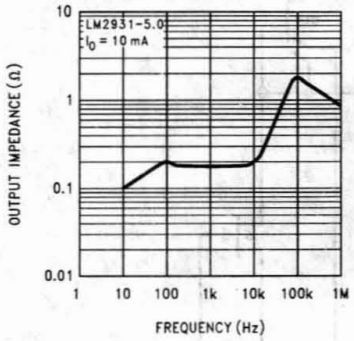
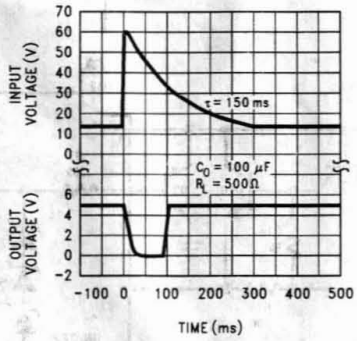
Typical Performance Characteristics

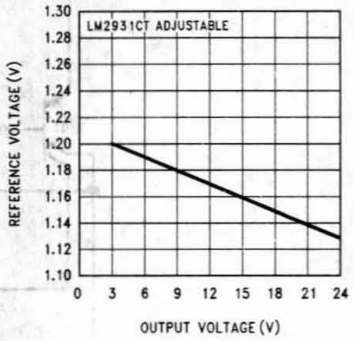
Output Impedance



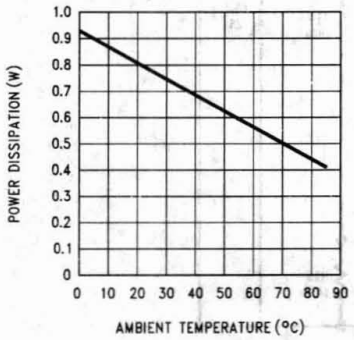
Operation During Load Dump



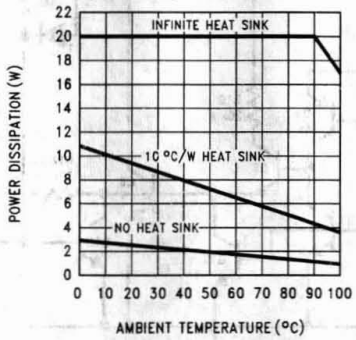
Reference Voltage



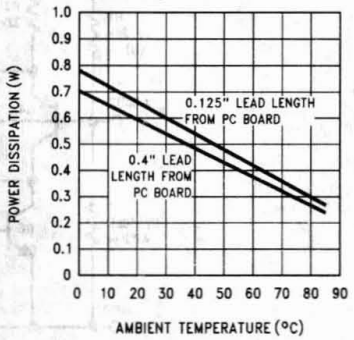
Maximum Power Dissipation (SO-8)



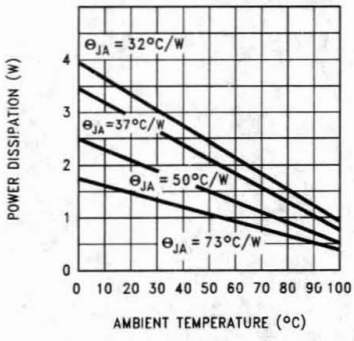
Maximum Power Dissipation (TO-220)



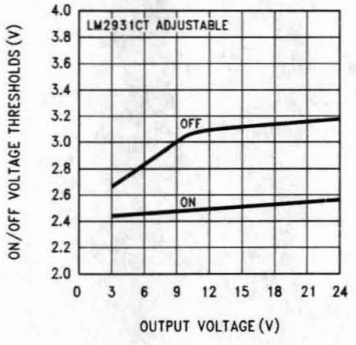
Maximum Power Dissipation (TO-92)



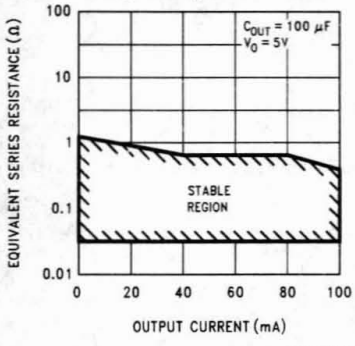
Maximum Power Dissipation (TO-263) (See Note 3)



On/Off Threshold



Output Capacitor ESR



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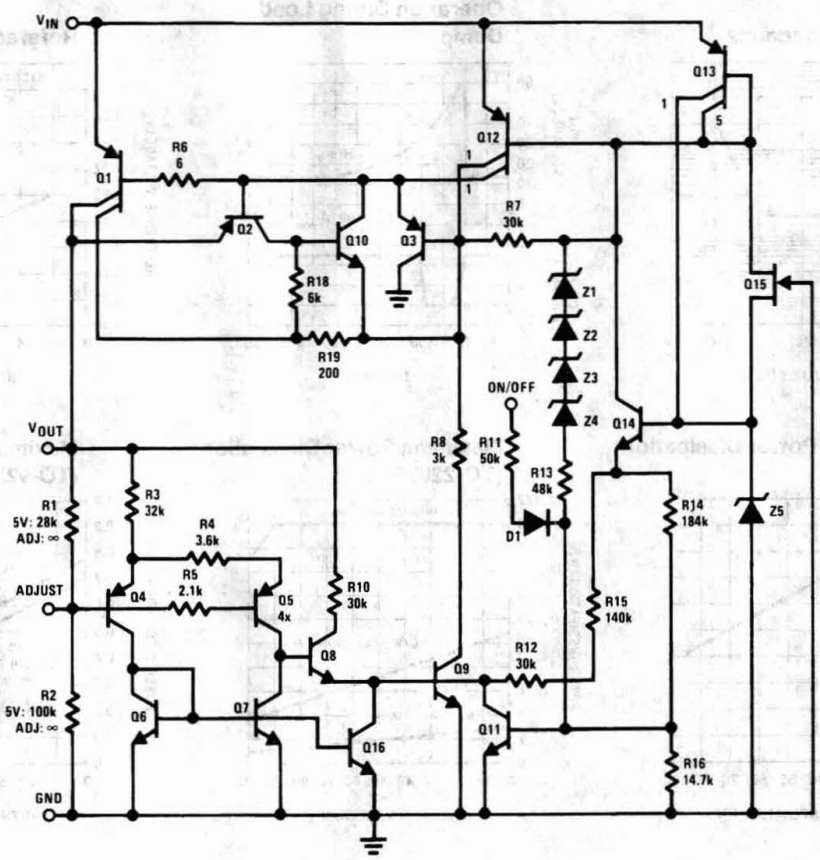
Schematic Diagram



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Application Hints

One of the distinguishing factors of the LM2931 series regulators is the requirement of an output capacitor for device stability. The value required varies greatly depending upon the application circuit and other factors. Thus some comments on the characteristics of both capacitors and the regulator are in order.

High frequency characteristics of electrolytic capacitors depend greatly on the type and even the manufacturer. As a result, a value of capacitance that works well with the LM2931 for one brand or type may not necessary be sufficient with an electrolytic of different origin. Sometimes actual bench testing, as described later, will be the only means to determine the proper capacitor type and value. Experience has shown that, as a rule of thumb, the more expensive and higher quality electrolytics generally allow a smaller value for regulator stability. As an example, while a high-quality 100 μF aluminum electrolytic covers all general application circuits, similar stability can be obtained with a tantalum electrolytic of only 47 μF. This factor of two can generally be applied to any special application circuit also.

Another critical characteristic of electrolytics is their performance over temperature. While the LM2931 is designed to operate to $-40°C$, the same is not always true with all electrolytics (hot is generally not a problem). The electrolyte in many aluminum types will freeze around $-30°C$, reducing their effective value to zero. Since the capacitance is needed for regulator stability, the natural result is oscillation (and lots of it) at the regulator output. For all application circuits where cold operation is necessary, the output capacitor must be rated to operate at the minimum temperature. By coincidence, worst-case stability for the LM2931 also occurs at minimum temperatures. As a result, in applications where the regulator junction temperature will never be less than 25°C, the output capacitor can be reduced approximately by a factor of two over the value needed for the entire temperature range. To continue our example with the tantalum electrolytic, a value of only 22 μF would probably thus suffice. For high-quality aluminum, 47 μF would be adequate in such an application.

Another regulator characteristic that is noteworthy is that stability decreases with higher output currents. This sensible fact has important connotations. In many applications, the LM2931 is operated at only a few milliamps of output current or less. In such a circuit, the output capacitor can be further reduced in value. As a rough estimation, a circuit that is required to deliver a maximum of 10 mA of output current from the regulator would need an output capacitor of only half the value compared to the same regulator required to deliver the full output current of 100 mA. If the example of the tantalum capacitor in the circuit rated at 25°C junction temperature and above were continued to include a maximum of 10 mA of output current, then the 22 μF output capacitor could be reduced to only 10 μF.

In the case of the LM2931CT adjustable regulator, the minimum value of output capacitance is a function of the output voltage. As a general rule, the value decreases with higher output voltages, since internal loop gain is reduced.

At this point, the procedure for bench testing the minimum value of an output capacitor in a special application circuit should be clear. Since worst-case occurs at minimum operating temperatures and maximum operating currents, the entire circuit, including the electrolytic, should be cooled to the minimum temperature. The input voltage to the regulator should be maintained at 0.6V above the output to keep internal power dissipation and die heating to a minimum. Worst-case occurs just after input power is applied and before the die has had a chance to heat up. Once the minimum value of capacitance has been found for the brand and type of electrolytic in question, the value should be doubled for actual use to account for production variations both in the capacitor and the regulator. (All the values in this section and the remainder of the data sheet were determined in this fashion.)

Definition of Terms

Dropout Voltage: The input-output voltage differential at which the circuit ceases to regulate against further reduction in input voltage. Measured when the output voltage has dropped 100 mV from the nominal value obtained at 14V input, dropout voltage is dependent upon load current and junction temperature.

Input Voltage: The DC voltage applied to the input terminals with respect to ground.

Input-Output Differential: The voltage difference between the unregulated input voltage and the regulated output voltage for which the regulator will operate.

Line Regulation: The change in output voltage for a change in the input voltage. The measurement is made under conditions of low dissipation or by using pulse techniques such that the average chip temperature is not significantly affected.

Load Regulation: The change in output voltage for a change in load current at constant chip temperature.

Long Term Stability: Output voltage stability under accelerated life-test conditions after 1000 hours with maximum rated voltage and junction temperature.

Output Noise Voltage: The rms AC voltage at the output, with constant load and no input ripple, measured over a specified frequency range.

Quiescent Current: That part of the positive input current that does not contribute to the positive load current. The regulator ground lead current.

Ripple Rejection: The ratio of the peak-to-peak input ripple voltage to the peak-to-peak output ripple voltage at a specified frequency.

Temperature Stability of V_O: The percentage change in output voltage for a thermal variation from room temperature to either temperature extreme.

National Semiconductor

LM2935 Low Dropout Dual Regulator

General Description

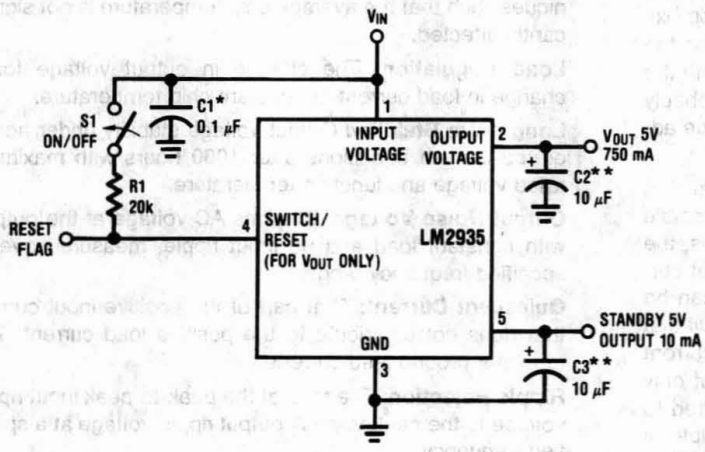
The LM2935 dual 5V regulator provides a 750 mA output as well as a 10 mA standby output. It features a low quiescent current of 3 mA or less when supplying 10 mA loads from the 5V standby regulator output. This unique characteristic and the extremely low input-output differential required for proper regulation (0.55V for output currents of 10 mA) make the LM2935 the ideal regulator for power systems that include standby memory. Applications include microprocessor power supplies demanding as much as 750 mA of output current.

Designed for automotive applications, the LM2935 and all regulated circuitry are protected from reverse battery installations or 2 battery jumps. During line transients, such as a load dump (60V) when the input voltage to the regulator can momentarily exceed the specified maximum operating voltage, the 0.75A regulator will automatically shut down to protect both internal circuits and the load while the standby regulator will continue to power any standby load. The LM2935 cannot be harmed by temporary mirror-image insertion. Familiar regulator features such as short circuit and thermal overload protection are also provided.

Features

- Two 5V regulated outputs
- Output current in excess of 750 mA
- Low quiescent current standby regulator
- Input-output differential less than 0.6V at 0.5A
- Reverse battery protection
- 60V load dump protection
- −50V reverse transient protection
- Short circuit protection
- Internal thermal overload protection
- Available in 5-lead TO-220
- ON/OFF switch controls high current output
- Reset error flag
- P+ Product Enhancement tested

Typical Application Circuit



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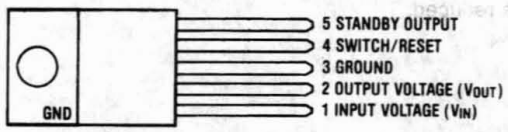
*Required if regulator is located far from power supply filter.

**C_{OUT} must be at least 10 μF to maintain stability. May be increased without bound to maintain regulation during transients. Locate as close as possible to the regulator. This capacitor must be rated over the same operating temperature range as the regulator. The equivalent series resistance (ESR) of this capacitor is critical; see curve.

FIGURE 1. Test and Application Circuit

Connection Diagram

TO-220 5-Lead



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Front View

Order Number LM2935T
See NS Package Number T05A

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Input Voltage	
Operating Range	26V
Overvoltage Protection	60V
Internal Power Dissipation (Note 1)	Internally Limited
Operating Temperature Range	−40°C to + 125°C
Maximum Junction Temperature	150°C
Storage Temperature Range	−65°C to + 150°C
Lead Temp. (Soldering, 10 seconds)	230°C

Electrical Characteristics for V_{OUT}

V_{IN} = 14V, I_O = 500 mA, T_J = 25°C (Note 4), C2 = 10 μF (unless otherwise specified)

Parameter	Conditions	Typ	Tested Limit (Note 3)	Units Limit
Output Voltage	6V ≤ V_{IN} ≤ 26V, 5 mA ≤ I_O ≤ 500 mA, −40°C ≤ T_J ≤ 125°C (Note 2)	5.00	5.25 4.75	V_{MAX} V_{MIN}
Line Regulation	9V ≤ V_{IN} ≤ 16V, I_O = 5 mA 6V ≤ V_{IN} ≤ 26V, I_O = 5 mA	4 10	25 50	mV_{MAX} mV_{MAX}
Load Regulation	5 mA ≤ I_O ≤ 500 mA	10	50	mV_{MAX}
Output Impedance	500 mA_{DC} and 10 mA_{rms}, 100 Hz–10 kHz	200		mΩ
Quiescent Current	I_O ≤ 10 mA, No Load on Standby I_O = 500 mA, No Load on Standby I_O = 750 mA, No Load on Standby	3 40 90	 100 	mA mA_{MAX} mA
Output Noise Voltage	10 Hz–100 kHz	100		μV_{rms}
Long Term Stability		20		mV/1000 hr
Ripple Rejection	f_O = 120 Hz	66		dB
Dropout Voltage	I_O = 500 mA I_O = 750 mA	0.45 0.82	0.6 	V_{MAX}
Current Limit		1.2	0.75	A_{MIN}
Maximum Operational Input Voltage		31	26	V_{MIN}
Maximum Line Transient	V_O ≤ 5.5V	70	60	V
Reverse Polarity Input Voltage, DC		−30	−15	V
Reverse Polarity Input Voltage, Transient	1% Duty Cycle, τ ≤ 100 ms, 10Ω Load	−80	−50	V
Reset Output Voltage Low High	 R1 = 20k, V_{IN} = 4.0V R1 = 20k, V_{IN} = 14V	 0.9 5.0	 1.2 6.0 4.5	 V_{MAX} V_{MAX} V_{MIN}
Reset Output Current	Reset = 1.2V	5		mA
ON/OFF Resistor	R1 (± 10% Tolerance)		20	$k\Omega_{MAX}$

Note 1: Thermal resistance without a heat sink for junction to case temperature is 3°C/W(TO-220). Thermal resistance for TO-220 case to ambient temperature is 50° C/W.

Note 2: The temperature extremes are guaranteed but not 100% production tested. This parameter is not used to calculate outgoing AQL.

Note 3: Tested Limits are guaranteed and 100% tested in production.

Note 4: To ensure constant junction temperature, low duty cycle pulse testing is used.

Electrical Characteristics for Standby Output

$I_O = 10$ mA, $V_{IN} = 14V$, S1 open, $C_{OUT} = 10\ \mu F$, $T_J = 25°C$ (Note 4), (unless otherwise specified)

Parameter	Standby Output Conditions	Typ	Tested Limit	Units Limit
Output Voltage	$I_O \leq 10$ mA, $6V \leq V_{IN} \leq 26V$, $-40°C \leq T_J \leq 125°C$	5.00	5.25 4.75	V_{MAX} V_{MIN}
Tracking	V_{OUT} − Standby Output Voltage	50	200	mV_{MAX}
Line Regulation	$6V \leq V_{IN} \leq 26V$	4	50	mV_{MAX}
Load Regulation	$1\ mA \leq I_O \leq 10$ mA	10	50	mV_{MAX}
Output Impedance	10 mA_{DC} and 1 mA_{rms}, 100 Hz–10 kHz	1		Ω
Quiescent Current	$I_O \leq 10$ mA, V_{OUT} OFF (Note 2)	2	3	mA_{MAX}
Output Noise Voltage	10 Hz–100 kHz	300		μV
Long Term Stability		20		mV/1000 hr
Ripple Rejection	$f_O = 120$ Hz	66		dB
Dropout Voltage	$I_O \leq 10$ mA	0.55	0.7	V_{MAX}
Current Limit		70	25	mA_{MIN}
Maximum Operational Input Voltage	$V_O \leq 6V$	70	60	V_{MIN}
Reverse Polarity Input Voltage, DC	$V_O \geq -0.3V$, 510Ω Load	−30	−15	V_{MIN}
Reverse Polarity Input Voltage, Transient	1% Duty Cycle $T \leq 100$ ms 500Ω Load	−80	−50	V_{MIN}

Typical Circuit Waveforms

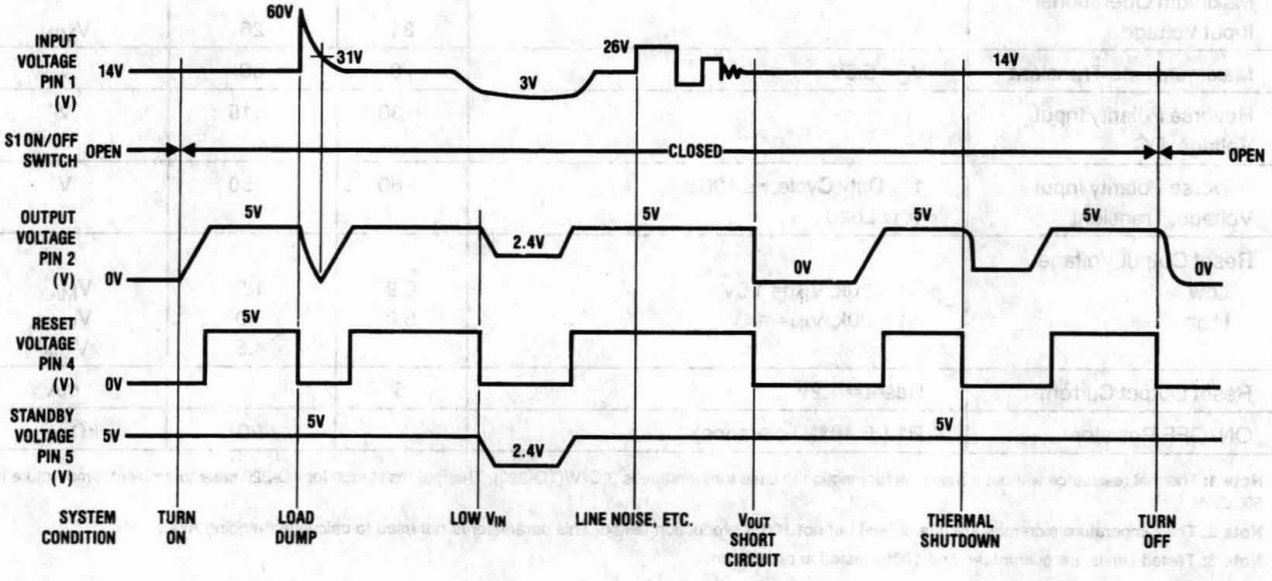

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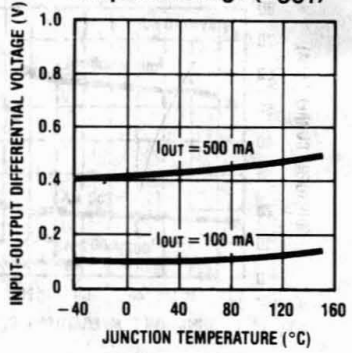
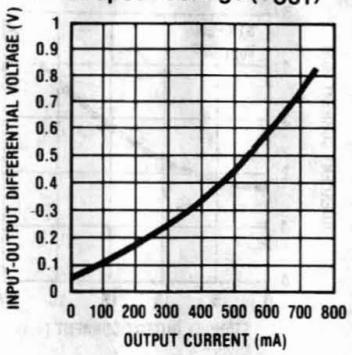
FIGURE 2

Typical Performance Characteristics

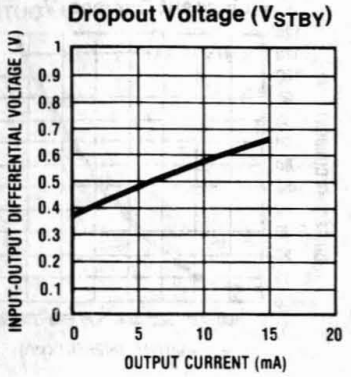
Dropout Voltage (V_{OUT})



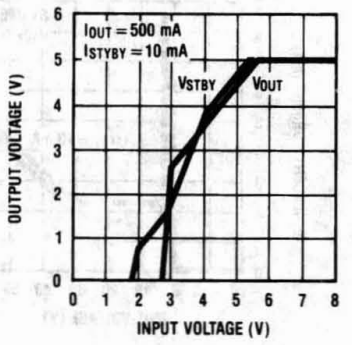
Dropout Voltage (V_{OUT})



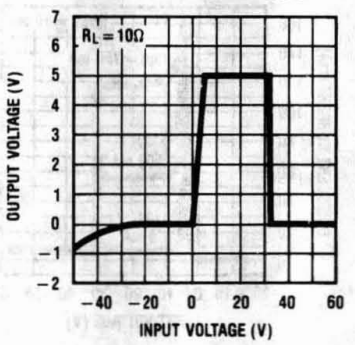
Dropout Voltage (V_{STBY})



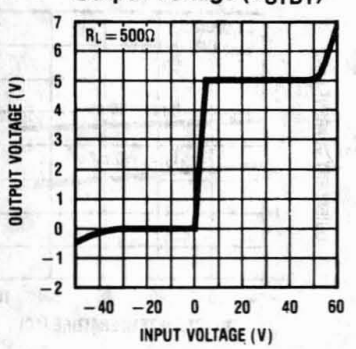
Low Voltage Behavior



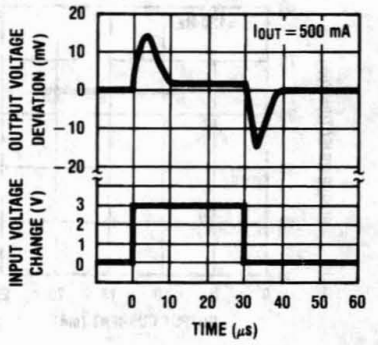
Output Voltage (V_{OUT})



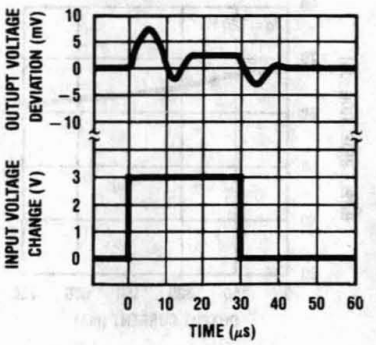
Output Voltage (V_{STBY})



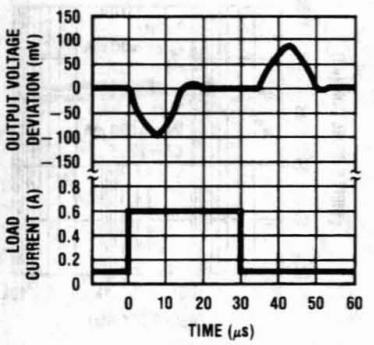
Line Transient Response (V_{OUT})



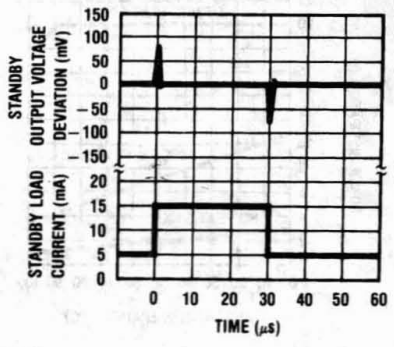
Line Transient Response (V_{STBY})



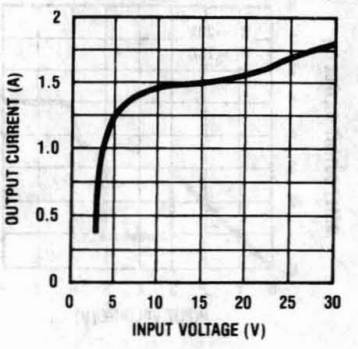
Load Transient Response (V_{OUT})



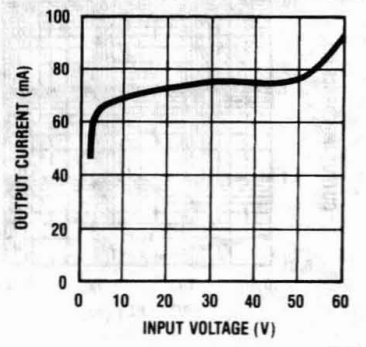
Load Transient Response (V_{STBY})



Peak Output Current (V_{OUT})



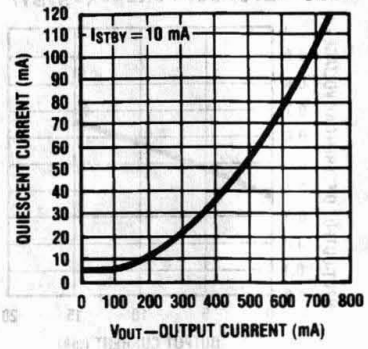
Peak Output Current (V_{STBY})



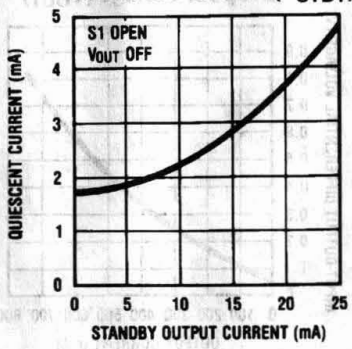
TL/H/5232–3

Typical Performance Characteristics (Continued)

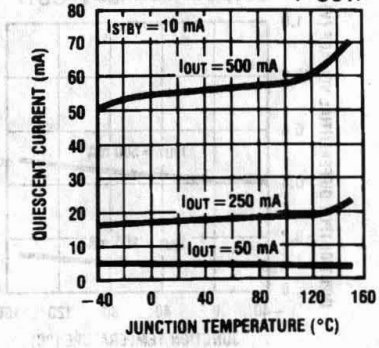
Quiescent Current (V_{OUT})



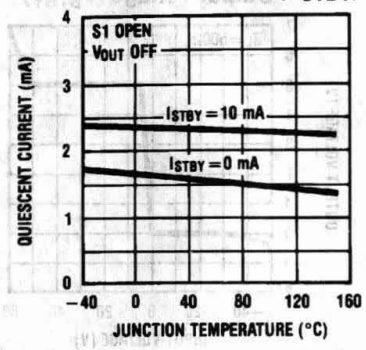
Quiescent Current (V_{STBY})



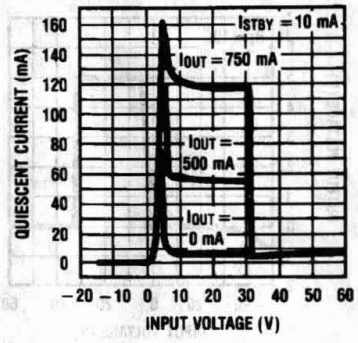
Quiescent Current (V_{OUT})



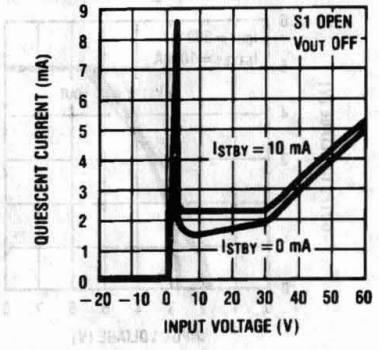
Quiescent Current (V_{STBY})



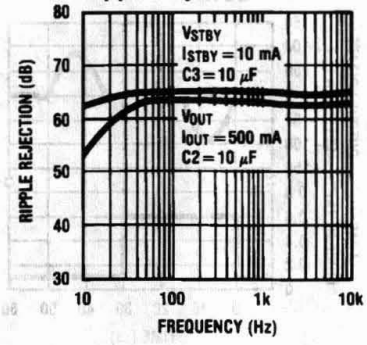
Quiescent Current



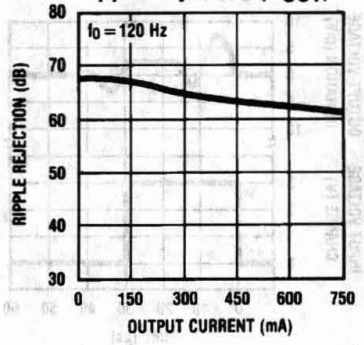
Quiescent Current (V_{STBY})



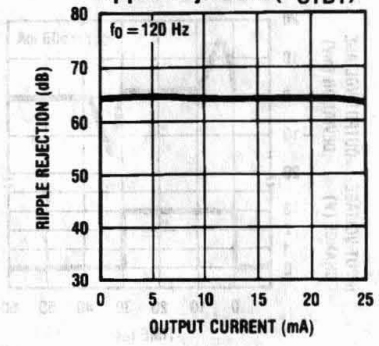
Ripple Rejection



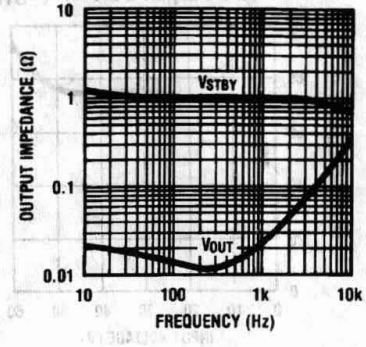
Ripple Rejection (V_{OUT})



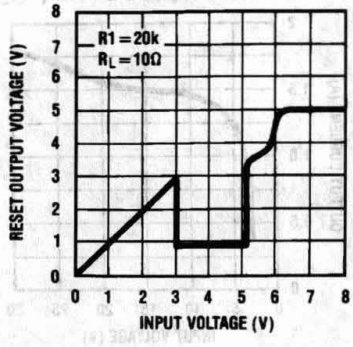
Ripple Rejection (V_{STBY})



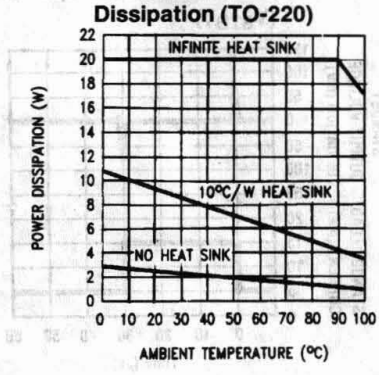
Output Impedance



Reset on Startup



Maximum Power Dissipation (TO-220)



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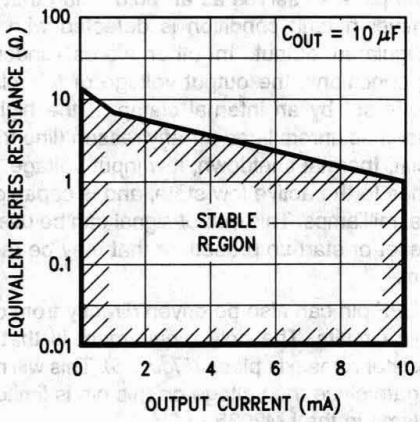
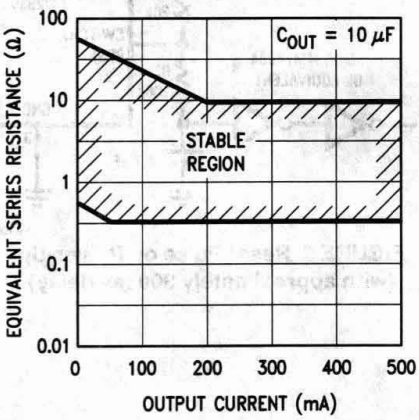
Typical Performance Characteristics (Continued)

Output Capacitor ESR (Standby Output, Pin 5)



TL/H/5232–9

Output Capacitor ESR (Main Output, Pin 2)



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Definition of Terms

Dropout Voltage: The input-output voltage differential at which the circuit ceases to regulate against further reduction in input voltage. Measured when the output voltage has dropped 100 mV from the nominal value obtained at 14V input, dropout voltage is dependent upon load current and junction temperature.

Input Voltage: The DC voltage applied to the input terminals with respect to ground.

Input-Output Differential: The voltage difference between the unregulated input voltage and the regulated output voltage for which the regulator will operate.

Line Regulation: The change in output voltage for a change in the input voltage. The measurement is made under conditions of low dissipation or by using pulse techniques such that the average chip temperature is not significantly affected.

Load Regulation: The change in output voltage for a change in load current at constant chip temperature.

Long Term Stability: Output voltage stability under accelerated life-test conditions after 1000 hours with maximum rated voltage and junction temperature.

Output Noise Voltage: The rms AC voltage at the output, with constant load and no input ripple, measured over a specified frequency range.

Quiescent Current: The part of the positive input current that does not contribute to the positive load current. The regulator ground lead current.

Ripple Rejection: The ratio of the peak-to-peak input ripple voltage to the peak-to-peak output ripple voltage.

Temperature Stability of V_O: The percentage change in output voltage for a thermal variation from room temperature to either temperature extreme.

Application Hints

EXTERNAL CAPACITORS

The LM2935 output capacitors are required for stability. Without them, the regulator outputs will oscillate, sometimes by many volts. Though the 10μF shown are the minimum recommended values, actual size and type may vary depending upon the application load and temperature range. Capacitor effective series resistance (ESR) also factors in the IC stability. Since ESR varies from one brand to the next, some bench work may be required to determine the minimum capacitor value to use in production. Worst-case is usually determined at the minimum ambient temperature and maximum load expected.

Output capacitors can be increased in size to any desired value above the minimum. One possible purpose of this would be to maintain the output voltage during brief conditions of negative input transients that might be characteristic of a particular system.

Capacitors must also be rated at all ambient temperatures expected in the system. Many aluminum type electrolytics will freeze at temperatures less than −30°C, reducing their effective capacitance to zero. To maintain regulator stability down to −40°C, capacitors rated at that temperature (such as tantalums) must be used.

No capacitor must be attached to the ON/OFF and ERROR FLAG pin. Due to the internal circuits of the IC, oscillation on this pin could result.

STANDBY OUTPUT

The LM2935 differs from most fixed voltage regulators in that it is equipped with two regulator outputs instead of one. The additional output is intended for use in systems requiring standby memory circuits. While the high current regulator output can be controlled with the ON/OFF pin described below, the standby output remains on under all conditions as long as sufficient input voltage is applied to the IC. Thus, memory and other circuits powered by this output remain unaffected by positive line transients, thermal shutdown, etc.

The standby regulator circuit is designed so that the quiescent current to the IC is very low (<3 mA) when the other regulator output is off.

Application Hints (Continued)

In applications where the standby output is not needed, it may be disabled by connecting a resistor from the standby output to the supply voltage. This eliminates the need for a more expensive capacitor on the output to prevent unwanted oscillations. The value of the resistor depends upon the minimum input voltage expected for a given system. Since the standby output is shunted with an internal 5.7V zener (*Figure 3*), the current through the external resistor should be sufficient to bias R2 and R3 up to this point. Approximately 60 μA will suffice, resulting in a 10k external resistor for most applications (*Figure 4*).

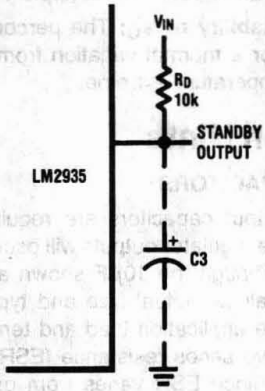


FIGURE 4. Disabling Standby Output to Eliminate C3

HIGH CURRENT OUTPUT

Unlike the standby regulated output, which must remain on whenever possible, the high current regulated output is fault protected against overvoltage and also incorporates thermal shutdown. If the input voltage rises above approximately 30V (e.g., load dump), this output will automatically shutdown. This protects the internal circuitry and enables the IC to survive higher voltage transients than would otherwise be expected. Thermal shutdown is effective against die overheating since the high current output is the dominant source of power dissipation in the IC.

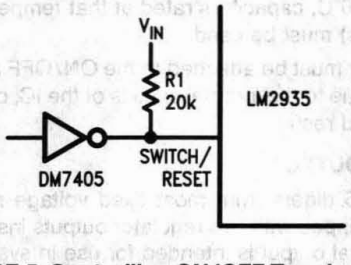


FIGURE 5. Controlling ON/OFF Terminal with a Typical Open Collector Logic Gate

ON/OFF AND ERROR FLAG PIN

This pin has the ability to serve a dual purpose if desired. When controlled in the manner shown in *Figure 1* (common in automotive systems where S1 is the ignition switch), the pin also serves as an output flag that is active low whenever a fault condition is detected with the high current regulated output. In other words, under normal operating conditions, the output voltage of this pin is high (5V). This is set by an internal clamp. If the high current output becomes unregulated for any reason (line transients, short circuit, thermal shutdown, low input voltage, etc.) the pin switches to the active low state, and is capable of sinking several milliamps. This output signal can be used to initiate any reset or start-up procedure that may be required of the system.

The ON/OFF pin can also be driven directly from open collector logic circuits. The only requirement is that the 20k pull-up resistor remain in place *(Figure 5)*. This will not affect the logic gate since the voltage on this pin is limited by the internal clamp in the LM2935 to 5V.

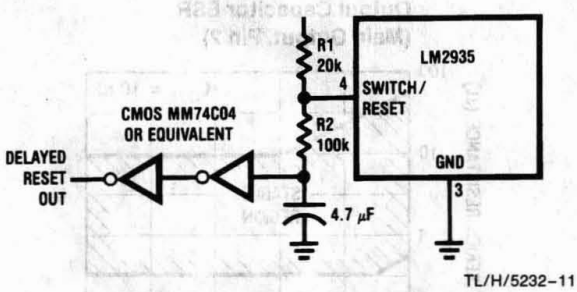


FIGURE 6. Reset Pulse on Power-Up (with approximately 300 ms delay)

Circuit Schematic

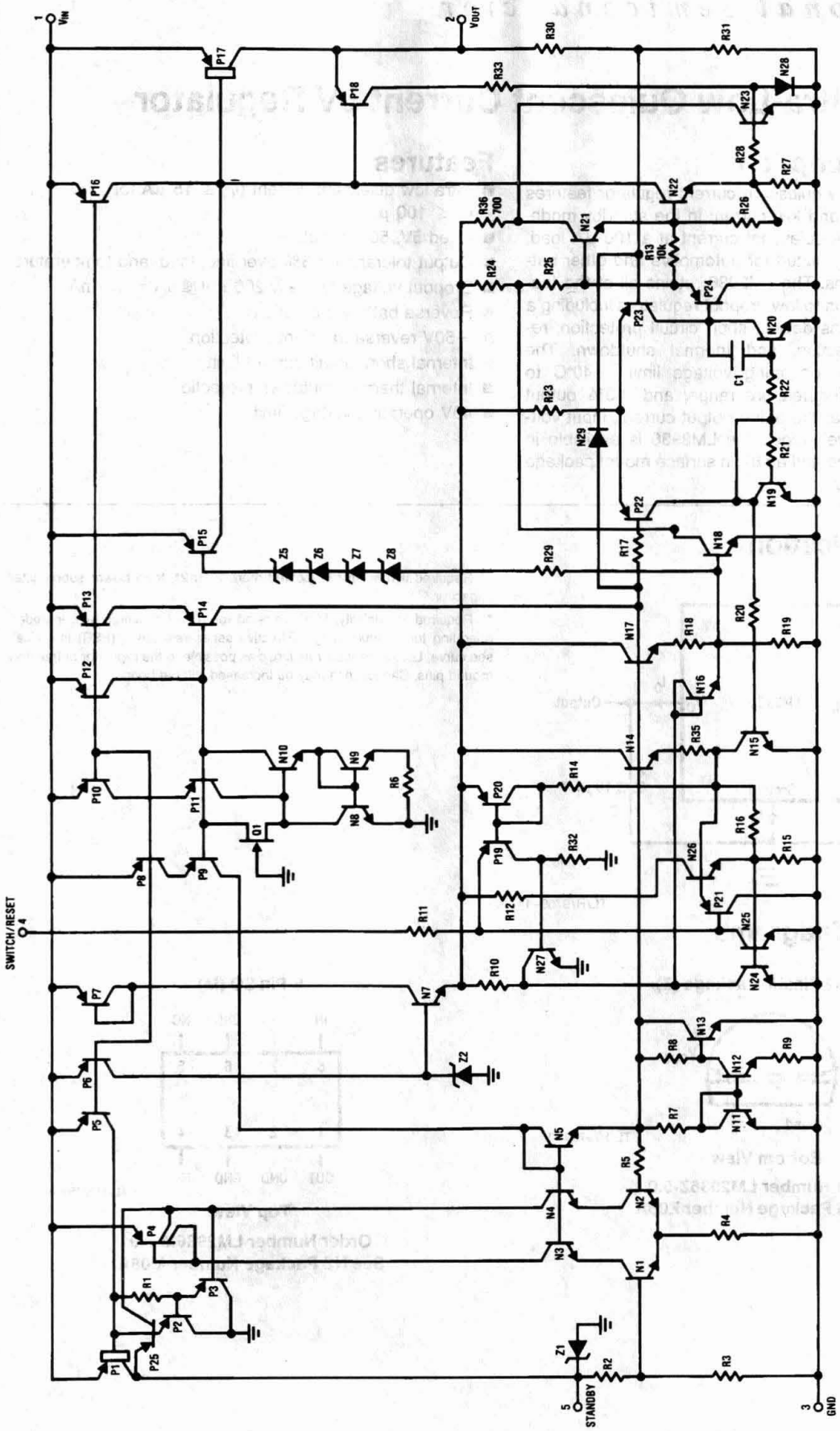


FIGURE 3

National Semiconductor

LM2936 Ultra-Low Quiescent Current 5V Regulator

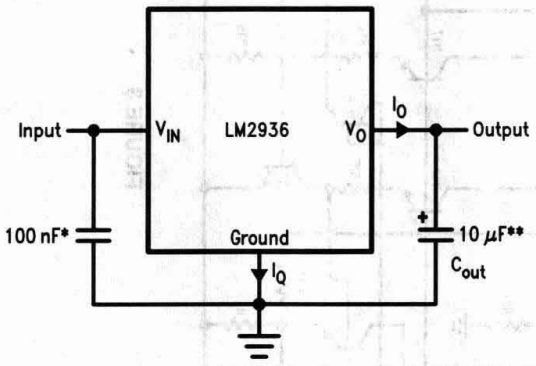
General Description

The LM2936 ultra-low quiescent current regulator features low dropout voltage and low current in the standby mode. With less than 15 μA quiescent current at a 100 μA load, the LM2936 is ideally suited for automotive and other battery operated systems. The LM2936 retains all of the features that are common to low dropout regulators including a low dropout PNP pass device, short circuit protection, reverse battery protection, and thermal shutdown. The LM2936 has a 40V operating voltage limit, −40°C to +125°C operating temperature range, and ±3% output voltage tolerance over the entire output current, input voltage, and temperature range. The LM2936 is available in both a TO-92 package and an 8-pin surface mount package with a fixed 5V output.

Features

- Ultra low quiescent current ($I_Q \leq 15$ μA for $I_O \leq 100$ μA)
- Fixed 5V, 50 mA output
- Output tolerance ±3% over line, load, and temperature
- Dropout voltage typically 200 mV @ I_O = 50 mA
- Reverse battery protection
- −50V reverse transient protection
- Internal short circuit current limit
- Internal thermal shutdown protection
- 40V operating voltage limit

Typical Application



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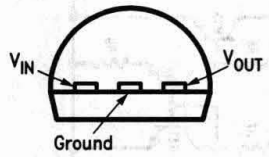
* Required if regulator is located more than 2" from power supply filter capacitor.

** Required for stability. Must be rated for 10 μF minimum over intended operating temperature range. Effective series resistance (ESR) is critical, see curve. Locate capacitor as close as possible to the regulator output and ground pins. Capacitance may be increased without bound.

Connection Diagrams

TO-92 Plastic Package (Z)



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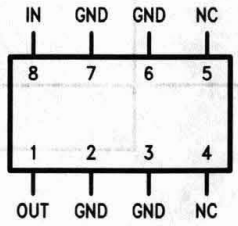
Bottom View

Order Number LM2936Z-5.0
See NS Package Number Z03A

8-Pin SO (M)



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Top View

Order Number LM2936M-5.0
See NS Package Number M08A

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Input Voltage (Survival)	+60V, −50V
ESD Susceptability (Note 2)	1900V
Power Dissipation (Note 3)	Internally limited
Junction Temperature (T_{Jmax})	150°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec.)	260°C

Operating Ratings

Operating Temperature Range	−40°C to +125°C
Maximum Input Voltage (Operational)	40V

Electrical Characteristics

V_{IN} = 14V, I_O = 10 mA, T_J = 25°C, unless otherwise specified. **Boldface** limits apply over entire operating temperature range

Parameter	Conditions	Typical (Note 4)	Tested Limit (Note 5)	Units
Output Voltage	5.5V ≤ V_{IN} ≤ 26V, I_O ≤ 50 mA (Note 6)		**4.85**	V_{min}
		5		V
			5.15	V_{max}
Line Regulation	9V ≤ V_{IN} ≤ 16V	5	10	mV_{max}
	6V ≤ V_{IN} ≤ 40V, I_O = 1 mA	10	30	
Load Regulation	100 μA ≤ I_O ≤ 5 mA	10	30	mV_{max}
	5 mA ≤ I_O ≤ 50 mA	10	30	
Output Impedance	I_O = 30 mAdc and 10 mArms, $_f$ = 1000 Hz	450		mΩ
Quiescent Current	I_O = 100 μA, 8V ≤ V_{IN} ≤ 24V	9	15	μA_{max}
	I_O = 10 mA, 8V ≤ V_{IN} ≤ 24V	0.20	0.50	mA_{max}
	I_O = 50 mA, 8V ≤ V_{IN} ≤ 24V	1.5	2.5	mA_{max}
Output Noise Voltage	10 Hz–100 kHz	500		μV_{rms}
Long Term Stability		20		mV/1000 Hr
Ripple Rejection	V_{ripple} = 1 V_{rms}, f_{ripple} = 120 Hz	60	40	dB_{min}
Dropout Voltage	I_O = 100 μA	0.05	0.10	V_{max}
	I_O = 50 mA	0.20	0.40	V_{max}
Reverse Polarity DC Input Voltage	R_L = 500Ω, V_O ≥ −0.3V		−15	V_{min}
Reverse Polarity Transient Input Voltage	R_L = 500Ω, T = 1 ms	−80	−50	V_{min}
Output Leakage with Reverse Polarity Input	V_{IN} = −15V, R_L = 500Ω	−0.1	−600	μA_{max}
Maximum Line Transient	R_L = 500Ω, V_O ≤ 5.5V, T = 40 ms		60	V_{min}
Short Circuit Current	V_O = 0V	120	250	mA_{max}
			65	mA_{min}

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications do not apply when operating the device beyond its specified operating ratings.

Note 2: Human body model, 100 pF discharge through a 1.5 kΩ resistor.

Note 3: The maximum power dissipation is a function of T_{Jmax}, Θ_{JA}, and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{Jmax} - T_A)/\Theta_{JA}$. If this dissipation is exceeded, the die temperature will rise above 150°C and the LM2936 will go into thermal shutdown. For the LM2936Z, the junction-to-ambient thermal resistance (Θ_{JA}) is 195°C/W. For the LM2936M, θja is 160°C/W.

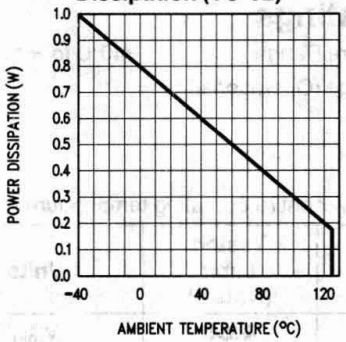
Note 4: Typicals are at 25°C (unless otherwise specified) and represent the most likely parametric norm.

Note 5: Tested limits are guaranteed to National's AOQL (Average Outgoing Quality Level) and 100% tested.

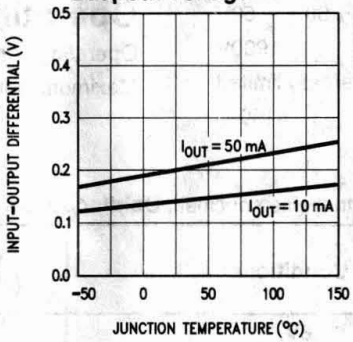
Note 6: To ensure constant junction temperature, pulse testing is used.

Typical Performance Characteristics

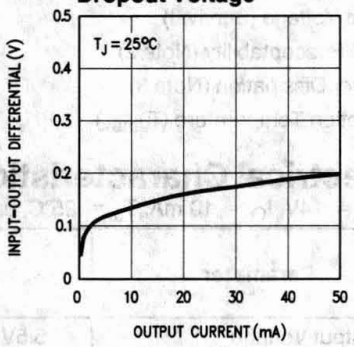
Maximum Power Dissipation (TO-92)



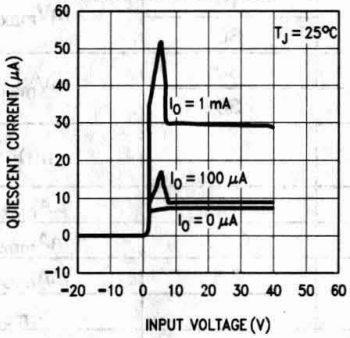
Dropout Voltage



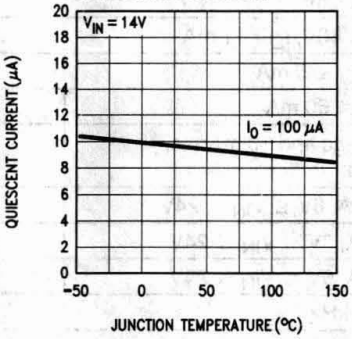
Dropout Voltage



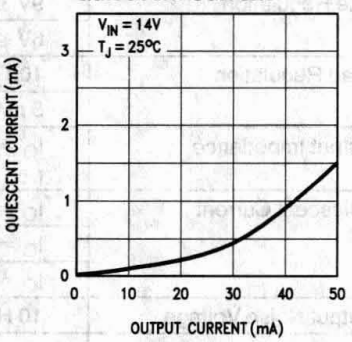
Quiescent Current



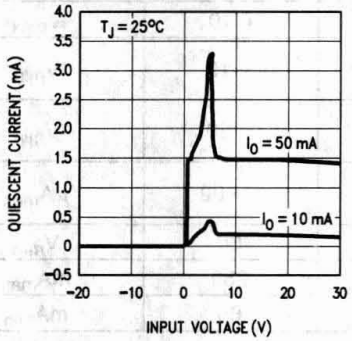
Quiescent Current



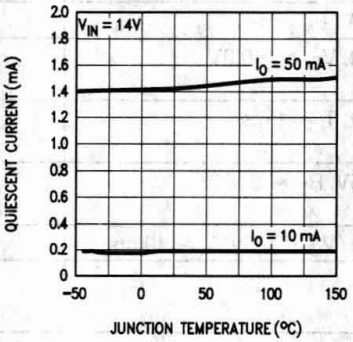
Quiescent Current



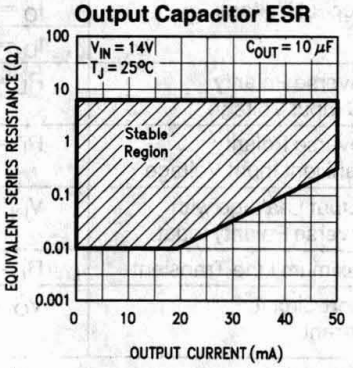
Quiescent Current



Quiescent Current



Output Capacitor ESR



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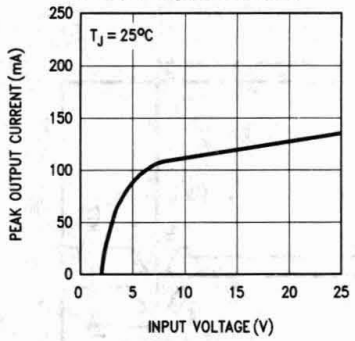
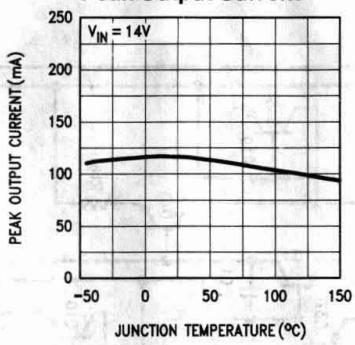
Typical Performance Characteristics (Continued)

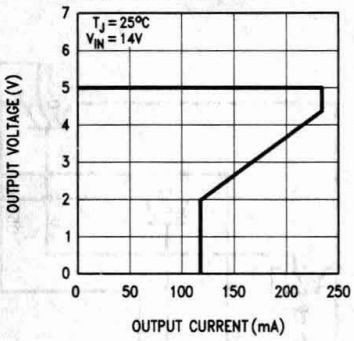
Peak Output Current



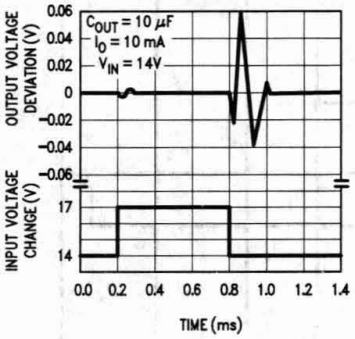
Peak Output Current



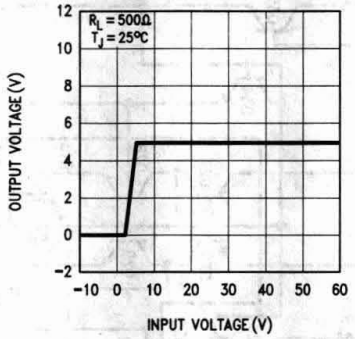
Current Limit



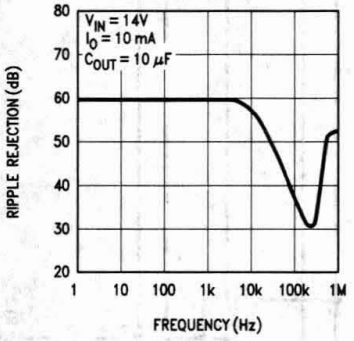
Line Transient Response



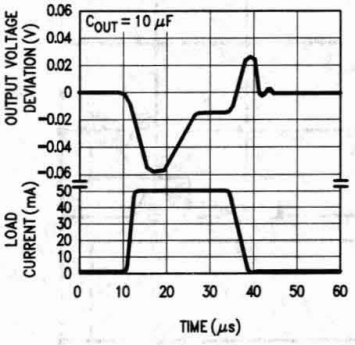
Output at Voltage Extremes



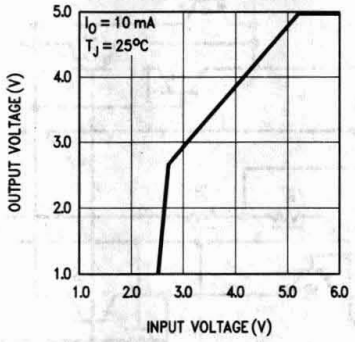
Ripple Rejection



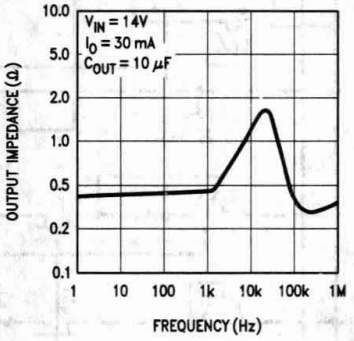
Load Transient Response



Low Voltage Behavior



Output Impedance



TL/H/9759–4

Applications Information

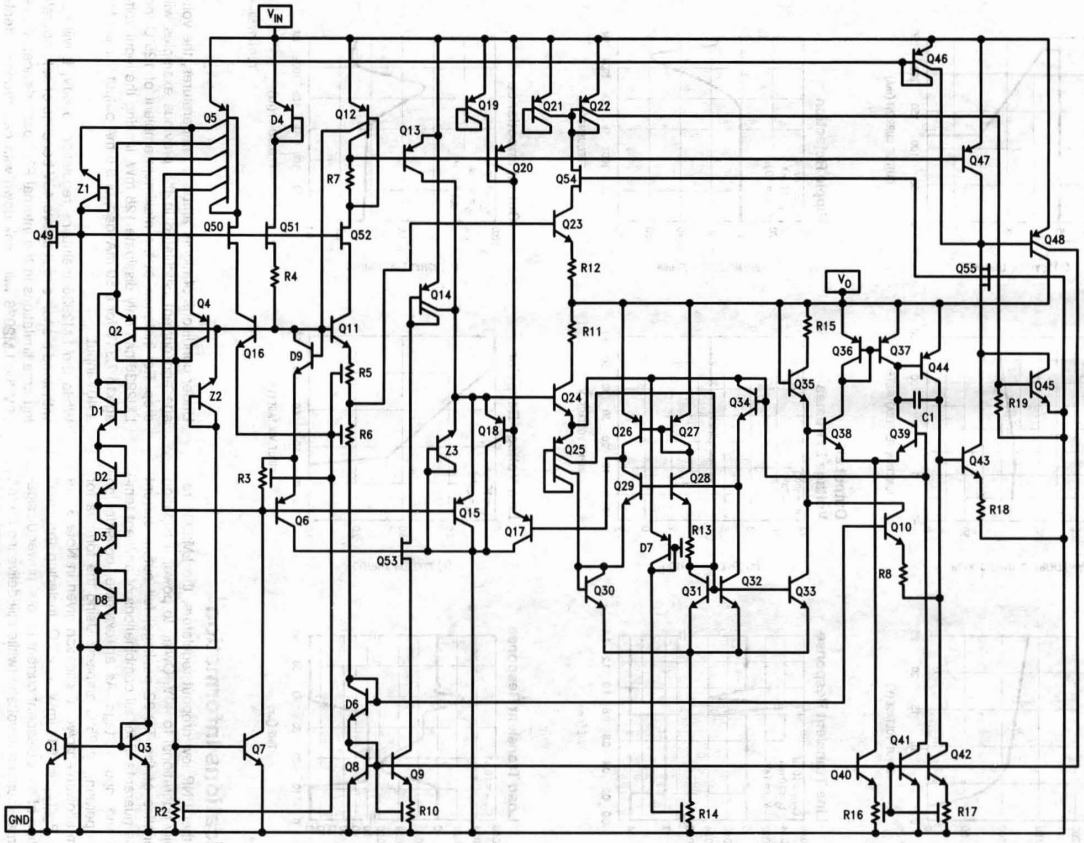
Unlike other PNP low dropout regulators, the LM2936 remains fully operational to 40V. Owing to power dissipation characteristics of the TO-92 package, full output current cannot be guaranteed for all combinations of ambient temperature and input voltage. As an example, consider an LM2936 operating at 25°C ambient. Using the formula for maximum allowable power dissipation given in Note 3, we find that P_{Dmax} = 641 mW at 25°C. Including the small contribution of the quiescent current to total power dissipation the maximum input voltage (while still delivering 50 mA output current) is 17.3V. The device will go into thermal shutdown if it attempts to deliver full output current with an input voltage of more than 17.3V. Similarly, at 40V input and 25°C ambient the LM2936 can deliver 18 mA maximum.

Under conditions of higher ambient temperatures, the voltage and current calculated in the previous examples will drop. For instance, at the maximum ambient of 125°C the LM2936 can only dissipate 128 mW, limiting the input voltage to 7.34V for a 50 mA load, or 3.5 mA output current for a 40V input.

While the LM2936 maintains regulation to 60V, it will not withstand a short circuit above 40V because of safe operating area limitations in the internal PNP pass device. Above 60V the LM2936 will break down with catastrophic effects on the regulator and possibly the load as well. Do not use this device in a design where the input operating voltage may exceed 40V, or where transients are likely to exceed 60V.

3

Equivalent Schematic Diagram



TL/H/9759–5

National Semiconductor

LM2937 500 mA Low Dropout Regulator

General Description

The LM2937 is a positive voltage regulator capable of supplying up to 500 mA of load current. The use of a PNP power transistor provides a low dropout voltage characteristic. With a load current of 500 mA the minimum input to output voltage differential required for the output to remain in regulation is typically 0.5V (1V guaranteed maximum over the full operating temperature range). Special circuitry has been incorporated to minimize the quiescent current to typically only 10 mA with a full 500 mA load current when the input to output voltage differential is greater than 3V.

The LM2937 requires an output bypass capacitor for stability. As with most low dropout regulators, the ESR of this capacitor remains a critical design parameter, but the LM2937 includes special compensation circuitry that relaxes ESR requirements. The LM2937 is stable for all ESR below 3Ω. This allows the use of low ESR chip capacitors.

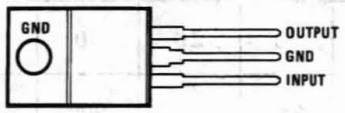
Ideally suited for automotive applications, the LM2937 will protect itself and any load circuitry from reverse battery connections, two-battery jumps and up to +60V/−50V load dump transients. Familiar regulator features such as short circuit and thermal shutdown protection are also built in.

Features

- Fully specified for operation over −40°C to +125°C
- Output current in excess of 500 mA
- Output trimmed for 5% tolerance under all operating conditions
- Typical dropout voltage of 0.5V at full rated load current
- Wide output capacitor ESR range, up to 3Ω
- Internal short circuit and thermal overload protection
- Reverse battery protection
- 60V input transient protection
- Mirror image insertion protection

Connection Diagram and Ordering Information

TO-220 Plastic Package

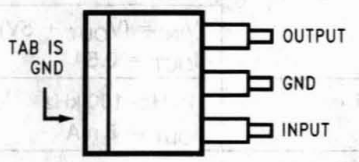


TL/H/11280–2

Front View

Order Number LM2937ET-5.0, LM2937ET-8.0, LM2937ET-10, LM2937ET-12 or LM2937ET-15
See NS Package Number T03B

TO-263 Surface-Mount Package



TL/H/11280–5

Top View

TL/H/11280–6

Side View

Order Number LM2937ES-5.0, LM2937ES-8.0, LM2937ES-10, LM2937ES-12 or LM2937ES-15
See NS Package Number TS3B

Temperature Range	Output Voltage					NSC Package Drawing	Package
	5.0	8.0	10	12	15		
−40°C ≤ T_A ≤ 125°C	LM2937ES-5.0	LM2937ES-8.0	LM2937ES-10	LM2937ES-12	LM2937ES-15	TS3B	TO-263
	LM2537ET-5.0	LM2537ET-8.0	LM2537ET-10	LM2537ET-12	LM2537ET-15	T03B	TO-220

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Input Voltage	
Continuous	26V
Transient (t ≤ 100 ms)	60V
Internal Power Dissipation (Note 2)	Internally Limited
Maximum Junction Temperature	150°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	230°C
ESD Susceptibility (Note 3)	2 kV

Operating Conditions (Note 1)

Temperature Range (T_J) (Note 2)	−40°C to +125°C
Maximum Input Voltage	26V

Electrical Characteristics

$V_{IN} = V_{NOM} + 5V$ (Note 4), $I_{OUT} = 500$ mA, $C_{OUT} = 10\ \mu F$ unless otherwise indicated. **Boldface limits apply over the entire operating temperature range, −40°C ≤ T_J ≤ +125°C**, all other specifications are for $T_A = T_J = 25°C$.

Output Voltage (V_{OUT})		5V		8V		10V		Units
Parameter	**Conditions**	**Typ**	**Limit**	**Typ**	**Limit**	**Typ**	**Limit**	
Output Voltage	5 mA ≤ I_{OUT} ≤ 0.5A	5.00	4.85 **4.75** 5.15 **5.25**	8.00	7.76 **7.60** 8.24 **8.40**	10.00	9.70 **9.50** 10.30 **10.50**	V(Min) V(Min) V(Max) V(Max)
Line Regulation	(V_{OUT} + 2V) ≤ V_{IN} ≤ 26V, I_{OUT} = 5 mA	15	**50**	24	**80**	30	**100**	mV(Max)
Load Regulation	5 mA ≤ I_{OUT} ≤ 0.5A	5	**50**	8	**80**	10	**100**	mV(Max)
Quiescent Current	(V_{OUT} + 2V) ≤ V_{IN} ≤ 26V, I_{OUT} = 5 mA	2	**10**	2	**10**	2	**10**	mA(Max)
	V_{IN} = (V_{OUT} + 5V), I_{OUT} = 0.5A	10	**20**	10	**20**	10	**20**	mA(Max)
Output Noise Voltage	10 Hz–100 kHz I_{OUT} = 5 mA	150		240		300		μVrms
Long Term Stability	1000 Hrs.	20		32		40		mV
Dropout Voltage	I_{OUT} = 500 mA	0.5	**1.0**	0.5	**1.0**	0.5	**1.0**	V(Max)
	I_{OUT} = 50 mA	110	**250**	110	**250**	110	**250**	mV(Max)
Short-Circuit Current		1.0	**0.6**	1.0	**0.6**	1.0	**0.6**	A(Min)
Peak Line Transient Voltage	t_f < 100 ms, R_L = 100Ω	75	**60**	75	**60**	75	**60**	V(Min)
Maximum Operational Input Voltage			**26**		**26**		**26**	V(Min)
Reverse DC Input Voltage	V_{OUT} ≥ −0.6V, R_L = 100Ω	−30	**−15**	−30	**−15**	−30	**−15**	V(Min)
Reverse Transient Input Voltage	t_r < 1 ms, R_L = 100Ω	−75	**−50**	−75	**−50**	−75	**−50**	V(Min)

Electrical Characteristics

$V_{IN} = V_{NOM} + 5V$ (Note 4), $I_{OUT} = 500$ mA, $C_{OUT} = 10\ \mu F$ unless otherwise indicated. **Boldface limits apply over the entire operating temperature range, $-40°C \le T_J \le +125°C$**, all other specifications are for $T_A = T_J = 25°C$.

Output Voltage (V_{OUT})		12V		15V		Units
Parameter	**Conditions**	**Typ**	**Limit**	**Typ**	**Limit**	
Output Voltage	5 mA ≤ I_{OUT} ≤ 0.5A	12.00	11.64 **11.40** 12.36 **12.60**	15.00	14.55 **14.25** 15.45 **15.75**	V (Min) V(Min) V(Max) V(Max)
Line Regulation	(V_{OUT} + 2V) ≤ V_{IN} ≤ 26V, I_{OUT} = 5 mA	36	**120**	45	**150**	mV(Max)
Load Regulation	5 mA ≤ I_{OUT} ≤ 0.5A	12	**120**	15	**150**	mV(Max)
Quiescent Current	(V_{OUT} + 2V) ≤ V_{IN} ≤ 26V, I_{OUT} = 5 mA	2	**10**	2	**10**	mA(Max)
	V_{IN} = (V_{OUT} + 5V), I_{OUT} = 0.5A	10	**20**	10	**20**	mA(Max)
Output Noise Voltage	10 Hz–100 kHz, I_{OUT} = 5 mA	360		450		μVrms
Long Term Stability	1000 Hrs.	44		56		mV
Dropout Voltage	I_{OUT} = 500 mA	0.5	**1.0**	0.5	**1.0**	V(Max)
	I_{OUT} = 50 mA	110	**250**	110	**250**	mV(Max)
Short-Circuit Current		1.0	**0.6**	1.0	**0.6**	A(Min)
Peak Line Transient Voltage	t_f < 100 ms, R_L = 100Ω	75	**60**	75	**60**	V(Min)
Maximum Operational Input Voltage			**26**		**26**	V(Min)
Reverse DC Input Voltage	$V_{OUT} \ge -0.6V$, R_L = 100Ω	−30	**−15**	−30	**−15**	V(Min)
Reverse Transient Input Voltage	t_r < 1 ms, R_L = 100Ω	−75	**−50**	−75	**−50**	V(Min)

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Electrical specifications do not apply when operating the device outside of its rated Operating Conditions.

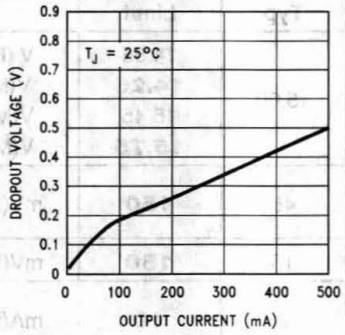
Note 2: The maximum allowable power dissipation at any ambient temperature is $P_{MAX} = (125 - T_A)/\theta_{JA}$, where 125 is the maximum junction temperature for operation, T_A is the ambient temperature, and θ_{JA} is the junction-to-ambient thermal resistance. If this dissipation is exceeded, the die temperature will rise above 125°C and the electrical specifications do not apply. If the die temperature rises above 150°C, the LM2937 will go into thermal shutdown. For the LM2937, the junction-to-ambient thermal resistance θ_{JA} is 65°C/W, for the TO-220, and 73°C/W for the TO-263. When used with a heatsink, θ_{JA} is the sum of the LM2937 junction-to-case thermal resistance θ_{JC} of 3°C/W and the heatsink case-to-ambient thermal resistance. If the TO-263 package is used, the thermal resistance can be reduced by increasing the P.C. board copper area thermally connected to the package. Using 0.5 Square inches of copper area, θ_{JA} is 50°C/W; with 1 square inch of copper area, θ_{JA} is 37°C/W; and with 1.6 or more sqaure inches of copper area, θ_{JA} is 32°C/W.

Note 3: ESD rating is based on the human body model, 100 pF discharged through 1.5 kΩ.

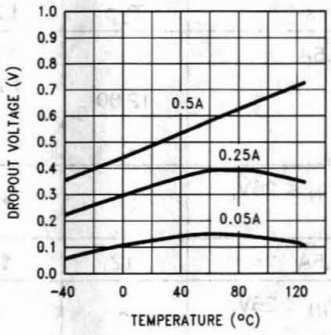
Note 4: Typicals are at T_J = 25°C and represent the most likely parametric norm.

Typical Performance Characteristics

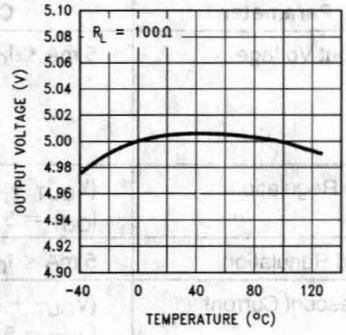
Dropout Voltage vs Output Current



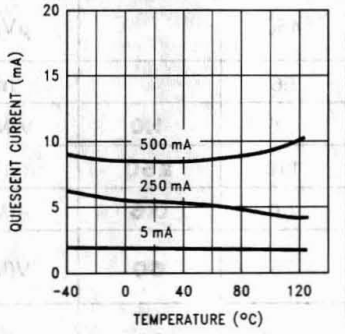
Dropout Voltage vs Temperature



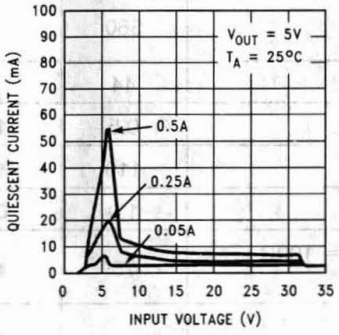
Output Voltage vs Temperature



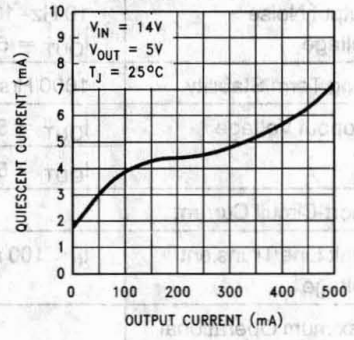
Quiescent Current vs Temperature



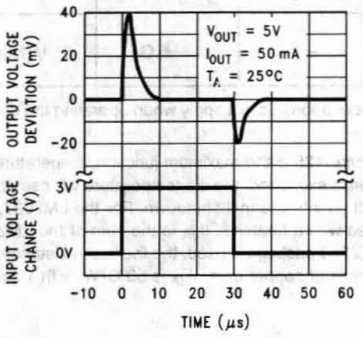
Quiescent Current vs Input Voltage



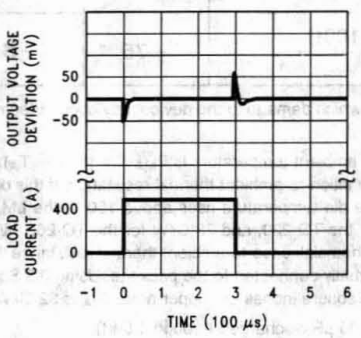
Quiescent Current vs Output Current



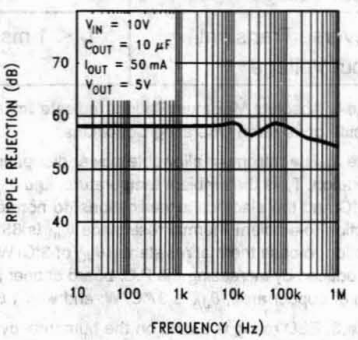
Line Transient Response



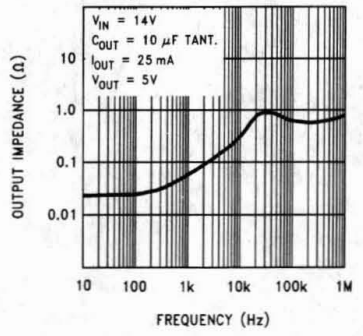
Load Transient Response



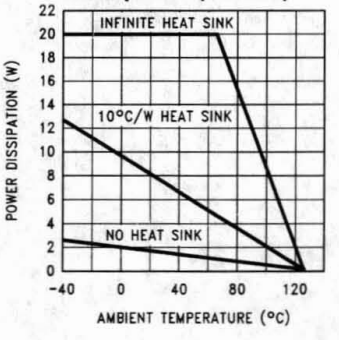
Ripple Rejection



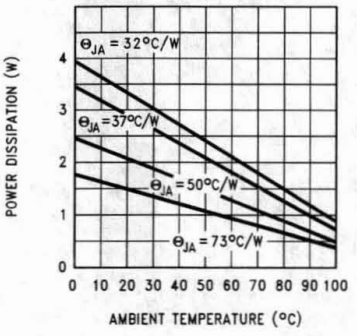
Output Impedance



Maximum Power Dissipation (TO-220)



Maximum Power Dissipation (TO-263) (See Note 2)



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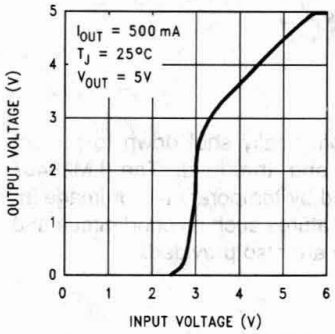
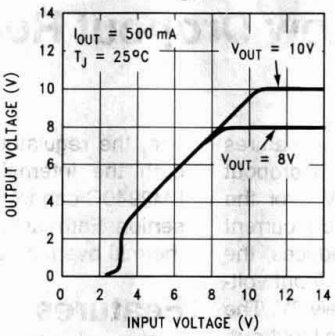
Typical Performance Characteristics (Continued)

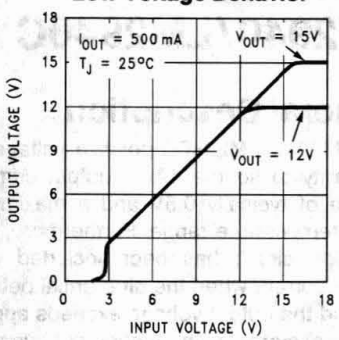
Low Voltage Behavior



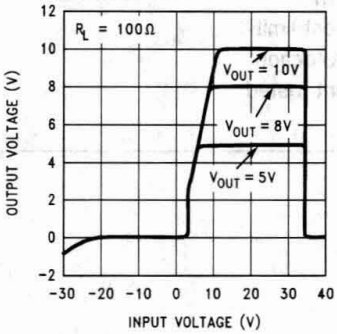
Low Voltage Behavior



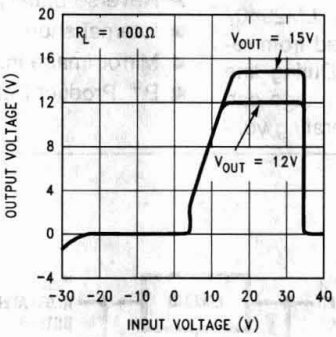
Low Voltage Behavior



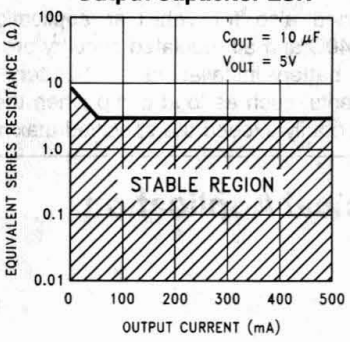
Output at Voltage Extremes



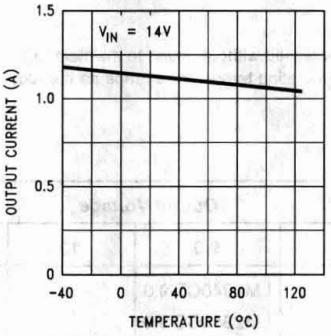
Output at Voltage Extremes



Output Capacitor ESR

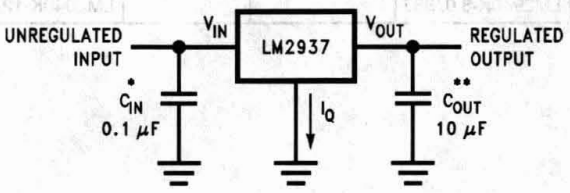


Peak Output Current



TL/H/11280–4

Typical Application



TL/H/11280–1

*Required if the regulator is located more than 3 inches from the power supply filter capacitors.

**Required for stability. C_{out} must be at least 10 μF (over the full expected operating temperature range) and located as close as possible to the regulator. The equivalent series resistance, ESR, of this capacitor may be as high as 3Ω.

3

National Semiconductor

LM2940/LM2940C 1A Low Dropout Regulator

General Description

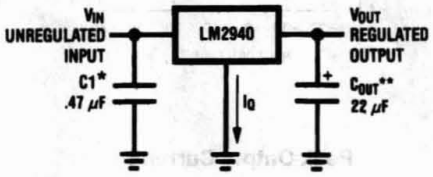
The LM2940/LM2940C positive voltage regulator features the ability to source 1A of output current with a dropout voltage of typically 0.5V and a maximum of 1V over the entire temperature range. Furthermore, a quiescent current reduction circuit has been included which reduces the ground current when the differential between the input voltage and the output voltage exceeds approximately 3V. The quiescent current with 1A of output current and an input-output differential of 5V is therefore only 30 mA. Higher quiescent currents only exist when the regulator is in the dropout mode ($V_{IN} - V_{OUT} \leq 3V$).

Designed also for vehicular applications, the LM2940/LM2940C and all regulated circuitry are protected from reverse battery installations or 2-battery jumps. During line transients, such as load dump when the input voltage can momentarily exceed the specified maximum operating voltage, the regulator will automatically shut down to protect both the internal circuits and the load. The LM2940/LM2940C cannot be harmed by temporary mirror-image insertion. Familiar regulator features such as short circuit and thermal overload protection are also provided.

Features

- Dropout voltage typically 0.5V @I_O = 1A
- Output current in excess of 1A
- Output voltage trimmed before assembly
- Reverse battery protection
- Internal short circuit current limit
- Mirror image insertion protection
- P+ Product Enhancement tested

Typical Application



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*Required if regulator is located far from power supply filter.

**C_{OUT} must be at least 22 μF to maintain stability. May be increased without bound to maintain regulation during transients. Locate as close as possible to the regulator. This capacitor must be rated over the same operating temperature range as the regulator and the ESR is critical; see curve.

Ordering Information

Temperature Range	Output Voltage						Package
	5.0	8.0	9.0	10	12	15	
0°C ≤ T_A ≤ 125°C	LM2940CT-5.0 LM2940CS-5.0		LM2940CT-9.0 LM2940CS-9.0		LM2940CT-12 LM2940CS-12	LM2940CT-15 LM2940CS-15	TO-220 TO-263
−40°C ≤ T_A ≤ 125°C	LM2940T-5.0 LM2940S-5.0	LM2940T-8.0 LM2940S-8.0	LM2940T-9.0 LM2940S-9.0	LM2940T-10 LM2940S-10	LM2940T-12 LM2940S-12		TO-220 TO-263
−55°C ≤ T_A ≤ 125°C	LM2940K-5.0/883	LM2940K-8.0/883			LM2940K-12/883	LM2940K-15/883	TO-3

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications. (Note 2)

LM2940S, T ≤ 100 ms	60V
LM2940T, T ≤ 100 ms	60V
LM2940K/883, T ≤ 20 ms	40V
LM2940CT, T ≤ 1 ms	45V
LM2940CS, T ≤ 1 ms	45V
Internal Power Dissipation (Note 3)	Internally Limited
Maximum Junction Temperature	150°C
Storage Temperature Range	$-65°C \le T_J \le +150°C$
Lead Temperature (Soldering, 10 seconds)	
TO-3 (K) Package	300°C
TO-220 (T) Package	260°C
TO-263 (S) Package	260°C
ESD Susceptibility (Note 4)	2 kV

Operating Conditions (Note 1)

Input Voltage	26V
Temperature Range	
LM2940K/883	$-55°C \le T_A \le 125°C$
LM2940T, LM2940S	$-40°C \le T_A \le 125°C$
LM2940CT, LM2940CS	$0°C \le T_A \le 125°C$

Electrical Characteristics

$V_{IN} = V_O + 5V$, $I_O = 1A$, $C_O = 22\ \mu F$, unless otherwise specified. **Boldface limits apply over the entire operating temperature range of the indicated device.** All other specifications apply for $T_A = T_J = 25°C$

Output Voltage (V_O)		5V			8V			
Parameter	**Conditions**	**Typ**	**LM2940 Limit (Note 5)**	**LM2940/883 Limit (Note 6)**	**Typ**	**LM2940 Limit (Note 5)**	**LM2940/883 Limit (Note 6)**	**Units**
		$6.25V \le V_{IN} \le 26V$			$9.4V \le V_{IN} \le 26V$			
Output Voltage	$5\ mA \le I_O \le 1A$	5.00	4.85/**4.75** 5.15/**5.25**	4.85/**4.75** 5.15/**5.25**	8.00	7.76/**7.60** 8.24/**8.40**	7.76/**7.60** 8.24/**8.40**	V_{MIN} V_{MAX}
Line Regulation	$V_O + 2V \le V_{IN} \le 26V$, $I_O = 5\ mA$	20	50	40/**50**	20	80	50/**80**	mV_{MAX}
Load Regulation	$50\ mA \le I_O \le 1A$ LM2940, LM2940/883 LM2940C	 35 35	 50/**80** 50	 50/**100**	 55 55	 80/**130** 80	 80/**130**	mV_{MAX}
Output Impedance	100 mADC and 20 mArms, $f_O = 120\ Hz$	35		1000/**1000**	55		1000/**1000**	mΩ
Quiescent Current	$V_O + 2V \le V_{IN} \le 26V$, $I_O = 5\ mA$ LM2940, LM2940/883 LM2940C	 10 10	 15/**20** 15	 15/**20**	 10	 15/**20**	 15/**20**	mA_{MAX}
	$V_{IN} = V_O + 5V$, $I_O = 1A$	30	45/**60**	50/**60**	30	45/**60**	50/**60**	mA_{MAX}
Output Noise Voltage	10 Hz − 100 kHz, $I_O = 5\ mA$	150		700/**700**	240		1000/**1000**	μV_{rms}
Ripple Rejection	$f_O = 120\ Hz$, $1\ V_{rms}$, $I_O = 100\ mA$ LM2940 LM2940C	 72 72	 60/**54** 60	 	 66 66	 54/**48** 54	 	dB_{MIN}
	$f_O = 1\ kHz$, $1\ V_{rms}$, $I_O = 5\ mA$			60/**50**			54/**48**	dB_{MIN}
Long Term Stability		20			32			mV/ 1000 Hr
Dropout Voltage	$I_O = 1A$	0.5	0.8/**1.0**	0.7/**1.0**	0.5	0.8/**1.0**	0.7/**1.0**	V_{MAX}
	$I_O = 100\ mA$	110	150/**200**	150/**200**	110	150/**200**	150/**200**	mV_{MAX}

3

Electrical Characteristics

$V_{IN} = V_O + 5V$, $I_O = 1A$, $C_O = 22\ \mu F$, unless otherwise specified. **Boldface limits apply over the entire operating temperature range of the indicated device.** All other specifications apply for $T_A = T_J = 25°C$ (Continued)

Output Voltage (V_O)		5V			8V			
Parameter	**Conditions**	**Typ**	**LM2940 Limit (Note 5)**	**LM2940/883 Limit (Note 6)**	**Typ**	**LM2940 Limit (Note 5)**	**LM2940/883 Limit (Note 6)**	**Units**
Short Circuit Current	(Note 7)	1.9	1.6	1.5/**1.3**	1.9	1.6	1.6/**1.3**	A_{MIN}
Maximum Line Transient	$R_O = 100\Omega$							
	LM2940, T ≤ 100 ms	75	60/**60**		75	60/**60**		
	LM2940/883, T ≤ 20 ms			40/**40**			40/**40**	V_{MIN}
	LM2940C, T ≤ 1 ms	55	45		55	45		
Reverse Polarity DC Input Voltage	$R_O = 100\Omega$							
	LM2940, LM2940/883	−30	−15/−**15**	−15/−**15**	−30	−15/−**15**	−15/−**15**	V_{MIN}
	LM2940C	−30	−15		−30	−15		
Reverse Polarity Transient Input Voltage	$R_O = 100\Omega$							
	LM2940, T ≤ 100 ms	−75	−50/−**50**		−75	−50/−**50**		
	LM2940/883, T ≤ 20 ms			−45/−**45**			−45/−**45**	V_{MIN}
	LM2940C, T ≤ 1 ms	−55	−45/−**45**					

Electrical Characteristics

$V_{IN} = V_O + 5V$, $I_O = 1A$, $C_O = 22\ \mu F$, unless otherwise specified. **Boldface limits apply over the entire operating temperature range of the indicated device.** All other specifications apply for $T_A = T_J = 25°C$ (Continued)

Output Voltage (V_O)		9V		10V		
Parameter	**Conditions**	**Typ**	**LM2940 Limit (Note 5)**	**Typ**	**LM2940 Limit (Note 5)**	**Units**
		10.5V ≤ V_{IN} ≤ 26V		**11.5V ≤ V_{IN} ≤ 26V**		
Output Voltage	5 mA ≤ I_O ≤ 1A	9.00	8.73/**8.55** 9.27/**9.45**	10.00	9.70/**9.50** 10.30/**10.50**	V_{MIN} V_{MAX}
Line Regulation	$V_O + 2V \le V_{IN} \le 26V$, $I_O = 5$ mA	20	90	20	100	mV_{MAX}
Load Regulation	50 mA ≤ I_O ≤ 1A LM2940 LM2940C	 60 60	 90/**150** 90	 65	 100/**165**	mV_{MAX}
Output Impedance	100 mADC and 20 mArms, $f_O = 120$ Hz	60		65		mΩ
Quiescent Current	$V_O + 2V \le V_{IN} < 26V$, $I_O = 5$ mA LM2940 LM2940C	 10 10	 15/**20** 15	 10	 15/**20**	mA_{MAX}
	$V_{IN} = V_O + 5V$, $I_O = 1A$	30	45/**60**	30	45/**60**	mA_{MAX}
Output Noise Voltage	10 Hz − 100 kHz, $I_O = 5$ mA	270		300		μV_{rms}
Ripple Rejection	$f_O = 120$ Hz, 1 V_{rms}, $I_O = 100$ mA LM2940 LM2940C	 64 64	 52/**46** 52	 63	 51/**45**	dB_{MIN}
Long Term Stability		34		36		mV/ 1000 Hr
Dropout Voltage	$I_O = 1A$	0.5	0.8/**1.0**	0.5	0.8/**1.0**	V_{MAX}
	$I_O = 100$ mA	110	150/**200**	110	150/**200**	mV_{MAX}
Short Circuit Current	(Note 7)	1.9	1.6	1.9	1.6	A_{MIN}
Maximum Line Transient	$R_O = 100\Omega$ T ≤ 100 ms LM2940 LM2940C	 75 55	 60/**60** 45	 75	 60/**60**	V_{MIN}
Reverse Polarity DC Input Voltage	$R_O = 100\Omega$ LM2940 LM2940C	 −30 −30	 −15/−**15** −15	 −30	 −15/−**15**	V_{MIN}
Reverse Polarity Transient Input Voltage	$R_O = 100\Omega$ T ≤ 100 ms LM2940 LM2940C	 −75 −55	 −50/−**50** −45/−**45**	 −75	 −50/−**50**	V_{MIN}

3

Electrical Characteristics $V_{IN} = V_O + 5V$, $I_O = 1A$, $C_O = 22\ \mu F$, unless otherwise specified. **Boldface limits apply over the entire operating temperature range of the indicated device.** All other specifications apply for $T_A = T_J = 25°C$ (Continued)

Output Voltage (V_O)		12V			15V			
Parameter	**Conditions**	**Typ**	**LM2940 Limit (Note 5)**	**LM2940/833 Limit (Note 6)**	**Typ**	**LM2940 Limit (Note 5)**	**LM2940/833 Limit (Note 6)**	**Units**
		$13.6V \le V_{IN} \le 26V$			$16.75V \le V_{IN} \le 26V$			
Output Voltage	$5\ mA \le I_O \le 1A$	12.00	11.64/**11.40** 12.36/**12.60**	11.64/**11.40** 12.36/**12.60**	15.00	14.55/**14.25** 15.45/**15.75**	14.55/**14.25** 15.45/**15.75**	V_{MIN} V_{MAX}
Line Regulation	$V_O + 2V \le V_{IN} \le 26V$, $I_O = 5\ mA$	20	120	75/**120**	20	150	95/**150**	mV_{MAX}
Load Regulation	$50\ mA \le I_O \le 1A$ LM2940, LM2940/883 LM2940C	 55 55	 120/**200** 120	 120/**190**	 70	 150	 150/**240**	 mV_{MAX}
Output Impedance	100 mADC and 20 mArms, $f_O = 120\ Hz$	80		1000/**1000**	100		1000/**1000**	mΩ
Quiescent Current	$V_O + 2V \le V_{IN} \le 26V$, $I_O = 5\ mA$ LM2940, LM2940/883 LM2940C	 10 10	 15/**20** 15	 15/**20**	 10	 15	 15/**20**	 mA_{MAX}
	$V_{IN} = V_O + 5V$, $I_O = 1A$	30	45/**60**	50/**60**	30	45/**60**	50/**60**	mA_{MAX}
Output Noise Voltage	10 Hz – 100 kHz, $I_O = 5\ mA$	360		1000/**1000**	450		1000/**1000**	μV_{rms}
Ripple Rejection	$f_O = 120\ Hz$, 1 V_{rms}, $I_O = 100\ mA$ LM2940 LM2940C	 66 66	 54/**48** 54	 	 64	 52	 	 dB_{MIN}
	$f_O = 1\ kHz$, 1 V_{rms}, $I_O = 5\ mA$			52/**46**			48/**42**	dB_{MIN}
Long Term Stability		48			60			mV/ 1000 Hr
Dropout Voltage	$I_O = 1A$	0.5	0.8/**1.0**	0.7/**1.0**	0.5	0.8/**1.0**	0.7/**1.0**	V_{MAX}
	$I_O = 100\ mA$	110	150/**200**	150/**200**	110	150/**200**	150/**200**	mV_{MAX}
Short Circuit Current	(Note 7)	1.9	1.6	1.6/**1.3**	1.9	1.6	1.6/**1.3**	A_{MIN}
Maximum Line Transient	$R_O = 100\Omega$ LM2940, $T \le 100\ ms$ LM2940/883, $T \le 20\ ms$ LM2940C, $T \le 1\ ms$	 75 55	 60/**60** 45	 40/**40**	 55	 45	 40/**40**	 V_{MIN}
Reverse Polarity DC Input Voltage	$R_O = 100\Omega$ LM2940, LM2940/883 LM2940C	 −30 −30	 −15/−**15** −15	 −15/−**15**	 −30	 −15	 −15/−**15**	 V_{MIN}
Reverse Polarity Transient Input Voltage	$R_O = 100\Omega$ LM2940, $T \le 100\ ms$ LM2940/883, $T \le 20\ ms$ LM2940C, $T \le 1\ ms$	 −75 −55	 −50/−**50** −45/−**45**	 −45/−**45**	 −55	 −45/−**45**	 −45/−**45**	 V_{MIN}

Note 1: Absolute Maximum Ratings are limits beyond which damage to the device may occur. Operating Conditions are conditions under which the device functions but the specifications might not be guaranteed. For guaranteed specifications and test conditions see the Electrical Characteristics.

Note 2: Military specifications complied with RETS/SMD at the time of printing. For current specifications refer to RETS LM2940K-5.0, LM2940K-8.0, LM2940K-12, and LM2940K-15. SMD numbers are 5962-8958701YA(5V), 5962-9083301YA(8V), 5962-9088401YA(12V), and 5962-9088501YA(15V).

Note 3: The maximum power dissipation is a function of the maximum junction temperature, T_J = 150°C, the junction-to-ambient thermal resistance, θ_{JA}, and the ambient temperature, T_A. The maximum allowable power dissipation at any ambient temperature is $P_{DMAX} = (150 - T_A)/\theta_{JA}$. If this dissipation is exceeded, the die temperature will rise above 150°C and the LM2940 will go into thermal shutdown. For the LM2940T and LM2940CT, the junction-to-ambient thermal resistance (θ_{JA}) is 53°C/W. When using a heatsink, θ_{JA} is the sum of the 3°C/W junction-to-case thermal resistance (θ_{JC}) of the LM2940T or LM2940CT and the case-to-ambient thermal resistance of the heatsink. If the TO-263 package is used, the thermal resistance can be used by increasing the P.C. board copper area thermally connected to the package. Using 0.5 square inches of copper area, θ_{JA} is 50°C/W; with 1 square inch of copper area, θ_{JA} is 37°C/W; and with 1.6 or more square inches of copper area , θ_{JA} is 32°C/W. For the LM2940K, θ_{JA} is 39°C/W and θ_{JC} is 4°C/W.

Note 4: ESD rating is based on the human body model, 100 pF discharged through 1.5 kΩ.

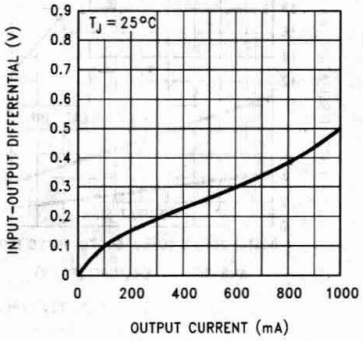
Note 5: All limits are guaranteed at $T_A = T_J$ = 25°C only (standard typeface) or over the entire operating temperature range of the indicated device (**boldface type**). All limits at $T_A = T_J$ = 25°C are 100% production tested. All limits at temperature extremes are guaranteed via correlation using standard Statistical Quality Control methods.

Note 6: All limits are guaranteed at $T_A = T_J$ = 25°C only (standard typeface) or over the entire operating temperature range of the indicated device (**boldface type**). All limits are 100% production tested and are used to calculate Outgoing Quality Levels.

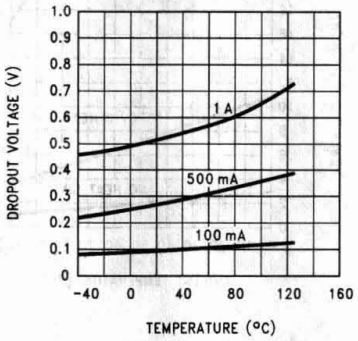
Note 7: Output current will decrease with increasing temperature but will not drop below 1A at the maximum specified temperature.

Typical Performance Characteristics

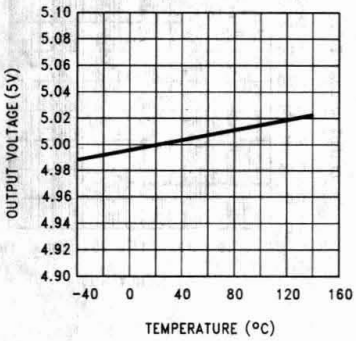
Dropout Voltage



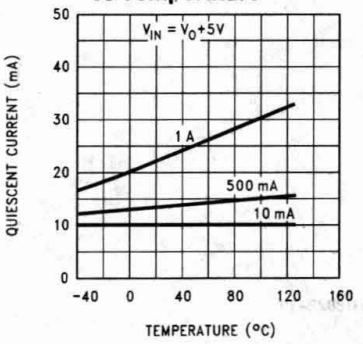
Dropout Voltage vs Temperature



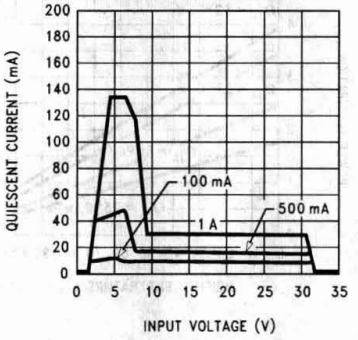
Output Voltage vs Temperature



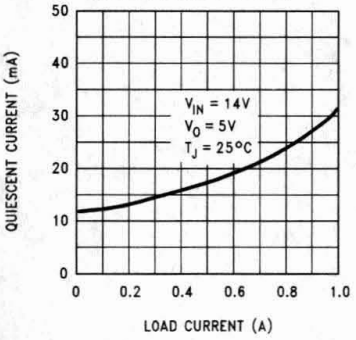
Quiescent Current vs Temperature



Quiescent Current



Quiescent Current



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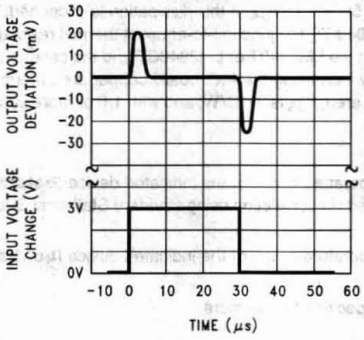
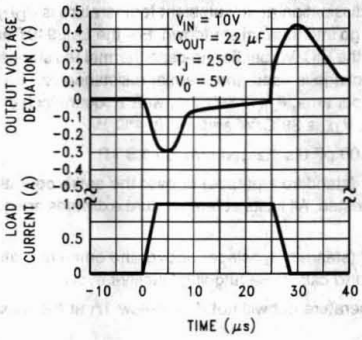
Typical Performance Characteristics (Continued)

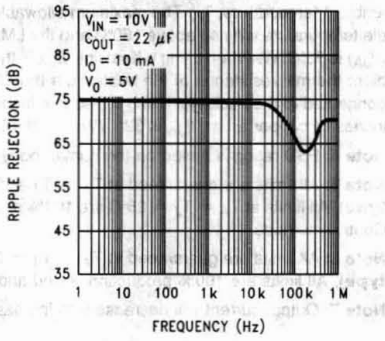
Line Transient Response



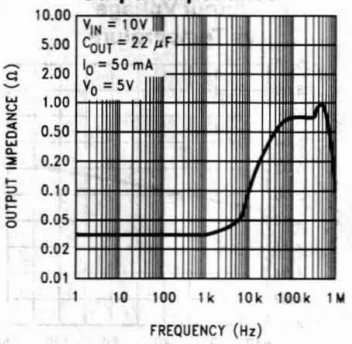
Load Transient Response



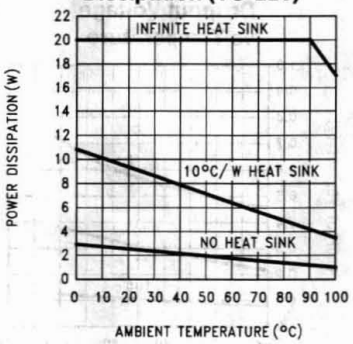
Ripple Rejection



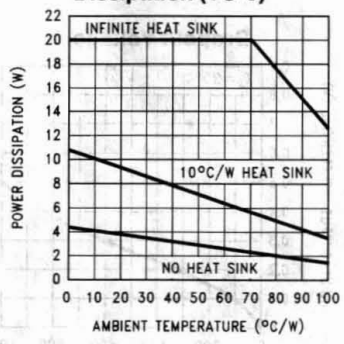
Output Impedance



Maximum Power Dissipation (TO-220)



Maximum Power Dissipation (TO-3)



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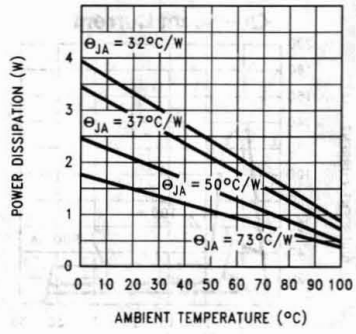
Maximum Power Dissipation (TO-263) (See Note 3)



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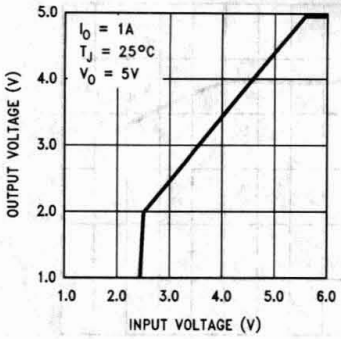
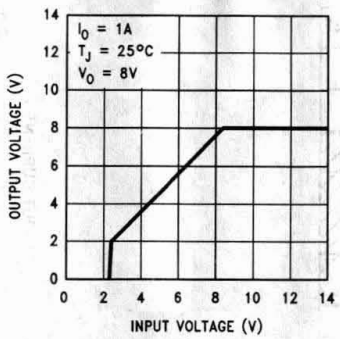
Typical Performance Characteristics (Continued)

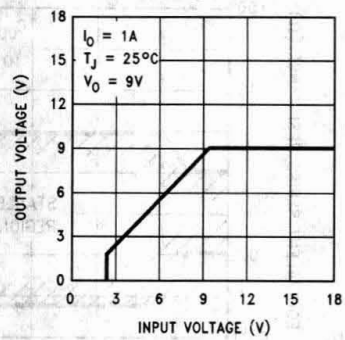
Low Voltage Behavior



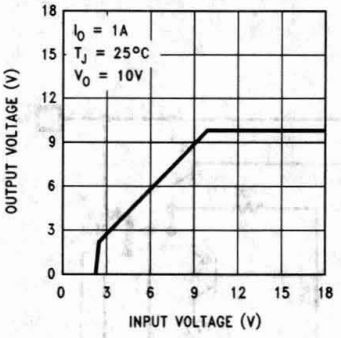
Low Voltage Behavior



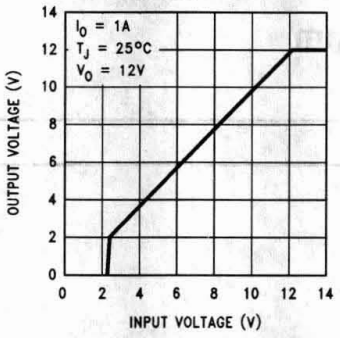
Low Voltage Behavior



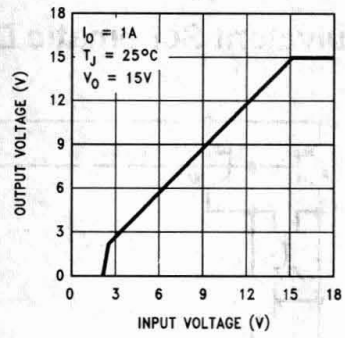
Low Voltage Behavior



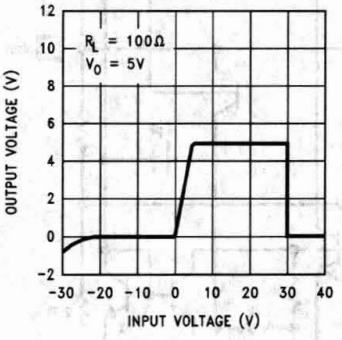
Low Voltage Behavior



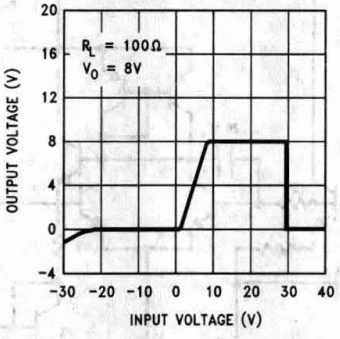
Low Voltage Behavior



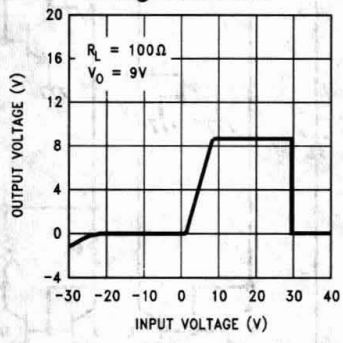
Output at Voltage Extremes



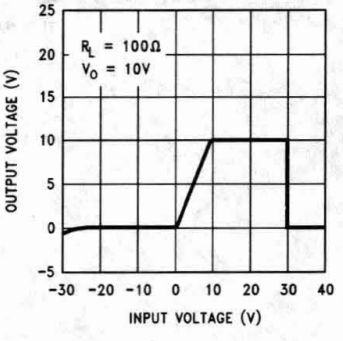
Output at Voltage Extremes



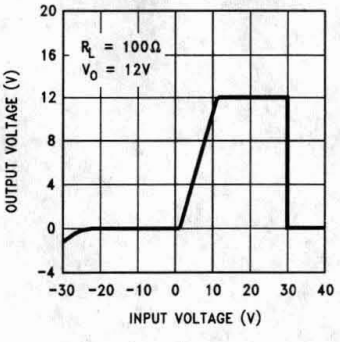
Output at Voltage Extremes



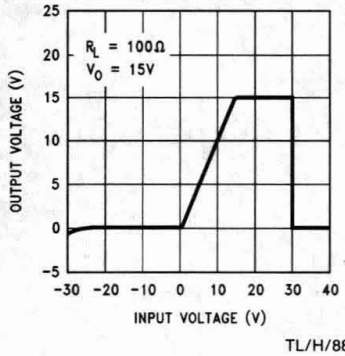
Output at Voltage Extremes



Output at Voltage Extremes



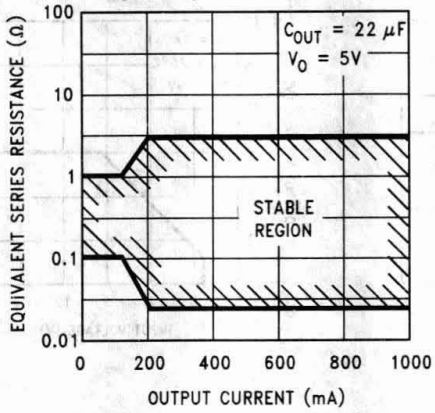
Output at Voltage Extremes



TL/H/8822–5

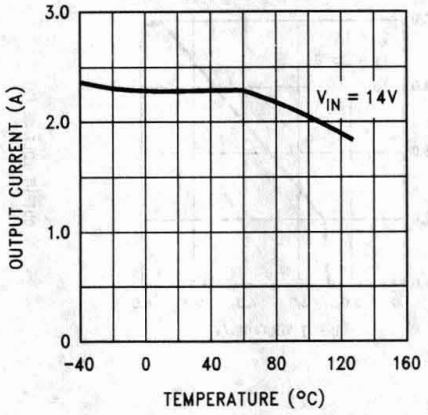
Typical Performance Characteristics (Continued)

Output Capacitor ESR



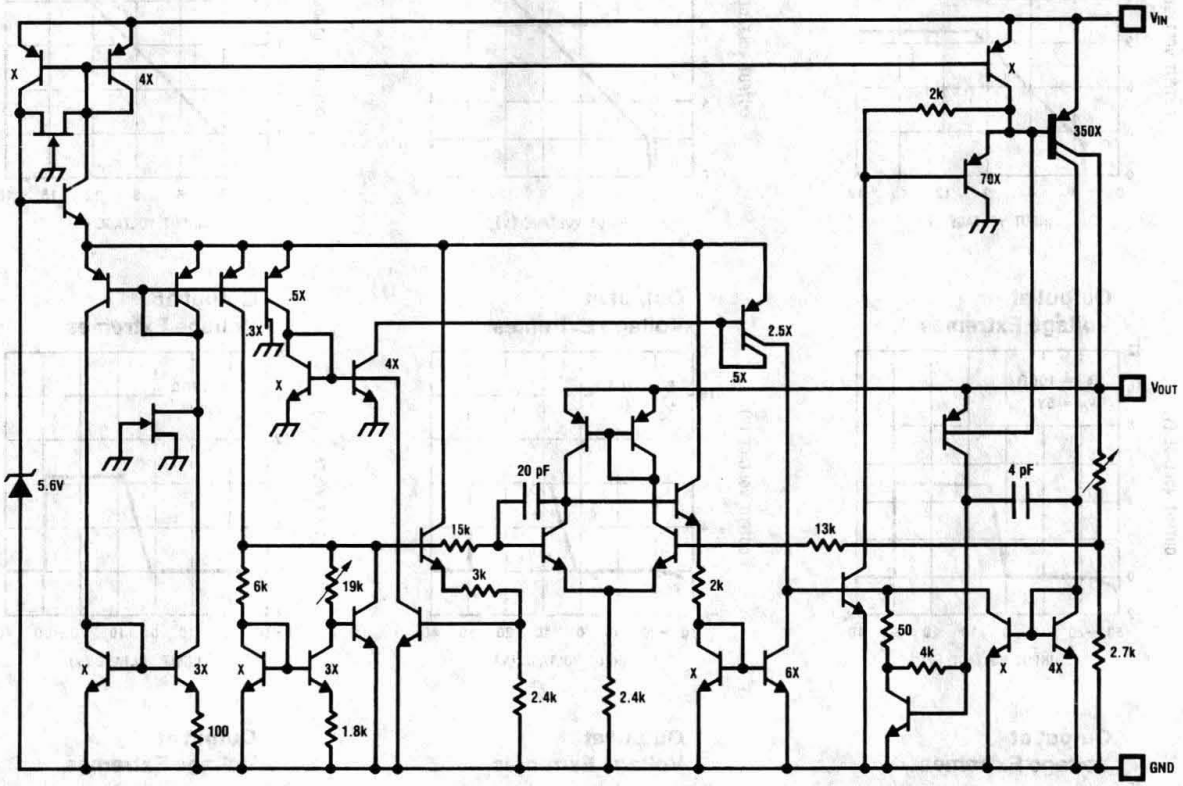
TL/H/8822–6

Peak Output Current



TL/H/8822–8

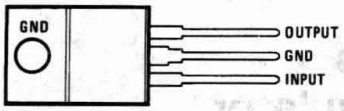
Equivalent Schematic Diagram



TL/H/8822–1

Connection Diagrams

(TO-220) Plastic Package

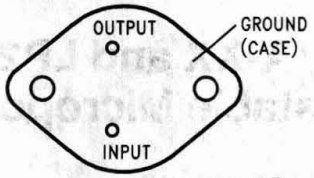


TL/H/8822–2

Front View

Order Number LM2940CT-5.0, LM2940CT-9.0, LM2940CT-12, LM2940CT-15, LM2940T-5.0, LM2940T-8.0, LM2940T-9.0, LM2940T-10 or LM2940T-12
See NS Package Number TO3B

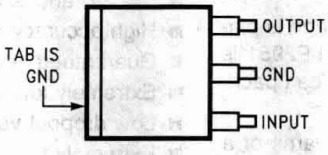
TO-3 Metal Can Package (K)



TL/H/8822–7

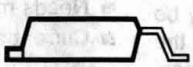
Bottom View
Order Number LM2940K-5.0/883, LM2940K-8.0/883, LM2940K-12/883, LM2940K-15/883
See NS Package Number K02A

(TO-263) Surface-Mount Package



TL/H/8822–11

Top View



TL/H/8822–12

Side View

Order Number LM2940CS-5.0, LM2940CS-9.0, LM2940CS-12, LM2940CS-15, LM2940S-5.0, LM2940S-8.0, LM2940S-9.0, LM2940S-10 or LM2940S-12
See NS Package Number TS3B

National Semiconductor

LP2950/A-XX and LP2951/A-XX Series of Adjustable Micropower Voltage Regulators

General Description

The LP2950 and LP2951 are micropower voltage regulators with very low quiescent current (75 μA typ.) and very low dropout voltage (typ. 40 mV at light loads and 380 mV at 100 mA). They are ideally suited for use in battery-powered systems. Furthermore, the quiescent current of the LP2950/LP2951 increases only slightly in dropout, prolonging battery life.

The LP2950-5.0 in the popular 3-pin TO-92 package is pin-compatible with older 5V regulators. The 8-lead LP2951 is available in plastic, ceramic dual-in-line, or metal can packages and offers additional system functions.

One such feature is an error flag output which warns of a low output voltage, often due to falling batteries on the input. It may be used for a power-on reset. A second feature is the logic-compatible shutdown input which enables the regulator to be switched on and off. Also, the part may be pin-strapped for a 5V, 3V, or 3.3V output (depending on the version), or programmed from 1.24V to 29V with an external pair of resistors.

Careful design of the LP2950/LP2951 has minimized all contributions to the error budget. This includes a tight initial tolerance (.5% typ.), extremely good load and line regulation (.05% typ.) and a very low output voltage temperature coefficient, making the part useful as a low-power voltage reference.

Features

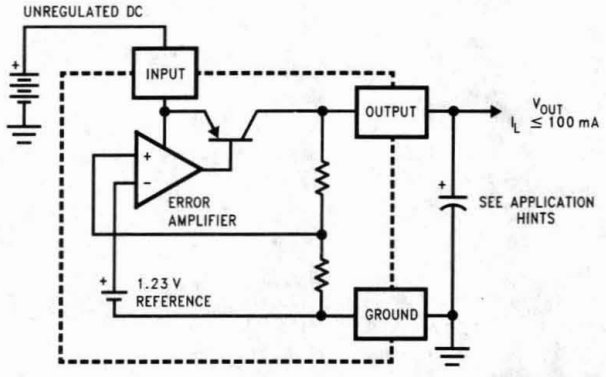
- 5V, 3V, and 3.3V versions available
- High accuracy output voltage
- Guaranteed 100 mA output current
- Extremely low quiescent current
- Low dropout voltage
- Extremely tight load and line regulation
- Very low temperature coefficient
- Use as Regulator or Reference
- Needs minimum capacitance for stability
- Current and Thermal Limiting

LP2951 versions only

- Error flag warns of output dropout
- Logic-controlled electronic shutdown
- Output programmable from 1.24 to 29V

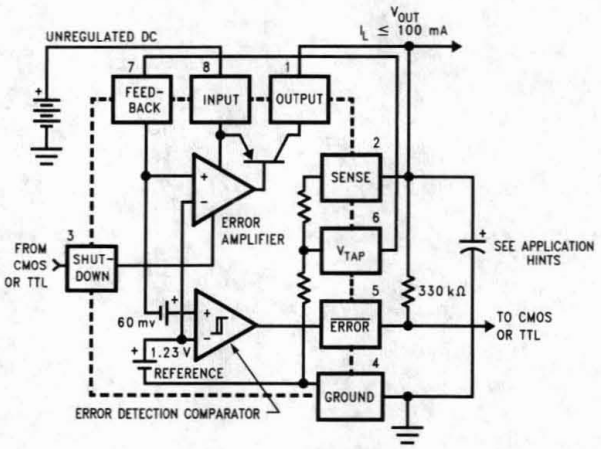
Block Diagram and Typical Applications

LP2950/A-XX



TL/H/8546–25

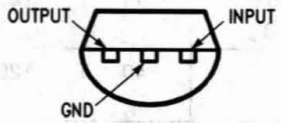
LP2951/A-XX



TL/H/8546–1

Connection Diagrams

TO-92 Plastic Package (Z)

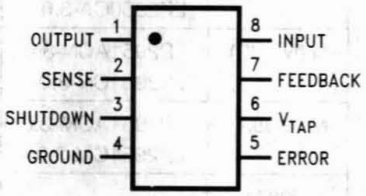


TL/H/8546–2

Bottom View

Order Number LP2950ACZ-3.0, LP2950CZ-3.0, LP2950ACZ-3.3, LP2950CZ-3.3 LP2950ACZ-5.0 or LP2950CZ-5.0
See NS Package Number Z03A

Dual-In-Line Packages (N, J)
Surface-Mount Package (M)



TL/H/8546–26

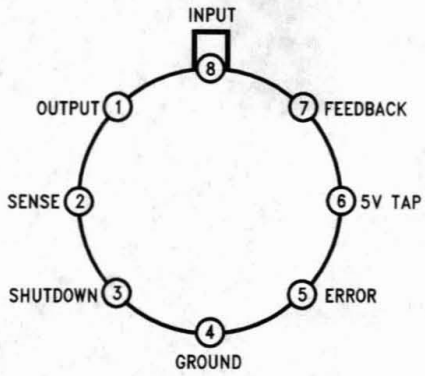
Top View

Order Number LP2951CJ, LP2951ACJ, LP2951J, LP2951J/883 or 5962-3870501MPA
See NS Package Number J08A

Order Number LP2951ACN, LP2951CN, LP2951ACN-3.0, LP2951CN-3.0, LP2951ACN-3.3 or LP2951CN-3.3
See NS Package Number N08E

Order Number LP2951ACM, LP2951CM, LP2951ACM-3.0, LP2951CM-3.0, LP2951ACM-3.3 or LP2951CM-3.3
See NS Package Number M08A

Metal Can Package (H)

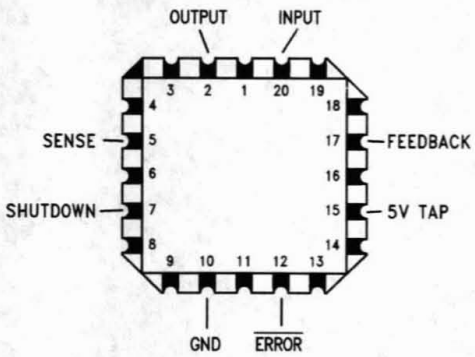


TL/H/8546–19

Top View

Order Number LP2951H/883 or 5962-3870501MGA
See NS Package Number H08C

Leadless Chip Carrier (E)



TL/H/8546–24

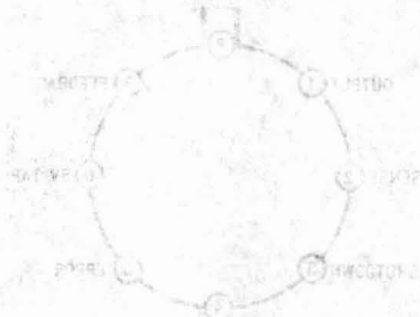
Top View

Order Number LP2951E/883 or 5962-3870501M2A
See NS Package Number E20A

3

Ordering Information

Package	Output Voltage			Temperature (°C)
	3.0V	3.3V	5.0V	
TO-92 (Z)	LP2950ACZ-3.0 LP2950CA-3.0	LP2950ACZ-3.3 LP2950CZ-3.3	LP2950ACZ-5.0 LP2950CZ-5.0	$-40 < T_J < 125$
N (N-08E)	LP2951ACN-3.0 LP2951CN-3.0	LP2951ACN-3.3 LP2951CN-3.3	LP2951ACN LP2950CN	$-40 < T_J < 125$
M (M08A)	LP2951ACM-3.0 LP2951CM-3.0	LP2951ACM-3.3 LP2951CM-3.3	LP2951ACM LP2951CM	$-40 < T_J < 125$
J (J08A)			LP2951ACJ LP2951CJ	$-40 < T_J < 125$
			LP2951J LP2951J/883 5926-3870501MPA	$-55 < T_J < 150$
H (H08C)			LP2951H/883 5962-3870501MGA	$-55 < T_J < 150$
E (E20A)			LP2951E/883 5962-3870501M2A	$-55 < T_J < 150$



Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Power Dissipation	Internally Limited
Lead Temp. (Soldering, 5 seconds)	260°C
Storage Temperature Range	−65° to +150°C
Operating Junction Temperature Range (Note 8)	
LP2951	−55° to +150°C
LP2950AC-XX, LP2950C-XX, LP2951AC-XX, LP2951C-XX	−40° to +125°C
Input Supply Voltage	−0.3 to +30V
Feedback Input Voltage (Notes 9 and 10)	−1.5 to +30V
Shutdown Input Voltage (Note 9)	−0.3 to +30V
Error Comparator Output Voltage (Note 9)	−0.3 to +30V
ESD Rating is to be determined.	

Electrical Characteristics (Note 1)

Parameter	Conditions (Note 2)	LP2951		LP2950AC-XX LP2951AC-XX			LP2950C-XX LP2951C-XX			Units
		Typ	Tested Limit (Notes 3, 16)	Typ	Tested Limit (Note 3)	Design Limit (Note 4)	Typ	Tested Limit (Note 3)	Design Limit (Note 4)	
3V VERSIONS (Note 17)										
Output Voltage	T_J = 25°C	3.0	3.015 2.985	3.0	3.015 2.985		3.0	3.030 2.970		V max V min
	−25°C ≤ T_J ≤ 85°C	3.0		3.0		3.030 2.970	3.0		3.045 2.955	V max V min
	Full Operating Temperature Range	3.0	**3.036** **2.964**	3.0		**3.036** **2.964**	3.0		**3.060** **2.940**	V max V min
Output Voltage	100 μA ≤ I_L ≤ 100 mA T_J ≤ T_{JMAX}	3.0	**3.045** **2.955**	3.0		**3.042** **2.958**	3.0		**3.072** **2.928**	V max V min
3.3V VERSIONS (Note 17)										
Output Voltage	T_J = 25°C	3.3	3.317 3.284	3.3	3.317 3.284		3.3	3.333 3.267		V max V min
	−25°C ≤ T_J ≤ 85°C	3.3		3.3		3.333 3.267	3.3		3.350 3.251	V max V min
	Full Operating Temperature Range	3.3	**3.340** **3.260**	3.3		**3.340** **3.260**	3.3		**3.366** **3.234**	V max V min
Output Voltage	100 μA ≤ I_L ≤ 100 mA T_J ≤ T_{JMAX}	3.3	**3.350** **3.251**	3.3		**3.346** **3.254**	3.3		**3.379** **3.221**	V max V min
5V VERSIONS (Note 17)										
Output Voltage	T_J = 25°C	5.0	5.025 4.975	5.0	5.025 4.975		5.0	5.05 4.95		V max V min
	−25°C ≤ T_J ≤ 85°C	5.0		5.0		5.05 4.95	5.0		5.075 4.925	V max V min
	Full Operating Temperature Range	5.0	**5.06** **4.94**	5.0		**5.06** **4.94**	5.0		**5.1** **4.9**	V max V min
Output Voltage	100 μA ≤ I_L ≤ 100 mA T_J ≤ T_{JMAX}	5.0	**5.075** **4.925**	5.0		**5.075** **4.925**	5.0		**5.12** **4.88**	V max V min
ALL VOLTAGE OPTIONS										
Output Voltage Temperature Coefficient	(Note 12)	**20**	**120**	**20**		**100**	**50**		**150**	ppm/°C
Line Regulation (Note 14)	(V_ONOM + 1)V ≤ V_{in} ≤ 30V (Note 15)	0.03	0.1 **0.5**	0.03	0.1	 **0.2**	0.04	0.2	 **0.4**	% max % max
Load Regulation (Note 14)	100 μA ≤ I_L ≤ 100 mA	0.04	0.1 **0.3**	0.04	0.1	 **0.2**	0.1	0.2	 **0.3**	% max % max

Electrical Characteristics (Note 1) (Continued)

Parameter	Conditions (Note 2)	LP2951		LP2950AC-XX LP2951AC-XX			LP2950C-XX LP2951C-XX			Units
		Typ	Tested Limit (Notes 3, 16)	Typ	Tested Limit (Note 3)	Design Limit (Note 4)	Typ	Tested Limit (Note 3)	Design Limit (Note 4)	
ALL VOLTAGE OPTIONS (Continued)										
Dropout Voltage (Note 5)	I_L = 100 μA	50	80 **150**	50	80	 **150**	50	80	 **150**	mV max mV max
	I_L = 100 mA	380	450 **600**	380	450	 **600**	380	450	 **600**	mV max mV max
Ground Current	I_L = 100 μA	75	120 **140**	75	120	 **140**	75	120	 **140**	μA max μA max
	I_L = 100 mA	8	12 **14**	8	12	 **14**	8	12	 **14**	mA max mA max
Dropout Ground Current	V_{in} = (V_ONOM − 0.5)V I_L = 100 μA	110	170 **200**	110	170	 **200**	110	170	 **200**	μA max μA max
Current Limit	V_{out} = 0	160	200 **220**	160	200	 **220**	160	200	 **220**	mA max mA max
Thermal Regulation	(Note 13)	0.05	0.2	0.05	0.2		0.05	0.2		%/W max
Output Noise, 10 Hz to 100 KHz	C_L = 1 μF (5V Only)	430		430			430			μV rms
	C_L = 200 μF	160		160			160			μV rms
	C_L = 3.3 μF (Bypass = 0.01 μF Pins 7 to 1 (LP2951))	100		100			100			μV rms
8-PIN VERSIONS ONLY		**LP2951**		**LP2951AC-XX**			**LP2951C-XX**			
Reference Voltage		1.235	1.25 **1.26** 1.22 **1.2**	1.235	1.25 1.22 	 **1.26** **1.2**	1.235	1.26 1.21 	 **1.27** **1.2**	V max V max V min V min
Reference Voltage	(Note 7)		**1.27** **1.19**			**1.27** **1.19**			**1.285** **1.185**	V max V min
Feedback Pin Bias Current		20	40 **60**	20	40	 **60**	20	40	 **60**	nA max nA max
Reference Voltage Temperature Coefficient	(Note 12)	20		20			50			ppm/°C
Feedback Pin Bias Current Temperature Coefficient		0.1		0.1			0.1			nA/°C
Error Comparator										
Output Leakage Current	V_{OH} = 30V	0.01	1 **2**	0.01	1	 **2**	0.01	1	 **2**	μA max μA max
Output Low Voltage	V_{in} = (V_ONOM − 0.5)V I_{OL} = 400 μA	150	250 **400**	150	250	 **400**	150	250	 **400**	mV max mV max
Upper Threshold Voltage	(Note 6)	60	40 **25**	60	40	 **25**	60	40	 **25**	mV min mV min
Lower Threshold Voltage	(Note 6)	75	95 **140**	75	95	 **140**	75	95	 **140**	mV max mV max
Hysteresis	(Note 6)	15		15			15			mV

Electrical Characteristics (Note 1) (Continued)

Parameter	Conditions (Note 2)	LP2951		LP2951AC-XX			LP2951C-XX			Units
		Typ	Tested Limit (Notes 3, 16)	Typ	Tested Limit (Note 3)	Design Limit (Note 4)	Typ	Tested Limit (Note 3)	Design Limit (Note 4)	
8-PIN VERSIONS ONLY (Continued)										
Shutdown Input										
Input Logic Voltage	Low (Regulator ON)	1.3	**0.6**	1.3		**0.7**	1.3		**0.7**	V V max
	High (Regulator OFF)		**2.0**			**2.0**			**2.0**	V min
Shutdown Pin Input Current	$V_{shutdown}$ = 2.4V	30	50 **100**	30	50	**100**	30	50	**100**	μA max μA max
	$V_{shutdown}$ = 30V	450	600 **750**	450	600	**750**	450	600	**750**	μA max μA max
Regulator Output Current in Shutdown	(Note 11)	3	10 **20**	3	10	**20**	3	10	**20**	μA max μA max

Note 1: Boldface limits apply at temperature extremes.

Note 2: Unless otherwise specified all limits guaranteed for T_J = 25°C, V_{in} = (V_ONOM + 1)V, I_L = 100 μA and C_L = 1 μF for 5V versions, and 2.2 μF for 3V and 3.3V versions. Additional conditions for the 8-pin versions are Feedback tied to V_{TAP}, Output tied to Output Sense and $V_{shutdown} \leq$ 0.8V.

Note 3: Guaranteed and 100% production tested.

Note 4: Guaranteed but not 100% production tested. These limits are not used to calculate outgoing AQL levels.

Note 5: Dropout Voltage is defined as the input to output differential at which the output voltage drops 100 mV below its nominal value measured at 1V differential. At very low values of programmed output voltage, the minimum input supply voltage of 2V **(2.3V over temperature)** must be taken into account.

Note 6: Comparator thresholds are expressed in terms of a voltage differential at the Feedback terminal below the nominal reference voltage measured at V_{in} = (V_ONOM + 1)V. To express these thresholds in terms of output voltage change, multiply by the error amplifier gain = V_{out}/V_{ref} = (R1 + R2)/R2. For example, at a programmed output voltage of 5V, the Error output is guaranteed to go low when the output drops by 95 mV × 5V/1.235V = 384 mV. Thresholds remain constant as a percent of V_{out} as V_{out} is varied, with the dropout warning occurring at typically 5% below nominal, 7.5% guaranteed.

Note 7: $V_{ref} \leq V_{out} \leq (V_{in} - 1V)$, 2.3V $\leq V_{in} \leq$ 30V, 100 μA $\leq I_L \leq$ 100 mA, $T_J \leq T_{JMAX}$.

Note 8: The junction-to-ambient thermal resistance of the TO-92 package is 180°C/W with 0.4″ leads and 160°C/W with 0.25″ leads to a PC board. The thermal resistance of the 8-pin DIP packages is 105°C/W for the molded plastic (N) and 130°C/W for the cerdip (J) junction to ambient when soldered directly to a PC board. Thermal resistance for the metal can (H) is 160°C/W junction to ambient and 20°C/W junction to case. Junction to ambient thermal resistance for the S.O. (M) package is 160°C/W. Thermal resistance for the leadless chip carrier (E) package is 95°C/W junction to ambient and 24°C/W junction to case.

Note 9: May exceed input supply voltage.

Note 10: When used in dual-supply systems where the output terminal sees loads returned to a negative supply, the output voltage should be diode-clamped to ground.

Note 11: $V_{shutdown} \geq$ 2V, $V_{in} \leq$ 30V, V_{out} = 0, Feedback pin tied to V_{TAP}.

Note 12: Output or reference voltage temperature coefficient is defined as the worst case voltage change divided by the total temperature range.

Note 13: Thermal regulation is defined as the change in output voltage at a time T after a change in power dissipation is applied, excluding load or line regulation effects. Specifications are for a 50 mA load pulse at V_{IN} = 30V (1.25W pulse) for T = 10 ms.

Note 14: Regulation is measured at constant junction temperature, using pulse testing with a low duty cycle. Changes in output voltage due to heating effects are covered under the specification for thermal regulation.

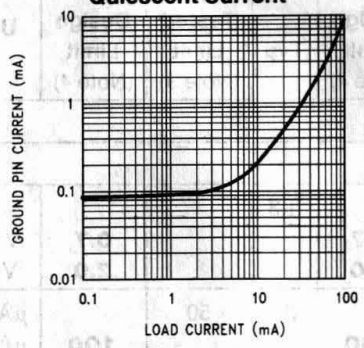
Note 15: Line regulation for the LP2951 is tested at 150°C for I_L = 1 mA. For I_L = 100 μA and T_J = 125°C, line regulation is guaranteed by design to 0.2%. See Typical Performance Characteristics for line regulation versus temperature and load current.

Note 16: A Military RETS spec is available on request. At time of printing, the LP2951 RETS spec complied with the boldface limits in this column. The LP2951H, E, or J may also be procured as Standard Military Drawing Spec #5962-3870501MGA, M2A, or MPA.

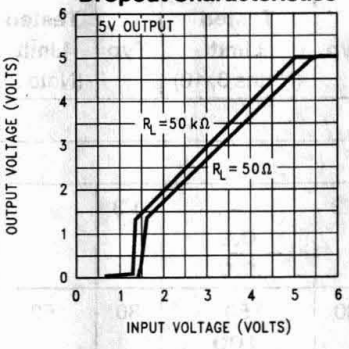
Note 17: All LP2950 devices have the nominal output voltage coded as the last two digits of the part number. In the LP2951 products, the 3.0V and 3.3V versions are designated by the last two digits, but the 5V version is denoted with no code at this location of the part number (refer to ordering information table).

Typical Performance Characteristics

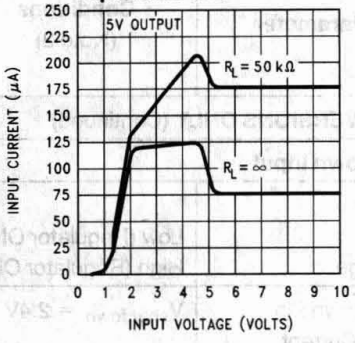
Quiescent Current



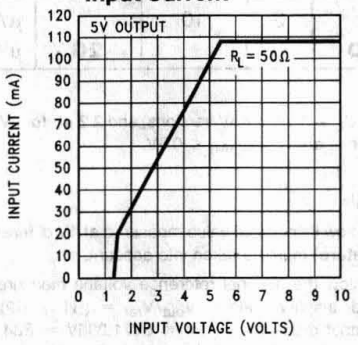
Dropout Characteristics



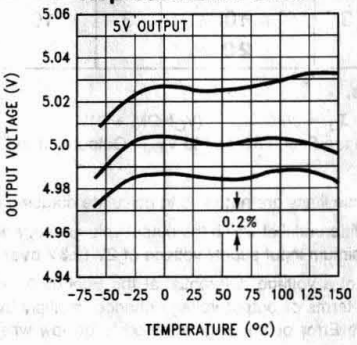
Input Current



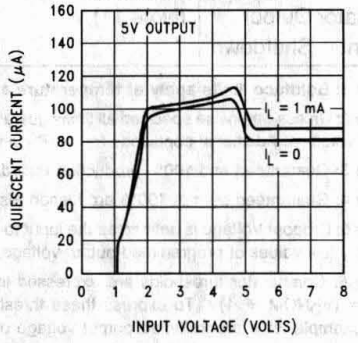
Input Current



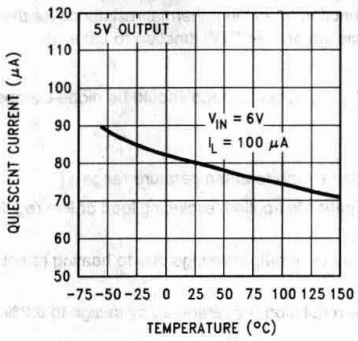
Output Voltage vs. Temperature of 3 Representative Units



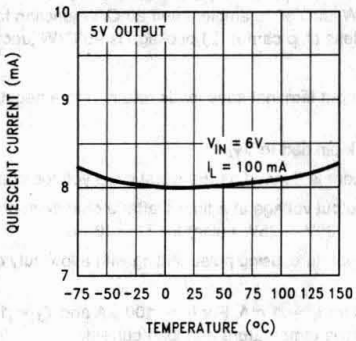
Quiescent Current



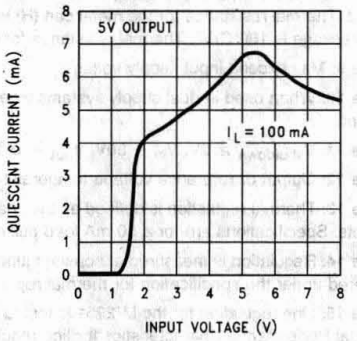
Quiescent Current



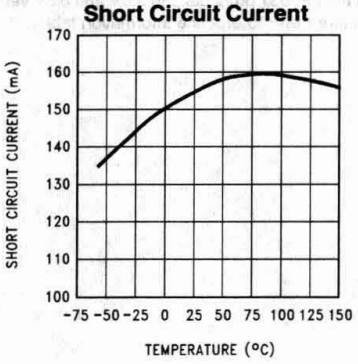
Quiescent Current



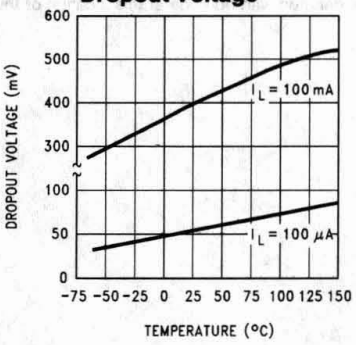
Quiescent Current



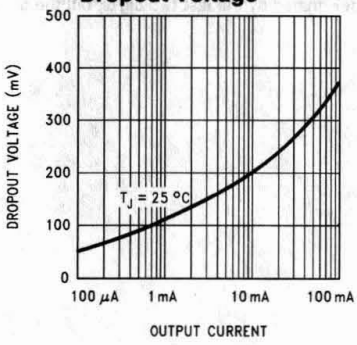
Short Circuit Current



Dropout Voltage



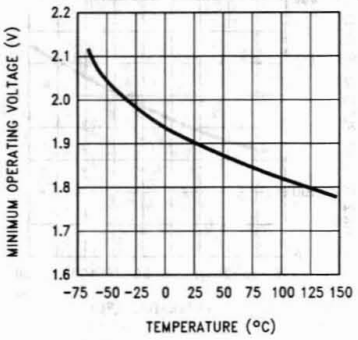
Dropout Voltage



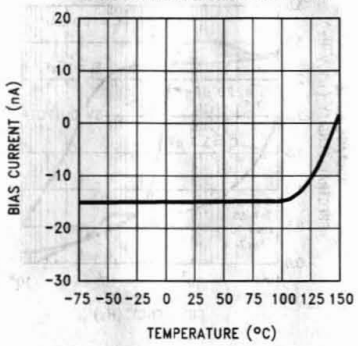
TL/H/8546–3

Typical Performance Characteristics (Continued)

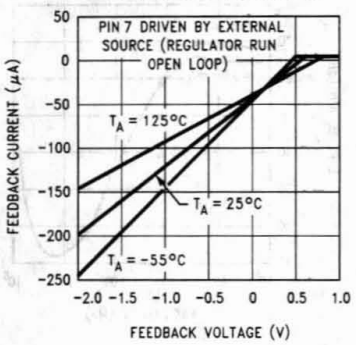
LP2951
Minimum Operating Voltage



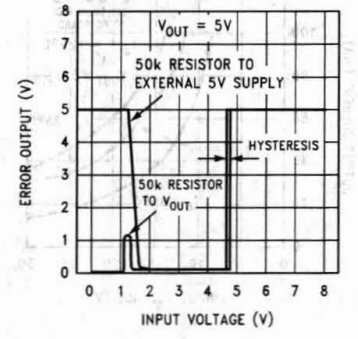
LP2951
Feedback Bias Current



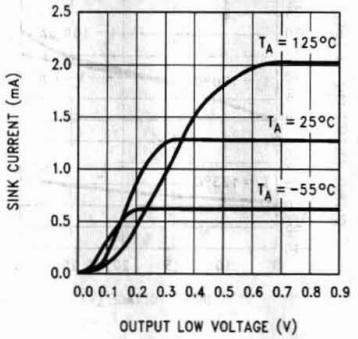
LP2951
Feedback Pin Current



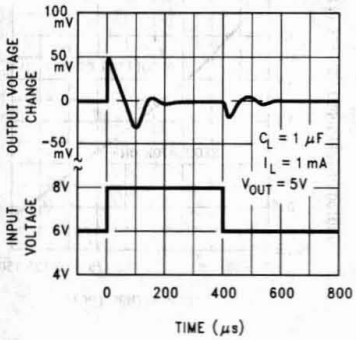
LP2951
Error Comparator Output



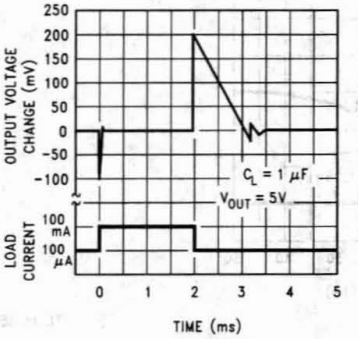
LP2951
Comparator Sink Current



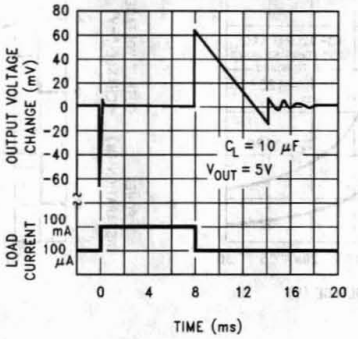
Line Transient Response



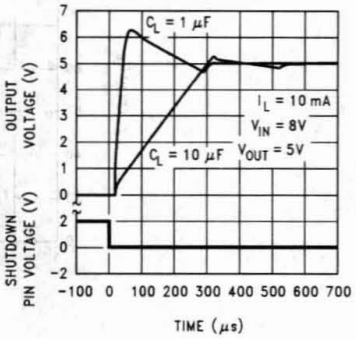
Load Transient Response



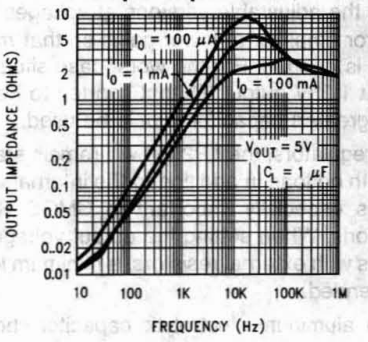
Load Transient Response



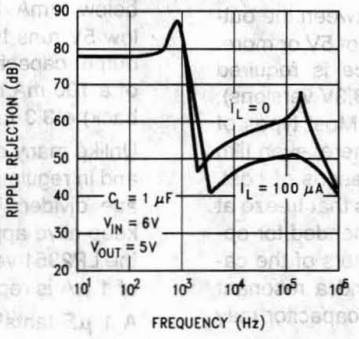
LP2951
Enable Transient



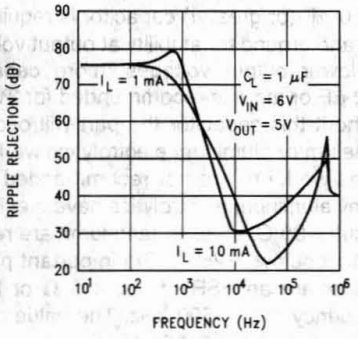
Output Impedance



Ripple Rejection



Ripple Rejection



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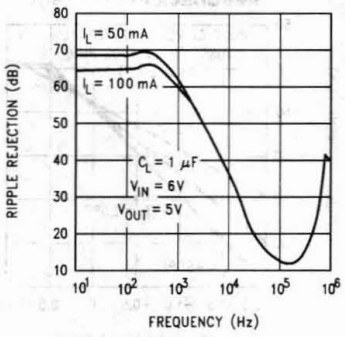
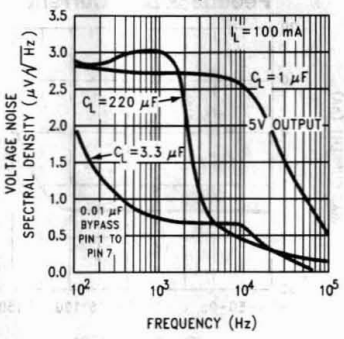
3

Typical Performance Characteristics (Continued)

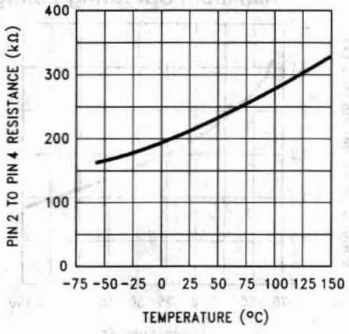
Ripple Rejection



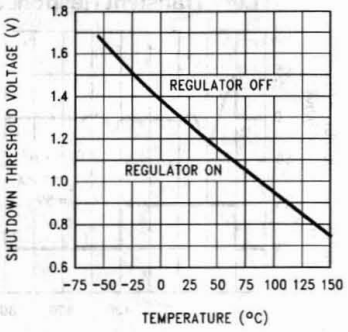
LP2951 Output Noise



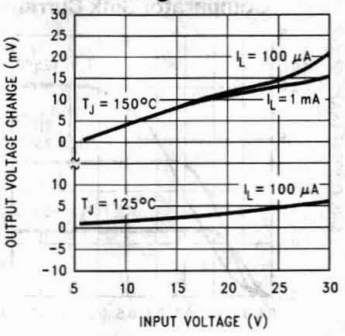
LP2951 Divider Resistance



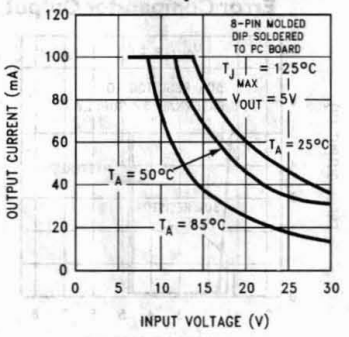
Shutdown Threshold Voltage



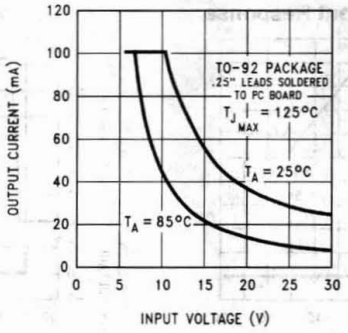
Line Regulation



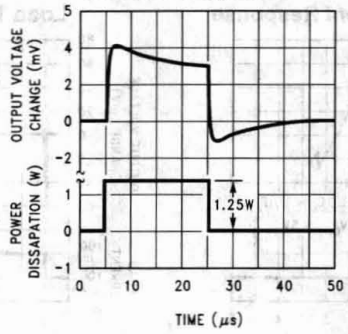
LP2951 Maximum Rated Output Current



LP2950 Maximum Rated Output Current



Thermal Response



TL/H/8546–5

Application Hints

EXTERNAL CAPACITORS

A 1.0 μF (or greater) capacitor is required between the output and ground for stability at output voltages of 5V or more. At lower output voltages, more capacitance is required (2.2 μF or more is recommended for 3V and 3.3V versions). Without this capacitor the part will oscillate. Most types of tantalum or aluminum electrolytics work fine here; even film types work but are not recommended for reasons of cost. Many aluminum electrolytics have electrolytes that freeze at about −30°C, so solid tantalums are recommended for operation below −25°C. The important parameters of the capacitor are an ESR of about 5 Ω or less and a resonant frequency above 500 kHz. The value of this capacitor may be increased without limit.

At lower values of output current, less output capacitance is required for stability. The capacitor can be reduced to 0.33 μF for currents below 10 mA or 0.1 μF for currents below 1 mA. Using the adjustable versions at voltages below 5V runs the error amplifier at lower gains so that *more* output capacitance is needed. For the worst-case situation of a 100 mA load at 1.23V output (Output shorted to Feedback) a 3.3 μF (or greater) capacitor should be used.

Unlike many other regulators, the LP2950 will remain stable and in regulation with no load in addition to the internal voltage divider. This is especially important in CMOS RAM keep-alive applications. When setting the output voltage of the LP2951 versions with external resistors, a minimum load of 1 μA is recommended.

A 1 μF tantalum or aluminum electrolytic capacitor should be placed from the LP2950/LP2951 input to ground if there is more than 10 inches of wire between the input and the AC filter capacitor or if a battery is used as the input.

Application Hints (Continued)

Stray capacitance to the LP2951 Feedback terminal can cause instability. This may especially be a problem when using high value external resistors to set the output voltage. Adding a 100 pF capacitor between Output and Feedback and increasing the output capacitor to at least 3.3 μF will fix this problem.

ERROR DETECTION COMPARATOR OUTPUT

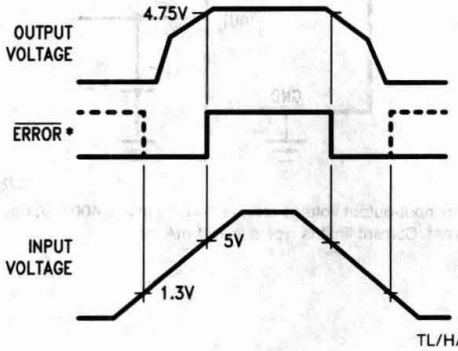
The comparator produces a logic low output whenever the LP2951 output falls out of regulation by more than approximately 5%. This figure is the comparator's built-in offset of about 60 mV divided by the 1.235 reference voltage. (Refer to the block diagram in the front of the datasheet.) This trip level remains "5% below normal" regardless of the programmed output voltage of the 2951. For example, the error flag trip level is typically 4.75V for a 5V output or 11.4V for a 12V output. The out of regulation condition may be due either to low input voltage, current limiting, or thermal limiting.

Figure 1 below gives a timing diagram depicting the $\overline{\text{ERROR}}$ signal and the regulated output voltage as the LP2951 input is ramped up and down. For 5V versions, the $\overline{\text{ERROR}}$ signal becomes valid (low) at about 1.3V input. It goes high at about 5V input (the input voltage at which V_{OUT} = 4.75). Since the LP2951's dropout voltage is load-dependent (see curve in typical performance characteristics), the **input** voltage trip point (about 5V) will vary with the load current. The **output** voltage trip point (approx. 4.75V) does not vary with load.

The error comparator has an open-collector output which requires an external pullup resistor. This resistor may be returned to the output or some other supply voltage depending on system requirements. In determining a value for this resistor, note that while the output is rated to sink 400 μA, this sink current adds to battery drain in a low battery condition. Suggested values range from 100k to 1 MΩ. The resistor is not required if this output is unused.

PROGRAMMING THE OUTPUT VOLTAGE (LP2951)

The LP2951 may be pin-strapped for the nominal fixed output voltage using its internal voltage divider by tying the output and sense pins together, and also tying the feedback and V_{TAP} pins together. Alternatively, it may be programmed for any output voltage between its 1.235V reference and its 30V maximum rating. As seen in *Figure 2,* an external pair of resistors is required.



TL/H/8546–20

*When $V_{IN} \leq$ 1.3V, the error flag pin becomes a high impedance, and the error flag voltage rises to its pull-up voltage. Using V_{OUT} as the pull-up voltage (see *Figure 2*), rather than an external 5V source, will keep the error flag voltage under 1.2V (typ.) in this condition. The user may wish to divide down the error flag voltage using equal-value resistors (10 kΩ suggested), to ensure a low-level logic signal during any fault condition, while still allowing a valid high logic level during normal operation.

FIGURE 1. $\overline{\text{ERROR}}$ Output Timing

The complete equation for the output voltage is

$$V_{OUT} = V_{REF} \bullet \left(1 + \frac{R_1}{R_2}\right) + I_{FB}R_1$$

where V_{REF} is the nominal 1.235 reference voltage and I_{FB} is the feedback pin bias current, nominally −20 nA. The minimum recommended load current of 1 μA forces an upper limit of 1.2 MΩ on the value of R_2, if the regulator must work with no load (a condition often found in CMOS in standby). I_{FB} will produce a 2% typical error in V_{OUT} which may be eliminated at room temperature by trimming R_1. For better accuracy, choosing R_2 = 100k reduces this error to 0.17% while increasing the resistor program current to 12 μA. Since the LP2951 typically draws 60 μA at no load with Pin 2 open-circuited, this is a small price to pay.

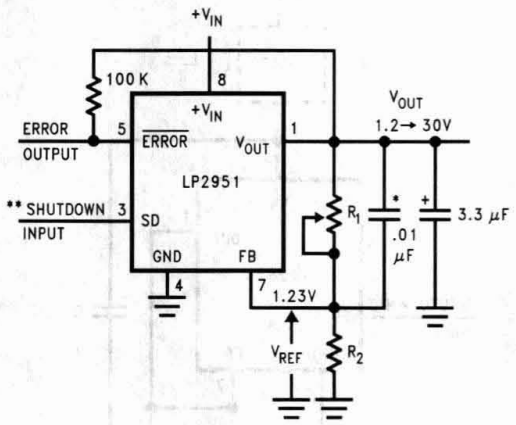
REDUCING OUTPUT NOISE

In reference applications it may be advantageous to reduce the AC noise present at the output. One method is to reduce the regulator bandwidth by increasing the size of the output capacitor. This is the only way noise can be reduced on the 3 lead LP2950 but is relatively inefficient, as increasing the capacitor from 1 μF to 220 μF only decreases the noise from 430 μV to 160 μV rms for a 100 kHz bandwidth at 5V output.

Noise can be reduced fourfold by a bypass capacitor across R_1, since it reduces the high frequency gain from 4 to unity. Pick

$$C_{BYPASS} \cong \frac{1}{2\pi R_1 \bullet 200\ \text{Hz}}$$

or about 0.01 μF. When doing this, the output capacitor must be increased to 3.3 μF to maintain stability. These changes reduce the output noise from 430 μV to 100 μV rms for a 100 kHz bandwidth at 5V output. With the bypass capacitor added, noise no longer scales with output voltage so that improvements are more dramatic at higher output voltages.



TL/H/8546–7

FIGURE 2. Adjustable Regulator

*See Application Hints

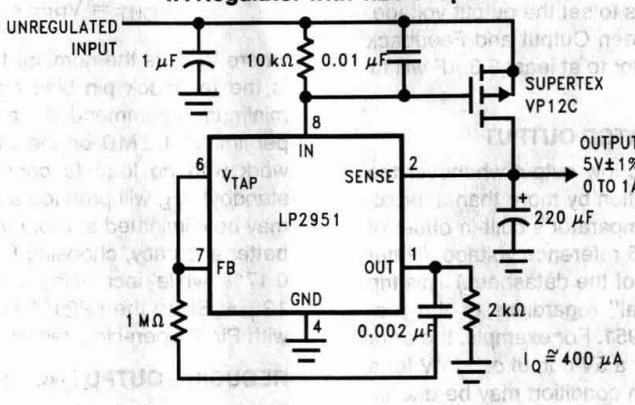
$$V_{out} = V_{Ref}\left(1 + \frac{R_1}{R_2}\right)$$

**Drive with TTL-high to shut down. Ground or leave open if shutdown feature is not to be used.

Note: Pins 2 and 6 are left open.

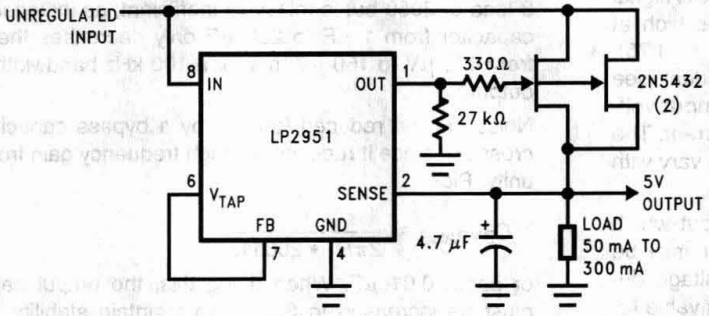
Typical Applications

1A Regulator with 1.2V Dropout



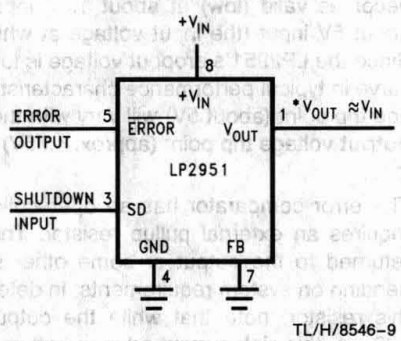
TL/H/8546–22

300 mA Regulator with 0.75V Dropout



TL/H/8546–21

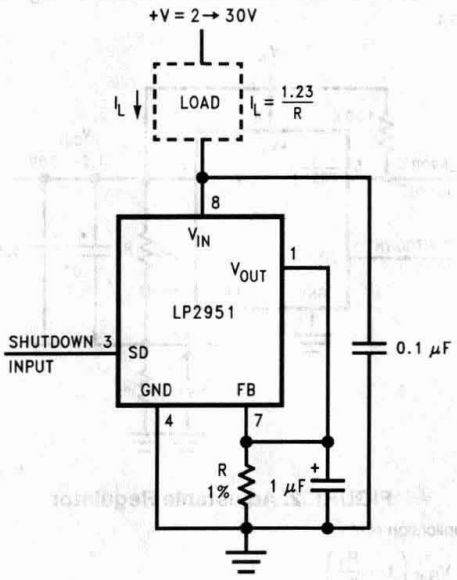
Wide Input Voltage Range Current Limiter



TL/H/8546–9

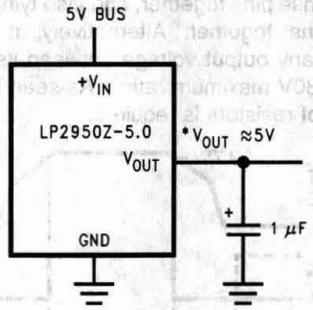
*Minimum input-output voltage ranges from 40 mV to 400 mV, depending on load current. Current limit is typically 160 mA.

Low Drift Current Source



TL/H/8546–8

5 Volt Current Limiter

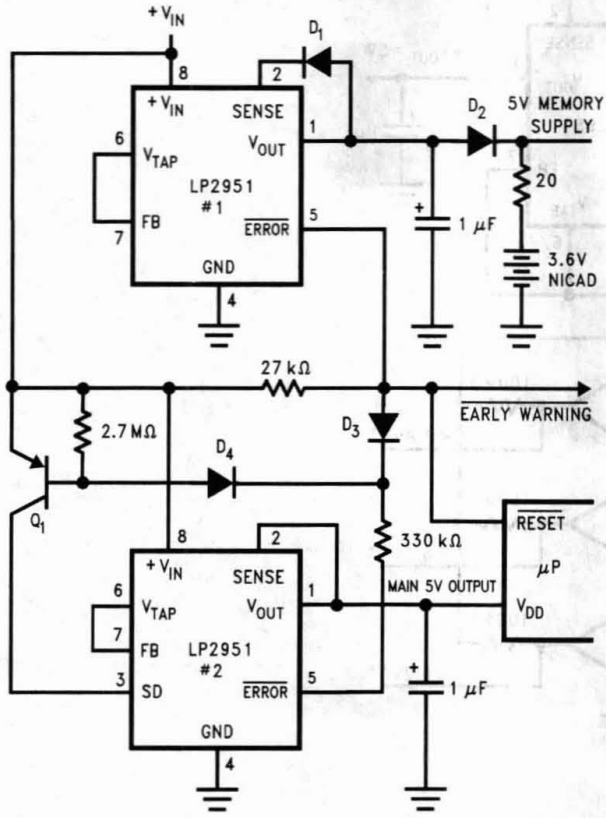


TL/H/8546–10

*Minimum input-output voltage ranges from 40 mV to 400 mV, depending on load current. Current limit is typically 160 mA.

Typical Applications (Continued)

Regulator with Early Warning and Auxiliary Output

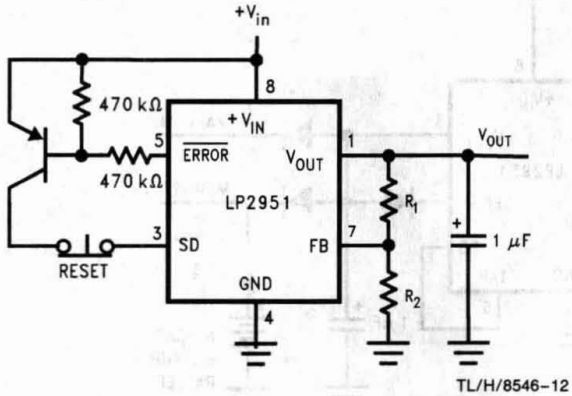


TL/H/8546–11

- Early warning flag on low input voltage
- Main output latches off at lower input voltages
- Battery backup on auxiliary output

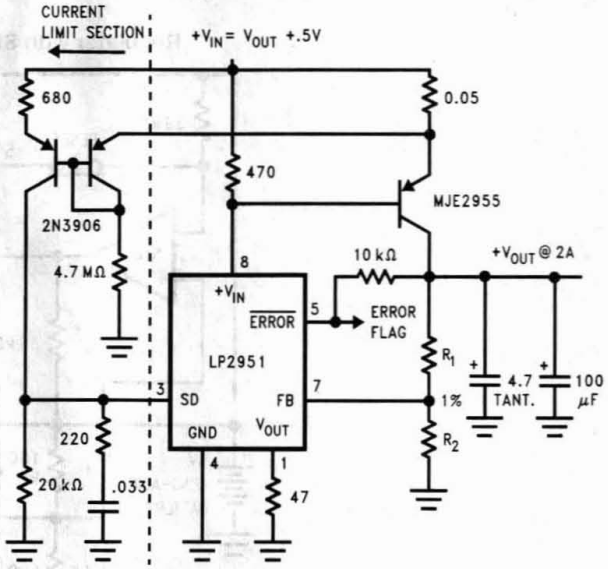
Operation: Reg. #1's V_{out} is programmed one diode drop above 5V. Its error flag becomes active when $V_{in} \leq 5.7V$. When V_{in} drops below 5.3V, the error flag of Reg. #2 becomes active and via Q1 latches the main output off. When V_{in} again exceeds 5.7V Reg. #1 is back in regulation and the early warning signal rises, unlatching Reg. #2 via D3.

Latch Off When Error Flag Occurs



TL/H/8546–12

2 Ampere Low Dropout Regulator

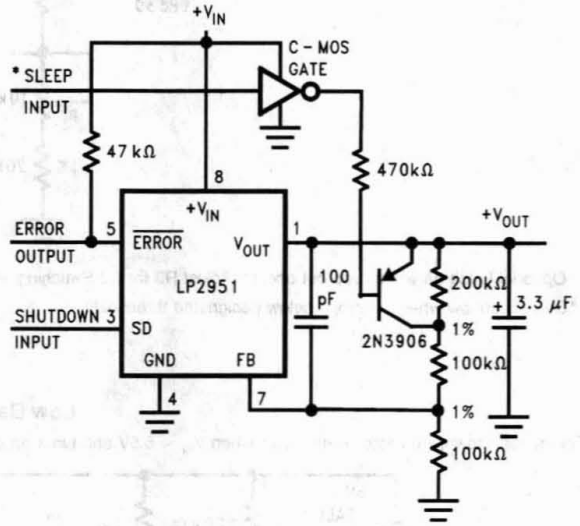


$$V_{out} = 1.23V\left(1 + \frac{R_1}{R_2}\right)$$

TL/H/8546–13

For $5V_{out}$, use internal resistors. Pin 6 to 7, & wire pin 2 to $+V_{out}$ Buss.

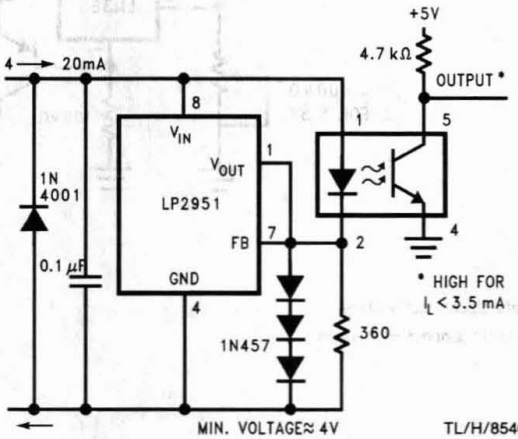
5V Regulator with 2.5V Sleep Function



*High input lowers V_{out} to 2.5V

TL/H/8546–14

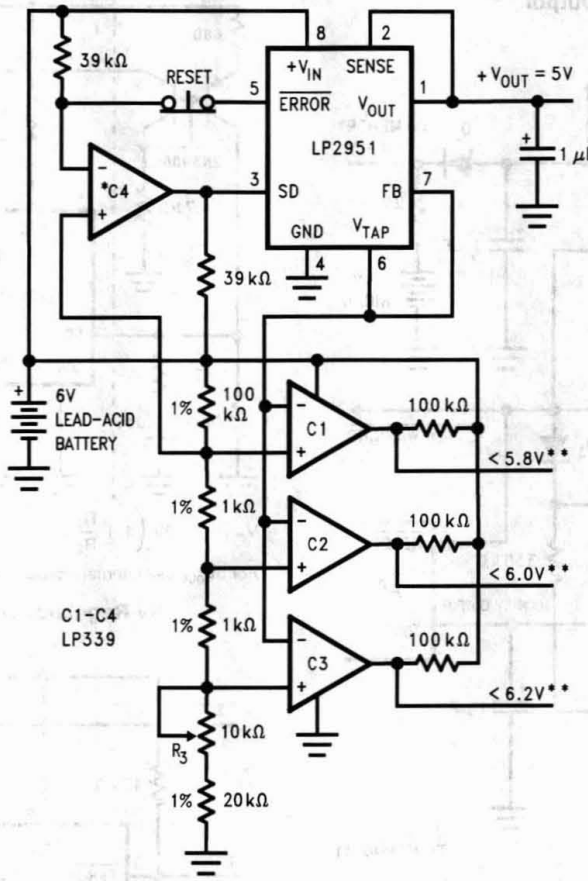
Open Circuit Detector for 4 ⟶ 20 mA Current Loop



TL/H/8546–15

Typical Applications (Continued)

Regulator with State-of-Charge Indicator



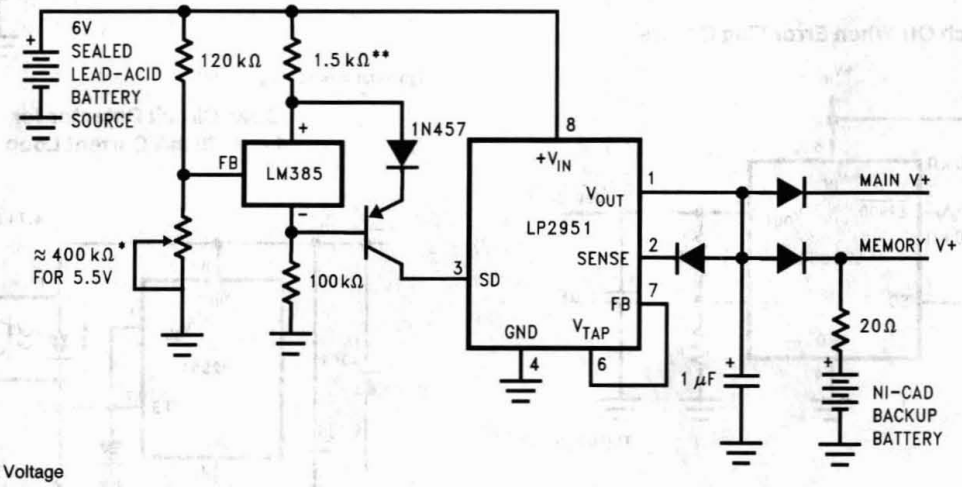
TL/H/8546–16

*Optional Latch off when drop out occurs. Adjust R3 for C2 Switching when V_{in} is 6.0V.

**Outputs go low when V_{in} drops below designated thresholds.

Low Battery Disconnect

For values shown, Regulator shuts down when V_{in} < 5.5V and turns on again at 6.0V. Current drain in disconnected mode is ≈ 150 µA.



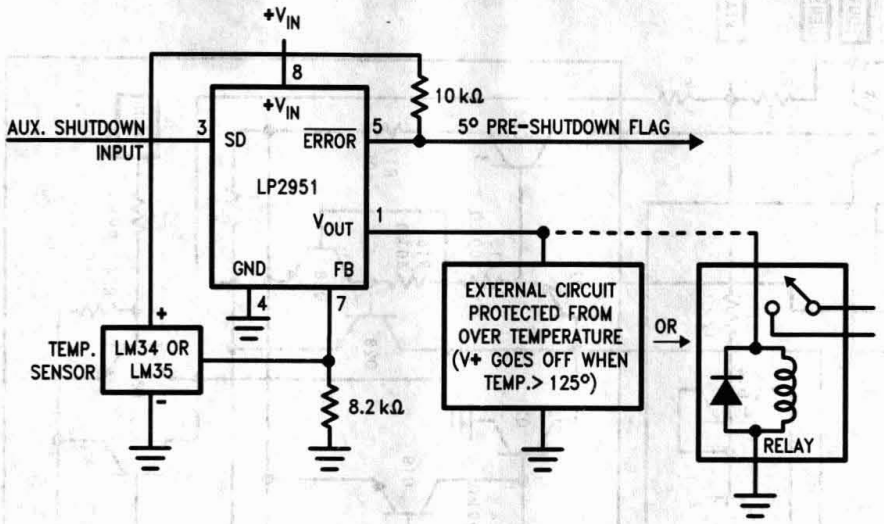
TL/H/8546–17

*Sets disconnect Voltage

**Sets disconnect Hysteresis

Typical Applications (Continued)

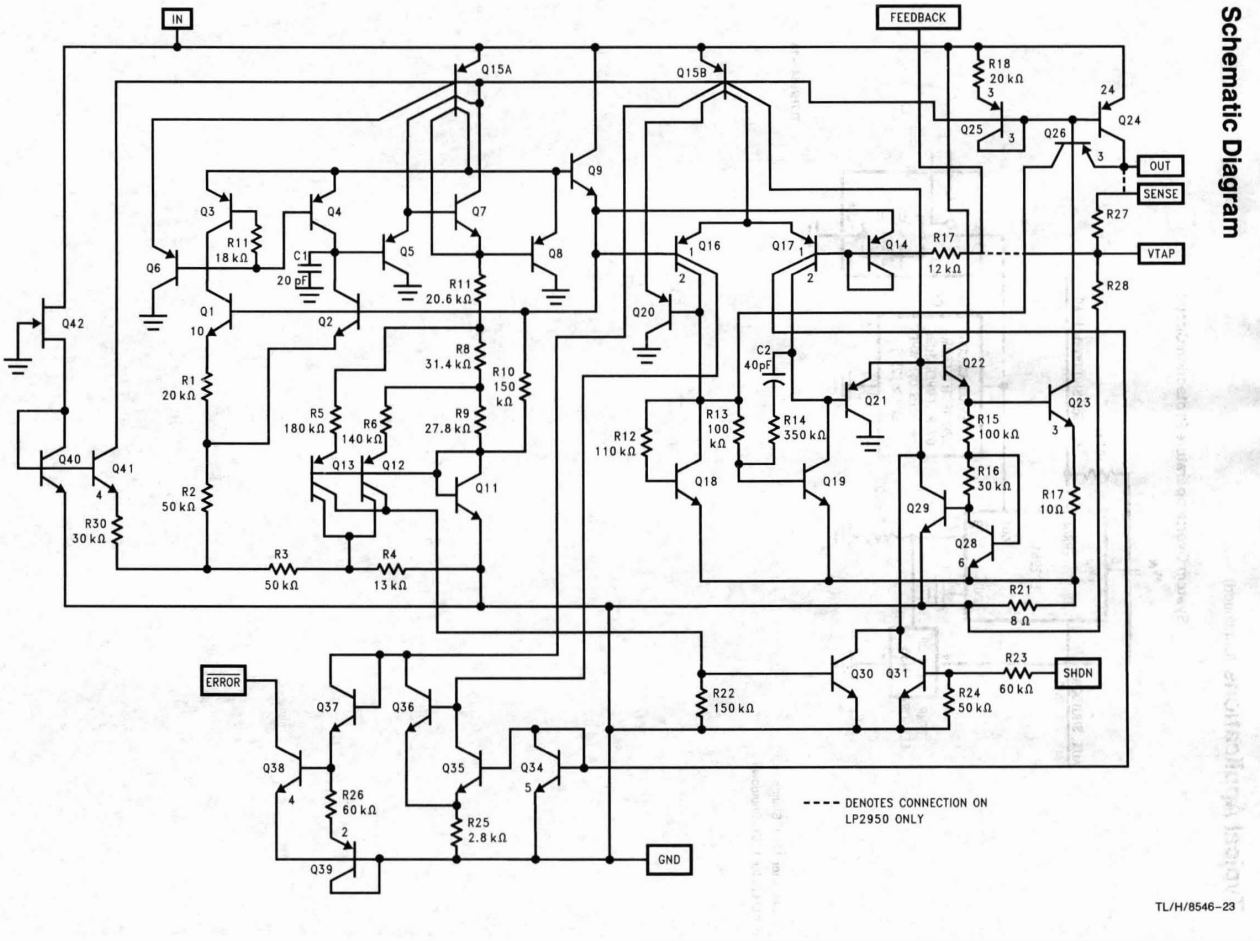
System Overtemperature Protection Circuit



TL/H/8546–18

LM34 for 125°F Shutdown
LM35 for 125°C Shutdown

Schematic Diagram



National Semiconductor

LM2984 Microprocessor Power Supply System

General Description

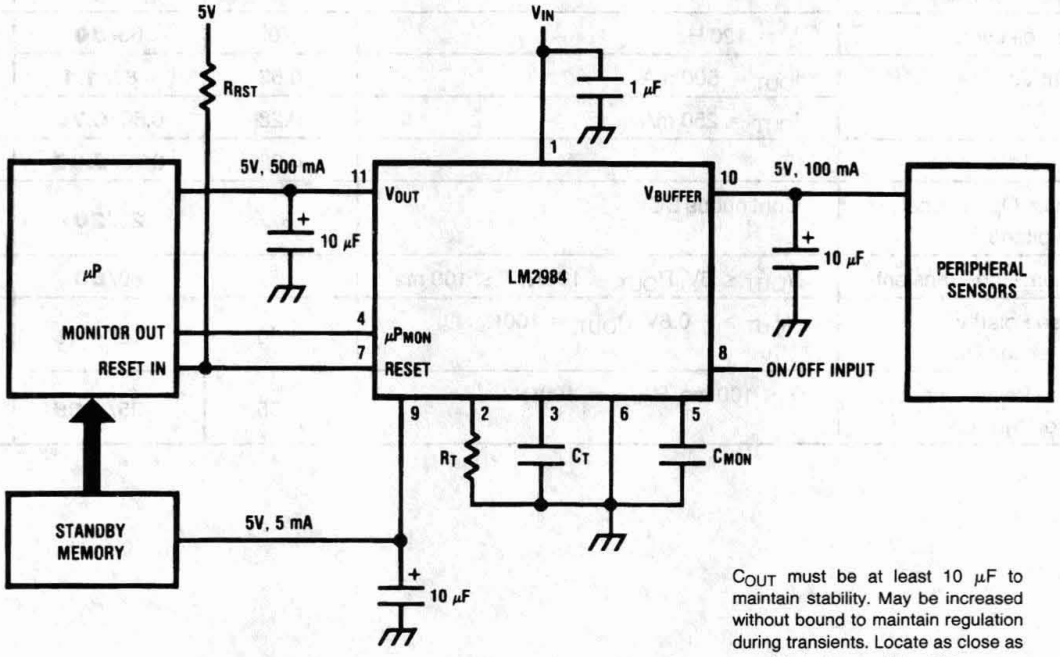
The LM2984 positive voltage regulator features three independent and tracking outputs capable of delivering the power for logic circuits, peripheral sensors and standby memory in a typical microprocessor system. The LM2984 includes circuitry which monitors both its own high-current output and also an external μP. If any error conditions are sensed in either, a reset error flag is set and maintained until the malfunction terminates. Since these functions are included in the same package with the three regulators, a great saving in board space can be realized in the typical microprocessor system. The LM2984 also features very low dropout voltages on each of its three regulator outputs (0.6V at the rated output current). Furthermore, the quiescent current can be reduced to 1 mA in the standby mode.

Designed also for vehicular applications, the LM2984 and all regulated circuitry are protected from reverse battery installations or 2-battery jumps. Familiar regulator features such as short circuit and thermal overload protection are also provided. Fixed outputs of 5V are available in the plastic TO-220 power package.

Features

- Three low dropout tracking regulators
- Output current in excess of 500 mA
- Fully specified for −40°C to +125°C operation
- Low quiescent current standby regulator
- Microprocessor malfunction RESET flag
- Delayed RESET on power-up
- Accurate pretrimmed 5V outputs
- Reverse battery protection
- Overvoltage protection
- Reverse transient protection
- Short circuit protection
- Internal thermal overload protection
- ON/OFF switch for high current outputs
- P+ Product Enhancement tested

Typical Application Circuit



Order Number LM2984T
See NS Package Number TA11B

C_{OUT} must be at least 10 μF to maintain stability. May be increased without bound to maintain regulation during transients. Locate as close as possible to the regulator. This capacitor must be rated over the same operating temperature range as the regulator. The equivalent series resistance (ESR) of this capacitor is critical; see curve.

TL/H/11252–1

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Input Voltage

Survival Voltage (<100 ms)	60V
Operational Voltage	26V

Internal Power Dissipation	Internally Limited
Operating Temperature Range (T_A)	−40°C to +125°C
Maximum Junction Temperature (Note 1)	150°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec.)	230°C
ESD Susceptability (Note 3)	2000V

Electrical Characteristics

V_{IN} = 14V, I_{OUT} = 5 mA, C_{OUT} = 10 μF, unless otherwise indicated. **Boldface** type refers to limits over the entire operating temperature range, −40°C ≤ T_A ≤ +125°C, all other limits are for T_A = T_j = 25°C (Note 6).

Parameter	Conditions	Typical	Limit (Note 2)	Units
V_{OUT} (Pin 11)				
Output Voltage	5 mA ≤ I_O ≤ 500 mA 6V ≤ V_{IN} ≤ 26V	5.00	4.85/**4.75** 5.15/**5.25**	V_{min} V_{max}
Line Regulation	9V ≤ V_{IN} ≤ 16V	2	25/**25**	mV_{max}
	7V ≤ V_{IN} ≤ 26V	5	50/**50**	mV_{max}
Load Regulation	5 mA ≤ I_{OUT} ≤ 500 mA	12	50/**50**	mV_{max}
Output Impedance	250 mA_{dc} and 10 mA_{rms}, f_o = 120 Hz	24		mΩ
Quiescent Current	I_{OUT} = 500 mA	38	100/**100**	mA_{max}
	I_{OUT} = 250 mA	14	50/**50**	mA_{max}
Output Noise Voltage	10 Hz–100 kHz, I_{OUT} = 100 mA	100		μV
Long Term Stability		20		mV/1000 hr
Ripple Rejection	f_o = 120 Hz	70	60/**50**	dB_{min}
Dropout Voltage	I_{OUT} = 500 mA	0.53	0.80/**1.1**	V_{max}
	I_{OUT} = 250 mA	0.28	0.50/**0.70**	V_{max}
Current Limit		0.92	0.75/**0.60**	A_{min}
Maximum Operational Input Voltage	Continuous DC	32	26/**26**	V_{min}
Maximum Line Transient	V_{OUT} ≤ 6V, R_{OUT} = 100Ω, T ≤ 100 ms	65	60/**60**	V_{min}
Reverse Polarity Input Voltage DC	V_{OUT} ≥ −0.6V, R_{OUT} = 100Ω	−30	−15/−**15**	V_{min}
Reverse Polarity Input Voltage Transient	T ≤ 100 ms, R_{OUT} = 100Ω	−55	−35/−**35**	V_{min}

Electrical Characteristics (Continued)

V_{IN} = 14V, I_{buf} = 5 mA, C_{buf} = 10 μF, unless otherwise indicated. **Boldface** type refers to limits over the entire operating temperature range, −40°C ≤ T_A ≤ +125°C, all other limits are for T_A = T_j = 25°C (Note 6).

Parameter	Conditions	Typical	Limit (Note 2)	Units
V_{buffer} (Pin 10)				
Output Voltage	5 mA ≤ I_O ≤ 100 mA 6V ≤ V_{IN} ≤ 26V	5.00	4.85/**4.75** 5.15/**5.25**	V_{min} V_{max}
Line Regulation	9V ≤ V_{IN} ≤ 16V	2	25/**25**	mV_{max}
	7V ≤ V_{IN} ≤ 26V	5	50/**50**	mV_{max}
Load Regulation	5 mA ≤ I_{buf} ≤ 100 mA	15	50/**50**	mV_{max}
Output Impedance	50 mA_{dc} and 10 mA_{rms}, f_O = 120 Hz	200		mΩ
Quiescent Current	I_{buf} = 100 mA	8.0	15/**15**	mA_{max}
Output Noise Voltage	10 Hz–100 kHz, I_{OUT} = 100 mA	100		μV
Long Term Stability		20		mV/1000 hr
Ripple Rejection	f_o = 120 Hz	70	60/**50**	dB_{min}
Dropout Voltage	I_{buf} = 100 mA	0.35	0.50/**0.80**	V_{max}
Current Limit		0.23	0.15/**0.15**	A_{min}
Maximum Operational Input Voltage	Continuous DC	32	26/**26**	V_{min}
Maximum Line Transient	V_{buf} ≤ 6V, R_{buf} = 100Ω, T ≤ 100 ms	65	60/**60**	V_{min}
Reverse Polarity Input Voltage DC	V_{buf} ≥ −0.6V, R_{buf} = 100Ω	−30	−15/−**15**	V_{min}
Reverse Polarity Input Voltage Transient	T ≤ 100 ms, R_{buf} = 100Ω	−55	−35/−**35**	V_{min}

Electrical Characteristics

V_{IN} = 14V, I_{stby} = 1 mA, C_{stby} = 10 μF, unless otherwise indicated. **Boldface** type refers to limits over the entire operating temperature range, −40°C ≤ T_A ≤ +125°C, all other limits are for T_A = T_j = 25°C (Note 6).

Parameter	Conditions	Typical	Limit (Note 2)	Units
$V_{standby}$ (Pin 9)				
Output Voltage	1 mA ≤ I_O ≤ 7.5 mA 6V ≤ V_{IN} ≤ 26V	5.00	4.85/**4.75** 5.15/**5.25**	V_{min} V_{max}
Line Regulation	9V ≤ V_{IN} ≤ 16V	2	25/**25**	mV_{max}
	7V ≤ V_{IN} ≤ 26V	5	50/**50**	mV_{max}
Load Regulation	0.5 mA ≤ I_{OUT} ≤ 7.5 mA	6	50/**50**	mV_{max}
Output Impedance	5 mA_{dc} and 1 mA_{rms}, f_o = 120 Hz	0.9		Ω
Quiescent Current	I_{stby} = 7.5 mA	1.2	2.0/**4.0**	mA_{max}
	I_{stby} = 2 mA	0.9	1.5/**4.0**	mA_{max}

Electrical Characteristics (Continued)

V_{IN} = 14V, I_{stby} = 1 mA, C_{stby} = 10 μF, unless otherwise indicated. **Boldface** type refers to limits over the entire operating temperature range, −40°C ≤ T_A ≤ +125°C, all other limits are for T_A = T_j = 25°C (Note 6).

Parameter	Conditions	Typical	Limit (Note 2)	Units
$V_{standby}$ (Pin 9) (Continued)				
Output Noise Voltage	10 Hz–100 kHz, I_{stby} = 1 mA	100		μV
Long Term Stability		20		mV/1000 hr
Ripple Rejection	f_o = 120 Hz	70	60/**50**	dB_{min}
Dropout Voltage	I_{stby} = 1 mA	0.26	0.50/**0.60**	V_{max}
	I_{stby} = 7.5 mA	0.38	0.60/**0.70**	V_{max}
Current Limit		15	12/**12**	mA_{min}
Maximum Operational Input Voltage	4.5V ≤ V_{stby} ≤ 6V, R_{stby} = 1000Ω	65	60/**60**	V_{min}
Maximum Line Transient	V_{stby} ≤ 6V, T ≤ 100 ms, R_{stby} = 1000Ω	65	60/**60**	V_{min}
Reverse Polarity Input Voltage DC	V_{stby} ≥ −0.6V, R_{stby} = 1000Ω	−30	−15/−**15**	V_{min}
Reverse Polarity Input Voltage Transient	T ≤ 100 ms, R_{stby} = 1000Ω	−55	−35/−**35**	V_{min}

Electrical Characteristics

V_{IN} = 14V, C_{OUT} = 10 μF, C_{buf} = 10 μF, C_{stby} = 10 μF, unless otherwise indicated. **Boldface** type refers to limits over the entire operating temperature range, −40°C ≤ T_A ≤ +125°C, all other limits are for T_A = T_j = 25°C (Note 6).

Parameter	Conditions	Typical	Limit (Note 2)	Units
Tracking and Isolation				
Tracking V_{OUT}–V_{stby}	I_{OUT} ≤ 500 mA, I_{buf} = 5 mA, I_{stby} ≤ 7.5 mA	±30	±100/±**100**	mV_{max}
Tracking V_{buf}–V_{stby}	I_{OUT} = 5 mA, I_{buf} ≤ 100 mA, I_{stby} ≤ 7.5 mA	±30	±100/±**100**	mV_{max}
Tracking V_{OUT}–V_{buf}	I_{OUT} ≤ 500 mA, I_{buf} ≤ 100 mA, I_{stby} = 1 mA	±30	±100/±**100**	mV_{max}
Isolation* V_{buf} from V_{OUT}	R_{OUT} = 1Ω, I_{buf} ≤ 100 mA	5.00	4.50/**4.50** 5.50/**5.50**	V_{min} V_{max}
Isolation* V_{stby} from V_{OUT}	R_{OUT} = 1Ω, I_{stby} ≤ 7.5 mA	5.00	4.50/**4.50** 5.50/**5.50**	V_{min} V_{max}
Isolation* V_{OUT} from V_{buf}	R_{buf} = 1Ω, I_{OUT} ≤ 500 mA	5.00	4.50/**4.50** 5.50/**5.50**	V_{min} V_{max}
Isolation* V_{stby} from V_{buf}	R_{buf} = 1Ω, I_{stby} ≤ 7.5 mA	5.00	4.50/**4.50** 5.50/**5.50**	V_{min} V_{max}

*Isolation refers to the ability of the specified output to remain within the tested limits when the other output is shorted to ground.

Electrical Characteristics (Continued)

V_{IN} = 14V, I_{OUT} = 5 mA, I_{buf} = 5 mA, I_{stby} = 5 mA, R_t = 130 kΩ, C_t = 0.33 μF, C_{mon} = 0.47 μF, unless otherwise indicated, **Boldface** type refers to limits over the entire operating temperature range, −40°C ≤ T_A ≤ +125°C, all other limits are for T_A = T_J = 25°C (Note 6)

Parameter	Conditions	Typical	Limit (Note 2)	Units
Computer Monitor/Reset Functions				
I_{reset} Low	V_{IN} = 4V, V_{rst} = 0.4V	5	2/**0.50**	mA_{min}
V_{reset} Low	V_{IN} = 4V, I_{rst} = 1 mA	0.10	0.40/**0.40**	V_{max}
R_t voltage	(Pin 2)	1.22	1.15/**0.75**	V_{min}
		1.22	1.30/**2.00**	V_{max}
Power On Reset Delay	$V\mu P_{mon}$ = 5V (T_{dly} = 1.2 R_t C_t)	50	45/**17.0**	ms_{min}
		50	55/**80.0**	ms_{max}
ΔV_{OUT} Low Reset Threshold	(Note 4)	−350	−225/−**175**	mV_{min}
			−500/−**550**	mV_{max}
ΔV_{OUT} High Reset Threshold	(Note 4)	600	225/**175**	mV_{min}
			750/**800**	mV_{max}
Reset Output Leakage	$V\mu P_{mon}$ = 5V, V_{rst} = 12V	0.01	1/**5.0**	μA_{max}
μP_{mon} Input Current (Pin 4)	$V\mu P_{mon}$ = 2.4V	7.5	25/**25**	μA_{max}
	$V\mu P_{mon}$ = 0.4V	0.01	10/**15**	μA_{max}
μP_{mon} Input Threshold Voltage		1.22	0.80/**0.80**	V_{min}
		1.22	2.00/**2.00**	V_{max}
μP Monitor Reset Oscillator Period	$V\mu P_{mon}$ = 0V (T_{window} = 0.82 $R_t C_{mon}$)	50	45/**30**	ms_{min}
		50	55/**70**	ms_{max}
μP Monitor Reset Oscillator Pulse Width	$V\mu P_{mon}$ = 0V ($RESET_{pw}$ = 2000 C_{mon})	1.0	0.7/**0.4**	ms_{min}
		1.0	1.3/**2.10**	ms_{max}
Minimum μP Monitor Input Pulse Width	(Note 5)	2		μs
Reset Fall Time	R_{rst} = 10k, V_{rst} = 5V, C_{rst} ≤ 10 pF	0.20	1.00/**1.00**	μs_{max}
Reset Rise Time	R_{rst} = 10k, V_{rst} = 5V, C_{rst} ≤ 10 pF	0.60	1.00/**1.50**	μs_{max}
On/Off Switch Input Current (Pin 8)	V_{ON} = 2.4V	7.5	25/**25**	μA_{max}
	V_{ON} = 0.4V	0.01	10/**10**	μA_{max}
On/Off Switch Input Threshold Voltage		1.22	0.80/**0.80**	V_{min}
		1.22	2.00/**2.00**	V_{max}

Note 1: Thermal resistance without a heatsink for junction-to-case temperature is 3°C/W. Thermal resistance case-to-ambient is 40°C/W.

Note 2: Tested Limits are guaranteed and 100% production tested.

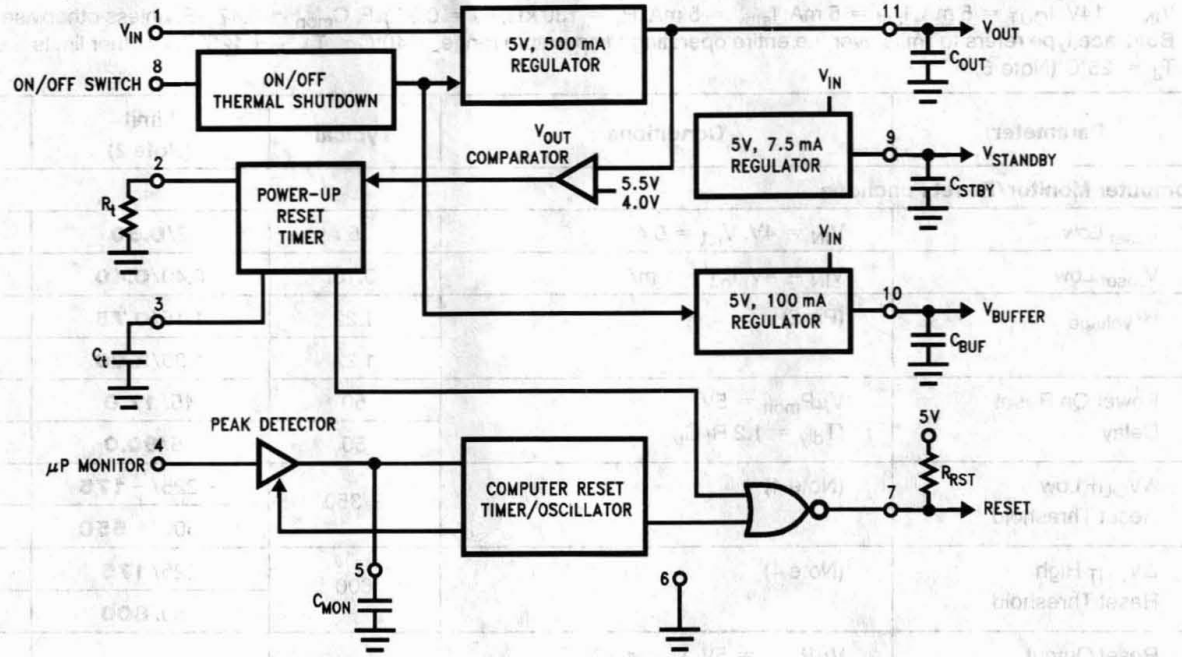
Note 3: Human body model, 100 pF capacitor discharged through a 1500Ω resistor.

Note 4: Internal comparators detect when the main regulator output (V_{OUT}) changes from the measured output voltage (with V_{IN} = 14V) by the specified amount, ΔV_{OUT} High or ΔV_{OUT} Low, and set the Reset Error Flag low. The Reset Error Flag is held low until V_{OUT} returns to regulation. The Reset Error Flag is then allowed to go high again after a delay set by R_t and C_t. (see application section).

Note 5: This parameter is a measure of how short a pulse can be detected at the μP Monitor Input. This parameter is primarily influenced by the value of C_{mon}. (See Application Hints Section.)

Note 6: To ensure constant junction temperature, low duty cycle pulse testing is used.

Block Diagram



TL/H/11252–2

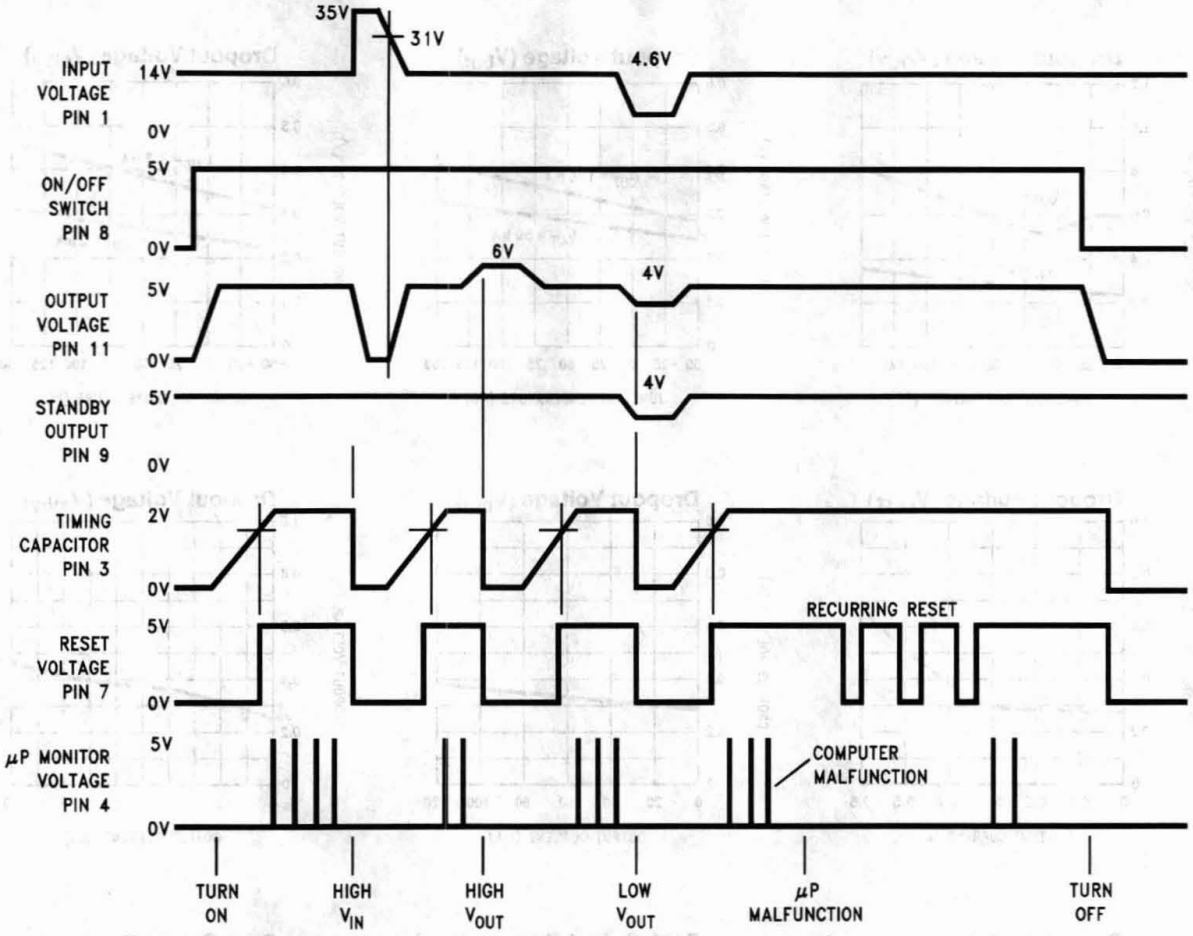
Pin Description

Pin No.	Pin Name	Comments
1	V_{IN}	Positive supply input voltage
2	R_t	Sets internal timing currents
3	C_t	Sets power-up reset delay timing
4	μP_{mon}	Microcomputer monitor input
5	C_{mon}	Sets μC monitor timing
6	Ground	Regulator ground
7	Reset	Reset error flag output
8	ON/OFF	Enables/disables high current regulators
9	$V_{standby}$	Standby regulator output (7.5 mA)
10	V_{buffer}	Buffer regulator output (100 mA)
11	V_{OUT}	Main regulator output (500 mA)

External Components

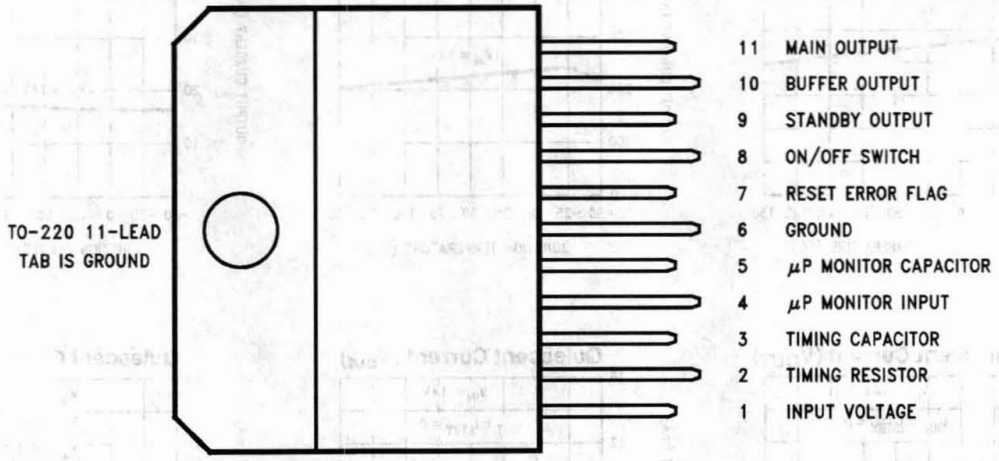
Component	Typical Value	Component Range	Comments
C_{IN}	1 μF	0.47 μF–10 μF	Required if device is located far from power supply filter.
R_t	130k	24k–510k	Sets internal timing currents.
C_t	0.33 μF	0.033 μF–3.3 μF	Sets power-up reset delay.
C_{tc}	0.01 μF	0.001 μF–0.1 μF	Establishes time constant of AC coupled computer monitor.
R_{tc}	10k	1k–100k	Establishes time constant of AC coupled computer monitor. (See applications section.)
C_{mon}	0.47 μF	0.047 μF–4.7 μF	Sets time window for computer monitor. Also determines period and pulse width of computer malfunction reset. (See applications section.)
R_{rst}	10k	5k–100k	Load for open collector reset output. Determined by computer reset input requirements.
C_{stby}	10 μF	10 μF–no bound	A 10 μF is required for stability but larger values can be used to maintain regulation during transient conditions.
C_{buf}	10 μF	10 μF–no bound	A 10 μF is required for stability but larger values can be used to maintain regulation during transient conditions.
C_{OUT}	10 μF	10 μF–no bound	A 10 μF is required for stability but larger values can be used to maintain regulation during transient conditions.

Typical Circuit Waveforms



TL/H/11252–3

Connection Diagram



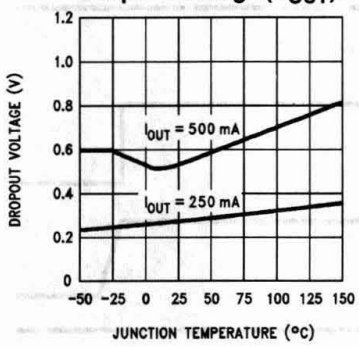
TL/H/11252–4

Order Number LM2984T
See NS Package Number TA11B

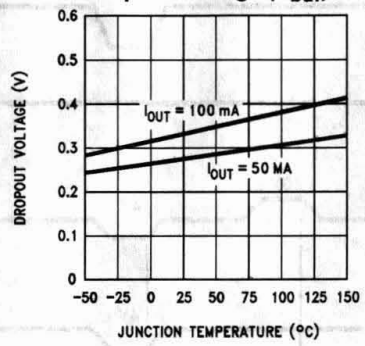
3

Typical Performance Characteristics

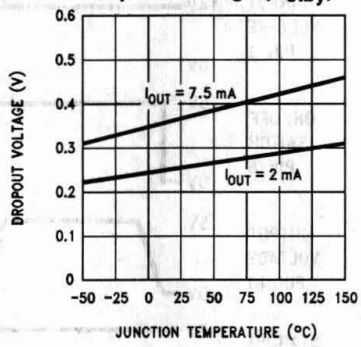
Dropout Voltage (V_{OUT})



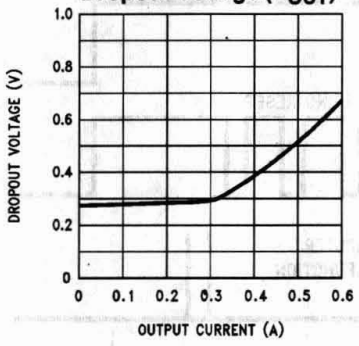
Dropout Voltage (V_{buf})



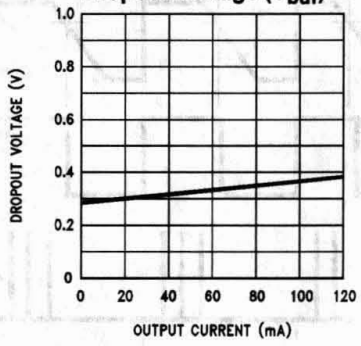
Dropout Voltage (V_{stby})



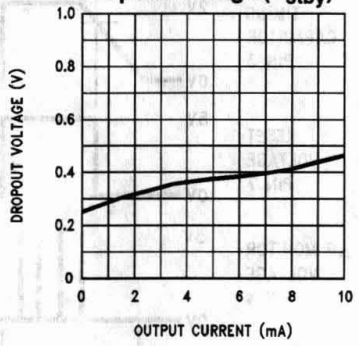
Dropout Voltage (V_{OUT})



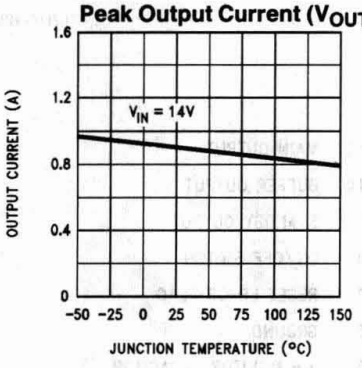
Dropout Voltage (V_{buf})



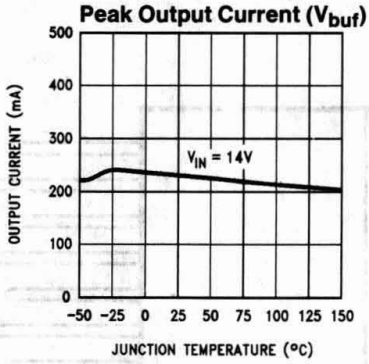
Dropout Voltage (V_{stby})



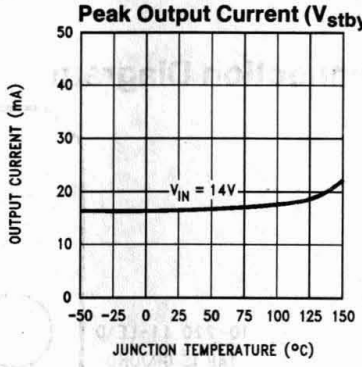
Peak Output Current (V_{OUT})



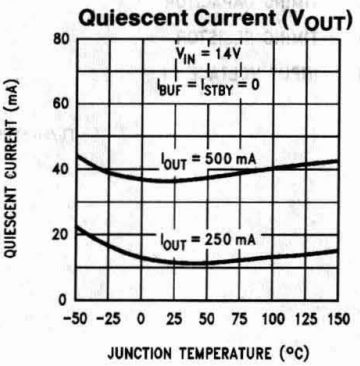
Peak Output Current (V_{buf})



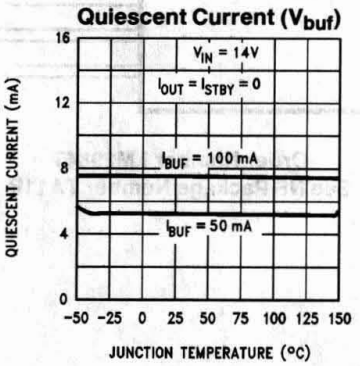
Peak Output Current (V_{stby})



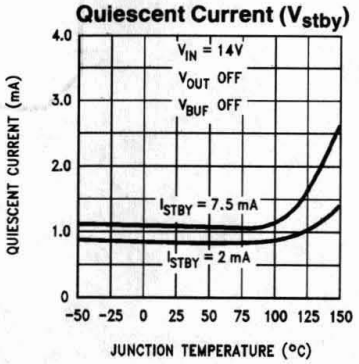
Quiescent Current (V_{OUT})



Quiescent Current (V_{buf})



Quiescent Current (V_{stby})



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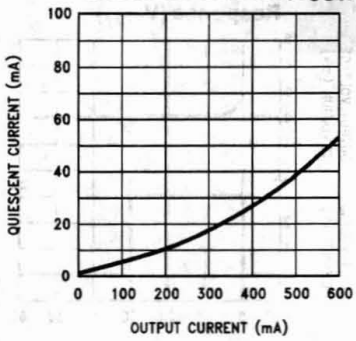
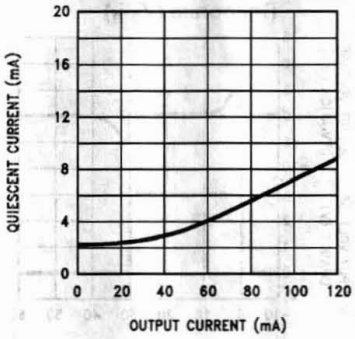
Typical Performance Characteristics (Continued)

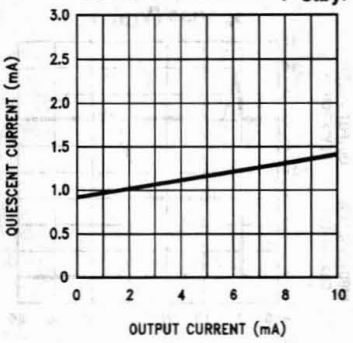
Quiescent Current (V_{OUT})



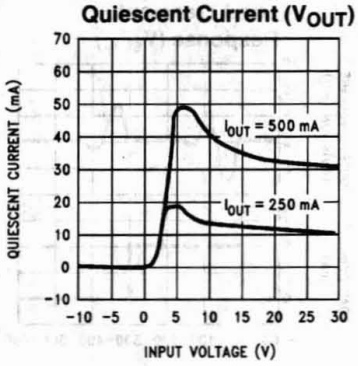
Quiescent Current (V_{buf})



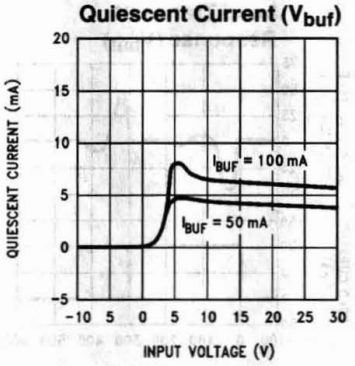
Quiescent Current (V_{stby})



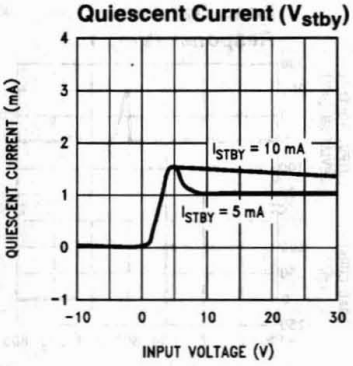
Quiescent Current (V_{OUT})



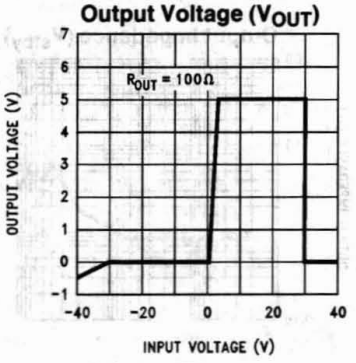
Quiescent Current (V_{buf})



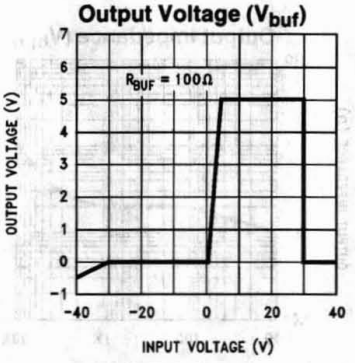
Quiescent Current (V_{stby})



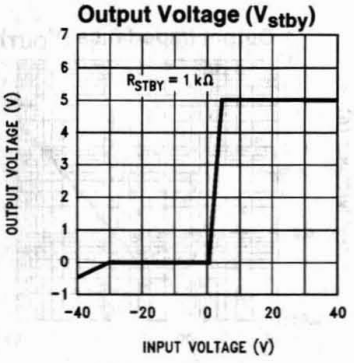
Output Voltage (V_{OUT})



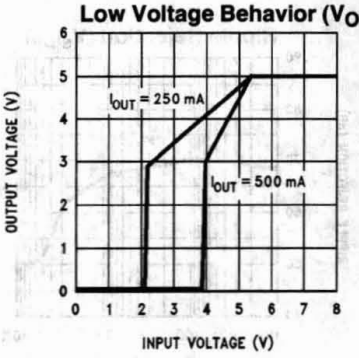
Output Voltage (V_{buf})



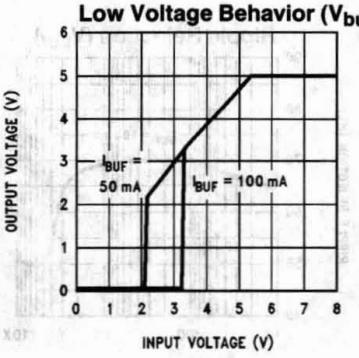
Output Voltage (V_{stby})



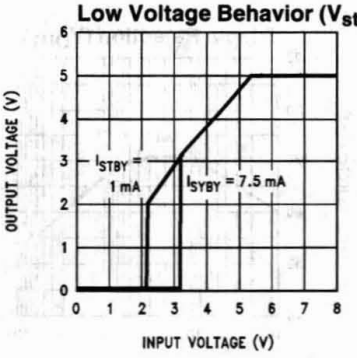
Low Voltage Behavior (V_{OUT})



Low Voltage Behavior (V_{buf})



Low Voltage Behavior (V_{stby})



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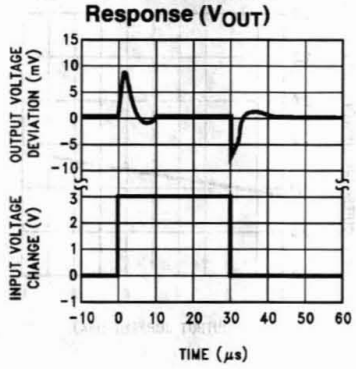
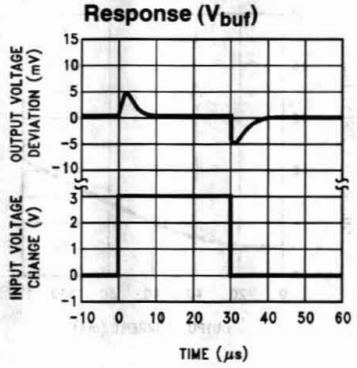
Typical Performance Characteristics (Continued)

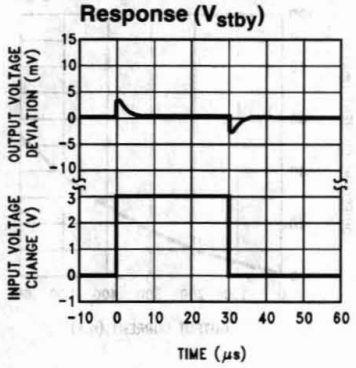
Line Transient Response (V_{OUT})



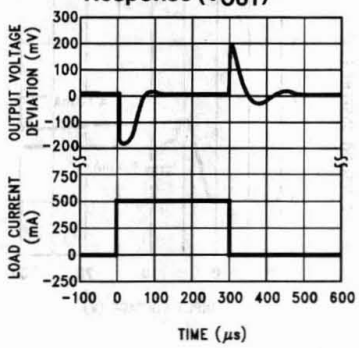
Line Transient Response (V_{buf})



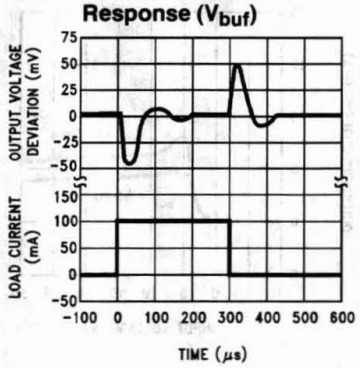
Line Transient Response (V_{stby})



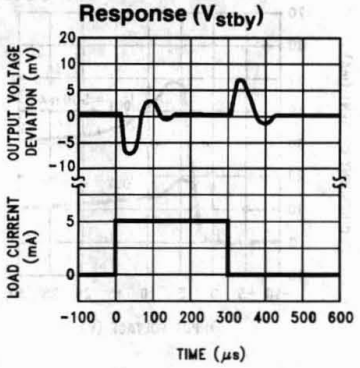
Load Transient Response (V_{OUT})



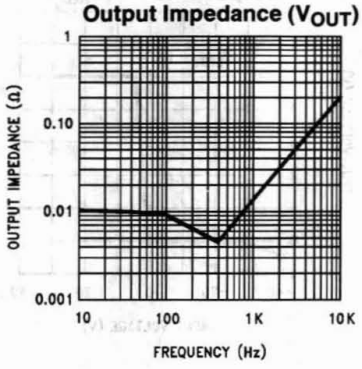
Load Transient Response (V_{buf})



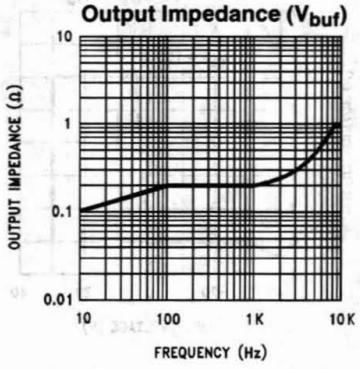
Load Transient Response (V_{stby})



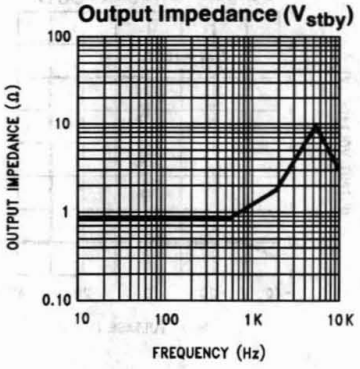
Output Impedance (V_{OUT})



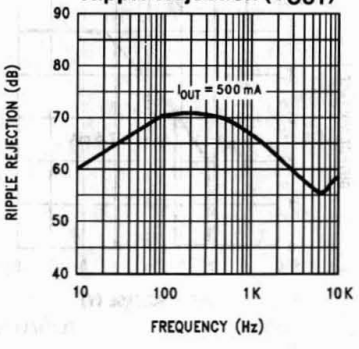
Output Impedance (V_{buf})



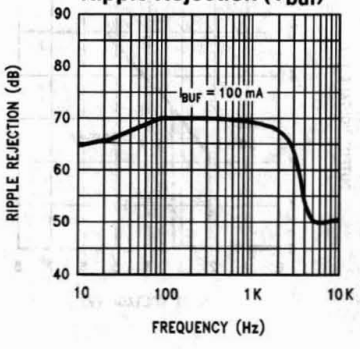
Output Impedance (V_{stby})



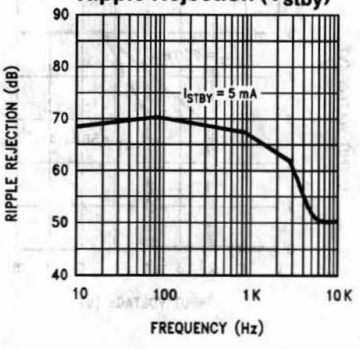
Ripple Rejection (V_{OUT})



Ripple Rejection (V_{buf})



Ripple Rejection (V_{stby})



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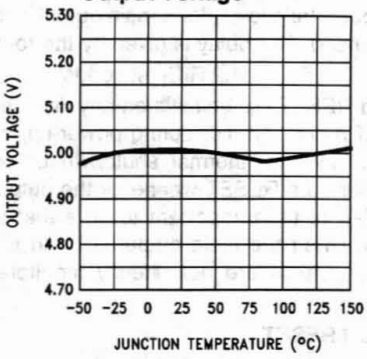
Typical Performance Characteristics (Continued)

Output Voltage



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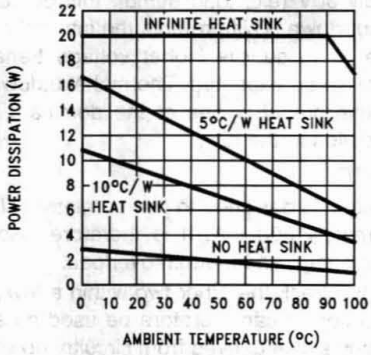
Device Dissipation vs Ambient Temperature


POWER DISSIPATION (W)
INFINITE HEAT SINK
5°C/W HEAT SINK
10°C/W HEAT SINK
NO HEAT SINK
0 10 20 30 40 50 60 70 80 90 100
AMBIENT TEMPERATURE (°C)

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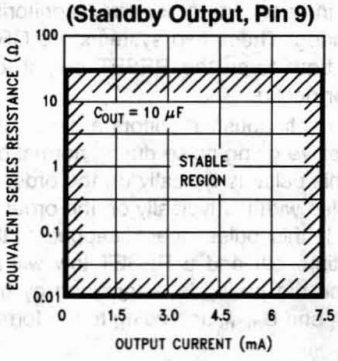
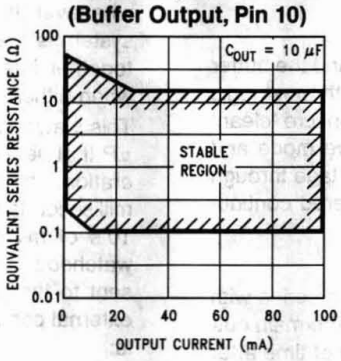
Output Capacitor ESR (Standby Output, Pin 9)



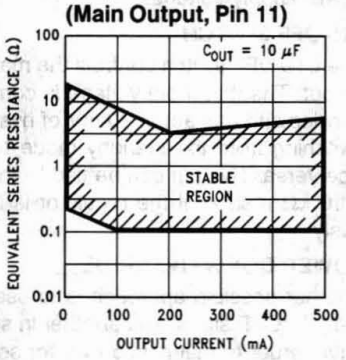
TL/H/11252–10

Output Capacitor ESR (Buffer Output, Pin 10)



TL/H/11252–11

Output Capacitor ESR (Main Output, Pin 11)



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Application Hints

OUTPUT CAPACITORS

The LM2984 output capacitors are required for stability. Without them, the regulator outputs will oscillate, sometimes by many volts. Though the 10 μF shown are the minimum recommended values, actual size and type may vary depending upon the application load and temperature range. Capacitor effective series resistance (ESR) also affects the IC stability. Since ESR varies from one brand to the next, some bench work may be required to determine the minimum capacitor value to use in production. Worst case is usually determined at the minimum ambient temperature and the maximum load expected.

Output capacitors can be increased in size to any desired value above the minimum. One possible purpose of this would be to maintain the output voltages during brief conditions of negative input transients that might be characteristic of a particular system.

Capacitors must also be rated at all ambient temperatures expected in the system. Many aluminum type electrolytics will freeze at temperatures less than −30°C, reducing their effective capacitance to zero. To maintain regulator stability down to −40°C, capacitors rated at that temperature (such as tantalums) must be used.

Each output **must** be terminated by a capacitor, even if it is not used.

STANDBY OUTPUT

The standby output is intended for use in systems requiring standby memory circuits. While the high current regulator outputs are controlled with the ON/OFF pin described later, the standby output remains on under all conditions as long as sufficient input voltage is supplied to the IC. Thus, memory and other circuits powered by this output remain unaffected by positive line transients, thermal shutdown, etc.

The standby regulator circuit is designed so that the quiescent current to the IC is very low (<1.5 mA) when the other regulator outputs are off.

The capacitor on the output of this regulator can be increased without bound. This will help maintain the output voltage during negative input transients and will also help to reduce the noise on all three outputs. Because the other two track the standby output: therefore any noise reduction here will also reduce the other two noise voltages.

BUFFER OUTPUT

The buffer output is designed to drive peripheral sensor circuitry in a μP system. It will track the standby and main regulator within a few millivolts in normal operation. Therefore, a peripheral sensor can be powered off this supply and have the same operating voltage as the μP system. This is important if a ratiometric sensor system is being used.

The buffer output can be short circuited while the other two outputs are in normal operation. This protects the μP system from disruption of power when a sensor wire, etc. is temporarily shorted to ground, i.e. only the sensor signal would be interrupted, while the μP and memory circuits would remain operational.

The buffer output is similar to the main output in that it is controlled by the ON/OFF switch in order to save power in

Application Hints (Continued)

the standby mode. It is also fault protected against overvoltage and thermal overload. If the input voltage rises above approximately 30V (e.g. load dump), this output will automatically shut down. This protects the internal circuitry and enables the IC to survive higher voltage transients than would otherwise be expected. Thermal shutdown is necessary since this output is one of the dominant sources of power dissipation in the IC.

MAIN OUTPUT

The main output is designed to power relatively large loads, i.e. approximately 500 mA. It is therefore also protected against overvoltage and thermal overload.

This output will track the other two within a few millivolts in normal operation. It can therefore be used as a reference voltage for any signal derived from circuitry powered off the standby or buffer outputs. This is important in a ratiometric sensor system or any system requiring accurate matching of power supply voltages.

ON/OFF SWITCH

The ON/OFF switch controls the main output and the buffer output. The threshold voltage is compatible with most logic families and has about 20 mV of hysteresis to insure 'clean' switching from the standby mode to the active mode and vice versa. This pin can be tied to the input voltage through a 10 kΩ resistor if the regulator is to be powered continuously.

POWER DOWN OVERRIDE

Another possible approach is to use a diode in series with the ON/OFF signal and another in series with the main output in order to maintain power for some period of time after the ON/OFF signal has been removed (see *Figure 1*). When the ON/OFF switch is initially pulled high through diode D1, the main output will turn on and supply power through diode D2 to the ON/OFF switch effectively latching the main output. An open collector transistor Q1 is connected to the ON/OFF pin along with the two diodes and forces the regulators off after a period of time determined by the μP. In this way, the μP can override a power down command and store data, do housekeeping, etc. before reverting back to the standby mode.

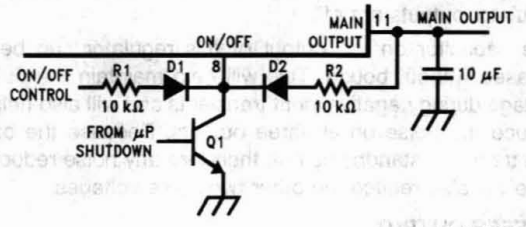

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FIGURE 1. Power Down Override

RESET OUTPUT

This output is an open collector NPN transistor which is forced low whenever an error condition is present at the main output or when a μP error is sensed (see μP Monitor section). If the main output voltage drops by 350 mV or rises out of regulation by 600 mV typically, the RESET output is forced low and held low for a period of time set by two external components, R_t and C_t. There is a slight amount of hysteresis in these two threshold voltages so that the RESET output has a fast rise and fall time compatible with the requirements of most μP RESET inputs.

DELAYED RESET

Resistor R_t and capacitor C_t set the period of time that the RESET output is held low after a main output error condition has been sensed. The delay is given by the formula:

$$T_{dly} = 1.2\ R_tC_t \text{ (seconds)}$$

The delayed RESET will be initiated any time the main output is out of regulation, i.e. during power-up, short circuit, overvoltage, low line, thermal shutdown or power-down. The μP is therefore RESET whenever the output voltage is out of regulation. (It is important to note that a RESET is only initiated when the main output is in error. The buffer and standby outputs are not directly monitored for error conditions.)

μP MONITOR RESET

There are two distinct and independent error monitoring systems in the LM2984. The one described above monitors the main regulator output and initiates a delayed RESET whenever this output is in error. The other error monitoring system is the μP watchdog. These two systems are OR'd together internally and both force the RESET output low when either type of error occurs.

This watchdog circuitry continuously monitors a pin on the μP that generates a positive going pulse during normal operation. The period of this pulse is typically on the order of milliseconds and the pulse width is typically on the order of 10's of microseconds. If this pulse ever disappears, the watchdog circuitry will time out and a RESET low will be sent to the μP. The time out period is determined by two external components, R_t and C_{mon}, according to the formula:

$$T_{window} = 0.82\ R_tC_{mon} \text{ (seconds)}$$

The width of the RESET pulse is set by C_{mon} and an internal resistor according to the following:

$$RESET_{pw} = 2000\ C_{mon} \text{ (seconds)}$$

A square wave signal can also be monitored for errors by filtering the C_{mon} input such that only the positive edges of the signal are detected. *Figure 2* is a schematic diagram of a typical circuit used to differentiate the input signal. Resistor R_{tc} and capacitor C_{tc} pass only the rising edge of the square wave and create a short positive pulse suitable for the μP monitor input. If the incoming signal continues in a high state or in a low state for too long a period of time, a RESET low will be generated.

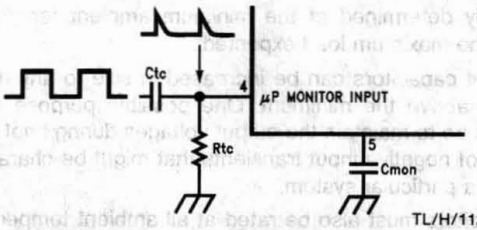

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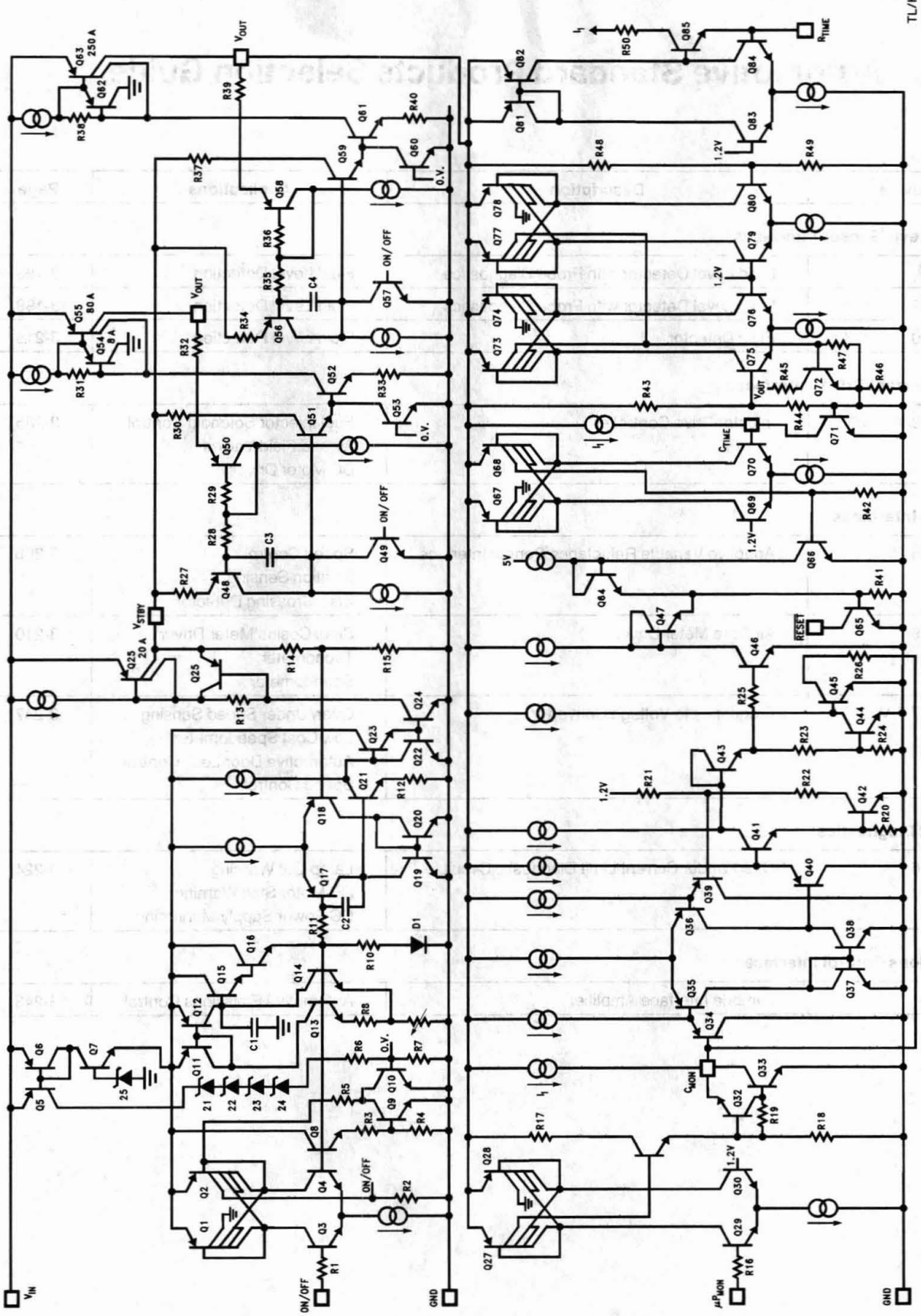
FIGURE 2. Monitoring Square Wave μP Signals

The threshold voltage and input characteristics of this pin are compatible with nearly all logic families.

There is a limit on the width of a pulse that can be reliably detected by the watchdog circuit. This is due to the output resistance of the transistor which discharges C_{mon} when a high state is detected at the input. The minimum detectable pulse width can be determined by the following formula:

$$PW_{min} = 20\ C_{mon} \text{ (seconds)}$$

Equivalent Schematic Diagram



National Semiconductor

Automotive Standard Products Selection Guide

Device	Description	Applications	Page
Fluid Level Sensor Interfaces			
LM903	Fluid Level Detector with Probe Diagnostics	Fluid Level Detection	3-193
LM1042	Fluid Level Detector with Probe Diagnostics	Fluid Level Detection	3-199
LM1830	Fluid Detector	Fluid Level Detection	3-218
High Current Driver Interfaces			
LM1949	Injector Drive Controller	Fuel Injector Solenoid Control Air and Fluid Valves DC Motor Drives	3-235
Speed Interfaces			
LM1815	Adaptive Variable Reluctance Sensor Interface	Speed Control Position Sensing Zero Crossing Detector	3-206
LM1819	Air Core Meter Driver	Sine/Cosine Meter Driver Tachometer Speedometer	3-210
LM2907/LM2917	Frequency to Voltage Convertor	Over/Under Speed Sensing Low Cost Speedometer Automotive Door Lock Control Speed Control	3-247
Circuit Diagnostics			
LM1946	Over/Under Current Limit Diagnostic Circuit	Lamp Out Warning DC Motor Stall Warning DC Power Supply Monitoring	3-224
Emissions Control Interface			
LM9044	Lambda Interface Amplifier	Automotive Emissions Control	3-243

National Semiconductor

LM903 Fluid Level Detector

General Description

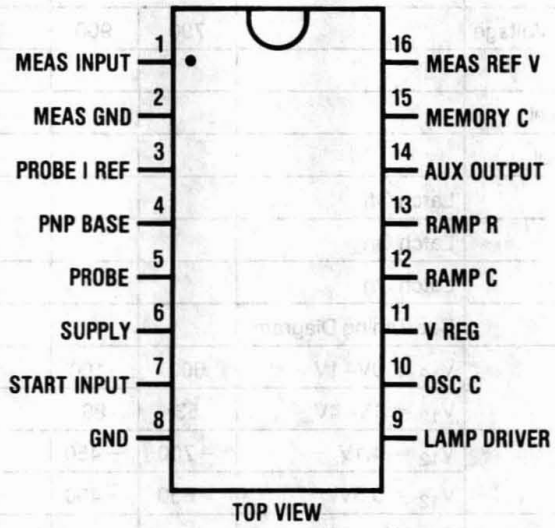
The LM903 uses the thermal-resistive probe technique to measure the level of nonflammable fluids. A low fluid level is indicated by a warning lamp operating in continuous or flashing mode. All supervisory requirements to control the thermal-resistive probe, including short and open circuit probe detection, are incorporated within the device. The circuit has possible applications in the detection of hydraulic fluid, oil level, etc., and may be used with partially conducting fluids.

Features

- Flashing or continuous warning indication
- Warning threshold externally adjustable
- Control circuitry for thermal-resistive probe
- Switch on reset and delay to avoid transients
- 600 mA flashing lamp drive capability
- Short and open circuit probe detection
- 70V transient protection on supply and control input
- 7V–18V supply range
- Internally regulated supply
- −40°C to +80°C operation

Connection Diagram

Dual-In-Line Package



TOP VIEW

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Order Number LM903N
See NS Package Number N16E

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Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage, V_{CC}	18V
Control Input Voltage (Pin 7)	18V
Transient Voltage (Pins, 6, 7, 9) 10 ms (Note 1)	70V
Output Current (Pin 4) I_4 (Sink)	10 mA
Operating Temperature Range	−40°C to +85°C
Storage Temperature	−55°C to +150°C
Maximum Junction Temperature	+150°C
Lead Temperature (Soldering, 10 sec.)	260°C

Electrical Characteristics

V_{CC} = 12V, C_T = 33 μF, R_T = 7.5 kΩ, T_A within operating range except where stated otherwise

Symbol	Parameter	Conditions	Tested Limits (Note 2)		Design Limits (Note 3)			Units
			Min	Max	Min	Typ	Max	
V_{CC}	Supply Voltage		7.0	18	7.0	13	18	V
I_S	Supply Current			50			50	mA
V_{REG}	Regulated Voltage		5.5	6.2	5.3	5.8	6.3	V
	Regulation Temperature Drift	V_{CC} = 7.2V–18V		105		 500		mV μV/°C
V_6–V_3	Probe Current Reference Voltage		2.0	2.35	1.95	2.20	2.40	V
V_{REF}	Measurement Reference Voltage		790	900	780	850	910	mV
R_{REF}	Reference Input Resistor					1.2		kΩ
V_7	Start Input Logic High Level				1.6			V
V_7	Start Input Logic Low Level						1.0	V
I_7	High Input Current	Latch Off					100	nA
I_7	Latch Holding Current	Latch On				2.5		nA
R_7	Resistance Pin 7	Latch On				22		kΩ
I_{12}	Ramp Current	See Timing Diagram						
	Charging	V_{12} = 0V–1V	600	1100	590		1100	μA
		V_{12} = 1V–4V	53	93	50		96	μA
	Discharging	V_{12} = 4.1V	−700	−450	−710		−440	μA
		V_{12} = 0.5V	−650	−400	−660		−390	μA
V_{12}	Ramp Threshold	See Timing Diagram						
	Probe Current Start		570	850	550	710	870	mV
	First Measurement		910	1200	890	1055	1220	mV
	Second Measurement		910	1240	890	1080	1270	mV
V_1	Probe Input Voltage Range	V_{CC} = 7.5V–18V			1		V_{REG} − 1.0	V
V_5	Probe Open-Circuit Threshold	At Pin 5			V_{REG} − 0.85	V_{REG} − 0.6		V
V_5	Probe Short-Circuit Threshold					0.6	0.85	V
I_1	Pin 1 Input Leakage Current	Pin 1 = 300 mV	−3.5	+3.5			+5.0	nA
I_{15}	Pin 15 Leakage Current	V_{15} = 2V, V_7 = 12V	−3.5	3.5				μA
	Pin 15 Charging Current	V_{15} = 4V, V_7 = 12V	60					μA
f_9	Lamp Oscillation Frequency	C_L = 3.3 μF			0.5	1.5	2.5	Hz
I_9	Lamp Driver Current	Flashing Mode					600	mA
V_9	Lamp Driver Saturation	I_9 = 200 mA		200			250	mA

Electrical Characteristics (Continued)

V_{CC} = 12V, C_T = 33 μF, R_T = 7.5 kΩ, T_A within operating range except where stated otherwise

Symbol	Parameter	Conditions	Tested Limits (Note 2)		Design Limits (Note 3)			Units
			Min	Max	Min	Typ	Max	
V_{14}	Auxiliary Output Voltage	Lamp OFF			5.0			V
		Lamp ON					1.2	V
V_1	Alarm Level	(Difference Between First and Second Measurement)			230	280	330	mV

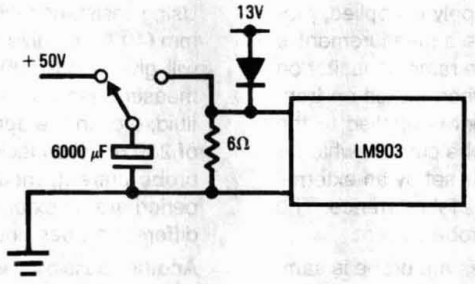
Sensitivity to Electrostatic Discharge: Pins 7, 10, 13, and 14 will withstand greater than 1500V when tested using 100 pF and 1500Ω in accordance with National Semiconductor standard ESD test procedures. All other pins will withstand in excess of 2 kV.

Note 1: Test circuit for overvoltage capability at pins 3, 6, 7.

Note 2: Guaranteed 100% production tested at 25°C. These limits are used to calculate outgoing quality levels.

Note 3: Limits guaranteed to include parametric variations. T_A = −40°C to +80°C and from V_{CC} = 7.5V–18V. These limits are not used to calculate AOQL figures.

Note 4: Variations over temperature range are not production tested.



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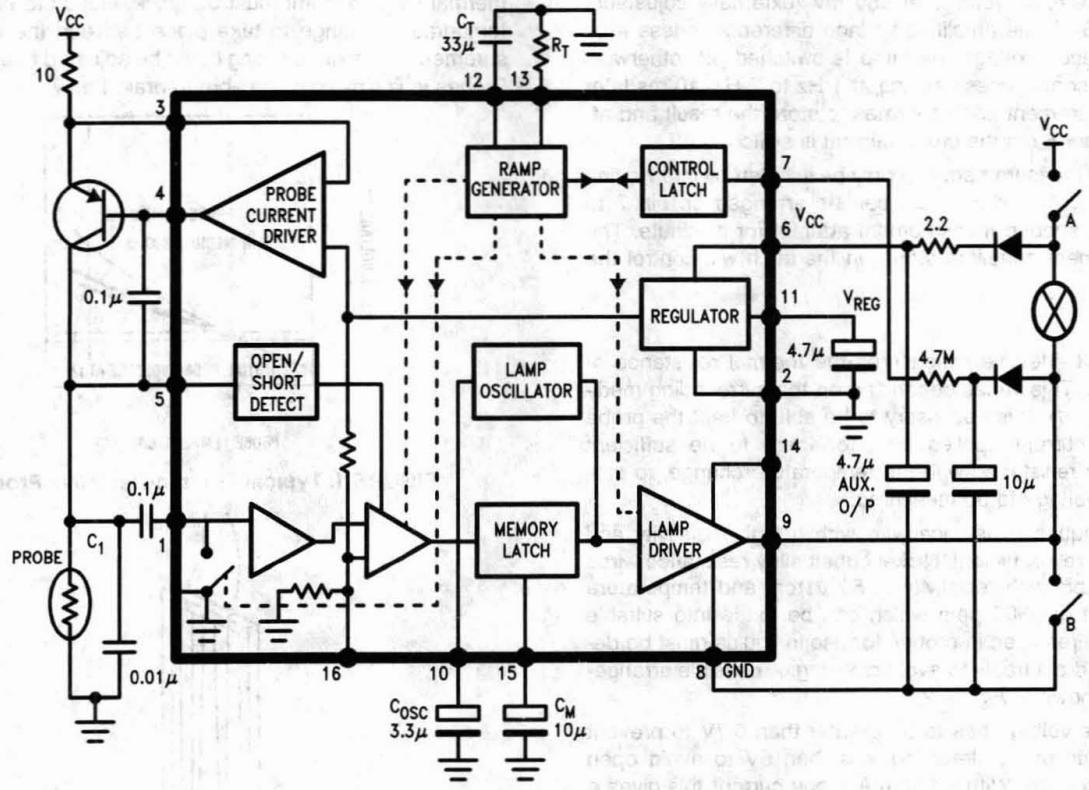
In Lamp ON condition, I_9 should be limited to 600 mA.

Block and Application Circuit



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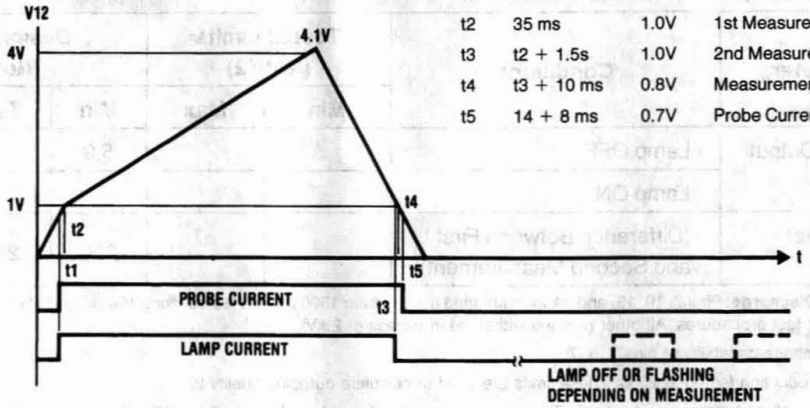
Memory capacitor on pin 15 is set

High—Lamp off

Low—Lamp on

Circuit Timing Diagram



t1	25 ms	0.7V	Threshold
t2	35 ms	1.0V	1st Measurement
t3	t2 + 1.5s	1.0V	2nd Measurement
t4	t3 + 10 ms	0.8V	Measurement Latched
t5	14 + 8 ms	0.7V	Probe Current Off

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Circuit Operation

A measurement is initiated when the supply is applied, provided the control input pin 7 is low. Once a measurement is commenced, pin 7 is latched low and the ramp capacitor on pin 12 begins to charge. After 25 ms when switch-on transients have subsided, a constant current is applied to the thermo-resistive probe. The value of probe current, which is supplied by an external PNP transistor, is set by an external resistor across an internally generated 21V reference. The lamp current is applied at the start of probe current.

35 ms after switch-on, the voltage across the probe is sampled and held on external capacitor C1 (leakage current at pin 1 less than 1 nA). After a further 1.5 seconds the difference between the present probe voltage and the initial probe voltage is measured, multiplied by 3 and compared with a reference voltage of 850 mV (externally adjustable via pin 16). If the amplified voltage difference is less than the reference voltage the lamp is switched off, otherwise the lamp commences flashing at 1 Hz to 2 Hz. 10 ms later the measurement latch operates to store the result and after a further 8 ms the probe current is switched off.

A second measurement can only be initiated by interrupting the supply. An external CR can be arranged on pin 7 to prevent a second measurement attempt for 1 minute. The measurement condition stored in the latch will control the lamp.

PROBES

The circuit effectively measures the thermal resistance of the probe. This varies depending on the surrounding medium (*Figure 1*). It is necessary to be able to heat the probe with the current applied and, for there to be sufficient change in resistance with the temperature change, to provide the voltage to be measured.

Probes require resistance wire with a high resistivity and temperature coefficient. Nickel cobalt alloy resistance wires are available with resistivity of 50 $\mu\Omega$cm and temperature coefficient of 3300 ppm which can be made into suitable probes. Wires used in probes for use in liquids must be designed to drain freely to avoid clogging. A possible arrangement is shown in *Figure 2*.

The probe voltage has to be greater than 0.7V to prevent short circuit probe detection less than 5V to avoid open circuit detection. With a 200 mA probe current this gives a probe resistance range of 4Ω to 25Ω. This low value makes it possible to use the probe in partially conducting fluids.

Using resistance wire of 50 $\mu\Omega$cm resistivity, 8 cm of 0.08 mm (40 AWG) give approximately 8Ω at 25°C. Such a probe will give about 500 mV change between first and second measurements in air, and 100 mV change with oil, hydraulic fluid, etc., in the application circuit. With an alarm threshold of 280 mV (typ) lack of fluid can readily be detected. As the probe current, measurement reference and measurement period are all externally adjustable, there is freedom to use different probes and fluids.

Another possibility is the use of high temperature coefficient resistors made for special applications and positive temperature coefficient thermistors. The encapsulation must have a sufficiently low thermal resistance so as not to mask the change due to the different surrounding mediums, and the thermal time constant must be quick enough to enable the temperature change to take place between the two measurements. The ramp timing could be adjusted to assist this. Probes in liquids must be able to drain freely.

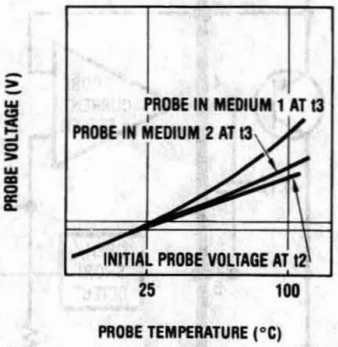

FIGURE 1. Typical Thermo-Resistive Probe

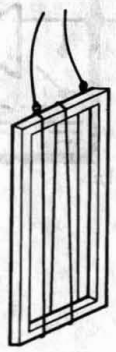

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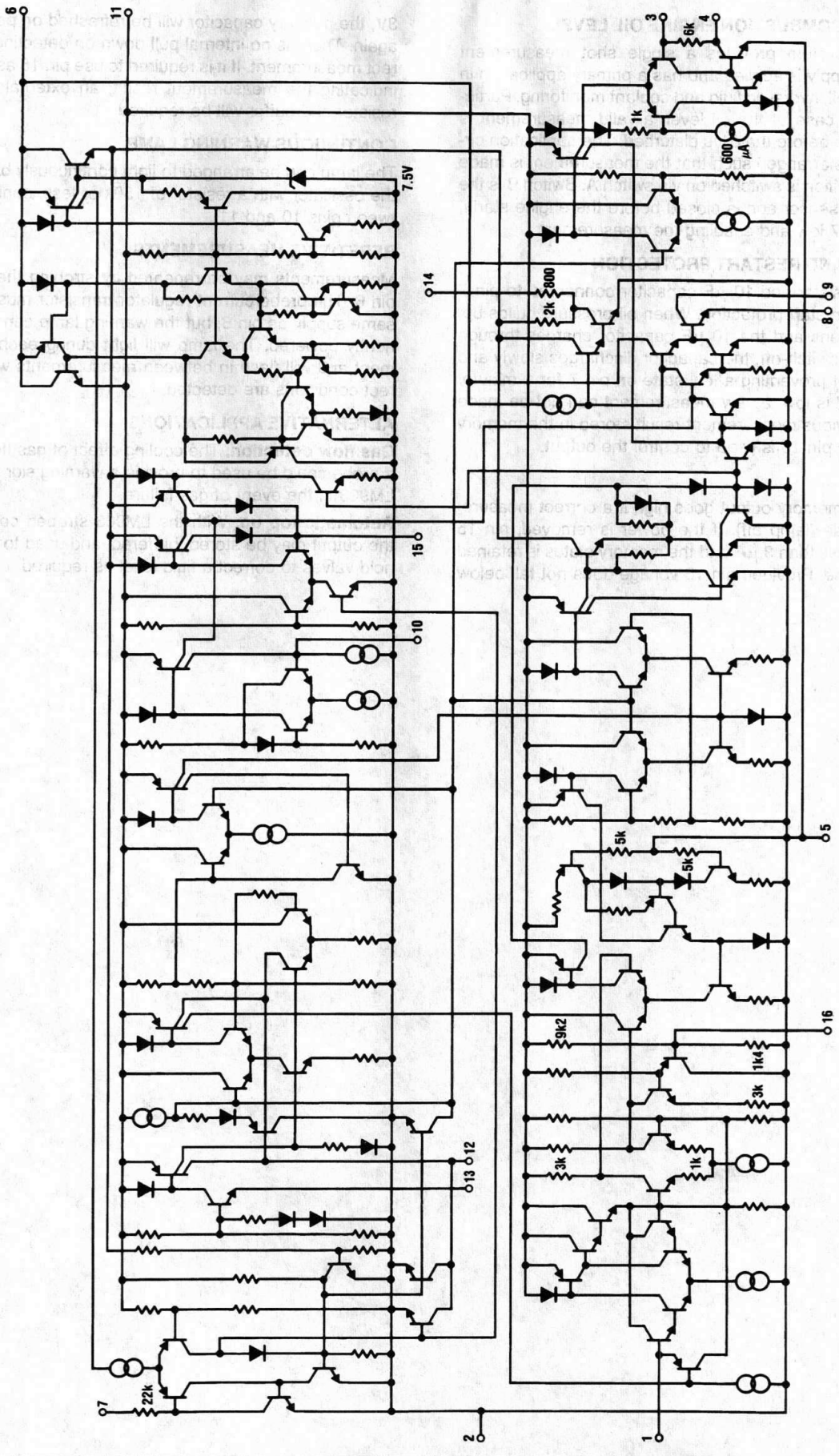
FIGURE 2

Equivalent Schematic Diagram



Application Hints

INTERNAL COMBUSTION ENGINE OIL LEVEL

The basic system provides a single shot measurement when the supply is applied and has a primary application in automotive oil, hydraulic fluid and coolant monitoring. Particularly in the case of the oil level, a valid measurement is only possible before the oil is disturbed. The application circuit shown is arranged such that the measurement is made when the ignition is switched on via switch A. Switch B is the oil pressure sensor and is closed before the engine starts, keeping pin 7 low and enabling the measurement.

STALLING AND RESTART PROTECTION

The 4M7 resistor and 10 μF capacitor connected to pin 7 provide the restart protection. When oil pressure builds up, switch B opens and the 10 μF capacitor charges through the bulb. At switch-off, the capacitor discharges slowly and is capable of preventing a low state on pin 7 for 1 minute. Unless pin 7 is low, a new measurement can not be made and the previous measurement result stored in the memory capacitor on pin 15 is used to control the output.

MEMORY

The pin 15 memory output goes high if a correct measurement is made (lamp off). If the power is removed, pin 15 leakage is less than 3 μA and the memory status is retained for some time. Provided pin 15 voltage does not fall below 3V, the memory capacitor will be refreshed on powering up again. There is no internal pull down on detecting an incorrect measurement. If it is required to use pin 15 as an output indicating the measurement result, an external pull down resistor and buffer will be required.

CONTINUOUS WARNING LAMP

The lamp can be arranged to light continuously by disabling the oscillator with a resistor of 150k or less, connected between pins 10 and 11.

REPETITIVE MEASUREMENTS

Measurements may be repeated by strobing the supply to pin 6. The probe current regulator transistor must have the same supply as pin 6, but the warning lamp can be permanently powered. The lamp will light during each measurement and will flash in between measurements when incorrect conditions are detected.

ALTERNATIVE APPLICATIONS

Gas flow detection: The cooling effect of gas flowing over a probe could be used to provide a warning signal from the LM903 in the event of gas failure.

Automatic top up: With the LM903 strobed continuously, the output may be stored, buffered, and used to drive solenoid valves to correct a fluid level as required.

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LM1042 Fluid Level Detector

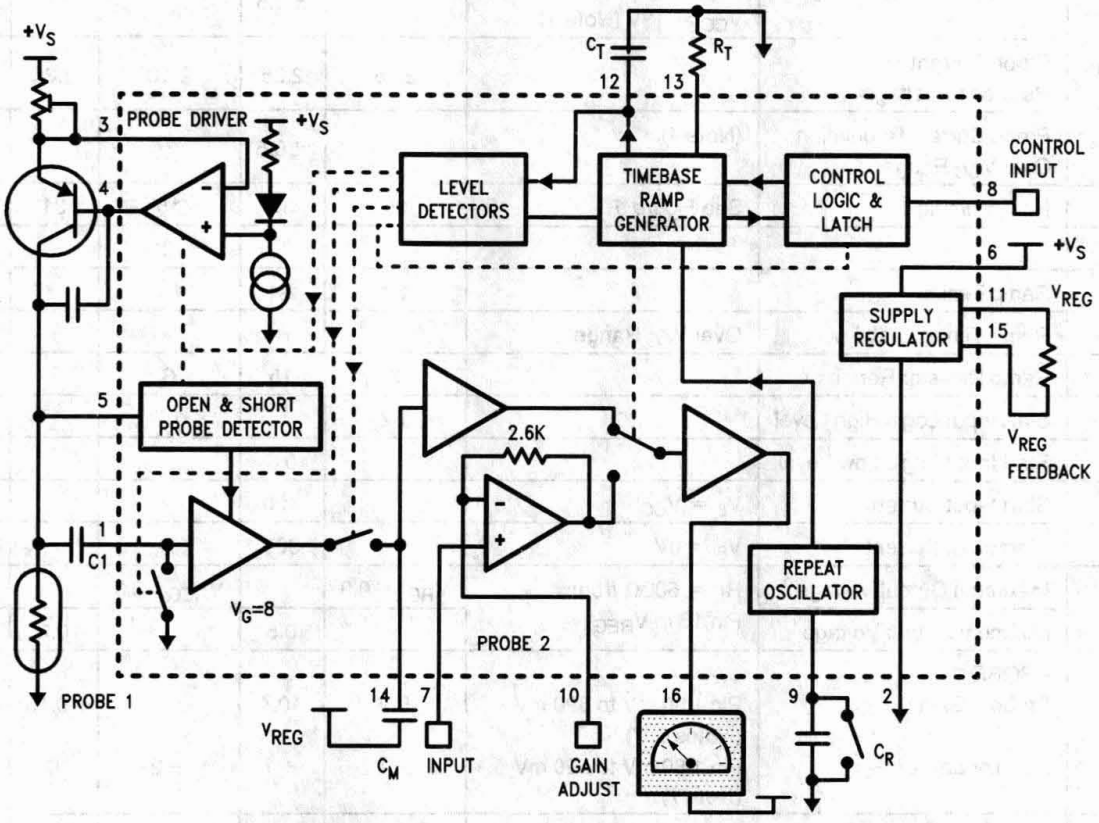
General Description

The LM1042 uses the thermal-resistive probe technique to measure the level of non-flammable fluids. An output is provided proportional to fluid level and single shot or repeating measurements may be made. All supervisory requirements to control the thermal-resistive probe, including short and open circuit probe detection, are incorporated within the device. A second linear input for alternative sensor signals may also be selected.

Features

- Selectable thermal-resistance or linear probe inputs
- Control circuitry for thermal-resistive probe
- Single-shot or repeating measurements
- Switch on reset and delay to avoid transients
- Output amplifier with 10 mA source and sink capability
- Short or open probe detection
- +50V transient protection on supply and control input
- 7.5V to 18V supply range
- Internally regulated supply
- −40°C to +80°C operation

Block Diagram



TL/H/8709–1

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage V_{CC}	32V
Voltage at Pin 8	32V
Positive Peak Voltage (Pins 6, 8, 3) (Note 1) 10 ms 2A	50V
Output Current Pin 4, (I_4)(sink)	10 mA
Output Current Pin 11 (source)	25 mA
Output Current Pin 16	±10 mA
Operating Temperature Range	−40°C to +80°C
Storage Temperature Range	−55°C to +150°C
Lead Temperature (Soldering 10 sec.)	260°C
Package Power Dissipation T_A = 25°C (Note 8)	1.8W
Device Power Dissipation	0.9W

Electrical Characteristics

V_{CC} = 13V, T_A within operating range except where stated otherwise. C_T = 22 μF, R_T = 12k

Symbol	Parameter	Conditions	Tested Limits (Note 2)		Design Limits (Note 3)			Units
			Min	Max	Min	Typ	Max	
V_{CC}	Supply Voltage		7.5	18	7.5	13	18	V
I_S	Supply Current			35			35	mA
V_{REG}	Regulated Voltage	Pins 15 and 11 connected	5.7	6.15	5.65	5.9	6.2	V
	Stability Over V_{CC} Range	Referred to value at V_{CC} = 13V (Note 4)		±0.5			±0.5	%
V_6-V_3	Probe Current Reference Voltage		2.15	2.35	2.10	2.25	2.40	V
	Probe Current Regulation Over V_{CC} Range	(Note 4)		±0.5			±0.8	%
T_1	Ramp Timing	See *Figure 5*	20	37	15	31	42	ms
T_2-T_1					3		16	ms
T_4-T_1	Ramp Timing		1.4	2.1	1.4	1.75	2.1	s
T_{STAB}	Ramp Timing Stability	Over V_{CC} Range		+5			±5	%
R_T	Ramp Resistor Range		3	15	3		15.0	kΩ
V_8	Start Input Logic High Level		1.7		1.7			V
V_8	Start Input Logic Low Level			0.5			0.5	V
I_8	Start Input Current	$V_8 = V_{CC}$		100			100	nA
I_8	Start Input Current	V_8 = 0V		300			300	nA
V_{16}	Maximum Output Voltage	R_L = 600Ω from Pin 16 to V_{REG}	$V_{REG}-0.3$		$V_{REG}-0.3$			V
	Minimum Output Voltage			0.5		0.2	0.6	V
	PROBE 1							
G_1	Probe 1 Gain	Pin 1 80 mV to 520 mV (Notes 6, 7)	9.9	10.4		10.15		
	Non-linearity of G_1	Pin 1 80 mV to 520 mV (Note 7)	−1	+1	−2	0	2	%
OS_1	Pin 1 Offset	(Note 7)				±5		mV
	PROBE 2							
G_2	Probe 2 Gain	Pin 7 240 mV to 1.562V (Note 7)	3.31	3.49		3.4		
	Non-linearity of G_2	Pin 7 240 mV to 1.562V (Note 7)	−1	+1	−2	0.2	2	%
OS_7	Pin 7 Offset	(Note 7)				±5		mV
R_7	Input impedance					5		MΩ

Electrical Characteristics

V_{CC} = 13V, T_A within operating range except where stated otherwise. C_T = 22 μF, R_T = 12k (Continued)

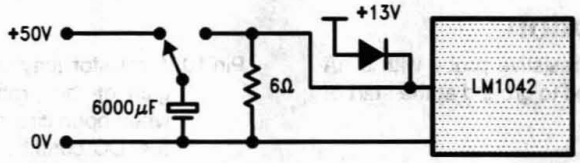
Symbol	Parameter	Conditions	Tested Limits (Note 2)		Design Limits (Note 3)			Units
			Min	Max	Min	Typ	Max	
V_1	Probe 1 Input Voltage Range	V_{CC} = 9V to 18V V_{CC} = 7.5V, I_4 < 2.5 mA (V_{REG} = 6.0V)	1	5	1 1		5 3.5	V V
V_5	Probe 1 Open Circuit Threshold	At Pin 5	$V_{REG}-0.7$	$V_{REG}-0.5$	$V_{REG}-0.85$	$V_{REG}-0.6$	$V_{REG}-0.35$	V
V_5	Probe 1 Short Circuit Threshold		0.5	0.7	0.35	0.6	0.85	V
I_{14}	Pin 14 Input Leakage Current	Pin 14 = 4V	−2.0	2.0			2.0	nA
I_1	Pin 1 Input Leakage Current	Pin 1 = 300 mV	−5.0	5.0		1.5	5.0	nA
T_R	Repeat Period	C_R = 22 μF (Note 5)	12	28	9.1	17	36	s
	C_R Discharge Time	C_R = 22 μF				70	135	ms
C_M	Memory Capacitor Value						0.47	μF
C_1	Input Capacitor Value						0.47	μF

Sensitivity fo Electrostatic Discharge—

Pins 7, 10, 13, and 14 will withstand greater than 1500V when tested using 100 pF and 1500Ω in accordance with National Semiconductor standard ESD test procedures.

All other pins will withstand in excess of 2 kV.

Note 1: Test circuit for over voltage capability at pins 3, 6, 8.



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Note 2: Guaranteed and 100% production tested at 25°C. These limits are used to calculate outgoing quality levels.

Note 3: Limits guardbanded to include parametric variations. T_A = −40°C to +80°C and from V_{CC} = 7.5V to 18V. These limits are not used to calculate AOQL figures.

Note 4: Variations over temperature range are not production tested.

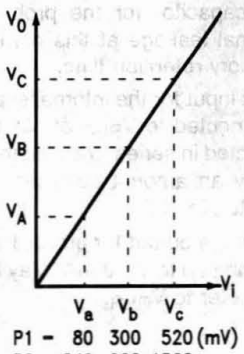
Note 5: Time for first repeat period, see *Figure 6*.

Note 6: Probe 1 amplifier tests are measured with pin 12 ramp voltage held between the T_3 and T_4 conditions (pin 12 ≈ 1.1V) having previously been held above 4.1V to simulate ramp action. See Figure 5.

Note 7: When measuring gain separate ground wire sensing is required at pin 2 to ensure sufficiently accurate results.

Linearity is defined as the difference between the predicted value of V_B (V_B*) and the measured value.

Note 8: Above T_A = 25°C derate with θ_{jA} = 70°C/W.



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For probe 1 and probe 2—Gain (G) = $\frac{V_C - V_A}{V_c - V_a}$

Input offset = $\left[\frac{V_C}{G} - V_c\right]$

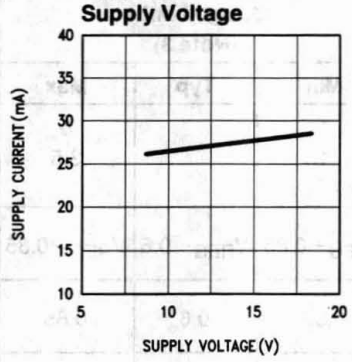
Linearity = $\left[\frac{V_B^*}{V_B} - 1\right] \times 100\%$

$V_B^* = V_A + G(V_b - V_a)$

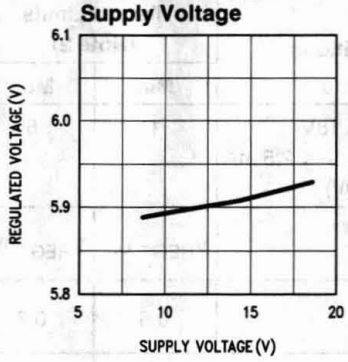
3

Typical Performance Characteristics

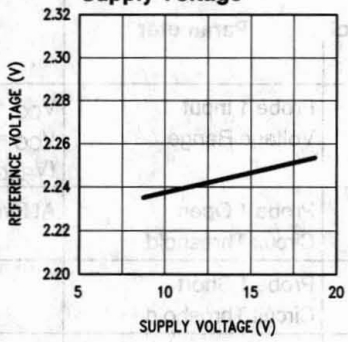
Supply Current vs Supply Voltage



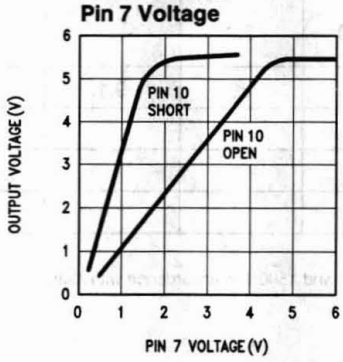
Regulated Voltage vs Supply Voltage



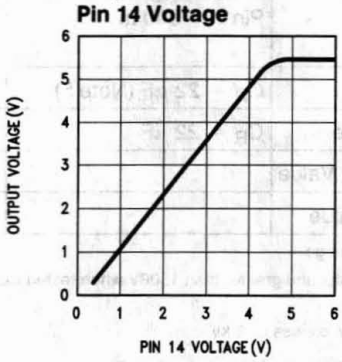
Probe Reference V vs Supply Voltage



Output Voltage vs Pin 7 Voltage



Output Voltage vs Pin 14 Voltage



TL/H/8709–3

Pin Function Description

Pin 1 Input amplifier for thermo-resistive probe with 5 nA maximum leakage. Clamped to ground at the start of a probe 1 measurement.

Pin 2 Device ground — 0V.

Pin 3 This pin is connected to the emitter of an external PNP transistor to supply a 200 mA constant current to the thermo-resistive probe. An internal reference maintains this pin at $V_{SUPPLY} - 2V$.

Pin 4 Base connection for the external PNP transistor.

Pin 5 This pin is connected to the thermo-resistive probe for short and open circuit probe detection.

Pin 6 Supply pin, +7.5V to +18V, protected against +50V transients.

Pin 7 High Impedance input for second linear voltage probe with an input range from 1V to 5V. The gain may be set externally using pin 10.

Pin 8 Probe select and control input. If this pin is taken to a logic low level, probe 1 is selected and the timing cycle is initiated. The selection logic is subsequently latched low until the end of the measurement. If kept at a low level one shot or repeating probe 1 measurements will be made depending upon pin 9 conditions. A high input level selects probe 2 except during a probe 1 measurement period.

Pin 9 The repeat oscillator timing capacitor is connected from this pin to ground. A 2 μA current charges up the capacitor towards 4.3V when the probe 1 measurement cycle is restarted. If this pin is grounded the repeat oscillator is disabled and only one probe 1 measurement will be made when pin 8 goes low.

Pin 10 A resistor may be connected to ground to vary the gain of the probe 2 input amplifier. Nominal gain when open circuit is 1.2 and when shorted to ground 3.4. DC conditions may be adjusted by means of a resistor divider network to V_{REG} and ground.

Pin 11 Regulated voltage output. Requires to be connected to pin 15 to complete the supply regulator control loop.

Pin 12 The capacitor connected from this pin to ground sets the timing cycle for probe 1 measurements.

Pin 13 The resistor connected between this pin and ground defines the charging current at pin 12. Typically 12k, the value should be within the range 3k to 15k.

Pin 14 A low leakage capacitor, typical value 0.1 μF and not greater than 0.47 μF, should be connected from this pin to the regulated supply at pin 11 to act as a memory capacitor for the probe 1 measurement. The internal leakage at this pin is 2 nA max for a long memory retention time.

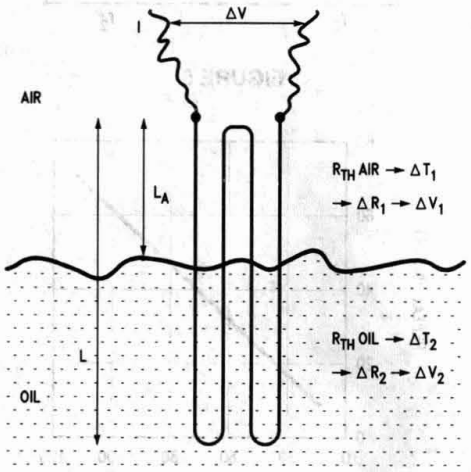
Pin 15 Feedback input for the internal supply regulator, normally connected to V_{REG} at pin 11. A resistor may be connected in series to adjust the regulated output voltage by an amount corresponding to the 1 mA current into pin 15.

Pin 16 Linear voltage output for probe 1 and probe 2 capable of driving up to ±10 mA. May be connected with a 600Ω meter to V_{REG}.

Application Notes

THERMO-RESISTIVE PROBES — OPERATION AND CONSTRUCTION

These probes work on the principle that when power is dissipated within the probe, the rise in probe temperature is dependent on the thermal resistance of the surrounding material and as air and other gases are much less efficient conductors of heat than liquids such as water and oil it is possible to obtain a measurement of the depth of immersion of such a probe in a liquid medium. This principle is illustrated in *Figure 1*.



TL/H/8709–4

FIGURE 1

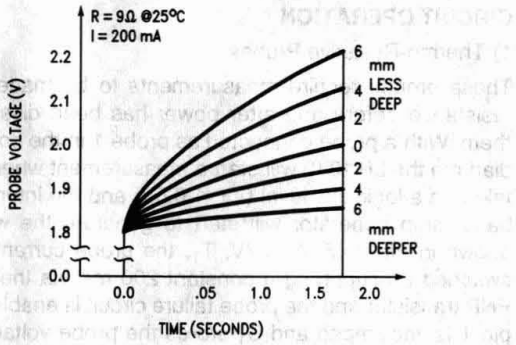
During the measurement period a constant current drive I is applied to the probe and the voltage across the probe is sampled both at the start and just before the end of the measurement period to give ΔV. R_{TH} Air and R_{TH} Oil represent the different thermal resistances from probe to ambient in air or oil giving rise fo temperature changes ΔT_1 and ΔT_2 respectively. As a result of these temperature changes the probe resistance will change by ΔR_1 or ΔR_2 and give corresponding voltage changes ΔV_1 or ΔV_2 per unit length.

Hence

$$\Delta V = \frac{L_A}{L}\Delta V_1 + \frac{(L - L_A)}{L}\Delta V_2$$

and for $\Delta V_1 > \Delta V_2$, R_{TH} Air > R_{TH} Oil, ΔV will increase as the probe length in air increases. For best results the probe needs to have a high temperature coefficient and low thermal time constant. One way to achieve this is to make use of resistance wires held in a suitable support frame allowing free liquid access. Nickel cobalt iron alloy resistance wires are available with resistivity 50 μΩcm and 3300 ppm temperature coefficient which when made up into a probe with 4 × 2 cm 0.08 mm diameter strands between supports (10 cm total) can give the voltage vs time curve shown in *Figure 2* for 200 mA probe current. The effect of varying the probe current is shown in *Figure 3*. To avoid triggering the probe failure detection circuits the probe voltage must be between 0.7V and 5.3V (V_{REG} − 6V), hence for 200 mA the permissible probe resistance range is from 3.5Ω to 24Ω. The example given has a resistance at room temperature of 9Ω which leaves plenty of room for increase during measurements and changes in ambient temperature.

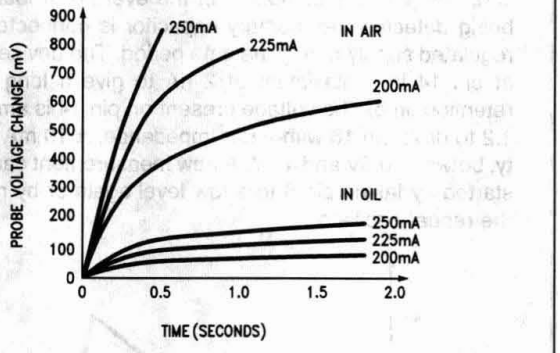
Various arrangements of probe wire are possible for any given wire gauge and probe current to suit the measurement range required, some examples are illustrated schematically in *Figure 4*. Naturally it is necessary to reduce the probe



TL/H/8709–5

FIGURE 2

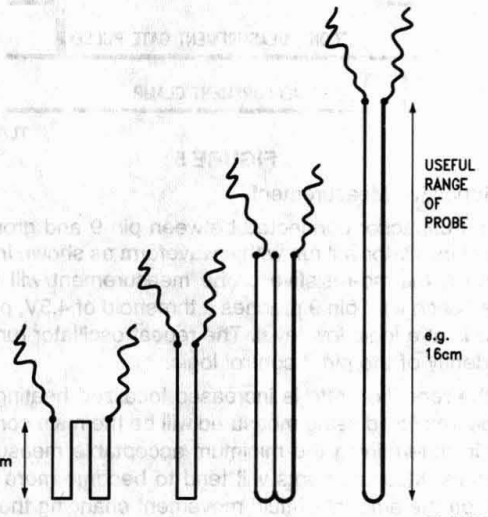
current with very fine wires to avoid excessive heating and this current may be optimized to suit a particular type of wire. The temperature changes involved will give rise to noticeable length changes in the wire used and more sophisticated holders with tensioning devices may be devised to allow for this.



TL/H/8709–6

FIGURE 3

Probes need not be limited to resistance wire types as any device with a positive temperature coefficient and sufficiently low thermal resistance to the encapsulation so as not to mask the change due to the different surrounding mediums, could be used. Positive temperature coefficient thermistors are a possibility and while their thermal time constant is likely to be longer than wire the measurement time may be increased by changing C_T to suit.



TL/H/8709–7

FIGURE 4

3

Application Notes (Continued)

CIRCUIT OPERATION

1) Thermo-Resistive Probes

These probes require measurements to be made of their resistance before and after power has been dissipated in them. With a probe connected as probe 1 in the connection diagram the LM1042 will start a measurement when pin 8 is taken to a logic low level ($V_8 < 0.5V$) and the internal time-base ramp generator will start to generate the waveform shown in *Figure 5*. At 0.7V, T_1, the probe current drive is switched on supplying a constant 200 mA via the external PNP transistor and the probe failure circuit is enabled. At 1V pin 1 is unclamped and C_1 stores the probe voltage corresponding to this time, T_2. The ramp charge rate is now reduced as C_T charges toward 4V. As the 4.1V threshold is passed a current sink is enabled and C_T now discharges. Between 1.3V and 1.0V, T_3 and T_4, the amplified pin 1 voltage, representing the change in probe voltage since T_2 (and as the current is constant this is proportional to the resistance change) is gated onto the memory capacitor at pin 14. At 0.7V, T_5, the probe current is switched off and the measurement cycle is complete. In the event of a faulty probe being detected the memory capacitor is connected to the regulated supply during the gate period. The device leakage at pin 14 is a maximum of 2 nA to give a long memory retention time. The voltage present on pin 14 is amplifed by 1.2 to drive pin 16 with a low impedance, ±10 mA capability, between 0.5V and 4.7V. A new measurement can only be started by taking pin 8 to a low level again or by means of the repeat oscillator.

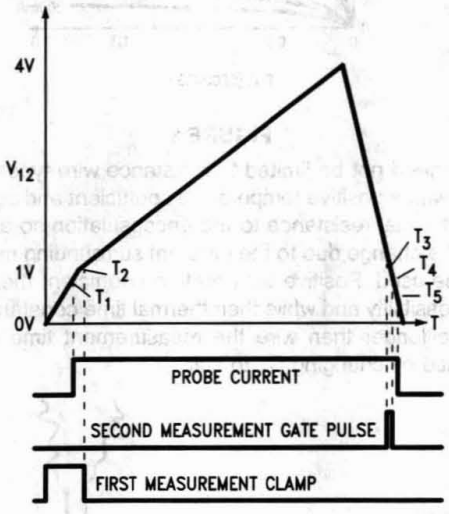


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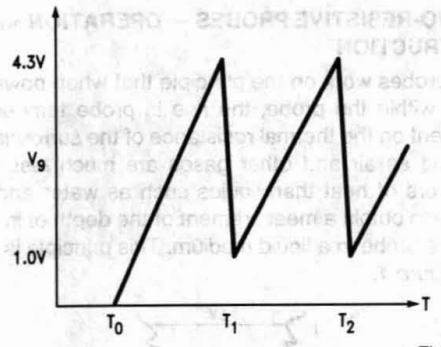
FIGURE 5

2) Repetitive Measurement

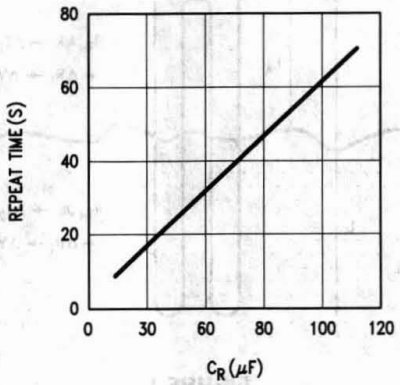
With a capacitor connected between pin 9 and ground the repeat oscillator will run with a waveform as shown in *Figure 6* and a thermo-resistive probe measurement will be triggered each time pin 9 reaches a threshold of 4.3V, provided pin 8 is at a logic low level. The repeat oscillator runs independently of the pin 8 control logic.

As the repetition rate is increased localized heating of the probe and liquid being measured will be the main consideration in determining the minimum acceptable measurement intervals. Measurements will tend to become more dependent on the amount of fluid movement changing the rate of heat transfer away from the probe. The typical repeat time versus timing capacitor value is shown in *Figure 7*.



TL/H/8709–9

FIGURE 6



TL/H/8709–10

FIGURE 7

3) Second Probe Input

A high impedance input for an alternative sensor is available at pin 7. The voltage applied to this input is amplified and output at pin 16 when the input is selected with a high level on pin 8. The gain is defined by the feedback arrangement shown in *Figure 8* with adjustment possible at pin 10. With pin 10 open the gain is set at a nominal value of 1.2, and this may be increased by connecting a resistor between pin 10 and ground up to a maximum of 3.4 with pin 10 directly grounded. A variable resistor may be used to calibrate for the variations in sensitivity of the sensor used for probe 2.

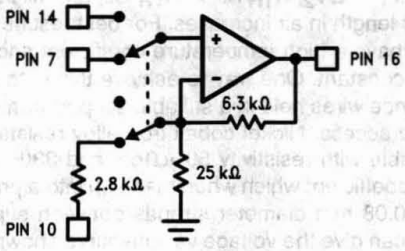


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FIGURE 8

POWER SUPPLY REGULATOR

The arrangement of the feedback for the supply regulator is shown in *Figure 9*. The circuit acts to maintain pin 15 at a constant 6V and when directly connected to pin 11 the regulated output is held at 6V. If required a resistor R may be connected between pins 15 and 11 to increase the output voltage by an amount corresponding typically to 1 mA flowing in R. In this way a variable resistor may be used to trim out the production tolerance of the regulator by adjusting for $V_{REG} \geq 6.2V$.

Application Notes (Continued)

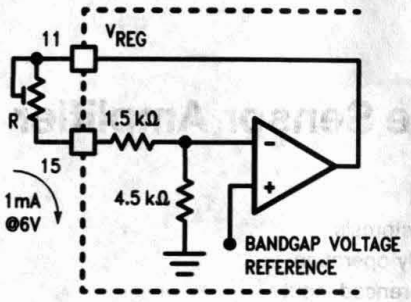

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FIGURE 9

PROBE CURRENT REFERENCE CIRCUIT

The circuit defining the probe circuit is given in *Figure 10.* A reference voltage is obtained from a bandgap regulator derived current flowing in a diode resistor chain to set up a voltage 2 volts below the supply. This is applied to an amplifier driving an external PNP transistor to maintain pin 3 at 2V below supply. The emitter resistance from pin 3 to supply defines the current which, less the base current, flows in the probe. Because of the sensitivity of the measurement to probe current evident in *Figure 3* the current should be adjusted by means of a variable resistor to the desired value. This adjustment may also be used to take out probe tolerances.

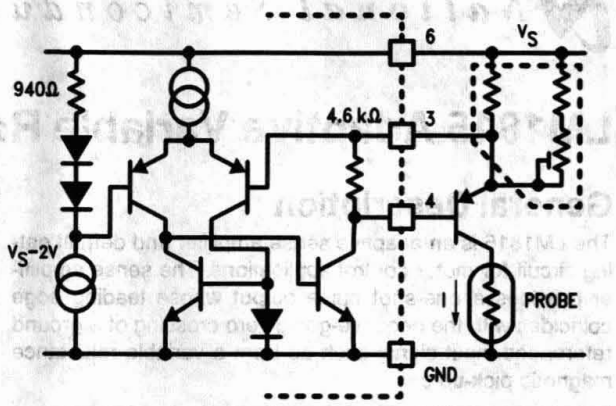

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FIGURE 10

TYPICAL APPLICATIONS CIRCUIT

A typical automotive application circuit is shown in *Figure 11* where the probe selection signal is obtained from the oil pressure switch. At power up (ignition on) the oil pressure switch is closed and pin 8 is held low by R4 causing a probe 1 (oil level) measurement to be made. Once the engine has started the oil pressure switch opens and D1 pulls pin 8 high changing over to the second auxiliary probe input. The capacitor C_5 holds pin 8 high in the event of a stalled engine so that a second probe 1 measurement can not occur in disturbed oil. Non-automotive applications may drive pin 8 directly with a logic signal.

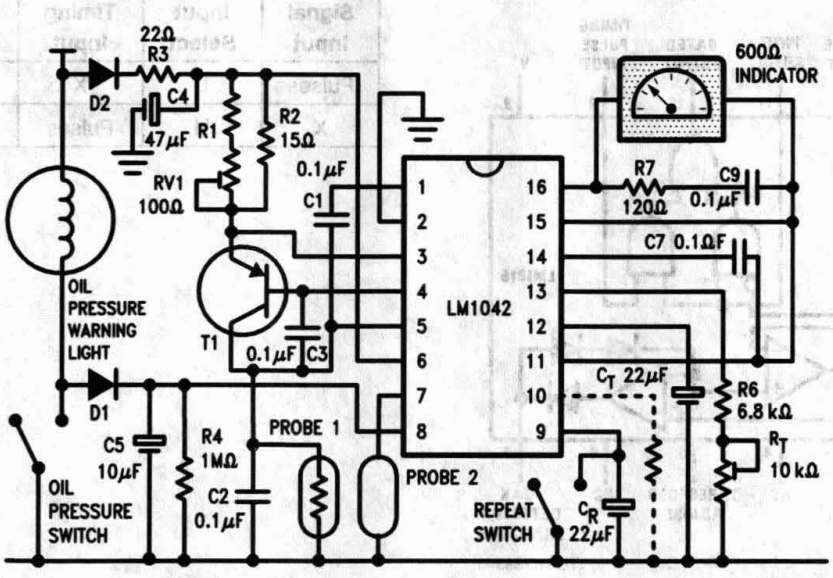

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FIGURE 11. Typical Application Circuit

National Semiconductor

LM1815 Adaptive Variable Reluctance Sensor Amplifier

General Description

The LM1815 is an adaptive sense amplifier and default gating circuit for motor control applications. The sense amplifier provides a one-shot pulse output whose leading edge coincides with the negative-going zero crossing of a ground referenced input signal such as from a variable reluctance magnetic pick-up coil.

In normal operation, this timing reference signal is processed (delayed) externally and returned to the LM1815. A logic input is then able to select either the timing reference or the processed signal for transmission to the output driver stage.

The adaptive sense amplifier operates with a positive-going threshold which is derived by peak detecting the incoming signal and dividing this down. Thus the input hysteresis varies with input signal amplitude. This enables the circuit to sense in situations where the high speed noise is greater than the low speed signal amplitude. Minimum input signal is 100 mVp-p.

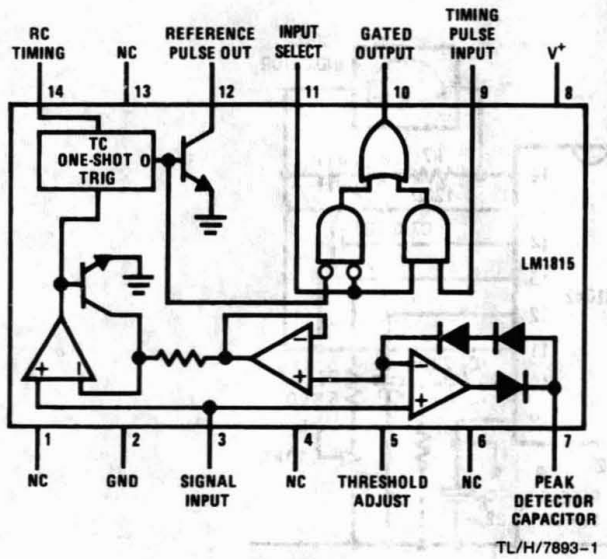
Features

- Adaptive hysteresis
- Single supply operation
- Ground referenced input
- True zero crossing timing reference
- Operates from 2V to 12V supply voltage
- Handles inputs from 100 mV to over 120V with external resistor
- CMOS compatible logic

Applications

- Position sensing with notched wheels
- Zero crossing switch
- Motor speed control
- Tachometer
- Engine testing

Connection Diagram



TL/H/7893–1

Top View

Order Number LM1815M or LM1815N
See NS Package Number M14A or N14A

Truth Table

Signal Input	Input Select	Timing Input	Gated Output
Pulses	L	X	Pulses
X	H	Pulses	Pulses

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	12V
Power Dissipation (Note 1)	1250 mW
Operating Temperature Range	−40°C to +125°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature (Note 2)	+125°C
Input Current	±30 mA
Lead Temperature (Soldering, 10 sec.)	260°C

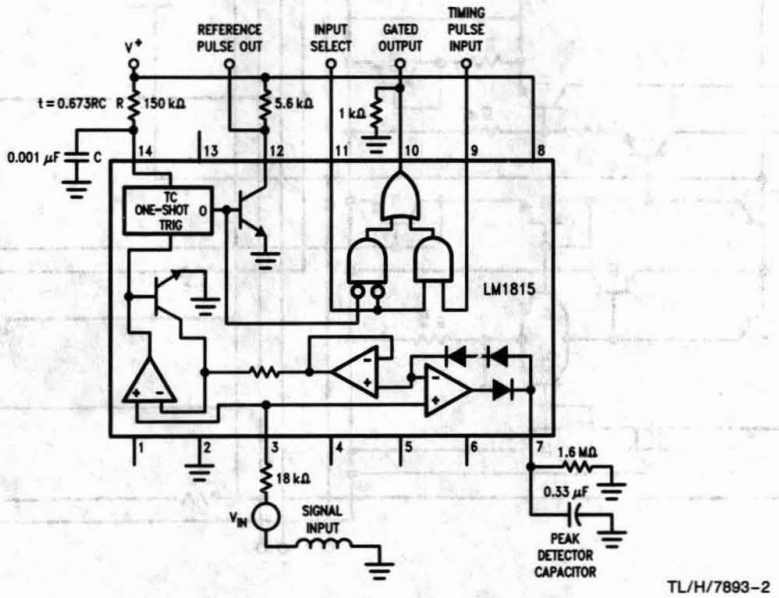
Electrical Characteristics (T_A = 25°C, V_{CC} = 10V, unless otherwise specified, see *Figure 1*)

Parameter	Conditions	Min	Typ	Max	Units
Operating Supply Voltage		2.5	10	12	V
Supply Current	f_{IN} = 500 Hz, Pin 9 = 2V, Pin 11 = 0.8V		3.6	6	mA
Reference Pulse Width	f_{IN} = 1 Hz to 2 kHz	70	100	130	μs
Input Bias Current	V_{IN} = 2V, (Pin 9 and Pin 11)			5	μA
Input Bias Current	V_{IN} = 0V dc, (Pin 3)		200		nA
Input Impedance	V_{IN} = 5 Vrms, (Note 3)	12	20	28	kΩ
Zero Crossing Threshold	V_{IN} = 100 mVp-p, (Pin 3)			25	mV
Logic Threshold	(Pin 9 and Pin 11)	0.8	1.1	2.0	V
V_{OUT} High	R_L = 1 kΩ, (Pin 10)	7.5	8.6		V
V_{OUT} Low	I_{SINK} = 0.1 mA, (Pin 10)		0.3	0.4	V
Input Arming Threshold	Pin 5 Open, $V_{IN} \leq$ 135 mVp-p	30	45	60	mV
	Pin 5 Open, $V_{IN} \geq$ 230 mVp-p	40	80	90	% of V_3 Pk
	Pin 5 to V^+	200			mV
	Pin 5 to Gnd	−25		25	mV
Output Leakage Pin 12	V_{12} = 11V		0.01	10	μA
Saturation Voltage P12	I_{12} = 2 mA		0.2	0.4	V

Note 1: For operation at elevated temperatures, the device must be derated based on a 125°C maximum junction temperature and a thermal resistance of 80°C/W (DIP), 120 °C/W (SO-14) junction to ambient.

Note 2: Temporary excursions to 150°C can be tolerated.

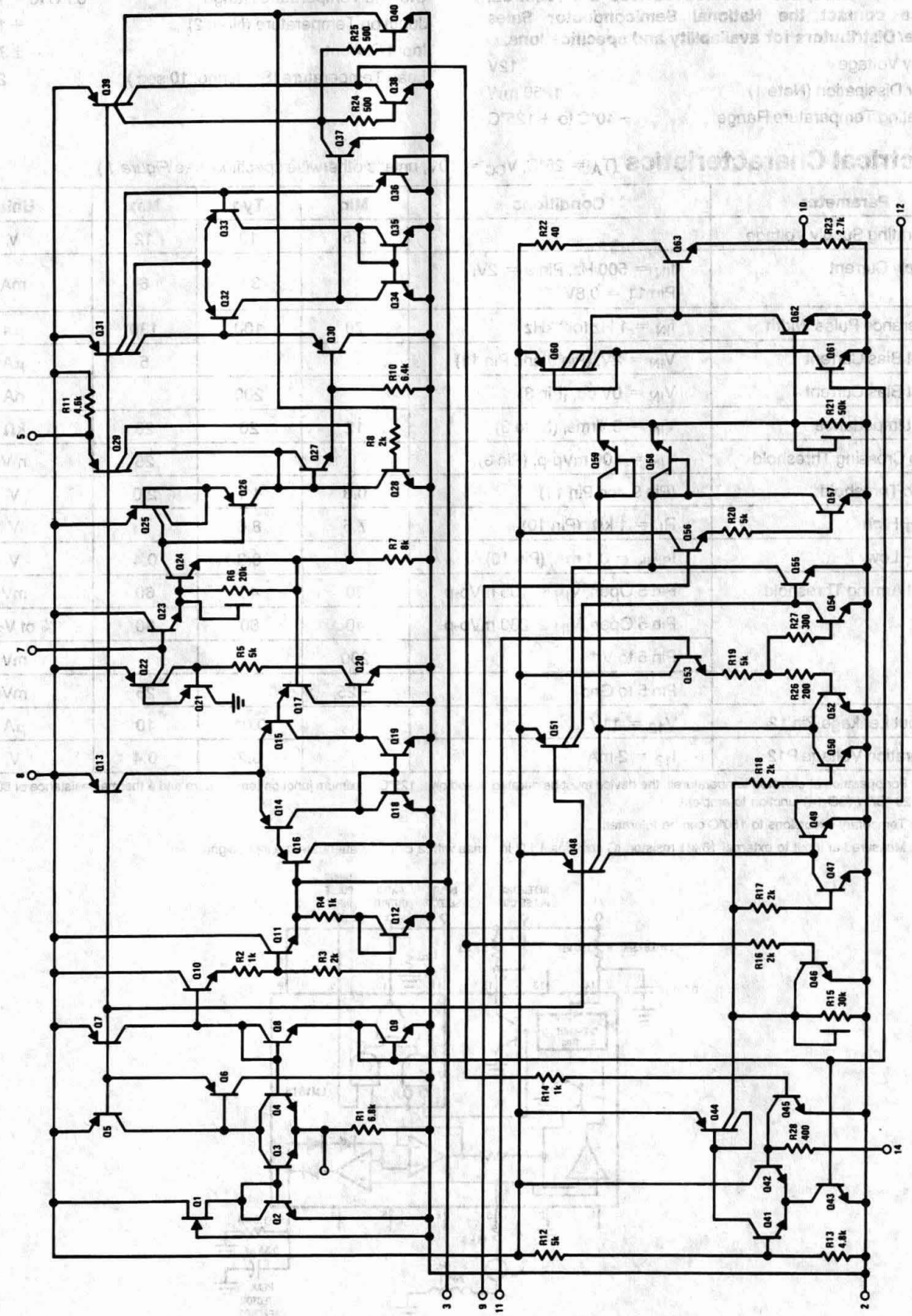
Note 3: Measured at input to external 18 kΩ resistor. IC contains 1 kΩ in series with a diode to attenuate the input signal.



TL/H/7893–2

FIGURE 1. LM1815 Adaptive Sense Amplifier

Schematic Diagram



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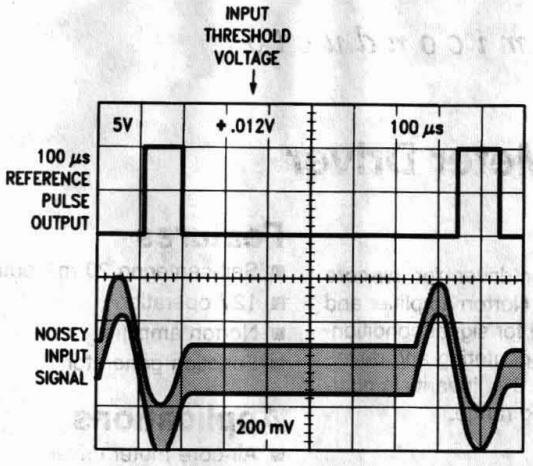


TL/H/7893–3

FIGURE 2. LM1815 Oscillograms

Application Hints

Input Clamp

The signal input at pin 3 is internally clamped. Current limit is provided by an external resistor which should be selected to allow a peak current of 3 mA in normal operation. Positive inputs are clamped by a 1 kΩ resistor and series diode, while an active clamp limits pin 3 to −350 mV for negative inputs (see R4, Q12, Q11 in internal schematic diagram).

Operation of Zero Crossing Detector

The LM1815 is designed to operate as a zero crossing detector, triggering an internal one shot on the negative-going edge of the input signal. Unlike other zero crossing detectors, the LM1815 cannot be triggered until the input signal has crossed an "arming" threshold on the positive-going portion of the waveform. The arming circuit is reset when the chip is triggered, and subsequent zero crossings are ignored until the arming threshold is exceeded again. This threshold varies depending on the connection at pin 5. Three different modes of operation are possible:

MODE 1, Pin 5 open. The adaptive mode is selected by leaving pin 5 open circuit. For input signals of less than 135 mVp-p, the input arming threshold is typically 45 mV. Under these conditions the input signal must first cross the 45 mV threshold in the positive direction to arm the zero crossing detector, and then cross zero in the negative direction to trigger it. If the signal is less than 30 mV peak (minimum rating in Electrical Characteristics), the one shot is guaranteed to not trigger.

Input signals of greater than 230 mVp-p cause the arming threshold to track at 80% of the peak input voltage. A peak detector (pin 7) stores a value relative to the positive input peaks to establish the arming threshold. Input signals must exceed this threshold in the positive direction to arm the zero crossing detector, which can then be triggered by a negative-going zero crossing. The peak detector tracks rapidly as the input signal amplitude increases, and decays by virtue of the resistor connected externally at pin 7 to track decreases in the input signal.

Note that since the input is clamped, the waveform observed at pin 3 is not identical to the waveform observed at the variable reluctance sensor. Similarly, the voltage stored at pin 7 is not identical to the peak voltage appearing at pin 3.

MODE 2, Pin 5 connected to V+. The input arming threshold is fixed at 200 mV minimum when pin 5 is connected to the positive supply. The chip has no output for signals of less than 200 mV peak, and triggers on the next negative-going zero crossing when the threshold is exceeded.

MODE 3, Pin 5 grounded. With pin 5 grounded, the input arming threshold is set to 0V (±25 mV maximum). Positive-going zero crossings arm the chip, and the next negative zero crossing triggers it.

The one shot timing is set by a resistor and capacitor connected to pin 14. The output pulse width is

$$\text{pulse width} = 0.673\,RC \qquad (1)$$

In some systems it is necessary to externally generate pulses, such as during stall conditions when the variable reluctance sensor has no output. External pulse inputs at pin 9 are gated through to pin 10 when Input Select (pin 11) is pulled high. Pin 12 is a direct output for the one shot and is unaffected by the status of pin 11.

Input/output pins 9, 11, 10 and 12 are all CMOS logic compatible. In addition, pins 9, 11 and 12 are TTL compatible. Pin 10 is not guaranteed to drive a TTL load.

Pins 1, 4, 6 and 13 have no internal connections and can be grounded.

National Semiconductor

LM1819 Air-Core Meter Driver

General Description

The LM1819 is a function generator/driver for air-core (moving-magnet) meter movements. A Norton amplifier and an NPN transistor are included on chip for signal conditioning as required. Driver outputs are self-centering and develop ±4.5V swing at 20 mA. Better than 2% linearity is guaranteed over a full 305-degree operating range.

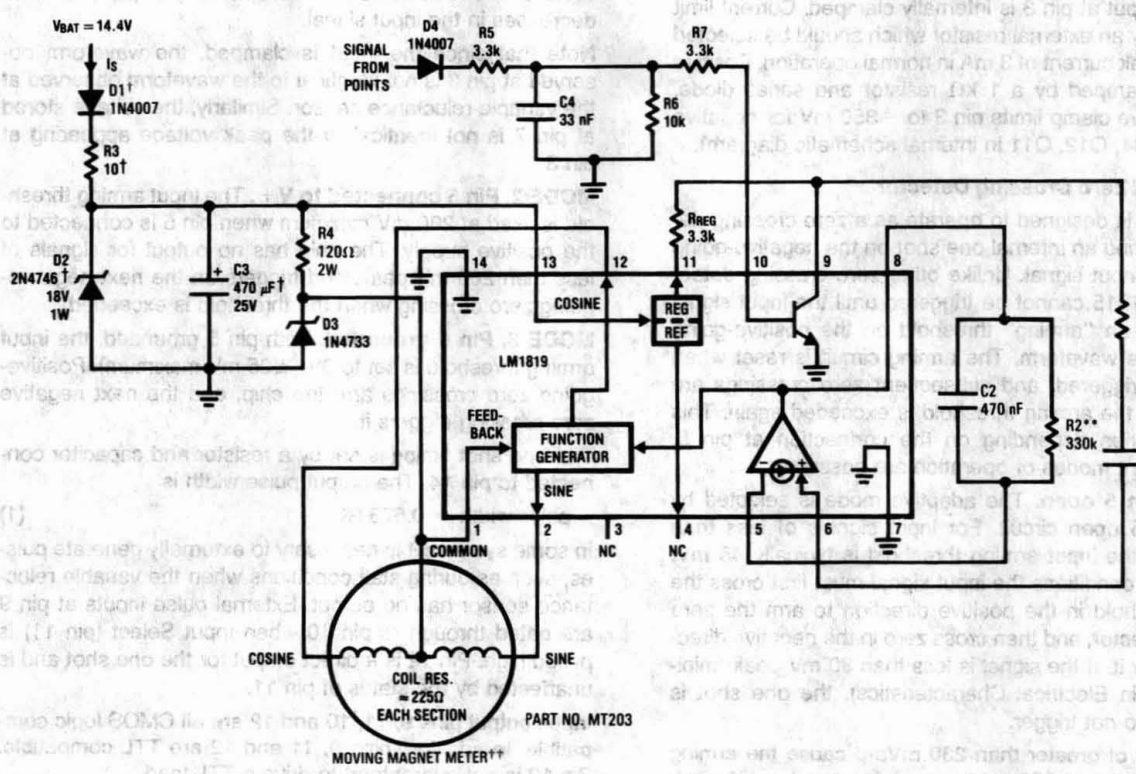
Features

- Self-centering 20 mA outputs
- 12V operation
- Norton amplifier
- Function generator

Applications

- Air-core meter driver
- Tachometers
- Ruggedized instruments

Typical Application



TL/H/5263–1

FIGURE 1. Automotive Tachometer Application. Circuit shown operates with 4 cylinder engine and deflects meter pointer (270°) at 6000 RPM.

Order Number LM1819M or LM1819N
See NS Package Number M14A or N14A

*TRW Type X463UW Polycarbonate Capacitor

**RN60D Low TC Resistor (±100 ppm)

†Components Required for Automotive Load Dump Protection

††Available from FARIA Co.
P O Box 983, Uncasville, CT 06382
Tel. 203-848-9271

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage, V^+ (pin 13)	20V
Power Dissipation (note 1)	1300 mW
Operating Temperature	−40°C to +85°C
Storage Temperature	−65°C to −150°C
Lead Temp. (Soldering, 10 seconds)	260°C
BV_{CEO}	$20V_{MIN}$

Electrical Characteristics V_S = 13.1V T_A = 25°C unless otherwise specified

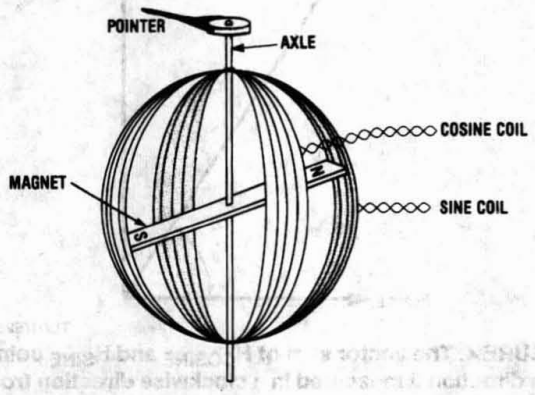
Symbol	Parameter	Pin(s)	Conditions	Min	Typ	Max	Units
I_S	Supply Current	13	Zero Input Frequency (See *Figure 1*)			65	mA
V_{REG}	Regulator Voltage	11	I_{REG} = 0 mA	8.1	8.5	8.9	V
	Regulator Output Resistance	11	I_{REG} = 0 mA to 3 mA		13.5		Ω
V_{REF}	Reference Voltage	4	I_{REF} = 0 mA	1.9	2.1	2.3	V
	Reference Output Resistance	4	I_{REF} = 0 μA to 50 μA		5.3		kΩ
	Norton Amplifier Mirror Gain	5, 6	I_{BIAS} ≅ 20 μA	0.9	1.0	1.1	
h_{FE}	NPN Transistor DC Gain	9, 10			125		
	Function Generator Feedback Bias Current	1	V_1 = 5.1V		1.0		mA
	Drive Voltage Extremes, Sine and Cosine	2, 12	I_{LOAD} = 20 mA	±4	±4.5		V
	Sine Output Voltage with Zero Input	2	$V_8 = V_{REF}$	−350	0	+350	mV
	Function Generator Linearity		FSD = 305°			±1.7	%FSD
k	Function Generator Gain		Meter Deflection/ΔV_8	50.75	53.75	56.75	°/V

Note 1: For operation above 25°C, the LM1819 must be derated based upon a 125°C maximum junction temperature and a thermal resistance of 76°C/W which applies for the device soldered in a printed circuit board and operating in a still-air ambient.

Application Hints

AIR-CORE METER MOVEMENTS

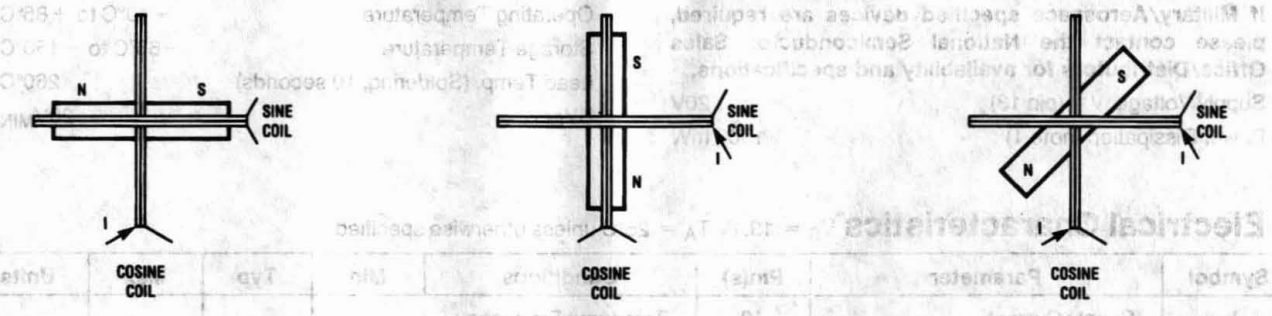
Air-core meters are often favored over other movements as a result of their mechanical ruggedness and their independence of calibration with age. A simplified diagram of an air-core meter is shown in *Figure 2*. There are three basic pieces: a magnet and pointer attached to a freely rotating axle, and two coils, each oriented at a right angle with respect to the other. The only moving part in this meter is the axle assembly. The magnet will tend to align itself with the vector sum of **H** fields of each coil, where **H** is the magnetic field strength vector. If, for instance, a current passes through the cosine coil (the reason for this nomenclature will become apparent later) as shown in *Figure 3(a)*, the magnet will align its magnetic axis with the coil's **H** field. Similarly, a current in the sine coil (*Figure 3(b)*) causes the magnet to align itself with the sine **H** field. If currents are applied simultaneously to both sine and cosine coils, the magnet will turn to the direction of the vector sum of the two **H** fields *(Figure 3(c))*. **H** is proportional to the voltage applied to a coil. Therefore, by varying both the polarity and magnitude of the coil voltages the axle assembly can be made to rotate a full 360°. The LM1819 is designed to drive the meter through a minimum of 305°.



TL/H/5263–2

FIGURE 2. Simplified Diagram of an Air Core Meter.

Application Hints (Continued)



(a) (b) (c)

FIGURE 3. Magnet and pointer position are controlled by the H field generated by the two drive coils.

In an air-core meter the axle assembly is supported by two nylon bushings. The torque exerted on the pointer is much greater than that found in a typical d'Arsonval movement. In contrast to a d'Arsonval movement, where calibration is a function of spring and magnet characteristics, air-core meter calibration is only affected by the mechanical alignment of the drive coils. Mechanical calibration, once set at manufacture, can not change.

Making pointer position a linear function of some input is a matter of properly ratioing the drive to each coil. The **H** field contributed by each coil is a function of the applied current, and the current is a function of the coil voltage. Our desired result is to have θ (pointer deflection, measured in degrees) proportional to an input voltage:

$$\theta = kV_{IN} \qquad [1]$$

where k is a constant of proportionality, with units of degrees/volt. The vector sum of each coils' **H** field must follow the deflection angle θ. We know that the axle assembly always points in the direction of the vector sum of $\mathbf{H}_{SINE}$ and $\mathbf{H}_{COSINE}$. This direction (see *Figure 4*) is found from the formula:

$$(\theta) = \arctan \{ |\mathbf{H}_{SINE}| / |\mathbf{H}_{COSINE}| \} \qquad [2]$$

Recalling some basic trigonometry,

$$(\theta) = \arctan(\sin(\theta) / \cos(\theta)) \qquad [3]$$

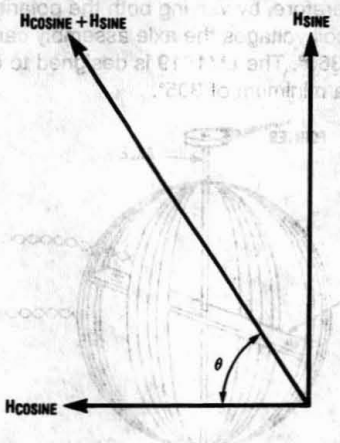


FIGURE 4. The vector sum of $\mathbf{H}_{COSINE}$ and $\mathbf{H}_{SINE}$ points in a direction θ measured in a clockwise direction from $\mathbf{H}_{COSINE}$.

Comparing [3] to [2] we see that if $\mathbf{H}_{SINE}$ varies as the sine of θ, and $\mathbf{H}_{COSINE}$ varies as the cosine of θ, we will generate a net **H** field whose direction is the same as θ. And since the axle assembly aligns itself with the net **H** field, the pointer will always point in the direction of θ.

THE LM1819

Included in the LM1819 is a function generator whose two outputs are designed to vary approximately as the sine and cosine of an input. A minimum drive of ± 20 mA at ± 4V is available at pins 2 (sine) and 12 (cosine). The common side of each coil is returned to a 5.1V zener diode reference and fed back to pin 1.

For the function generator, $k \cong 54°/V$ (in equation 1). The input (pin 8) is internally connected to the Norton amplifier's output. V_{IN} as considered in equation [1] is actually the difference of the voltages at pins 8 (Norton output/function generator input) and 4. Typically the reference voltage at pin 4 is 2.1V. Therefore,

$$\theta = k(V_8 - V_{REF}) = 54\ (V_8 - 2.1) \qquad [4]$$

As V_8 varies from 2.1V to 7.75V, the function generator will drive the meter through the chip's rated 305° range.

Air-core meters are mechanically zeroed during manufacture such that when only the cosine coil is driven, the pointer indicates zero degrees deflection. However, in some applications a slight trim or offset may be required. This is accomplished by sourcing or sinking a DC current of a few microamperes at pin 4.

A Norton amplifier is available for conditioning various input signals and driving the function generator. A Norton amplifier was chosen since it makes a simple frequency to voltage converter. While the non-inverting input (pin 6) bias is at one diode drop above ground, the inverting input (5) is at 2.1V, equal to the pin 4 reference. Mirror gain remains essentially flat to $I_{MIRROR} = 5$ mA. The Norton amplifier's output (8) is designed to source current into its load. To bypass the Norton amplifier simply ground the non-inverting input, tie the inverting input to the reference, and drive pin 8 (Norton output/function generator input) directly.

An NPN transistor is included on chip for buffering and squaring input signals. Its usefulness is exemplified in *Figures 1* & *6* where an ignition pulse is converted to a rectangular waveform by an RC network and the transistor. The emitter is internally connected to ground. It is important not to allow the base to drop below $-5V_{dc}$, as damage may occur. The 2.1V reference previously described is derived from an 8.5V regulator at pin 11. Pin 11 is used as a stable supply for collector loads, and currents of up to 5 mA are easily accommodated.

Application Hints (Continued)

TACHOMETER APPLICATION

A measure of the operating level of any motor or engine is the rotational velocity of its output shaft. In the case of an automotive engine the crankshaft speed is measured using the units "revolutions per minute" (RPM). It is possible to indirectly measure the speed of the crankshaft by using the signal present on the engine's ignition coil. The fundamental frequency of this signal is a function of engine speed and the number of cylinders and is calculated (for a four-stroke engine) from the formula:

$$f = n\omega/120 \quad \text{(Hz)} \quad (5)$$

where n = number of cylinders, and ω = rotational velocity of the crankshaft in RPM. From this formula the maximum frequency normally expected (for an 8 cylinder engine turning 4500RPM) is 300 Hz. In certain specialized ignition systems (motorcycles and some automobiles) where the coil waveform is operated at twice this frequency ($f = \omega/60$). These systems are identified by the fact that multiple coils are used in lieu of a single coil and distributor. Also, the coils have two outputs instead of one.

A typical automotive tachometer application is shown in *Figure 1*. The coil waveform is filtered, squared and limited by the RC network and NPN transistor. The frequency of the pulse train at pin 9 is converted to a proportional voltage by the Norton amplifier's charge pump configuration. The ignition circuit shown in *Figure 5* is typical of automotive systems. The switching element "S" is opened and closed in synchronism with engine rotation. When "S" is closed, energy is stored in Lp. When opened, the current in Lp diverts from "S" into C. The high voltage produced in Ls when "S" is opened is responsible for the arcing at the spark plug. The coil voltage (see *Figure 6*) can be used as an input to the LM1819 tachometer circuit. This waveform is essentially constant *duty cycle*. D4 rectifies this waveform thereby preventing negative voltages from reaching the chip. C4 and R5 form a low pass filter which attenuates the high frequency ringing, and R7 limits the input current to about 2.5mA. R6 acts as a base bleed to shut the transistor OFF when "S" is closed. The collector is pulled up to the internal regulator by R_{REG}. The output at pin 9 is a clean rectangular pulse.

Many ignition systems use magnetic, hall effect or optical sensors to trigger a solid state switching element at "S." These systems (see the LM1815) typically generate pulses of constant *width* and amplitude suitable for driving the charge pump directly.

The charge pump circuit in *Figure 7* can be operated in two modes: constant input pulse width (C1 acts as a coupling capacitor) and constant input duty cycle (C1 acts as a differentiating capacitor). The transfer functions for these two modes are quite diverse. However, deflection is always directly proportional to R2 and ripple is proportional to C2.

The following variables are used in the calculation of meter deflection:

symbol	description
n	number of cylinders
ω, ω_{IDLE}	engine speed at redline and idle, RPM
θ	pointer deflection at redline, degrees
δ	charge pump input pulse width, seconds
V_{IN}	peak to peak input voltages, volts
$\Delta\theta$	maximum desired ripple, degrees
k	function generator gain, degrees/volt
f, f_{IDLE}	input frequency at redline and idle, Hz

Where the NPN transistor and regulator are used to create a pulse $V_{IN} = 8.5V$. Acceptable ripple ranges from 3 to 10 degrees (a typical pointer is about 3 degrees wide) depending on meter damping and the input frequency.

The constant pulse width circuit is designed using the following equations:

(1) $$100\ \mu A < \frac{V_{IN}}{R1} < 3\ mA$$

(2) $$C_1 \geq \frac{10\delta}{R_1}$$

(3) $$R_2 = \frac{R_1\theta}{V_{IN}\delta k f} = \frac{120R_1\theta}{V_{IN}n\omega\delta k}$$

(4) $$C_2 = \frac{1}{R_2\Delta\theta f_{IDLE}} = \frac{1}{R_2\Delta\theta n\omega_{IDLE}}$$

The constant duty cycle equations are as follows:

$R_{REG} \geq 3\ k\Omega$

$R_1 \leq V_{IN} \times 10^4 - R_{REG}$

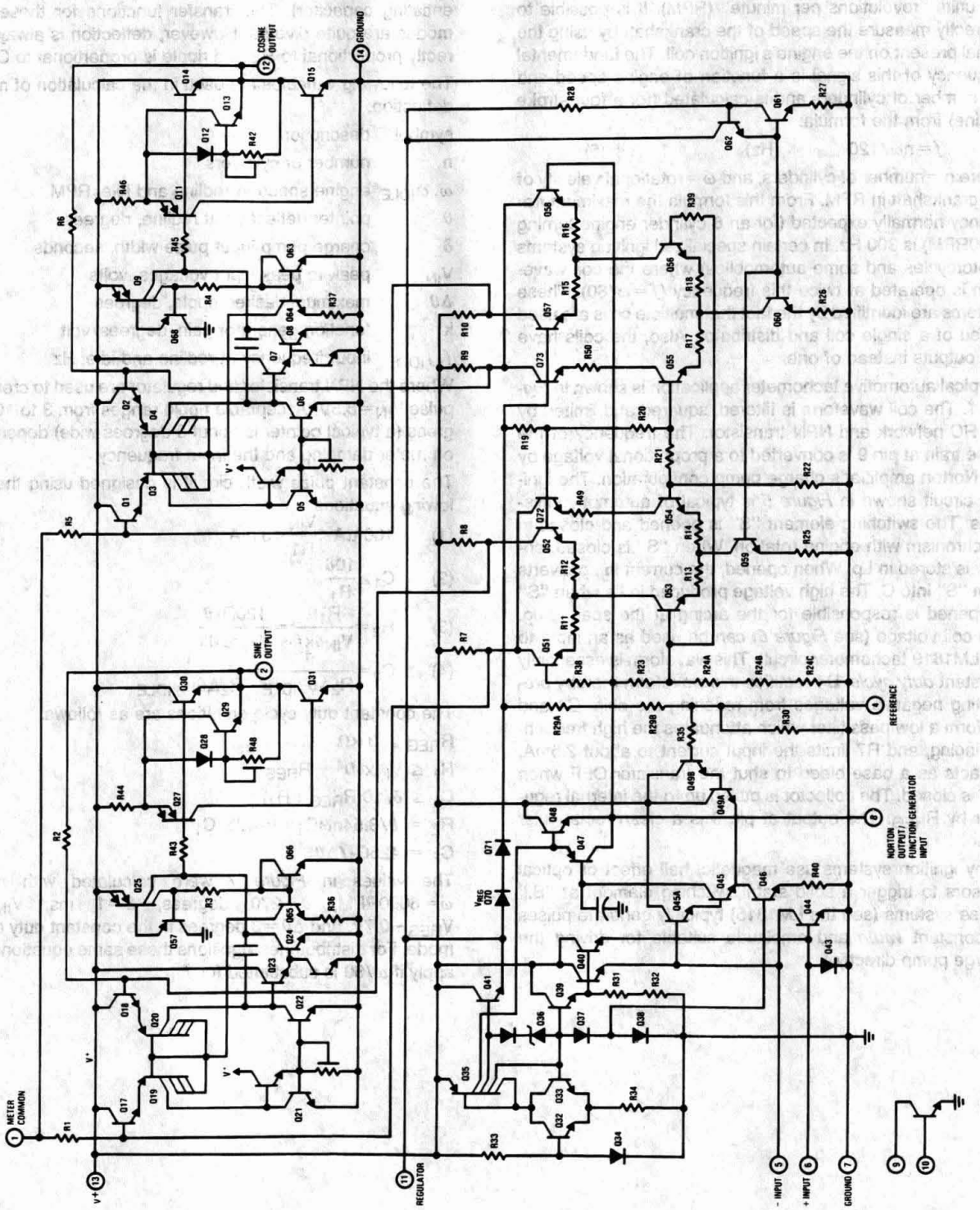
$C_1 \leq \delta/10(R_{REG} + R_1)$

$R_Z = \theta/3.54n\omega C_1 = \theta/425 f C_1$

$C_2 = 425C_1/\Delta\theta$

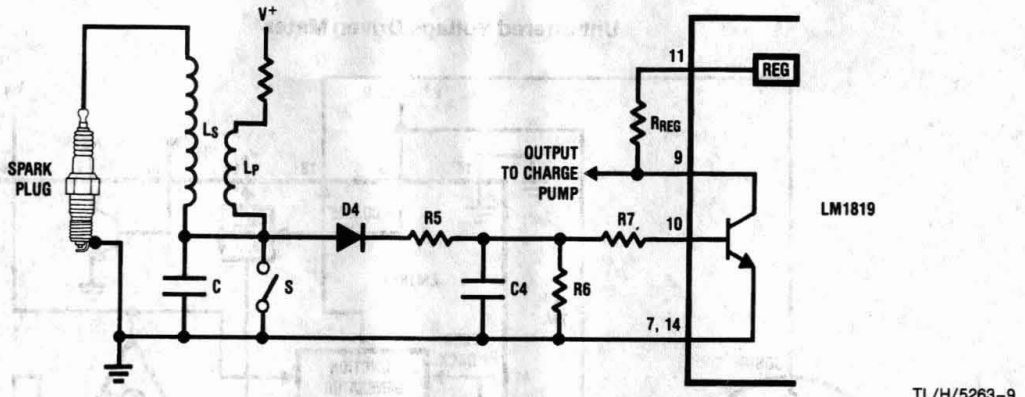
The values in *Figure 1* were calculated with n = 4, ω = 6000RPM, θ = 270 degrees, δ = 1 ms, V_{IN} is $V_{REG} - 0.7V$, and $\Delta\theta$ = 3 degrees in the constant duty cycle mode. For distributorless ignitions these same equations will apply if $\omega/60$ is substituted for f.

Equivalent Schematic



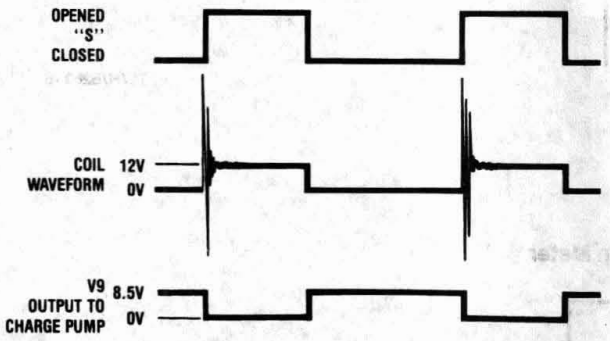
TL/H/5263–12

Typical Applications



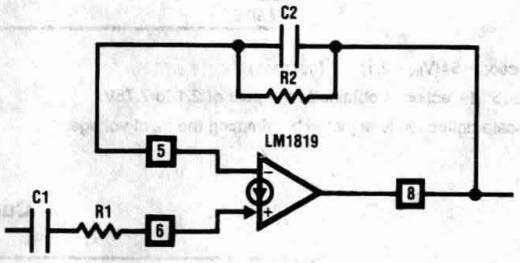
TL/H/5263–9

FIGURE 5. Typical Pulse-Squaring Circuit for Automotive Tachometers.



TL/H/5263–10

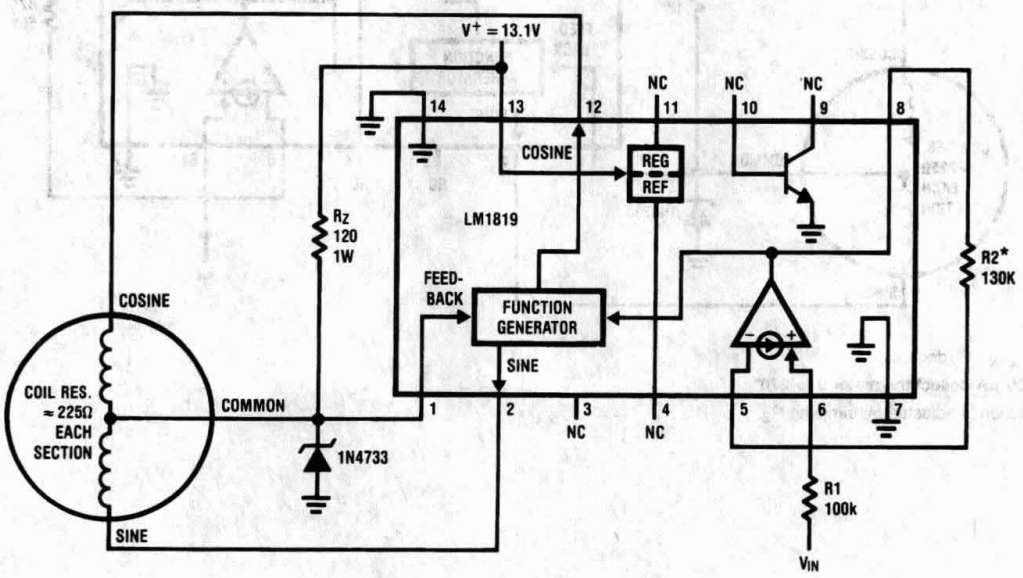
FIGURE 6. Waveforms Encountered in Automotive Tachometer Circuit.



TL/H/5263–11

FIGURE 7. Tachometer Charge Pump.

Voltage Driven Meter with Norton Amplifier Buffer



TL/H/5263–5

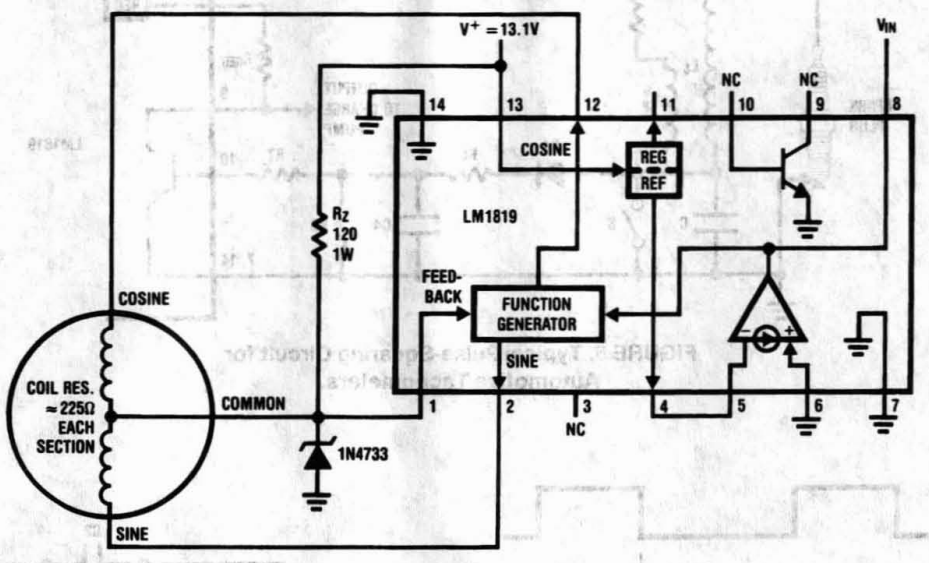
Deflection = 54 $(V_{IN} - .7)R_2/R_1$ (degrees)

0 to 305° deflection is obtained with .7 to 5V input.

*Full scale deflection is adjusted by trimming R_2.

Typical Applications (Continued)

Unbuffered Voltage Driven Meter



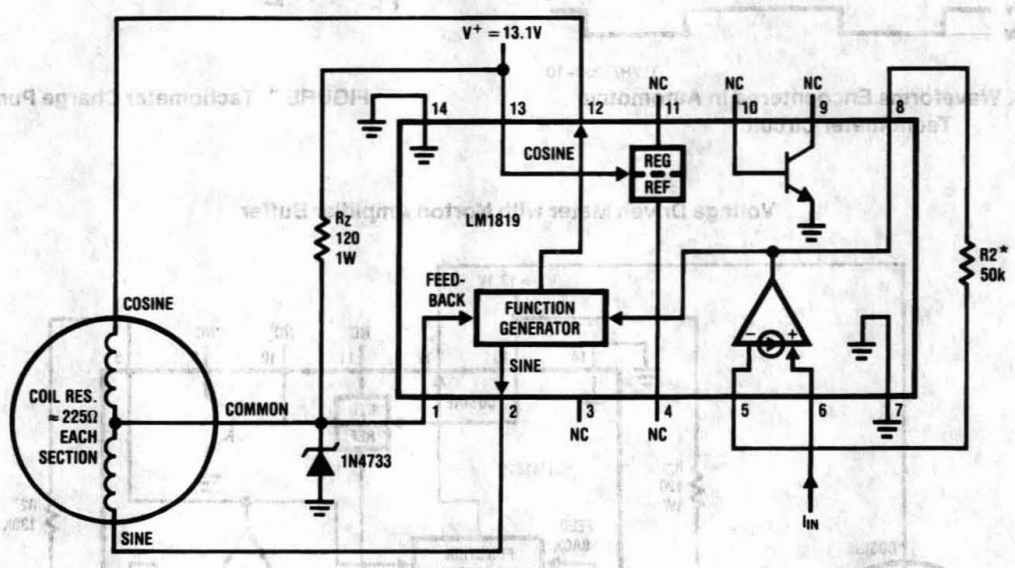
TL/H/5263–6

Deflection = $54(V_{IN} - 2.1)$ (degrees)

0 to 305° deflection is obtained for inputs of 2.1 to 7.75V.

Full scale deflection is adjusted by trimming the input voltage.

Current Driven Meter



TL/H/5263–7

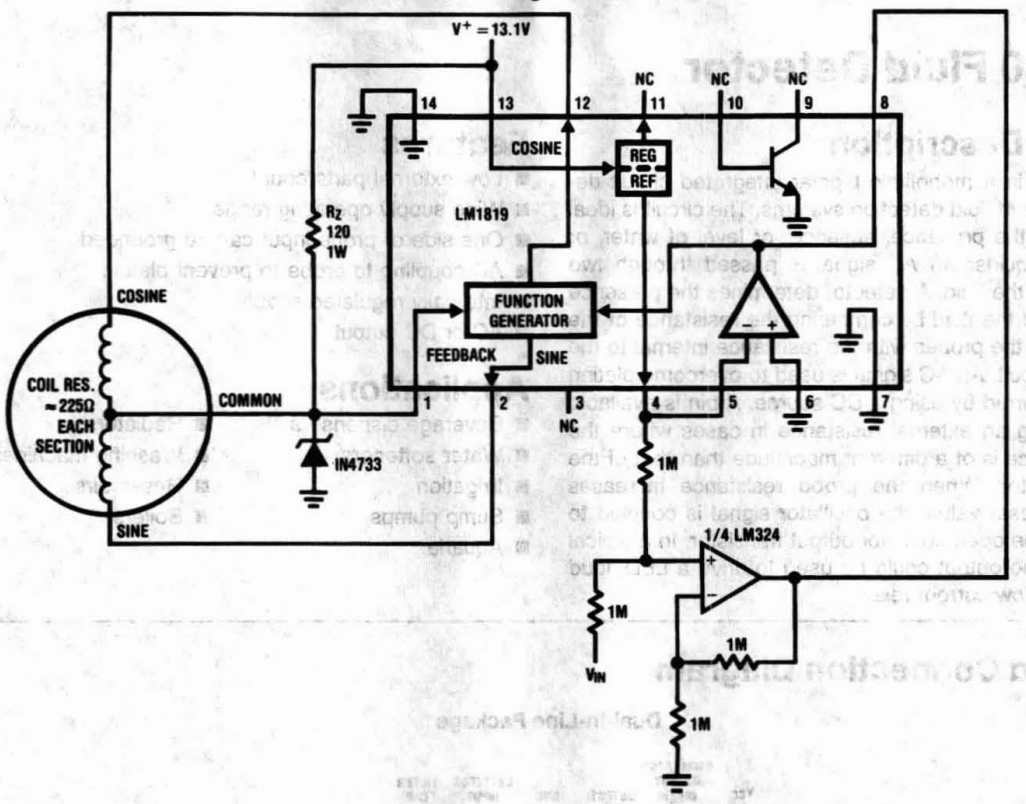
Deflection = $54R_2I_{IN}$ (degrees)

Inputs of 0 to 100 μA deflect the meter 0 to 270°.

*Full scale deflection is adjusted by trimming R_2.

Typical Applications (Continued)

Level Shifted Voltage Driven Meter



TL/H/5263–8

Deflection = $54V_{IN}$ (degrees)

Inputs of 0 to 5.65V deflect the meter through a range of 0 to 305°.

Full scale deflection is adjusted by trimming the input voltage.

National Semiconductor

LM1830 Fluid Detector

General Description

The LM1830 is a monolithic bipolar integrated circuit designed for use in fluid detection systems. The circuit is ideal for detecting the presence, absence, or level of water, or other polar liquids. An AC signal is passed through two probes within the fluid. A detector determines the presence or absence of the fluid by comparing the resistance of the fluid between the probes with the resistance internal to the integrated circuit. An AC signal is used to overcome plating problems incurred by using a DC source. A pin is available for connecting an external resistance in cases where the fluid impedance is of a different magnitude than that of the internal resistor. When the probe resistance increases above the preset value, the oscillator signal is coupled to the base of the open-collector output transistor. In a typical application, the output could be used to drive a LED, loud speaker or a low current relay.

Features

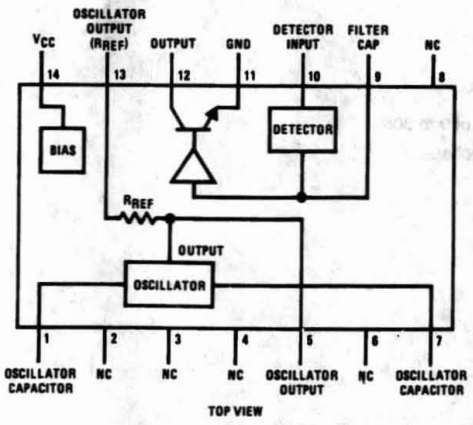
- Low external parts count
- Wide supply operating range
- One side of probe input can be grounded
- AC coupling to probe to prevent plating
- Internally regulated supply
- AC or DC output

Applications

- Beverage dispensers
- Water softeners
- Irrigation
- Sump pumps
- Aquaria
- Radiators
- Washing machines
- Reservoirs
- Boilers

Logic and Connection Diagram

Dual-In-Line Package



TL/H/5700–1

Order Number LM1830N
See NS Package Number N14A

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

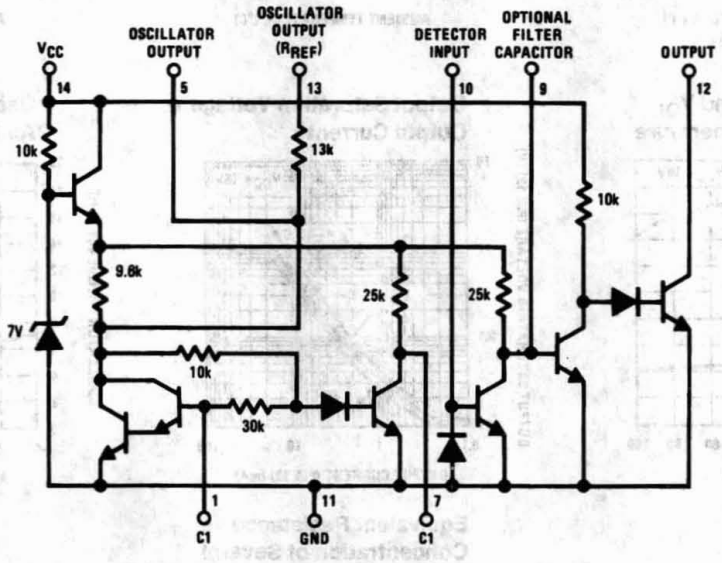
Supply Voltage	28V
Power Dissipation (Note 1)	1400 mW
Output Sink Current	20 mA
Operating Temperature Range	−40°C to +85°C
Storage Temperature Range	−40°C to +150°C
Lead Temp. (Soldering, 10 seconds)	260°C

Electrical Characteristics ($V^+ = 16V$, $T_A = 25°C$ unless otherwise specified)

Parameter	Conditions	Min	Typ	Max	Units
Supply Current			5.5	10	mA
Oscillator Output Voltage					
Low			1.1		V
High			4.2		V
Internal Reference Resistor		8	13	25	kΩ
Detector Threshold Voltage			680		mV
Detector Threshold Resistance		5	10	15	kΩ
Output Saturation Voltage	$I_O = 10$ mA		0.5	2.0	V
Output Leakage	$V_{PIN\ 12} = 16V$			10	μA
Oscillator Frequency	C1 = 0.00 1μF	4	7	12	kHz

Note 1: The maximum junction temperature rating of the LM1830N is 150°C. For operation at elevated temperatures, devices in the dual-in-line plastic package must be derated based on a thermal resistance of 89°C/W.

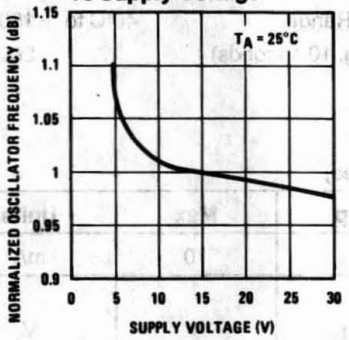
Schematic Diagram



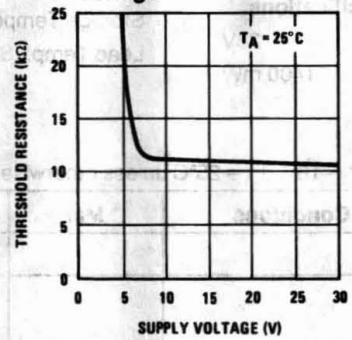
TL/H/5700–2

Typical Performance Characteristics

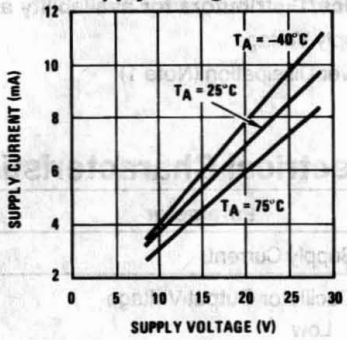
Normalized Oscillator Frequency vs Supply Voltage



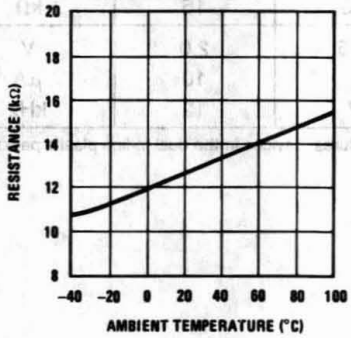
Threshold Resistance vs Supply Voltage



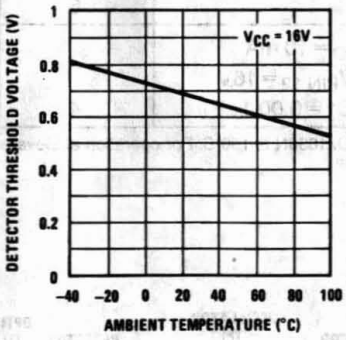
Power Supply Current vs Supply Voltage



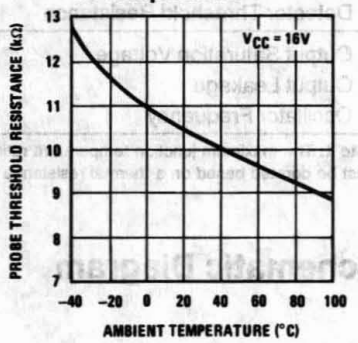
Reference Resistor vs Ambient Temperature



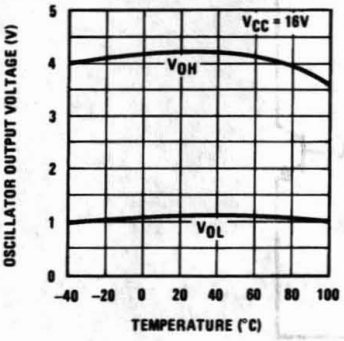
Detector Threshold Voltage vs Temperature



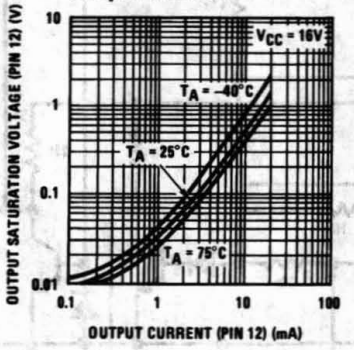
Probe Threshold Resistance vs Temperature



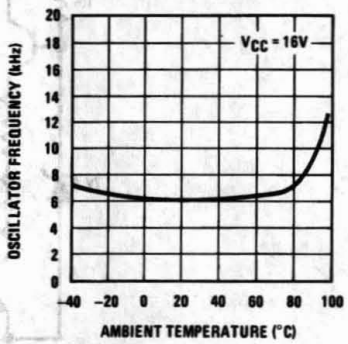
Oscillator V_{OH} and V_{OL} vs Ambient Temperature



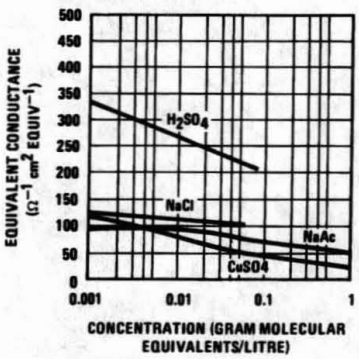
Output Saturation Voltage vs Output Current



Oscillator Frequency vs Ambient Temperature



Equivalent Resistance vs Concentration of Several Solutions



TL/H/5700–3

Application Hints

The LM1830 requires only an external capacitor to complete the oscillator circuit. The frequency of oscillation is inversely proportional to the external capacitor value. Using 0.001μF capacitor, the output frequency is approximately 6 kHz. The output from the oscillator is available at pin 5. In normal applications, the output is taken from pin 13 so that the internal 13k resistor can be used to compare with the probe resistance. Pin 13 is coupled to the probe by a blocking capacitor so that there is no net dc on the probe.

Since the output amplitude from the oscillator is approximately 4 V_{BE}, the detector (which is an emitter base junction) will be turned "ON" when the probe resistance to ground is equal to the internal 13 kΩ resistor. An internal diode across the detector emitter base junction provides symmetrical limiting of the detector input signal so that the probe is excited with ±2 V_{BE} from a 13 kΩ source. In cases where the 13 kΩ resistor is not compatible with the probe resistance range, an external resistor may be added by coupling the probe to pin 5 through the external resistor as shown in *Figure 2*. The collector of the detecting transistor is brought out to pin 9 enabling a filter capacitor to be connected so that the output will switch "ON" or "OFF" depending on the probe resistance. If this capacitor is omitted, the output will be switched at approximately 50% duty cycle when the probe resistance exceeds the reference resistance. This can be useful when an audio output is required and the output transistor can be used to directly drive a loud speaker. In addition, LED indicators do not require dc excitation. Therefore, the cost of a capacitor for filtering can be saved.

In the case of inductive loads or incandescent lamp loads, it is recommended that a filter capacitor be employed.

In a typical application where the device is employed for sensing low water level in a tank, a simple steel probe may be inserted in the top of the tank with the tank grounded. Then when the water level drops below the tip of the probe, the resistance will rise between the probe and the tank and the alarm will be operated. This is illustrated in *Figure 3*. In situations where a non-conductive container is used, the probe may be designed in a number of ways. In some cases a simple phono plug can be employed. Other probe designs include conductive parallel strips on printed circuit boards.

It is possible to calculate the resistance of any aqueous solution of an electrolyte for different concentrations, provided the dimensions of the electrodes and their spacing is known.

The resistance of a simple parallel plate probe is given by:

$$R = \frac{1000}{c.p} \bullet \frac{d}{A}\ \Omega$$

where A = area of plates (cm^2)
d = separation of plates (cm)
c = concentration (gm. mol. equivalent/litre)
p = equivalent conductance
(Ω^{-1} cm^2 equiv. $^{-1}$)

(An equivalent is the number of moles of a substance that gives one mole of positive charge and one mole of negative charge. For example, one mole of NaCl gives $Na^+ + Cl^-$ so the equivalent is 1. One mole of $CaCl_2$ gives $Ca^{++} + 2Cl^-$ so the equivalent is 1/2.)

Usually the probe dimensions are not measured physically, but the ratio d/A is determined by measuring the resistance of a cell of known concentration c and equivalent conductance of 1. A graph of common solutions and their equivalent conductances is shown for reference. The data was derived from D.A. MacInnes, "The Principles of Electrochemistry," Reinhold Publishing Corp., New York., 1939.

In automotive and other applications where the power source is known to contain significant transient voltages, the internal regulator on the LM1830 allows protection to be provided by the simple means of using a series resistor in the power supply line as illustrated in *Figure 4*. If the output load is required to be returned directly to the power supply because of the high current required, it will be necessary to provide protection for the output transistor if the voltages are expected to exceed the data sheet limits.

Although the LM1830 is designed primarily for use in sensing conductive fluids, it can be used with any variable resistance device, such as light dependent resistor or thermistor or resistive position transducer.

The following table lists some common fluids which may and may not be detected by resistive probe techniques.

Conductive Fluids	Non-Conductive Fluids
City water	Pure water
Sea water	Gasoline
Copper sulphate solution	Oil
Weak acid	Brake fluid
Weak base	Alcohol
Household ammonia	Ethylene glycol
Water and glycol mixture	Paraffin
Wet soil	Dry soil
Coffee	Whiskey

Typical Applications V_{CC} = 16V

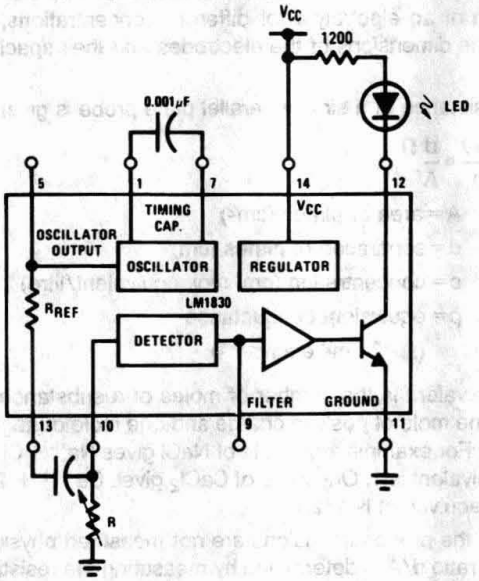


FIGURE 1. Test Circuit

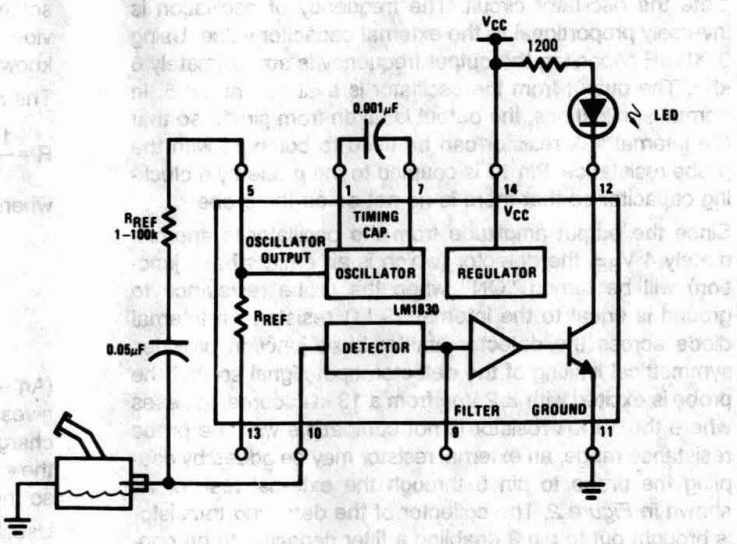


FIGURE 2. Application Using External Reference Resistor

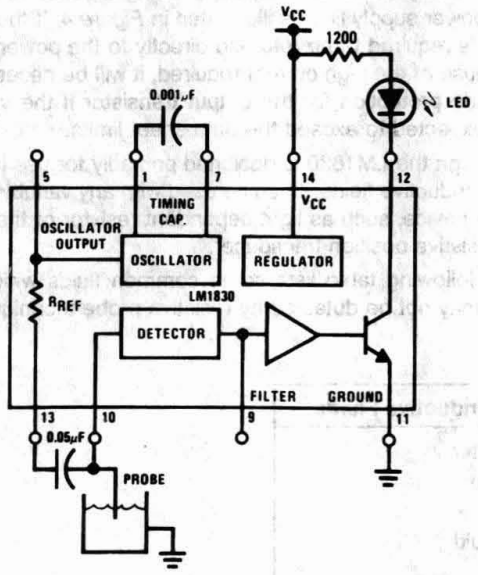
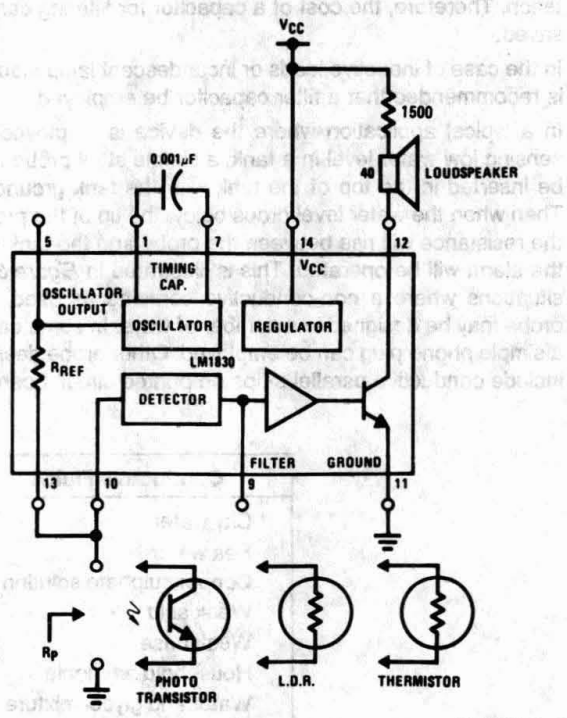


FIGURE 3. Basic Low Level Warning Device with LED Indication



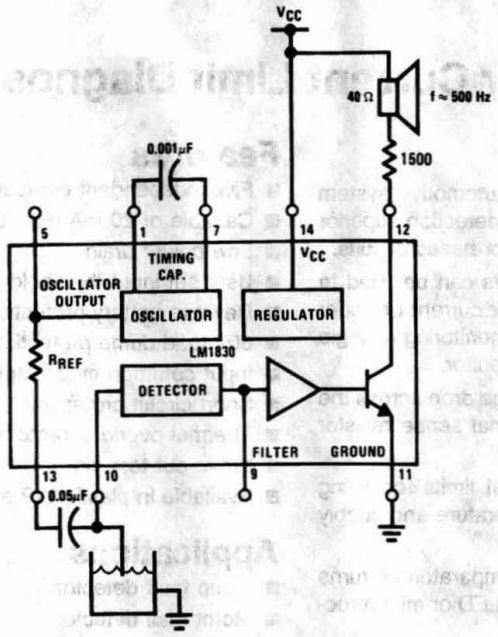
TL/H/5700–4

Output is activated when R_P is approximately greater than ⅓ R_{REF}

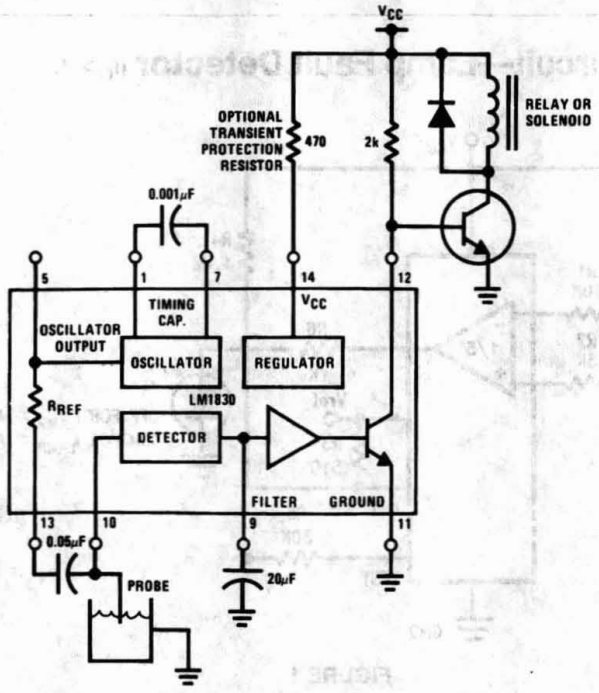
FIGURE 4. Direct Coupled Applications

Typical Applications V_{CC} = 16V (Continued)

Low Level Warning with Audio Output



High Level Warning Device



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The Output is suitable for driving a sump pump or opening a drain valve, etc.

National Semiconductor

LM1946 Over/Under Current Limit Diagnostic Circuit

General Description

The LM1946 provides the industrial or automotive system designer with over or under current limit detection superior to that of ordinary transistor or comparator-based circuits.

Each of the five independent comparators can be used to monitor a separate load as either an over current or under current limit detector. Two comparators monitoring a single load can function as a current window monitor.

Current is sensed by monitoring the voltage drop across the wiring harness, pc board trace, or external sense resistor that feeds the load.

Provisions for compensating the user set limits for wiring harness resistance variations over temperature and supply voltage variations are also available.

When a limit is reached in one of the comparators, it turns on its output which can drive an external LED or microprocessor.

One side of the load can be grounded (not possible with ordinary comparator designs), which is important for automotive systems.

Features

- Five independent comparators
- Capable of 20 mA per output
- Low power drain
- User set input threshold voltages
- Reverse battery protection
- 60V load dump protection on supply and all inputs
- Input common mode range exceeds V_{CC}
- Short circuit protection
- Thermal overload protection
- Prove-out test pin
- Available in plastic DIP and SO packages

Applications

- Lamp fault detector
- Motor stall detector
- Power supply bus monitoring

Typical Application Circuit—Lamp Fault Detector (I_L > 1A)

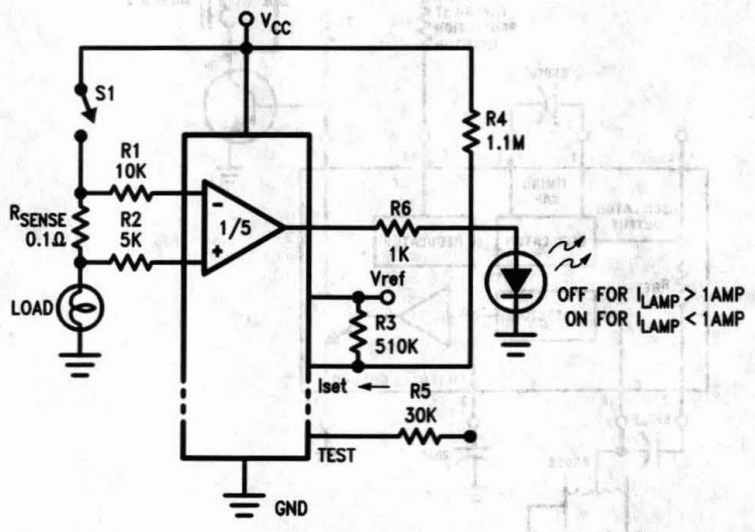

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FIGURE 1

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC} and Input Pins)	
Survival Voltage ($T \leq 100$ ms)	−50V to +60V
Operational Voltage	9V to 26V
Internal Power Dissipation (Note 1)	Internally Limited
Output Short Circuit to Ground or V_{CC}	Continuous
Operating Temperature Range (T_A)	−40°C to +85°C
Maximum Junction Temperature	+150°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec.)	+260°C
ESD Susceptibility (Note 3)	600V

Electrical Characteristics

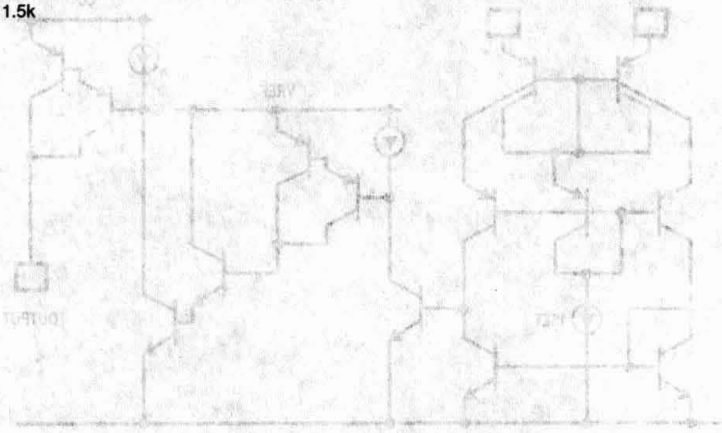
$9V \leq V_{CC} \leq 16V$, Iset = 20 μA, $T_j = 25°C$ (unless otherwise specified)

Parameter	Conditions	Min	Typ	Max	Units
Quiescent Current	All Outputs "Off"		1.40	3.00	mA_{dc}
Reference Voltage	I_{ref} = 10 μA	5.8	6.4	7.0	V_{dc}
Reference Voltage Line Regulation	$9V \leq V_{CC} \leq 16V$, I_{ref} = 10 μA		±5	±50	mV_{dc}
Iset Voltage	Iset = 20 μA	1.20	1.40	1.60	V_{dc}
Input Offset Voltage	At Output Switch Point. V_O = 2V $9V \leq V_{CM} \leq 16V$		±1.0	±5.0	mV_{dc}
Input Offset Current	$I_{IN(+)} - I_{IN(-)}$, $9V \leq V_{CM} \leq 16V$		±0.10	±1.00	μA_{dc}
Input Bias Current	$I_{IN(+)}$ or $I_{IN(-)}$, $9V \leq V_{CM} \leq 16V$	18.00	20.00	22.00	μA_{dc}
Input Common Mode Voltage Range		4.00		26.0	V_{dc}
Maximum Positive Input Transient	Either Input. T ≤ 100 ms	60	70		V
Maximum Negative Input Transient	Either Input. T ≤ 100 ms	−50	−60		V
Output Saturation Voltage	I_O = 2 mA, $9V \leq V_{CC} \leq 16V$		0.80	1.00	V_{dc}
	I_O = 10 mA, $9V \leq V_{CC} \leq 16V$		1.00	1.20	V_{dc}
Output Short Circuit Current	$V_O = 0V_{dc}$, Comparator "ON"	20	45	120.0	mA_{dc}
Output Leakage Current	$V_O = 0V_{dc}$. Comparator "Off"		0.01	1.00	μA_{dc}
Test Threshold Voltage	At Switch Point on Any Output V_O = 2V (Note 2)	0.80	1.25	2.00	V_{dc}
Test Threshold Current			0.2		μA_{dc}

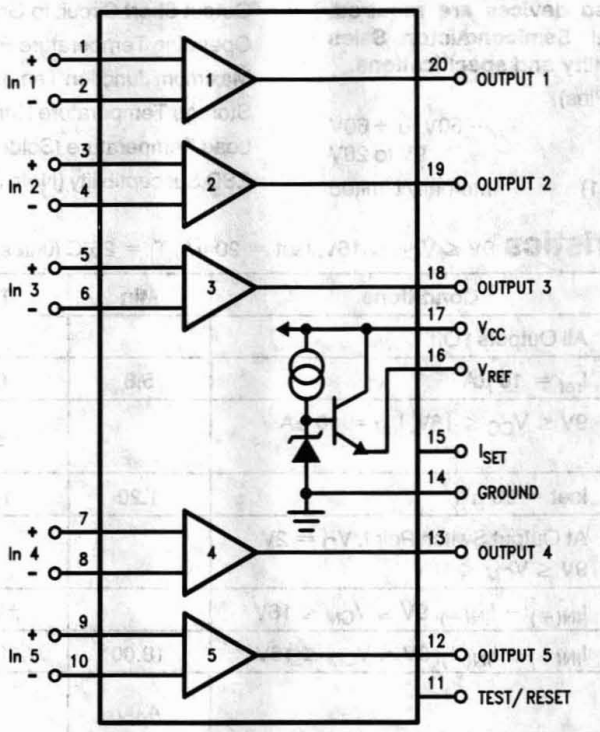
Note 1: Thermal resistance from junction to ambient is typically 53°C/W (board mounted).

Note 2: The test pin is an active high input, i.e. all five will be forced high when this pin is driven high.

Note 3: C_{ESD} = 100 pF, R_{ESD} = 1.5k



Connection Diagram



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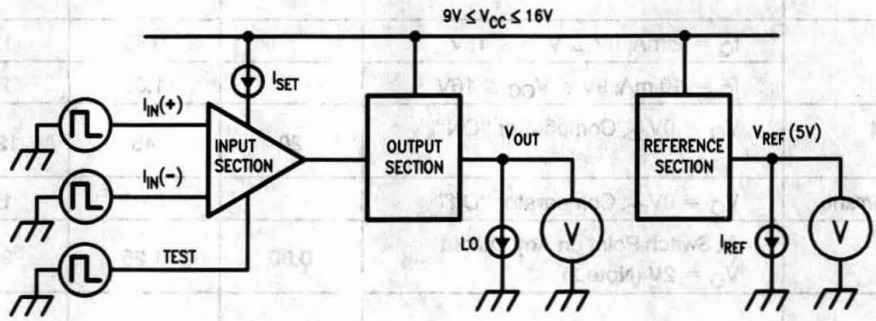
Order Number LM1946N or LM1946M
See NS Package Number M20B or N20A

Typical Test Circuit



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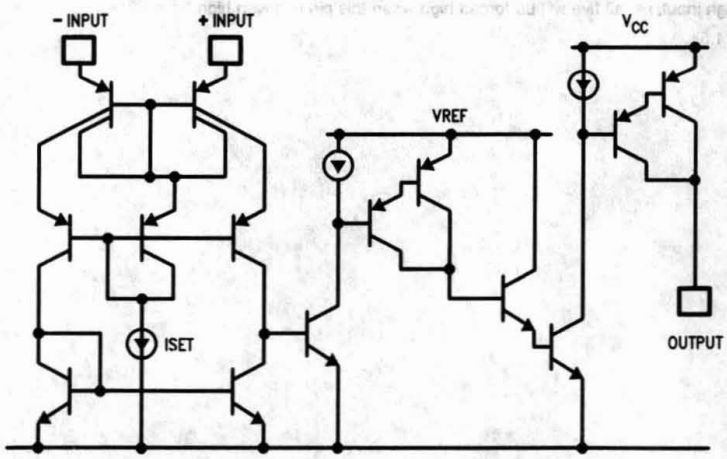
Simplified Comparator Schematic



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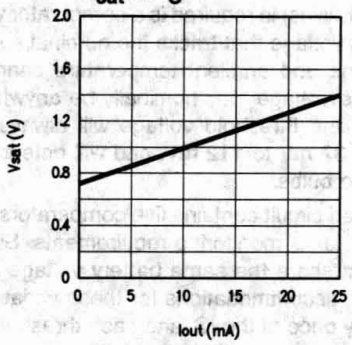
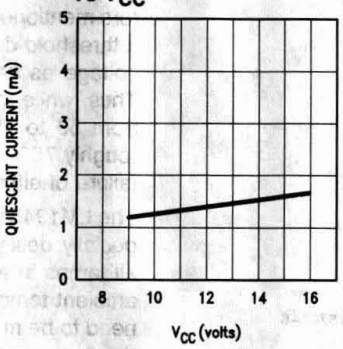
Typical Performance Characteristics

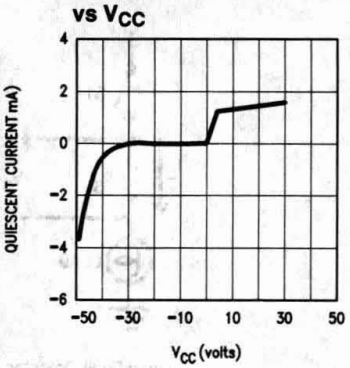
V_{sat} vs I_O



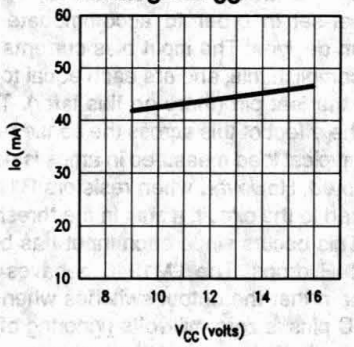
Quiescent Current vs V_{CC}



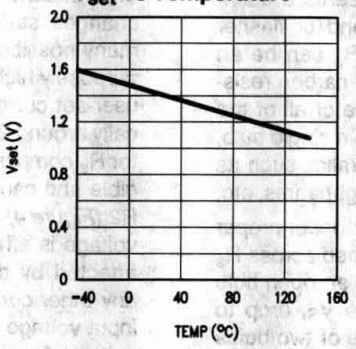
Quiescent Current vs V_{CC}



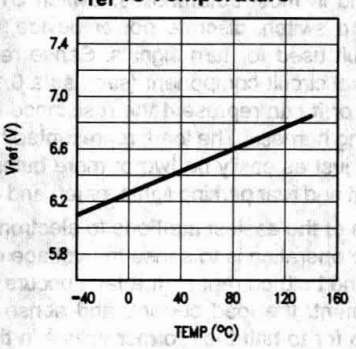
Peak I_O vs V_{CC}



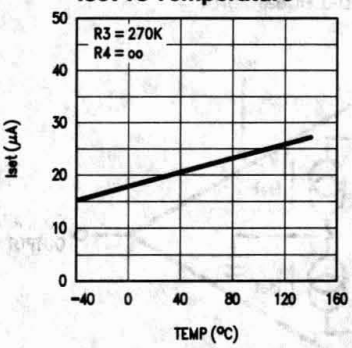
V_{set} vs Temperature



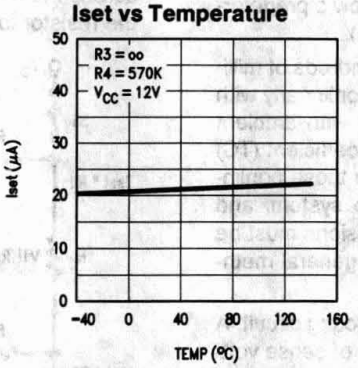
V_{ref} vs Temperature



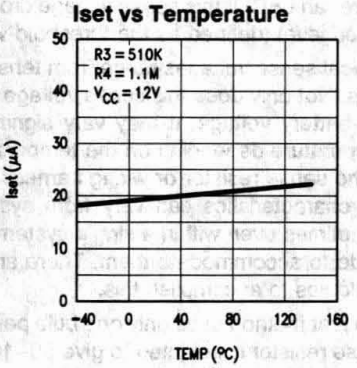
Iset vs Temperature



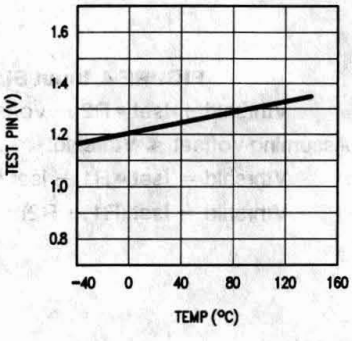
Iset vs Temperature



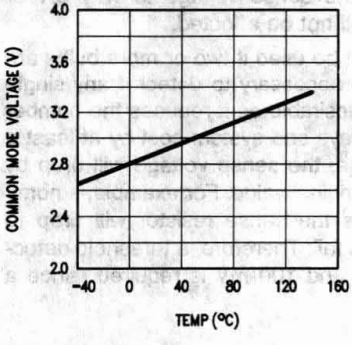
Iset vs Temperature



Test Threshold



Common Mode Lower Limit



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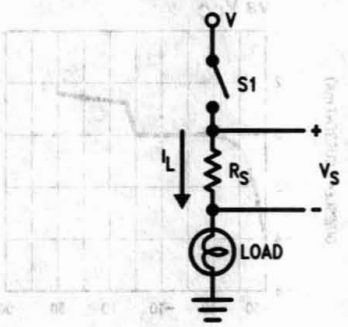
Application Hints

THEORY OF OPERATION: UNDER-CURRENT LIMIT DETECTOR



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Lamp Fault Detector

FIGURE 3. Equivalent Automotive Lamp Circuit

The diagram of *Figure 3* represents the typical lamp circuit found in most automobiles. Switch S1 represents a dashboard switch, discrete power device, relay and/or flasher circuit used for turn signals. Sense resistor R_S can be an actual circuit component (such as a 0.1Ω 1W carbon resistor) or it can represent the resistance of some or all of the wiring harness. The load, represented here as a single bulb, can just as easily be two or more bulbs in parallel, such as front and rear parking lights, or left and right highbeams, etc.

One of the easiest methods to electronically monitor proper bulb operation is to sense the voltage developed across R_S by the bulb current I_L. If a fault occurs due to an open bulb filament, the load current, and sense voltage V_S, drop to zero (or to half their former values in the case of two bulbs wired in parallel). A comparator circuit can then monitor this sense voltage, and alert the system or system user (e.g. power an LED) if this sense voltage drops below a predetermined level (defined as the threshold voltage).

Typical sense voltages range from tens to hundreds of millivolts. Not only does this sense voltage vary nonlinearly with the battery voltage, it may vary significantly with ambient temperature depending on the temperature coefficient (TC) of the sense resistor or wiring harness. Since these nonlinear characteristics can vary from system to system, and sometimes even within a single system, provisions must be made to accommodate them. There are two general methodologies to accomplish this.

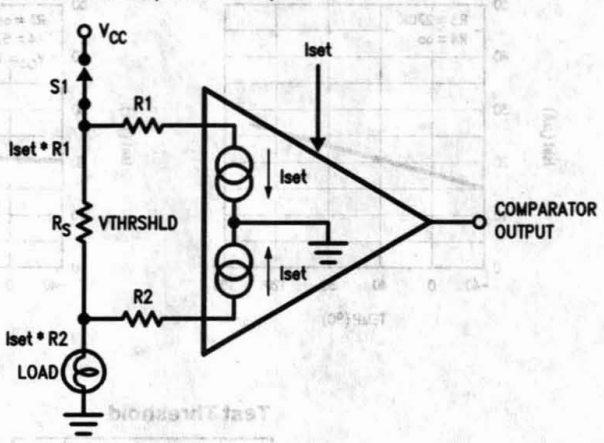
The first method uses only one bulb per monitoring circuit. A sense resistor is selected to give 50–100 mV of sense voltage in an operational circuit, and a comparator threshold detecting voltage of approximately 10 mV is set. Even if component tolerances, battery line variations, and temperature coefficients cause the sense voltage to vary 3:1 or more, circuit operation will not be affected.

The second method must be used if two or more bulbs are wired in parallel and it is necessary to detect if any single lamp fails. This is often desirable as it reduces the number of comparators and displays and system cost by at least a factor of two. In this case, the sense voltage will drop by only half (or less) of it's original value. For example, a nominal 100 mV drop across the sense resistor will drop to 50 mV if one of two bulbs fail. Therefore, a threshold detection voltage between 50 and 100 mV is required (since a 10 mV threshold would alert the system only if **both** bulbs failed). Yet a fixed threshold of 75 mV may not work if the nominal 100 mV sense voltage can vary 3:1 due to the factors mentioned earlier. What is required is a comparator with a threshold-detecting voltage that tracks the nominal sense voltage as battery line and ambient temperature change. Thus, while the sense voltage may nominally be anywhere from 50 to 150 mV, the threshold voltage will always be roughly 75% of it, or 37 mV to 112 mV, and will detect the failure of either of two bulbs.

The LM1946 integrated circuit contains five comparators especially designed for lamp monitoring requirements. Since all lamps in a system share the same battery voltage and ambient temperature, accommodations for these variations need to be made only once at the IC, and each threshold of the five comparators then tracks these variations.

SETTING THE COMPARATOR THRESHOLD VOLTAGE

The threshold voltage at which the comparator output changes state is user-set in order to accommodate the many possible system designs. The input bias currents are purposely high to accomplish this, and are each equal to the user-set current into the Iset pin (more on this later). Typically around 20 μA, the effect of this across the sense resistor R_S compared to a typical load measured in amps is negligible and can be ignored. However, when resistors R1 and R2 *(Figure 4)* are added to the circuit, a shift in the threshold voltage is effected. This occurs since each input has been affected by different IR drops. The LM1946 behaves like any other comparator in that the output switches when the input voltage at the IC pins is zero millivolts (ignoring offset voltage for the moment). If the output therefore has just switched states due to just the right threshold voltage across the sense resistor, then the sum of voltages around the resistor loop should equal zero:



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Vthrshld = Iset (R1 − R2)

FIGURE 4. Input Bias Current

$$V_{thrshld} + I_{set} \bullet R2 - V_{offset} - I_{set} \bullet R1 = 0$$

Assuming $V_{offset} \ll V_{thrshld}$:

$$V_{thrshld} = I_{set} \bullet R1 - I_{set} \bullet R2$$

$$V_{thrshld} = I_{set}(R1 - R2)$$

Application Hints (Continued)

Typical values are:

R1 = 6.2k ±5%

R2 = 1.2k ±5%

Iset = 20 μA @ 25°C

Vthrshld = 20 μA (6.2k − 1.2k) = 100 mV

For values of sense voltages greater than 100 mV, the comparator output is off (low). Sense voltages less than 100 mV turn the output on (high).

It's also important that the output of the comparator be in the "off" state when the inputs are taken to ground, i.e. S1 is opened and the lamp is turned "off". The input section of LM1946 has been designed to turn "off" when the inputs are grounded and therefore not deliver an erroneous bulb out indication. The comparator is only activated when the inputs are above ground by at least 3V.

R1 and R2 are necessary for another reason. These resistors protect the input terminals of the IC from the many transients in an automobile found on the battery line, some of which can exceed a thousand volts for a few microseconds. A minimum value of approximately 1 kΩ is therefore recommended.

COMPENSATING FOR BATTERY VOLTAGE

The current through a typical automotive lamp, whether a headlight or dashboard illumination lamp, will vary as battery voltage changes. The change, however, is nonlinear. Doubling the battery voltage does not double the lamp current.

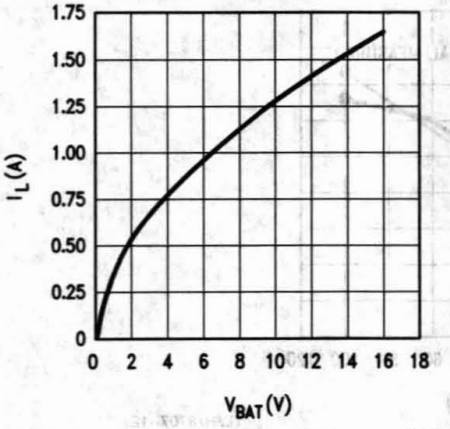

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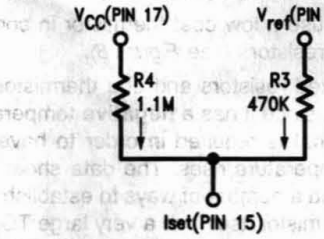
FIGURE 5

This occurs since a higher voltage will heat the filament more, increasing its resistance and allowing less current to flow than expected. *Figure 5* shows this effect. A best fit straight line over the normal battery range of 9V to 16V for this particular example can be given by:

$$I_L \text{ (Amps)} = 0.62 + 0.069 \bullet \text{Vbattery}$$



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$$\text{Iset} = \frac{V_{CC} - 1.4}{R4} + \frac{Vref - 1.4}{R3}$$

$$\text{Iset} = \frac{V_{CC}}{R4} + \frac{Vref}{R3} - 1.4\left(\frac{1}{R3} + \frac{1}{R4}\right)$$

FIGURE 6

Thus, in actual use, the LM1946 threshold voltage should track the variations in bulb current with respect to battery voltage. To accomplish this, Iset should have a component that varies with the battery. As shown in the LM1946 circuit schematic of *Figure 18*, the Iset pin is two diode drops above ground, or approximately 1.4V. A resistor from this pin to the 6.4V reference sets the fixed component of Iset; a resistor to the battery line sets the variable component. Thus, the best fit straight line in *Figure 5* can be realized exactly with only two resistors. The result is shown in *Figure 6*, giving a nominal Iset of 20 μA that tracks the bulb current as supply varies from 9V to 16V. The graph of *Figure 7* shows the final result comparing a typical sense voltage across Rs with the comparator threshold voltage as the supply varies.

COMPENSATING FOR AMBIENT TEMPERATURE VARIATION

If the sense resistors used in a system are perfect components with no temperature coefficient, then the compensation to be subsequently detailed here is unnecessary. However, resistors of the very small values usually required in a lamp monitoring system are sometimes difficult or expensive to acquire. A convenient alternative is the wiring harness, a length of wire, or even a trace on a printed circuit board. All of these are of copper material and therefore can vary by as much as 3900 ppm/°C. The LM1946 has been designed to accommodate a wide range of temperature compensation techniques. If the Iset current is designed to increase or decrease with temperature, nearly any temperature coefficient can be produced in the threshold voltage of the five input pairs.

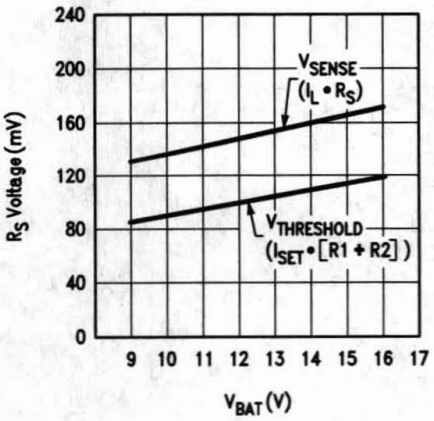

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FIGURE 7

3

Application Hints (Continued)

One solution is to use a low cost thermistor in conjunction with some low-TC resistors (see *Figure 8*).

There are three fixed resistors and one thermistor. This is an NTC thermistor, since it has a **negative** temperature coefficient. This is what is required in order to have Iset **increase** as the temperature rises. The data sheet with the thermistor described a number of ways to establish different final TC's. The thermistor itself has a very large TC which is somewhat difficult to describe mathematically. But, if it is used with some other fixed resistors, such as Rmin and Rmax, definite end point limits can be established and an approximate staight line TC generated. See *Figure 9* for a graphic representation of the ideal calculated values of Iset and the actual measured values generated. Notice that there is very close agreement between the two graphs. The circuit actually creates an S-shaped curve around the ideal.

The low-cost thermistor is available from Keystone and is listed as follows: RL2008-52.3K-155-D1.

OVER-CURRENT LIMIT DETECTOR

Other applications include an over-current detector, as shown in *Figure 10*. The load represented here can be either a single component or an entire system. Resistors R3

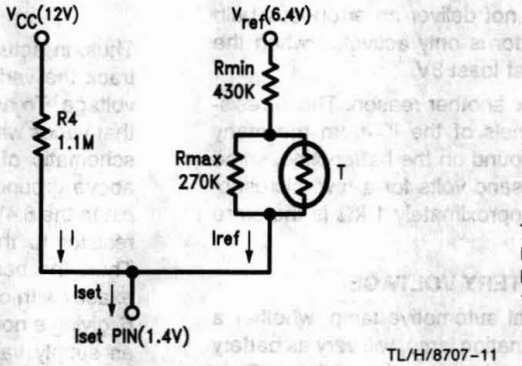

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FIGURE 8. Thermistor/Resistor Network

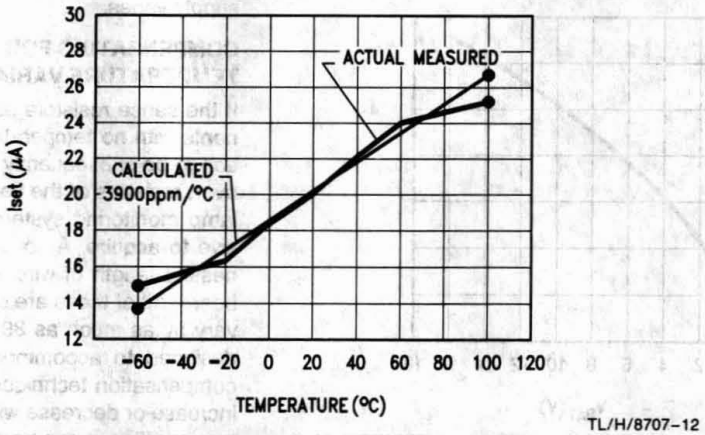

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FIGURE 9. Iset vs Temperature with *Figure 8* Circuit

Application Hints (Continued)

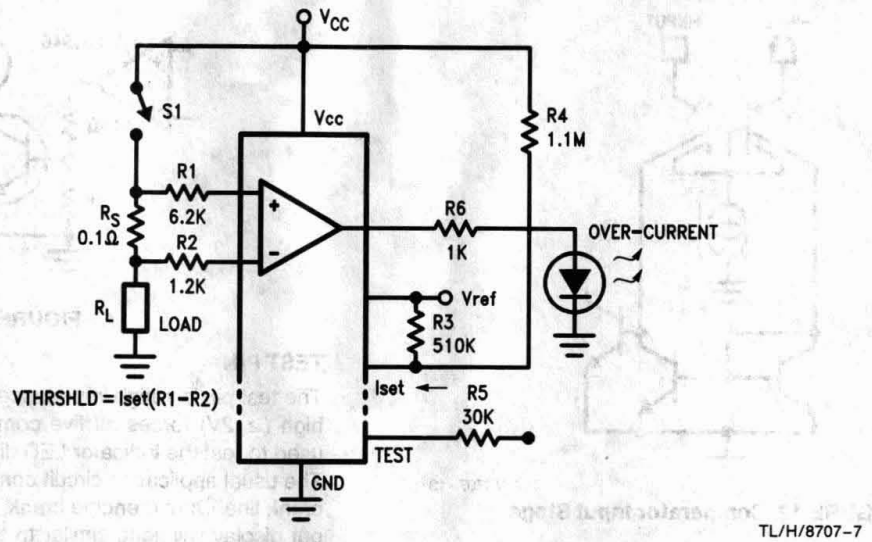

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FIGURE 10. Using the LM1946 as an Over-Current Limit Detector

and R4 again allow the system designer to tailor the threshold limit to the V/I characteristics of each particular system. The input threshold voltage is determined by, and directly proportional to, Iset into pin 20. R3, from the on-chip reference voltage, provides a current and threshold that is independent of the supply voltage, V_{CC}. R4 provides a current directly proportional to supply. These resistors allow thresholds to be either independent of, or directly proportional to supply voltage, or anything in between. For example, the values in *Figure 10* are tailored to match the V/I characteristics of the bulb filament used in earlier examples. However, if the load had purely resistive characteristics, Iset and the threshold would be set with R4 only, eliminating R3. Likewise, if the load current was independent of supply, such as in many systems powered by a voltage regulator, Iset would be better set by R3 only, eliminating R4. Further details on this and how to handle variations with ambient temperature with resistor and thermistor combinations are discussed in detail in previous sections. Compensation for temperature variations, however, is rarely necessary since short circuit or over-current values are usually much greater than the nominal value. For example, if the load in *Figure 10* represented a DC motor, the circuit could be used to detect the motor stall condition. Stall current through the sense resistor, Rs, would typically be five times the nominal running current. By setting the threshold at three times the nominal current value, enough margin exists that minor variations due to temperature can be ignored. The variation in stall current due to battery or supply voltage can be significant, however. Being approximately proportional, Iset would best be set in this case by R4 only.

WINDOW DETECTOR

The availability of more than one comparator per IC allows many other applications. One is the current sense window detector. Many times it is useful to know that a certain current is within both an upper and lower limit. Using two of the LM1946 comparators and the circuit of *Figure 11* will accomplish this. In this particular case, high and low limits are approximately 3A and 1A respectively. The outputs can be kept separate or wired-or, as shown, to a single output load as a simple out-of-bounds detector.

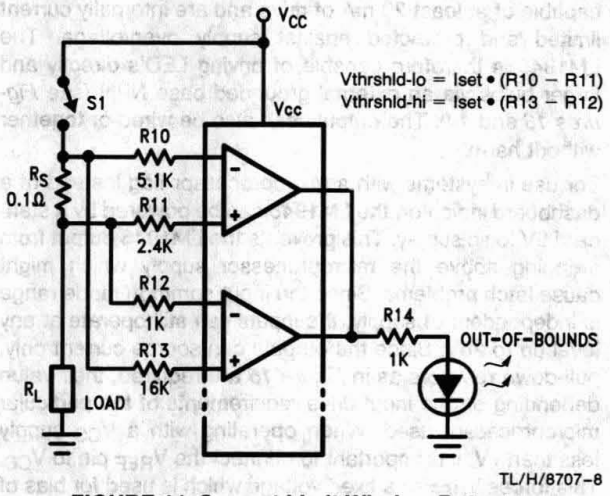

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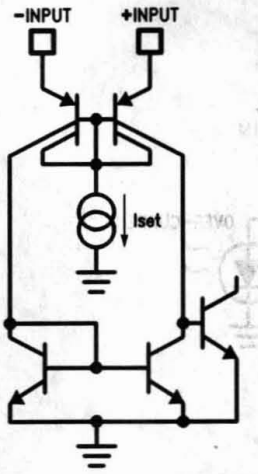
FIGURE 11. Current Limit Window Detector

COMPARATOR INPUT STAGE

The LM1946 IC consists of five specially designed comparator input circuits to monitor the IR drop across the wiring harness or the sense resistor between the battery and the light bulb. These comparators have been designed to accommodate a wide range of input signals without damage to the IC or the load circuitry. The inputs can easily withstand a common mode voltage above the positive supply since the inputs are the emitters of two matched PNP devices (see *Figure 12*). This is vital in a system which must operate in the conditions present under the hood of an automobile. The inputs can also survive when taken well below ground. If a negative voltage is present at the inputs of the comparator, the two emitter-base PNP junctions become reverse biased and block any current flow in or out of the device. To disable an unused comparator it is recommended that the inputs be connected to ground.

Application Hints (Continued)



TL/H/8707–13

FIGURE 12. Comparator Input Stage

THE OUTPUT SECTION

The output section of the LM1946 is different from most automotive comparators as it employs high beta proprietary PNP transistors which are very rugged and capable of higher output currents. Each of the five comparator outputs is capable of at least 20 mA of drive and are internally current limited and protected against supply overvoltage. The LM1946 is therefore capable of driving LED's directly and larger bulbs via an external grounded base NPN (see *Figures 13* and *14*). The outputs can also be wired-or together without harm.

For use in systems with a microprocessor flag instead of a dashboard indicator, the LM1946 can be powered by a standard 5V logic supply. This prevents the LM1946 output from swinging above the microprocessor supply which might cause latch problems. Since the input common mode range is independent of supply, the inputs can still operate at any level up to 26V. Since the outputs can source current only, pull-down resistors as in *Figure 15* are required, their value depending on the input drive requirements of the particular microprocessor used. When operating with a V_{CC} supply less than 7V, it is important to connect the V_{REF} pin to V_{CC}. This forces V_{REF} to a fixed voltage which is used for bias of internal circuitry.

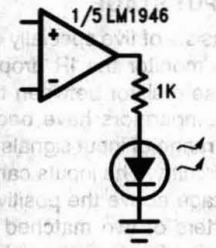


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FIGURE 13

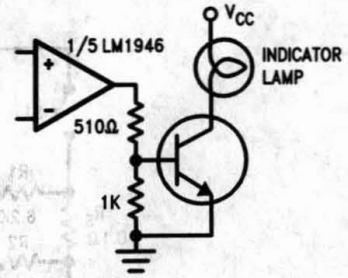

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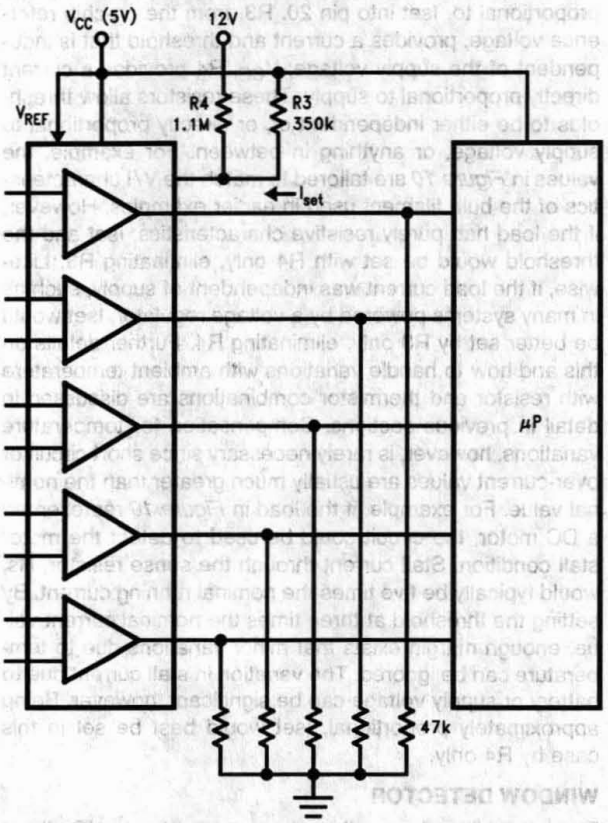
FIGURE 14

TEST PIN

The test pin is a high impedance logic input. Forcing this pin high (≥ 2V) forces all five comparator outputs on. This is used to test the indicator LED display (or other output load). The usual application circuit connects this pin to the ignition crank line. During engine crank, therefore, the LM1946 output display will light, similar to the usual dashboard indicators. The test pin was designed to operate with the usual transient voltages found on the crank line as long as a limiting resistor (e.g. 30k) separates them *(Figure 1)*.

Minimum pulse width (ms) ≈ 0.01 + 1.5 • C1 (μF)



TL/H/8707–15

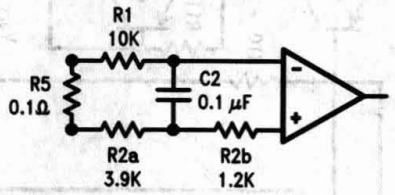
FIGURE 15

Application Hints (Continued)

MORE NOISE FILTERING

The current flowing through the sense resistor and certain loads can sometimes be very noisy, particularly when the load is a DC motor, or switching supply. Large amounts of noise on the supply line can also cause problems when threshold voltages are set to very small values. In these cases, while the average current level may remain well below the threshold trip point, noise peaks may exceed it. A LED display could then flicker or appear dimly lit, or excessive software routines and processor time may be required for a μP to disregard such noise. Often such noise must be filtered directly at the inputs, using the input resistors R1 and R2 and a capacitor. Care must be taken, however, that such a filter will not cause an erroneous output state upon power-up or whenever switch S1 is closed. The most effective general methodology to achieve this is to split the resistor in the positive input lead into two resistor values and connect a capacitor from here to the negative input. For example, the 1.2k resistor R2 of *Figure 10* could be replaced with 3.9k and 1.2k resistors as shown in *Figure 16a* (R1 increasing from 6.2k to 10k to compensate). The value of capacitor C2 depends upon the degree of filtering required, the amount of noise present, and the response times desired. The choice of values for the new resistors is almost arbitrary. Generally the larger value is attached to the sense resistor for better decoupling. The smaller value must be large enough so that the DC voltage across it upon power-up exceeds the maximum offset voltage expected of the comparator (i.e. Iset*R2b > 5.0mV). It is this requirement that guarantees that the output will not be in an erroneous high state upon power-up or whenever S1 is closed. (Should this feature be unnecessary to a particular application circuit, the methodology described can be replaced with a simple capacitor across the comparator input pins).

For extremely severe cases, additional filter stages can be cascaded at the inputs (see *Figure 17*). Since the input bias currents of the comparator are equal at the input threshold level, the voltage drops across the 1k resistors cancel and do not affect the DC operation of the circuit (ignoring resistor match tolerance and Ios). If an application circuit is noisy enough to require such an elaborate filter, then ferrite beads, shown here as L1 and L2, will also probably help.



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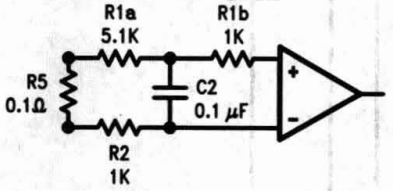
a. Open-Circuit Detector



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b. Over-Current Limit Detector

FIGURE 16. Input Noise Filters for Various Application Circuits

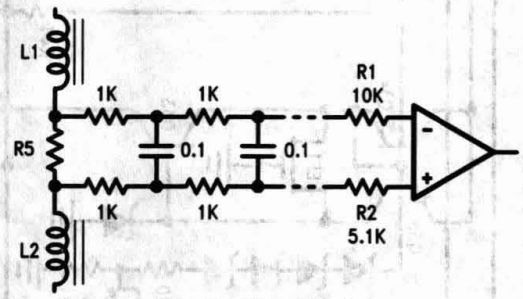

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FIGURE 17. Additional Noise Filters

Circuit Schematic

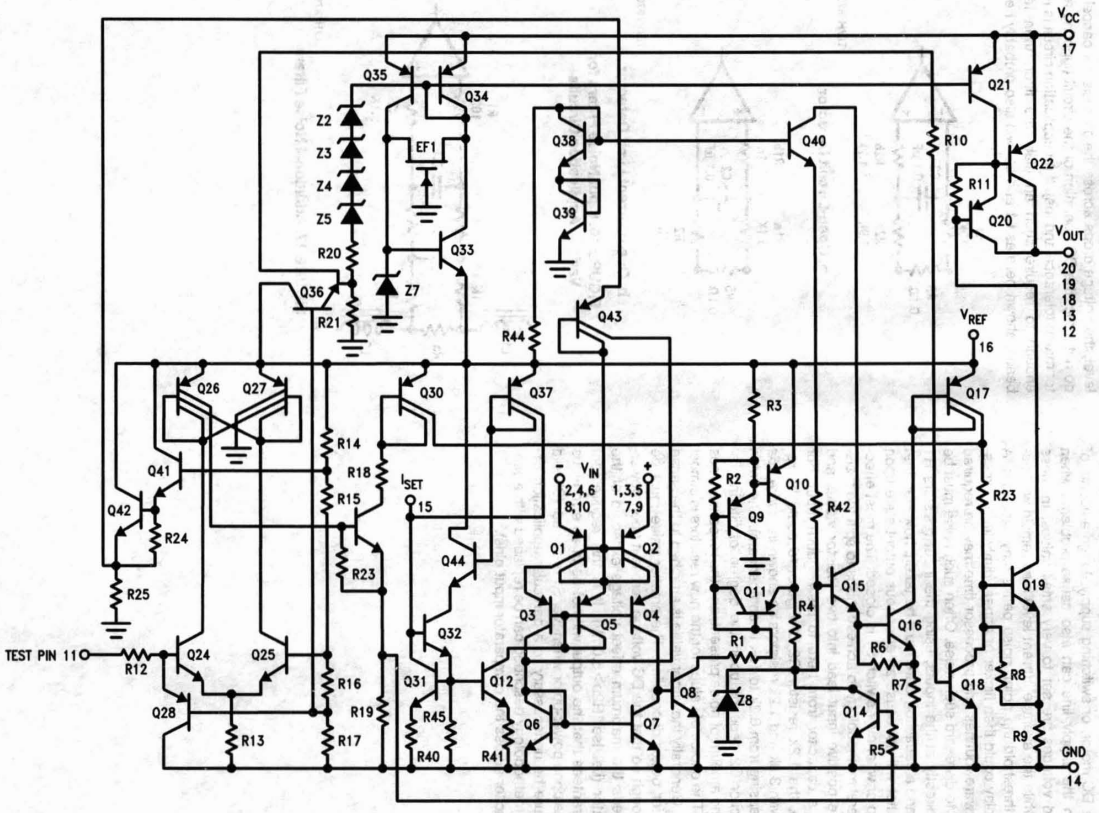

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FIGURE 18

National Semiconductor

LM1949 Injector Drive Controller

General Description

The LM1949 linear integrated circuit serves as an excellent control of fuel injector drive circuitry in modern automotive systems. The IC is designed to control an external power NPN Darlington transistor that drives the high current injector solenoid. The current required to open a solenoid is several times greater than the current necessary to merely hold it open; therefore, the LM1949, by directly sensing the actual solenoid current, initially saturates the driver until the "peak" injector current is four times that of the idle or "holding" current *(Figure 3–Figure 7).* This guarantees opening of the injector. The current is then automatically reduced to the sufficient holding level for the duration of the input pulse. In this way, the total power consumed by the system is dramatically reduced. Also, a higher degree of correlation of fuel to the input voltage pulse (or duty cycle) is achieved, since opening and closing delays of the solenoid will be reduced.

Normally powered from a 5V ±10% supply, the IC is typically operable over the entire temperature range (−55°C to +125°C ambient) with supplies as low as 3 volts. This is particularly useful under "cold crank" conditions when the battery voltage may drop low enough to deregulate the 5-volt power supply.

The LM1949 is available in the plastic miniDIP, (contact factory for other package options).

Features

- Low voltage supply (3V–5.5V)
- 22 mA output drive current
- No RFI radiation
- Adaptable to all injector current levels
- Highly accurate operation
- TTL/CMOS compatible input logic levels
- Short circuit protection
- High impedance input
- Externally set holding current, I_H
- Internally set peak current ($4 \times I_H$)
- Externally set time-out
- Can be modified for full switching operation
- Available in plastic 8-pin miniDIP

Applications

- Fuel injection
- Throttle body injection
- Solenoid controls
- Air and fluid valves
- DC motor drives

Typical Application Circuit

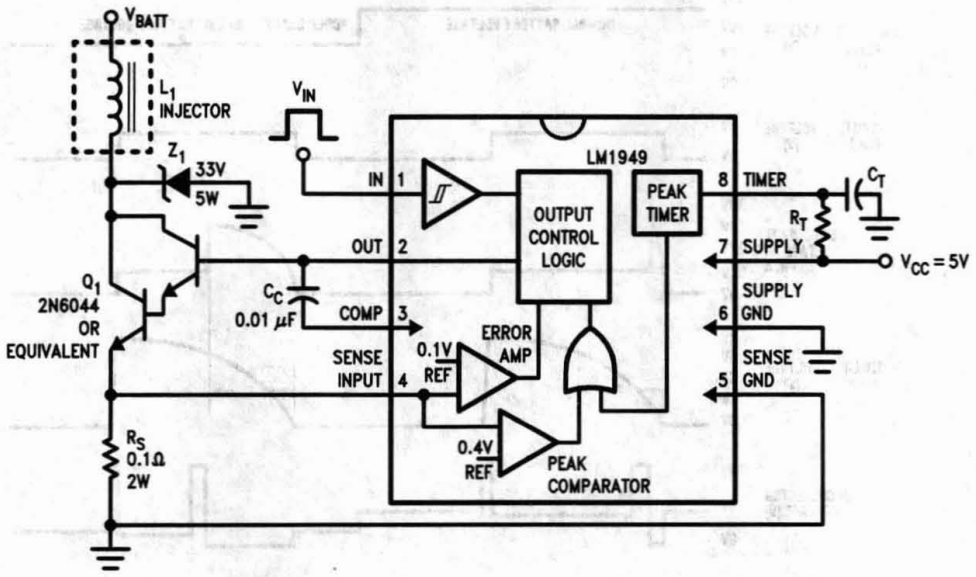

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FIGURE 1. Typical Application and Test Circuit

Order Number LM1949M or LM1949N
See NS Package Number M08A or N08E

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

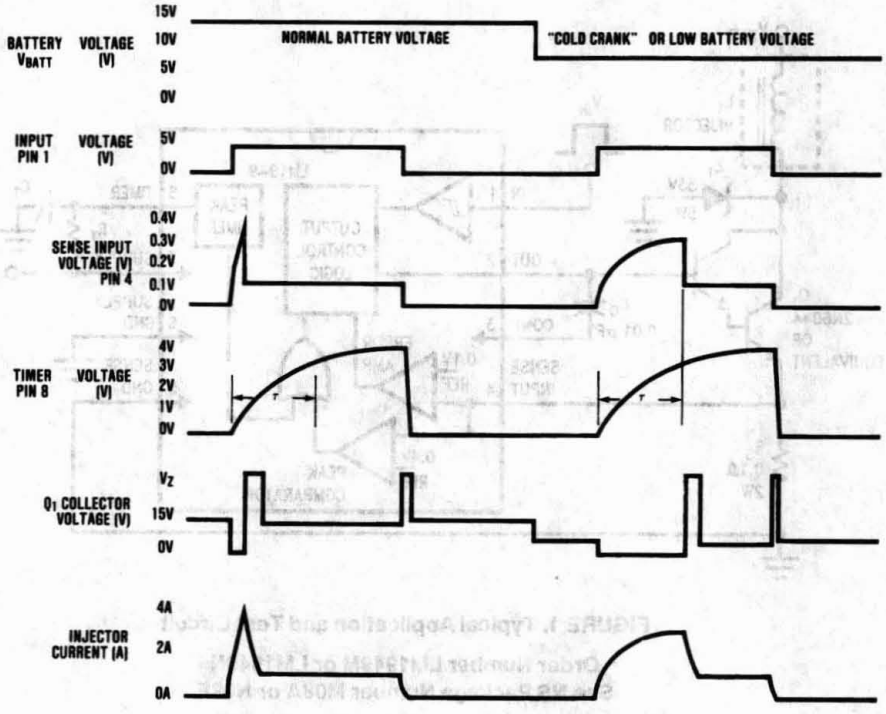
Supply Voltage	8V
Power Dissipation (Note 1)	1235 mW
Input Voltage Range	−0.3V to V_{CC}
Operating Temperature Range	−40°C to +125°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature	150°C
Lead Temp. (Soldering 10 sec.)	260°C

Electrical Characteristics (V_{CC} = 5.5V, V_{IN} = 2.4V, T_j = 25°C, *Figure 1*, unless otherwise specified.)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
I_{CC}	Supply Current					
	Off	V_{IN} = 0V		11	23	mA
	Peak	Pin 8 = 0V		28	54	mA
	Hold	Pin 8 Open		16	26	mA
V_{OH}	Input On Level	V_{CC} = 5.5V		1.4	2.4	V
		V_{CC} = 3.0V		1.2	1.6	V
V_{OL}	Input Off Level	V_{CC} = 5.5V	1.0	1.35		V
		V_{CC} = 3.0V	0.7	1.15		V
I_B	Input Current		−25	3	+25	μA
I_{OP}	Output Current					
	Peak	Pin 8 = 0V	−10	−22		mA
	Hold	Pin 8 Open	−1.5	−5		mA
V_S	Output Saturation Voltage	10 mA, V_{IN} = 0V		0.2	0.4	V
	Sense Input					
V_p	Peak Threshold	V_{CC} = 4.75V	350	386	415	mV
V_H	Hold Reference		88	94	102	mV
t	Time-out, t	$t \div R_T C_T$	90	100	110	%

NOTE 1: For operation in ambient temperatures above 25°C, the device must be derated based on a 150°C maximum junction temperature and a thermal resistance of 100°C/W junction to ambient.

Typical Circuit Waveforms



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Schematic Diagram

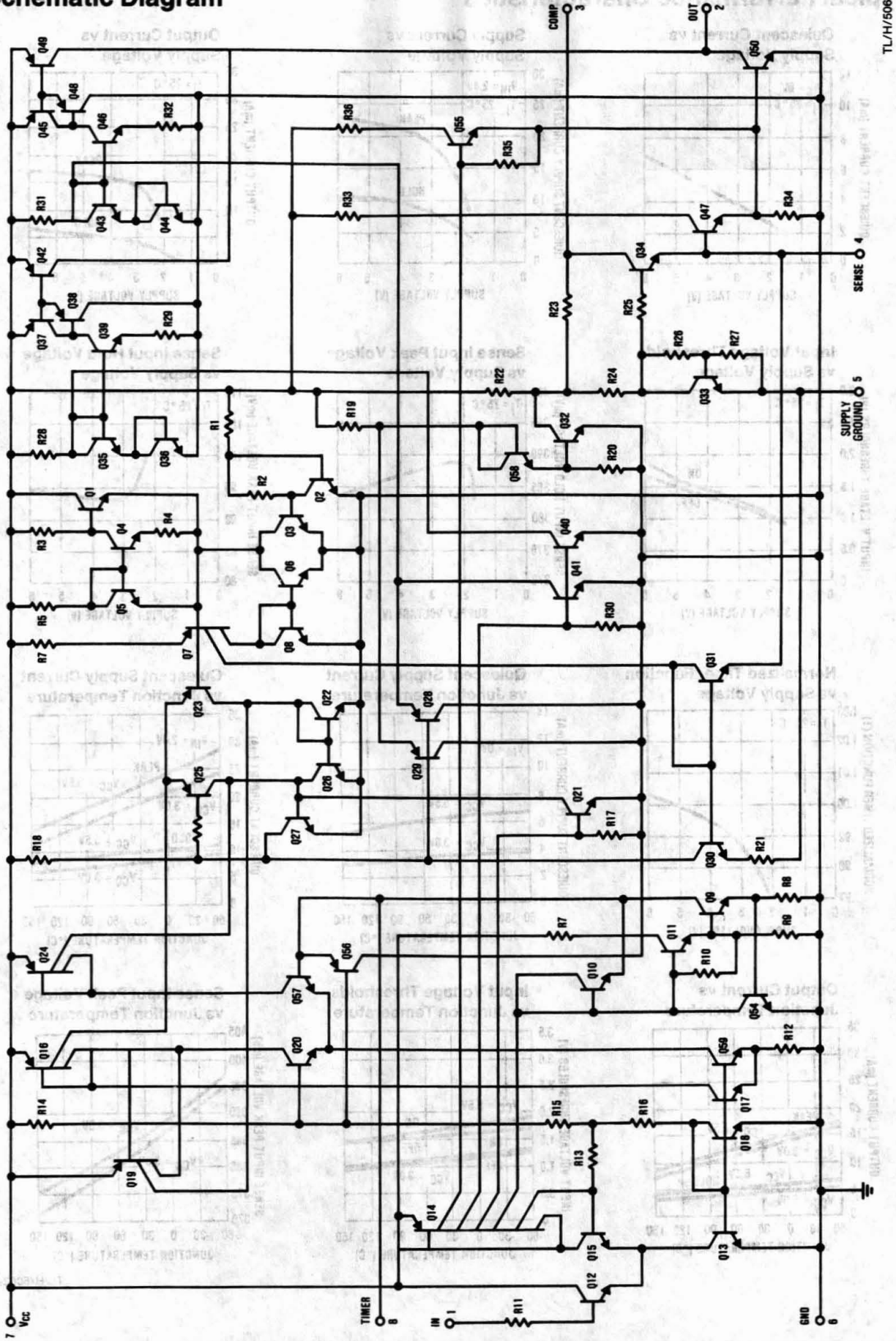
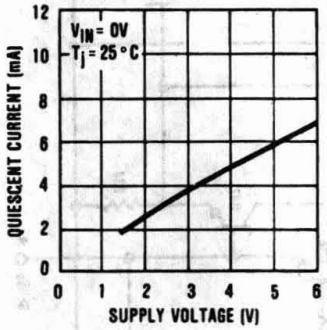


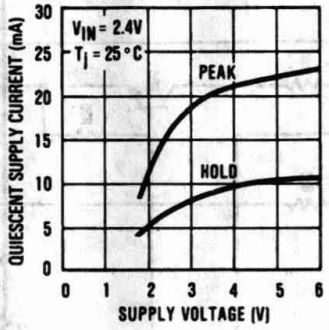
FIGURE 2. LM1949 Circuit

Typical Performance Characteristics

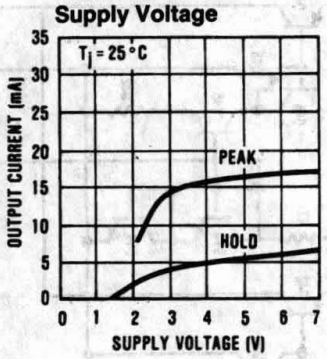
Quiescent Current vs Supply Voltage



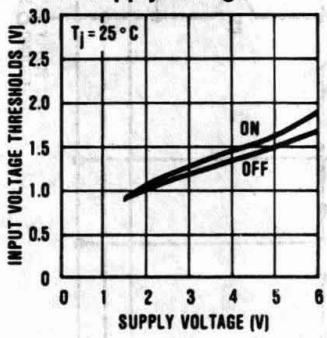
Supply Current vs Supply Voltage



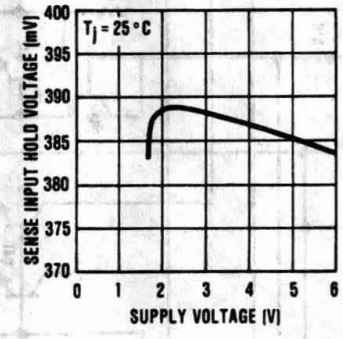
Output Current vs Supply Voltage



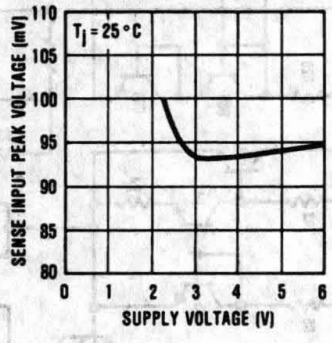
Input Voltage Thresholds vs Supply Voltage



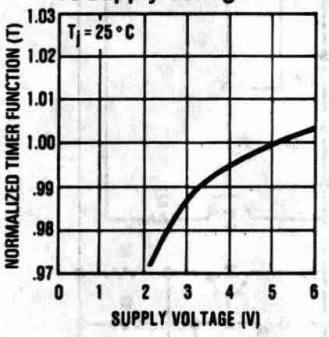
Sense Input Peak Voltage vs Supply Voltage



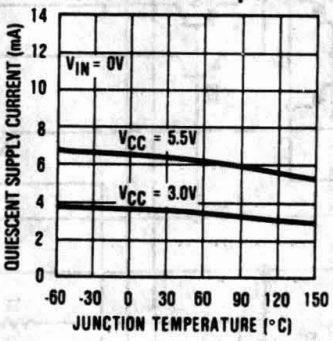
Sense Input Hold Voltage vs Supply Voltage



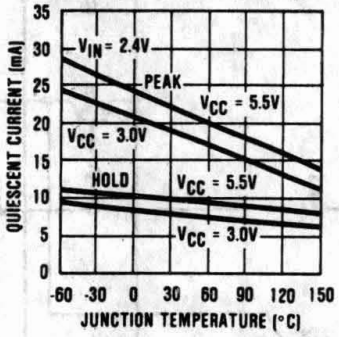
Normalized Timer Function vs Supply Voltage



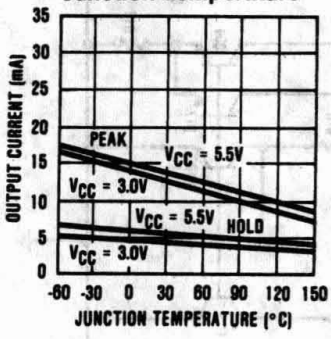
Quiescent Supply Current vs Junction Temperature



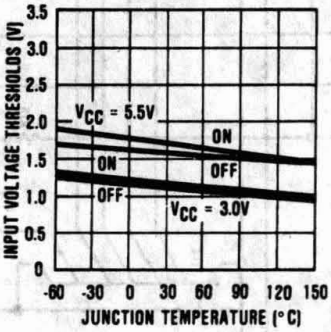
Quiescent Supply Current vs Junction Temperature



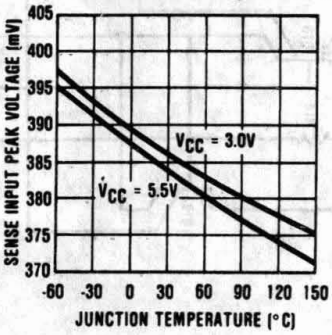
Output Current vs Junction Temperature



Input Voltage Thresholds vs Junction Temperature



Sense Input Peak Voltage vs Junction Temperature



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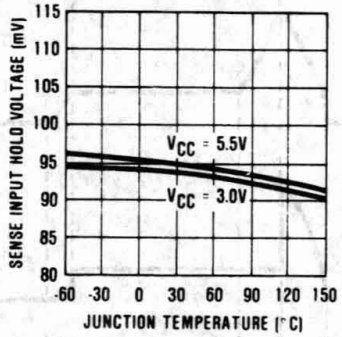
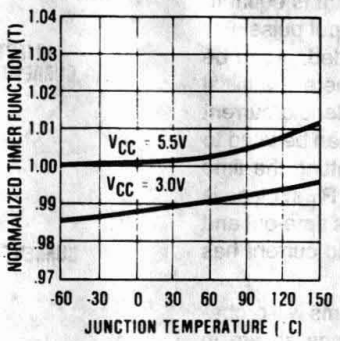
Typical Performance Characteristics (Continued)

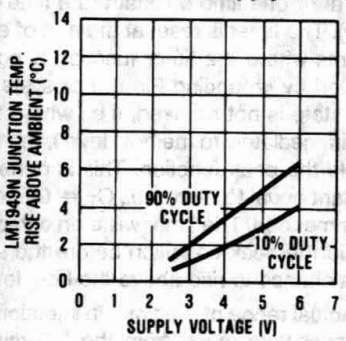
Sense Input Hold Voltage vs Junction Temperature



Normalized Timer Function vs Junction Temperature



LM1949N Junction Temperature Rise Above Ambient vs Supply Voltage



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Application Hints

The injector driver integrated circuits were designed to be used in conjunction with an external controller. The LM1949 derives its input signal from either a control oriented processor (COPS™), microprocessor, or some other system. This input signal, in the form of a square wave with a variable duty cycle and/or variable frequency, is applied to Pin 1. In a typical system, input frequency is proportional to engine RPM. Duty cycle is proportional to the engine load. The circuits discussed are suitable for use in either open or closed loop systems. In closed loop systems, the engine exhaust is monitored and the air-to-fuel mixture is varied (via the duty cycle) to maintain a perfect, or stochiometric, ratio.

INJECTORS

Injectors and solenoids are available in a vast array of sizes and characteristics. Therefore, it is necessary to be able to design a drive system to suit each type of solenoid. The purpose of this section is to enable any system designer to use and modify the LM1949 and associated circuitry to meet the system specifications.

Fuel injectors can usually be modeled by a simple RL circuit. *Figure 3* shows such a model for a typical fuel injector. In actual operation, the value of L_1 will depend upon the status of the solenoid. In other words, L_1 will change depending upon whether the solenoid is open or closed. This effect, if pronounced enough, can be a valuable aid in determining the current necessary to open a particular type of injector. The change in inductance manifests itself as a breakpoint in the initial rise of solenoid current. The waveforms on Page 2 at the sense input show this occurring at approximately 130 mV. Thus, the current necessary to overcome the constrictive forces of that particular injector is 1.3 amperes.

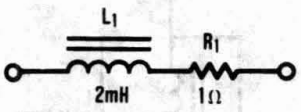

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FIGURE 3. Model of a Typical Fuel Injector

PEAK AND HOLD CURRENTS

The peak and hold currents are determined by the value of the sense resistor R_S. The driver IC, when initiated by a logic 1 signal at Pin 1, initially drives Darlington transistor Q_1 into saturation. The injector current will rise exponentially from zero at a rate dependent upon L_1, R_1, the battery voltage and the saturation voltage of Q_1. The drop across the sense resistor is created by the solenoid current, and when this drop reaches the peak threshold level, typically 385 mV, the IC is tripped from the peak state into the hold state. The IC now behaves more as an op amp and drives Q_1 within a closed loop system to maintain the hold reference voltage, typically 94 mV, across R_S. Once the injector current drops from the peak level to the hold level, it remains there for the duration of the input signal at Pin 1. This mode of operation is preferable when working with solenoids, since the current required to overcome kinetic and constriction forces is often a factor of four or more times the current necessary to hold the injector open. By holding the injector current at one fourth of the peak current, power dissipation in the solenoids and Q_1 is reduced by at least the same factor.

In the circuit of *Figure 1*, it was known that the type of injector shown opens when the current exceeds 1.3 amps and closes when the current then falls below 0.3 amps. In order to guarantee injector operation over the life and temperature range of the system, a peak current of approximately 4 amps was chosen. This led to a value of R_S of 0.1Ω. Dividing the peak and hold thresholds by this factor gives peak and hold currents through the solenoid of 3.85 amps and 0.94 amps respectively.

Different types of solenoids may require different values of current. The sense resistor R_S may be changed accordingly. An 8-amp peak injector would use R_S equal to .05Ω, etc. Note that for large currents above one amp, IR drops within the component leads or printed circuit board may create substantial errors unless appropriate care is taken. The sense input and sense ground leads (Pins 4 and 5 respectively), should be Kelvin connected to R_S. High current should not be allowed to flow through any part of these traces or connections. An easy solution to this problem on double-sided PC boards (without plated-through holes) is to have the high current trace and sense trace attach to the R_S lead from opposite sides of the board.

TIMER FUNCTION

The purpose of the timer function is to limit the power dissipated by the injector or solenoid under certain conditions. Specifically, when the battery voltage is low due to engine cranking, or just undercharged, there may not be sufficient voltage available for the injector to achieve the peak current. In the *Figure 2* waveforms under the low battery condition, the injector current can be seen to be leveling out at 3

Timer Function (Continued)

amps, or 1 amp below the normal threshold. Since continuous operation at 3 amps may overheat the injectors, the timer function on the IC will force the transition into the hold state after one time constant (the time constant is equal to R_TC_T). The timer is reset at the end of each input pulse. For systems where the timer function is not needed, it can be disabled by grounding Pin 8. For systems where the initial peak state is not required, (i.e., where the solenoid current rises immediately to the hold level), the timer can be used to disable the peak function. This is done by setting the time constant equal to zero, (i.e., $C_T = 0$). Leaving R_T in place is recommended. The timer will then complete its time-out and disable the peak condition before the solenoid current has had a chance to rise above the hold level.

The actual range of the timer in injection systems will probably never vary much from the 3.9 milliseconds shown in *Figure 1*. However, the actual useful range of the timer extends from microseconds to seconds, depending on the component values chosen. The useful range of R_T is approximately 1k to 240k. The capacitor C_T is limited only by stray capacitances for low values and by leakages for large values.

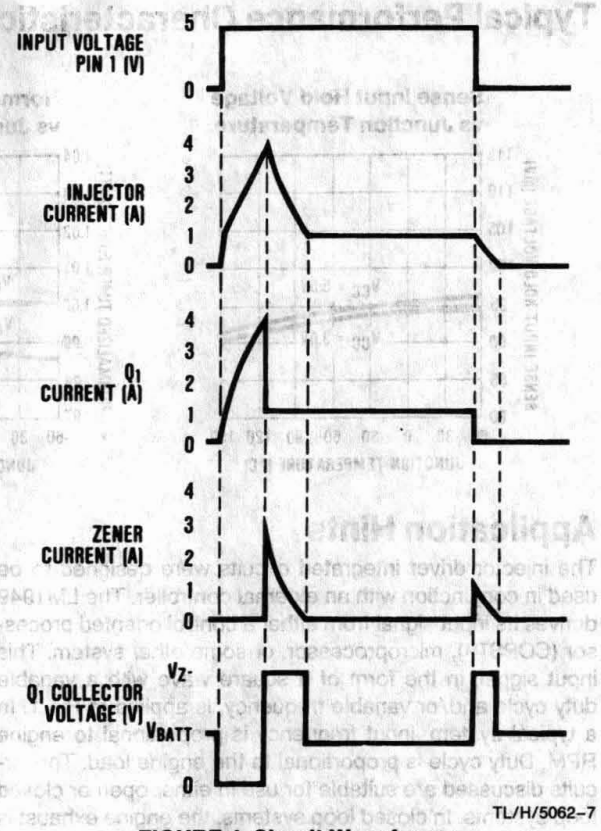
The capacitor reset time at the end of each controller pulse is determined by the supply voltage and the capacitor value. The IC resets the capacitor to an initial voltage (V_{BE}) by discharging it with a current of approximately 15 mA. Thus, a 0.1 μF cap is reset in approximately 25 μs.

COMPENSATION

Compensation of the error amplifier provides stability for the circuit during the hold state. External compensation (from Pin 2 to Pin 3) allows each design to be tailored for the characteristics of the system and/or type of Darlington power device used. In the vast majority of designs, the value or type of the compensation capacitor is not critical. Values of 100 pF to 0.1 μF work well with the circuit of *Figure 1*. The value shown of .01 μF (disc) provides a close optimum in choice between economy, speed, and noise immunity. In some systems, increased phase and gain margin may be acquired by bypassing the collector of Q_1 to ground with an appropriately rated 0.1 μF capacitor. This is, however, rarely necessary.

FLYBACK ZENER

The purpose of zener Z_1 is twofold. Since the load is inductive, a voltage spike is produced at the collector of Q_1 anytime the injector current is reduced. This occurs at the peak-to-hold transition, (when the current is reduced to one fourth of its peak value), and also at the end of each input pulse, (when the current is reduced to zero). The zener provides a current path for the inductive kickback, limiting the voltage spike to the zener value and preventing Q_1 from damaging voltage levels. Thus, the rated zener voltage at the system peak current must be less than the guaranteed minimum breakdown of Q_1. Also, even while Z_1 is conducting the majority of the injector current during the peak-to-hold transition (see *Figure 4*), Q_1 is operating at the hold current level. This fact is easily overlooked and, as described in the following text, can be corrected if necessary. Since the error amplifier in the IC demands 94 mV across R_S, Q_1 will be biased to provide exactly that. Thus, the safe operating area (SOA) of Q_1 must include the hold current with a V_{CE} of Z_1 volts. For systems where this is not desired, the zener anode may be reconnected to the top of R_S as shown in *Figure 5*. Since the voltage across the sense resistor now accurately portrays the injector current at all times, the error



TL/H/5062–7

FIGURE 4. Circuit Waveforms

amplifier keeps Q_1 off until the injector current has decayed to the proper value. The disadvantage of this particular configuration is that the ungrounded zener is more difficult to heat sink if that becomes necessary.

The second purpose of Z_1 is to provide system transient protection. Automotive systems are susceptible to a vast array of voltage transients on the battery line. Though their duration is usually only milliseconds long, Q_1 could suffer permanent damage unless buffered by the injector and Z_1. This is one reason why a zener is preferred over a clamp diode back to the battery line, the other reason being long decay times.

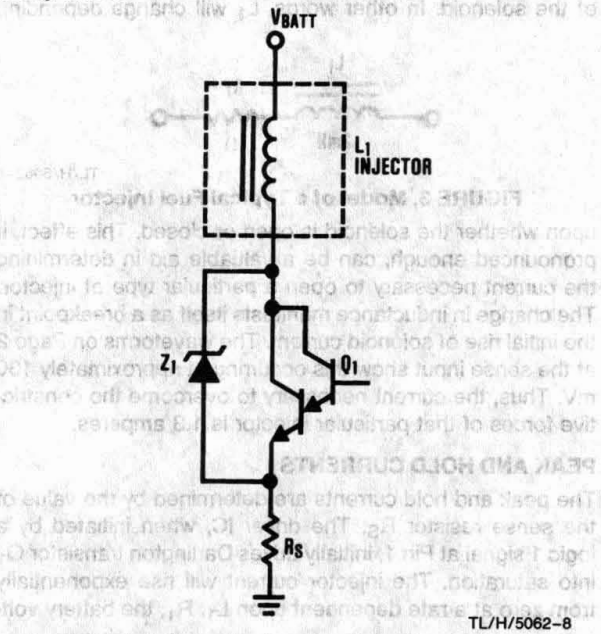


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FIGURE 5. Alternate Configuration for Zener Z_1

POWER DISSIPATION

The power dissipation of the system shown in *Figure 1* is dependent upon several external factors, including the frequency and duty cycle of the input waveform to Pin 1. Calculations are made more difficult since there are many discontinuities and breakpoints in the power waveforms of the various components, most notably at the peak-to-hold transition. Some generalizations can be made for normal operation. For example, in a typical cycle of operation, the majority of dissipation occurs during the hold state. The hold state is usually much longer than the peak state, and in the peak state nearly all power is stored as energy in the magnetic field of the injector, later to be dumped mostly through the zener. While this assumption is less accurate in the case of low battery voltage, it nevertheless gives an unexpectedly accurate set of approximations for general operation.

The following nomenclature refers to *Figure 1*. Typical values are given in parentheses:

R_S = Sense Resistor (0.1Ω)
V_H = Sense Input Hold Voltage (.094V)
V_p = Sense Input Peak Voltage (.385V)
V_Z = Z_1 Zener Breakdown Voltage (33V)
V_{BATT} = Battery Voltage (14V)
L_1 = Injector Inductance (.002H)
R_1 = Injector Resistance (1Ω)
n = Duty Cycle of Input Voltage of Pin 1 (0 to 1)
f = Frequency of Input (10Hz to 200Hz)

Q_1 Power Dissipation:

$$P_Q \approx n \bullet V_{BATT} \bullet \frac{V_H}{R_S} \text{ Watts}$$

Zener Dissipation:

$$P_Z \approx V_Z \bullet L_1 \bullet f \bullet \frac{(V_P^2 + V_H^2)}{((V_Z - V_{BATT}) \bullet R_S^2)} \text{ Watts}$$

Injector Dissipation:

$$P_I \approx n \bullet R_1 \bullet \frac{V_H^2}{R_S^2} \text{ Watts}$$

Sense Resistor:

$$P_R \approx n \frac{V_H^2}{R_S^2} \text{ Watts}$$

$$P_R \text{ (worst case)} \approx n \frac{V_P^2}{R_S^2} \text{ Watts}$$

SWITCHING INJECTOR DRIVER CIRCUIT

The power dissipation of the system, and especially of Q_1, can be reduced by employing a switching injector driver circuit. Since the injector load is mainly inductive, transistor Q_1 can be rapidly switched on and off in a manner similar to switching regulators. The solenoid inductance will naturally integrate the voltage to produce the required injector current, while the power consumed by Q_1 will be reduced. A note of caution: The large amplitude switching voltages that are present on the injector can and do generate a tremendous amount of radio frequency interference (RFI). Because of this, switching circuits are not recommended. The extra cost of shielding can easily exceed the savings of reduced power. In systems where switching circuits are mandatory, extensive field testing is required to guarantee that RFI cannot create problems with engine control or entertainment equipment within the vicinity.

The LM1949 can be easily modified to function as a switcher. Accomplished with the circuit of *Figure 7*, the only additional components required are two external resistors, R_A and R_B. Additionally, the zener needs to be reconnected, as shown, to R_S. The amount of ripple on the hold current is easily controlled by the resistor ratio of R_A to R_B. R_B is kept small so that sense input bias current (typically 0.3 mA) has negligible effect on V_H. Duty cycle and frequency of oscillation during the hold state are dependent on the injector characteristics, R_A, R_B, and the zener voltage as shown in the following equations.

$$\text{Hold Current} \approx \frac{V_H}{R_S}$$

$$\text{Minimum Hold Current} \approx \frac{\left(V_H - \frac{R_B}{R_A} \bullet V_Z\right)}{R_S}$$

$$\text{Ripple or } \Delta I \text{ Hold} \approx \frac{R_B}{R_A} \bullet V_Z \bullet \frac{1}{R_S}$$

$$f_o \approx \frac{R_S}{L_1} \bullet \frac{R_A}{R_B} \bullet \frac{V_{BATT}}{V_Z} \bullet \left(1 - \frac{V_{BATT}}{V_Z}\right)$$

f_o = Hold State Oscillation Frequency

$$\text{Duty Cycle of } f_o \approx \frac{V_{BATT}}{V_Z}$$

Component Power Dissipation

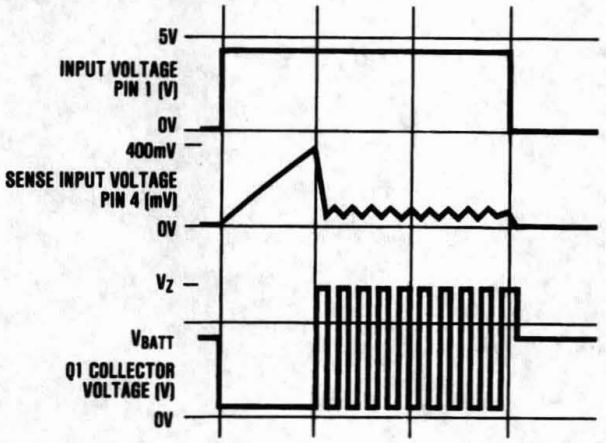
$$P_Q \approx n \bullet \left(1 - \frac{V_{BATT}}{V_Z}\right) \bullet \frac{V_{SAT}}{R_S} \bullet V_H$$

V_{SAT} = Q_1 Saturation Volt @ ~ 1 Amp (1.5V)

$$P_Z \approx n \bullet \frac{V_{BATT} \bullet V_H}{R_S}$$

$$P_{RA} \approx \frac{V_B \bullet V_Z}{R_1}$$

As shown, the power dissipation by Q_1 in this manner is substantially reduced. Measurements made with a thermocouple on the bench indicated better than a fourfold reduction in power in Q_1. However, the power dissipation of the zener (which is independent of the zener voltage chosen) is increased over the circuit of *Figure 1*.



TL/H/5062–9

FIGURE 6. Switching Waveforms

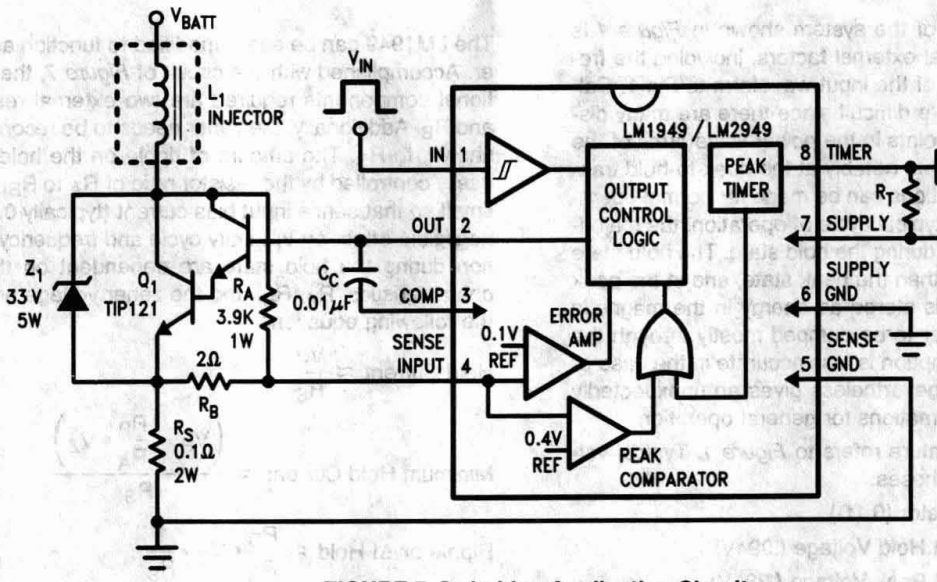


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FIGURE 7. Switching Application Circuit

National Semiconductor

LM9044 Lambda Sensor Interface Amplifier

General Description

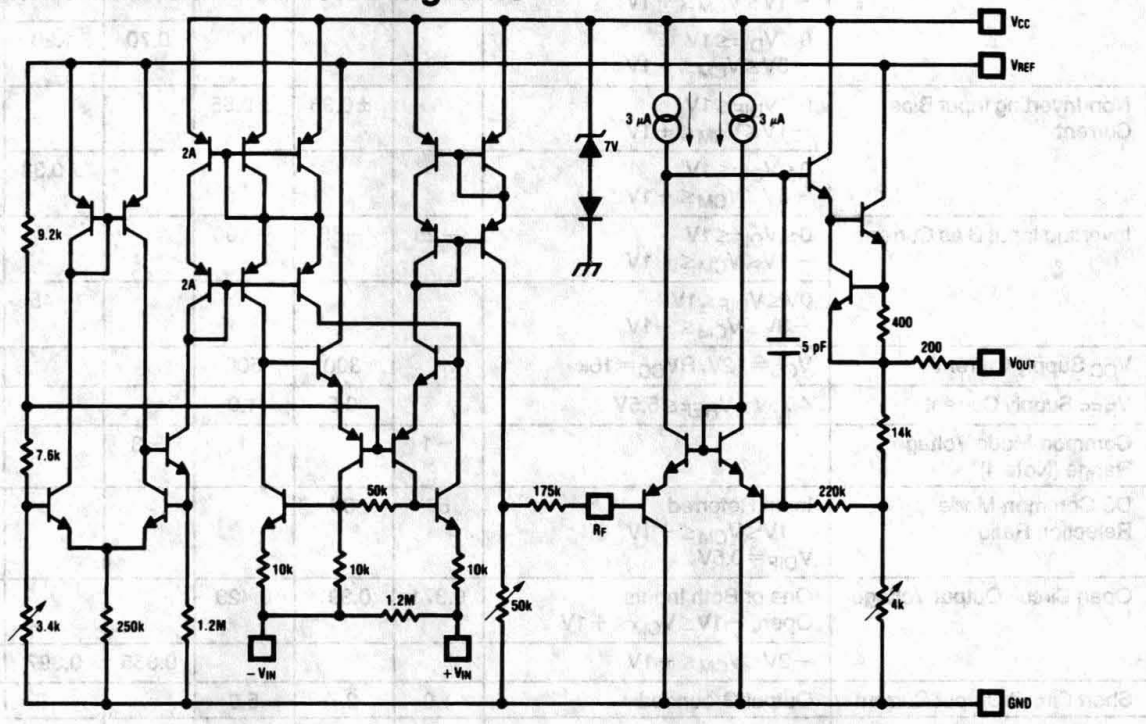
The LM9044 is a precision differential amplifier specifically designed for operation in the automotive environment. Gain accuracy is guaranteed over the entire automotive temperature range (−40°C to +125°C) and is factory trimmed prior to package assembly. The input circuitry has been specifically designed to reject common-mode signals as much as 3V below ground on a single positive power supply. This facilitates the use of sensors which are grounded at the engine block while the LM9044 itself is grounded at chassis potential. An external capacitor sets the maximum operating frequency of the amplifier, thereby filtering high frequency transients. Both inputs are protected against accidental shorting to the battery and against load dump transients. The input impedance is typically 1 MΩ.

The output op amp is capable of driving capacitive loads and is fully protected. Also, internal circuitry has been provided to detect open circuit conditions on either or both inputs and force the output to a "home" position (a ratio of the external reference voltage).

Features

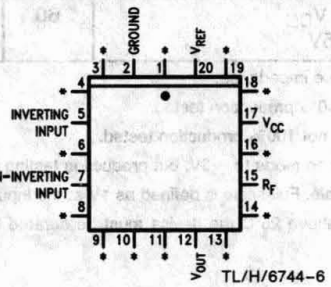
- Normal circuit operation guaranteed with inputs up to 3V below ground on a single supply
- Gain factory trimmed and guaranteed over temperature (±3% of full-scale from −40°C to +125°C)
- Low power consumption (typically 1 mA)
- Fully protected inputs
- Input open circuit detection
- Operation guaranteed over the entire automotive temperature range (−40°C to +125°C)
- Single supply operation

Schematic and Connection Diagrams



TL/H/6744-1

Plastic Chip Carrier Package



TL/H/6744-6

Top View

Order Number LM9044V
See NS Package Number V20A

*Pins 1, 3, 4, 6, 8, 9, 10, 11, 13, 14, 16, 18, 19 are trim pins and should be left floating.

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

V_{CC} Supply Voltage (RV_{CC} = 15 kΩ)	±60V
V_{REF} Supply Voltage	−0.3V to +6V
DC Input Voltage (Either Input)	−3V to +16V
Input Transients (Note 1)	±60V
Power Dissipation (see Note 6)	1350 mW
Output Short Circuit Duration	Indefinite
Operating Temperature Range	−40°C to +125°C
Storage Temperature Range	−65°C to +150°C
Soldering Information	
Plastic Chip Carrier Package	
Vapor Phase (60 seconds)	215°C
Infrared (15 seconds)	220°C

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.

Electrical Characteristics V_{CC} = 12V, V_{REF} = 5V, −40°C ≤ T_A ≤ 125°C unless otherwise noted

Parameter	Conditions	(Note 2)			(Note 3)			Units
		Min	Typ	Max	Min	Typ	Max	
Differential Voltage Gain	V_{DIF} = 0.5V −1V ≤ V_{CM} ≤ +1V	4.41	4.50	4.59				V/V
	V_{DIF} = 0.5V, −3V ≤ V_{CM} ≤ +1V				4.36	4.50	4.64	V/V
Gain Error (Note 5)	0 ≤ V_{DIF} ≤ 1V −1V ≤ V_{CM} ≤ +1V	−2	0	2				%/FS
	0 ≤ V_{DIF} ≤ 1V −3V ≤ V_{CM} ≤ +1V				−3	0	3	%/FS
Differential Input Resistance	0 ≤ V_{DIF} ≤ 1V −1V ≤ V_{CM} ≤ +1V	0.95	1.20	3.00				MΩ
	0 ≤ V_{DIF} ≤ 1V −3V ≤ V_{CM} ≤ +1V				0.70	1.20	4.00	MΩ
Non-Inverting Input Bias Current	0 ≤ V_{DIF} ≤ 1V −1V ≤ V_{CM} ≤ +1V		±0.38	±0.65				μA
	0 ≤ V_{DIF} ≤ 1V −3V ≤ V_{CM} ≤ +1V					±0.38	±1.5	μA
Inverting Input Bias Current	0 ≤ V_{DIF} ≤ 1V −1V ≤ V_{CM} ≤ +1V	−25	−65	−100				μA
	0V ≤ V_{DIF} ≤ 1V −3V ≤ V_{CM} ≤ +1V					−45	−150	μA
V_{CC} Supply Current	V_{CC} = 12V, RV_{CC} = 15k		300	500				μA
V_{REF} Supply Current	4.75V ≤ V_{REF} ≤ 5.5V		0.5	1.0				mA
Common-Mode Voltage Range (Note 4)		−1		1	−3		1	V
DC Common-Mode Rejection Ratio	Input Referred −1V ≤ V_{CM} ≤ +1V V_{DIF} = 0.5V	50	60					dB
Open Circuit Output Voltage	One or Both Inputs Open, −1V ≤ V_{CM} ≤ +1V	0.371	0.397	0.423				XV_{REF}
	−3V ≤ V_{CM} ≤ +1V				0.365	0.397	0.429	XV_{REF}
Short Circuit Output Current	Output Grounded	1.0	2.7	5.0				mA
V_{CC} Power Supply Rejection Ratio	V_{CC} = 12V, RV_{CC} = 15K V_{DIF} = 0.5V	50	65					dB
V_{REF} Power Supply Rejection Ratio	V_{REF} = 5 V_{DC} V_{DIF} = 0.5V	60	74					dB

Note 1: This test is performed with a 1000Ω source impedance.

Note 2: These parameters are guaranteed and 100% production tested.

Note 3: These parameters will be guaranteed but not 100% production tested.

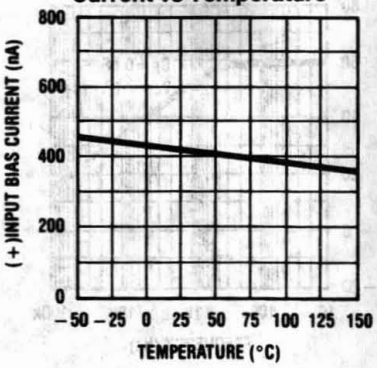
Note 4: The LM9044 has been designed to common-mode to −3V, but production testing is only performed at ±1V.

Note 5: Gain error is given as a percent of full-scale. Full-scale is defined as 1V at the input and 4.5V at the output.

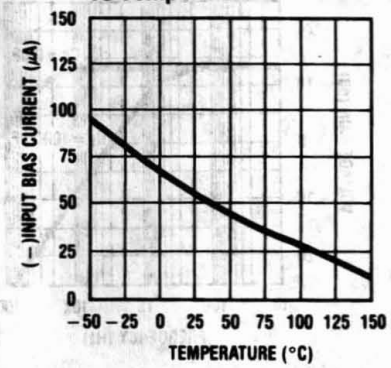
Note 6: For operation in ambient temperatures above 25°C the device must be derated based on a maximum junction temperature of 150°C and a thermal resistance of 93°C/W junction to ambient.

Typical Performance Characteristics

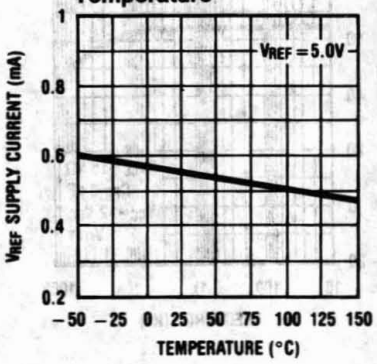
Non-Inverting Input Bias Current vs Temperature



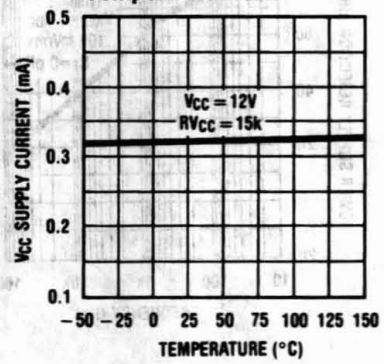
Inverting Input Bias Current vs Temperature



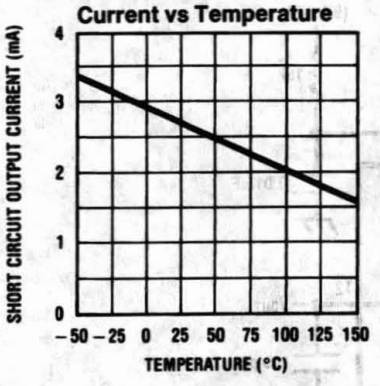
V_{REF} Supply Current vs Temperature



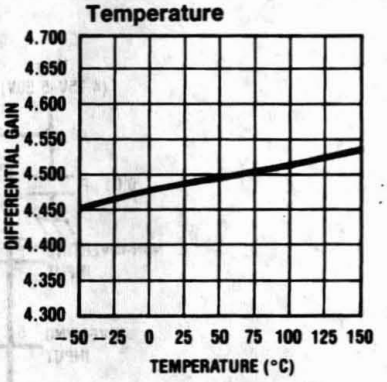
V_{CC} Supply Current vs Temperature



Short Circuit Output Current vs Temperature



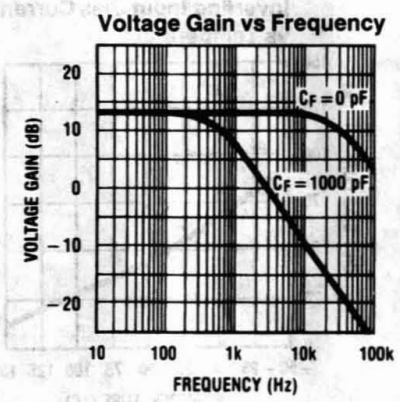
Differential Gain vs Temperature

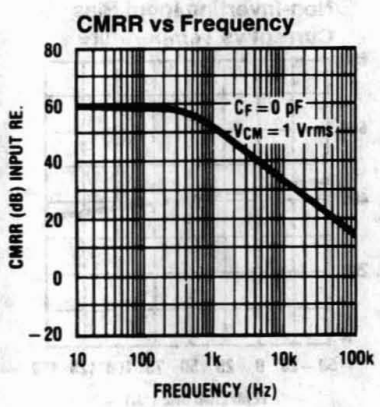


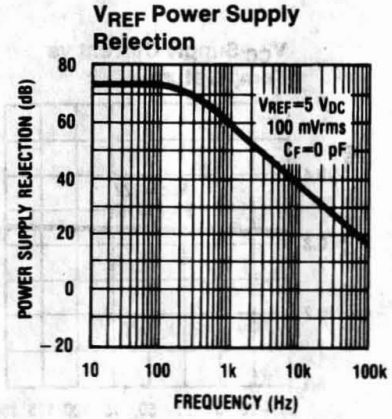
TL/H/6744–3

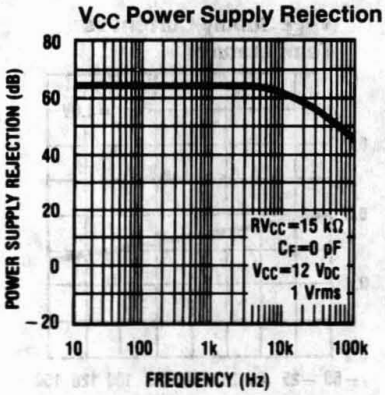
3

Typical Performance Characteristics (Continued)



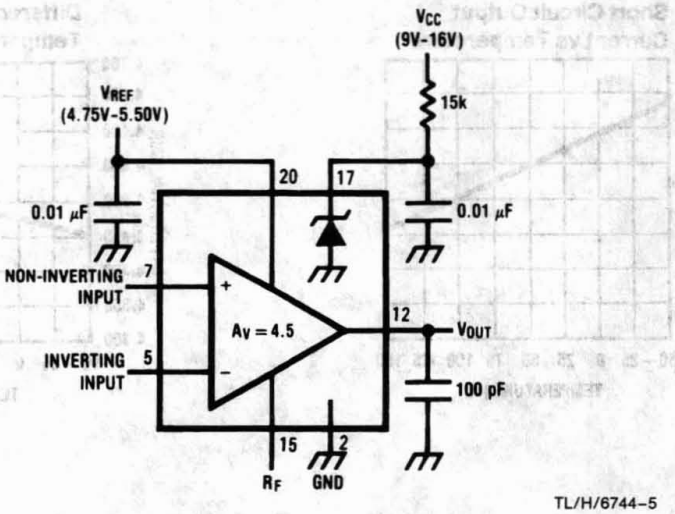






TL/H/6744–4

Test Circuit



TL/H/6744–5

National Semiconductor

LM2907/LM2917 Frequency to Voltage Converter

General Description

The LM2907, LM2917 series are monolithic frequency to voltage converters with a high gain op amp/comparator designed to operate a relay, lamp, or other load when the input frequency reaches or exceeds a selected rate. The tachometer uses a charge pump technique and offers frequency doubling for low ripple, full input protection in two versions (LM2907-8, LM2917-8) and its output swings to ground for a zero frequency input.

Advantages

- Output swings to ground for zero frequency input
- Easy to use; $V_{OUT} = f_{IN} \times V_{CC} \times R1 \times C1$
- Only one RC network provides frequency doubling
- Zener regulator on chip allows accurate and stable frequency to voltage or current conversion (LM2917)

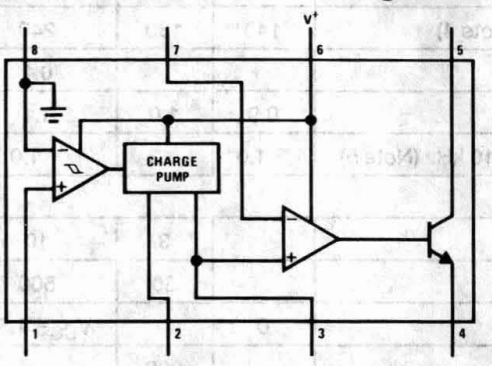
Features

- Ground referenced tachometer input interfaces directly with variable reluctance magnetic pickups
- Op amp/comparator has floating transistor output
- 50 mA sink or source to operate relays, solenoids, meters, or LEDs
- Frequency doubling for low ripple
- Tachometer has built-in hysteresis with either differential input or ground referenced input
- Built-in zener on LM2917
- ±0.3% linearity typical
- Ground referenced tachometer is fully protected from damage due to swings above V_{CC} and below ground

Applications

- Over/under speed sensing
- Frequency to voltage conversion (tachometer)
- Speedometers
- Breaker point dwell meters
- Hand-held tachometer
- Speed governors
- Cruise control
- Automotive door lock control
- Clutch control
- Horn control
- Touch or sound switches

Block and Connection Diagrams Dual-In-Line and Small Outline Packages, Top Views



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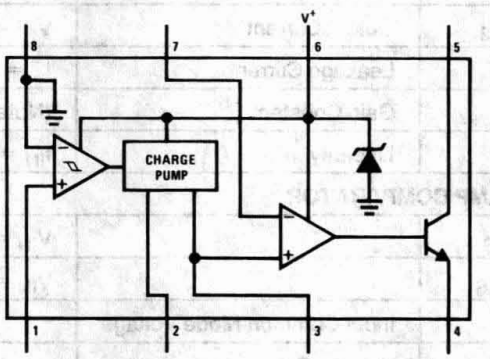
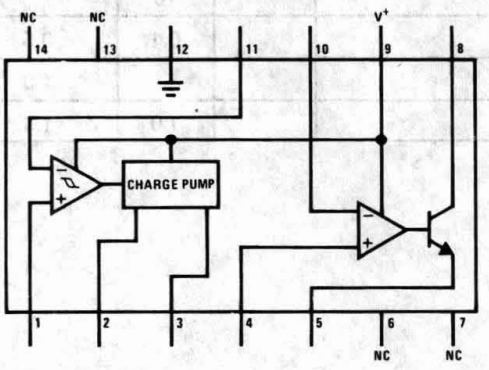
Order Number LM2907M-8 or LM2907N-8
See NS Package Number M08A or N08E



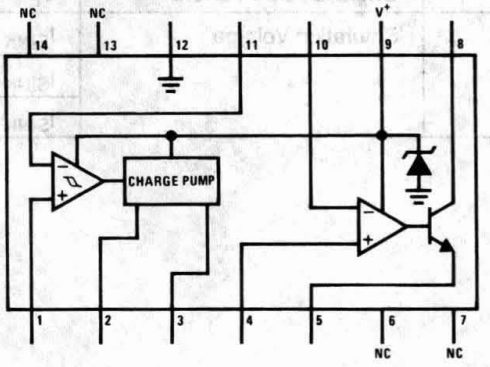
TL/H/7942–2

Order Number LM2917M-8 or LM2917N-8
See NS Package Number M08A or N08E



TL/H/7942–3

Order Number LM2907N
See NS Package Number N14A



TL/H/7942–4

Order Number LM2917M or LM2917N
See NS Package Number M14A or N14A

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	28V
Supply Current (Zener Options)	25 mA
Collector Voltage	28V
Differential Input Voltage	
Tachometer	28V
Op Amp/Comparator	28V
Input Voltage Range	
Tachometer LM2907-8, LM2917-8	±28V
LM2907, LM2917	0.0V to +28V
Op Amp/Comparator	0.0V to +28V
Power Dissipation	
LM2907-8, LM2917-8	1200 mW
LM2907-14, LM2917-14	1580 mW
(See Note 1)	
Operating Temperature Range	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Soldering Information	
Dual-In-Line Package	
Soldering (10 seconds)	260°C
Small Outline Package	
Vapor Phase (60 seconds)	215°C
Infrared (15 seconds)	220°C

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.

Electrical Characteristics V_{CC} = 12 V_{DC}, T_A = 25°C, see test circuit

Symbol	Parameter	Conditions	Min	Typ	Max	Units
TACHOMETER						
	Input Thresholds	V_{IN} = 250 mVp-p @ 1 kHz (Note 2)	±10	±25	±40	mV
	Hysteresis	V_{IN} = 250 mVp-p @ 1 kHz (Note 2)		30		mV
	Offset Voltage	V_{IN} = 250 mVp-p @ 1 kHz (Note 2)				
	LM2907/LM2917			3.5	10	mV
	LM2907-8/LM2917-8			5	15	mV
	Input Bias Current	V_{IN} = ±50 mV_{DC}		0.1	1	μA
V_{OH}	Pin 2	V_{IN} = +125 mV_{DC} (Note 3)		8.3		V
V_{OL}	Pin 2	V_{IN} = −125 mV_{DC} (Note 3)		2.3		V
I_2, I_3	Output Current	V2 = V3 = 6.0V (Note 4)	140	180	240	μA
I_3	Leakage Current	I2 = 0, V3 = 0			0.1	μA
K	Gain Constant	(Note 3)	0.9	1.0	1.1	
	Linearity	f_{IN} = 1 kHz, 5 kHz, 10 kHz (Note 5)	−1.0	0.3	+1.0	%
OP/AMP COMPARATOR						
V_{OS}		V_{IN} = 6.0V		3	10	mV
I_{BIAS}		V_{IN} = 6.0V		50	500	nA
	Input Common-Mode Voltage		0		V_{CC}−1.5V	V
	Voltage Gain			200		V/mV
	Output Sink Current	V_C = 1.0	40	50		mA
	Output Source Current	V_E = V_{CC} −2.0		10		mA
	Saturation Voltage	I_{SINK} = 5 mA		0.1	0.5	V
		I_{SINK} = 20 mA			1.0	V
		I_{SINK} = 50 mA		1.0	1.5	V

Electrical Characteristics V_{CC} = 12 V_{DC}, T_A = 25°C, see test circuit (Continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
ZENER REGULATOR						
	Regulator Voltage	R_{DROP} = 470Ω		7.56		V
	Series Resistance			10.5	15	Ω
	Temperature Stability			+1		mV/°C
	TOTAL SUPPLY CURRENT			3.8	6	mA

Note 1: For operation in ambient temperatures above 25°C, the device must be derated based on a 150°C maximum junction temperature and a thermal resistance of 101°C/W junction to ambient for LM2907-8 and LM2917-8, and 79°C/W junction to ambient for LM2907-14 and LM2917-14.

Note 2: Hysteresis is the sum $+V_{TH} - (-V_{TH})$, offset voltage is their difference. See test circuit.

Note 3: V_{OH} is equal to $\frac{3}{4} \times V_{CC} - 1 V_{BE}$, V_{OL} is equal to $\frac{1}{4} \times V_{CC} - 1 V_{BE}$ therefore $V_{OH} - V_{OL} = V_{CC}/2$. The difference, $V_{OH} - V_{OL}$, and the mirror gain, I_2/I_3, are the two factors that cause the tachometer gain constant to vary from 1.0.

Note 4: Be sure when choosing the time constant R1 × C1 that R1 is such that the maximum anticipated output voltage at pin 3 can be reached with $I_3 \times$ R1. The maximum value for R1 is limited by the output resistance of pin 3 which is greater than 10 MΩ typically.

Note 5: Nonlinearity is defined as the deviation of V_{OUT} (@ pin 3) for f_{IN} = 5 kHz from a straight line defined by the V_{OUT} @ 1 kHz and V_{OUT} @ 10 kHz. C1 = 1000 pF, R1 = 68k and C2 = 0.22 mFd.

General Description (Continued)

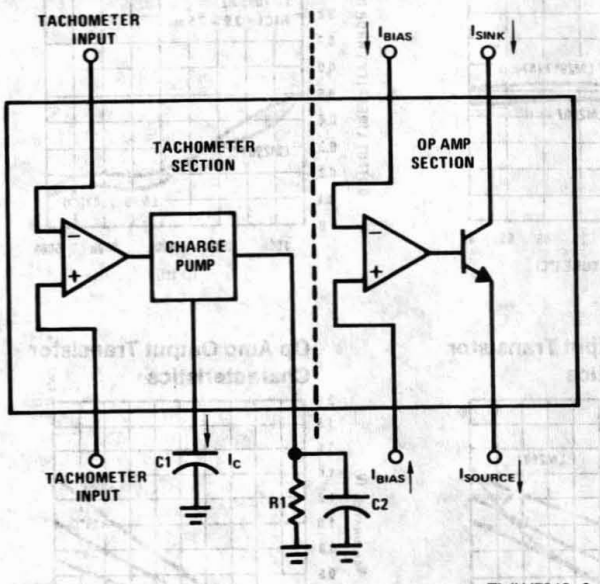
The op amp/comparator is fully compatible with the tachometer and has a floating transistor as its output. This feature allows either a ground or supply referred load of up to 50 mA. The collector may be taken above V_{CC} up to a maximum V_{CE} of 28V.

The two basic configurations offered include an 8-pin device with a *ground referenced tachometer* input and an internal connection between the tachometer output and the op amp non-inverting input. This version is well suited for single speed or frequency switching or fully buffered frequency to voltage conversion applications.

The more versatile configurations provide differential tachometer input and uncommitted op amp inputs. With this version the tachometer input may be floated and the op amp becomes suitable for active filter conditioning of the tachometer output.

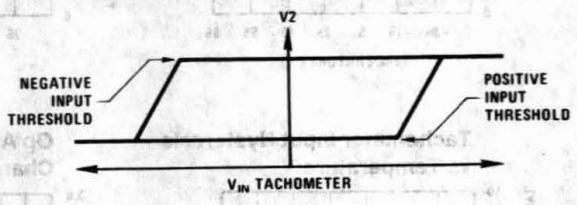
Both of these configurations are available with an active shunt regulator connected across the power leads. The regulator clamps the supply such that stable frequency to voltage and frequency to current operations are possible with any supply voltage and a suitable resistor.

Test Circuit and Waveform



TL/H/7942–6

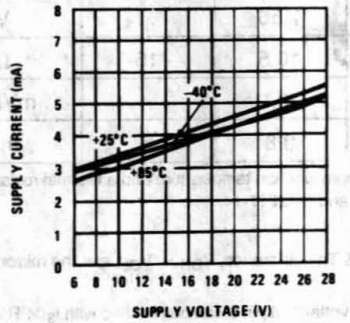
Tachometer Input Threshold Measurement



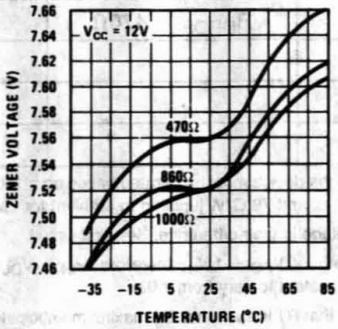
TL/H/7942–7

Typical Performance Characteristics

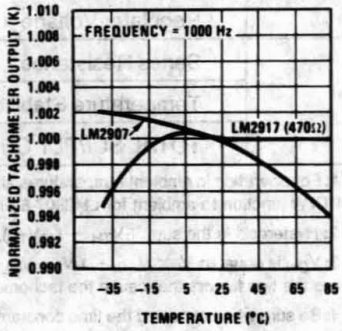
Total Supply Current



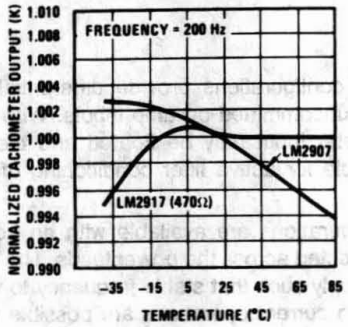
Zener Voltage vs Temperature



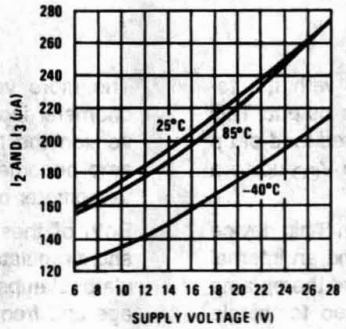
Normalized Tachometer Output vs Temperature



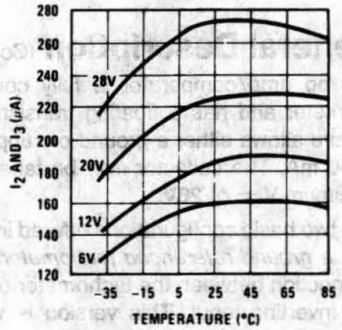
Normalized Tachometer Output vs Temperature



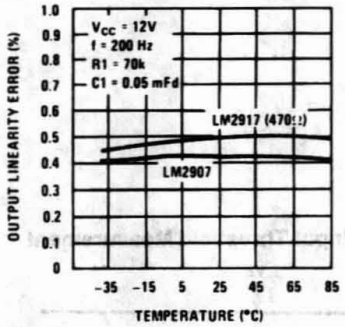
Tachometer Currents I_2 and I_3 vs Supply Voltage



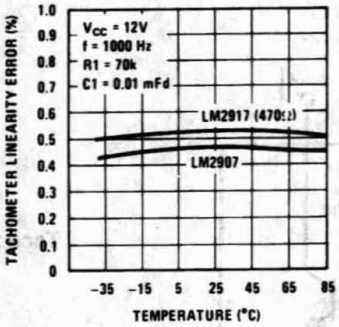
Tachometer Currents I_2 and I_3 vs Temperature



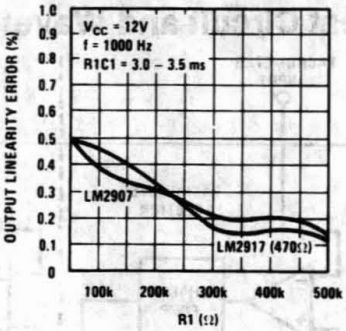
Tachometer Linearity vs Temperature



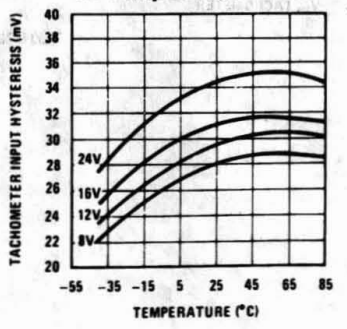
Tachometer Linearity vs Temperature



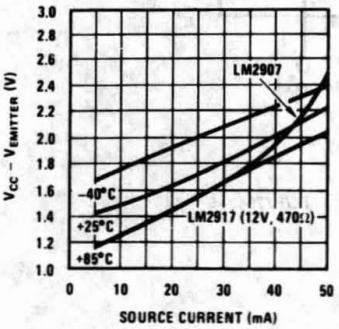
Tachometer Linearity vs R1



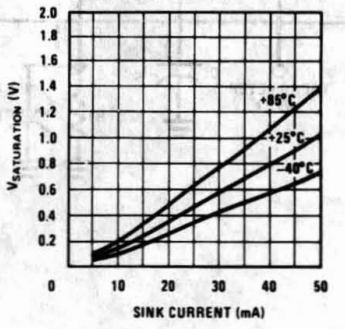
Tachometer Input Hysteresis vs Temperature



Op Amp Output Transistor Characteristics



Op Amp Output Transistor Characteristics



TL/H/7942–5

Applications Information

The LM2907 series of tachometer circuits is designed for minimum external part count applications and maximum versatility. In order to fully exploit its features and advantages let's examine its theory of operation. The first stage of operation is a differential amplifier driving a positive feedback flip-flop circuit. The input threshold voltage is the amount of differential input voltage at which the output of this stage changes state. Two options (LM2907-8, LM2917-8) have one input internally grounded so that an input signal must swing above and below ground and exceed the input thresholds to produce an output. This is offered specifically for magnetic variable reluctance pickups which typically provide a single-ended ac output. This single input is also fully protected against voltage swings to ±28V, which are easily attained with these types of pickups.

The differential input options (LM2907, LM2917) give the user the option of setting his own input switching level and still have the hysteresis around that level for excellent noise rejection in any application. Of course in order to allow the inputs to attain common-mode voltages above ground, input protection is removed and neither input should be taken outside the limits of the supply voltage being used. It is very important that an input not go below ground without some resistance in its lead to limit the current that will then flow in the epi-substrate diode.

Following the input stage is the charge pump where the input frequency is converted to a dc voltage. To do this requires one timing capacitor, one output resistor, and an integrating or filter capacitor. When the input stage changes state (due to a suitable zero crossing or differential voltage on the input) the timing capacitor is either charged or discharged linearly between two voltages whose difference is $V_{CC}/2$. Then in one half cycle of the input frequency or a time equal to $1/2\ f_{IN}$ the change in charge on the timing capacitor is equal to $V_{CC}/2 \times C1$. The average amount of current pumped into or out of the capacitor then is:

$$\frac{\Delta Q}{T} = i_{c(AVG)} = C1 \times \frac{V_{CC}}{2} \times (2f_{IN}) = V_{CC} \times f_{IN} \times C1$$

The output circuit mirrors this current very accurately into the load resistor R1, connected to ground, such that if the pulses of current are integrated with a filter capacitor, then $V_O = i_c \times R1$, and the total conversion equation becomes:

$$V_O = V_{CC} \times f_{IN} \times C1 \times R1 \times K$$

Where K is the gain constant—typically 1.0.

The size of C2 is dependent only on the amount of ripple voltage allowable and the required response time.

CHOOSING R1 AND C1

There are some limitations on the choice of R1 and C1 which should be considered for optimum performance. The timing capacitor also provides internal compensation for the charge pump and should be kept larger than 500 pF for very accurate operation. Smaller values can cause an error current on R1, especially at low temperatures. Several considerations must be met when choosing R1. The output current at pin 3 is internally fixed and therefore $V_O/R1$ must be less than or equal to this value. If R1 is too large, it can become a significant fraction of the output impedance at pin 3 which degrades linearity. Also output ripple voltage must be considered and the size of C2 is affected by R1. An expression that describes the ripple content on pin 3 for a single R1C2 combination is:

$$V_{RIPPLE} = \frac{V_{CC}}{2} \times \frac{C1}{C2} \times \left(1 - \frac{V_{CC} \times f_{IN} \times C1}{I_2}\right) \text{ pk-pk}$$

It appears R1 can be chosen independent of ripple, however response time, or the time it takes V_{OUT} to stabilize at a new voltage increases as the size of C2 increases, so a compromise between ripple, response time, and linearity must be chosen carefully.

As a final consideration, the maximum attainable input frequency is determined by V_{CC}, C1 and I_2:

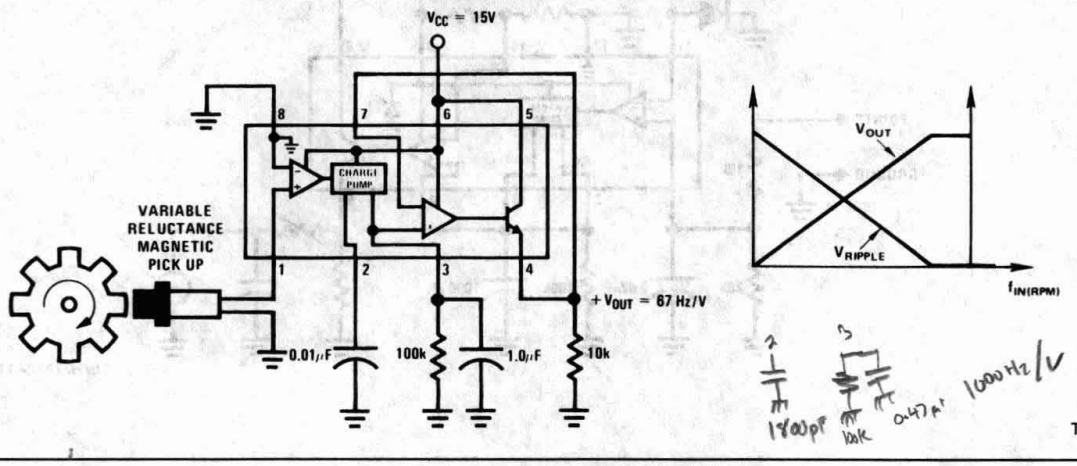
$$f_{MAX} = \frac{I_2}{C1 \times V_{CC}}$$

USING ZENER REGULATED OPTIONS (LM2917)

For those applications where an output voltage or current must be obtained independent of supply voltage variations, the LM2917 is offered. The most important consideration in choosing a dropping resistor from the unregulated supply to the device is that the tachometer and op amp circuitry alone require about 3 mA at the voltage level provided by the zener. At low supply voltages there must be some current flowing in the resistor above the 3 mA circuit current to operate the regulator. As an example, if the raw supply varies from 9V to 16V, a resistance of 470Ω will minimize the zener voltage variation to 160 mV. If the resistance goes under 400Ω or over 600Ω the zener variation quickly rises above 200 mV for the same input variation.

Typical Applications

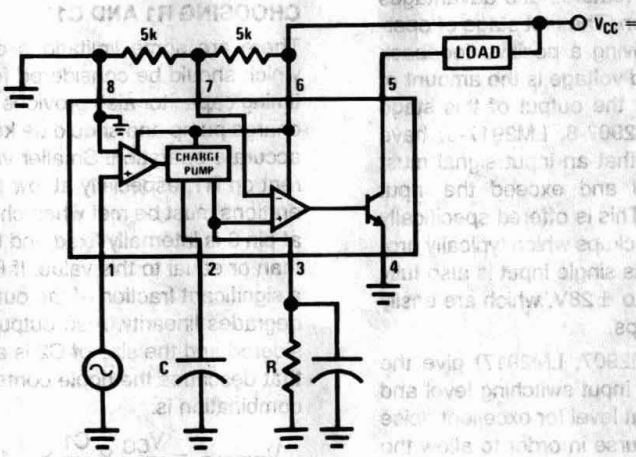
Minimum Component Tachometer



TL/H/7942–8

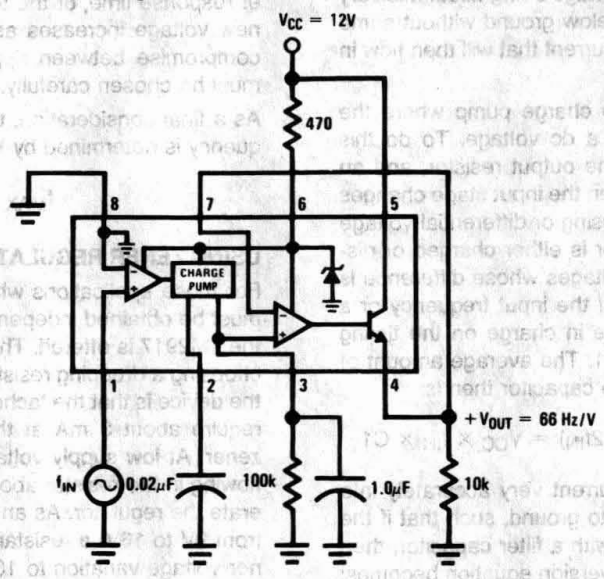
Typical Applications (Continued)

"Speed Switch" Load is Energized When $f_{IN} \geq \frac{1}{2RC}$



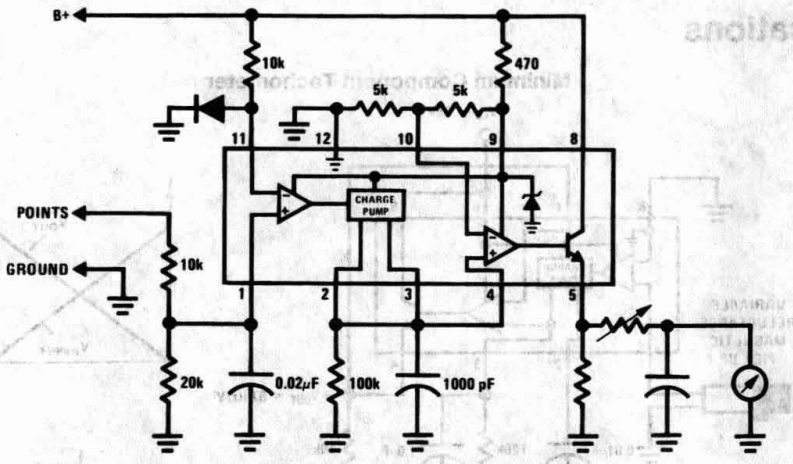
TL/H/7942–9

Zener Regulated Frequency to Voltage Converter



TL/H/7942–10

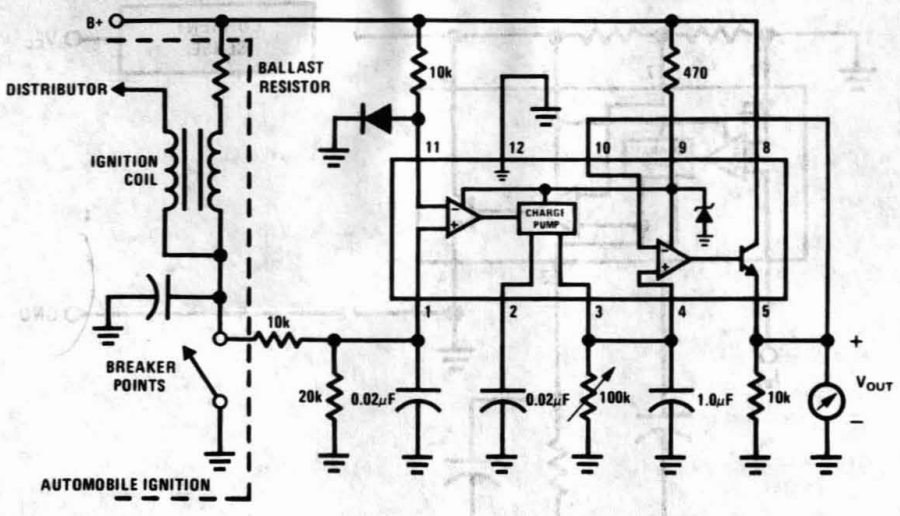
Breaker Point Dwell Meter



TL/H/7942–11

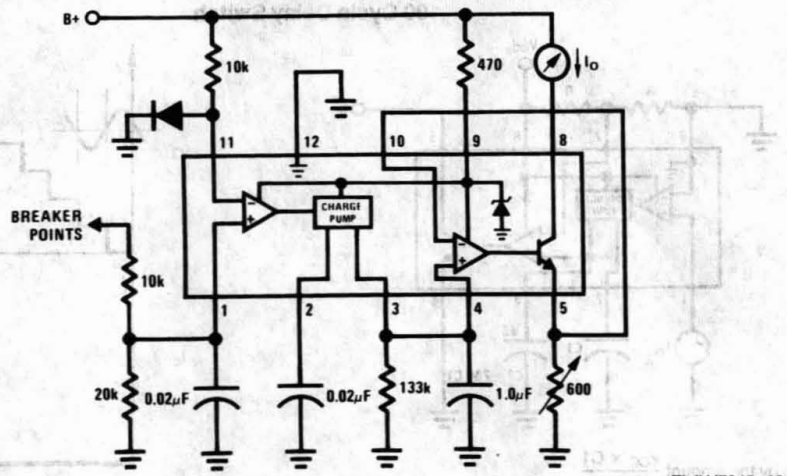
Typical Applications (Continued)

Voltage Driven Meter Indicating Engine RPM
V_O = 6V @ 400 Hz or 6000 ERPM (8 Cylinder Engine)



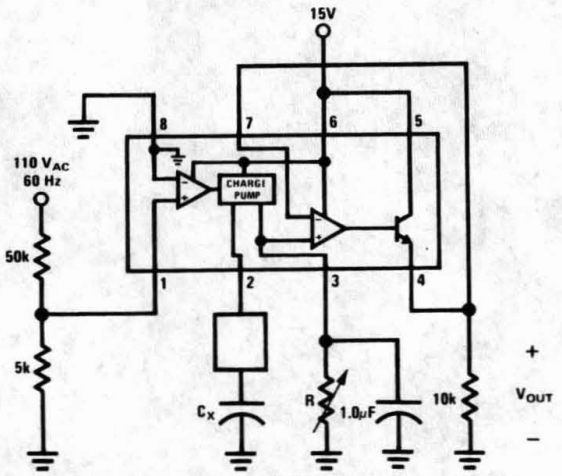
TL/H/7942–12

Current Driven Meter Indicating Engine RPM
I_O = 10 mA @ 300 Hz or 6000 ERPM (6 Cylinder Engine)



TL/H/7942–13

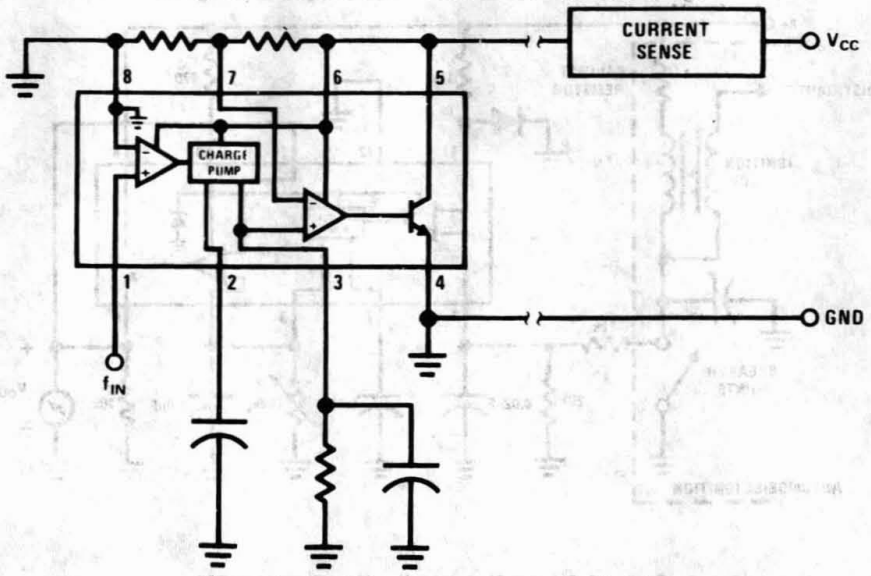
Capacitance Meter
V_{OUT} = 1V–10V for C_X = 0.01 to 0.1 mFd
(R = 111k)



TL/H/7942–14

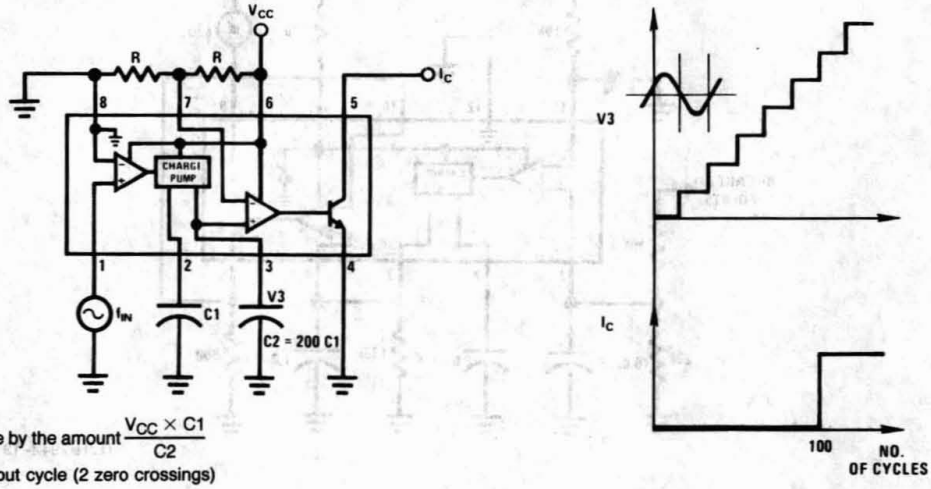
Typical Applications (Continued)

Two-Wire Remote Speed Switch



TL/H/7942–15

100 Cycle Delay Switch



TL/H/7942–16

V3 steps up in voltage by the amount $\frac{V_{CC} \times C1}{C2}$

for each complete input cycle (2 zero crossings)

Example:

If C2 = 200 C1 after 100 consecutive input cycles.

V3 = 1/2 V_{CC}

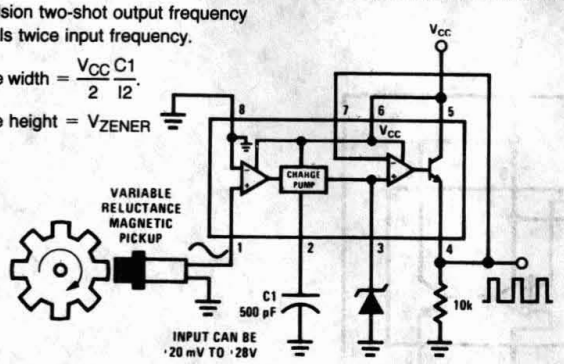
Typical Applications (Continued)

Variable Reluctance Magnetic Pickup Buffer Circuits

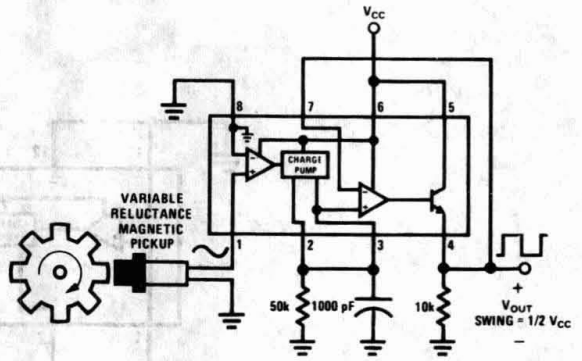
Precision two-shot output frequency equals twice input frequency.

Pulse width = $\frac{V_{CC}}{2}\frac{C1}{I2}$.

Pulse height = V_{ZENER}

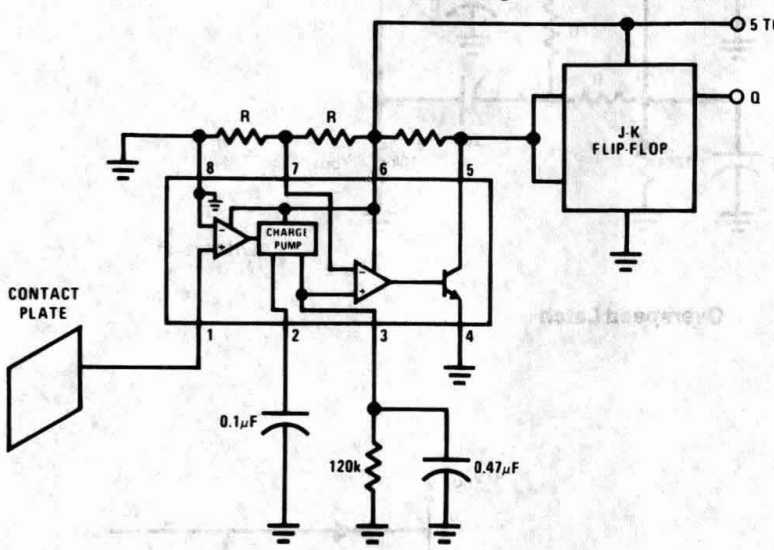


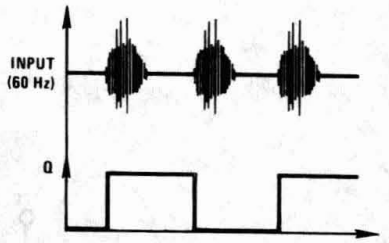
TL/H/7942–39



TL/H/7942–17

Finger Touch or Contact Switch

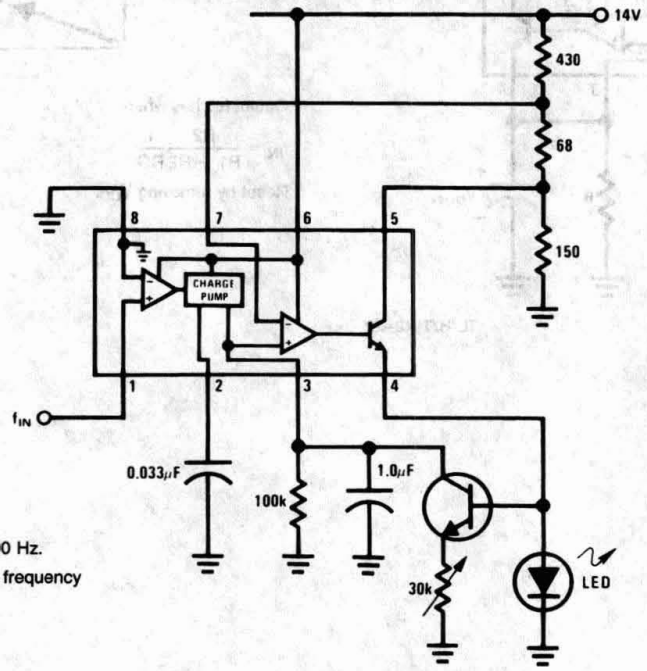




TL/H/7942–19

TL/H/7942–18

Flashing LED Indicates Overspeed



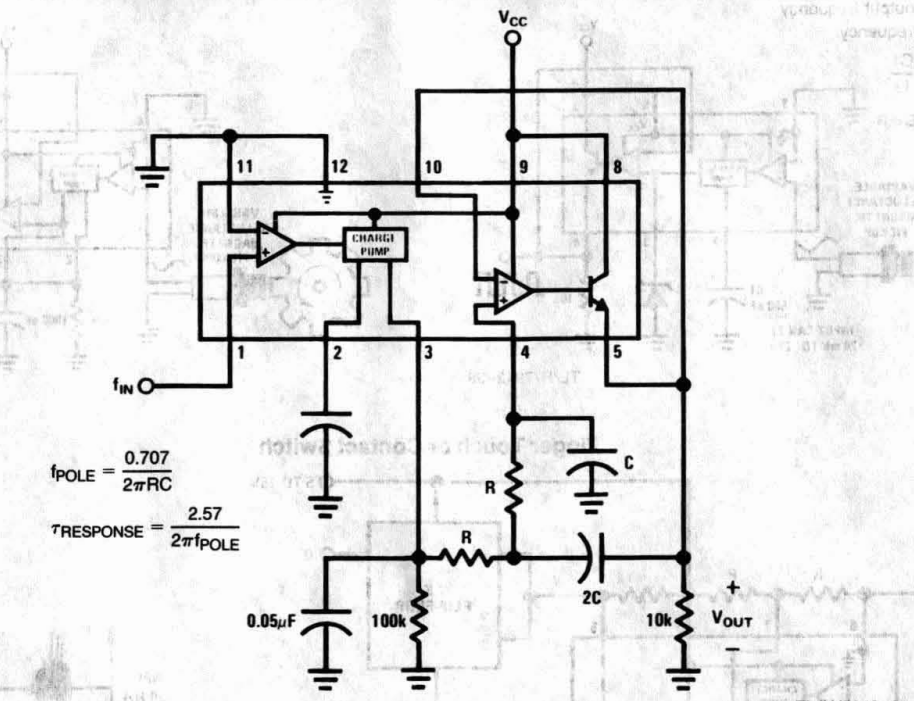
Flashing begins when $f_{IN} \geq 100$ Hz.

Flash rate increases with input frequency increase beyond trip point.

TL/H/7942–20

Typical Applications (Continued)

Frequency to Voltage Converter with 2 Pole Butterworth Filter to Reduce Ripple

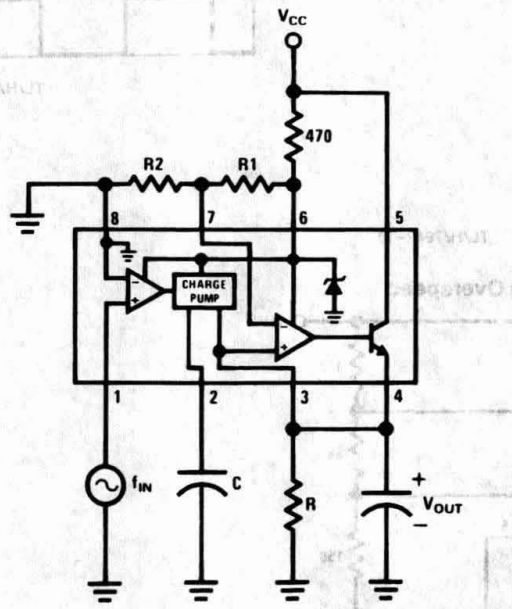


$$f_{POLE} = \frac{0.707}{2\pi RC}$$

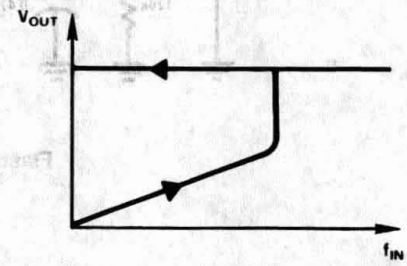
$$\tau_{RESPONSE} = \frac{2.57}{2\pi f_{POLE}}$$

TL/H/7942–21

Overspeed Latch



TL/H/7942–22



TL/H/7942–23

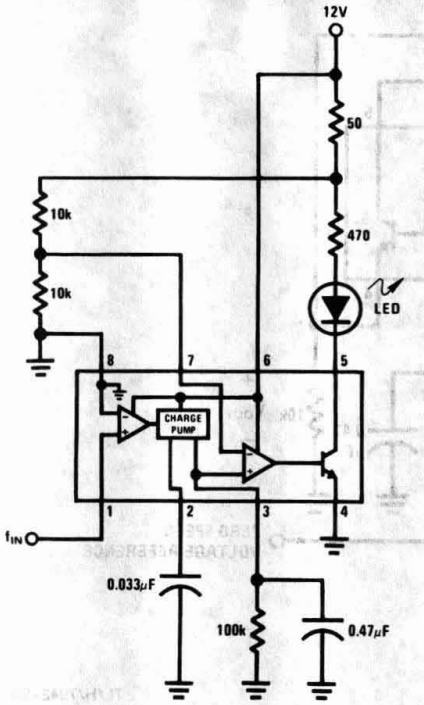
Output latches when

$$f_{IN} = \frac{R2}{R1 + R2}\frac{1}{RC}$$

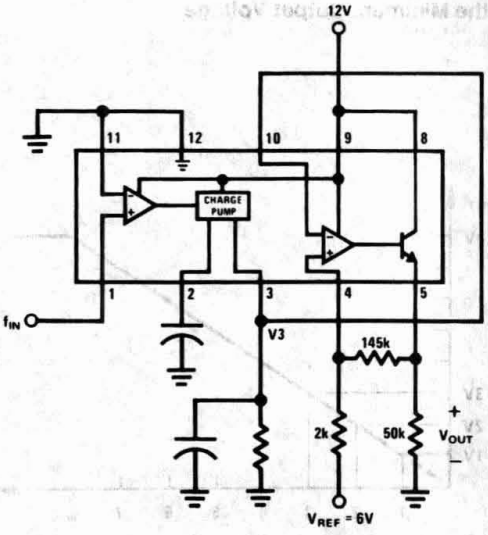
Reset by removing V_{CC}.

Typical Applications (Continued)

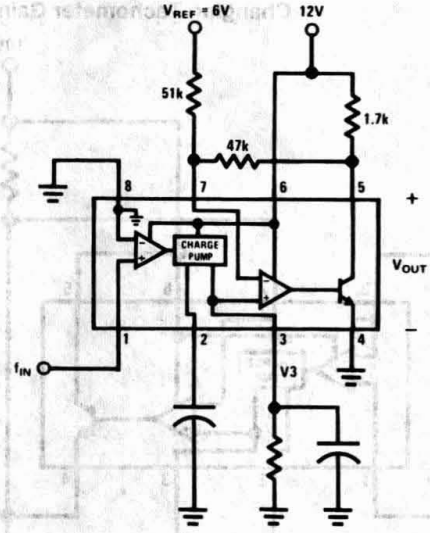
Some Frequency Switch Applications May Require Hysteresis in the Comparator Function Which can be Implemented in Several Ways:



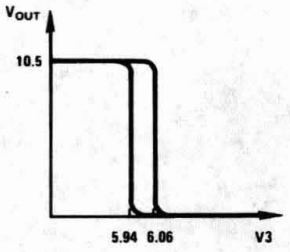
TL/H/7942–24



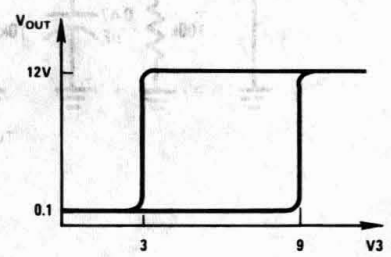
TL/H/7942–25



TL/H/7942–26



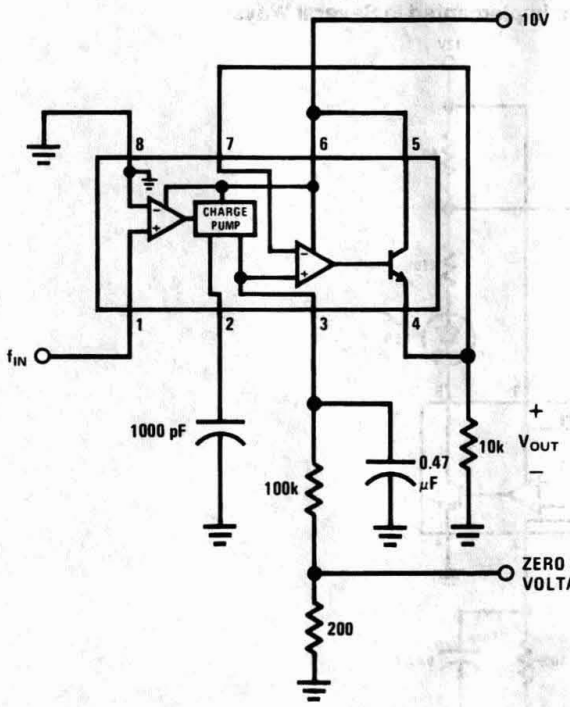
TL/H/7942–27

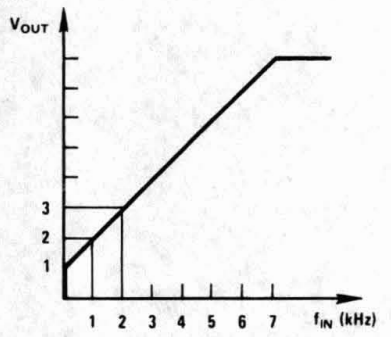


TL/H/7942–28

Typical Applications (Continued)

Changing the Output Voltage for an Input Frequency of Zero

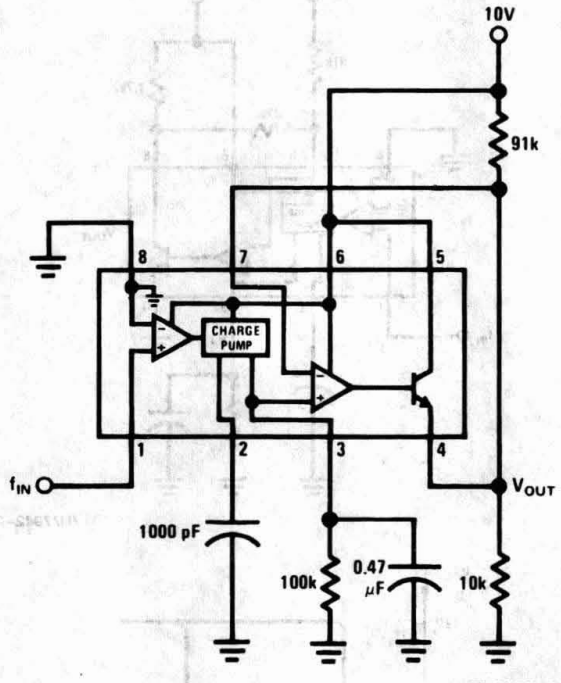


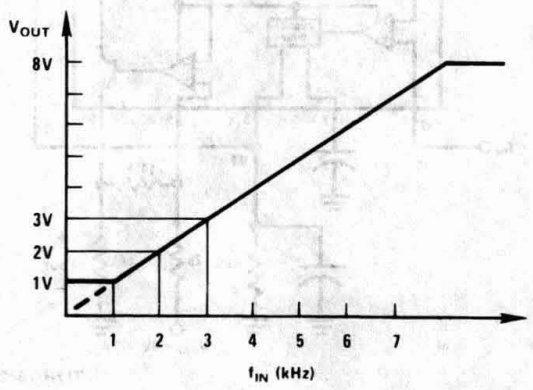


TL/H/7942–30

TL/H/7942–29

Changing Tachometer Gain Curve or Clamping the Minimum Output Voltage



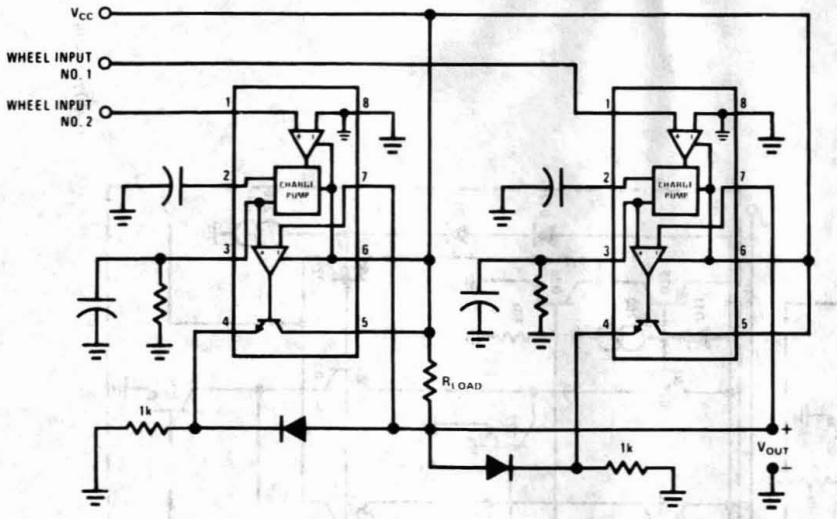


TL/H/7942–32

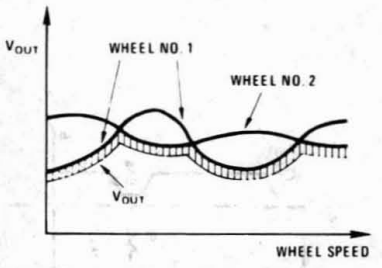
TL/H/7942–31

Anti-Skid Circuit Functions

"Select-Low" Circuit



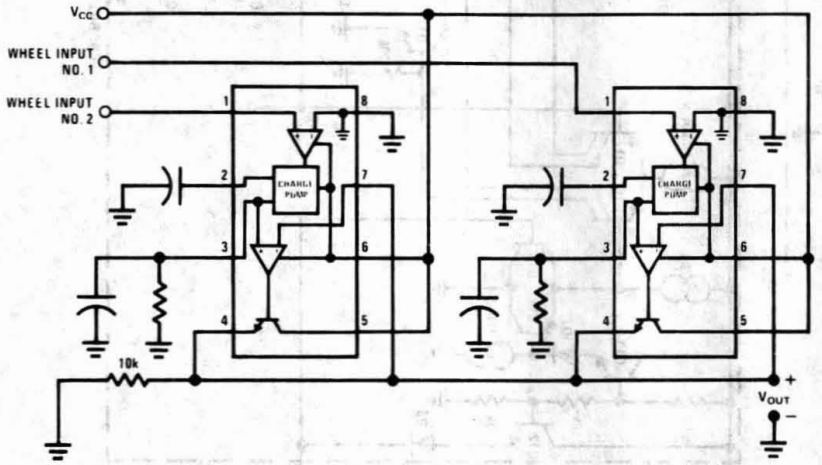
TL/H/7942–33



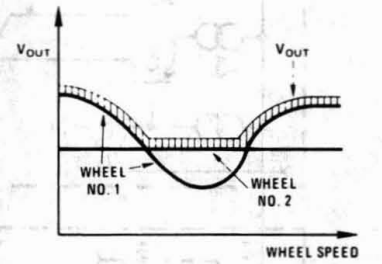
TL/H/7942–34

V_{OUT} is proportional to the lower of the two input wheel speeds.

"Select-High" Circuit



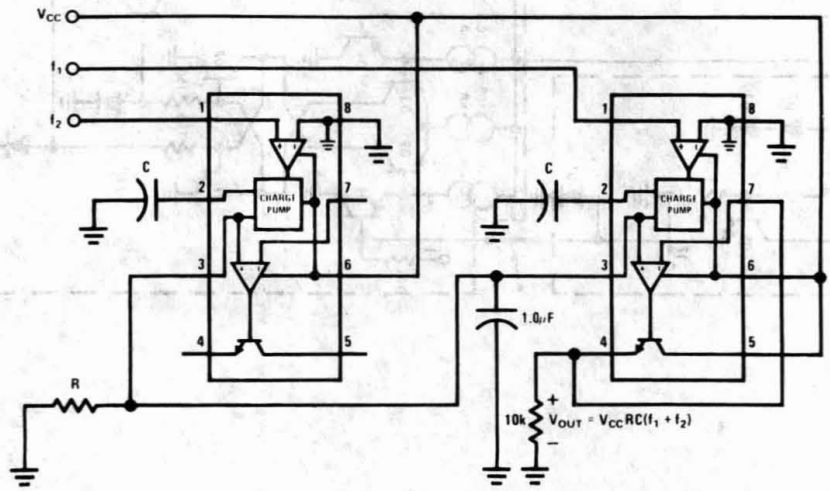
TL/H/7942–35



TL/H/7942–36

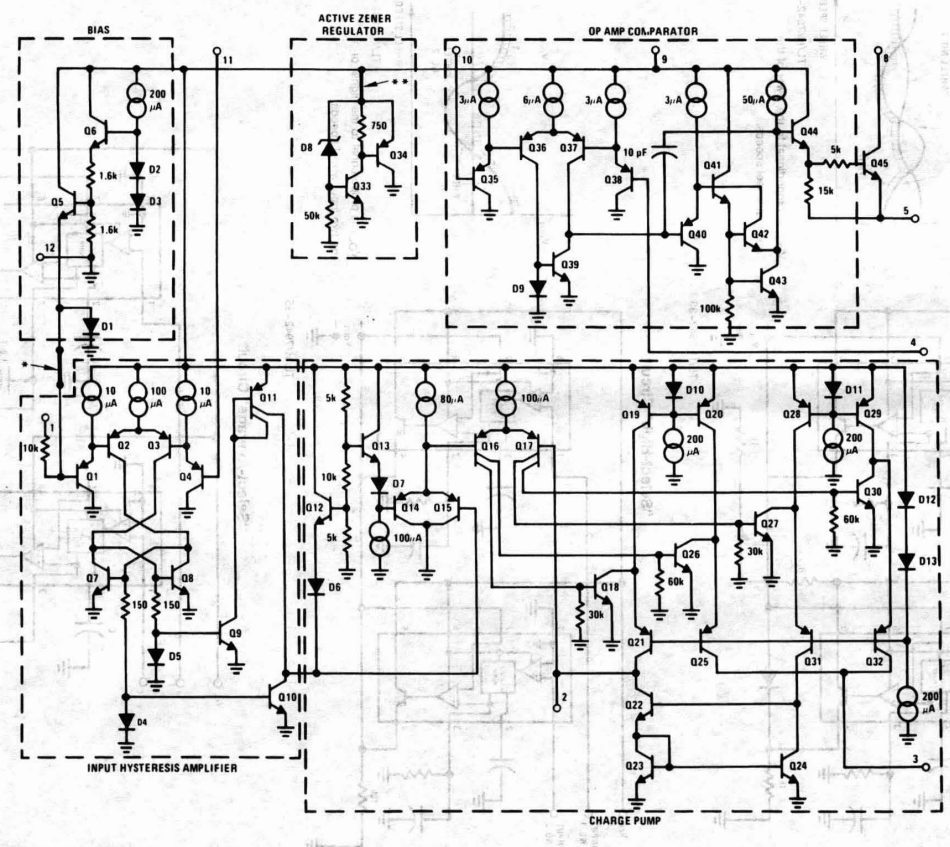
V_{OUT} is proportional to the higher of the two input wheel speeds.

"Select-Average" Circuit



TL/H/7942–37

Equivalent Schematic Diagram



TL/H/7942–38

*This connection made on LM2907-8 and LM2917-8 only.

**This connection made on LM2917 and LM2917-8 only.

Section 4
Special Functions

Section 4 Contents

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Display Drivers

MOS/LSI DISPLAY DRIVERS

National's comprehensive family of display drivers provides direct interface to all of the common display technologies—light-emitting diode (LED), liquid crystal display (LCD), and vacuum fluorescent (VF).

FUNCTION SIMILAR FAMILY

Each driver utilizes a simple serial-data input channel, on-chip shift register, latches and buffer/driver outputs. The serial input channel allows direct interface to most microprocessors, including COPS™, NSC800™, 8080 series, and TMS1000 series. Besides a serial-data input, each driver requires a clock input. Some offer a latch (data) input and/or data output for easy cascade interconnect of additional drivers.

Once loaded, the shift register data can be transferred to the on-chip latches, which then output to the buffer/driver and respective display. This buffer/driver is where each provides the unique driver interface desired by the particular display technology—LED, LCD, or VF.

THE MM58241 SERIES—VF

Each of the products in the MM58241 series provides high-voltage (several up to 60V) drive of VF displays. All are ideal for direct or multiplexed interface to large complex VF panel arrays or 5 × 7 (or larger) dot-matrix character strings. Each of the drivers are cascadable for further expansion. Application note AN-371 provides further details and other application information.

THE MM5450 SERIES—LED

National's MM5450 series of LED display drivers rounds out this comprehensive product family. This popular series offers direct drive of LED displays by providing up to 25 mA of current drive per LED segment.

CMOS/LSI

Many of the products in the display driver family utilize CMOS technology. Detailed features/functions of the 12-member display driver family are high-lighted in the following product guide.

In addition, National offers a line of bipolar segment and digit drivers with a broad range of output sink and source currents.

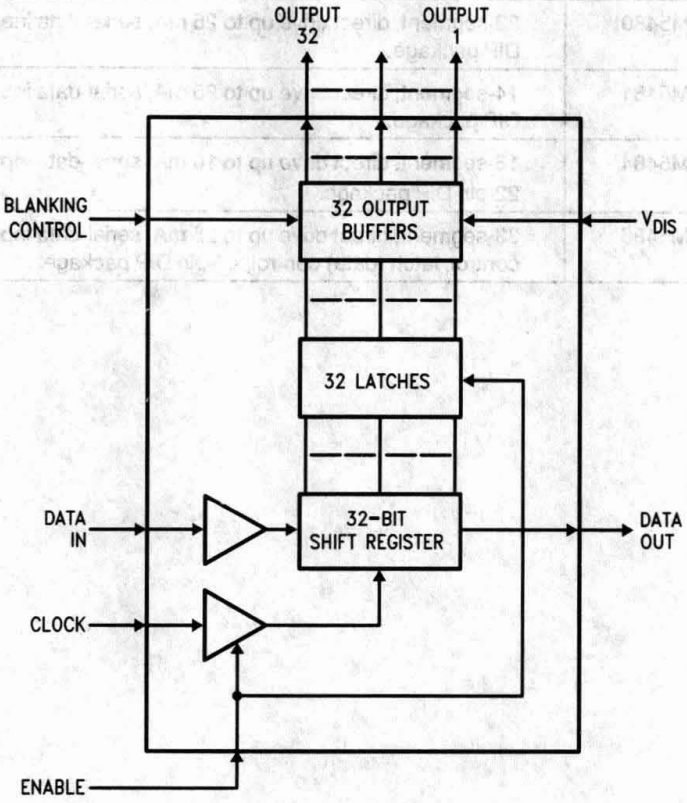

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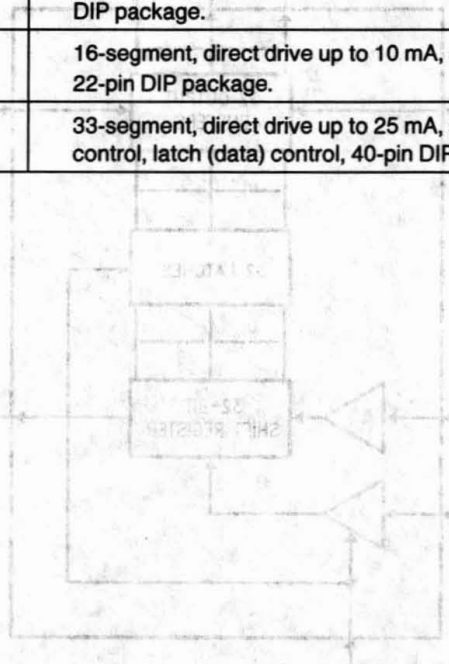
FIGURE 1. Typical Block Diagram

National Semiconductor

LSI Display Driver Selection Guide

Display Technology	Product Number	Features
Vacuum Fluorescent (VF)	MM58241	32-segment, direct/multiplexed drive to 60V, data enable, brightness control, cascadable, 40-pin DIP or 44-pin PCC package.
VF	MM58341	32-segment, direct/multiplexed drive to 35V, data enable, brightness control, cascadable, 40-pin DIP or 44-pin PCC package.
VF	MM58342	20-digit, direct/multiplexed drive to 35V, data enable, brightness control, cascadable, 28-pin DIP or PCC package.
Liquid Crystal (LCD)	MM5452	32-segment, direct drive, serial-data input, data enable, on-chip backplane (B/P) oscillator, 40-pin DIP or 44-pin PCC package.
LCD	MM5453	33-segment, direct drive, serial-data input, B/P oscillator, 40-pin DIP or 44-pin PCC package.
LCD	MM5483	31-segment, direct drive, serial-data input/output, latch (data) control, 40-pin DIP or 44-pin PCC package.
Light-Emitting Diode (LED)	MM5450	34-segment, direct drive up to 25 mA, brightness control, data enable, 40-pin DIP or 44-pin PCC package.
LED	MM5451	35-segment, direct drive up to 25 mA, brightness control, 40-pin DIP or 44-pin PCC package.
LED	MM5480	23-segment, direct drive up to 25 mA, serial-data input, brightness control, 28-pin DIP package.
LED	MM5481	14-segment, direct drive up to 25 mA, serial-data input, brightness control, 20-pin DIP package.
LED	MM5484	16-segment, direct drive up to 10 mA, serial-data input/output, cascadable, 22-pin DIP package.
LED	MM5486	33-segment, direct drive up to 25 mA, serial-data input/output, brightness control, latch (data) control, 40-pin DIP package.



National Semiconductor

Bipolar Display Driver Selection Guide

Product Number	Drivers/ Package	I_O/Digit (mA)		V_{MAX} (V)		Comments
		Sink (Common Anode)	Source (Common Cathode)	Input	Supply	
DS75491	4		50	10	10	
DS75494	6	150		10	10	Enable Control
DS75492	6	250		10	10	
LM3909	1	45	45	2.1	6.4	LED Flasher/Oscillator
LM3914	10	0	30*	35	25	Dot/Bar Driver Linear Scale
LM3915	10	0	30*	35	25	Dot/Bar Driver Log Scale
LM3916	10	0	30*	35	25	Dot/Bar Driver VU Meter Scale

*Per segment, use common external supply for anodes

National Semiconductor

DS0026 5 MHz Two Phase MOS Clock Driver

General Description

DS0026 is a low cost monolithic high speed two phase MOS clock driver and interface circuit. Unique circuit design provides both very high speed operation and the ability to drive large capacitive loads. The device accepts standard TTL outputs and converts them to MOS logic levels. The device may be driven from standard 54/74 series and 54S/74S series gates and flip-flops or from drivers such as the DS8830 or DM7440. The DS0026 is intended for applications in which the output pulse width is logically controlled; i.e., the output pulse width is equal to the input pulse width.

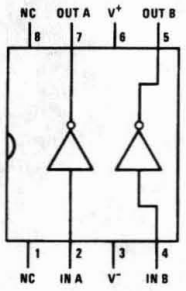
The DS0026 is designed to fulfill a wide variety of MOS interface requirements. As a MOS clock driver for long silicon-gate shift registers, a single device can drive over 10k bits at 5 MHz. Six devices provide input address and precharge drive for a 8k by 16-bit 1103 RAM memory system. Information on the correct usage of the DS0026 in these as well as other systems is included in the application note AN-76.

Features

- Fast rise and fall times—20 ns 1000 pF load
- High output swing—20V
- High output current drive—±1.5 amps
- TTL compatible inputs
- High rep rate—5 to 10 MHz depending on power dissipation
- Low power consumption in MOS "0" state—2 mW
- Drives to 0.4V of GND for RAM address drive

Connection Diagrams (Top Views)

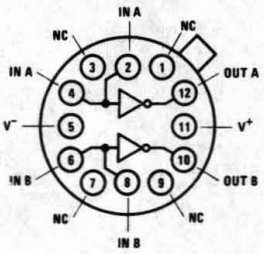
Dual-In-Line Package



TL/F/5853–2

Order Number DS0026CJ-8, DS0026CL or DS0026CN See NS Package Number J08A or N08E

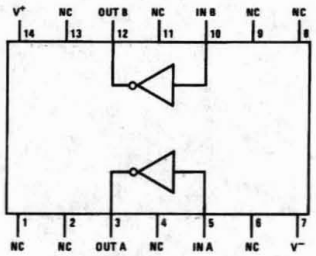
TO-8 Package



TL/F/5853–3

Order Number DS0026G or DS0026CG See NS Package Number G12B

Dual-In-Line Package



TL/F/5853–4

Order Number DS0026J or DS0026CJ See NS Package Number J14A

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

$V^+ - V^-$ Differential Voltage	22V
Input Current	100 mA
Input Voltage ($V_{IN} - V^-$)	5.5V
Peak Output Current	1.5A
Maximum Power Dissipation* at 25°C	
Cavity Package (8-Pin)	1150 mW
Cavity Package (14-Pin)	1380 mW
Molded Package	1040 mW
EIAJ SO Package	800 mW
Operating Temperature Range	
DS0026	−55°C to +125°C
DS0026C	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec.)	300°C

* Derate 8-pin cavity package 7.7 mW/°C above 25°C; derate 14-pin cavity package 9.3 mW/°C above 25°C; derate molded package 8.4 mW/°C above 25°C; derate metal can (TO-5) package 4.4 mW/°C above 25°C; derate EIAJ SO package 5.5 mW/°C above 25°C.

Electrical Characteristics (Notes 2 and 3)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
V_{IH}	Logic "1" Input Voltage	$V^- = 0V$		2	1.5		V
I_{IH}	Logic "1" Input Current	$V_{IN} - V^- = 2.4V$			10	15	mA
V_{IL}	Logic "0" Input Voltage	$V^- = 0V$			0.6	0.4	V
I_{IL}	Logic "0" Input Current	$V_{IN} - V^- = 0V$			−3	−10	μA
V_{OL}	Logic "1" Output Voltage	$V_{IN} - V^- = 2.4V$, $I_{OL} = 1$ mA			$V^- + 0.7$	$V^- + 1.0$	V
V_{OH}	Logic "0" Output Voltage	$V_{IN} - V^- = 0.4V$, $V_{SS} \geq V^+ + 1.0V$ $I_{OH} = -1$ mA		$V^+ - 1.0$	$V^+ - 0.8$		V
$I_{CC(ON)}$	"ON" Supply Current (one side on)	$V^+ - V^- = 20V$, $V_{IN} - V^- = 2.4V$			30	40	mA
$I_{CC(OFF)}$	"OFF" Supply Current	$V^+ - V^- = 20V$, $V_{IN} - V^- = 0V$	70°C		10	100	μA
			125°C		10	500	μA

Switching Characteristics (T_A = 25°C) (Notes 5 and 6)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
t_{ON}	Turn-On Delay	*(Figure 1)*		5	7.5	12	ns
		(Figure 2)			11		ns
t_{OFF}	Turn-Off Delay	*(Figure 1)*			12	15	ns
		(Figure 2)			13		ns
t_r	Rise Time	*(Figure 1)*, (Note 5)	C_L = 500 pF		15	18	ns
			C_L = 1000 pF		20	35	ns
		(Figure 2), (Note 5)	C_L = 500 pF		30	40	ns
			C_L = 1000 pF		36	50	ns
t_f	Fall Time	*(Figure 1)*, (Note 5)	C_L = 500 pF		12	16	ns
			C_L = 1000 pF		17	25	ns
		(Figure 2), (Note 5)	C_L = 500 pF		28	35	ns
			C_L = 1000 pF		31	40	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics provides conditions for actual device operation.

Note 2: These specifications apply for $V^+ - V^- = 10V$ to 20V, $C_L = 1000$ pF, over the temperature range of −55°C to +125°C for the DS0026, and 0°C to +70°C for the DS0026C.

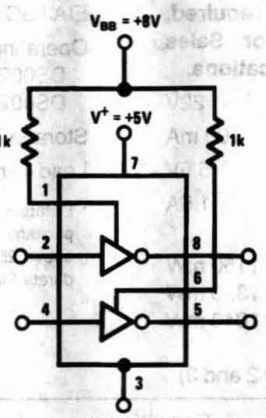
Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

Note 4: All typical values for T_A = 25°C.

Note 5: Rise and fall time are given for MOS logic levels; i.e., rise time is transition from logic "0" to logic "1" which is voltage fall.

Note 6: The high current transient (as high as 1.5A) through the resistance of the internal interconnecting V^- lead during the output transition from the high state to the low state can appear as negative feedback to the input. If the external interconnecting lead from the driving circuit to V^- is electrically long, or has significant dc resistance, it can subtract from the switching response.

Typical V_{BB} Connection



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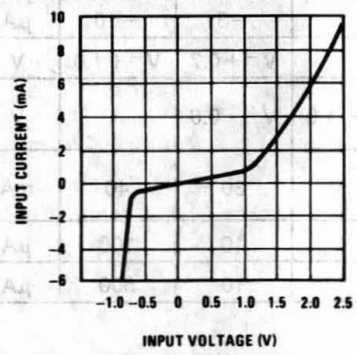
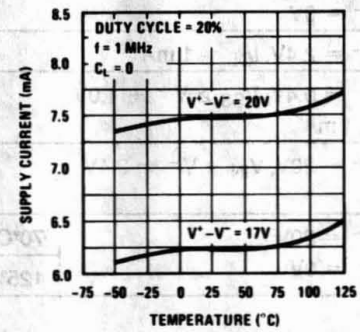
Typical Performance Characteristics

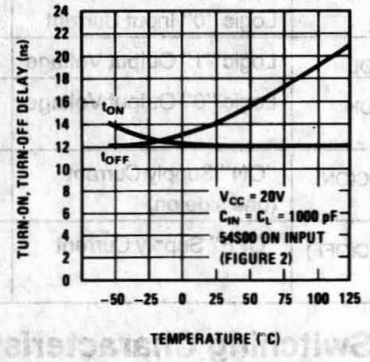
Input Current vs Input Voltage



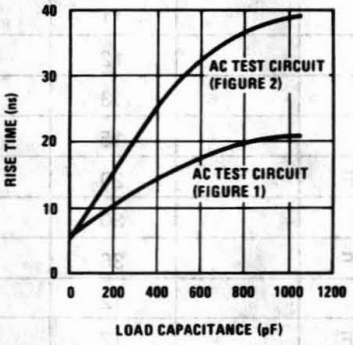
Supply Current vs Temperature



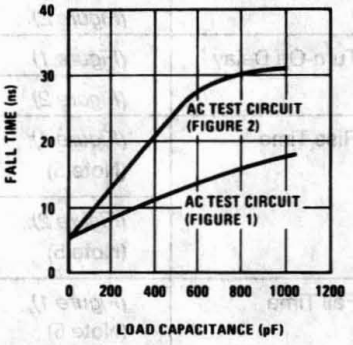
Turn-On and Turn-Off Delay vs Temperature



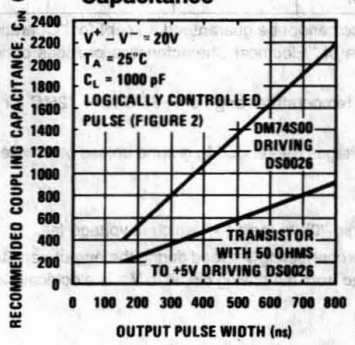
Rise Time vs Load Capacitance



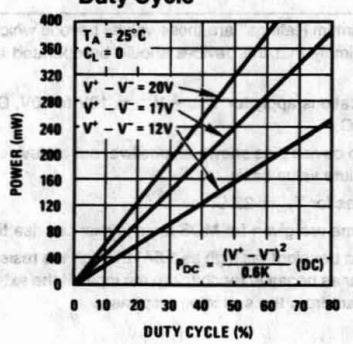
Fall Time vs Load Capacitance



Recommended Input Coding Capacitance



DC Power (P_{DC}) vs Duty Cycle



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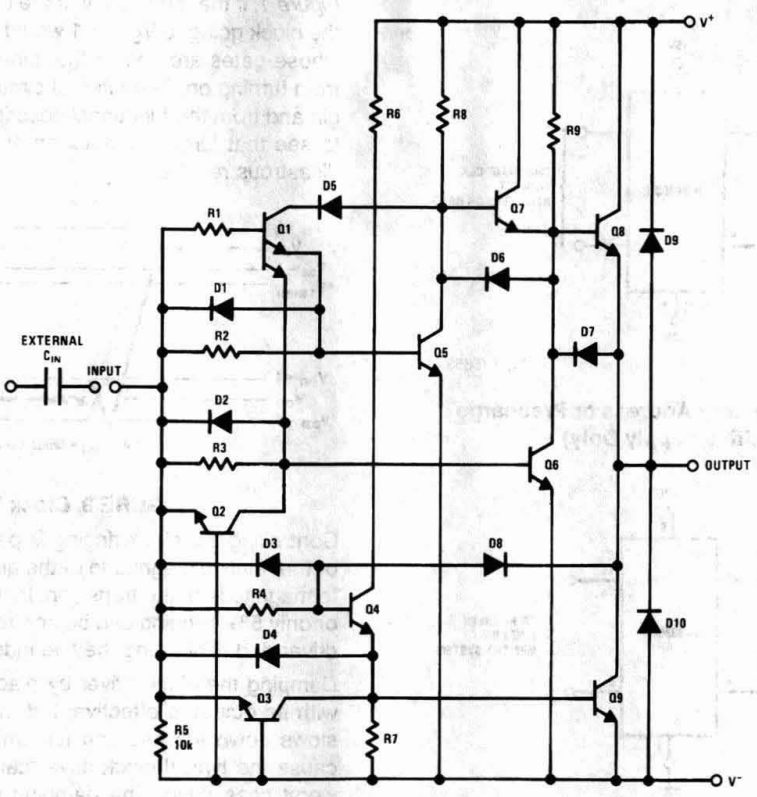
Schematic Diagram

1/2 DS0026



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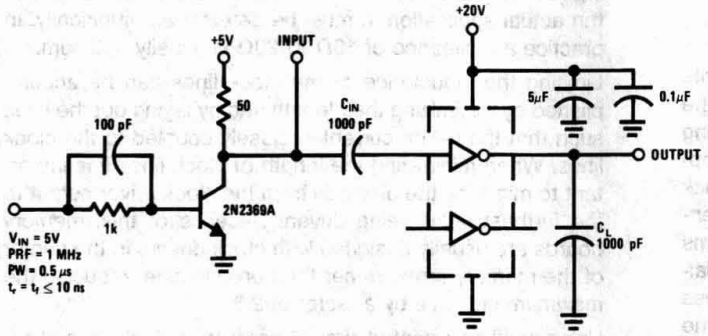
AC Test Circuits and Switching Time Waveforms



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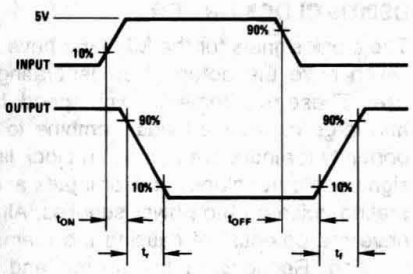
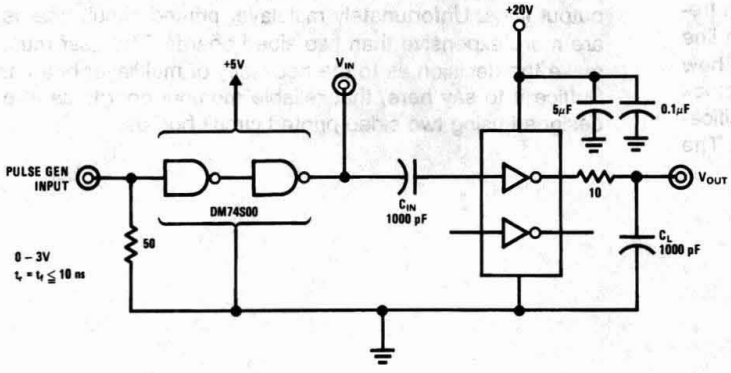
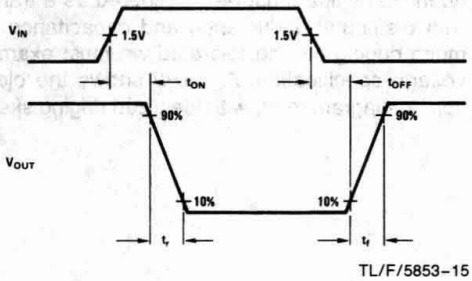


TL/F/5853–13

FIGURE 1



TL/F/5853–14

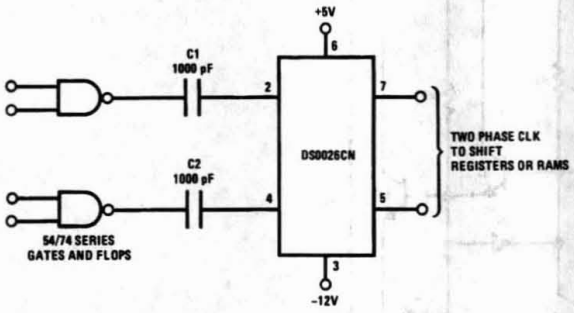


TL/F/5853–15

FIGURE 2

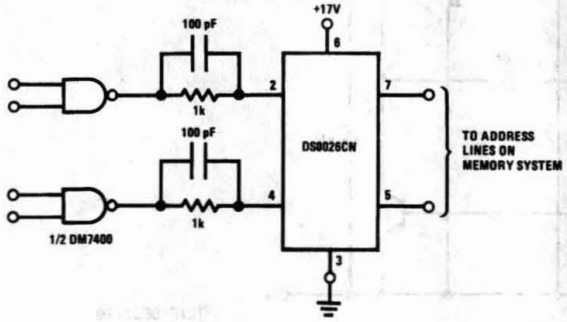
Typical Applications

AC Coupled MOS Clock Driver



TL/F/5853–16

DC Coupled RAM Memory Address or Precharge Driver (Positive Supply Only)



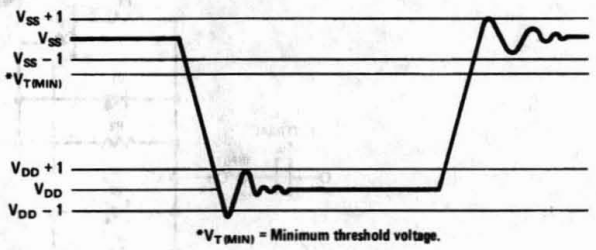
TL/F/5853–17

Application Hints

DRIVING THE MM5262 WITH THE DS0026 CLOCK DRIVER

The clock signals for the MM5262 have three requirements which have the potential of generating problems for the user. These requirements, high speed, large voltage swing and large capacitive loads, combine to provide ample opportunity for inductive ringing on clock lines, coupling clock signals to other clocks and/or inputs and outputs and generating noise on the power supplies. All of these problems have the potential of causing the memory system to malfunction. Recognizing the source and potential of these problems early in the design of a memory system is the most critical step. The object here is to point out the source of these problems and give a quantitative feel for their magnitude.

Line ringing comes from the fact that at a high enough frequency any line must be considered as a transmission line with distributed inductance and capacitance. To see how much ringing can be tolerated we must examine the clock voltage specification. *Figure 3* shows the clock specification, in diagram form, with idealized ringing sketched in. The ringing of the clock about the V_{SS} level is particularly critical. If the $V_{SS} - 1$ V_{OH} is not maintained, at *all* times, the information stored in the memory could be altered. Referring to *Figure 1*, if the threshold voltage of a transistor were −1.3V, the clock going to $V_{SS} - 1$ would mean that all the devices, whose gates are tied to that clock, would be only 300 mV from turning on. The internal circuitry needs this noise margin and from the functional description of the RAM it is easy to see that turning a clock on at the wrong time can have disastrous results.



TL/F/5853–18

FIGURE 3. Clock Waveform

Controlling the clock ringing is particularly difficult because of the relative magnitude of the allowable ringing, compared to magnitude of the transition. In this case it is 1V out of 20V or only 5%. Ringing can be controlled by damping the clock driver and minimizing the line inductance.

Damping the clock driver by placing a resistance in series with its output is effective, but there is a limit since it also slows down the rise and fall time of the clock signal. Because the typical clock driver can be much faster than the worst case driver, the damping resistor serves the useful function of limiting the minimum rise and fall time. This is very important because the faster the rise and fall times, the worse the ringing problem becomes. The size of the damping resistor varies because it is dependent on the details of the actual application. It must be determined empirically. In practice a resistance of 10Ω to 20Ω is usually optimum.

Limiting the inductance of the clock lines can be accomplished by minimizing their length and by laying out the lines such that the return current is closely coupled to the clock lines. When minimizing the length of clock lines it is important to minimize the distance from the clock driver output to the furthest point being driven. Because of this, memory boards are usually designed with clock drivers in the center of the memory array, rather than on one side, reducing the maximum distance by a factor of 2.

Using multilayer printed circuit boards with clock lines sandwiched between the V_{DD} and V_{SS} power plains minimizes the inductance of the clock lines. It also serves the function of preventing the clocks from coupling noise into input and output lines. Unfortunately multilayer printed circuit boards are more expensive than two sided boards. The user must make the decision as to the necessity of multilayer boards. Suffice it to say here, that reliable memory boards can be designed using two sided printed circuit boards.

Application Hints (Continued)

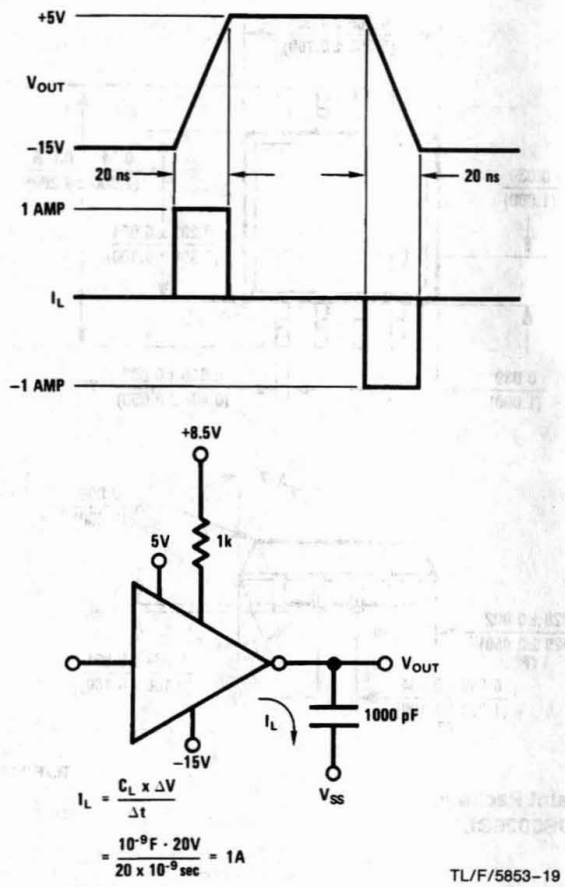


FIGURE 4. Clock Waveforms (Voltage and Current)

Because of the amount of current that the clock driver must supply to its capacitive load, the distribution of power to the clock driver must be considered. *Figure 4* gives the idealized voltage and current waveforms for a clock driver driving a 1000 pF capacitor with 20 ns rise and fall time.

As can be seen the current is significant. This current flows in the V_{DD} and V_{SS} power lines. Any significant inductance in the lines will produce large voltage transients on the power supplies. A bypass capacitor, as close as possible to the clock driver, is helpful in minimizing this problem. This bypass is most effective when connected between the V_{SS} and V_{DD} supplies. The size of the bypass capacitor depends on the amount of capacitance being driven. Using a low inductance capacitor, such as a ceramic or silver mica, is most effective. Another helpful technique is to run the V_{DD} and V_{SS} lines, to the clock driver, adjacent to each other. This tends to reduce the lines inductance and therefore the magnitude of the voltage transients.

While discussing the clock driver, it should be pointed out that the DS0026 is a relatively low input impedance device. It is possible to couple current noise into the input without seeing a significant voltage. Since the noise is difficult to detect with an oscilloscope it is often overlooked.

Lastly, the clock lines must be considered as noise generators. *Figure 5* shows a clock coupled through a parasitic coupling capacitor, C_C, to eight data input lines being driven by a 7404. A parasitic lumped line inductance, L, is also shown. Let us assume, for the sake of argument, that C_C is 1 pF and that the rise time of the clock is high enough to completely isolate the clock transient from the 7404 because of the inductance, L.

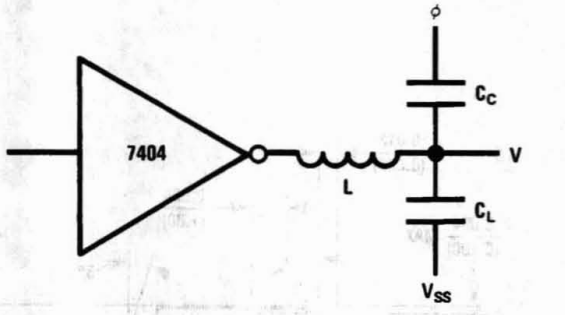


FIGURE 5. Clock Coupling

With a clock transition of 20V the magnitude of the voltage generated across C_L is:

$$V = 20V \times \frac{C_C}{C_L + C_C} = 20V \times \left(\frac{1}{56+1}\right) = 0.35V$$

This has been a hypothetical example to emphasize that with 20V low rise/fall time transitions, parasitic elements can not be neglected. In this example, 1 pF of parasitic capacitance could cause system malfunction, because a 7404 without a pull up resistor has typically only 0.3V of noise margin in the "1" state at 25°C. Of course it is stretching things to assume that the inductance, L, completely isolates the clock transient from the 7404. However, it does point out the need to minimize inductance in input/output as well as clock lines.

The output is current, so it is more meaningful to examine the current that is coupled through a 1 pF parasitic capacitance. The current would be:

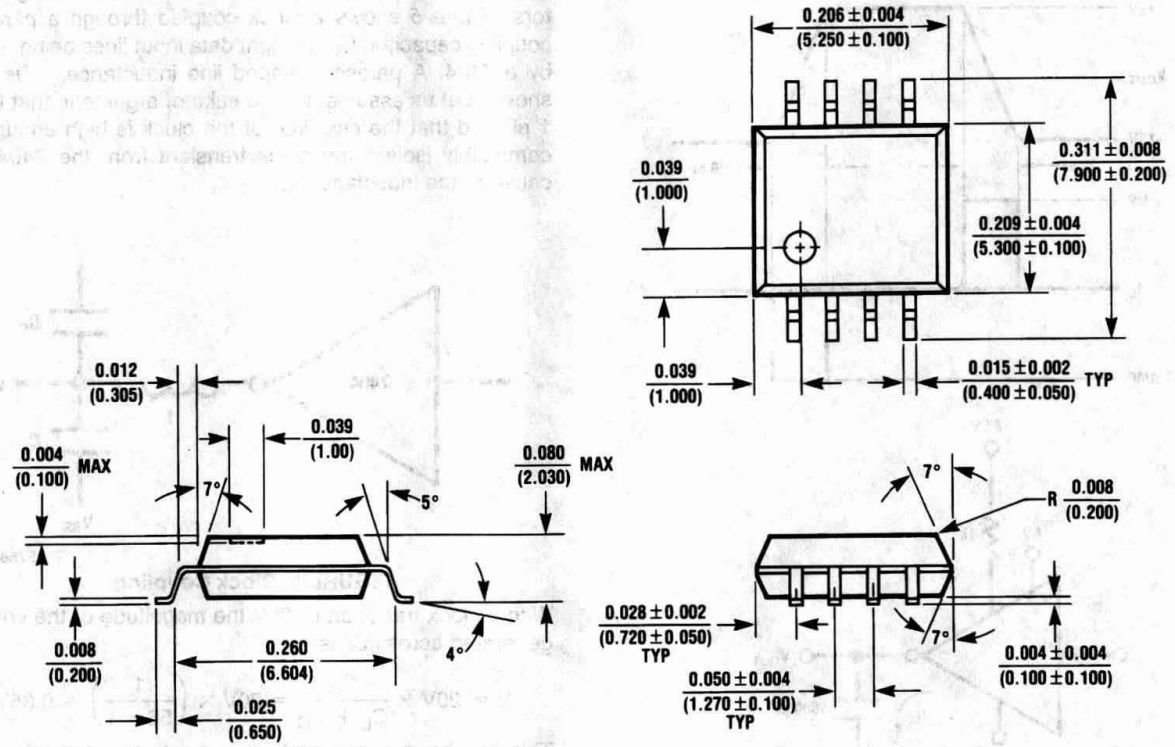
$$I = C_C \times \frac{\Delta V}{\Delta t} = \frac{1 \times 10^{-12} \times 20}{20 \times 10^{-9}} = 1\ mA$$

This exceeds the total output current swing so it is obviously significant.

Clock coupling to inputs and outputs can be minimized by using multilayer printed circuit boards, as mentioned previously, physically isolating clock lines and/or running clock lines at right angles to input/output lines. All of these techniques tend to minimize parasitic coupling capacitance from the clocks to the signals in question.

In considering clock coupling it is also important to have a detailed knowledge of the functional characteristics of the device being used. As an example, for the MM5262, coupling noise from the $\phi 2$ clock to the address lines is of no particular consequence. On the other hand the address inputs will be sensitive to noise coupled from $\phi 1$ clock.

Packaging Information



TL/F/5853–21

8-Lead Surface Mount Package
Order Number DS0026CL

National Semiconductor

DS75491 MOS-to-LED Quad Segment Driver
DS75492 MOS-to-LED Hex Digit Driver

General Description

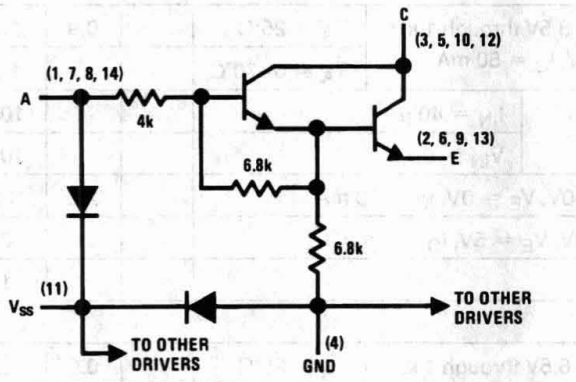
The DS75491 and DS75492 are interface circuits designed to be used in conjunction with MOS integrated circuits and common-cathode LEDs in serially addressed multi-digit displays. The number of drivers required for this time-multiplexed system is minimized as a result of the segment-address-and-digit-scan method of LED drive.

Features

- 50 mA source or sink capability per driver (DS75491)
- 250 mA sink capability per driver (DS75492)
- MOS compatability (low input current)
- Low standby power
- High-gain Darlington circuits

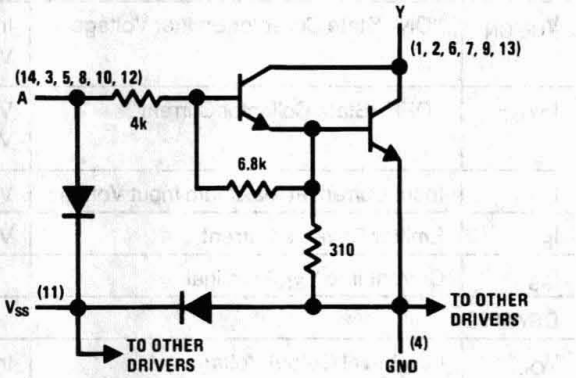
Schematic and Connection Diagrams

DS75491 (each driver)



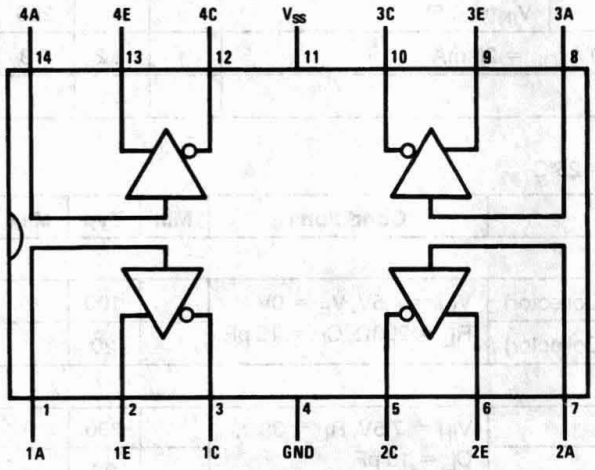
TL/F/5830–1

DS75492 (each driver)



TL/F/5830–2

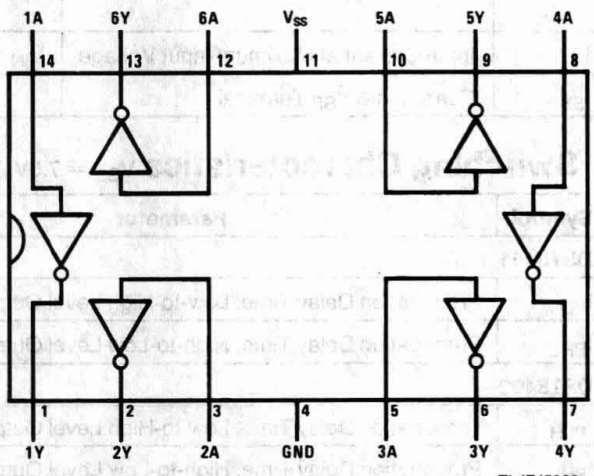
DS75491 Dual-In-Line Package



TL/F/5830–3

Top View

DS75492 Dual-In-Line Package



TL/F/5830–4

Top View

Order Number DS75491N, DS75492M or DS75492N
See NS Package Number M14A or N14A

4

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

	DS75491	DS75492
Input Voltage Range (Note 4)	−5V to V_{SS}	
Collector Output Voltage (Note 5)	10V	10V
Collector Output to Input Voltage	10V	10V
Emitter to Ground Voltage ($V_I \geq 5V$)	10V	
Emitter to Input Voltage	5V	
Voltage at V_{SS} Terminal with Respect to any Other Device Terminal	10V	10V
Collector Output Current		
Each Collector Output	50 mA	250 mA
All Collector Outputs	200 mA	600 mA

	DS75491	DS75492
Continuous Total Dissipation	600 mW	600 mW
Operating Temperature Range	0°C to +70°C	
Storage Temperature Range	−65°C to +150°C	
Lead Temp. (Soldering, 10 sec)	300°C	300°C
Maximum Power Dissipation at 25°C		
Molded Package	1207 mW*	1280 mW†

*Derate molded package 9.66 mW/°C above 25°C.

†Derate molded package 10.24 mW/°C above 25°C.

Electrical Characteristics V_{SS} = 10V (Notes 2 and 3)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
DS75491							
$V_{CE\ ON}$	"ON" State Collector Emitter Voltage	Input = 8.5V through 1 kΩ, V_E = 5V, I_C = 50 mA	T_A = 25°C		0.9	1.2	V
			T_A = 0–70°C			1.5	V
$I_{C\ OFF}$	"OFF" State Collector Current	V_C = 10V, V_E = 0V	I_{IN} = 40 μA			100	μA
			V_{IN} = 0.7V			100	μA
I_I	Input Current at Maximum Input Voltage	V_{IN} = 10V, V_E = 0V, I_C = 20 mA			2.2	3.3	mA
I_E	Emitter Reverse Current	V_{IN} = 0V, V_E = 5V, I_C = 0 mA				100	μA
I_{SS}	Current Into V_{SS} Terminal					1	mA
DS75492							
V_{OL}	Low Level Output Voltage	Input = 6.5V through 1 kΩ, I_{OUT} = 250 mA	T_A = 25°C		0.9	1.2	V
			T_A = 0–70°C			1.5	V
I_{OH}	High Level Output Current	V_{OH} = 10V	I_{IN} = 40 μA			200	μA
			V_{IN} = 0.5V			200	μA
I_I	Input Current at Maximum Input Voltage	V_{IN} = 10V, I_{OL} = 20 mA			2.2	3.3	mA
I_{SS}	Current Into V_{SS} Terminal					1	mA

Switching Characteristics V_{SS} = 7.5V, T_A = 25°C

Symbol	Parameter	Conditions	Min	Typ	Max	Units
DS75491						
t_{PLH}	Propagation Delay Time, Low-to-High Level Output (Collector)	V_{IH} = 4.5V, V_E = 0V, R_L = 200Ω, C_L = 15 pF		100		ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output (Collector)			20		ns
DS75492						
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	V_{IH} = 7.5V, R_L = 39Ω, C_L = 15 pF		300		ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output			30		ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the 0°C to +70°C temperature range for the DS75491 and DS75492.

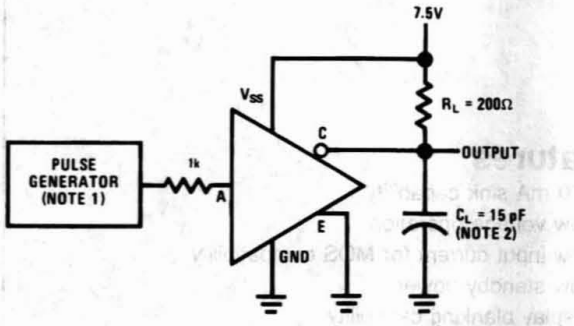
Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

Note 4: The input is the only device terminal which may be negative with respect to ground.

Note 5: Voltage values are with respect to network ground terminal unless otherwise noted.

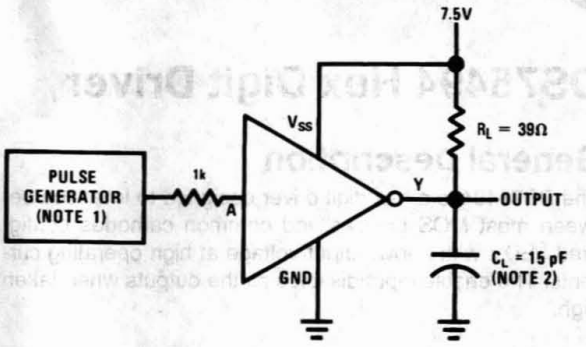
AC Test Circuits and Switching Time Waveforms

DS75491

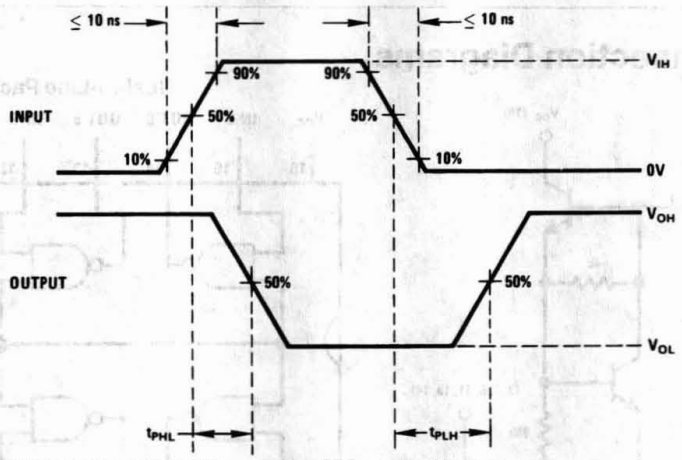


TL/F/5830–5

DS75492



TL/F/5830–6



TL/F/5830–7

Note 1: The pulse generator has the following characteristics: Z_{OUT} = 50Ω, PRR = 100 kHz, t_W = 1 μs.

Note 2: C_L includes probe and jig capacitance.

National Semiconductor

DS75494 Hex Digit Driver

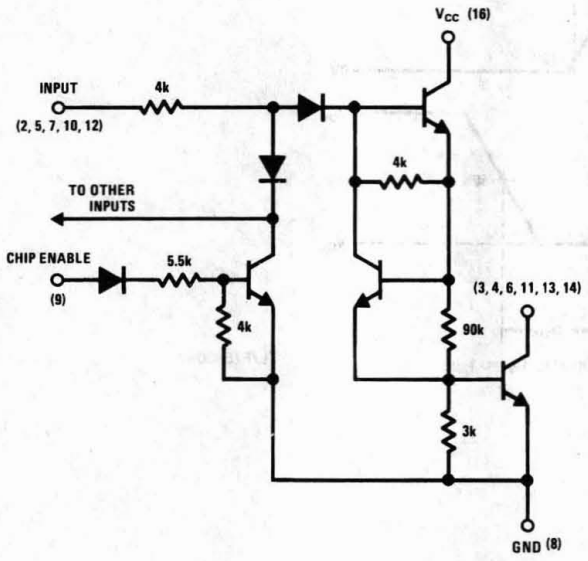
General Description

The DS75494 is a hex digit driver designed to interface between most MOS devices and common cathodes configured LED's with a low output voltage at high operating currents. The enable input disables all the outputs when taken high.

Features

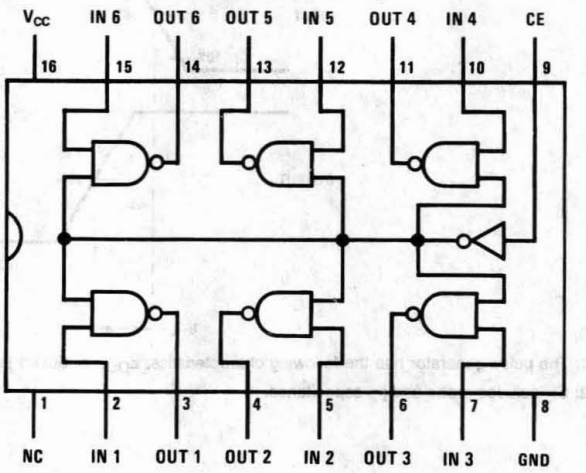
- 150 mA sink capability
- Low voltage operation
- Low input current for MOS compatibility
- Low standby power
- Display blanking capability
- Low voltage saturating outputs
- Hex high gain circuits

Schematic and Connection Diagrams



TL/F/5832–1

Dual-In-Line Package



TL/F/5832–2

Top View

Order Number DS75494N
See NS Package Number N16A

Truth Table

Enable	V_{IN}	V_{OUT}
0	0	1
0	1	0
1	X	1

X = don't care

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	10V
Input Voltage	10V
Output Voltage	10V
Storage Temperature Range	−65°C to +150°C
Maximum Power Dissipation* at 25°C	
Cavity Package	1433 mW
Molded Package	1362 mW
Lead Temperature (Soldering 4 seconds)	260°C

*Derate molded package 10.9 mW/°C above 25°C.

Operating Conditions

	Min	Max	Units
Supply Voltage, V_{CC}	3.2	8.8	V
Temperature, T_A			
DS75494	0	+70	°C

Electrical Characteristics (Notes 2 and 3)

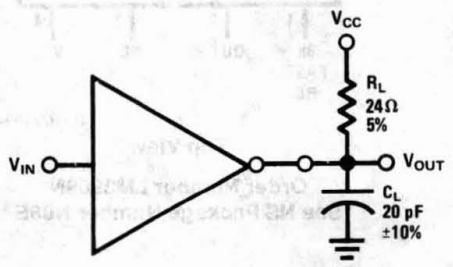
Symbol	Parameter	Conditions			Min	Typ	Max	Units
I_{IH}	Logical "1" Input Current	V_{CC} = Min, V_{IN} = 8.8V	V_{CE} = 8.8V through 100k				2.0	mA
			V_{CE} = 8.8V				2.7	mA
I_{IL}	Logical "0" Input Current	V_{CC} = Max, V_{IN} = −5.5V					−20	μA
I_{OH}	Logical "1" Output Current	V_{CC} = Max, V_{OH} = 8.8V	V_{IN} = 8.8V through 100k, V_{CE} = 0V				400	μA
			V_{IN} = 8.8V, V_{CE} = 6.5V through 1.0k				400	μA
V_{OL}	Logical "0" Output Voltage	V_{CC} = Min, I_{OL} = 150 mA, V_{IN} = 6.5V through 1.0k, V_{CE} = 8.8V through 100k		DS75494		0.25	0.35	V
I_{CC}	Supply Currents	V_{CC} = Max	One Driver "ON", V_{IN} = 8.8V	DS75474			8.0	mA
			All Other Pins to GND	V_{CE} = 6.5V through 1.0k			100	μA
				V_{IN} = 8.8V through 100k			100	μA
			All Other Pins to GND				40	μA
t_{OFF}	Output "OFF" Time	C_L = 20 pF, R_L = 24Ω, V_{CC} = 4.0V, See AC Test Circuits				0.04	1.2	μs
t_{ON}	Output "ON" Time	C_L = 20 pF, R_L = 24Ω, V_{CC} = 4.0V, See AC Test Circuits				13	100	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

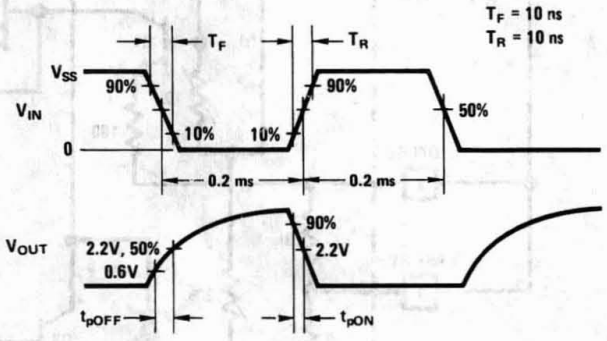
Note 2: Unless otherwise specified min/max limits apply across the 0°C to +70°C range for the DS75494.

Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

AC Test Circuit and Switching Time Waveforms



TL/F/5832–3



TL/F/5832–4

National Semiconductor

LM3909 LED Flasher/Oscillator

General Description

The LM3909 is a monolithic oscillator specifically designed to flash Light Emitting Diodes. By using the timing capacitor for voltage boost, it delivers pulses of 2 or more volts to the LED while operating on a supply of 1.5V or less. The circuit is inherently self-starting, and requires addition of only a battery and capacitor to function as an LED flasher.

Packaged in an 8-lead plastic mini-DIP, the LM3909 will operate over the extended consumer temperature range of −25°C to +70°C. It has been optimized for low power drain and operation from weak batteries so that continuous operation life exceeds that expected from battery rating.

Application is made simple by inclusion of internal timing resistors and an internal LED current limit resistor. As shown in the first two application circuits, the timing resistors supplied are optimized for nominal flashing rates and minimum power drain at 1.5V and 3V.

Timing capacitors will generally be of the electrolytic type, and a small 3V rated part will be suitable for any LED flasher using a supply up to 6V. However, when picking flash rates, it should be remembered that some electrolytics have very broad capacitance tolerances, for example −20% to +100%.

Features

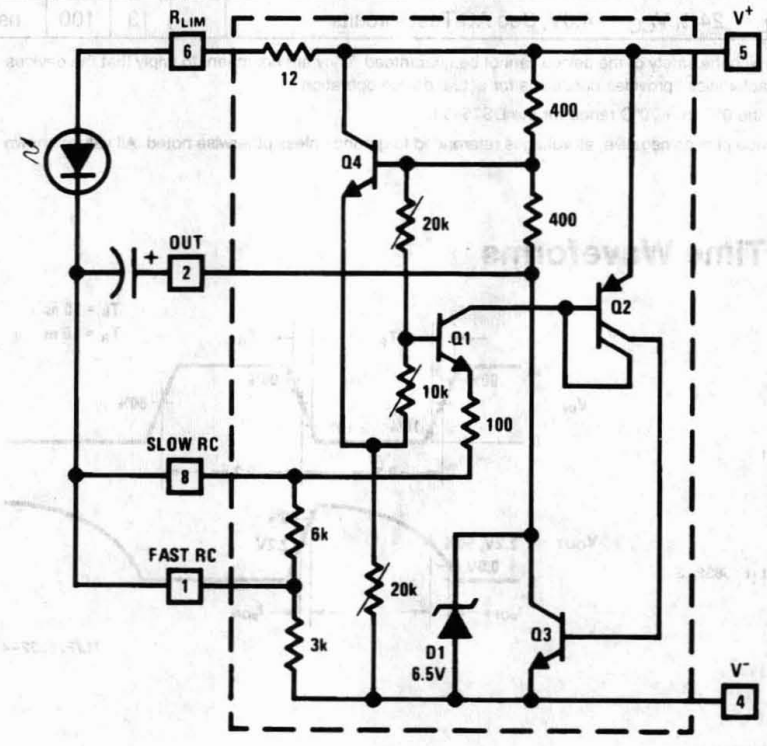
- Operation over one year from one C size flashlight cell
- Bright, high current LED pulse
- Minimum external parts
- Low cost
- Low voltage operation, from just over 1V to 5V
- Low current drain, averages under 0.5 mA during battery life
- Powerful; as an oscillator directly drives an 8Ω speaker
- Wide temperature range

Applications

- Finding flashlights in the dark, or locating boat mooring floats
- Sales and advertising gimmicks
- Emergency locators, for instance on fire extinguishers
- Toys and novelties
- Electronic applications such as trigger and sawtooth generators
- Siren for toy fire engine, (combined oscillator, speaker driver)
- Warning indicators powered by 1.4V to 200V

Schematic Diagram

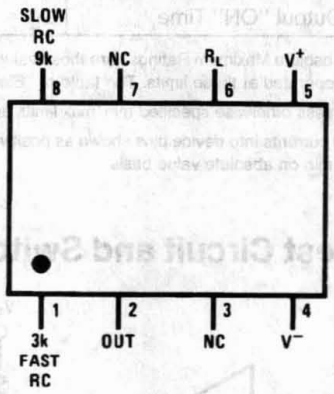
Typical 1.5V Flasher



TL/H/7969–1

Connection Diagram

Dual-In-Line Package



TL/H/7969–2

Top View

Order Number LM3909N
See NS Package Number N08E

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

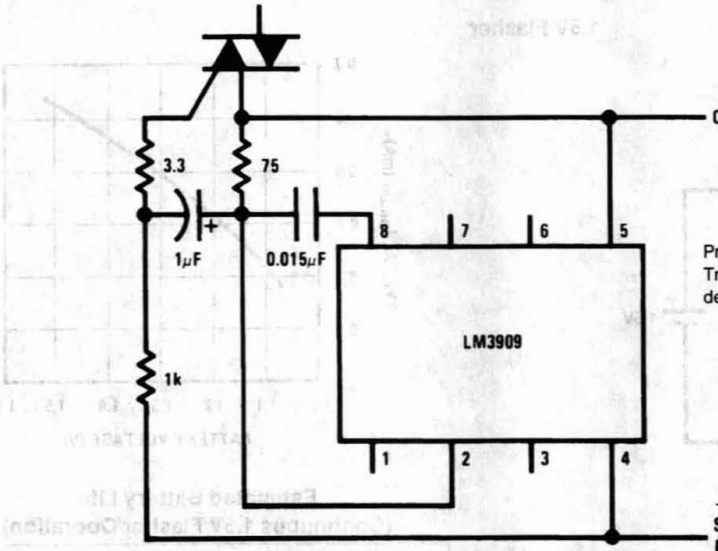
Power Dissipation	500 mW
V^+ Voltage	6.4V
Operating Temperature Range	−25°C to +70°C
Lead Temperature (Soldering, 10 sec.)	260°C

Electrical Characteristics

Parameter	Conditions (Applications Note 3)	Min	Typ	Max	Units
Supply Voltage	(In Oscillation)	1.15		6.0	V
Operating Current			0.55	0.75	mA
Flash Frequency	300 μF, 5% Capacitor	0.65	1.0	1.3	Hz
High Flash Frequency	0.30 μF, 5% Capacitor		1.1		kHz
Compatible LED Forward Drop	1 mA Forward Current	1.35		2.1	V
Peak LED Current	350 μF Capacitor		45		mA
Pulse Width	350 μF Capacitors at ½ Amplitude		6.0		ms

Typical Applications (See applications notes on following page)

Triac Trigger

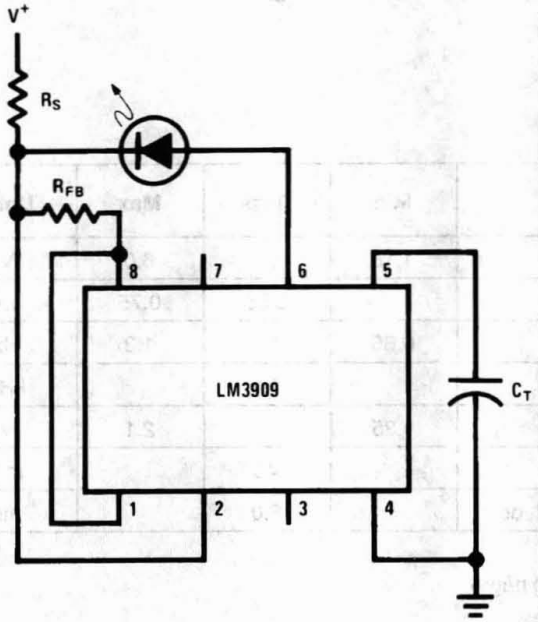


Provides 40 mA. 10 μs pulses at about 8 kHz. Triac gate may be pulse transformer isolated if desired.

TL/H/7969–3

Typical Applications (Continued)(See applications notes below)

Warning Flasher High Voltage Powered

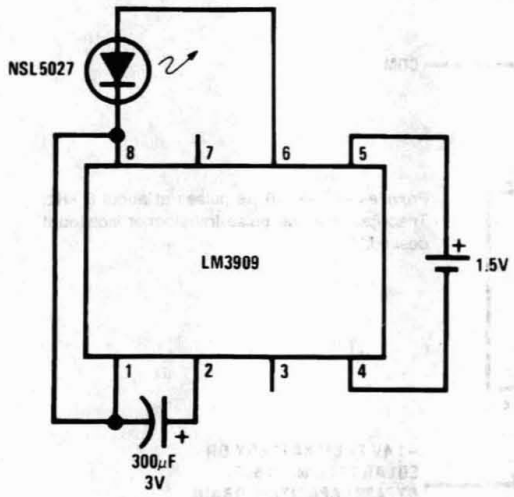


TL/H/7969–4

Typical Operating Conditions

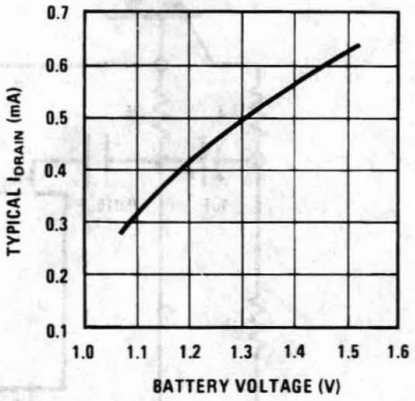
V+	Nominal Flash Hz	C_T	R_S	R_{FB}	V^+_{RANGE}
6V	2	400 μF	1k	1.5k	5V–25V
15V	2	180 μF	3.9k	1k	13V–50V
100V	1.7	180 μF	43k 1W	1k	85V–200V

1.5V Flasher



TL/H/7969–5

Note: Nominal flash rate: 1 Hz.



TL/H/7969–6

Estimated Battery Life (Continuous 1.5V Flasher Operation)

Size Cell	Type	
	Standard	Alkaline
AA	3 months	6 months
C	7 months	15 months
D	1.3 years	2.6 years

Note: Estimates are made from our tests and manufacturers data. Conditions are fresh batteries and room temperature. Clad or "leak-proof" batteries are recommended for any application of five months or more. Nickel Cadmium cells are not recommended.

APPLICATIONS NOTES

Note 1: All capacitors shown are electrolytic unless marked otherwise.

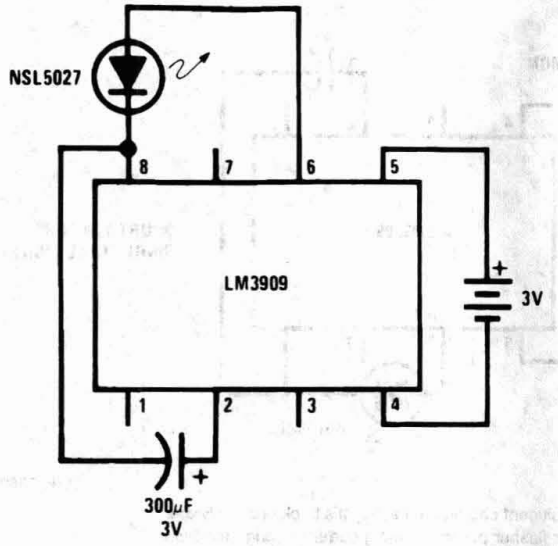
Note 2: Flash rates and frequencies assume a ±5% capacitor tolerance. Electrolytics may vary −20% to +100% of their stated value.

Note 3: Unless noted, measurements above are made with a 1.4V supply, a 25°C ambient temperature, and an LED with a forward drop of 1.5V to 1.7V at 1 mA forward current.

Note 4: Occasionally a flasher circuit will fail to oscillate due to an LED defect that may be missed because it only reduces light output 10% or so. Such LEDs can be identified by a large increase in conduction between 0.9V and 1.2V.

Typical Applications (Continued) (See applications notes on previous page)

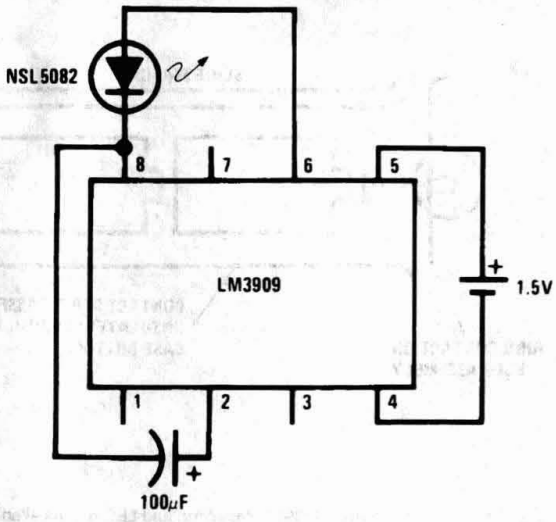
3V Flasher



TL/H/7969–7

Note: Nominal flash rate: 1 Hz. Average $I_{DRAIN} = 0.77$ mA.

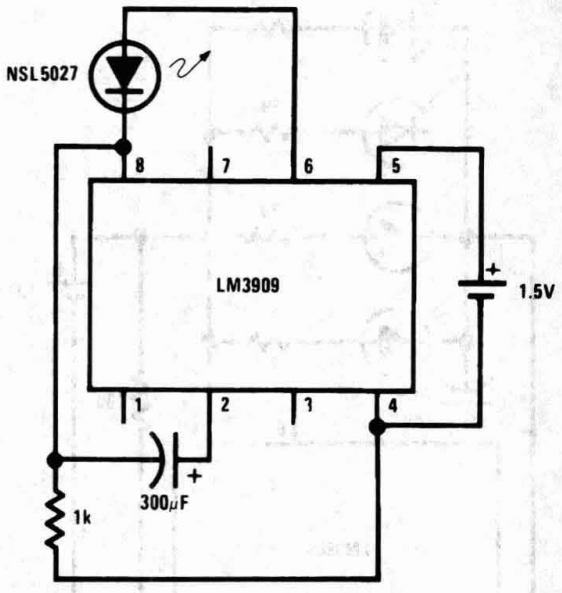
Minimum Power at 1.5V



TL/H/7969–8

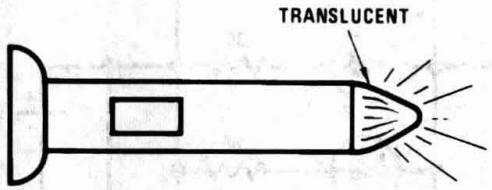
Note: Nominal flash rate: 1.1 Hz. Average $I_{DRAIN} = 0.32$ mA.

Fast Blinker



TL/H/7969–9

Note: Nominal flash rate: 2.6 Hz. Average $I_{DRAIN} = 1.2$ mA.

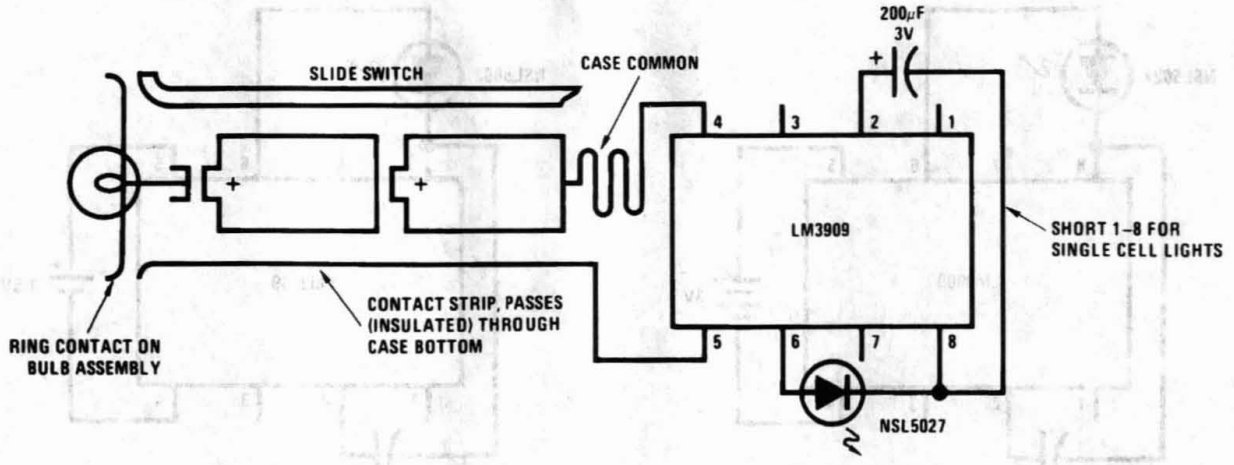


TL/H/7969–11

Note: Winking LED inside, locates light in total darkness.

Typical Applications (Continued) (See applications notes above)

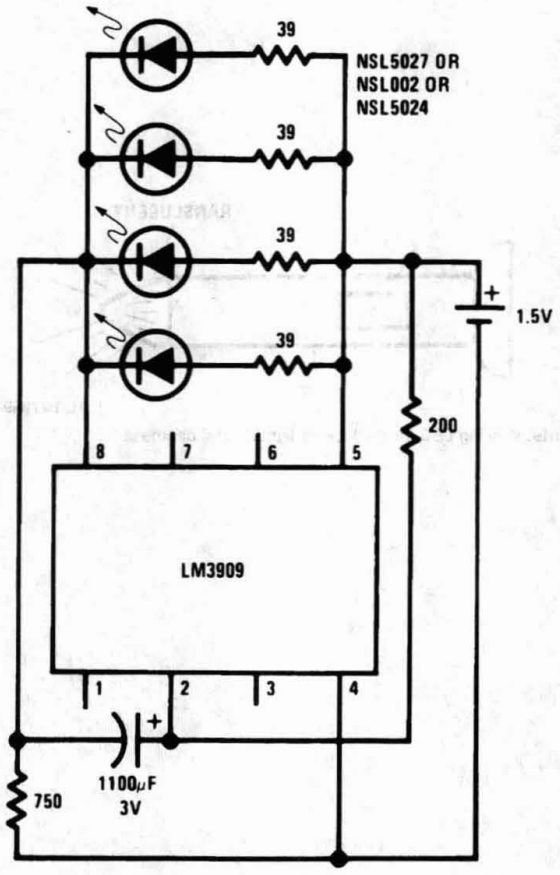
Flashlight Finder



TL/H/7969–10

Note: LM3909, capacitor, and LED are installed in a white translucent cap on the flashlight's back end. Only one contact strip (in addition to the case connection) is needed for flasher power. Drawing current through the bulb simplifies wiring and causes negligible loss since bulb resistance cold is typically less than 2Ω.

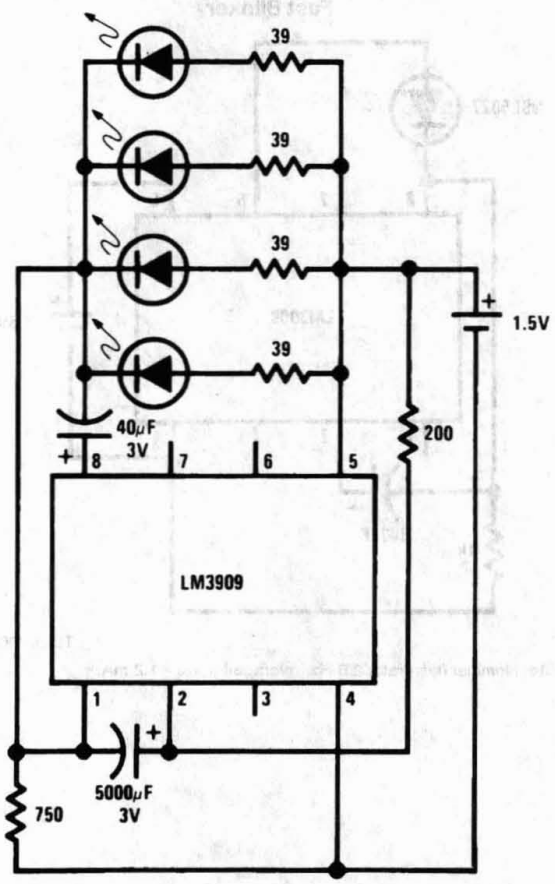
4 Parallel LEDs



TL/H/7969–12

Note: Nominal flash rate: 1.3 Hz. Average I_{DRAIN} = 2 mA.

High Efficiency Parallel Circuit

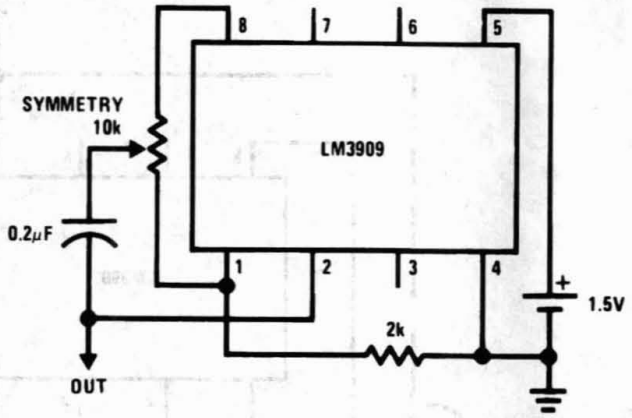


TL/H/7969–13

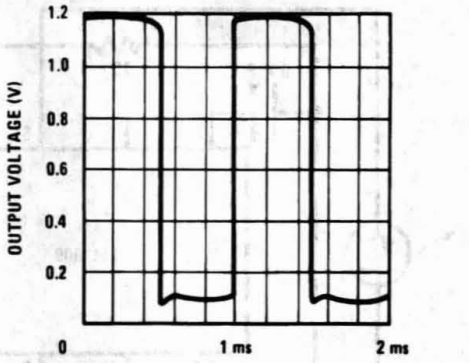
Note: Nominal flash rate: 1.5 Hz. Average I_{DRAIN} = 1.5 mA.

Typical Applications (Continued) (See applications notes above)

1 kHz Square Wave



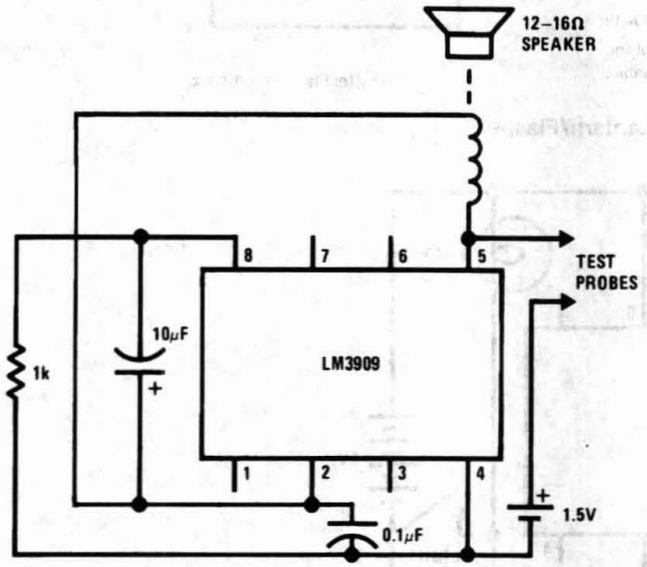
TL/H/7969–14



TL/H/7969–15

Note: Output voltage through a 10k load to ground.

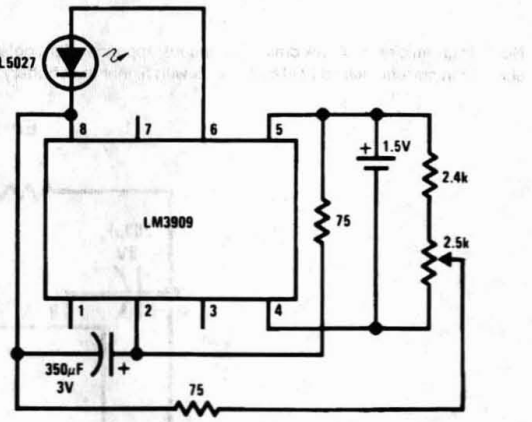
"Buzz Box" Continuity and Coil Checker



TL/H/7969–16

Note: Differences between shorts, coils, and a few ohms of resistance can be heard.

Variable Flasher

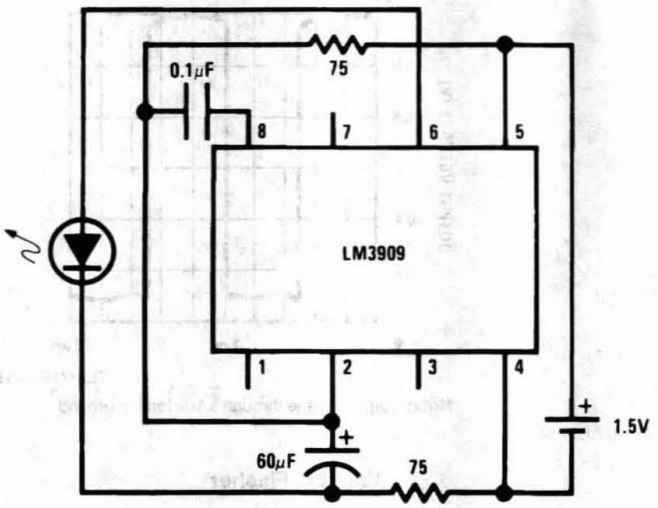


TL/H/7969–17

Note: Flash rate: 0 Hz–20 Hz.

Typical Applications (Continued) (See applications notes above)

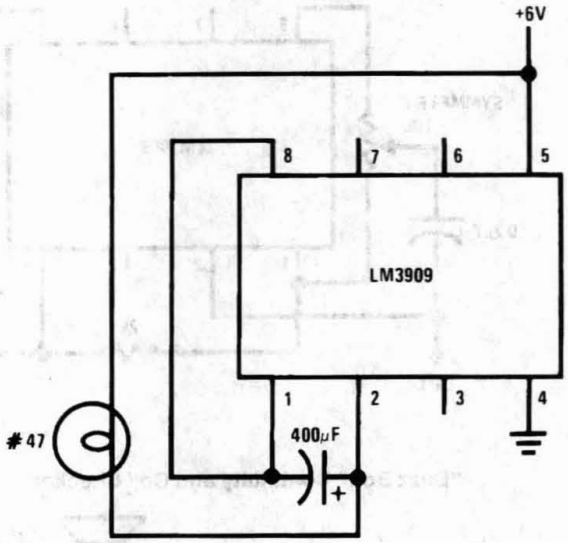
LED Booster



TL/H/7969–18

Note: High efficiency, 4 mA drain. Continuous appearing light obtained by supplying short, high current, pulses (2 kHz) to LEDs with higher than battery voltage available.

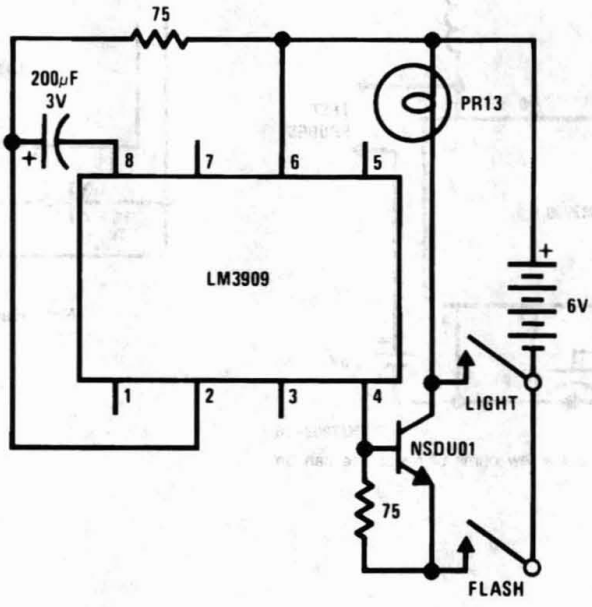
Incandescent Bulb Flasher



TL/H/7969–19

Note: Flash rate: 1.5 Hz.

Emergency Lantern/Flasher



TL/H/7969–20

Note: Nominal flash rate: 1.5 Hz.

National Semiconductor

LM3914 Dot/Bar Display Driver

General Description

The LM3914 is a monolithic integrated circuit that senses analog voltage levels and drives 10 LEDs, providing a linear analog display. A single pin changes the display from a moving dot to a bar graph. Current drive to the LEDs is regulated and programmable, eliminating the need for resistors. This feature is one that allows operation of the whole system from less than 3V.

The circuit contains its own adjustable reference and accurate 10-step voltage divider. The low-bias-current input buffer accepts signals down to ground, or V^-, yet needs no protection against inputs of 35V above or below ground. The buffer drives 10 individual comparators referenced to the precision divider. Indication non-linearity can thus be held typically to ½%, even over a wide temperature range.

Versatility was designed into the LM3914 so that controller, visual alarm, and expanded scale functions are easily added on to the display system. The circuit can drive LEDs of many colors, or low-current incandescent lamps. Many LM3914s can be "chained" to form displays of 20 to over 100 segments. Both ends of the voltage divider are externally available so that 2 drivers can be made into a zero-center meter.

The LM3914 is very easy to apply as an analog meter circuit. A 1.2V full-scale meter requires only 1 resistor and a single 3V to 15V supply in addition to the 10 display LEDs. If the 1 resistor is a pot, it becomes the LED brightness control. The simplified block diagram illustrates this extremely simple external circuitry.

When in the dot mode, there is a small amount of overlap or "fade" (about 1 mV) between segments. This assures that at no time will all LEDs be "OFF", and thus any ambiguous display is avoided. Various novel displays are possible.

Much of the display flexibility derives from the fact that all outputs are individual, DC regulated currents. Various effects can be achieved by modulating these currents. The individual outputs can drive a transistor as well as a LED at the same time, so controller functions including "staging" control can be performed. The LM3914 can also act as a programmer, or sequencer.

The LM3914 is rated for operation from 0°C to +70°C. The LM3914N is available in an 18-lead molded (N) package.

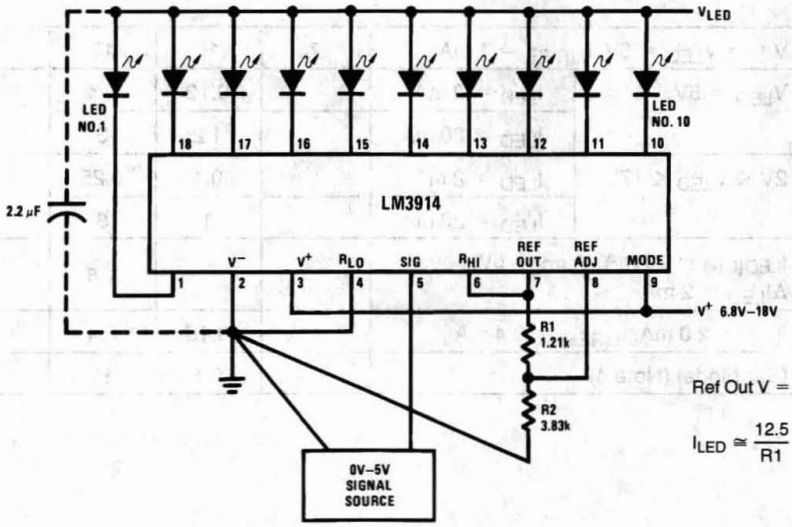
The following typical application illustrates adjusting of the reference to a desired value, and proper grounding for accurate operation, and avoiding oscillations.

Features

- Drives LEDs, LCDs or vacuum fluorescents
- Bar or dot display mode externally selectable by user
- Expandable to displays of 100 steps
- Internal voltage reference from 1.2V to 12V
- Operates with single supply of less than 3V
- Inputs operate down to ground
- Output current programmable from 2 mA to 30 mA
- No multiplex switching or interaction between outputs
- Input withstands ±35V without damage or false outputs
- LED driver outputs are current regulated, open-collectors
- Outputs can interface with TTL or CMOS logic
- The internal 10-step divider is floating and can be referenced to a wide range of voltages

Typical Applications

0V to 5V Bar Graph Meter



Note 1: Grounding method is typical of *all* uses. The 2.2 µF tantalum or 10 µF aluminum electrolytic capacitor is needed if leads to the LED supply are 6" or longer.

$$\text{Ref Out V} = 1.25\left(1 + \frac{R2}{R1}\right)$$ 2.28

$$I_{LED} \cong \frac{12.5}{R1}$$ 2.6 mA

TL/H/7970–1

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Power Dissipation (Note 5)	
Molded DIP (N)	1365 mW
Supply Voltage	25V
Voltage on Output Drivers	25V
Input Signal Overvoltage (Note 3)	±35V
Divider Voltage	−100 mV to V^+
Reference Load Current	10 mA
Storage Temperature Range	−55°C to +150°C
Soldering Information	
Dual-In-Line Package	
Soldering (10 seconds)	260°C
Plastic Chip Carrier Package	
Vapor Phase (60 seconds)	215°C
Infrared (15 seconds)	220°C

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.

Electrical Characteristics (Notes 1 and 3)

Parameter	Conditions (Note 1)		Min	Typ	Max	Units
COMPARATOR						
Offset Voltage, Buffer and First Comparator	$0V \le V_{RLO} = V_{RHI} \le 12V$, I_{LED} = 1 mA			3	10	mV
Offset Voltage, Buffer and Any Other Comparator	$0V \le V_{RLO} = V_{RHI} \le 12V$, I_{LED} = 1 mA			3	15	mV
Gain ($\Delta I_{LED}/\Delta V_{IN}$)	$I_{L(REF)}$ = 2 mA, I_{LED} = 10 mA		3	8		mA/mV
Input Bias Current (at Pin 5)	$0V \le V_{IN} \le V^+ - 1.5V$			25	100	nA
Input Signal Overvoltage	No Change in Display		−35		35	V
VOLTAGE-DIVIDER						
Divider Resistance	Total, Pin 6 to 4		8	12	17	kΩ
Accuracy	(Note 2)			0.5	2	%
VOLTAGE REFERENCE						
Output Voltage	0.1 mA ≤ $I_{L(REF)}$ ≤ 4 mA, $V^+ = V_{LED}$ = 5V		1.2	1.28	1.34	V
Line Regulation	$3V \le V^+ \le 18V$			0.01	0.03	%/V
Load Regulation	0.1 mA ≤ $I_{L(REF)}$ ≤ 4 mA, $V^+ = V_{LED}$ = 5V			0.4	2	%
Output Voltage Change with Temperature	0°C ≤ T_A ≤ +70°C, $I_{L(REF)}$ = 1 mA, V^+ = 5V			1		%
Adjust Pin Current				75	120	μA
OUTPUT DRIVERS						
LED Current	$V^+ = V_{LED}$ = 5V, $I_{L(REF)}$ = 1 mA		7	10	13	mA
LED Current Difference (Between Largest and Smallest LED Currents)	V_{LED} = 5V	I_{LED} = 2 mA		0.12	0.4	mA
		I_{LED} = 20 mA		1.2	3	
LED Current Regulation	2V ≤ V_{LED} ≤ 17V	I_{LED} = 2 mA		0.1	0.25	mA
		I_{LED} = 20 mA		1	3	
Dropout Voltage	$I_{LED(ON)}$ = 20 mA, V_{LED} = 5V, ΔI_{LED} = 2 mA				1.5	V
Saturation Voltage	I_{LED} = 2.0 mA, $I_{L(REF)}$ = 0.4 mA			0.15	0.4	V
Output Leakage, Each Collector	(Bar Mode) (Note 4)			0.1	10	μA

Electrical Characteristics (Note 1) (Continued)

Parameter	Conditions (Note 1)		Min	Typ	Max	Units
OUTPUT DRIVERS (Continued)						
Output Leakage	(Dot Mode) (Note 4)	Pins 10–18		0.1	10	μA
		Pin 1	60	150	450	μA
SUPPLY CURRENT						
Standby Supply Current (All Outputs Off)	$V^+ = 5V$, $I_{L(REF)} = 0.2$ mA			2.4	4.2	mA
	$V^+ = 20V$, $I_{L(REF)} = 1.0$ mA			6.1	9.2	mA

Note 1: Unless otherwise stated, all specifications apply with the following conditions:
$3\ V_{DC} \le V^+ \le 20\ V_{DC}$ $V_{REF}, V_{RHI}, V_{RLO} \le (V^+ - 1.5V)$
$3\ V_{DC} \le V_{LED} \le V^+$ $0V \le V_{IN} \le V^+ - 1.5V$
$-0.015V \le V_{RLO} \le 12\ V_{DC}$ $T_A = +25°C$, $I_{L(REF)} = 0.2$ mA, $V_{LED} = 3.0V$, pin 9 connected to pin 3 (Bar Mode).
$-0.015V \le V_{RHI} \le 12\ V_{DC}$
For higher power dissipations, pulse testing is used.

Note 2: Accuracy is measured referred to $+10.000\ V_{DC}$ at pin 6, with $0.000\ V_{DC}$ at pin 4. At lower full-scale voltages, buffer and comparator offset voltage may add significant error.

Note 3: Pin 5 input current must be limited to ±3 mA. The addition of a 39k resistor in series with pin 5 allows ±100V signals without damage.

Note 4: Bar mode results when pin 9 is within 20 mV of V^+. Dot mode results when pin 9 is pulled at least 200 mV below V^+ or left open circuit. LED No. 10 (pin 10 output current) is disabled if pin 9 is pulled 0.9V or more below V_{LED}.

Note 5: The maximum junction temperature of the LM3914 is 100°C. Devices must be derated for operation at elevated temperatures. Junction to ambient thermal resistance is 55°C/W for the molded DIP (N package).

Definition of Terms

Accuracy: The difference between the observed threshold voltage and the ideal threshold voltage for each comparator. Specified and tested with 10V across the internal voltage divider so that resistor ratio matching error predominates over comparator offset voltage.

Adjust Pin Current: Current flowing out of the reference adjust pin when the reference amplifier is in the linear region.

Comparator Gain: The ratio of the change in output current (I_{LED}) to the change in input voltage (V_{IN}) required to produce it for a comparator in the linear region.

Dropout Voltage: The voltage measured at the current source outputs required to make the output current fall by 10%.

Input Bias Current: Current flowing out of the signal input when the input buffer is in the linear region.

LED Current Regulation: The change in output current over the specified range of LED supply voltage (V_{LED}) as measured at the current source outputs. As the forward voltage of an LED does not change significantly with a small change in forward current, this is equivalent to changing the voltage at the LED anodes by the same amount.

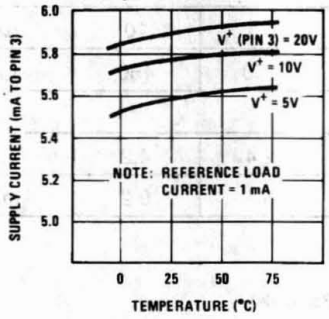
Line Regulation: The average change in reference output voltage over the specified range of supply voltage (V^+).

Load Regulation: The change in reference output voltage (V_{REF}) over the specified range of load current ($I_{L(REF)}$).

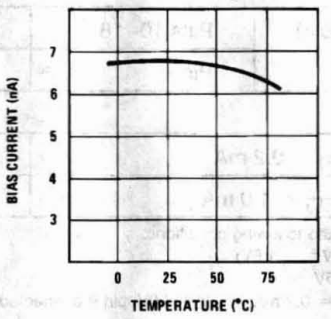
Offset Voltage: The differential input voltage which must be applied to each comparator to bias the output in the linear region. Most significant error when the voltage across the internal voltage divider is small. Specified and tested with pin 6 voltage (V_{RHI}) equal to pin 4 voltage (V_{RLO}).

Typical Performance Characteristics

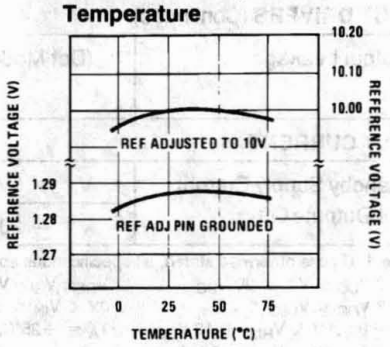
Supply Current vs Temperature



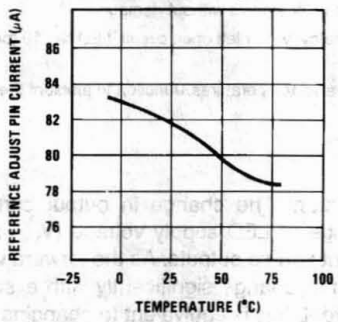
Operating Input Bias Current vs Temperature



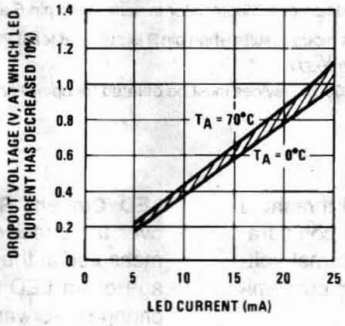
Reference Voltage vs Temperature



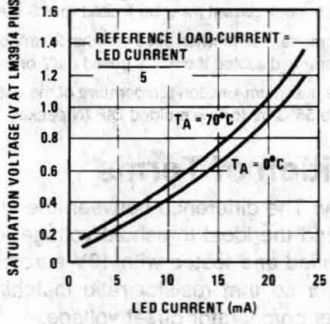
Reference Adjust Pin Current vs Temperature



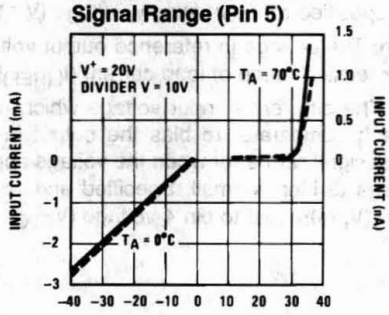
LED Current-Regulation Dropout



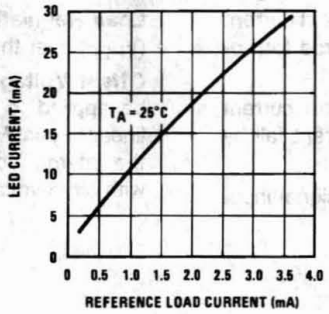
LED Driver Saturation Voltage



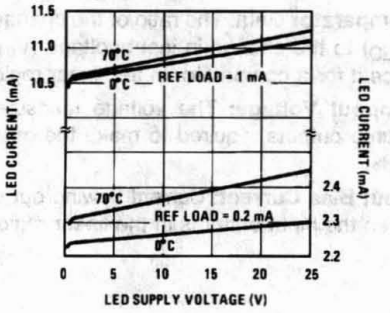
Input Current Beyond Signal Range (Pin 5)



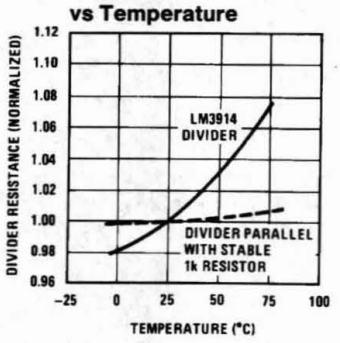
LED Current vs Reference Loading



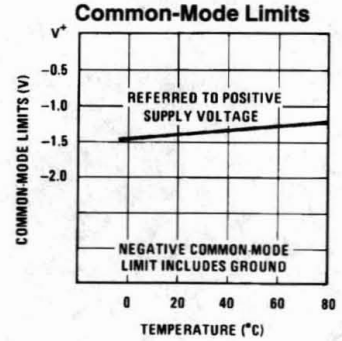
LED Driver Current Regulation



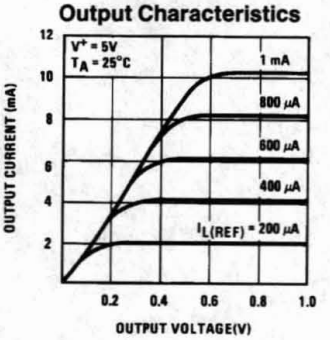
Total Divider Resistance vs Temperature



Common-Mode Limits

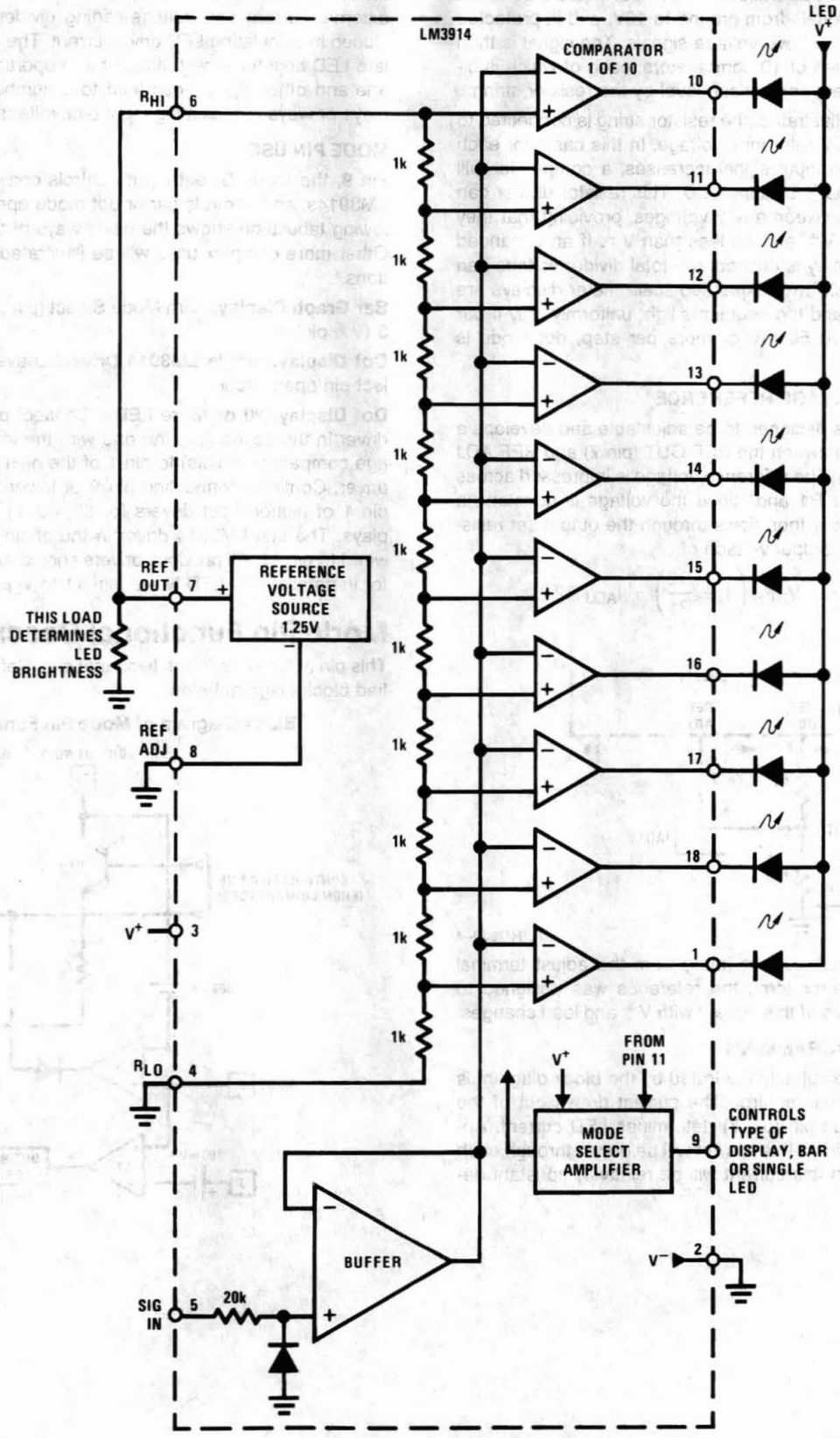


Output Characteristics



TL/H/7970–2

Block Diagram (Showing Simplest Application)



TL/H/7970–3

Functional Description

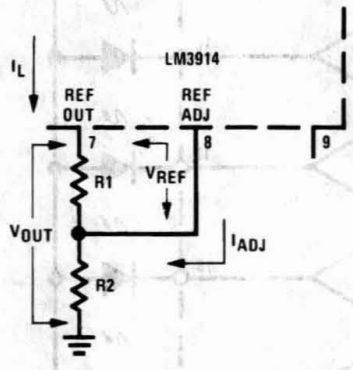
The simplifed LM3914 block diagram is to give the general idea of the circuit's operation. A high input impedance buffer operates with signals from ground to 12V, and is protected against reverse and overvoltage signals. The signal is then applied to a series of 10 comparators; each of which is biased to a different comparison level by the resistor string.

In the example illustrated, the resistor string is connected to the internal 1.25V reference voltage. In this case, for each 125 mV that the input signal increases, a comparator will switch on another indicating LED. This resistor divider can be connected between any 2 voltages, providing that they are 1.5V below V^+ and no less than V^-. If an expanded scale meter display is desired, the total divider voltage can be as little as 200 mV. Expanded-scale meter displays are more accurate and the segments light uniformly only if bar mode is used. At 50 mV or more per step, dot mode is usable.

INTERNAL VOLTAGE REFERENCE

The reference is designed to be adjustable and develops a nominal 1.25V between the REF OUT (pin 7) and REF ADJ (pin 8) terminals. The reference voltage is impressed across program resistor R1 and, since the voltage is constant, a constant current I_1 then flows through the output set resistor R2 giving an output voltage of:

$$V_{OUT} = V_{REF}\left(1 + \frac{R2}{R1}\right) + I_{ADJ}\,R2$$



TL/H/7970–4

Since the 120 μA current (max) from the adjust terminal represents an error term, the reference was designed to minimize changes of this current with V^+ and load changes.

CURRENT PROGRAMMING

A feature not completely illustrated by the block diagram is the LED brightness control. The current drawn out of the reference voltage pin (pin 7) determines LED current. Approximately 10 times this current will be drawn through each lighted LED, and this current will be relatively constant despite supply voltage and temperature changes. Current drawn by the internal 10-resistor divider, as well as by the external current and voltage-setting divider should be included in calculating LED drive current. The ability to modulate LED brightness with time, or in proportion to input voltage and other signals can lead to a number of novel displays or ways of indicating input overvoltages, alarms, etc.

MODE PIN USE

Pin 9, the Mode Select input controls chaining of multiple LM3914s, and controls bar or dot mode operation. The following tabulation shows the basic ways of using this input. Other more complex uses will be illustrated in the applications.

Bar Graph Display: Wire Mode Select (pin 9) *directly* to pin 3 (V^+ pin).

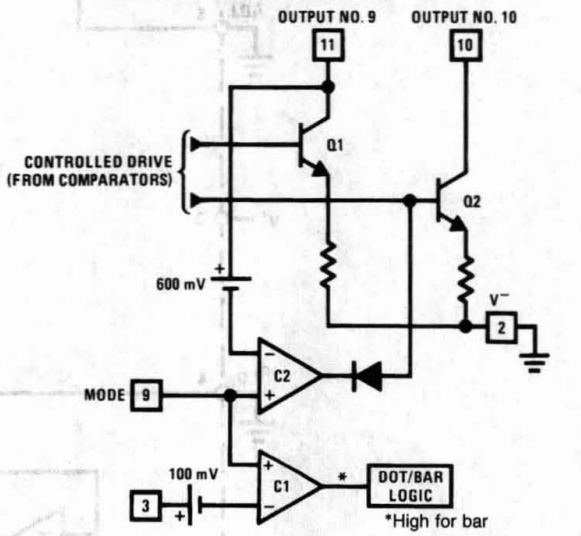
Dot Display, Single LM3914 Driver: Leave the Mode Select pin open circuit.

Dot Display, 20 or More LEDs: Connect pin 9 of the *first* driver in the series (i.e., the one with the lowest input voltage comparison points) to pin 1 of the next higher LM3914 driver. Continue connecting pin 9 of lower input drivers to pin 1 of higher input drivers for 30, 40, or more LED displays. The last LM3914 driver in the chain will have pin 9 wired to pin 11. All previous drivers should have a 20k resistor in parallel with LED No. 9 (pin 11 to V_{LED}).

Mode Pin Functional Description

This pin actually performs two functions. Refer to the simplified block diagram below.

Block Diagram of Mode Pin Function



TL/H/7970–5

Mode Pin Functional Description (Continued)

DOT OR BAR MODE SELECTION

The voltage at pin 9 is sensed by comparator C1, nominally referenced to ($V^+ - 100$ mV). The chip is in bar mode when pin 9 is above this level; otherwise it's in dot mode. The comparator is designed so that pin 9 can be left open circuit for dot mode.

Taking into account comparator gain and variation in the 100 mV reference level, pin 9 should be no more than 20 mV below V^+ for bar mode and more than 200 mV below V^+ (or open circuit) for dot mode. In most applications, pin 9 is either open (dot mode) or tied to V^+ (bar mode). In bar mode, pin 9 should be connected directly to pin 3. Large currents drawn from the power supply (LED current, for example) should not share this path so that large IR drops are avoided.

DOT MODE CARRY

In order for the display to make sense when multiple LM3914s are cascaded in dot mode, special circuitry has been included to shut off LED No. 10 of the first device when LED No. 1 of the second device comes on. The connection for cascading in dot mode has already been described and is depicted below.

As long as the input signal voltage is below the threshold of the second LM3914, LED No. 11 is off. Pin 9 of LM3914 No. 1 thus sees effectively an open circuit so the chip is in dot mode. As soon as the input voltage reaches the threshold of LED No. 11, pin 9 of LM3914 No. 1 is pulled an LED drop (1.5V or more) below V_{LED}. This condition is sensed by comparator C2, referenced 600 mV below V_{LED}. This forces the output of C2 low, which shuts off output transistor Q2, extinguishing LED No. 10.

V_{LED} is sensed via the 20k resistor connected to pin 11. The very small current (less than 100 μA) that is diverted from LED No. 9 does not noticeably affect its intensity.

An auxiliary current source at pin 1 keeps at least 100 μA flowing through LED No. 11 even if the input voltage rises high enough to extinguish the LED. This ensures that pin 9 of LM3914 No. 1 is held low enough to force LED No. 10 off when *any* higher LED is illuminated. While 100 μA does not normally produce significant LED illumination, it may be noticeable when using high-efficiency LEDs in a dark environment. If this is bothersome, the simple cure is to shunt LED No. 11 with a 10k resistor. The 1V IR drop is more than the 900 mV worst case required to hold off LED No. 10 yet small enough that LED No. 11 does not conduct significantly.

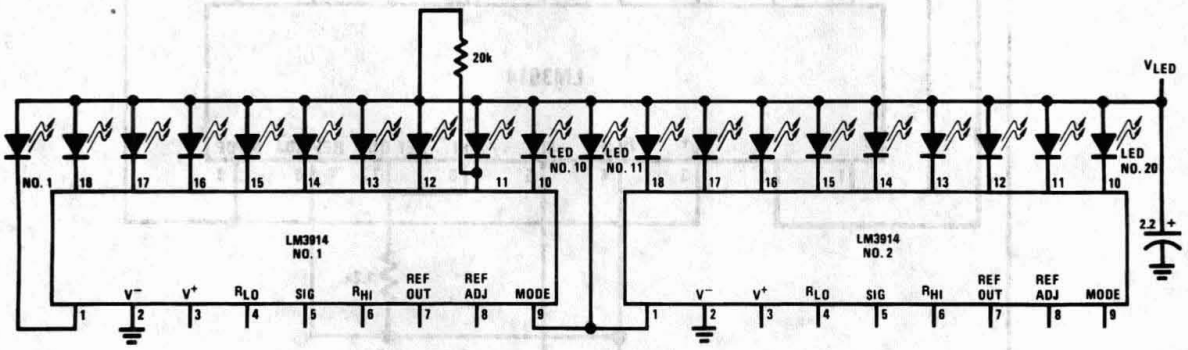
OTHER DEVICE CHARACTERISTICS

The LM3914 is relatively low-powered itself, and since any number of LEDs can be powered from about 3V, it is a very efficient display driver. Typical standby supply current (all LEDs OFF) is 1.6 mA (2.5 mA max). However, any reference loading adds 4 times that current drain to the V^+ (pin 3) supply input. For example, an LM3914 with a 1 mA reference pin load (1.3k), would supply almost 10 mA to every LED while drawing only 10 mA from its V^+ pin supply. At full-scale, the IC is typically drawing less than 10% of the current supplied to the display.

The display driver does not have built-in hysteresis so that the display does not jump instantly from one LED to the next. Under rapidly changing signal conditions, this cuts down high frequency noise and often an annoying flicker. An "overlap" is built in so that at no time between segments are all LEDs completely OFF in the dot mode. Generally 1 LED fades in while the other fades out over a mV or more of range (Note 2). The change may be much more rapid between LED No. 10 of one device and LED No. 1 of a *second* device "chained" to the first.

The LM3914 features individually current regulated LED driver transistors. Further internal circuitry detects when any driver transistor goes into saturation, and prevents other circuitry from drawing excess current. This results in the ability of the LM3914 to drive and regulate LEDs powered from a pulsating DC power source, i.e., largely unfiltered. (Due to possible oscillations at low voltages a nominal bypass capacitor consisting of a 2.2 μF solid tantalum connected from the pulsating LED supply to pin 2 of the LM3914 is recommended.) This ability to operate with low or fluctuating voltages also allows the display driver to interface with logic circuitry, opto-coupled solid-state relays, and low-current incandescent lamps.

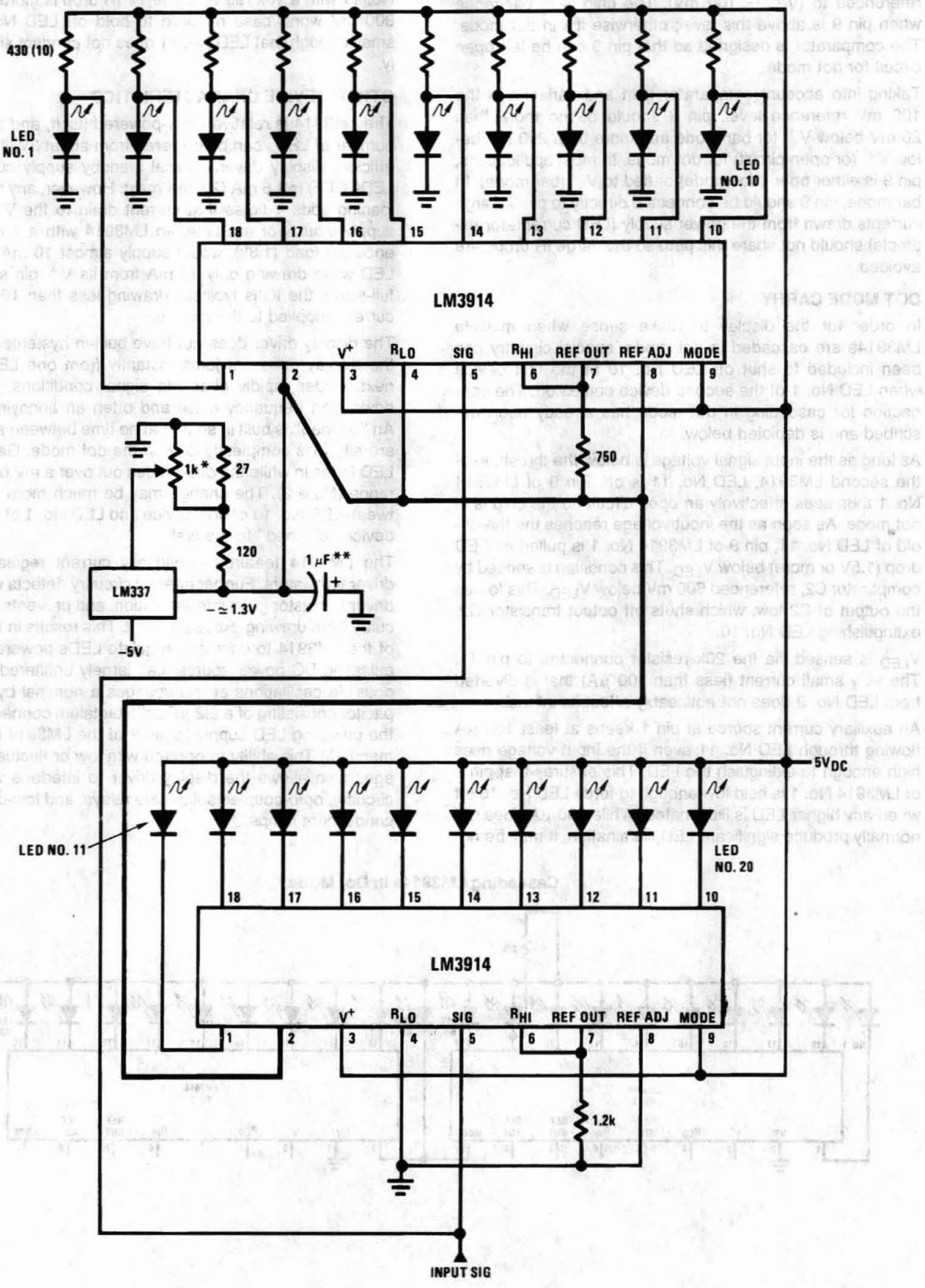
Cascading LM3914s in Dot Mode



TL/H/7970–6

Typical Applications (Continued)

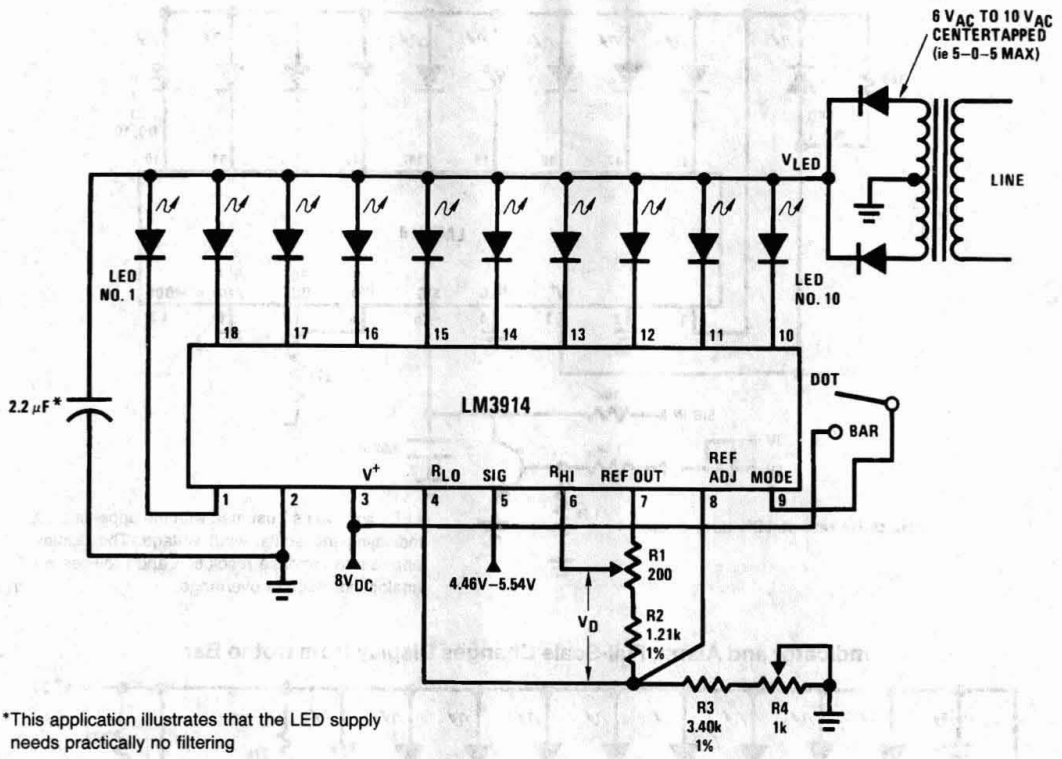
Zero-Center Meter, 20-Segment



TL/H/7970–7

Typical Applications (Continued)

Expanded Scale Meter, Dot or Bar



*This application illustrates that the LED supply needs practically no filtering

Calibration: With a precision meter between pins 4 and 6 adjust R1 for voltage V_D of 1.20V. Apply 4.94V to pin 5, and adjust R4 until LED No. 5 just lights. The adjustments are non-interacting.

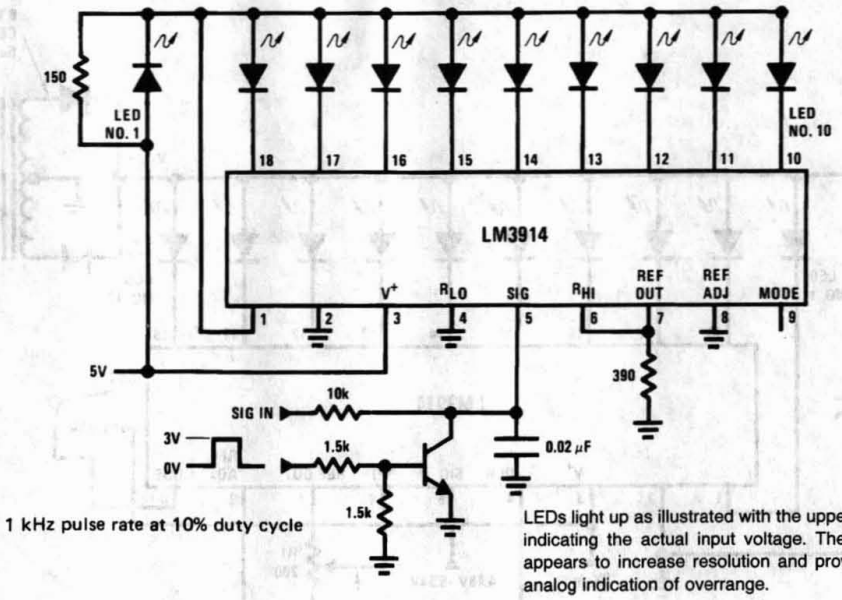
TL/H/7970–8

Application Example: Grading 5V Regulators

Highest No. LED on	Color	$V_{OUT(MIN)}$
10	Red	5.54
9	Red	5.42
8	Yellow	5.30
7	Green	5.18
6	Green	5.06
5V		
5	Green	4.94
4	Green	4.82
3	Yellow	4.7
2	Red	4.58
1	Red	4.46

Typical Applications (Continued)

"Exclamation Point" Display

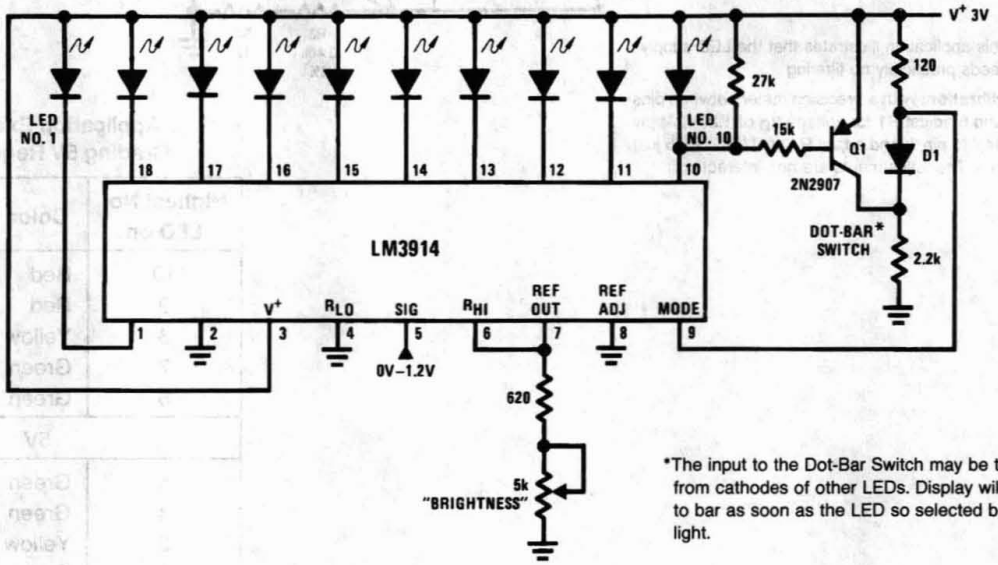


1 kHz pulse rate at 10% duty cycle

LEDs light up as illustrated with the upper lit LED indicating the actual input voltage. The display appears to increase resolution and provides an analog indication of overrange.

TL/H/7970–9

Indicator and Alarm, Full-Scale Changes Display from Dot to Bar

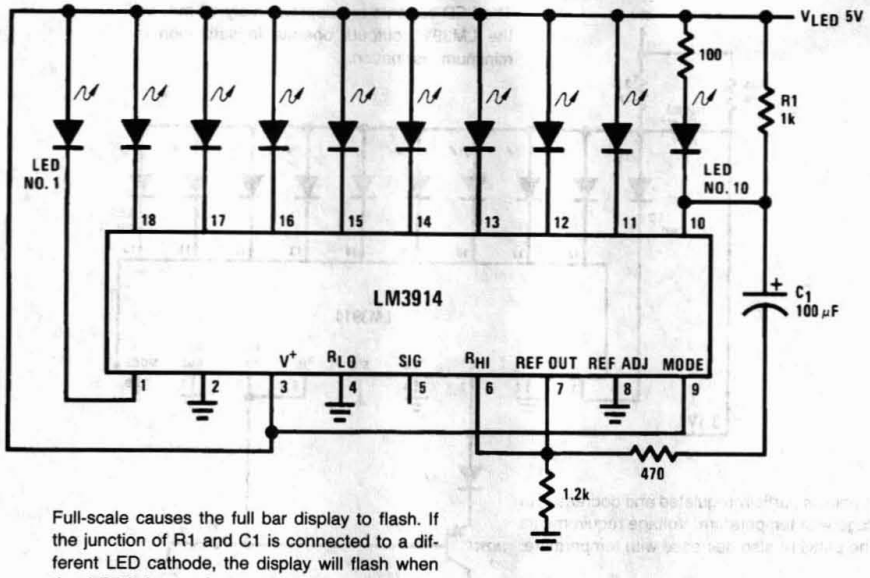


*The input to the Dot-Bar Switch may be taken from cathodes of other LEDs. Display will change to bar as soon as the LED so selected begins to light.

TL/H/7970–10

Typical Applications (Continued)

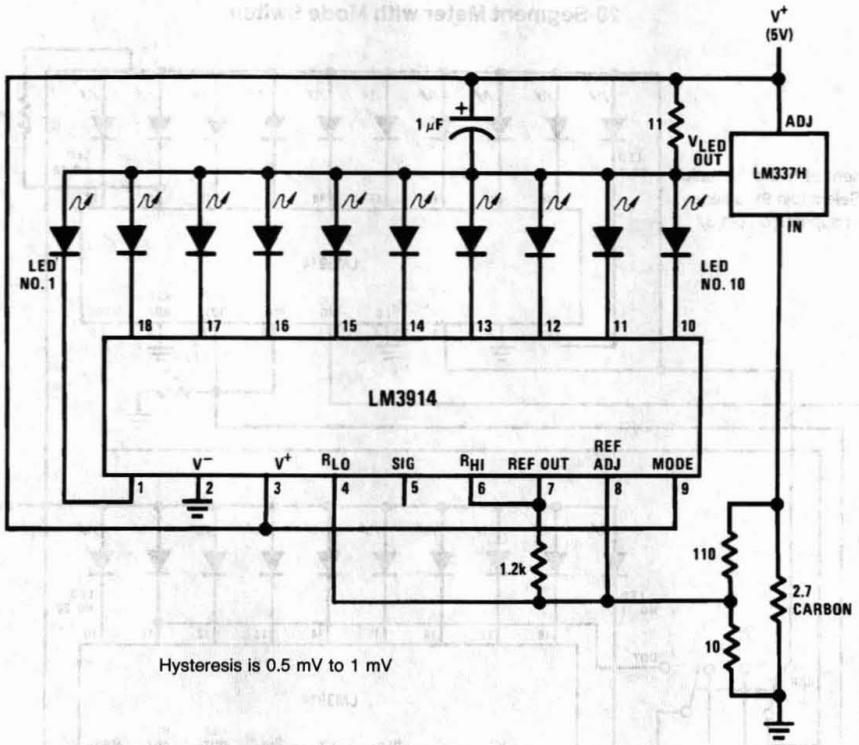
Bar Display wih Alarm Flasher



Full-scale causes the full bar display to flash. If the junction of R1 and C1 is connected to a different LED cathode, the display will flash when that LED lights, and at any higher input signal.

TL/H/7970–11

Adding Hysteresis (Single Supply, Bar Mode Only)

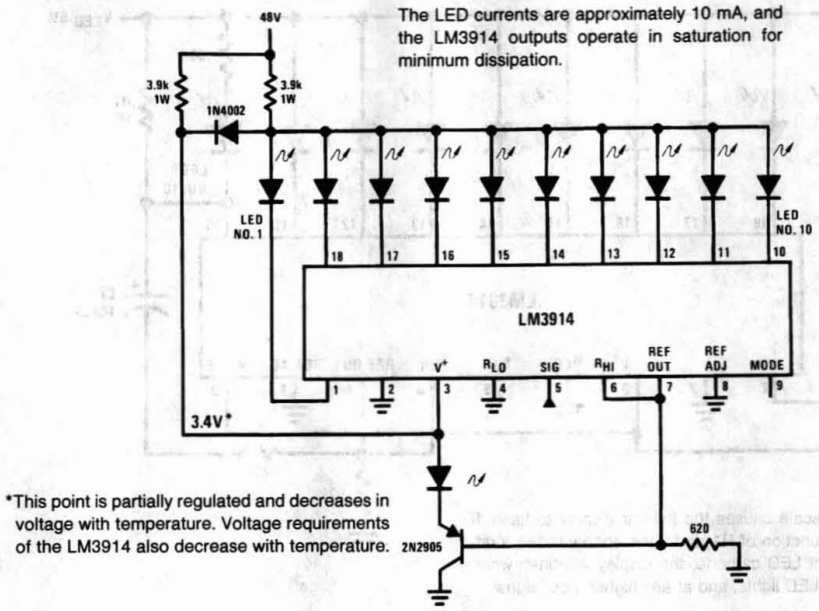


Hysteresis is 0.5 mV to 1 mV

TL/H/7970–12

Typical Application (Continued)

Operating with a High Voltage Supply (Dot Mode Only)



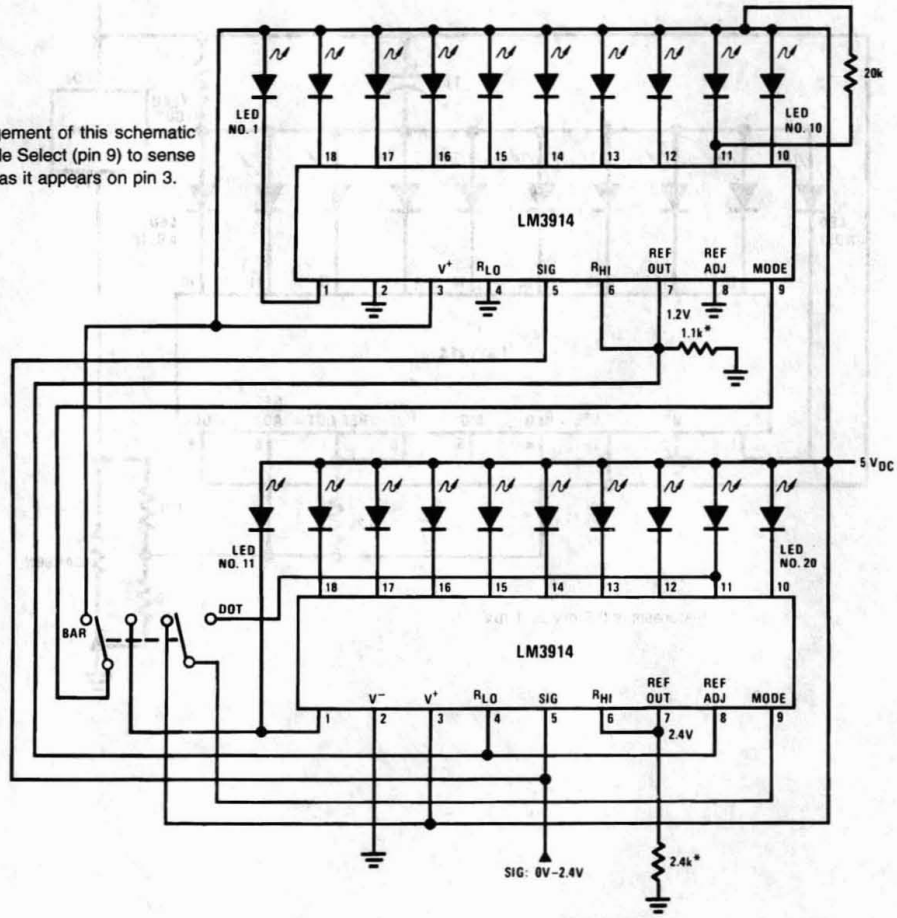
The LED currents are approximately 10 mA, and the LM3914 outputs operate in saturation for minimum dissipation.

*This point is partially regulated and decreases in voltage with temperature. Voltage requirements of the LM3914 also decrease with temperature.

TL/H/7970–13

20-Segment Meter with Mode Switch

*The exact wiring arrangement of this schematic shows the need for Mode Select (pin 9) to sense the V^+ voltage exactly as it appears on pin 3.



*Programs LEDs to 10 mA

TL/H/7970–14

Application Hints

Three of the most commonly needed precautions for using the LM3914 are shown in the first typical application drawing (see page 9-108) showing a 0V–5V bar graph meter. The most difficult problem occurs when large LED currents are being drawn, especially in bar graph mode. These currents flowing out of the ground pin cause voltage drops in external wiring, and thus errors and oscillations. Bringing the return wires from signal sources, reference ground and bottom of the resistor string (as illustrated) to a single point very near pin 2 is the best solution.

Long wires from V_{LED} to LED anode common can cause oscillations. Depending on the severity of the problem 0.05 μF to 2.2 μF decoupling capacitors from LED anode common to pin 2 will damp the circuit. If LED anode line wiring is inaccessible, often similar decoupling from pin 1 to pin 2 will be sufficient.

If LED turn ON seems slow (bar mode) or several LEDs light (dot mode), oscillation or excessive noise is usually the problem. In cases where proper wiring and bypassing fail to stop oscillations, V^+ voltage at pin 3 is usually below suggested limits (see Note 2, page 9-108). Expanded scale meter applications may have one or both ends of the internal voltage divider terminated at relatively high value resistors. These high-impedance ends should be bypassed to pin 2 with at least a 0.001 μF capacitor, or up to 0.1 μF in noisy environments.

Power dissipation, especially in bar mode should be given consideration. For example, with a 5V supply and all LEDs programmed to 20 mA the driver will dissipate over 600 mW. In this case a 7.5Ω resistor in series with the LED supply will cut device heating in half. The negative end of the resistor should be bypassed with a 2.2 μF solid tantalum capacitor to pin 2 of the LM3914.

Turning OFF of most of the internal current sources is accomplished by pulling positive on the reference with a current source or resistance supplying 100 μA or so. Alternately, the input signal can be gated OFF with a transistor switch.

Other special features and applications characteristics will be illustrated in the following applications schematics. Notes have been added in many cases, attempting to cover any special procedures or unusual characteristics of these applications. A special section called "Application Tips for the LM3914 Adjustable Reference" has been included with these schematics.

APPLICATION TIPS FOR THE LM3914 ADJUSTABLE REFERENCE

GREATLY EXPANDED SCALE (BAR MODE ONLY)

Placing the LM3914 internal resistor divider in parallel with a section ($\cong$230Ω) of a stable, low resistance divider greatly reduces voltage changes due to IC resistor value changes with temperature. Voltage V_1 should be trimmed to 1.1V first by use of R2. Then the voltage V_2 across the IC divider string can be adjusted to 200 mV, using R5 without affecting V_1. LED current will be approximately 10 mA.

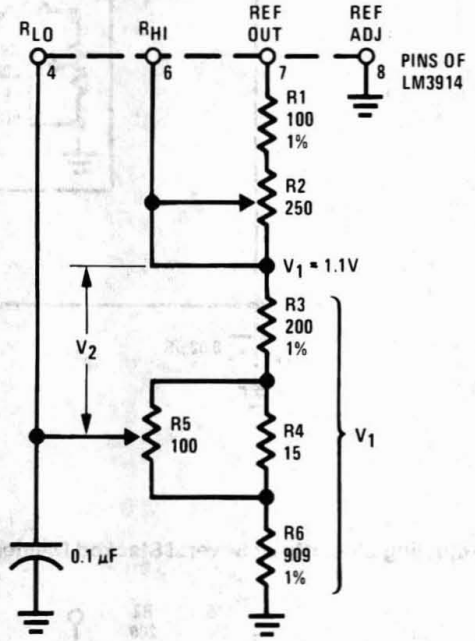
NON-INTERACTING ADJUSTMENTS FOR EXPANDED SCALE METER (4.5V to 5V, Bar *or* Dot Mode)

This arrangement allows independent adjustment of LED brightness regardless of meter span and zero adjustments.

First, V_1 is adjusted to 5V, using R2. Then the span (voltage across R4) can be adjusted to exactly 0.5V using R6 without affecting the previous adjustment.

R9 programs LED currents within a range of 2.2 mA to 20 mA after the above settings are made.

Greatly Expanded Scale (Bar Mode Only)



TL/H/7970–15

ADJUSTING LINEARITY OF SEVERAL STACKED DIVIDERS

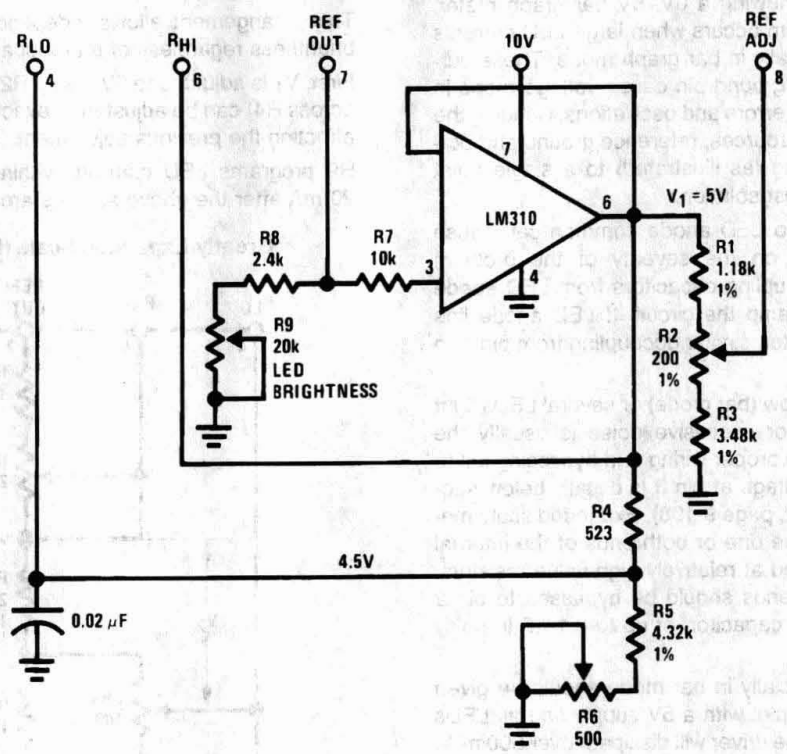
Three internal voltage dividers are shown connected in series to provide a 30-step display. If the resulting analog meter is to be accurate and linear the voltage on each divider must be adjusted, preferably without affecting any other adjustments. To do this, adjust R2 first, so that the voltage across R5 is exactly 1V. Then the voltages across R3 and R4 can be independently adjusted by shunting each with selected resistors of 6 kΩ or higher resistance. This is possible because the reference of LM3914 No. 3 is acting as a constant current source.

The references associated with LM3914s No. 1 and No. 2 should have their Ref Adj pins (pin 8) wired to ground, and their Ref Outputs loaded by a 620Ω resistor to ground. This makes available similar 20 mA current outputs to all the LEDs in the system.

If an independent LED brightness control is desired (as in the previous application), a unity gain buffer, such as the LM310, should be placed between pin 7 and R1, similar to the previous application.

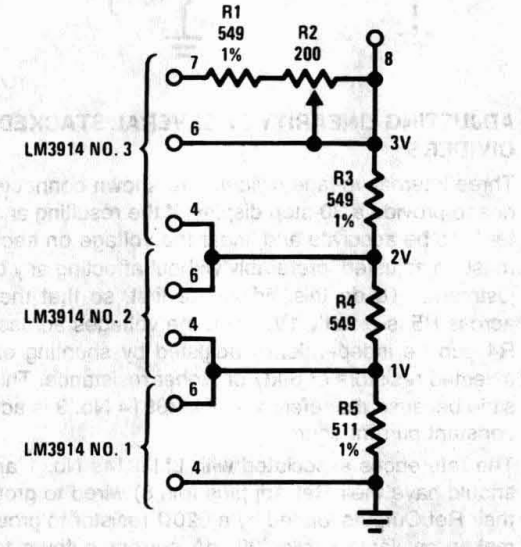
Application Hints (Continued)

Non-Interacting Adjustments for Expanded Scale Meter (4.5V to 5V, Bar *or* Dot Mode)



TL/H/7970–16

Adjusting Linearity of Several Stacked Dividers



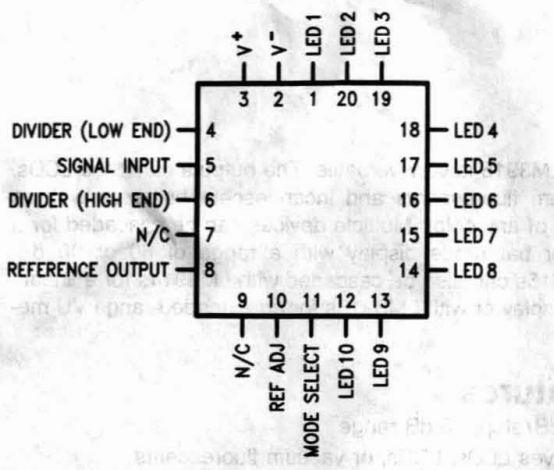
TL/H/7970–17

Other Applications

- "Slow"—fade bar or dot display (doubles resolution)
- 20-step meter with single pot brightness control
- 10-step (or multiples) programmer
- Multi-step or "staging" controller
- Combined controller and process deviation meter
- Direction and rate indicator (to add to DVMs)
- Exclamation point display for power saving
- Graduations can be added to dot displays. Dimly light every other LED using a resistor to ground
- Electronic "meter-relay"—display could be circle or semi-circle
- Moving "hole" display—indicator LED is dark, rest of bar lit
- Drives vacuum-fluorescent and LCDs using added passive parts

Connection Diagrams

Plastic Chip Carrier Package

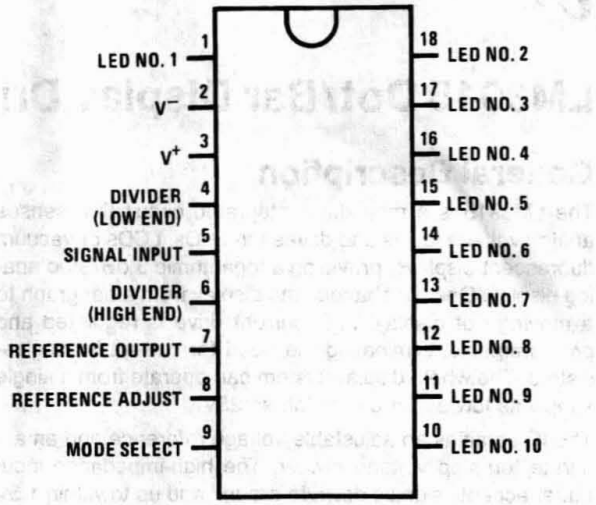


TL/H/7970–18

Top View

Order Number LM3914V
See NS Package Number V20A

Dual-In-Line Package



TL/H/7970–19

Top View

Order Number LM3914N
See NS Package Number N18A

National Semiconductor

LM3915 Dot/Bar Display Driver

General Description

The LM3915 is a monolithic integrated circuit that senses analog voltage levels and drives ten LEDs, LCDs or vacuum fluorescent displays, providing a logarithmic 3 dB/step analog display. One pin changes the display from a bar graph to a moving dot display. LED current drive is regulated and programmable, eliminating the need for current limiting resistors. The whole display system can operate from a single supply as low as 3V or as high as 25V.

The IC contains an adjustable voltage reference and an accurate ten-step voltage divider. The high-impedance input buffer accepts signals down to ground and up to within 1.5V of the positive supply. Further, it needs no protection against inputs of ±35V. The input buffer drives 10 individual comparators referenced to the precision divider. Accuracy is typically better than 1 dB.

The LM3915's 3 dB/step display is suited for signals with wide dynamic range, such as audio level, power, light intensity or vibration. Audio applications include average or peak level indicators, power meters and RF signal strength meters. Replacing conventional meters with an LED bar graph results in a faster responding, more rugged display with high visibility that retains the ease of interpretation of an analog display.

The LM3915 is extremely easy to apply. A 1.2V full-scale meter requires only one resistor in addition to the ten LEDs. One more resistor programs the full-scale anywhere from 1.2V to 12V independent of supply voltage. LED brightness is easily controlled with a single pot.

The LM3915 is very versatile. The outputs can drive LCDs, vacuum fluorescents and incandescent bulbs as well as LEDs of any color. Multiple devices can be cascaded for a dot or bar mode display with a range of 60 or 90 dB. LM3915s can also be cascaded with LM3914s for a linear/log display or with LM3916s for an extended-range VU meter.

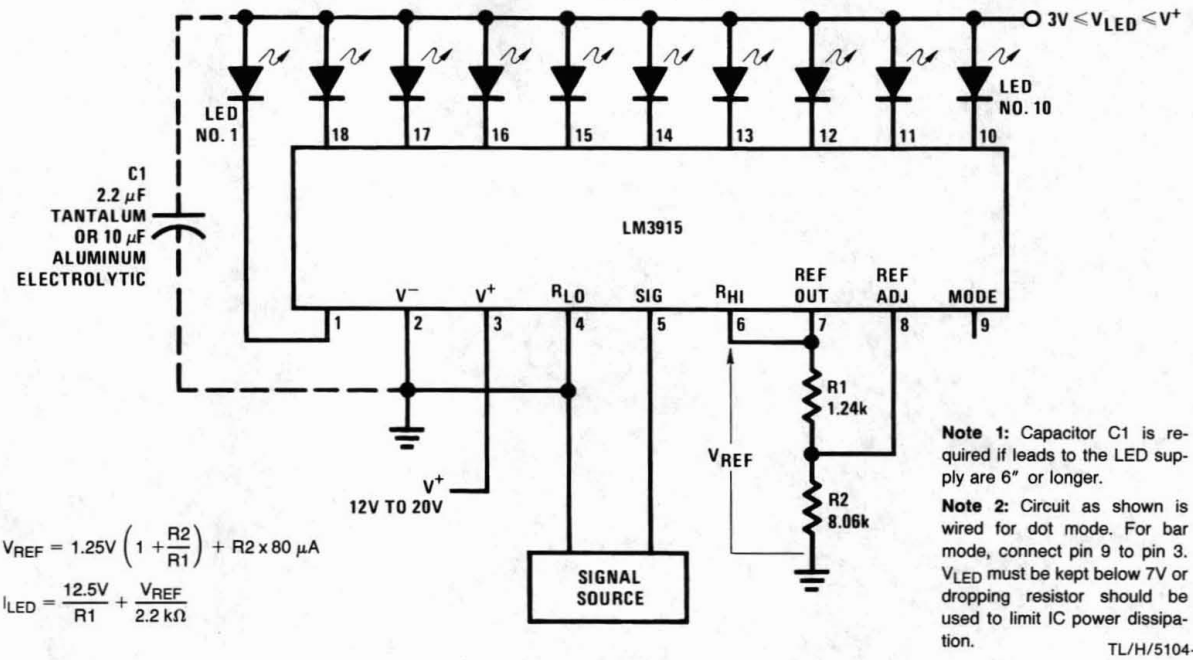
Features

- 3 dB/step, 30 dB range
- Drives LEDs, LCDs, or vacuum fluorescents
- Bar or dot display mode externally selectable by user
- Expandable to displays of 90 dB
- Internal voltage reference from 1.2V to 12V
- Operates with single supply of 3V to 25V
- Inputs operate down to ground
- Output current programmable from 1 mA to 30 mA
- Input withstands ±35V without damage or false outputs
- Outputs are current regulated, open collectors
- Directly drives TTL or CMOS
- The internal 10-step divider is floating and can be referenced to a wide range of voltages

The LM3915 is rated for operation from 0°C to +70°C. The LM3915N is available in an 18-lead molded DIP package.

Typical Applications

0V to 10V Log Display



$$V_{REF} = 1.25V\left(1 + \frac{R2}{R1}\right) + R2 \times 80\ \mu A$$

$$I_{LED} = \frac{12.5V}{R1} + \frac{V_{REF}}{2.2\ k\Omega}$$

Note 1: Capacitor C1 is required if leads to the LED supply are 6" or longer.

Note 2: Circuit as shown is wired for dot mode. For bar mode, connect pin 9 to pin 3. V_{LED} must be kept below 7V or dropping resistor should be used to limit IC power dissipation.

TL/H/5104–1

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Power Dissipation (Note 5) Molded DIP(N)	1365 mW
Supply Voltage	25V
Voltage on Output Drivers	25V
Input Signal Overvoltage (Note 3)	±35V
Divider Voltage	−100 mV to V^+
Reference Load Current	10 mA
Storage Temperature Range	−55°C to +150°C
Lead Temperature (Soldering, 10 sec.)	260°C

Electrical Characteristics (Notes 1 and 3)

Parameter	Conditions (Note 1)	Min	Typ	Max	Units
Comparators					
Offset Voltage, Buffer and First Comparator	$0V \le V_{RLO} = V_{RHI} \le 12V$, $I_{LED} = 1$ mA		3	10	mV
Offset Voltage, Buffer and Any Other Comparator	$0V \le V_{RLO} = V_{RHI} \le 12V$, $I_{LED} = 1$ mA		3	15	mV
Gain ($\Delta I_{LED}/\Delta V_{IN}$)	$I_{L(REF)} = 2$ mA, $I_{LED} = 10$ mA	3	8		mA/mV
Input Bias Current (at Pin 5)	$0V \le V_{IN} \le (V^+ - 1.5V)$		25	100	nA
Input Signal Overvoltage	No Change in Display	−35		35	V
Voltage-Divider					
Divider Resistance	Total, Pin 6 to 4	16	28	36	kΩ
Relative Accuracy (Input Change Between Any Two Threshold Points)	(Note 2)	2.0	3.0	4.0	dB
Absolute Accuracy at Each Threshold Point	(Note 2)				
	$V_{IN} = -3, -6$ dB	−0.5		+0.5	dB
	$V_{IN} = -9$ dB	−0.5		+0.65	dB
	$V_{IN} = -12, -15, -18$ dB	−0.5		+1.0	dB
	$V_{IH} = -21, -24, -27$ dB	−0.5		+1.5	dB
Voltage Reference					
Output Voltage	$0.1\text{ mA} \le I_{L(REF)} \le 4$ mA, $V^+ = V_{LED} = 5V$	1.2	1.28	1.34	V
Line Regulation	$3V \le V^+ \le 18V$		0.01	0.03	%/V
Load Regulation	$0.1\text{ mA} \le I_{L(REF)} \le 4$ mA, $V^+ = V_{LED} = 5V$		0.4	2	%
Output Voltage Change with Temperature	$0°C \le T_A \le +70°C$, $I_{L(REF)} = 1$ mA, $V^+ = V_{LED}$ 5V		1		%
Adjust Pin Current			75	120	μA

Electrical Characteristics (Note 1) (Continued)

Parameter	Conditions (Note 1)	Min	Typ	Max	Units
Output Drivers					
LED Current	$V^+ = V_{LED} = 5V$, $I_{L(REF)} = 1$ mA	7	10	13	mA
LED Current Difference (Between Largest and Smallest LED Currents)	$V_{LED} = 5V$, $I_{LED} = 2$ mA		0.12	0.4	mA
	$V_{LED} = 5V$, I_{LED} 20 mA		1.2	3	mA
LED Current Regulation	$2V \le V_{LED} \le 17V$, $I_{LED} = 2$ mA		0.1	0.25	mA
	$I_{LED} = 20$ mA		1	3	mA
Dropout Voltage	$I_{LED(ON)} = 20$ mA @ $V_{LED} = 5V$, $\Delta I_{LED} = 2$ mA			1.5	V
Saturation Voltage	$I_{LED} = 2.0$ mA, $I_{L(REF)} = 0.4$ mA		0.15	0.4	V
Output Leakage, Each Collector	Bar Mode (Note 4)		0.1	10	μA
Output Leakage	Dot Mode (Note 4)				
Pins 10-18			0.1	10	μA
Pin 1		60	150	450	μA
Supply Current					
Standby Supply Current (All Outputs Off)	$V^+ = +5V$, $I_{L(REF)} = 0.2$ mA		2.4	4.2	mA
	$V^+ = +20V$, $I_{L(REF)} = 1.0$ mA		6.1	9.2	mA

Note 1: Unless otherwise stated, all specifications apply with the following conditions:

$3\ V_{DC} \le V^+ \le 20\ V_{DC}$ $\quad -0.015V \le V_{RLO} \le 12\ V_{DC}$ $\quad T_A = 25°C$, $I_{L(REF)} = 0.2$ mA, pin 9 connected to pin 3 (bar mode).

$3\ V_{DC} \le V_{LED} \le V^+$ $\quad V_{REF}, V_{RHI}, V_{RLO} \le (V^+ - 1.5V)$ For higher power dissipations, pulse testing is used.

$-0.015V \le V_{RHI} \le 12\ V_{DC}$ $\quad 0V \le V_{IN} \le V^+ - 1.5V$

Note 2: Accuracy is measured referred to 0 dB = + 10.000 V_{DC} at pin 5, with + 10.000 V_{DC} at pin 6, and 0.000 V_{DC} at pin 4. At lower full scale voltages, buffer and comparator offset voltage may add significant error. See table for threshold voltages.

Note 3: Pin 5 input current must be limited to ±3 mA. The addition of a 39k resistor in series with pin 5 allows ±100V signals without damage.

Note 4: Bar mode results when pin 9 is within 20 mV of V^+. Dot mode results when pin 9 is pulled at least 200 mV below V^+. LED #10 (pin 10 output current) is disabled if pin 9 is pulled 0.9V or more below V_{LED}.

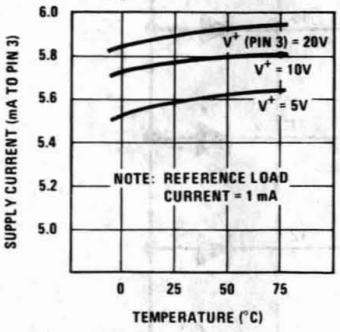
Note 5: The maximum junction temperature of the LM3915 is 100°C. Devices must be derated for operation at elevated temperatures. Junction to ambient thermal resistance is 55°C/W for the molded DIP (N package).

THRESHOLD VOLTAGE (Note 2)

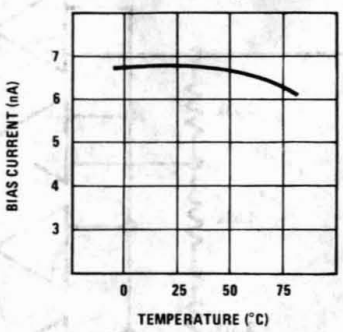
Output	dB	Min	Typ	Max	Output	dB	Min	Typ	Max
1	−27	0.422	0.447	0.531	6	−12	2.372	2.512	2.819
2	−24	0.596	0.631	0.750	7	−9	3.350	3.548	3.825
3	−21	0.841	0.891	1.059	8	−6	4.732	5.012	5.309
4	−18	1.189	1.259	1.413	9	−3	6.683	7.079	7.498
5	−15	1.679	1.778	1.995	10	0	9.985	10	10.015

Typical Performance Characteristics

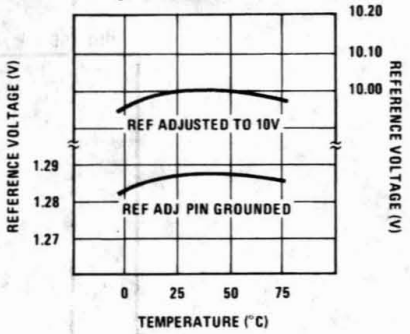
Supply Current vs Temperature



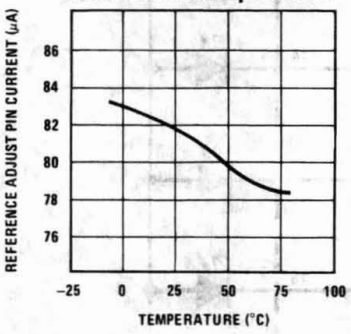
Operating Input Bias Current vs Temperature



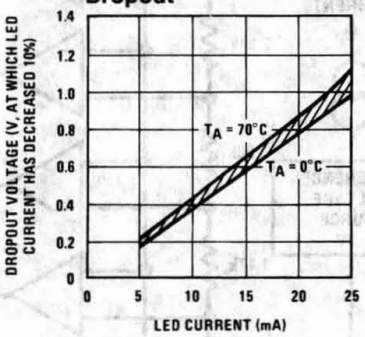
Reference Voltage vs Temperature



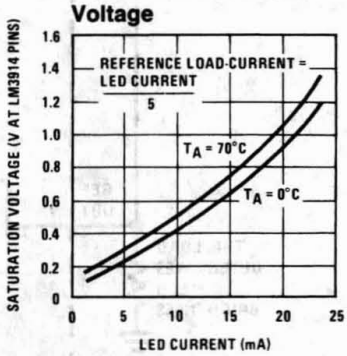
Reference Adjust Pin Current vs Temperature



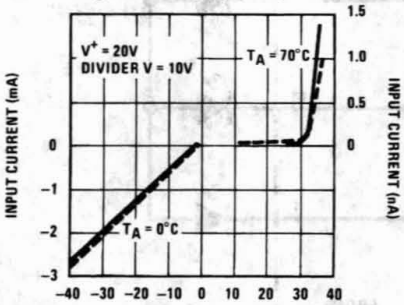
LED Current-Regulation Dropout



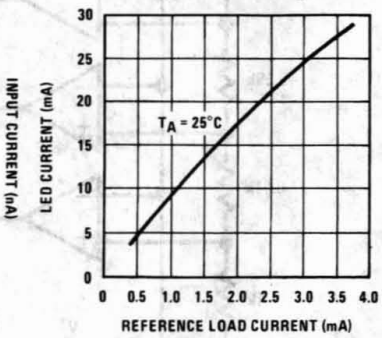
LED Driver Saturation Voltage



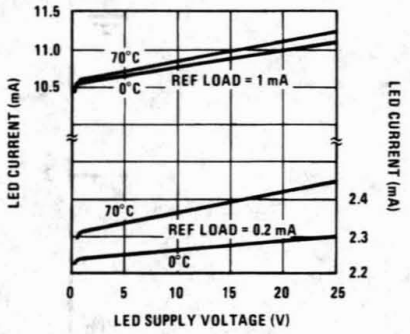
Input Current Beyond Signal Range (Pin 5)



LED Current vs Reference Loading



LED Driver Current Regulation



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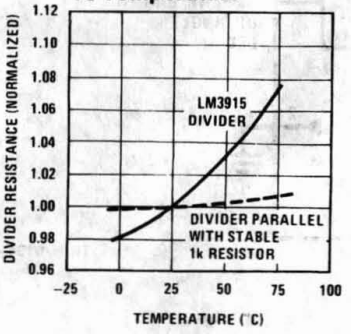
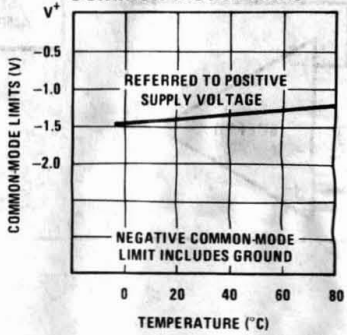
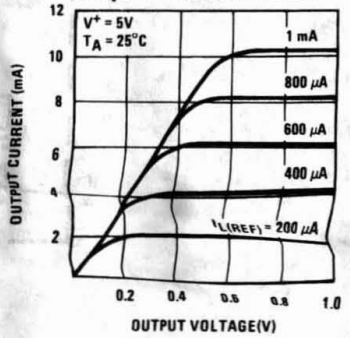
Total Divider Resistance vs Temperature



Common-Mode Limits



Output Characteristics



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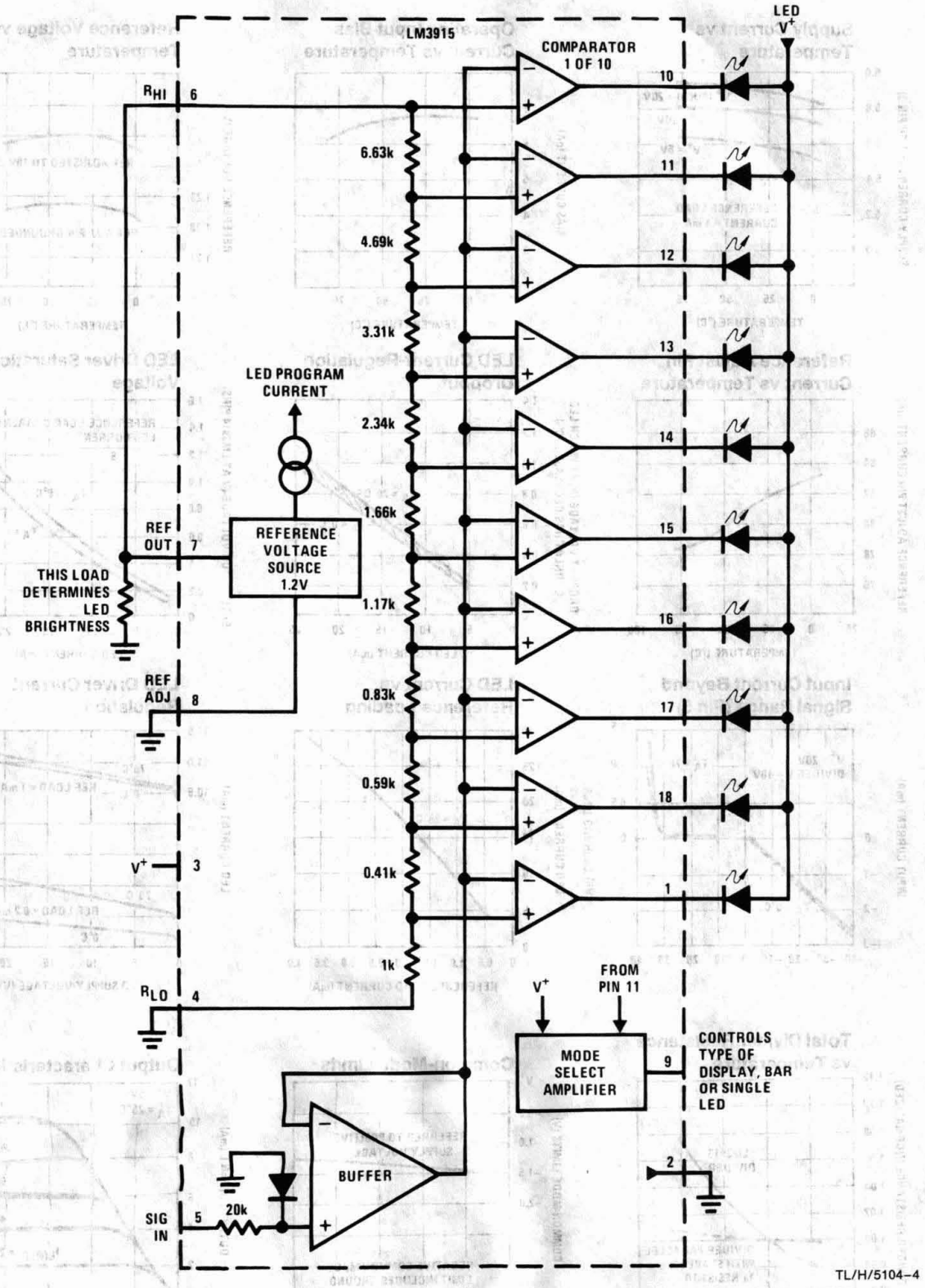
Block Diagram (Showing Simplest Application)



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Functional Description

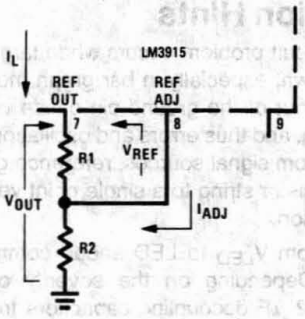
The simplified LM3915 block diagram is included to give the general idea of the circuit's operation. A high input impedance buffer operates with signals from ground to 12V, and is protected against reverse and overvoltage signals. The signal is then applied to a series of 10 comparators; each of which is biased to a different comparison level by the resistor string.

In the example illustrated, the resistor string is connected to the internal 1.25V reference voltage. In this case, for each 3 dB that the input signal increases, a comparator will switch on another indicating LED. This resistor divider can be connected between any 2 voltages, providing that they are at least 1.5V below V^+ and no lower than V^-.

INTERNAL VOLTAGE REFERENCE

The reference is designed to be adjustable and develops a nominal 1.25V between the REF OUT (pin 7) and REF ADJ (pin 8) terminals. The reference voltage is impressed across program resistor R1 and, since the voltage is constant, a constant current I_1 then flows through the output set resistor R2 giving an output voltage of:

$$V_{OUT} = V_{REF}\left(1 + \frac{R2}{R1}\right) + I_{ADJ}\,R2$$



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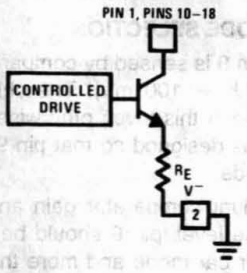
Since the 120 μA current (max) from the adjust terminal represents an error term, the reference was designed to minimize changes of this current with V^+ and load changes. For correct operation, reference load current should be between 80 μA and 5 mA. Load capacitance should be less than 0.05 μF.

CURRENT PROGRAMMING

A feature not completely illustrated by the block diagram is the LED brightness control. The current drawn out of the reference voltage pin (pin 7) determines LED current. Approximately 10 times this current will be drawn through each lighted LED, and this current will be relatively constant despite supply voltage and temperature changes. Current drawn by the internal 10-resistor divider, as well as by the external current and voltage-setting divider should be included in calculating LED drive current. The ability to modulate LED brightness with time, or in proportion to input voltage and other signals can lead to a number of novel displays or ways of indicating input overvoltages, alarms, etc.

The LM3915 outputs are current-limited NPN transistors as shown below. An internal feedback loop regulates the transistor drive. Output current is held at about 10 times the reference load current, independent of output voltage and processing variables, as long as the transistor is not saturated.

LM3915 Output Circuit



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Outputs may be run in saturation with no adverse effects, making it possible to directly drive logic. The effective saturation resistance of the output transistors, equal to R_E plus the transistors' collector resistance, is about 50Ω. It's also possible to drive LEDs from rectified AC with no filtering. To avoid oscillations, the LED supply should be bypassed with a 2.2 μF tantalum or 10 μF aluminum electrolytic capacitor.

MODE PIN USE

Pin 9, the Mode Select input, permits chaining of multiple LM3915s, and controls bar or dot mode operation. The following tabulation shows the basic ways of using this input. Other more complex uses will be illustrated in the applications.

Bar Graph Display: Wire Mode Select (pin 9) *directly* to pin 3 (V^+ pin).

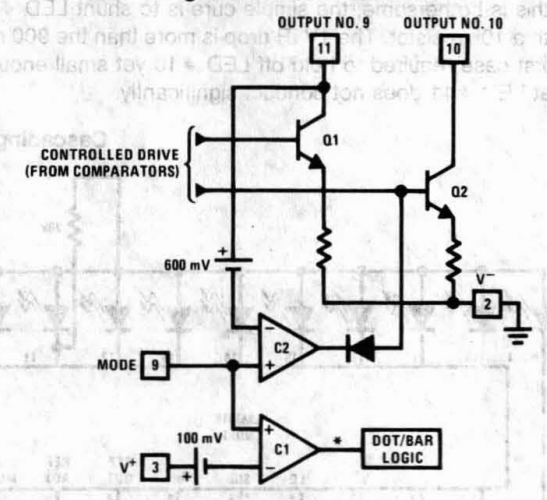
Dot Display, Single LM3915 Driver: Leave the Mode Select pin open circuit.

Dot Display, 20 or More LEDs: Connect pin 9 of the *first* driver in the series (i.e., the one with the lowest input voltage comparison points) to pin 1 of the next higher LM3915 driver. Continue connecting pin 9 of lower input drivers to pin 1 of higher input drivers for 30 or more LED displays. The last LM3915 driver in the chain will have pin 9 left open. All previous drivers should have a 20k resistor in parallel with LED #9 (pin 11 to V_{LED}).

Mode Pin Functional Description

This pin actually performs two functions. Refer to the simplified block diagram below.

Block Diagram of Mode Pin Function



*High for bar

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Mode Pin Functional Description
(Continued)

DOT OR BAR MODE SELECTION

The voltage at pin 9 is sensed by comparator C1, nominally referenced to (V^+ − 100 mV). The chip is in bar mode when pin 9 is above this level; otherwise it's in dot mode. The comparator is designed so that pin 9 can be left open circuit for dot mode.

Taking into account comparator gain and variation in the 100 mV reference level, pin 9 should be no more than 20 mV below V^+ for bar mode and more than 200 mV below V^+ (or open circuit) for dot mode. In most applications, pin 9 is either open (dot mode) or tied to V^+ (bar mode). In bar mode, pin 9 should be connected directly to pin 3. Large currents drawn from the power supply (LED current, for example) should not share this path so that large IR drops are avoided.

DOT MODE CARRY

In order for the display to make sense when multiple LM3915s are cascaded in dot mode, special circuitry has been included to shut off LED #10 of the first device when LED #1 of the second device comes on. The connection for cascading in dot mode has already been described and is depicted below.

As long as the input signal voltage is below the threshold of the second LM3915, LED #11 is off. Pin 9 of LM3915 #1 thus sees effectively an open circuit so the chip is in dot mode. As soon as the input voltage reaches the threshold of LED #11, pin 9 of LM3915 #1 is pulled an LED drop (1.5V or more) below V_{LED}. This condition is sensed by comparator C2, referenced 600 mV below V_{LED}. This forces the output of C2 low, which shuts off output transistor Q2, extinguishing LED #10.

V_{LED} is sensed via the 20k resistor connected to pin 11. The very small current (less than 100 μA) that is diverted from LED #9 does not noticeably affect its intensity.

An auxiliary current source at pin 1 keeps at least 100 μA flowing through LED #11 even if the input voltage rises high enough to extinguish the LED. This ensures that pin 9 of LM3915 #1 is held low enough to force LED #10 off when *any* higher LED is illuminated. While 100 μA does not normally produce significant LED illumination, it may be noticeable when using high-efficiency LEDs in a dark environment. If this is bothersome, the simple cure is to shunt LED #11 with a 10k resistor. The 1V IR drop is more than the 900 mV worst case required to hold off LED #10 yet small enough that LED #11 does not conduct significantly.

OTHER DEVICE CHARACTERISTICS

The LM3916 is relatively low-powered itself, and since any number of LEDs can be powered from about 3V, it is a very efficient display driver. Typical standby supply current (all LEDs OFF) is 1.6 mA. However, any reference loading adds 4 times that current drain to the V^+ (pin 3) supply input. For example, an LM3916 with a 1 mA reference pin load (1.3k) would supply almost 10 mA to every LED while drawing only 10 mA from its V^+ pin supply. At full-scale, the IC is typically drawing less than 10% of the current supplied to the display.

The display driver does not have built-in hysteresis so that the display does not jump instantly from one LED to the next. Under rapidly changing signal conditions, this cuts down high frequency noise and often an annoying flicker. An "overlap" is built in so that at no time are all segments completely off in the dot mode. Generally 1 LED fades in while the other fades out over a mV or more of range. The change may be much more rapid between LED #10 of one device and LED #1 of a *second* device "chained" to the first.

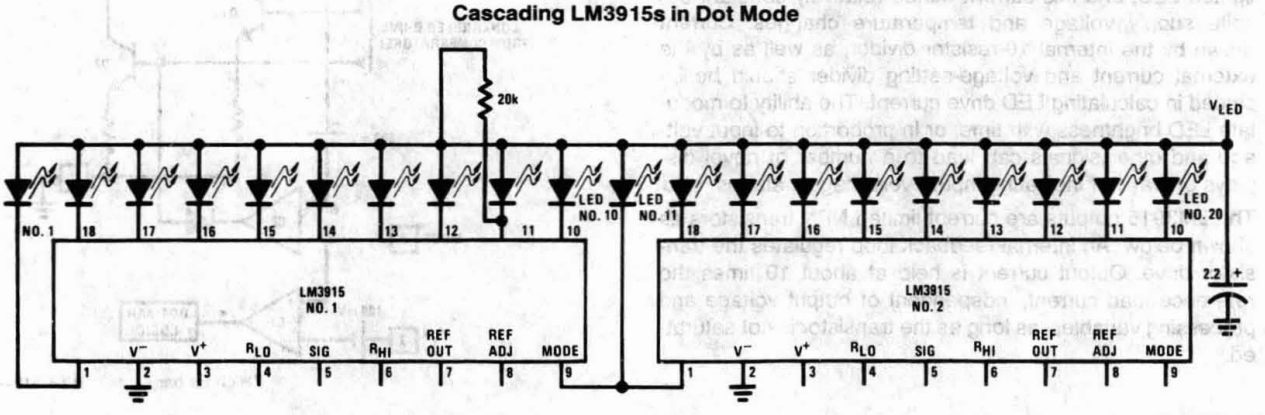
Application Hints

The most difficult problem occurs when large LED currents are being drawn, especially in bar graph mode. These currents flowing out of the ground pin cause voltage drops in external wiring, and thus errors and oscillations. Bringing the return wires from signal sources, reference ground and bottom of the resistor string to a single point very near pin 2 is the best solution.

Long wires from V_{LED} to LED anode common can cause oscillations. Depending on the severity of the problem 0.05 μF to 2.2 μF decoupling capacitors from LED anode common to pin 2 will damp the circuit. If LED anode line wiring is inaccessible, often similar decoupling from pin 1 to pin 2 will be sufficient.

If LED turn ON seems slow (bar mode) or several LEDs light (dot mode), oscillation or excessive noise is usually the problem. In cases where proper wiring and bypassing fail to stop oscillations, V^+ voltage at pin 3 is usually below suggested limits. Expanded scale meter applications may have one or both ends of the internal voltage divider terminated at relatively high value resistors. These high-impedance ends should be bypassed to pin 2 with at least a 0.001 μF capacitor, or up to 0.1 μF in noisy environments.

Cascading LM3915s in Dot Mode



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Application Hints (Continued)

Power dissipation, especially in bar mode should be given consideration. For example, with a 5V supply and all LEDs programmed to 20 mA the driver will dissipate over 600 mW. In this case a 7.5Ω resistor in series with the LED supply will cut device heating in half. The negative end of the resistor should be bypassed with a 2.2 μF solid tantalum capacitor to pin 2.

TIPS ON RECTIFIER CIRCUITS

The simplest way to display an AC signal using the LM3915 is to apply it right to pin 5 unrectified. Since the LED illuminated represents the instantaneous value of the AC waveform, one can readily discern both peak and average values of audio signals in this manner. The LM3915 will respond to positive half-cycles only but will not be damaged by signals up to ±35V (or up to ±100V if a 39k resistor is in series with the input). It's recommended to use dot mode and to run the LEDs at 30 mA for high enough average intensity.

True average or peak detection requires rectification. If an LM3915 is set up with 10V full scale across its voltage divider, the turn-on point for the first LED is only 450 mV. A simple silicon diode rectifier won't work well at the low end due to the 600 mV diode threshold. The half-wave peak detector in *Figure 1* uses a PNP emitter-follower in front of the diode. Now, the transistor's base-emitter voltage cancels out the diode offset, within about 100 mV. This approach is usually satisfactory when a single LM3915 is used for a 30 dB display.

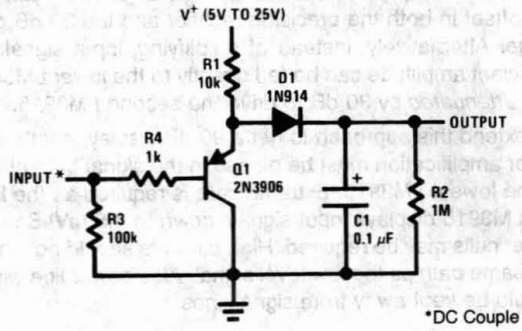
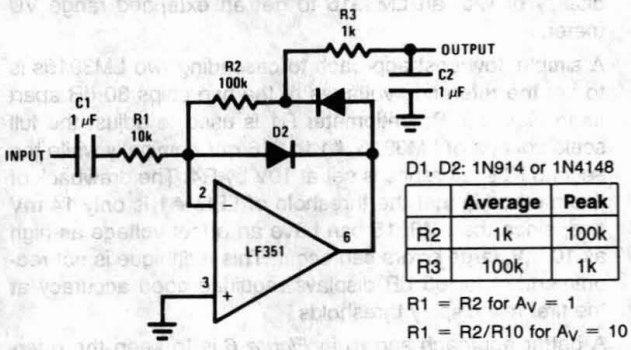


FIGURE 1. Half-Wave Peak Detector

Display circuits using two or more LM3915s for a dynamic range of 60 dB or greater require more accurate detection. In the precision half-wave rectifier of *Figure 2* the effective diode offset is reduced by a factor equal to the open-loop gain of the op amp. Filter capacitor C2 charges through R3 and discharges through R2 and R3, so that appropriate selection of these values results in either a peak or an average detector. The circuit has a gain equal to R2/R1.

It's best to capacitively couple the input. Audio sources frequently have a small DC offset that can cause significant error at the low end of the log display. Op amps that slew quickly, such as the LF351, LF353, or LF356, are needed to faithfully respond to sudden transients. It may be necessary to trim out the op amp DC offset voltage to accurately cover a 60 dB range. Best results are obtained if the circuit is adjusted for the correct output when a low-level AC signal (10 to 20 mV) is applied, rather than adjusting for zero output with zero input.

For precision full-wave averaging use the circuit in *Figure 3*. Using 1% resistors for R1 through R4, gain for positive and negative signal differs by only 0.5 dB worst case. Substituting 5% resistors increases this to 2 dB worst case. (A 2 dB gain difference means that the display may have a ±1 dB error when the input is a nonsymmetrical transient). The averaging time constant is R5–C2. A simple modification results in the precision full-wave detector of *Figure 4*. Since the filter capacitor is not buffered, this circuit can drive only high impedance loads such as the input of an LM3915.



	Average	Peak
R2	1k	100k
R3	100k	1k

FIGURE 2. Precision Half-Wave Rectifier

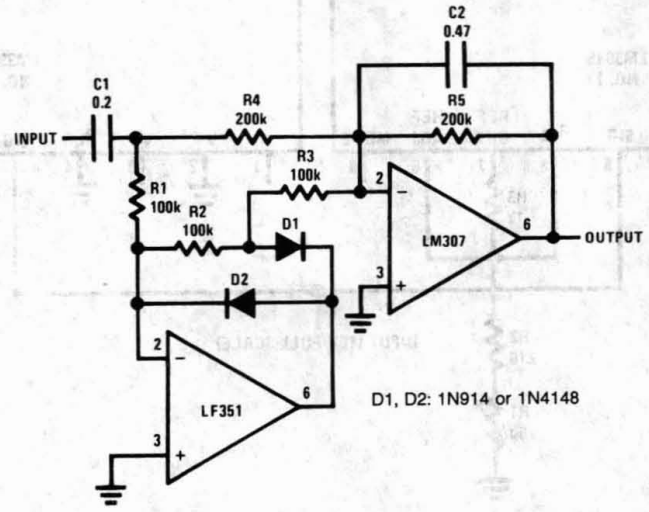


FIGURE 3. Precision Full-Wave Average Detector

Application Hints (Continued)

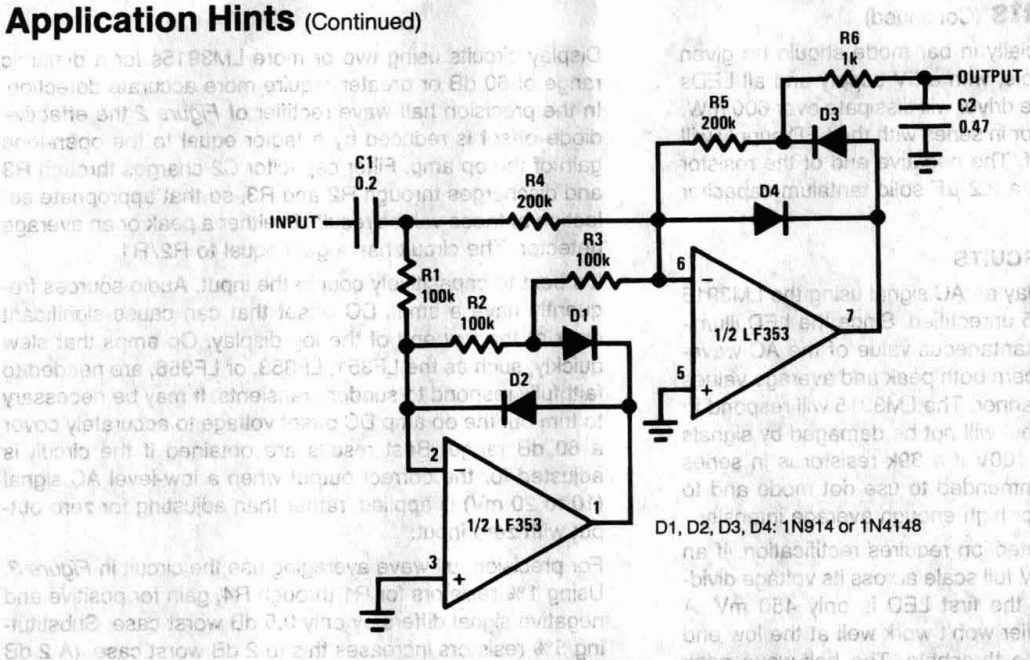


FIGURE 4. Precision Full-Wave Peak Detector

CASCADING THE LM3915

To display signals of 60 or 90 dB dynamic range, multiple LM3915s can be easily cascaded. Alternatively, it is possible to cascade an LM3915 with LM3914s for a log/linear display or with an LM3916 to get an extended range VU meter.

A simple, low cost approach to cascading two LM3915s is to set the reference voltages of the two chips 30 dB apart as in *Figure 5*. Potentiometer R1 is used to adjust the full scale voltage of LM3915 #1 to 316 mV nominally while the second IC's reference is set at 10V by R4. The drawback of this method is that the threshold of LED #1 is only 14 mV and, since the LM3915 can have an offset voltage as high as 10 mV, large errors can occur. This technique is not recommended for 60 dB displays requiring good accuracy at the first few display thresholds.

A better approach shown in *Figure 6* is to keep the reference at 10V for both LM3915s and amplify the input signal to the lower LM3915 by 30 dB. Since two 1% resistors can set the amplifier gain within ±0.2 dB, a gain trim is unnecessary. However, an op amp offset voltage of 5 mV will shift the first LED threshold as much as 4 dB, so that an offset trim may be required. Note that a single adjustment can null out offset in both the precision rectifier and the 30 dB gain stage. Alternatively, instead of amplifying, input signals of sufficient amplitude can be fed directly to the lower LM3915 and *attenuated* by 30 dB to drive the second LM3915.

To extend this approach to get a 90 dB display, another 30 dB of amplification must be placed in the signal path ahead of the lowest LM3915. Extreme care is required as the lowest LM3915 displays input signals down to 0.5 mV! Several offset nulls may be required. High currents should not share the same path as the low level signal. Also power line wiring should be kept away from signal lines.

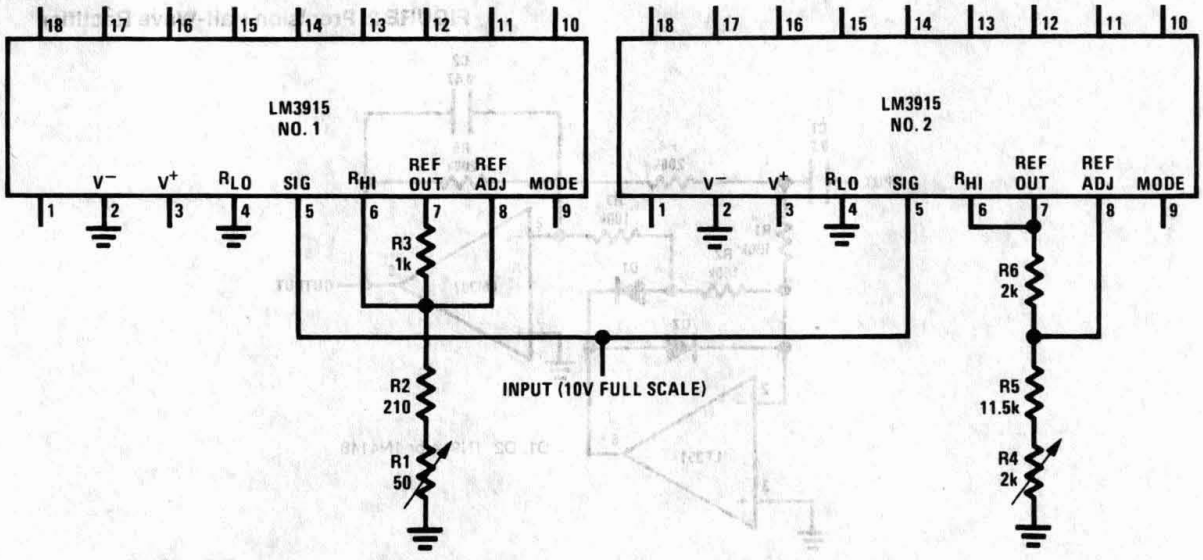


FIGURE 5. Low Cost Circuit for 60 dB Display

Application Hints (Continued)

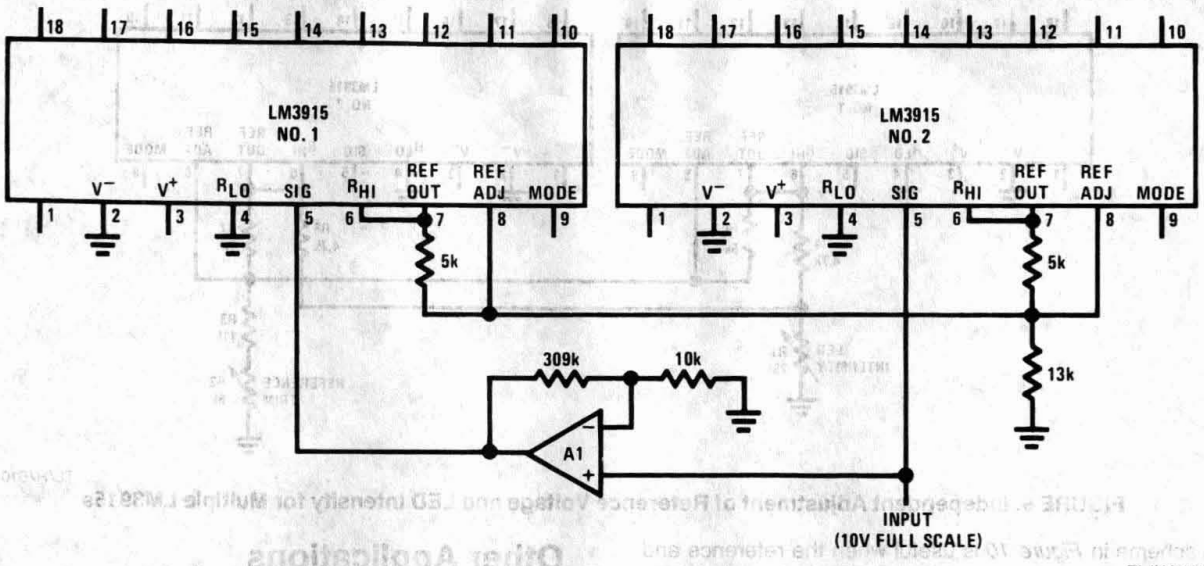


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FIGURE 6. Improved Circuit for 60 dB Display

TIPS ON REFERENCE VOLTAGE AND LED CURRENT PROGRAMMING

SINGLE LM3915

The equations in *Figure 7* illustrate how to choose resistor values to set reference voltage for the simple case where no LED intensity adjustment is required. A LED current of 10 mA to 20 mA generally produces adequate illumination. Having 10V full-scale across the internal voltage divider gives best accuracy by keeping signal level high relative to the offset voltage of the internal comparators. However, this causes 450 μA to flow from pin 7 into the divider which means that the LED current will be at least 5 mA. R1 will typically be between 1 kΩ and 2 kΩ. To trim the reference voltage, vary R2.

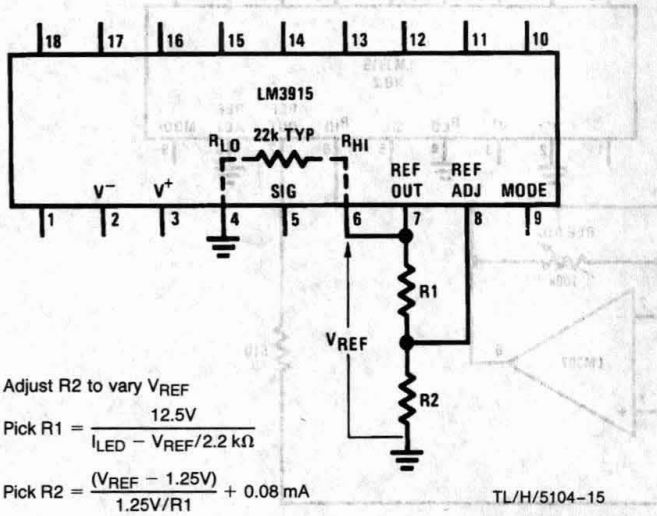
LM3915
18 17 16 15 14 13 12 11 10
RLO 22k TYP RHI
V⁻ V⁺ SIG REF OUT REF ADJ MODE
1 2 3 4 5 6 7 8 9
R1
VREF
R2
Adjust R2 to vary VREF
Pick R1 = 12.5V / (ILED − VREF/2.2 kΩ)
Pick R2 = (VREF − 1.25V) / 1.25V/R1 + 0.08 mA

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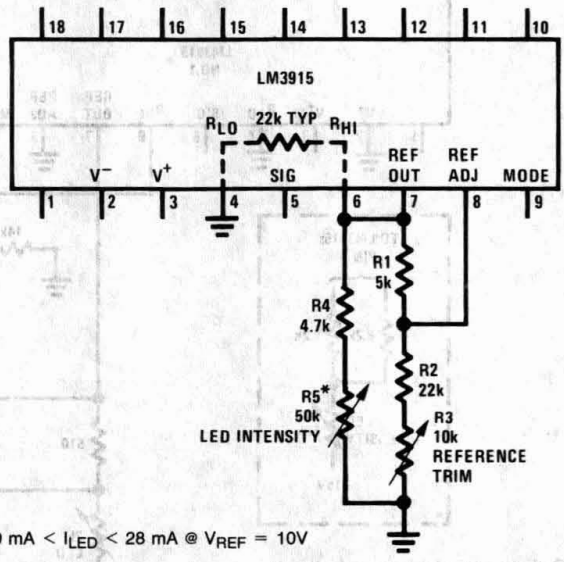
FIGURE 7. Design Equations for Fixed LED Intensity

The circuit in *Figure 8* shows how to add a LED intensity control which can vary LED current from 9 mA to 28 mA. The reference adjustment has some effect on LED intensity but the reverse is not true.

MULTIPLE LM3915s

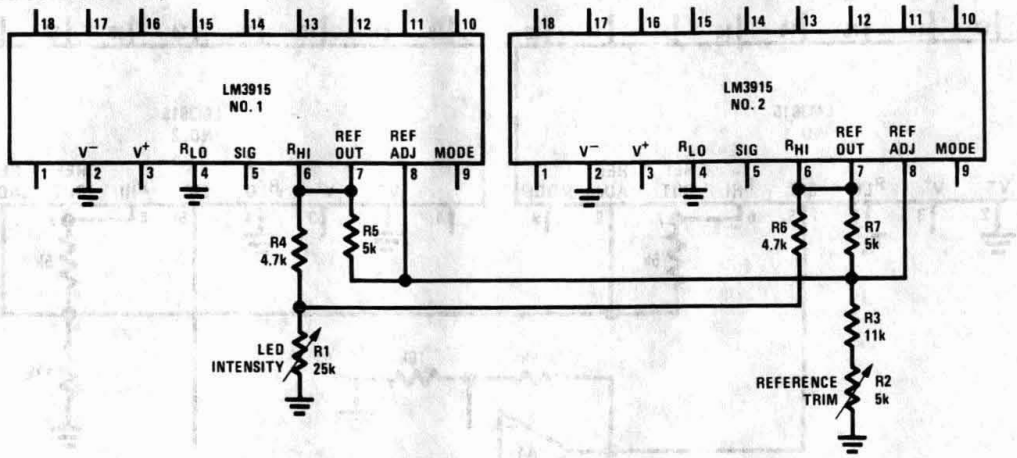
Figure 9 shows how to obtain a common reference trim and intensity control for two LM3915s. The two ICs may be connected in cascade for a 60 dB display or may be handling separate channels for stereo. This technique can be extended for larger numbers of LM3915s by varying the values of R1, R2 and R3 in inverse proportion to the number of devices tied in. The ICs' internal references track within 100 mV so that worst case error from chip to chip is only 0.1 dB for V_{REF} = 10V.



TL/H/5104–16

FIGURE 8. Varying LED Intensity

Application Hints (Continued)



TL/H/5104–17

FIGURE 9. Independent Adjustment of Reference Voltage and LED Intensity for Multiple LM3915s

The scheme in *Figure 10* is useful when the reference and LED intensity must be adjusted independently over a wide range. The R_{HI} voltage can be adjusted from 1.2V to 10V with no effect on LED current. Since the internal divider here does not load down the reference, minimum LED current is much lower. At the minimum recommended reference load of 80 μA, LED current is about 0.8 mA. The resistor values shown give a LED current range from 1.5 mA to 20 mA.

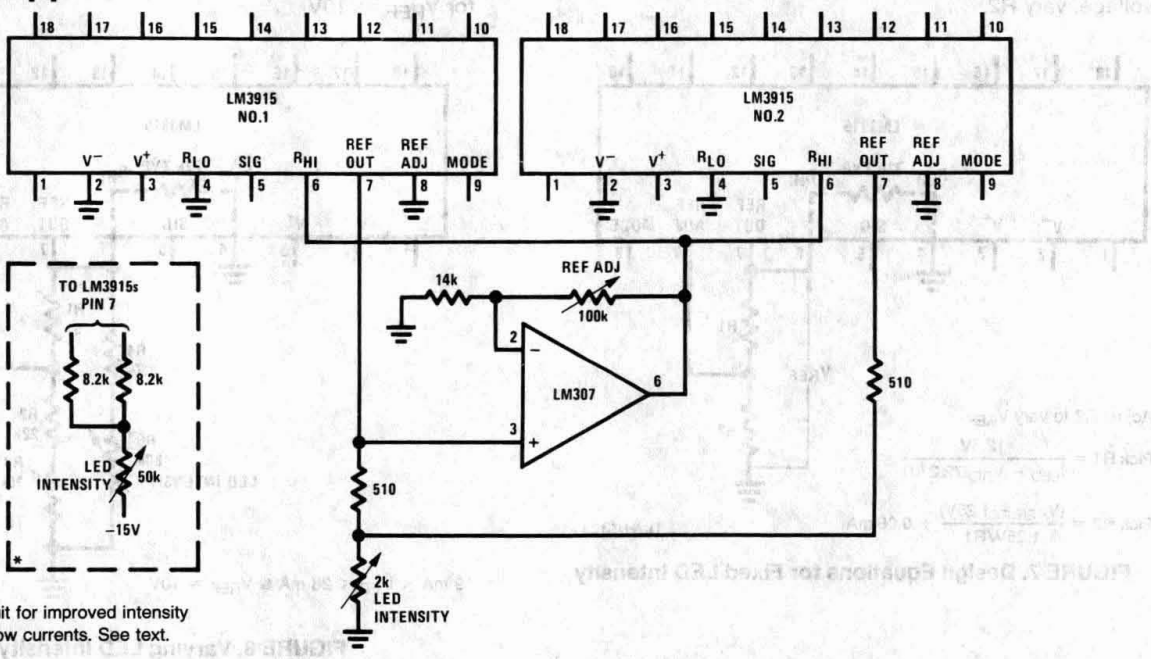
At the low end of the intensity adjustment, the voltage drop across the 510Ω current-sharing resistors is so small that chip to chip variation in reference voltage may yield a visible variation in LED intensity. The optional approach shown of connecting the bottom end of the intensity control pot to a negative supply overcomes this problem by allowing a larger voltage drop across the (larger) current-sharing resistors.

Other Applications

For increased resolution, it's possible to obtain a display with a smooth transition between LEDs. This is accomplished by varying the reference level at pin 6 by 3 dBp-p as shown in *Figure 11*. The signal can be a triangle, sawtooth or sine wave from 60 Hz to 1 kHz. The display can be run in either dot or bar mode.

When an exponentially decaying RC discharge waveform is applied to pin 5, the LM3915's outputs will switch at equal intervals. This makes a simple timer or sequencer. Each time interval is equal to RC/3. The output may be used to drive logic, opto-couplers, relays or PNP transistors, for example.

Typical Applications

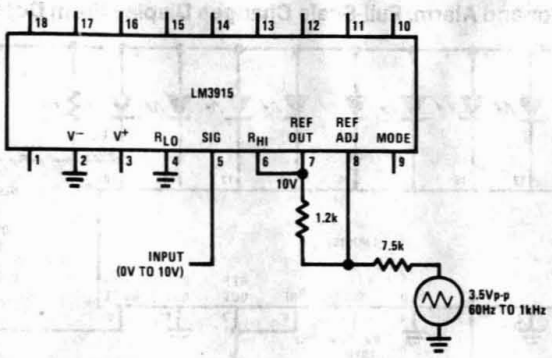


*Optional circuit for improved intensity matching at low currents. See text.

TL/H/5104–18

FIGURE 10. Wide-Range Adjustment of Reference Voltage and LED Intensity for Multiple LM3915s

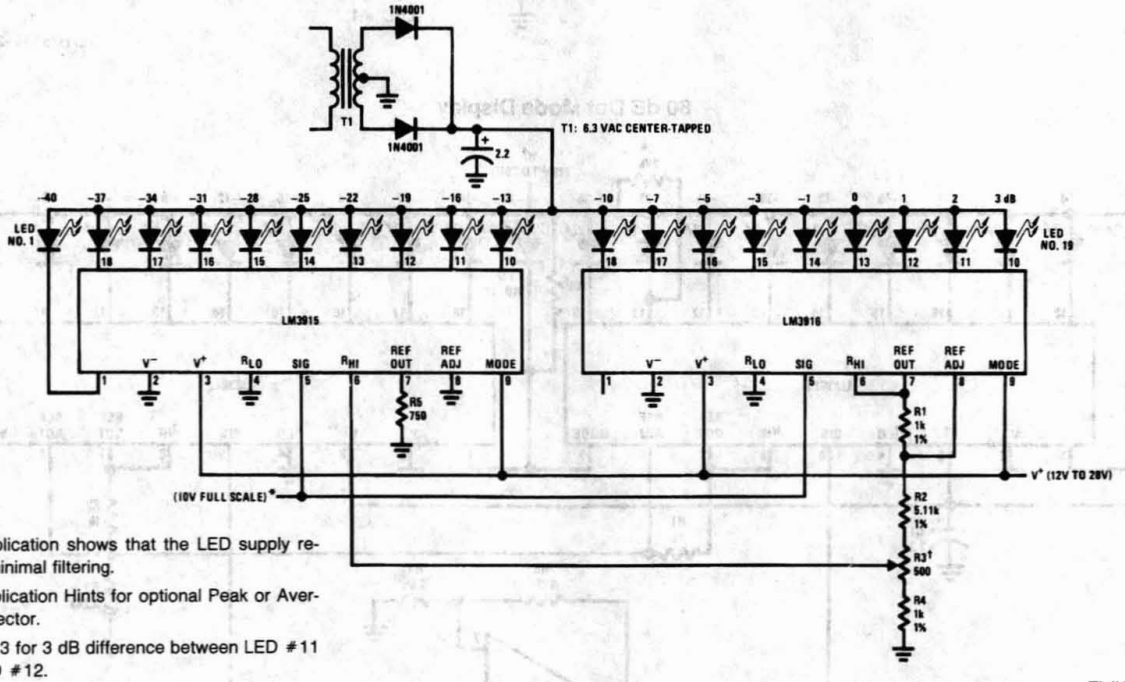
Typical Applications (Continued)



TL/H/5104–19

FIGURE 11. 0V to 10V Log Display with Smooth Transitions

Extended Range VU Meter



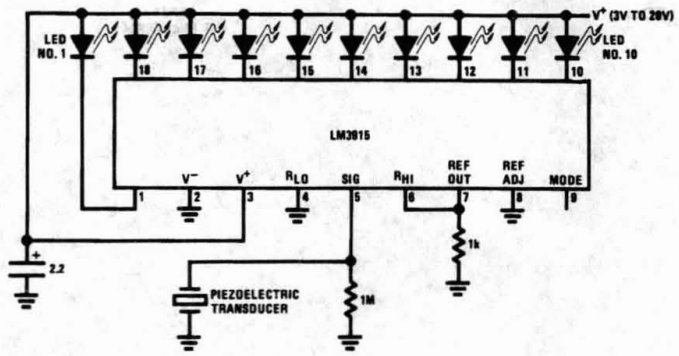
This application shows that the LED supply requires minimal filtering.

*See Application Hints for optional Peak or Average Detector.

†Adjust R3 for 3 dB difference between LED #11 and LED #12.

TL/H/5104–20

Vibration Meter

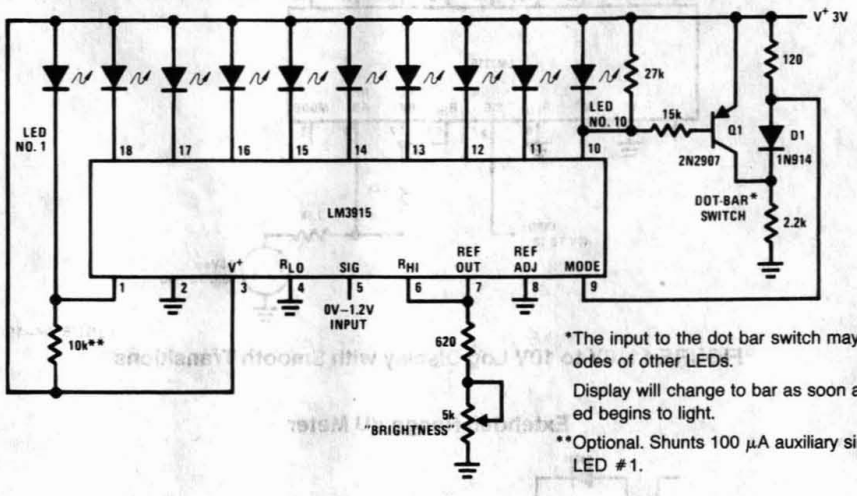


TL/H/5104–21

LED	Threshold
1	60 mV
2	80 mV
3	110 mV
4	160 mV
5	220 mV
6	320 mV
7	440 mV
8	630 mV
9	890 mV
10	1.25V

Typical Applications (Continued)

Indicator and Alarm, Full-Scale Changes Display From Dot to Bar



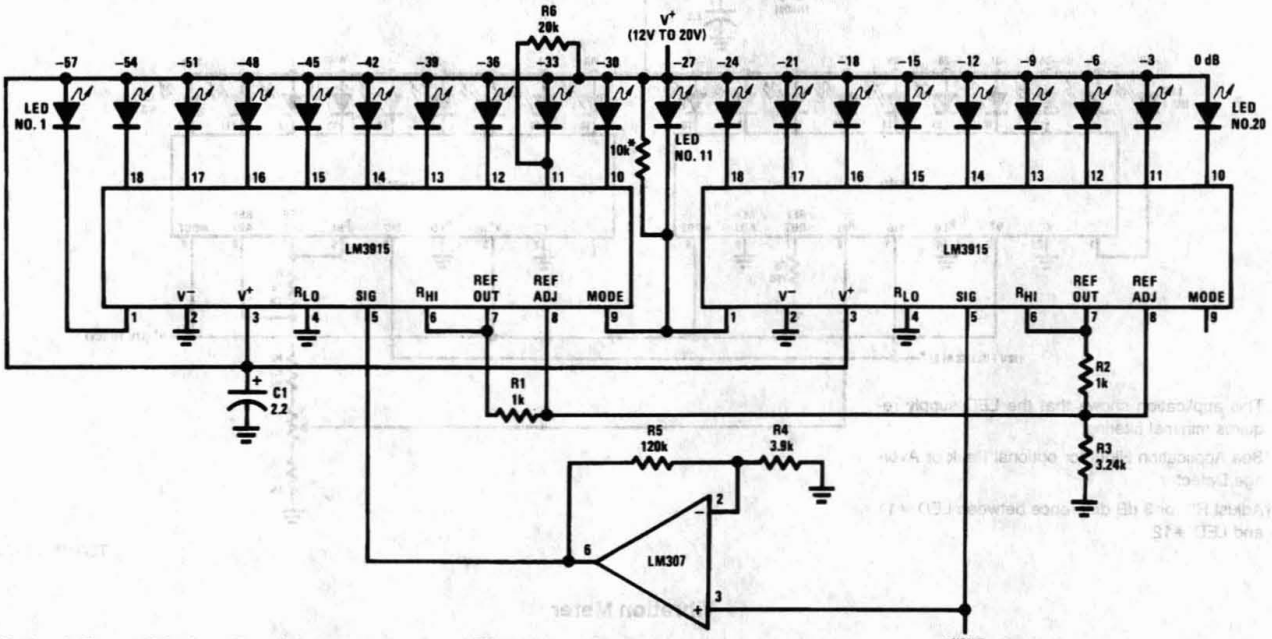
*The input to the dot bar switch may be taken from cathodes of other LEDs.

Display will change to bar as soon as the LED so selected begins to light.

**Optional. Shunts 100 μA auxiliary sink current away from LED #1.

TL/H/5104–22

60 dB Dot Mode Display

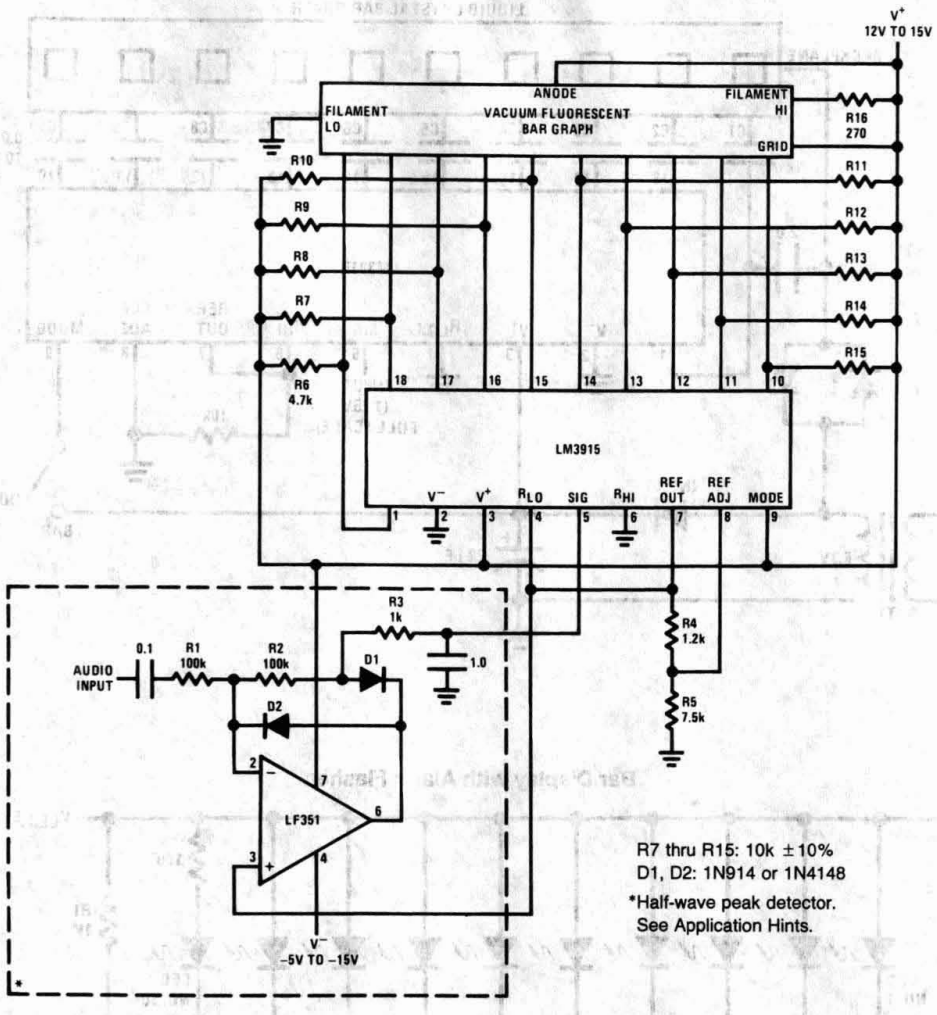


*Optional. Shunts 100 μA auxiliary sink current away from LED #11.

TL/H/5104–23

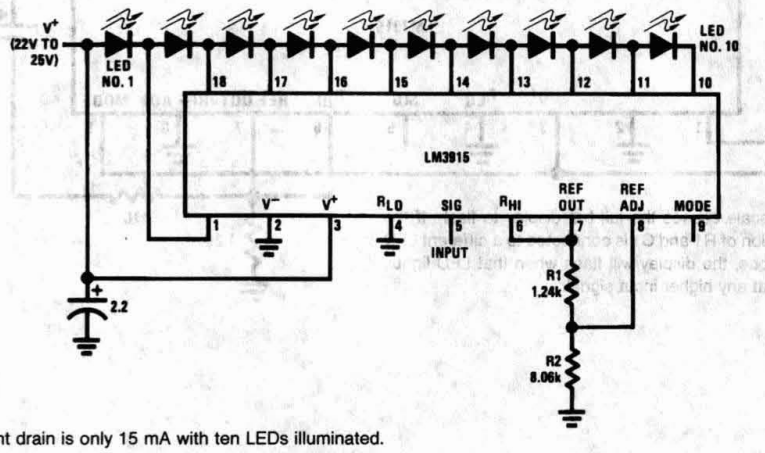
Typical Applications (Continued)

Driving Vacuum Fluorescent Display



TL/H/5104–24

Low Current Bar Mode Display

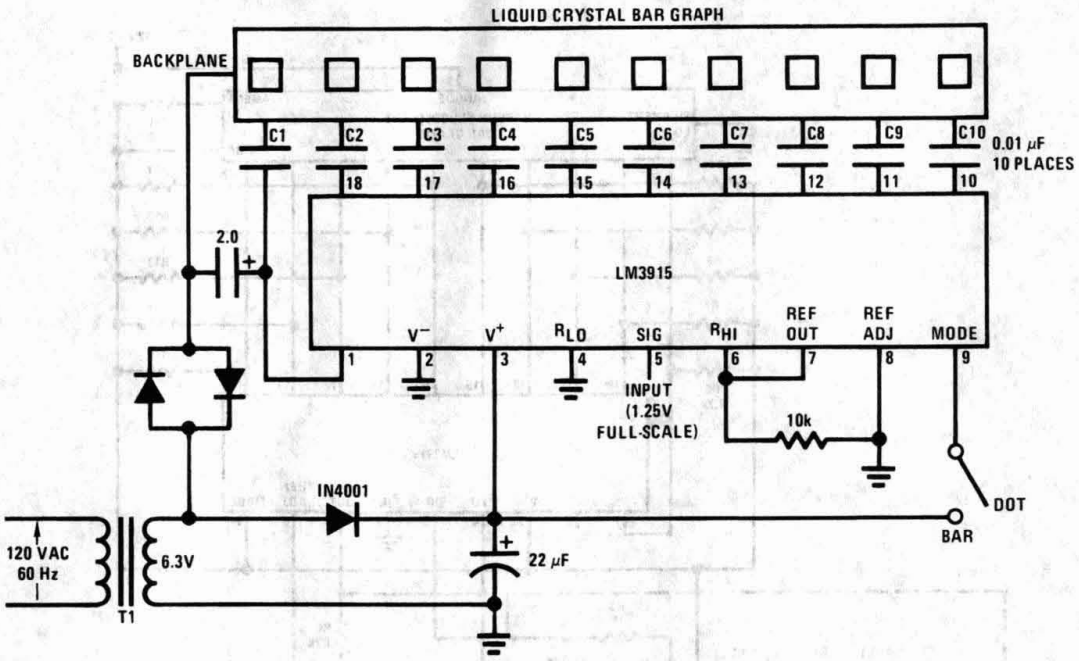


Supply current drain is only 15 mA with ten LEDs illuminated.

TL/H/5104–25

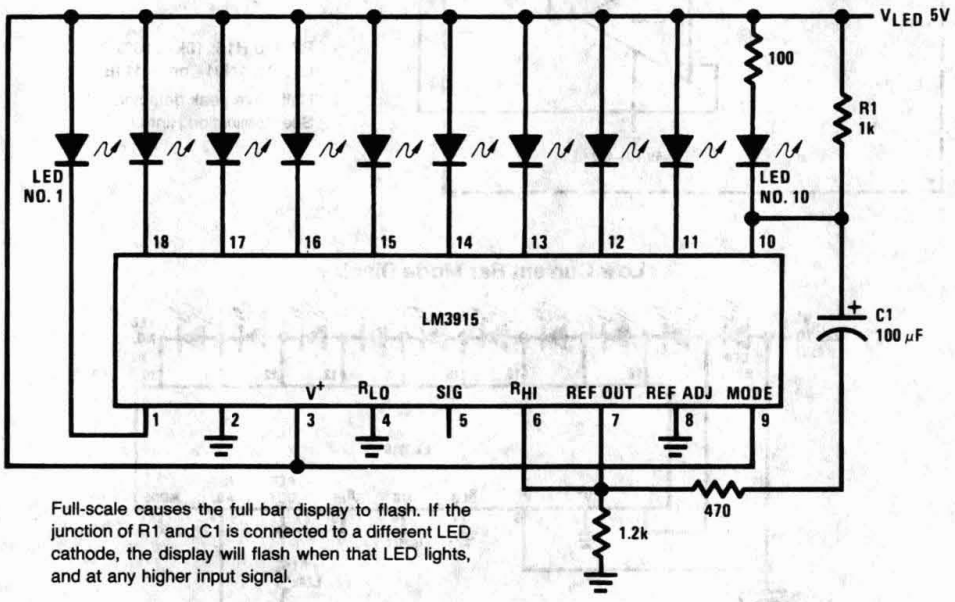
Typical Applications (Continued)

Driving Liquid Crystal Display



TL/H/5104–26

Bar Display with Alarm Flasher

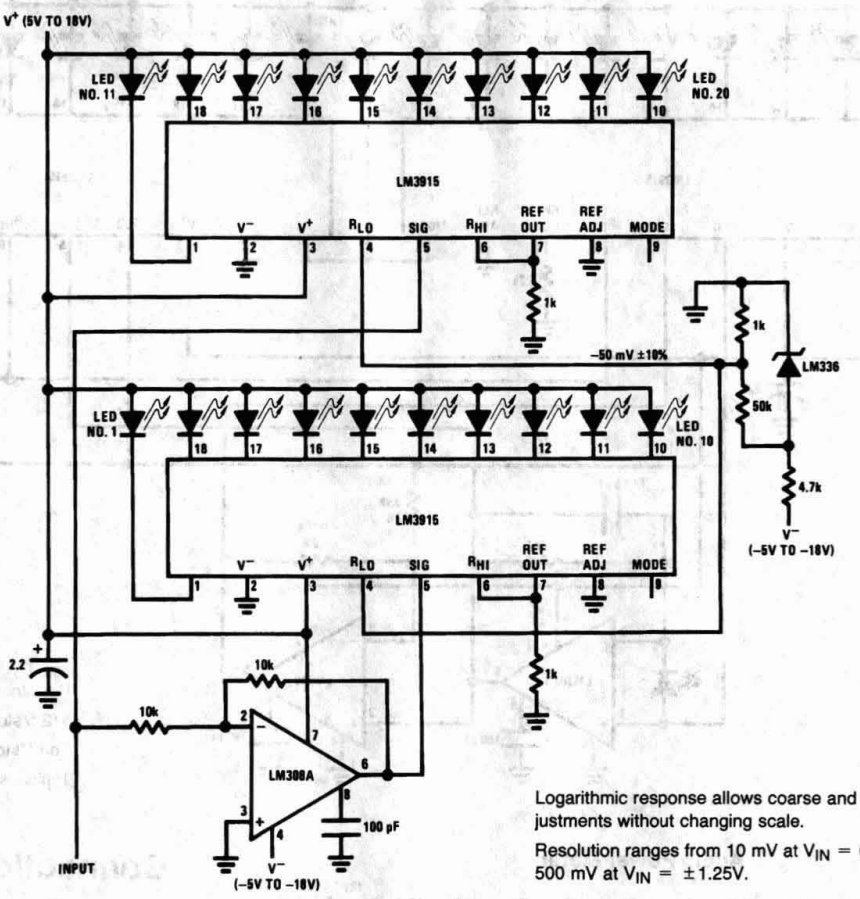


Full-scale causes the full bar display to flash. If the junction of R1 and C1 is connected to a different LED cathode, the display will flash when that LED lights, and at any higher input signal.

TL/H/5104–27

Typical Applications (Continued)

Precision Null Meter

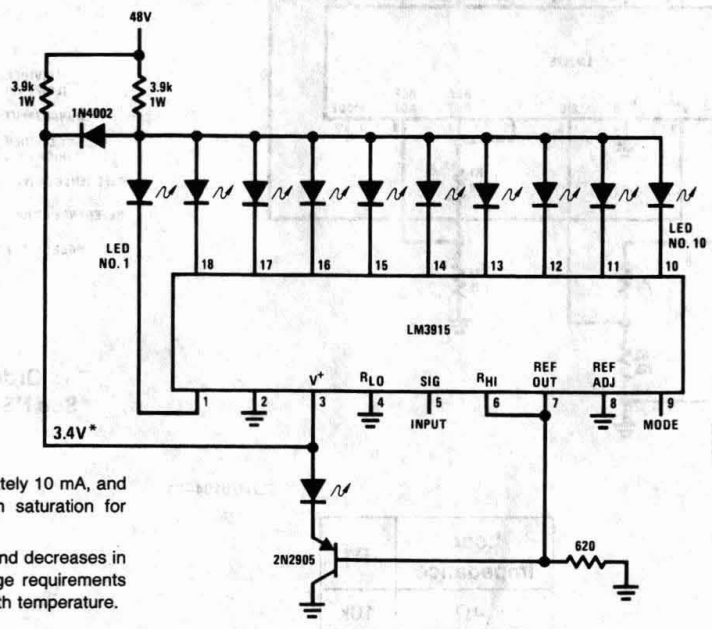


Logarithmic response allows coarse and fine adjustments without changing scale.

Resolution ranges from 10 mV at V_{IN} = 0 mV to 500 mV at V_{IN} = ±1.25V.

TL/H/5104–28

Operating with a High Voltage Supply (Dot Mode Only)



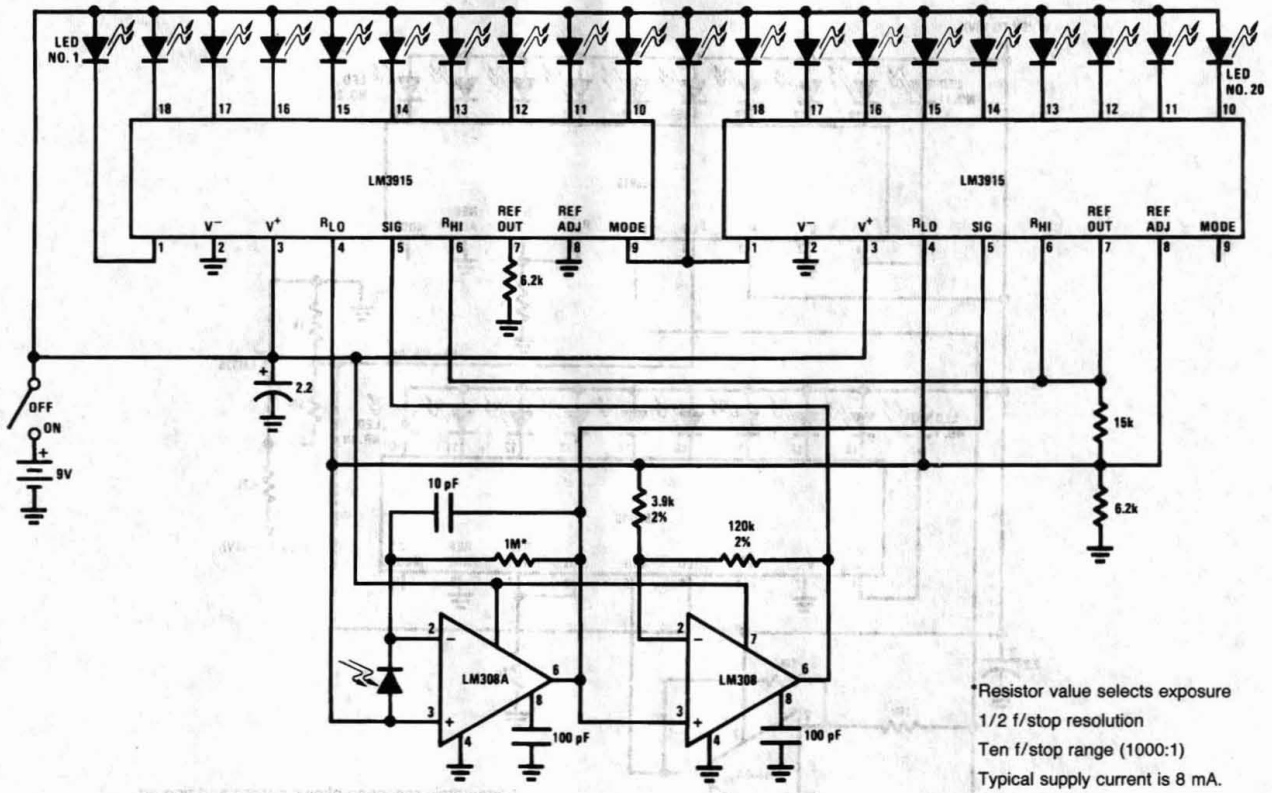
The LED currents are approximately 10 mA, and the LM3915 outputs operate in saturation for minimum dissipation.

*This point is partially regulated and decreases in voltage with temperature. Voltage requirements of the LM3915 also decrease with temperature.

TL/H/5104–29

Typical Applications (Continued)

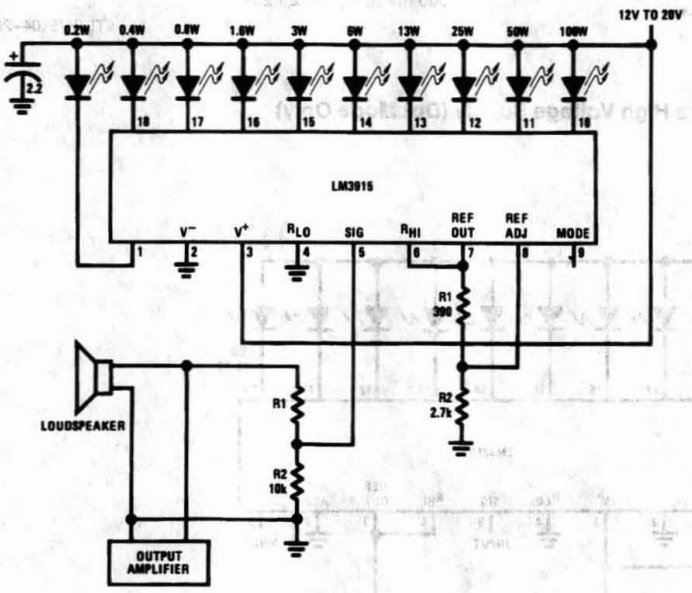
Light Meter



*Resistor value selects exposure
1/2 f/stop resolution
Ten f/stop range (1000:1)
Typical supply current is 8 mA.

TL/H/5104–30

Audio Power Meter



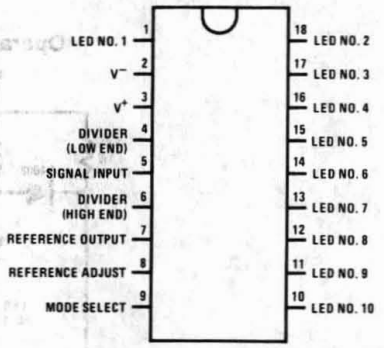
TL/H/5104–31

Load Impedance	R1
4Ω	10k
8Ω	18k
16Ω	30k

See Application Hints for optional Peak or Average Detector

Connection Diagram

Dual-In-Line Package



TL/H/5104–32

Top View

Order Number LM3915N
See NS Package Number N18A

Definition of Terms

Absolute Accuracy: The difference between the observed threshold voltage and the ideal threshold voltage for each comparator. Specified and tested with 10V across the internal voltage divider so that resistor ratio matching error predominates over comparator offset voltage.

Adjust Pin Current: Current flowing out of the reference adjust pin when the reference amplifier is in the linear region.

Comparator Gain: The ratio of the change in output current (I_{LED}) to the change in input voltage (V_{IN}) required to produce it for a comparator in the linear region.

Dropout Voltage: The voltage measured at the current source outputs required to make the output current fall by 10%.

Input Bias Current: Current flowing out of the signal input when the input buffer is in the linear region.

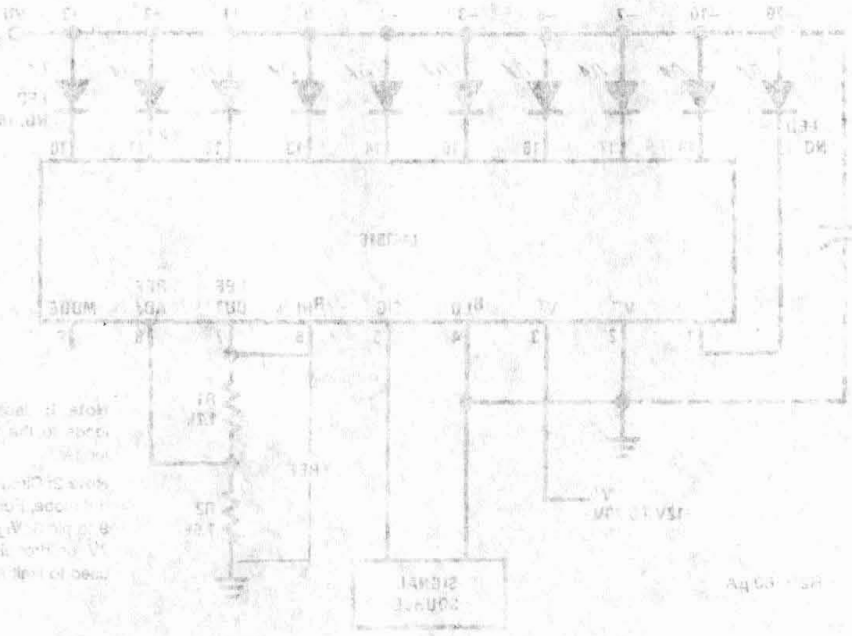
LED Current Regulation: The change in output current over the specified range of LED supply voltage (V_{LED}) as measured at the current source outputs. As the forward voltage of an LED does not change significantly with a small change in forward current, this is equivalent to changing the voltage at the LED anodes by the same amount.

Line Regulation: The average change in reference output voltage (V_{REF}) over the specified range of supply voltage (V^+).

Load Regulation: The change in reference output voltage over the specified range of load current ($I_{L(REF)}$).

Offset Voltage: The differential input voltage which must be applied to each comparator to bias the output in the linear region. Most significant error when the voltage across the internal voltage divider is small. Specified and tested with pin 6 voltage (V_{RHI}) equal to pin 4 voltage (V_{RLO}).

Relative Accuracy: The difference between any two adjacent threshold points. Specified and tested with 10V across the internal voltage divider so that resistor ratio matching error predominates over comparator offset voltage



National Semiconductor

LM3916 Dot/Bar Display Driver

General Description

The LM3916 is a monolithic integrated circuit that senses analog voltage levels and drives ten LEDs, LCDs or vacuum fluorescent displays, providing an electronic version of the popular VU meter. One pin changes the display from a bar graph to a moving dot display. LED current drive is regulated and programmable, eliminating the need for current limiting resistors. The whole display system can operate from a single supply as low as 3V or as high as 25V.

The IC contains an adjustable voltage reference and an accurate ten-step voltage divider. The high-impedance input buffer accepts signals down to ground and up to within 1.5V of the positive supply. Further, it needs no protection against inputs of ±35V. The input buffer drives 10 individual comparators referenced to the precision divider. Accuracy is typically better than 0.2 dB.

Audio applications include average or peak level indicators, and power meters. Replacing conventional meters with an LED bar graph results in a faster responding, more rugged display with high visibility that retains the ease of interpretation of an analog display.

The LM3916 is extremely easy to apply. A 1.2V full-scale meter requires only one resistor in addition to the ten LEDs. One more resistor programs the full-scale anywhere from 1.2V to 12V independent of supply voltage. LED brightness is easily controlled with a single pot.

The LM3916 is very versatile. The outputs can drive LCDs, vacuum fluorescents and incandescent bulbs as well as LEDs of any color. Multiple devices can be cascaded for a dot or bar mode display for increased range and/or resolution. Useful in other applications are the linear LM3914 and the logarithmic LM3915.

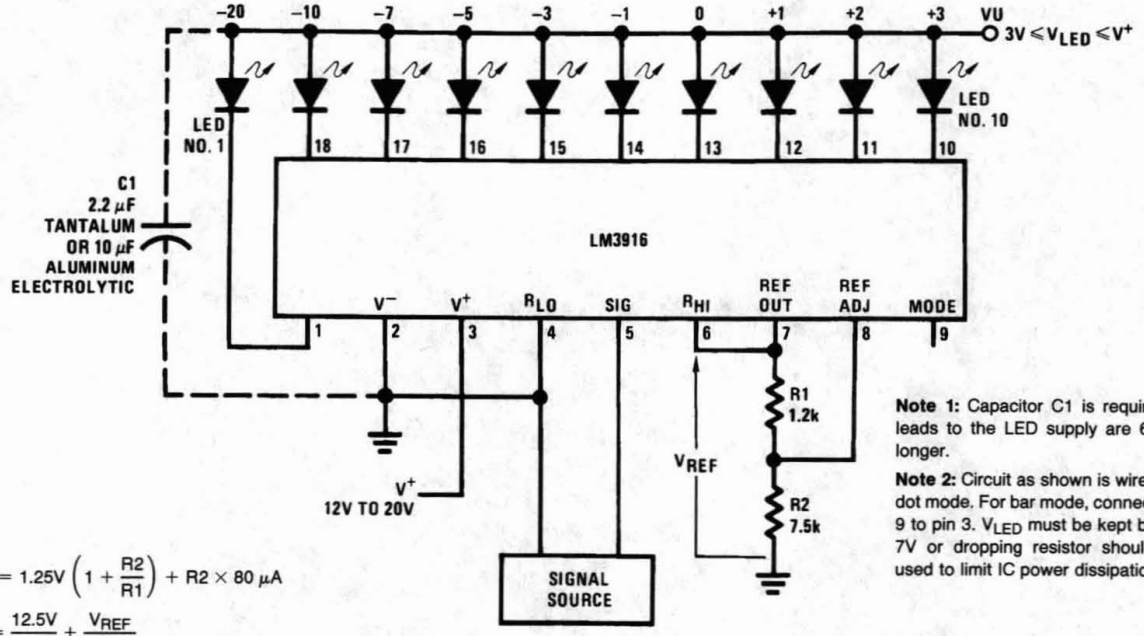
Features

- Fast responding electonic VU meter
- Drivers LEDs, LCDs, or vacuum fluorescents
- Bar or dot display mode externally selectable by user
- Expandable to displays of 70 dB
- Internal voltage reference from 1.2V to 12V
- Operates with single supply of 3V to 25V
- Inputs operate down to ground
- Output current programmable from 1 mA to 30 mA
- Input withstands ±35V without damage or false outputs
- Outputs are current regulated, open collectors
- Directly drives TTL or CMOS
- The internal 10-step divider is floating and can be referenced to a wide range of voltages

The LM3916 is rated for operation from 0°C to + 70°C. The LM3916N is available in an 18-lead molded DIP package.

Typical Applications

0V TO 10V VU Meter



$$V_{REF} = 1.25V\left(1 + \frac{R2}{R1}\right) + R2 \times 80\ \mu A$$

$$I_{LED} = \frac{12.5V}{R1} + \frac{V_{REF}}{2.2\ k\Omega}$$

Note 1: Capacitor C1 is required if leads to the LED supply are 6" or longer.

Note 2: Circuit as shown is wired for dot mode. For bar mode, connect pin 9 to pin 3. V_{LED} must be kept below 7V or dropping resistor should be used to limit IC power dissipation.

TL/H/7971–1

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Power Dissipation (Note 5)	
Molded DIP (N)	1365 mW
Supply Voltage	25V
Voltage on Output Drivers	25V
Input Signal Overvoltage (Note 3)	±35V
Divider Voltage	−100 mV to V+
Reference Load Current	10 mA
Storage Temperature Range	−55°C to +150°C
Lead Temperature (Soldering, 10 seconds)	260°C

Electrical Characteristics (Notes 1 and 3)

Parameter	Conditions (Note 1)	Min	Typ	Max	Units
COMPARATORS					
Offset Voltage, Buffer and First Comparator	$0V \le V_{RLO} = V_{RHI} \le 12V$, I_{LED} = 1 mA		3	10	mV
Offset Voltage, Buffer and Any Other Comparator	$0V \le V_{RLO} = V_{RHI} \le 12V$, I_{LED} = 1 mA		3	15	mV
Gain ($\Delta I_{LED}/\Delta V_{IN}$)	$I_{(REF)}$ = 2 mA, I_{LED} = 10 mA	3	8		mA/mV
Input Bias Current (at Pin 5)	$0V \le V_{IN} \le (V^+ - 1.5V)$		25	100	nA
Input Signal Overvoltage	No Change in Display	−35		35	V
VOLTAGE DIVIDER					
Divider Resistance	Total, Pin 6 to 4	8	12	17	kΩ
Relative Accuracy (Input Change Between Any Two Threshold Points)	(Note 2) −1 dB ≤ V_{IN} ≤ 3 dB −7 dB ≤ V_{IN} ≤ −1 dB −10 dB ≤ V_{IN} ≤ −7 dB	 0.75 1.5 2.5	 1.0 2.0 3.0	 1.25 2.5 2.5	 dB dB dB
Absolute Accuracy	(Note 2) V_{IN} = 2, 1, 0, −1 dB V_{IN} = −3, −5 dB V_{IN} = −7, −10, −20 dB	 −0.25 −0.5 −1		 +0.25 +0.5 +1	 dB dB dB
VOLTAGE REFERENCE					
Output Voltage	0.1 mA ≤ $I_{L(REF)}$ ≤ 4mA, $V^+ = V_{LED}$ = 5V	1.2	1.28	1.34	V
Line Regulation	$3V \le V^+ \le 18V$		0.01	0.03	%/V
Load Regulation	0.1 mA ≤ $I_{L(REF)}$ ≤ 4mA, $V^+ = V_{LED}$ = 5V		0.4	2	%
Output Voltage Change with Temperature	0°C ≤ T_A ≤ +70°C, $I_{L(REF)}$ = 1 mA, $V^+ = V_{LED}$ = 5V		1		%
Adjust Pin Current			75	120	μA
OUTPUT DRIVERS					
LED Current	$V^+ = V_{LED}$ = 5V, $I_{L(REF)}$ = 1 mA	7	10	13	mA
LED Current Difference (Between Largest and Smallest LED Currents)	V_{LED} = 5V, I_{LED} = 2 mA V_{LED} = 5V, I_{LED} = 20 mA		0.12 1.2	0.4 3	mA mA
LED Current Regulation	2V ≤ V_{LED} ≤ 17V I_{LED} = 2 mA I_{LED} = 20 mA		0.1 1	0.25 3	mA mA
Dropout Voltage	$I_{LED(ON)}$ = 20 mA @ V_{LED} = 5V, ΔI_{LED} = 2 mA			1.5	V
Saturation Voltage	I_{LED} = 2.0 mA, $I_{L(REF)}$ = 0.4 mA		0.15	0.4	V
Output Leakage, Each Collector	Bar Mode (Note 4)		0.1	100	μA
Output Leakage	Dot Mode (Note 4)				
Pins 10–18			0.1	100	μA
Pin 1		60	150	450	μA

Electrical Characteristics (Note 1) (Continued)

Parameter	Conditions (Note 1)	Min	Typ	Max	Units
SUPPLY CURRENT					
Standby Supply Current	$V^+ = +5V$, $I_{L(REF)} = 0.2$ mA		2.4	4.2	mA
(All Outputs Off)	$V^+ = +20V$, $I_{L(REF)} = 1.0$ mA		6.1	9.2	mA

Note 1: Unless otherwise stated, all specifications apply with the following conditions:

$3\ V_{DC} \le V^+ \le 20\ V_{DC}$ $\quad -0.015V \le V_{RLO} \le 12\ V_{DC}$ $\quad T_A = 25°C$, $I_{L(REF)} = 0.2$ mA, pin 9 connected to pin 3 (bar mode).

$3\ V_{DC} \le V_{LED} \le V^+$ $\quad V_{REF}, V_{RHI}, V_{RLO} \le (V^+ - 1.5V)$ For higher power dissipations, pulse testing is used.

$-0.015V \le V_{RHI} \le 12\ V_{DC}$ $\quad 0V \le V_{IN} \le V^+ - 1.5V$

Note 2: Accuracy is measured referred to +3 dB = +10.000 V_{DC} at pin 5, with +10.000 V_{DC} at pin 6, and 0.000 V_{DC} at pin 4. At lower full-scale voltages, buffer and comparator offset voltage may add significant error. See table for threshold voltages.

Note 3: Pin 5 input current must be limited to ±3 mA. The addition of a 39k resistor in series with pin 5 allows ±100V signals without damage.

Note 4: Bar mode results when pin 9 is within 20 mV of V^+. Dot mode results when pin 9 is pulled at least 200 mV below V^+. LED #10 (pin 10 output current) is disabled if pin 9 is pulled 0.9V or more below V_{LED}.

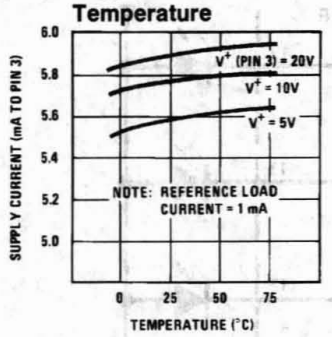
Note 5: The maximum junction temperature of the LM3916 is 100°C. Devices must be derated for operation at elevated temperatures. Junction to ambient thermal resistance is 55°C/W for the molded DIP (N package).

LM3916 Threshold Voltage (Note 2)

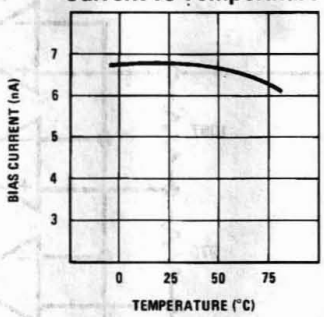
dB	Volts			dB	Volts		
	Min	Typ	Max		Min	Typ	Max
3	9.985	10.000	10.015	−3 ± ½	4.732	5.012	5.309
2 ± ¼	8.660	8.913	9.173	−5 ± ½	3.548	3.981	4.467
1 ± ¼	7.718	7.943	8.175	−7 ± 1	2.818	3.162	3.548
0 ± ¼	6.879	7.079	7.286	−10 ± 1	1.995	2.239	2.512
−1 ± ½	5.957	6.310	6.683	−20 ± 1	0.631	0.708	0.794

Typical Performance Characteristics

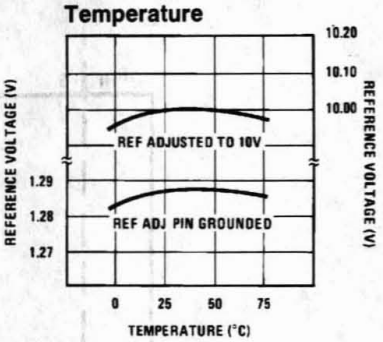
Supply Current vs Temperature



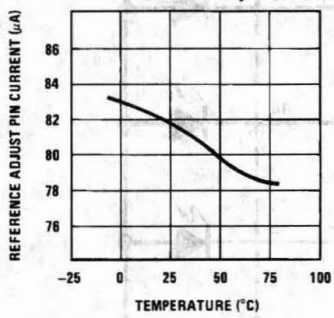
Operating Input Bias Current vs Temperature



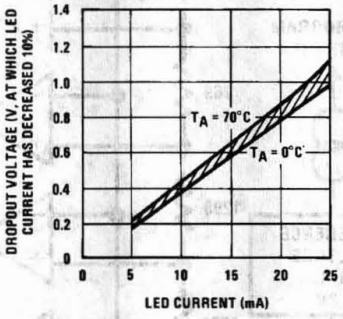
Reference Voltage vs Temperature



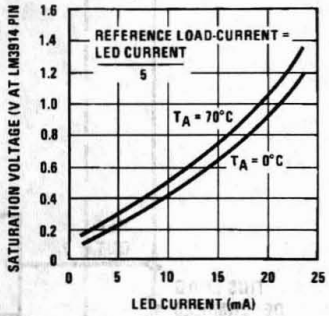
Reference Adjust Pin Current vs Temperature



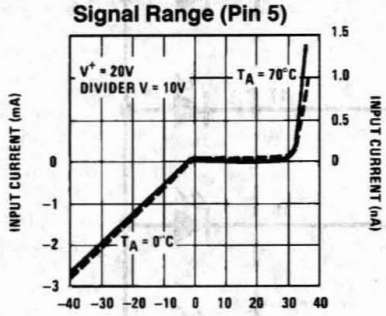
LED Current-Regulation Dropout



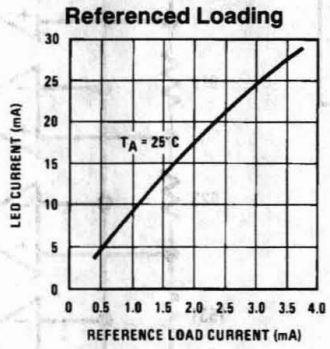
LED Driver Saturation Voltage



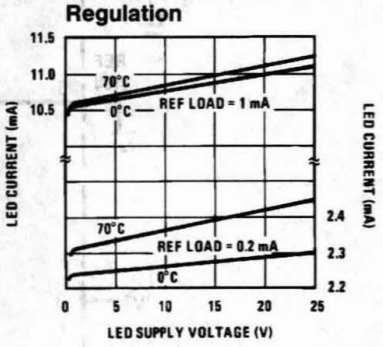
Input Current Beyond Signal Range (Pin 5)



LED Current vs Referenced Loading

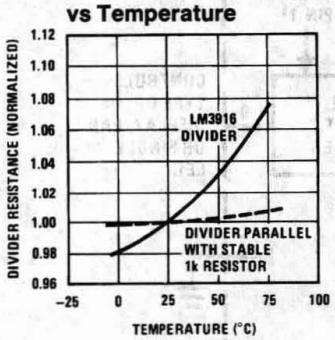


LED Driver Current Regulation

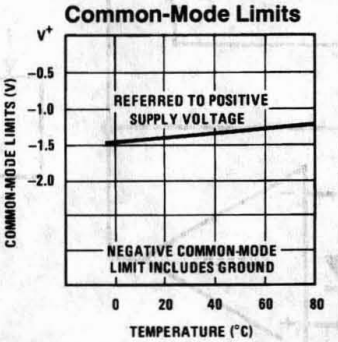


TL/H/7971–2

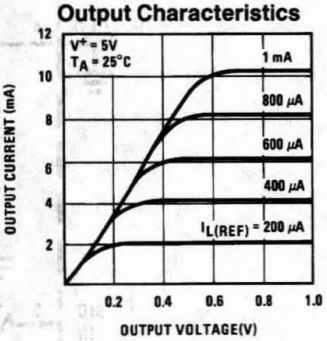
Total Divider Resistance vs Temperature



Common-Mode Limits



Output Characteristics



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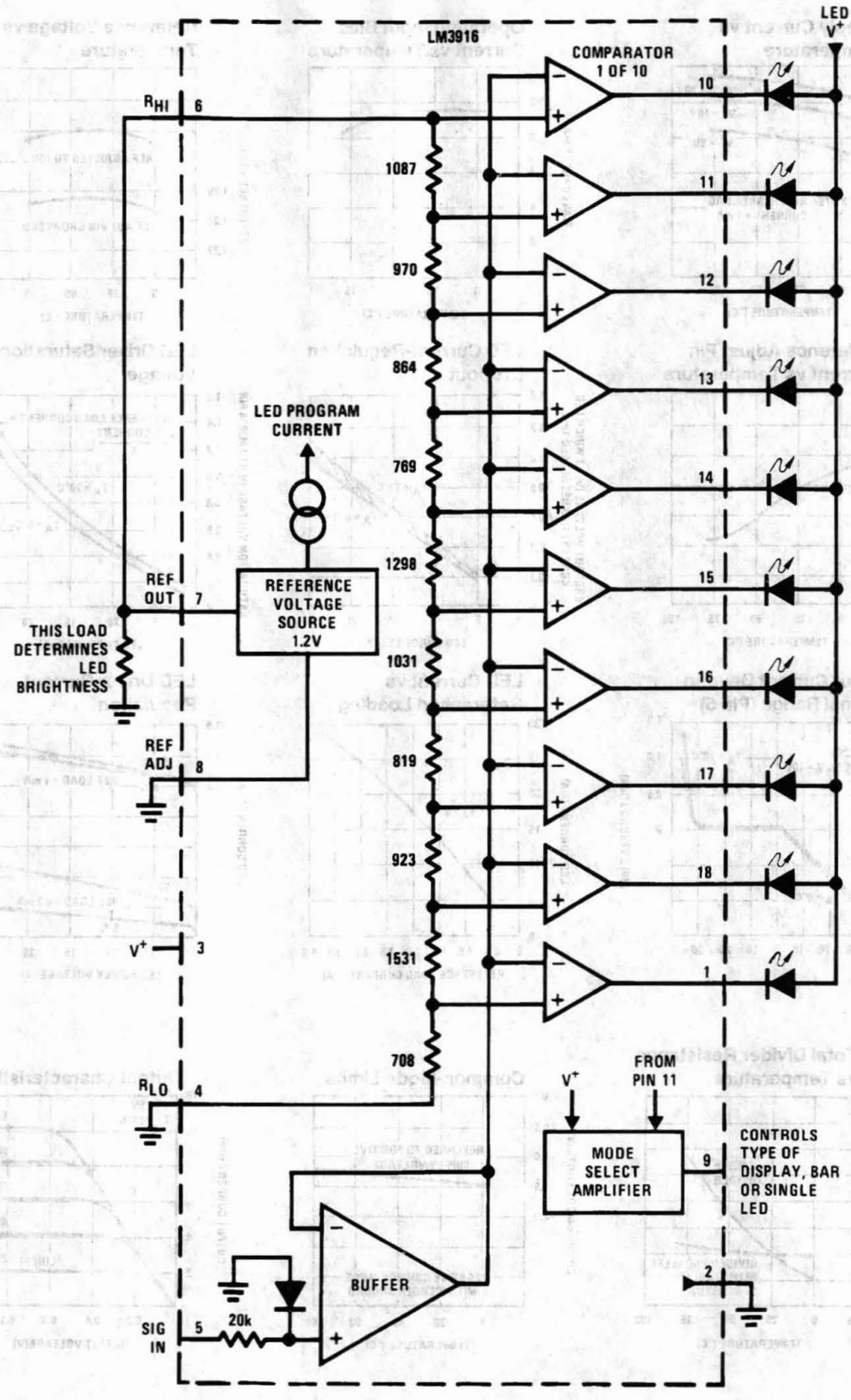
Block Diagram (Showing Simplest Application)



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Functional Description

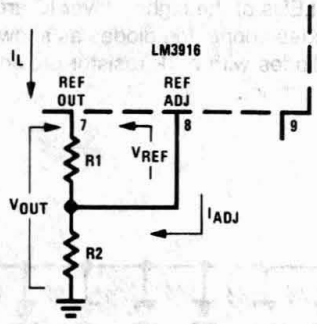
The simplified LM3916 block diagram is included to give the general idea of the circuit's operation. A high input impedance buffer operates with signals from ground to 12V, and is protected against reverse and overvoltage signals. The signal is then applied to a series of 10 comparators; each of which is biased to a different comparison level by the resistor string.

In the example illustrated, the resistor string is connected to the internal 1.25V reference voltage. As the input voltage varies from 0 to 1.25, the comparator outputs are driven low one by one, switching on the LED indicators. The resistor divider can be connected between any 2 voltages, providing that they are at least 1.5V below V^+ and no lower than V^-.

INTERNAL VOLTAGE REFERENCE

The reference is designed to be adjustable and develops a nominal 1.25V between the REF OUT (pin 7) and REF ADJ (pin 8) terminals. The reference voltage is impressed across program resistor R1 and, since the voltage is constant, a constant current I_1 then flows through the output set resistor R2 giving an output voltage of:

$$V_{OUT} = V_{REF}\left(1 + \frac{R2}{R1}\right) + I_{ADJ}\,R2$$



TL/H/7971–5

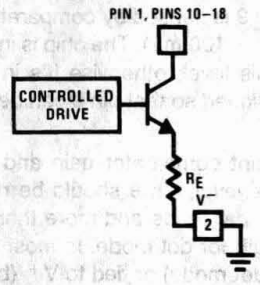
Since the 120 μA current (max) from the adjust terminal represents an error term, the reference was designed to minimize changes of this current with V^+ and load changes. For correct operation, reference load current should be between 80 μA and 5 mA. Load capacitance should be less than 0.05 μF.

CURRENT PROGRAMMING

A feature not completely illustrated by the block diagram is the LED brightness control. The current drawn out of the reference voltage pin (pin 7) determines LED current. Approximately 10 times this current will be drawn through each lighted LED, and this current will be relatively constant despite supply voltage and temperature changes. Current drawn by the internal 10-resistor divider, as well as by the external current and voltage-setting divider should be included in calculating LED drive current. The ability to modulate LED brightness with time, or in proportion to input voltage and other signals can lead to a number of novel displays or ways of indicating input overvoltages, alarms, etc.

The LM3916 outputs are current-limited NPN transistors as shown below. An internal feedback loop regulates the transistor drive. Output current is held at about 10 times the reference load current, independent of output voltage and processing variables, as long as the transistor is not saturated.

LM3916 Output Circuit



TL/H/7971–6

Outputs may be run in saturation with no adverse effects, making it possible to directly drive logic. The effective saturation resistance of the output transistors, equal to R_E plus the transistors' collector resistance, is about 50Ω. It's also possible to drive LEDs from rectified AC with no filtering. To avoid oscillations, the LED supply should be bypassed with a 2.2 μF tantalum or 10 μF aluminum electrolytic capacitor.

MODE PIN USE

Pin 9, the Mode Select input, permits chaining of multiple devices, and controls bar or dot mode operation. The following tabulation shows the basic ways of using this input. Other more complex uses will be illustrated in the applications.

Bar Graph Display: Wire Mode Select (pin 9) *directly* to pin 3 (V^+ pin).

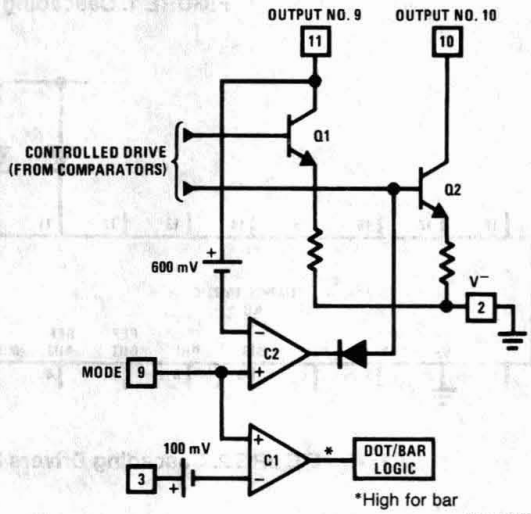
Dot Display, Single LM3916 Driver: Leave the Mode Select pin open circuit.

Dot Display, 20 or More LEDs: Connect pin 9 of the *first* drivers in the series (i.e., the one with the lowest input voltage comparison points) to pin 1 of the next higher LM3916 driver. Continue connecting pin 9 of lower input drivers to pin 1 of higher input drivers for 30 or more LED displays. The last LM3916 driver in the chain will have pin 9 left open. All previous drivers should have a 20k resistor in parallel with LED #9 (pin 11 to V_{LED}).

Mode Pin Functional Description

This pin actually performs two functions. Refer to the simplified block diagram below.

Block Diagram of Mode Pin Function



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Mode Pin Functional Description (Continued)

DOT OR BAR MODE SELECTION

The voltage at pin 9 is sensed by comparator C1, nominally referenced to ($V^+ - 100$ mV). The chip is in bar mode when pin 9 is above this level; otherwise it's in dot mode. The comparator is designed so that pin 9 can be left open circuit for dot mode.

Taking into account comparator gain and variation in the 100 mV reference level, pin 9 should be no more than 20 mV below V^+ for bar mode and more than 200 mV below V^+ (or open circuit) for dot mode. In most applications, pin 9 is either open (dot mode) or tied to V^+ (bar mode). In bar mode, pin 9 should be connected directly to pin 3. Large currents drawn from the power supply (LED current, for example) should not share this path so that large IR drops are avoided.

DOT MODE CARRY

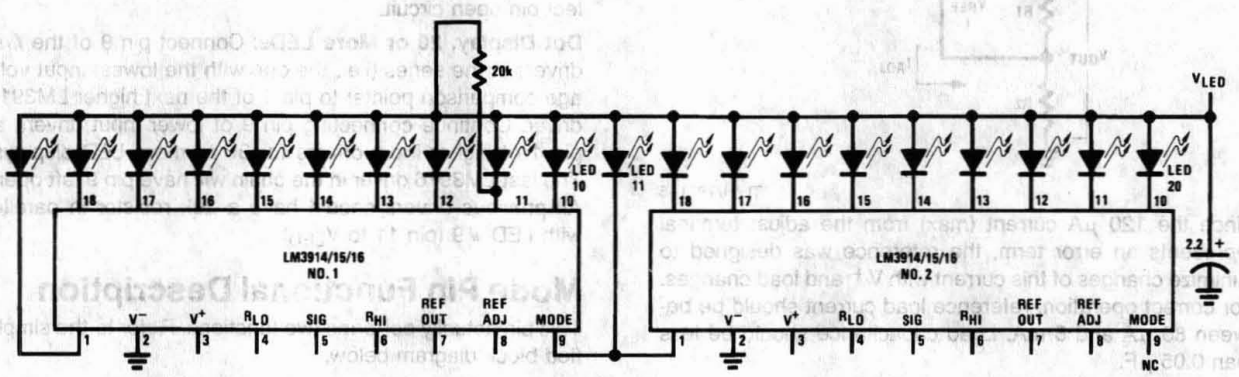
In order for display to make sense when multiple drivers are cascaded in dot mode, special circuitry has been included to shut off LED #10 of the first device when LED #1 of the second device comes on. The connection for cascading in dot mode has already been described and is depicted in *Figure 1*.

As long as the input signal voltage is below the threshold of the second driver, LED #11 is off. Pin 9 of driver #1 thus sees effectively an open circuit so the chip is in dot mode. As soon as the input voltage reaches the threshold of LED #11, pin 9 of driver #1 is pulled an LED drop (1.5V or more) below V_{LED}. This condition is sensed by comparator C2, referenced 600 mV below V_{LED}. This forces the output of C2 low, which shuts off output transistor Q2, extinguishing LED #10.

V_{LED} is sensed via the 20k resistor connected to pin 11. The very small current (less than 100 μA) that is diverted from LED #9 does not noticeably affect its intensity.

An auxiliary current source at pin 1 keeps at least 100 μA flowing through LED #11 even if the input voltage rises high enough to extinguish the LED. This ensures that pin 9 of driver #1 is held low enough to force LED #10 off when *any* higher LED is illuminated. While 100 μA does not normally produce significant LED illumination, it may be noticeable when using high-efficiency LEDs in a dark environment. If this is bothersome, the simple cure is to shunt LED #11 (and LED #1) with a 10k resistor. The 1V 1R drop is more than the 900 mV worst case required to hold off LED #10 yet small enough that LED #11 does not conduct significantly.

In some circuits a number of outputs on the higher device are not used. Examples include the high resolution VU meter and the expanded range VU meter circuits (see Typical Applications). To provide the proper carry sense voltage in dot mode, the LEDs of the higher driver IC are tied to V_{LED} through two series-connected diodes as shown in *Figure 2*. Shunting the diodes with a 1k resistor provides a path for driver leakage current.



TL/H/7971–8

FIGURE 1. Cascading LM3914/15/16 Series in Dot Mode

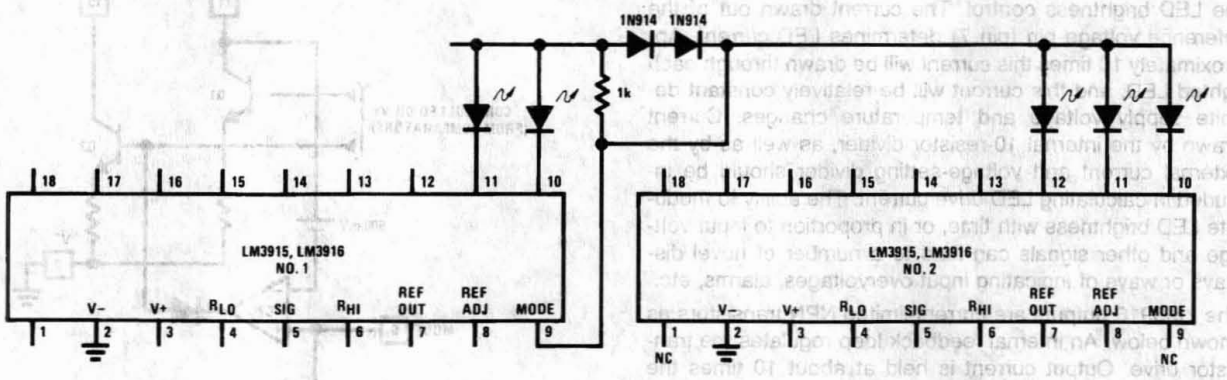


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FIGURE 2. Cascading Drivers in Dot Mode with Pin 1 of Driver #2 Unused

Mode Pin Functional Description (Continued)

OTHER DEVICE CHARACTERISTICS

The LM3915 is relatively low-powered itself, and since any number of LEDs can be powered from about 3V, it is a very efficient display driver. Typical standby supply current (all LEDs OFF) is 1.6 mA. However, any reference loading adds 4 times that current drain to the V^+ (pin 3) supply input. For example, an LM3915 with a 1 mA reference pin load (1.3k) would supply almost 10 mA to every LED while drawing only 10 mA from its V^+ pin supply. At full-scale, the IC is typically drawing less than 10% of the current supplied to the display.

The display driver does not have built-in hysteresis so that the display does not jump instantly from one LED to the next. Under rapidly changing signal conditions, this cuts down high frequency noise and often an annoying flicker. An "overlap" is built in so that at no time are all segments completely off the dot mode. Generally one LED fades in while the other fades out over a 1 mV range. The change may be much more rapid between LED #10 of one device and LED #1 of a *second* device cascaded.

Application Hints

The most difficult problem occurs when large LED currents are being drawn, especially in bar graph mode. These currents flowing out of the ground pin cause voltage drops in external wiring, and thus errors and oscillations. Bringing the return wires from signal sources, reference ground and bottom of the resistor string to a single point very near pin 2 is the best solution.

Long wires from V_{LED} to LED anode common can cause oscillations. The usual cure is bypassing the LED anodes with a 2.2 μF tantalum or 10 μF aluminum electrolytic capacitor. If the LEd anode line wiring is inaccessible, often a 0.1 μF capacitor from pin 1 to pin 2 will be sufficient.

If there is a large amount of LED overlap in the bar mode, oscillation or excessive noise is usually the problem. In cases where proper wiring and bypassing fail to stop oscillations, V^+ voltage at pin 3 is usually below suggested limits. When several LEDs are lit in dot mode, the problem is usually an AC component of the input signal which should be filtered out. Expanded scale meter applications may have one or both ends of the internal voltage divider terminated at relatively high value resistors. These high-impedance ends should be bypassed to pin 2 with 0.1 μF.

Power dissipation, especially in bar mode should be given consideration. For example, with a 5V supply and all LEDs programmed to 20 mA the driver will dissipate over 600 mW. In this case a 7.5Ω resistor in series with the LED supply will cut device heating in half. The negative end of the resistor should be bypassed with a 2.2 μF solid tantalum or 10 μF aluminum electrolytic capacitor to pin 2.

TIPS ON RECTIFIER CIRCUITS

The simplest way to display an AC signal using the LM3916 is to apply it right to pin 5 unrectified. Since the LED illuminated represents the instantaneous value of the AC waveform, one can readily discern both peak and average values of audio signals in this manner. The LM3916 will respond to positive half-cycles only but will not be damaged by signals up to $\pm$35V (or up to $\pm$100V if a 39k resistor is in series with the input). A smear or bar type display results even though the LM3916 is connected for dot mode. The LEDs should be run at 20 mA to 30 mA for high enough average intensity.

True average or peak detection requires rectification. If an LM3916 is set up with 10V full scale across its voltage divider, the turn-on point for the first LED is only 450 mV. A simple silicon diode rectifier won't work well at the low end due to the 600 mV diode threshold. The half-wave peak detector in *Figure 3* uses a PNP emitter-follower in front of the diode. Now, the transistor's base-emitter voltage cancels out the diode offset, within about 100 mV. This approach is usually satisfactory when a single LM3916 is used for a 23 dB display.

Display circuits such as the extended range VU meter using two or more drivers for a dynamic range of 40 dB or greater require more accurate detection. In the precision half-wave rectifier of *Figure 4* the effective diode offset is reduced by a factor equal to the open-loop gain of the op amp. Filter capacitor C2 charges through R3 and discharges through R2 and R3, so that appropriate selection of these values results in either a peak or an average detector. The circuit has a gain equal to R2/R1.

It's best to capacitively couple the input. Audio sources frequently have a small DC offset that can cause significant error at the low end of the log display. Op amps that slew quickly, such as the LF351, LF353 or LF356, are needed to faithfully respond to sudden transients. It may be necessary to trim out the op amp DC offset voltage to accurately cover a 60 dB range. Best results are obtained if the circuit is adjusted for the correct output when a low-level AC signal (10 to 20 mV) is applied, rather than adjusting for zero output with zero input.

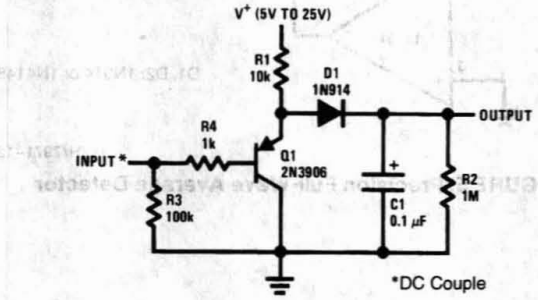

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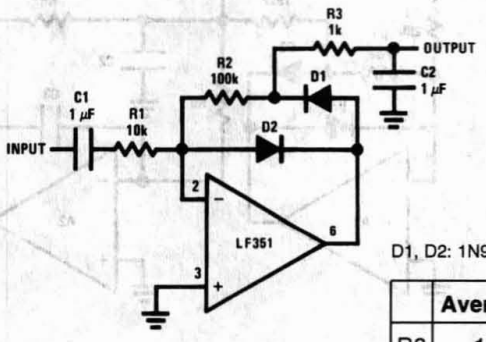
FIGURE 3. Half-Wave Peak Detector



D1, D2: 1N914 or 1N4148

	Average	Peak
R2	1k	100k
R3	100k	1k

R1 = R2 for A_V = 1

R1 = R2/10 for A_V = 10

C1 = 10/R1

TL/H/7971–11

FIGURE 4. Precision Half-Wave Rectifier

Application Hints (Continued)

For precision full-wave averaging use the circuit in *Figure 5.* Using 1% resistors for R1 through R4, gain for positive and negative signal differs by only 0.5 dB worst case. Substituting 5% resistors increases this to 2 dB worst case. (A 2 dB gain difference means that the display may have a ±1 dB error when the input is a nonsymmetrical transient). The averaging time constant is R5•C2. A simple modification results in the precision full-wave detector of *Figure 6.* Since the filter capacitor is not buffered, this circuit can drive only high impedance loads such as the input of an LM3916.

AUDIO METER STANDARDS

VU Meter

The audio level meter most frequently encountered is the VU meter. Its characteristics are defined as the ANSI specification C165. The LM3916's outputs correspond to the meter indications specified with the omission of the −2 VU indication. The VU scale divisions differ slightly from a linear scale in order to obtain whole numbers in dB.

Some of the most important specifications for an AC meter are its dynamic characteristics. These define how the meter responds to transients and how fast the reading decays. The VU meter is a relatively slow full-wave averaging type, specified to reach 99% deflection in 300 ms and overshoot by 1 to 1.5%. In engineering terms this means a slightly underdamped second order response with a resonant frequency of 2.1 Hz and a Q of 0.62. *Figure 7* depicts a simple rectifier/filter circuit that meets these criteria.

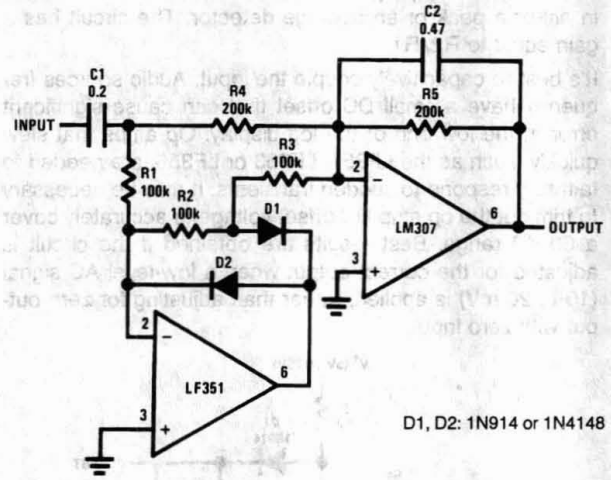


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FIGURE 5. Precision Full-Wave Average Detector

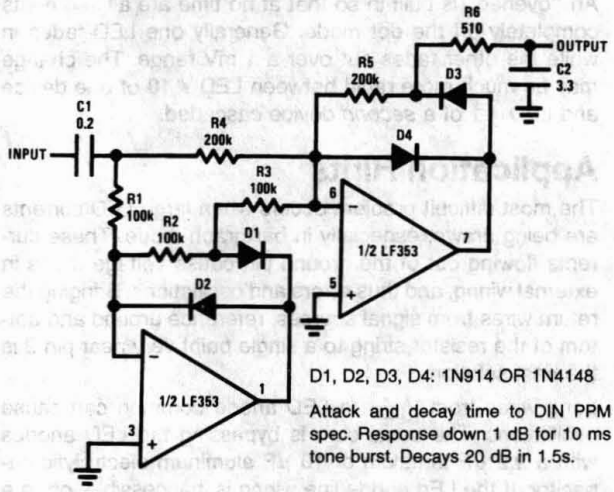

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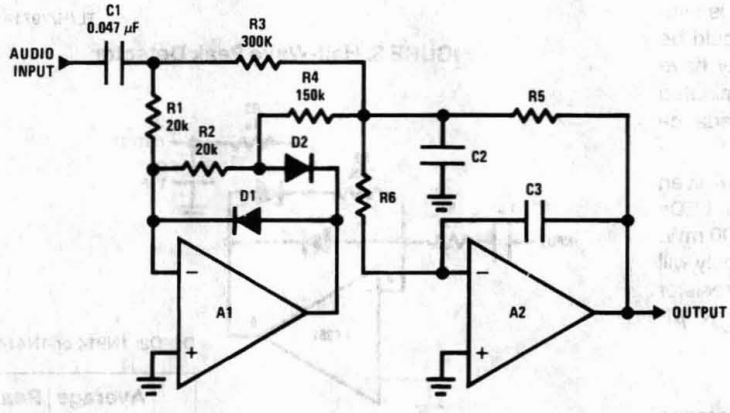
FIGURE 6. Precision Full-Wave Peak Detector



TL/H/7971–14

GAIN	R5	R6	C2	C3
1	100k	43k	2.0	0.56 µF
10	1M	100k	1.0	0.056 µF

Design Equations

$$\frac{1}{R5 \bullet R6 \bullet C2 \bullet C3} = \omega_0^2 = 177\ \text{sec}^{-2}$$

$$\frac{1}{C2}\left(\frac{1}{R3}+\frac{1}{R4}+\frac{1}{R5}+\frac{1}{R6}\right) = \frac{\omega_0}{Q} = 21.5\ \text{sec}^{-1}$$

R3 = 2R4

R1 = R2 ≪ R4

A1, A2: ½ LF353

D1, D2: 1N914 OR 1N4148

*Reaches 99% level at 300 ms after applied tone burst and overshoots 1.2%.

FIGURE 7. Full-Wave Average Detector to VU Meter Specifications*

Application Hints (Continued)

Peak Program Meter

The VU meter, originally intended for signals sent via telephone lines, has shortcomings when used in high fidelity systems. Due to its slow response time, a VU meter will not accurately display transients that can saturate a magnetic tape or drive an amplifier into clipping. The fast-attack peak program meter (PPM) which does not have this problem is becoming increasingly popular.

While several European organizations have specifications for peak program meters, the German DIN specification 45406 is becoming a de facto standard. Rather than respond instantaneously to peak, however, PPM specifications require a finite "integration time" so that only peaks wide enough to be audible are displayed. DIN 45406 calls for a response of 1 dB down from steady-state for a 10 ms tone burst and 4 dB down for a 3 ms tone burst. These requirements are consistent with the other frequently encountered spec of 2 dB down for a 5 ms burst and are met by an attack time constant of 1.7 ms.

The specified return time of 1.5s to −20 dB requires a 650 ms decay time constant. The full-wave peak detector of *FIGURE 6* satisfies both the attack and decay time criteria.

Cascading The LM3916

The LM3916 by itself covers the 23 dB range of the conventional VU meter. To display signals of 40 dB or 70 dB dynamic range, the LM3916 may be cascaded with the 3 dB/step LM3915s. Alternatively, two LM3916s may be cascaded for increased resolution over a 28 dB range. Refer to the Extended Range VU Meter and High Resolution VU Meter in the Typical Applications section for the complete circuits for both dot and bar mode displays.

To obtain a display that makes sense when an LM3915 and an LM3916 are cascaded, the −20 dB output from the LM3916 is dropped. The full-scale display for the LM3915 is set at 3 dB below the LM3916's −10 dB output and the rest of the thresholds continue the 3 dB/step spacing. A simple, low cost approach is to set the reference voltage of the two chips 16 dB apart as in *Figure 5*. The LM3915, with pin 8 grounded, runs at 1.25V full-scale. R1 and R2 set the LM3916's reference 16 dB higher or 7.89V. Variation in the two on-chip references and resistor tolerance may cause a ± 1 dB error in the −10 dB to −13 dB transition. If this is objectionable, R2 can be trimmed.

The drawback of the aforementioned approach is that the threshold of LED #1 on the LM3915 is only 56 mV. Since comparator offset voltage may be as high as 10 mV, large errors can occur at the first few thresholds. A better approach, as shown in *Figure 9,* is to keep the reference the same for both drivers (10V in the example) and *amplify* the input signal by 16 dB ahead of the LM3915. Alternatively,

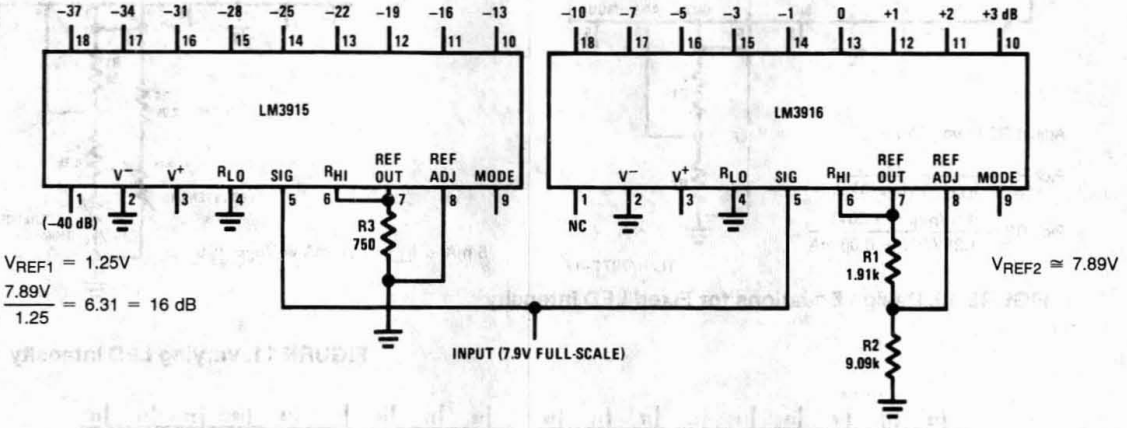


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FIGURE 8. Low Cost Circuit for 40 dB Display

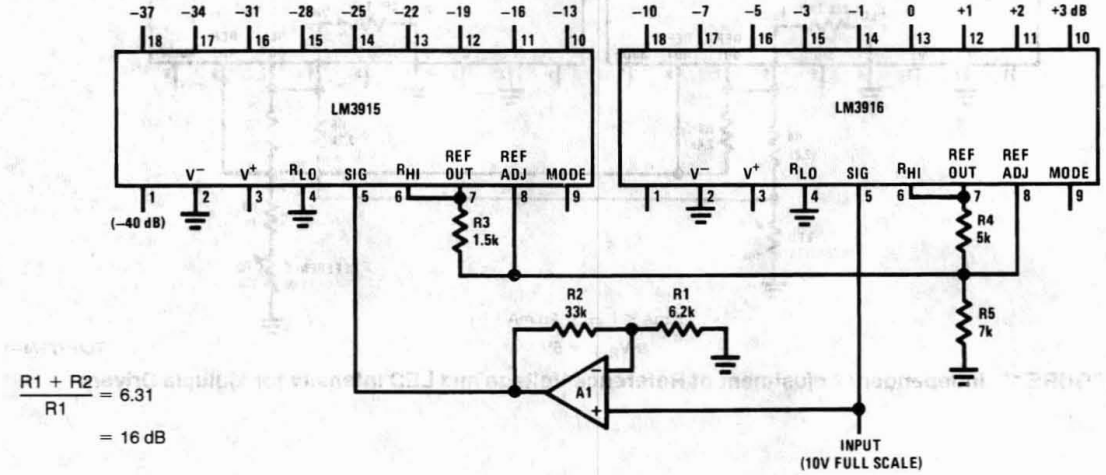

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FIGURE 9. Improved Circuit for 40 dB Display

Application Hints (Continued)

instead of amplifying, input signals of sufficient amplitude can be fed directly to the LM3916 and *attenuated* by 16 dB to drive the LM3915.

To extend this approach to get a 70 dB display, another 30 dB of amplification must be placed in the signal path ahead of the lowest LM3915. Extreme care is required as the lowest LM3915 displays input signals down to 2 mV! Several offset nulls may be required. High currents should not share the same path as the low level signal. Also power line wiring should be kept away from signal lines.

TIPS ON REFERENCE VOLTAGE AND LED CURRENT PROGRAMMING

Single Driver

The equations in *Figure 10* illustrate how to choose resistor values to set reference voltage for the simple case where no LED intensity adjustment is required. A LED current of 10 mA to 20 mA generally produces adequate illumination. Having 10V full-scale across the internal voltage divider gives best accuracy by keeping signal level high relative to the offset voltage of the internal comparators. However, this causes 1 mA to flow from pin 7 into the divider which means that the LED current will be at least 10 mA. R1 will typically be between 1 kΩ and 5 kΩ. To trim the reference voltage, vary R2.

The current in *Figure 11* shows how to add a LED intensity control which can vary LED current from 5 mA to 28 mA. Choosing V_{REF} = 5V lowers the current drawn by the ladder, increasing the intensity adjustment range. The reference adjustment has some effect on LED intensity but the reverse is not true.

Multiple Drivers

Figure 12 shows how to obtain a common reference trim and intensity control for two drivers. The two ICs may be connected in cascade or may be handling separate channels for stereo. This technique can be extended for larger numbers of drivers by varying the values of R1, R2 and R3. Because the LM3915 has a greater ladder resistance, R5 was picked less than R7 in such a way as to provide equal reference load currents. The ICs' internal references track within 100 mV so that worst case error from chip to chip is only 0.2 dB for V_{REF} = 5V.

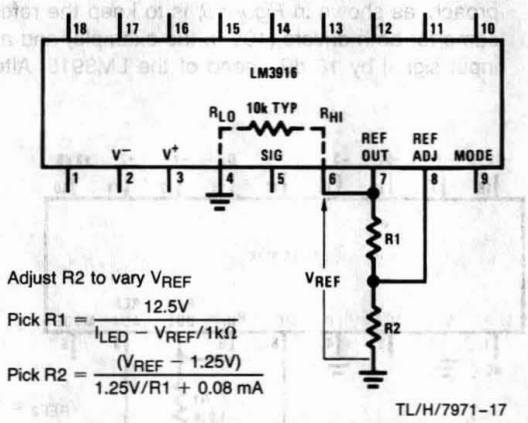


FIGURE 10. Design Equations for Fixed LED Intensity

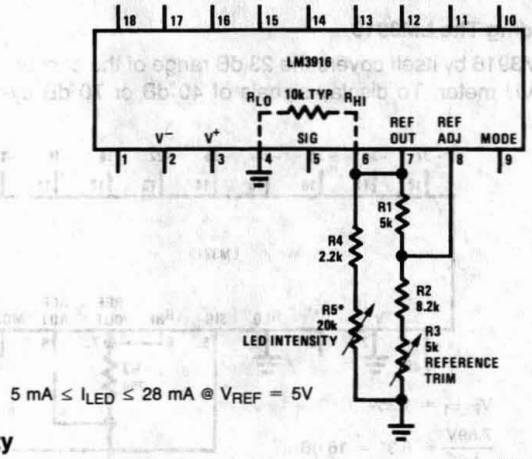


FIGURE 11. Varying LED Intensity

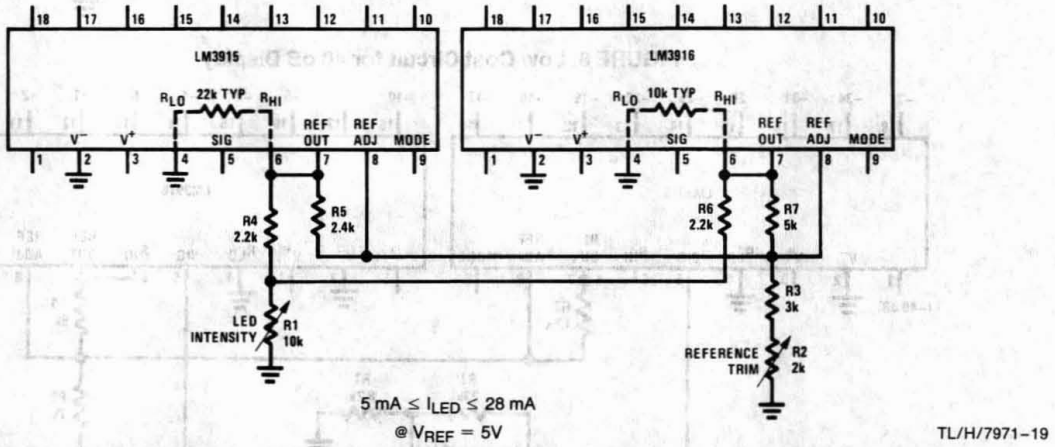


FIGURE 12. Independent Adjustment of Reference Voltage and LED Intensity for Multiple Drivers

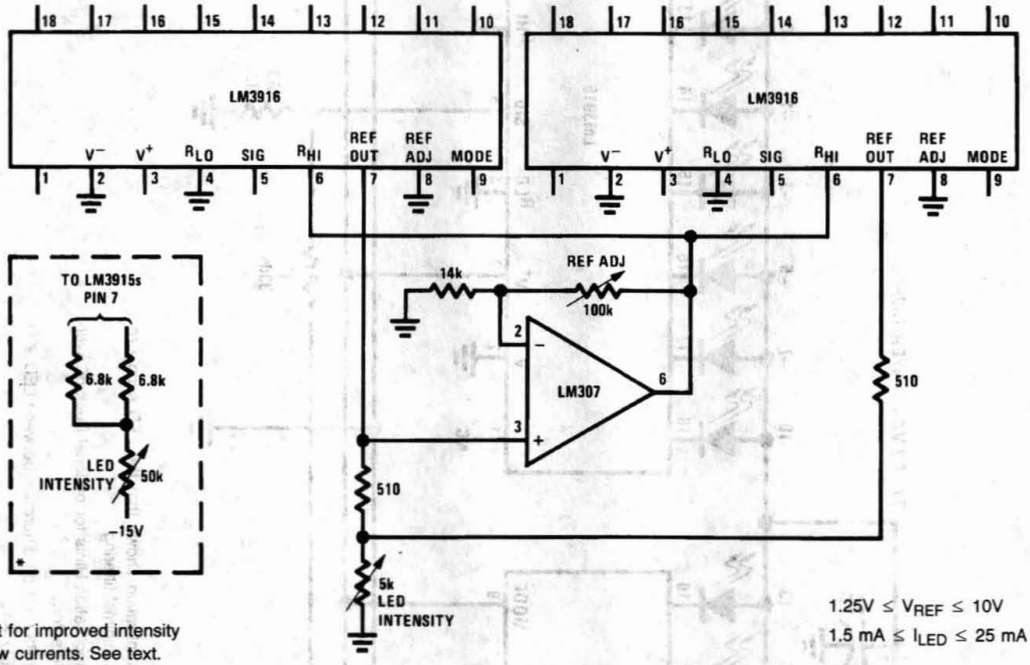
Application Hints (Continued)

The scheme in *Figure 13* is useful when the reference and LED intensity must be adjusted independently over a wide range. The R_{HI} voltage can be adjusted from 1.2V to 10V with no effect on LED current. Since the internal divider here does not load down the reference, minimum LED current is much lower. At the minimum recommended reference load of 80 μA, LED current is about 0.8 mA. The resistor values shown give a LED current range from 1.5 mA to 25 mA.

At the low end of the intensity adjustment, the voltage drop across the 510Ω current-sharing resistors is so small that chip to chip variation in reference voltage may yield a visible variation in LED intensity. The optional approach shown of connecting the bottom end of the intensity control pot to a negative supply overcomes this problem by allowing a larger voltage drop across the (larger) current-sharing resistors.

Other Applications

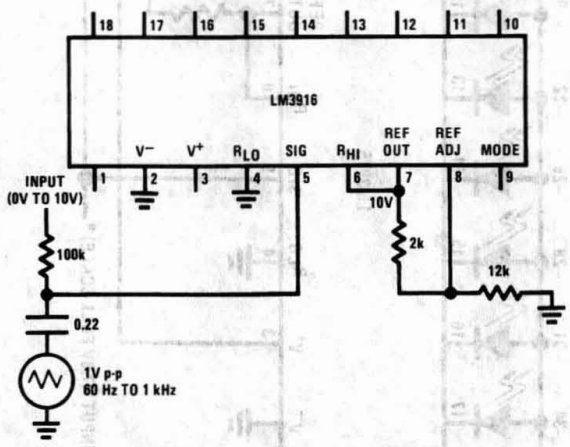
For increased resolution, it's possible to obtain a display with a smooth transition between LEDs. This is accomplished by superimposing an AC waveform on top of the input level as shown in *Figure 14*. The signal can be a triangle, sawtooth or sine wave from 60 Hz to 1 kHz. The display can be run in either dot or bar mode.



*Optional circuit for improved intensity matching at low currents. See text.

TL/H/7971–20

FIGURE 13. Wide-Range Adjustment of Reference Voltage and LED intensity for Multiple Drivers

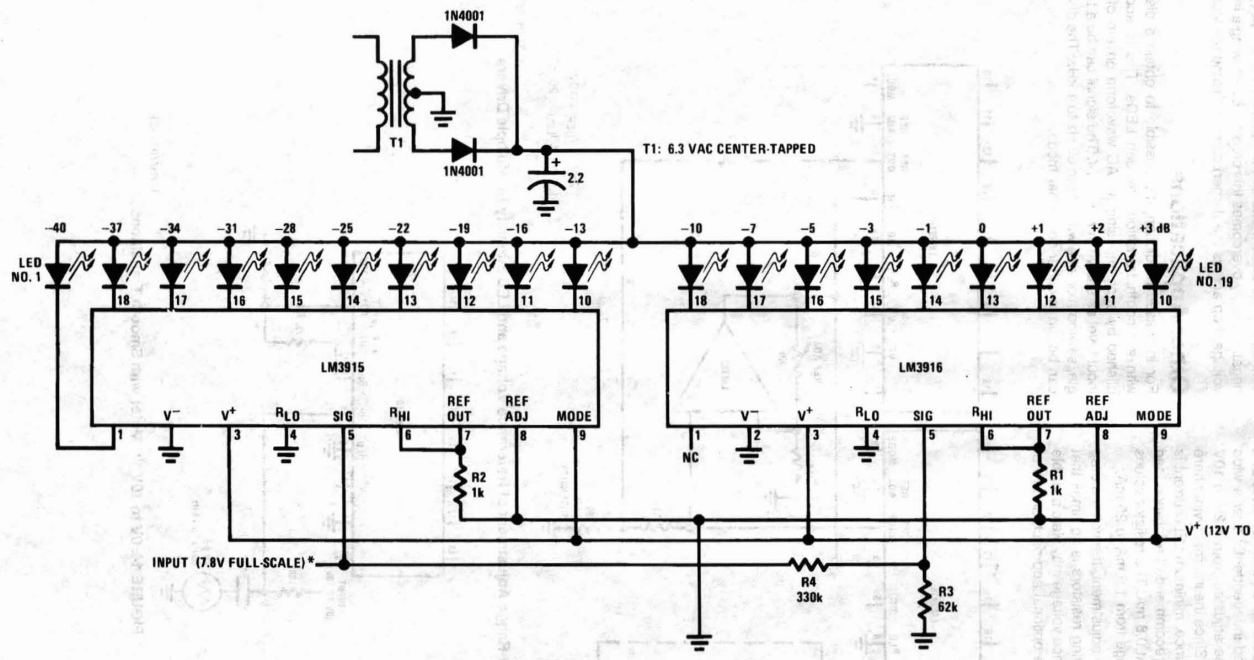


TL/H/7971–21

FIGURE 14. 0V to 10V VU Meter with Smooth Transitions

Typical Applications (Continued)

Extended Range VU Meter (Bar Mode)



TL/H/7971–22

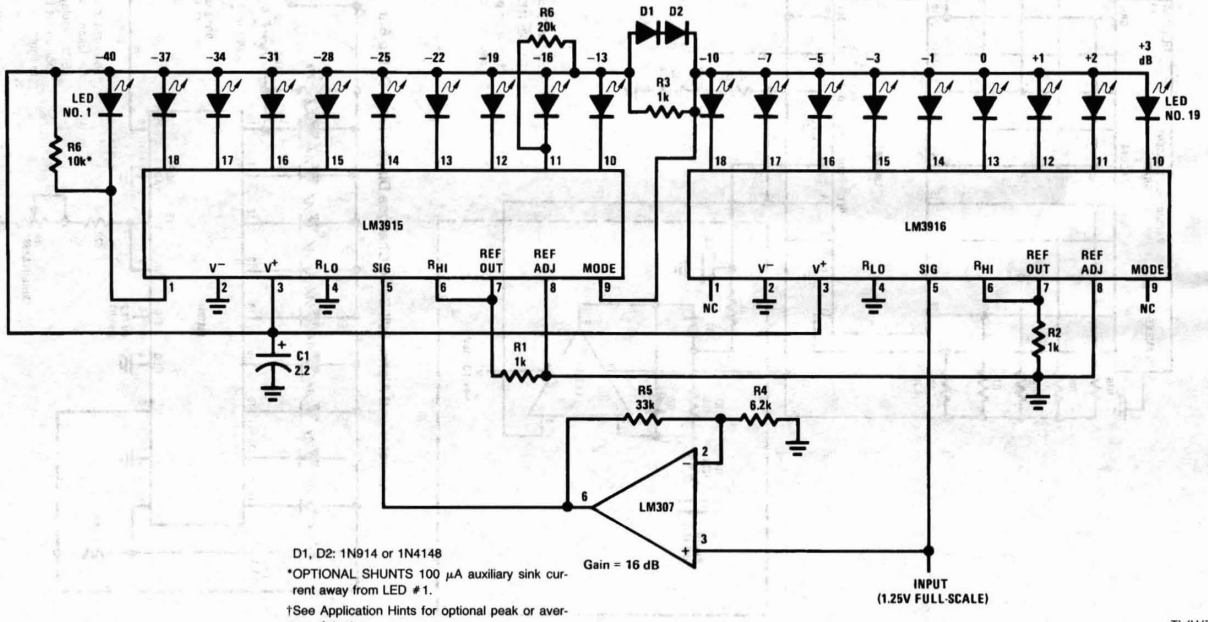
This application shows that the LED supply requires minimal filtering.

*See Application Hints for optional Peak or Average Detector.

†Adjust R3 for 3 dB difference between LED #11 and LED #12

$$\frac{R3}{R3 + R4} = 0.158 = -16\ dB$$

Extended Range VU Meter (Dot Mode)



D1, D2: 1N914 or 1N4148

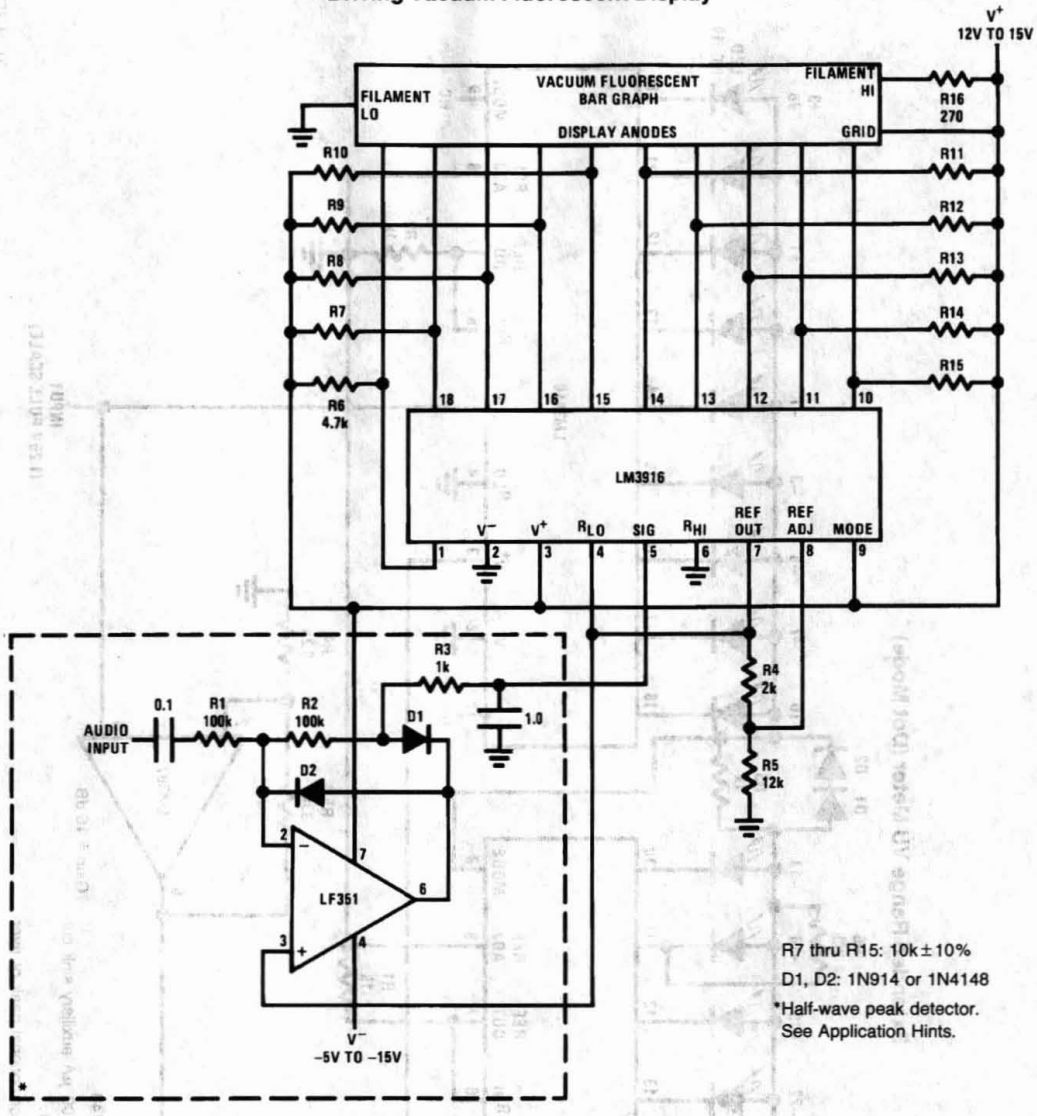
*OPTIONAL SHUNTS 100 μA auxiliary sink current away from LED #1.

†See Application Hints for optional peak or average detector.

TL/H/7971–23

Typical Applications (Continued)

Driving Vacuum Fluorescent Display



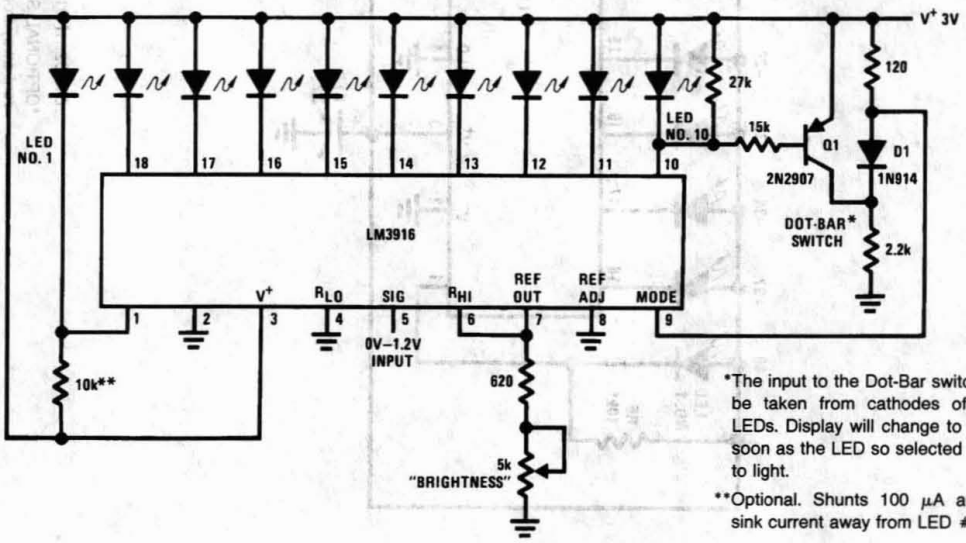
R7 thru R15: 10k ± 10%

D1, D2: 1N914 or 1N4148

*Half-wave peak detector. See Application Hints.

TL/H/7971–24

Indicator and Alarm, Full-Scale Changes Display From Dot to Bar



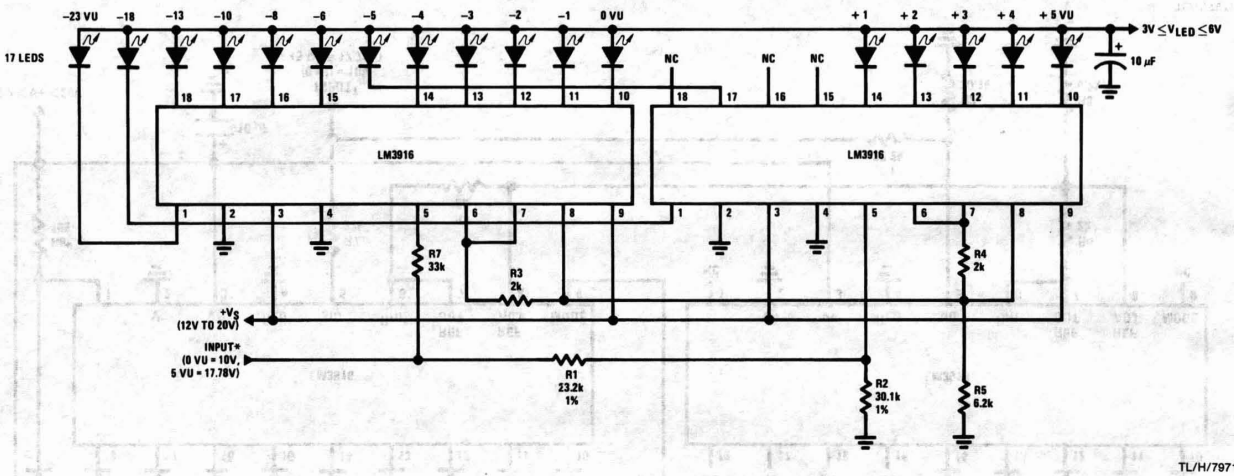
*The input to the Dot-Bar switch may be taken from cathodes of other LEDs. Display will change to bar as soon as the LED so selected begins to light.

**Optional. Shunts 100 μA auxiliary sink current away from LED #1.

TL/H/7971–25

Typical Applications (Continued)

High Resolution VU Meter (Bar Mode)



TL/H/7971–26

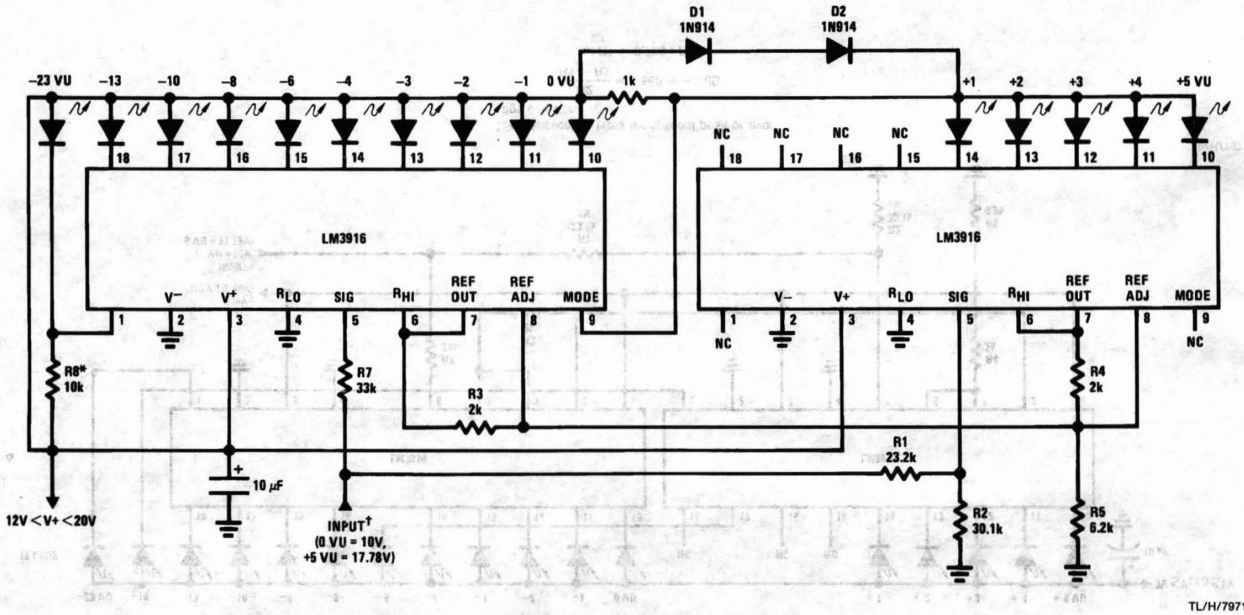
*See Application Hints for optional peak or average detector.

$$\frac{R2}{R1 + R2} \cong 0.562 = -5\ dB$$

or $R1 \cong 0.788 \cdot R2$

Typical Applications (Continued)

High Resolution VU Meter (Dot Mode)



TL/H/7971–27

*Optional shunts 100 µA auxiliary sink current away from LED #1.

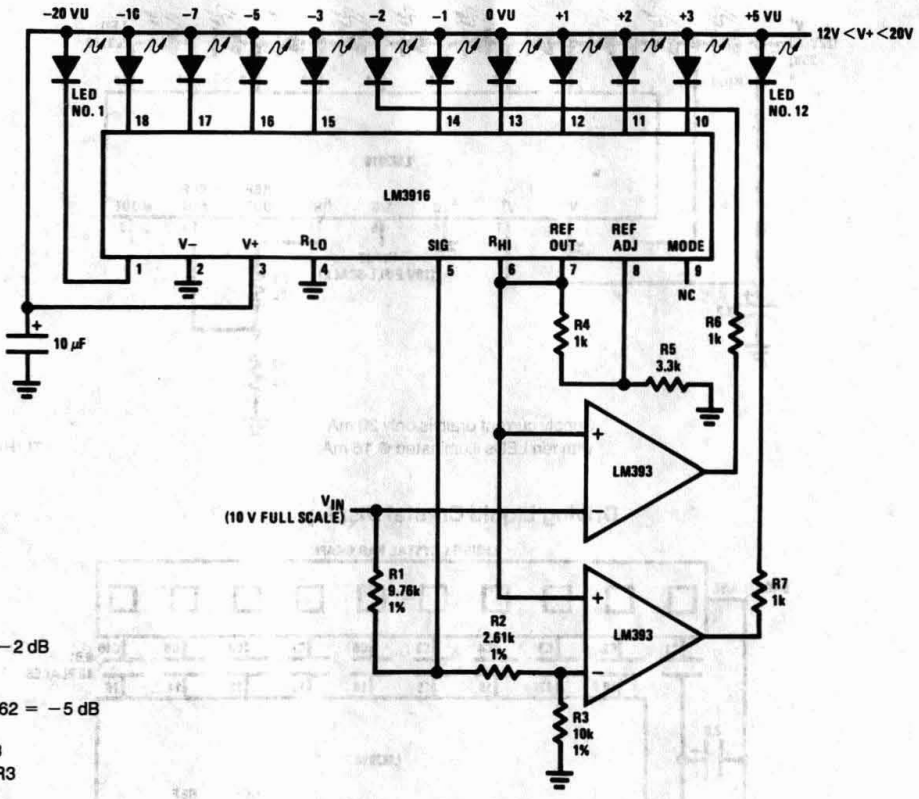
†See Application Hints for optional peak or average detector.

$$\frac{R2}{R1 + R2} \cong 0.562 = -5\ dB$$

$$\text{or } R1 \cong 0.788 \bullet R2$$

Typical Applications (Continued)

Displaying Additional Levels



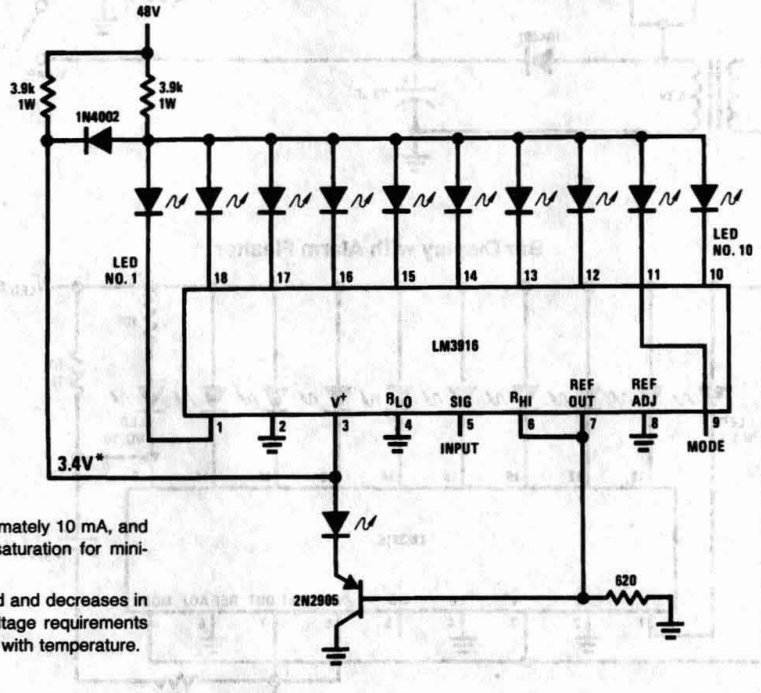
$$\frac{R3}{R2 + R3} \cong 0.794 = -2\,dB$$

$$\frac{R2 + R3}{R1 + R2 + R3} \cong 0.562 = -5\,dB$$

or R2 = 0.259 • R3
and R1 = 0.979 • R3

TL/H/7971–28

Operating with a High Voltage Supply (Dot Mode Only)



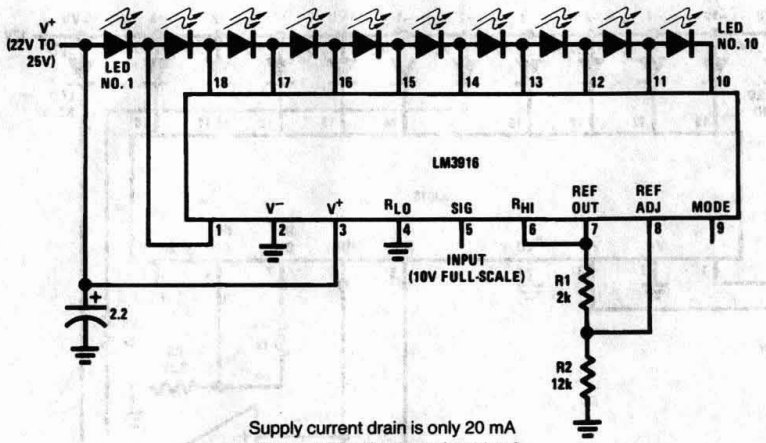
The LED currents are approximately 10 mA, and LM3916 outputs operate in saturation for minimum dissipation.

*This point is partially regulated and decreases in voltage with temperature. Voltage requirements of the LM3916 also decrease with temperature.

TL/H/7971–29

Typical Applications (Continued)

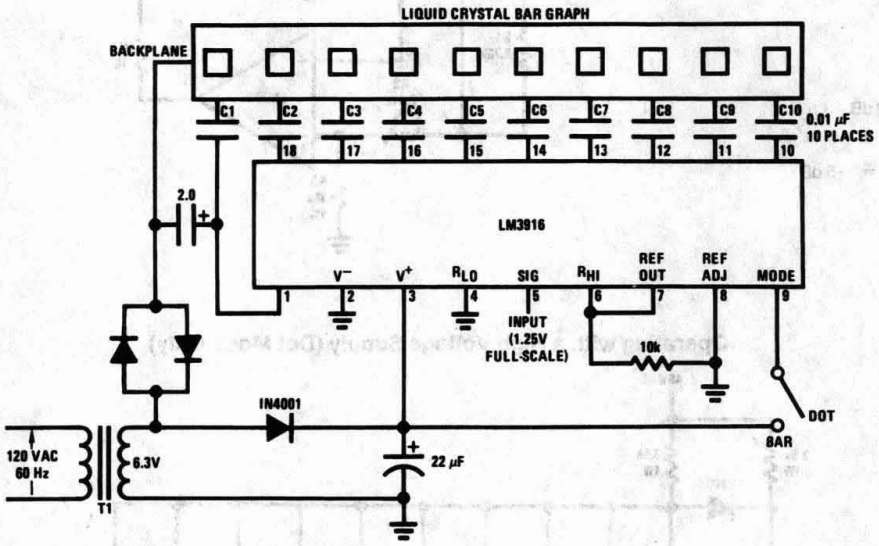
Low Current Bar Mode Display



Supply current drain is only 20 mA with ten LEDs illuminated @ 16 mA.

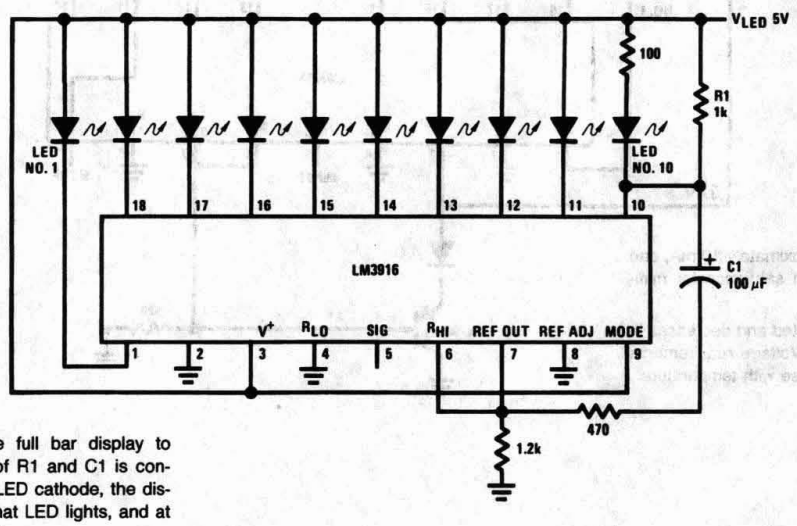
TL/H/7971–30

Driving Liquid Crystal Display



TL/H/7971–31

Bar Display with Alarm Flasher

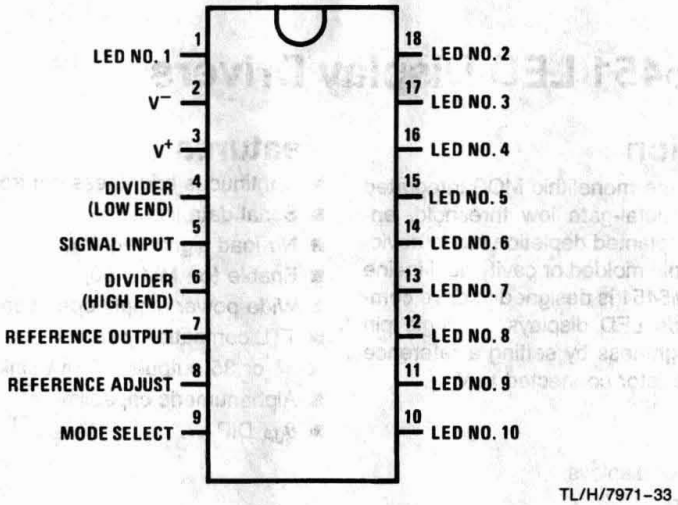


Full-scale causes the full bar display to flash. If the junction of R1 and C1 is connected to a different LED cathode, the display will flash when that LED lights, and at any higher input signal.

TL/H/7971–32

Connection Diagram

Dual-In-Line Package



TL/H/7971–33

Top View

Order Number LM3916N
See NS Package Number N18A

Definition of Terms

Absolute Accuracy: The difference between the observed threshold voltage and the ideal threshold voltage for each comparator. Specified and tested with 10V across the internal voltage divider so that resistor ratio matching error predominates over comparator offset voltage.

Adjust Pin Current: Current flowing out of the reference amplifier pin when the reference amplifier is in the linear region.

Comparator Gain: The ratio of the change in output current (I_{LED}) to the change in input voltage (V_{IN}) required to produce it for a comparator in the linear region.

Dropout Voltage: The voltage measured at the current source outputs required to make the output current fall by 10%.

Input Bias Current: Current flowing out of the signal input when the input buffer is in the linear region.

LED Current Regulation: The change in output current over the specified range of LED supply voltage (V_{LED}) as measured at the current source outputs. As the forward voltage of an LED does not change significantly with a small change in forward current, this is equivalent to changing the voltage at the LED anodes by the same amount.

Line Regulation: The average change in reference output voltage (V_{REF}) over the specified range of supply voltage (V^+).

Load Regulation: The change in reference output voltage over the specified range of load current ($I_{L(REF)}$).

Offset Voltage: The differential input voltage which must be applied to each comparator to bias the output in the linear region. Most significant error when the voltage across the internal voltage divider is small. Specified and tested with pin 6 voltage (V_{RHI}) equal to pin 4 voltage (V_{RLO}).

Relative Accuracy: The difference between any two adjacent threshold points. Specified and tested with 10V across the internal voltage divider so that resistor ratio matching error predominates over comparator offset voltage.

National Semiconductor

MM5450/MM5451 LED Display Drivers

General Description

The MM5450 and MM5451 are monolithic MOS integrated circuits utilizing N-channel metal-gate low threshold, enhancement mode, and ion-implanted depletion mode devices. They are available in 40-pin molded or cavity dual-in-line packages. The MM5450/MM5451 is designed to drive common anode-separate cathode LED displays. A single pin controls the LED display brightness by setting a reference current through a variable resistor connected to V_{DD}.

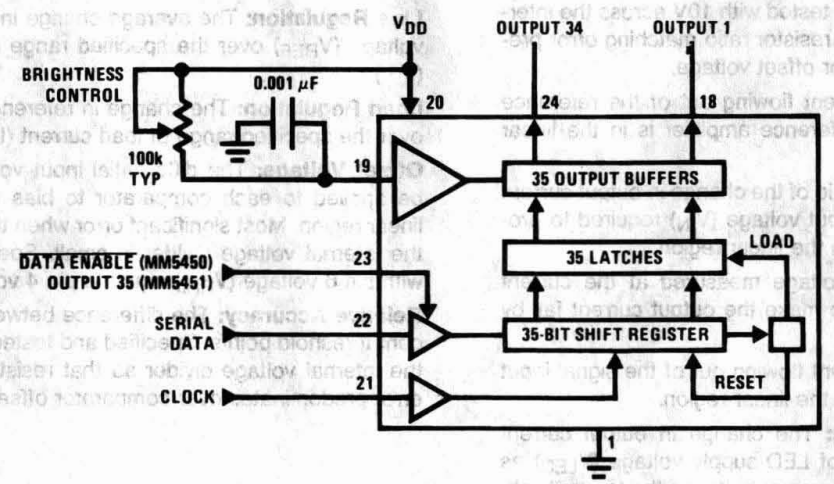
Applications

- COPS™ or microprocessor displays
- Industrial control indicator
- Relay driver
- Digital clock, thermometer, counter, voltmeter
- Instrumentation readouts

Features

- Continuous brightness control
- Serial data input
- No load signal required
- Enable (on MM5450)
- Wide power supply operation
- TTL compatibility
- 34 or 35 outputs, 15 mA sink capability
- Alphanumeric capability
- θ_{JA} DIP — Board = 49°C/W, Socket = 54°C/W

Block Diagram



TL/F/6136–1

FIGURE 1

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Voltage at Any Pin	$V_{SS} - 0.3V$ to $V_{SS} + 12V$
Operating Temperature	−25°C to +85°C
Storage Temperature	−65°C to +150°C
Junction Temperature	+150°C
Lead Temperature (Soldering, 10 sec.)	300°C

Power Dissipation at +25°C

Molded DIP Package, Board Mount	2.5W*
Molded DIP Package, Socket Mount	2.3W**

*Molded DIP Package board mount, θ_{JA} = 49°C/W, Derate 20.4 mW/°C above 25°C.

**Molded DIP Package, socket mount, θ_{JA} = 54°C/W, Derate 18.5 mW/°C above 25°C.

Electrical Characteristics T_A within operating range, V_{DD} = 4.75V to 11.0V, V_{SS} = 0V unless otherwise specified

Parameter	Conditions	Min	Typ	Max	Units
Power Supply		4.75		11	V
Power Supply Current	Excluding Output Loads			7	mA
Input Voltages					
Logical "0" Level (V_L)	±10 μA Input Bias	−0.3		0.8	V
Logical "1" Level (V_H)	$4.75V \le V_{DD} \le 5.25V$	2.2		V_{DD}	V
	$V_{DD} > 5.25V$	$V_{DD} - 2V$		V_{DD}	V
Brightness Input (Note 2)		0		0.75	mA
Output Sink Current					
Segment OFF	V_{OUT} = 3.0V			10	μA
Segment ON	V_{OUT} = 1V (Note 3)				
	Brightness Input = 0 μA	0		10	μA
	Brightness Input = 100 μA	2.0	2.7	4	mA
	Brightness Input = 750 μA	15		25	mA
Brightness Input Voltage (Pin 19)	Input Current 750 μA	3.0		4.3	V
Output Matching (Note 1)				±20	%
Clock Input	(Notes 5 and 6)				
Frequency, f_C				500	kHz
High Time, t_h		950			ns
Low Time, t_l		950			ns
Data Input					
Set-Up Time, t_{DS}		300			ns
Hold Time, t_{DH}		300			ns
Data Enable Input					
Set-Up Time, t_{DES}		100			ns

Note 1: Output matching is calculated as the percent variation $(I_{MAX} + I_{MIN})/2$.

Note 2: With a fixed resistor on the brightness input pin, some variation in brightness will occur from one device to another. Maximum brightness input current can be 2 mA as long as Note 3 and junction temperature equation are complied with.

Note 3: See *Figures 5, 6,* and *7* for Recommended Operating Conditions and limits. Absolute maximum for each output should be limited to 40 mA.

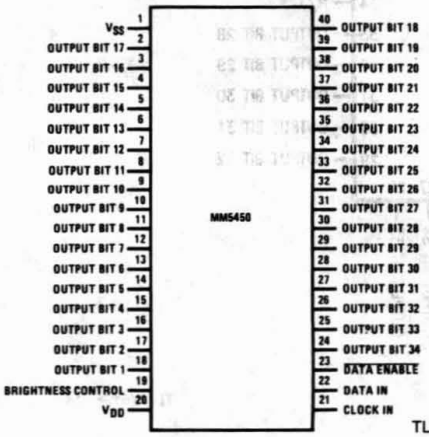
Note 4: The V_{OUT} voltage should be regulated by the user. See *Figures 6* and *7* for allowable V_{OUT} vs I_{OUT} operation.

Note 5: AC input waveform specification for test purpose: $t_r \le 20$ ns, $t_f \le 20$ ns, f = 500 kHz, 50% ±10% duty cycle.

Note 6: Clock input rise and fall times must not exceed 300 ns.

Connection Diagrams

Dual-In-Line Package

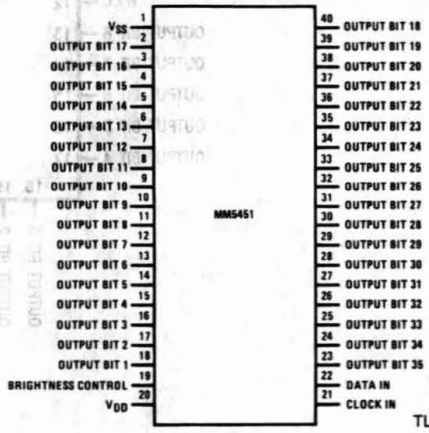


TL/F/6136–2

Top View

FIGURE 2a

Dual-In-Line Package



TL/F/6136–3

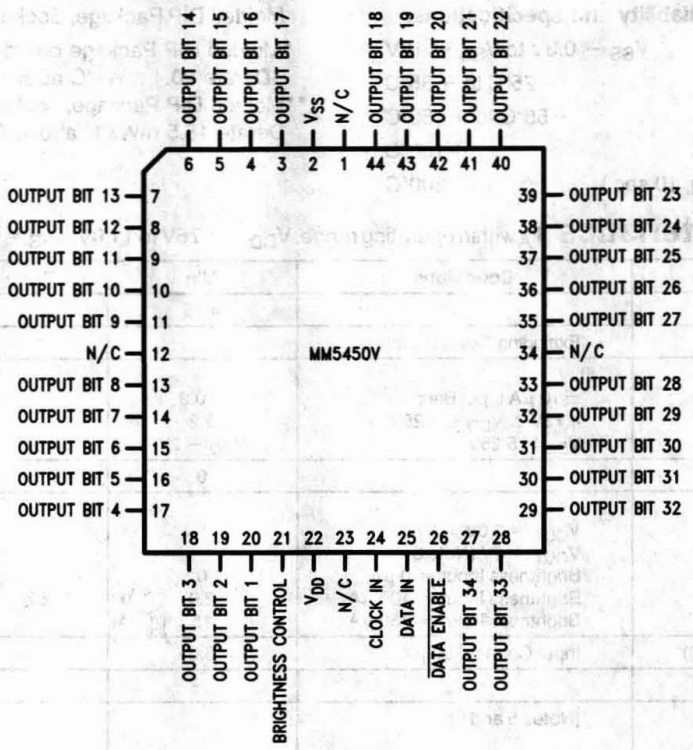
Top View

FIGURE 2b

Order Number MM5450N, MM5451N, MM5450V or MM5451V
See NS Package Number N40A or V44A

Connection Diagrams (Continued)

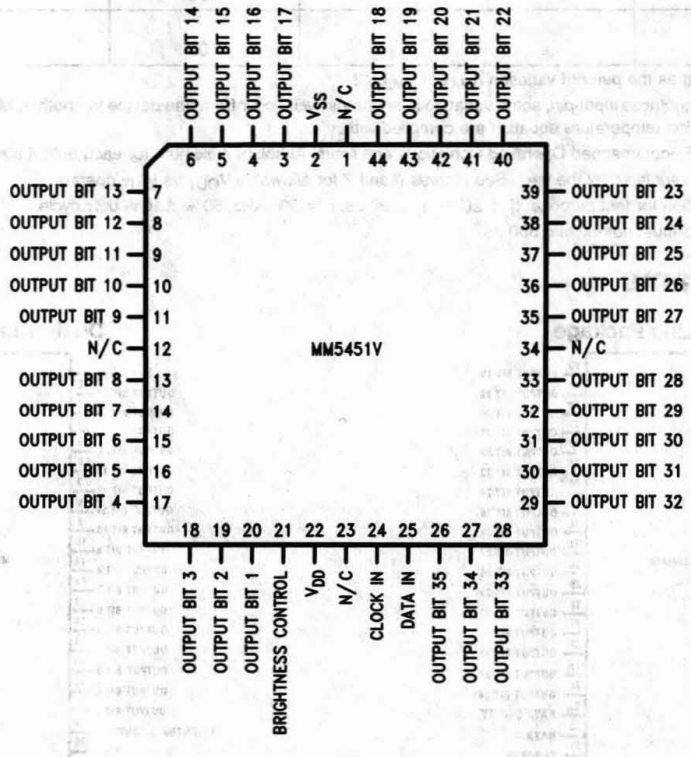
Plastic Chip Carrier



TL/F/6136–13

Top View

Plastic Chip Carrier



TL/F/6136–14

Top View

Functional Description

Both the MM5450 and the MM5451 are specifically designed to operate 4- or 5-digit alphanumeric displays with minimal interface with the display and the data source. Serial data transfer from the data source to the display driver is accomplished with 2 signals, serial data and clock. Using a format of a leading "1" followed by the 35 data bits allows data transfer without an additional load signal. The 35 data bits are latched after the 36th bit is complete, thus providing non-multiplexed, direct drive to the display. Outputs change only if the serial data bits differ from the previous time. Display brightness is determined by control of the output current for LED displays. A 0.001 capacitor should be connected to brightness control, pin 19, to prevent possible oscillations.

A block diagram is shown in *Figure 1.* For the MM5450 a $\overline{\text{DATA ENABLE}}$ is used instead of the 35th output. The $\overline{\text{DATA ENABLE}}$ input is a metal option for the MM5450. The output current is typically 20 times greater than the current into pin 19, which is set by an external variable resistor. There is an internal limiting resistor of 400Ω nominal value.

Figure 4 shows the input data format. A start bit of logical "1" precedes the 35 bits of data. At the 36th clock a LOAD signal is generated synchronously with the high state of the clock, which loads the 35 bits of the shift registers into the latches. At the low state of the clock a RESET signal is generated which clears all the shift registers for the next set of data. The shift registers are static master-slave configuration. There is no clear for the master portion of the first shift register, thus allowing continuous operation.

There must be a complete set of 36 clocks or the shift registers will not clear.

When the chip first powers ON an internal power ON reset signal is generated which resets all registers and all latches. The START bit and the first clock return the chip to its normal operation.

Figure 2 shows the pin-out of the MM5450 and MM5451. Bit 1 is the first bit following the start bit and it will appear on pin 18. A logical "1" at the input will turn on the appropriate LED.

Figure 3 shows the timing relationships between data, clock and $\overline{\text{DATA ENABLE}}$. A max clock frequency of 0.5 MHz is assumed.

For applications where a lesser number of outputs are used, it is possible to either increase the current per output, or operate the part at higher than 1V V_{OUT}. The following equation can be used for calculations.

$$T_j = (V_{OUT})\,(I_{LED})\,(\text{No. of segments})(\theta_{JA}) + T_A$$

where:

T_j = junction temperature, 150°C max

V_{OUT} = the voltage at the LED driver outputs

I_{LED} = the LED current

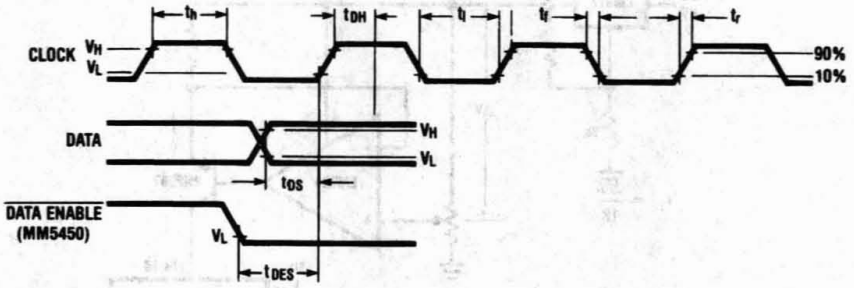
θ_{JA} = thermal coefficient of the package

T_A = ambient temperature

θ_{JA} (Socket Mount) = 54°C/W

θ_{JA} (Board Mount) = 49°C/W

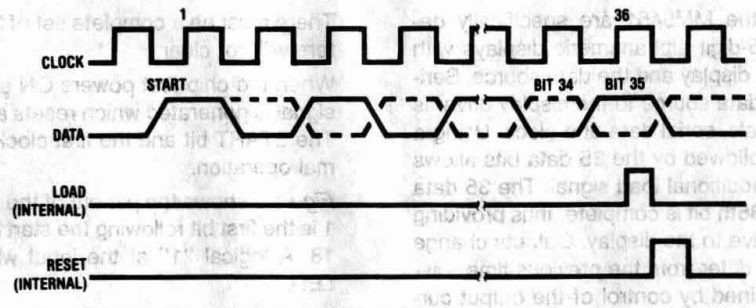
The above equation was used to plot *Figure 5, Figure 6* and *Figure 7.*



TL/F/6136–4

FIGURE 3

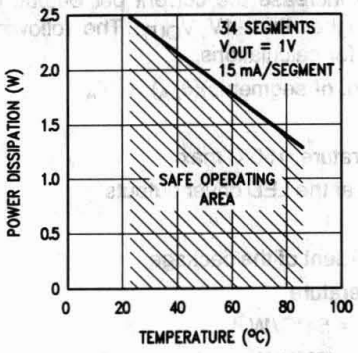
Functional Description (Continued)



TL/F/6136–5

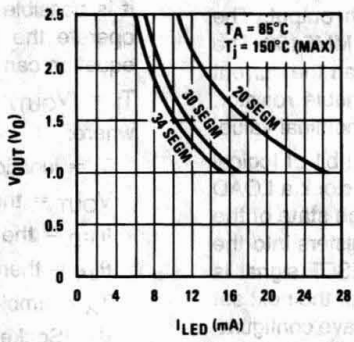
FIGURE 4. Input Data Format

Typical Performance Characteristics



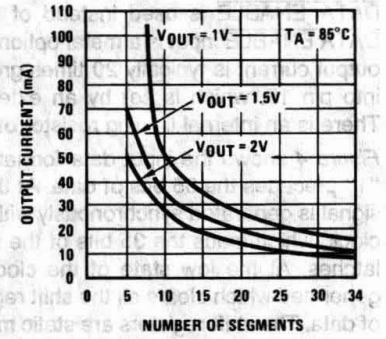
TL/F/6136–6

FIGURE 5



TL/F/6136–7

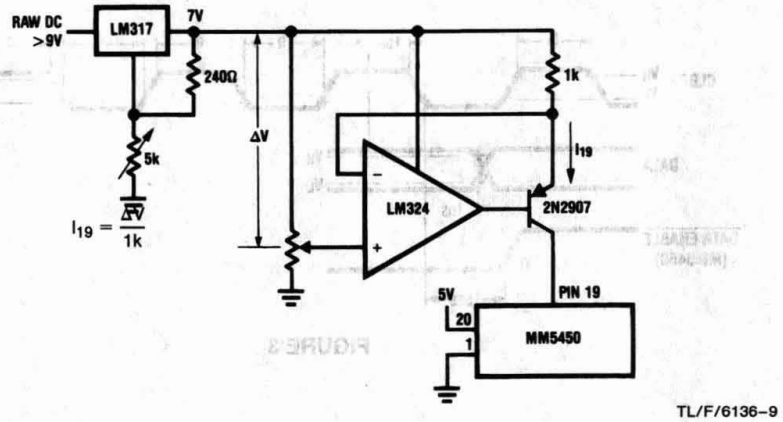
FIGURE 6



TL/F/6136–8

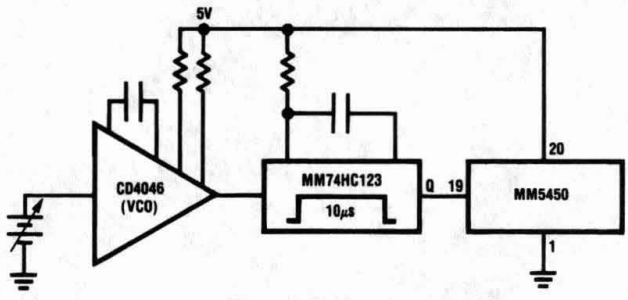
FIGURE 7

Typical Applications



TL/F/6136–9

FIGURE 8. Typical Application of Constant Current Brightness Control

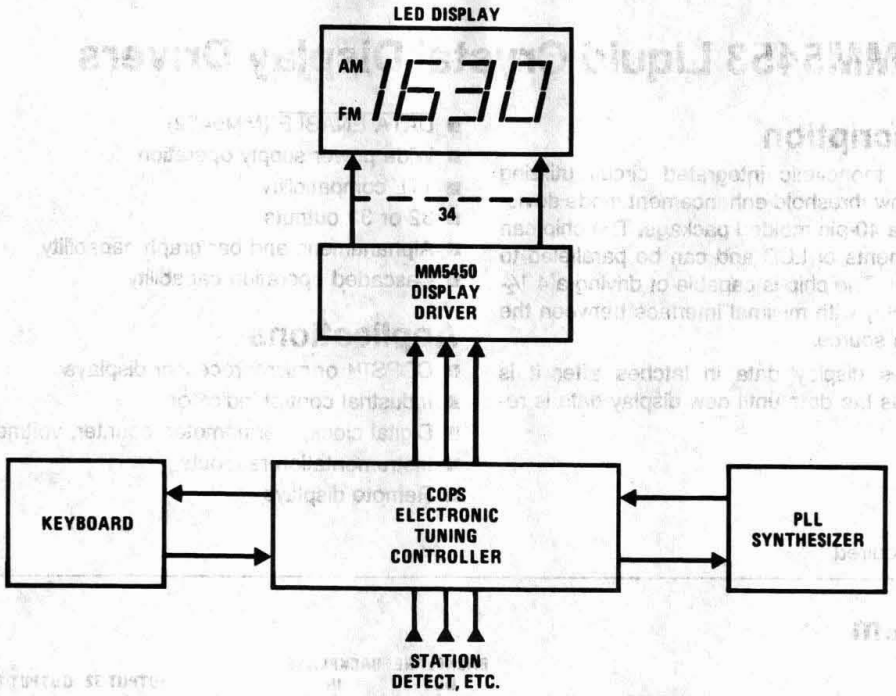


TL/F/6136–10

FIGURE 9. Brightness Control Varying the Duty Cycle

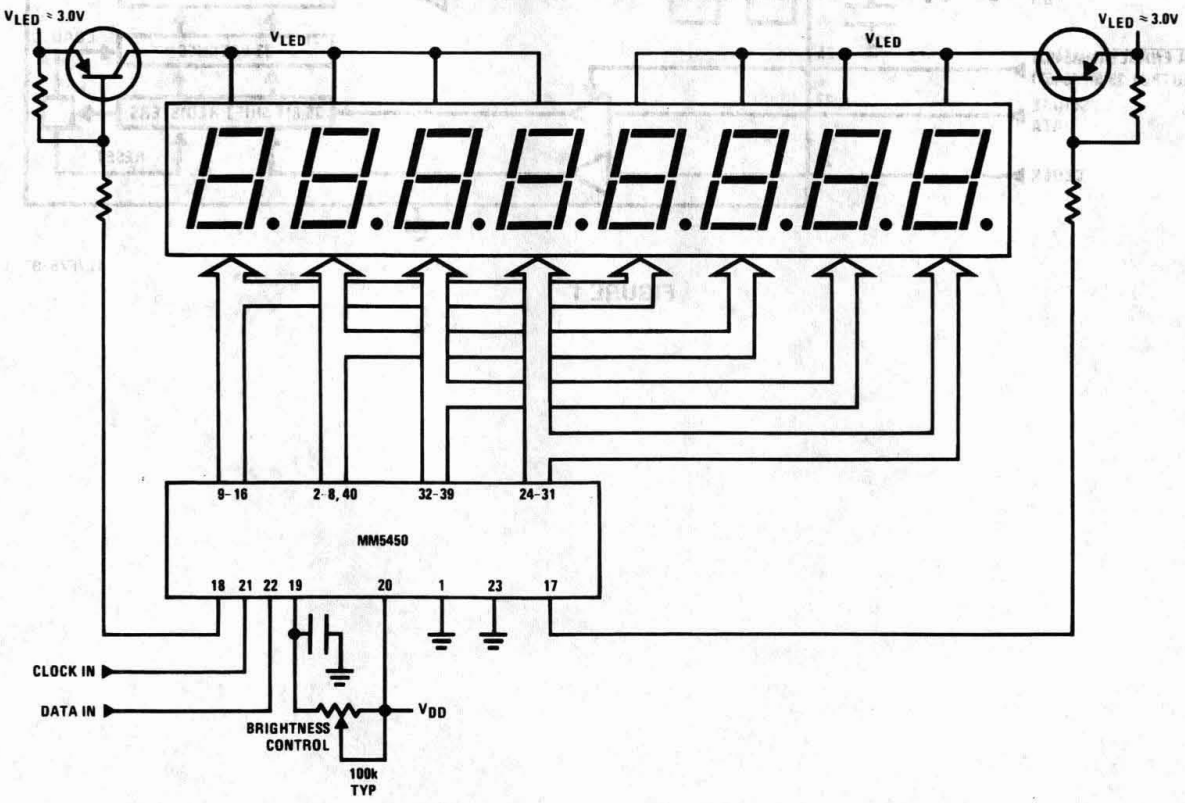
Typical Applications (Continued)

Basic Electronically Tuned Radio System



TL/F/6136–11

Duplexing 8 Digits with One MM5450



TL/F/6136–12

National Semiconductor

MM5452/MM5453 Liquid Crystal Display Drivers

General Description

The MM5452 is a monolithic integrated circuit utilizing CMOS metal gate, low threshold enhancement mode devices. It is available in a 40-pin molded package. The chip can drive up to 32 segments of LCD and can be paralleled to increase this number. The chip is capable of driving a 4 ½-digit 7-segment display with minimal interface between the display and the data source.

The MM5452 stores display data in latches after it is clocked in, and holds the data until new display data is received.

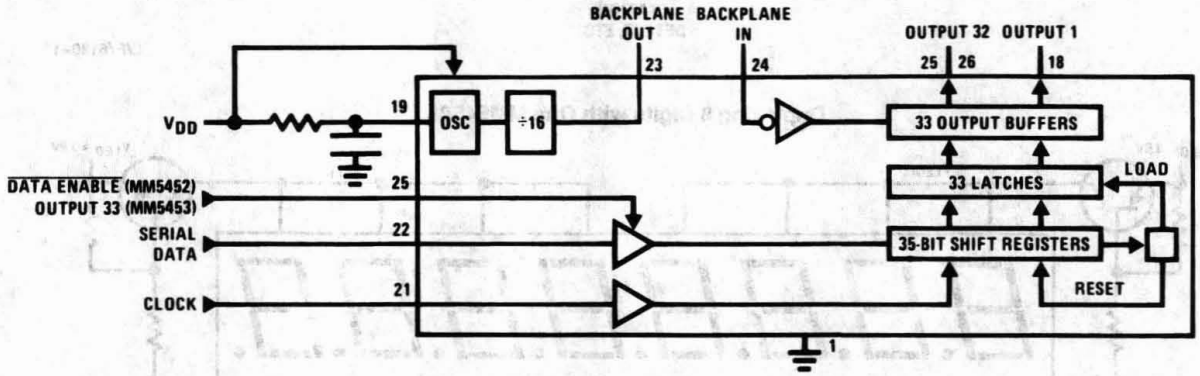
Features

- Serial data input
- No load signal required
- $\overline{\text{DATA ENABLE}}$ (MM5452)
- Wide power supply operation
- TTL compatibility
- 32 or 33 outputs
- Alphanumeric and bar graph capability
- Cascaded operation capability

Applications

- COPS™ or microprocessor displays
- Industrial control indicator
- Digital clock, thermometer, counter, voltmeter
- Instrumentation readouts
- Remote displays

Block Diagram



TL/F/6137–1

FIGURE 1

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Voltage at Any Pin	V_{SS} to V_{SS} + 10V
Operating Temperature	0°C to +70°C
Storage Temperature	−65°C to +150°C
Power Dissipation	300 mW at +70°C 350 mW at +25°C
Junction Temperature	+150°C
Lead Temperature (Soldering, 10 sec.)	300°C

Electrical Characteristics

T_A within operating range, V_{DD} = 3.0V to 10V, V_{SS} = 0V, unless otherwise specified

Parameter	Conditions	Min	Typ	Max	Units
Power Supply		3		10	V
Power Supply Current	Excluding Outputs				
	OSC = V_{SS}, BP IN @ 32 Hz			40	μA
	V_{DD} = 5V, Open Outputs, No Clock			10	μA
Clock Frequency				500	kHz
Input Voltages					
Logical '0' Level	$V_{DD} < 4.75$	−0.3		0.1 V_{DD}	V
	$V_{DD} \geq 4.75$	−0.3		0.8	V
Logical '1' Level	$V_{DD} > 5.25$	0.8 V_{DD}		V_{DD}	V
	$V_{DD} \leq 5.25$	2.0		V_{DD}	V
Output Current Levels					
Segments					
Sink	V_{DD} = 3V, V_{OUT} = 0.3V			−20	μA
Source	V_{DD} = 3V, V_{OUT} = V_{DD} − 0.3V	20			μA
Backplane					
Sink	V_{DD} = 3V, V_{OUT} = 0.3V			−320	μA
Source	V_{DD} = 3V, V_{OUT} = V_{DD} − 0.3V	320			μA
Output Offset Voltage	Segment Load 250 pF Backplane Load 8750 pF (Note 1)			±50	mV
Clock Input Frequency, f_C	(Notes 2 and 3)			500	kHz
High Time, t_h		950			ns
Low Time, t_l		950			ns
Data Input					
Set-Up Time, t_{DS}		300			ns
Hold Time, t_{DH}		300			ns
Data Enable Input					
Set-Up Time, t_{DES}		100			ns

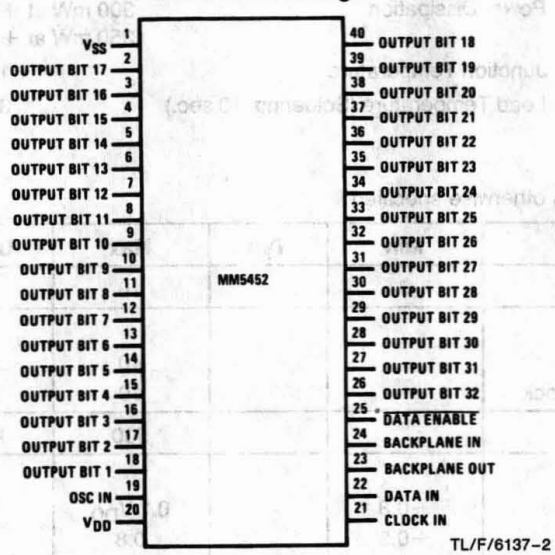
Note 1: This parameter is guaranteed (not 100% production tested) over operating temperature and supply voltage ranges. Not to be used in Q.A. testing.

Note 2: AC input waveform for test purpose: $t_r \leq 20$ ns, $t_f \leq 20$ ns, f = 500 kHz, 50% ±10% duty cycle.

Note 3: Clock input rise and fall times must not exceed 300 ns.

Connection Diagrams

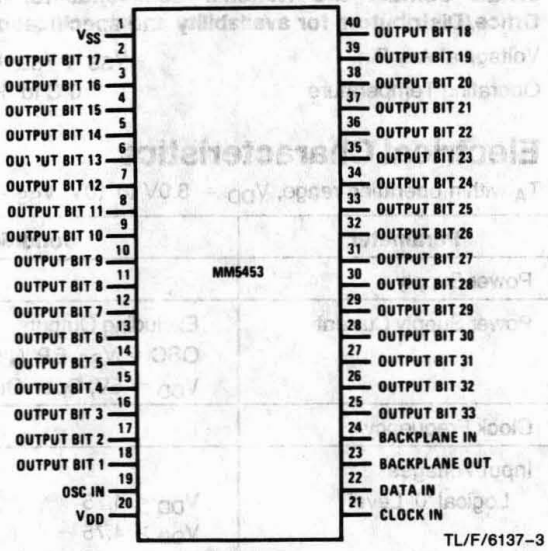
Dual-In-Line Package



TL/F/6137–2

Top View
FIGURE 2a

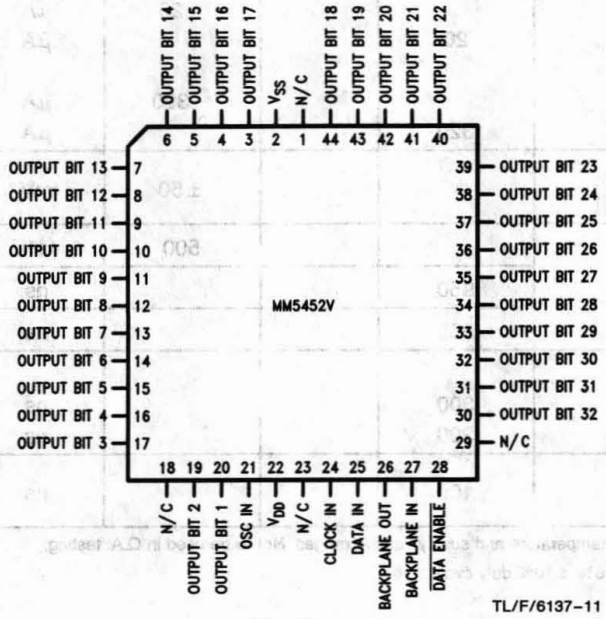
Dual-In-Line Package



TL/F/6137–3

Top View
FIGURE 2b

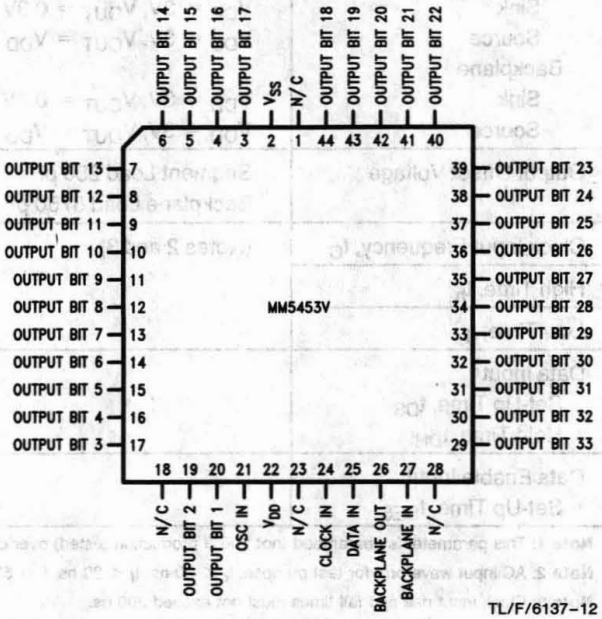
Plastic Chip Carrier



TL/F/6137–11

Top View

Plastic Chip Carrier



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Top View

Order Number MM5452N, MM5453N,
MM5452V or MM5453V
See NS Package Number N40A or V44A

Functional Description

The MM5452 is specifically designed to operate 4 ½-digit 7-segment displays with minimal interface with the display and the data source. Serial data transfer from the data source to the display driver is accomplished with 2 signals, serial data and clock. Since the MM5452 does not contain a character generator, the formatting of the segment information must be done prior to inputting the data to the MM5452. Using a format of a leading "1" followed by the 32 data bits allows data transfer without an additional load signal. The 32 data bits are latched after the 36th clock is complete, thus providing non-multiplexed, direct drive to the display. Outputs change only if the serial data bits differ from the previous time.

A block diagram is shown in *Figure 1.* For the MM5452 a $\overline{\text{DATA ENABLE}}$ is used instead of the 33rd output. If the $\overline{\text{DATA ENABLE}}$ signal is not required, the 33rd output can be brought out. This is the MM5453 device.

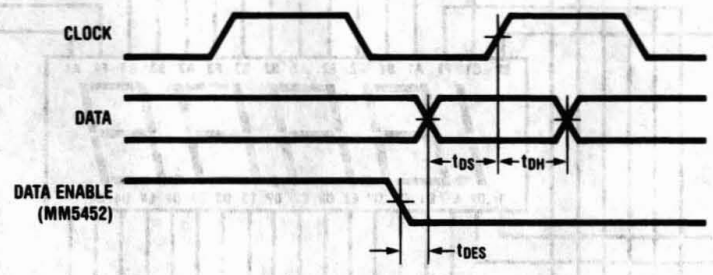
Functional Description (Continued)

Figure 4 shows the input data format. A start bit of logical "1" precedes the 32 bits of data. At the 36th clock a LOAD signal is generated synchronously with the high state of the clock, which loads the 32 bits of the shift registers into the latches. At the low state of the clock a RESET signal is generated which clears all the shift registers for the next set of data. The shift registers are static master-slave configuration. There is no clear for the master portion of the first shift register, thus allowing continuous operation.

If the clock is not continuous, there must be a complete set of 36 clocks otherwise the shift registers will not clear.

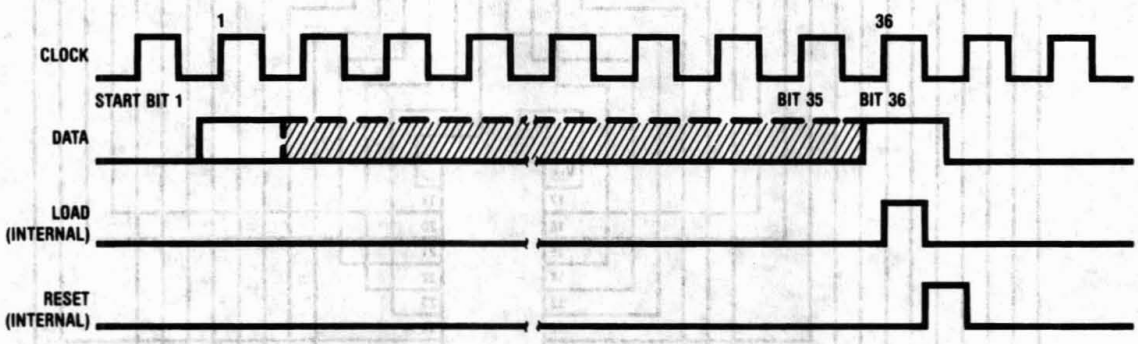
Figure 2a shows the pin-out of the MM5452. Bit 1 is the first bit following the start bit and it will appear on pin 18.

Figure 3 shows the timing relationships between data, clock and DATA ENABLE.



TL/F/6137–4

FIGURE 3

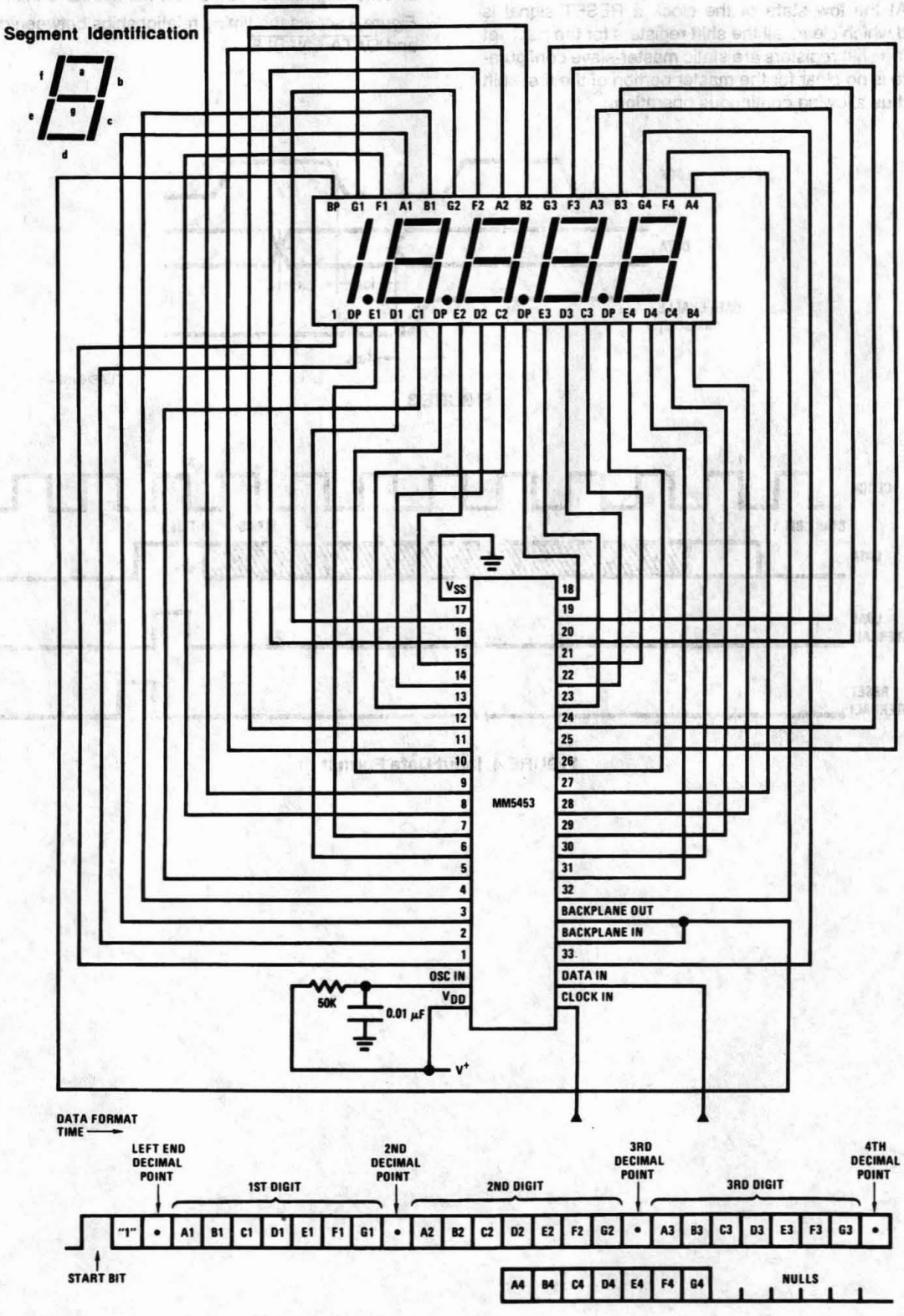


TL/F/6137–5

FIGURE 4. Input Data Format

Functional Description (Continued)

Figure 5 shows a typical application. Note how the input data maps to the output pins and the display. The MM5452 and MM5453 do not have format restrictions, as all outputs are controllable. This application assumes a specific display pinout. Different display/driver connection patterns will, of course, yield a different input data format.

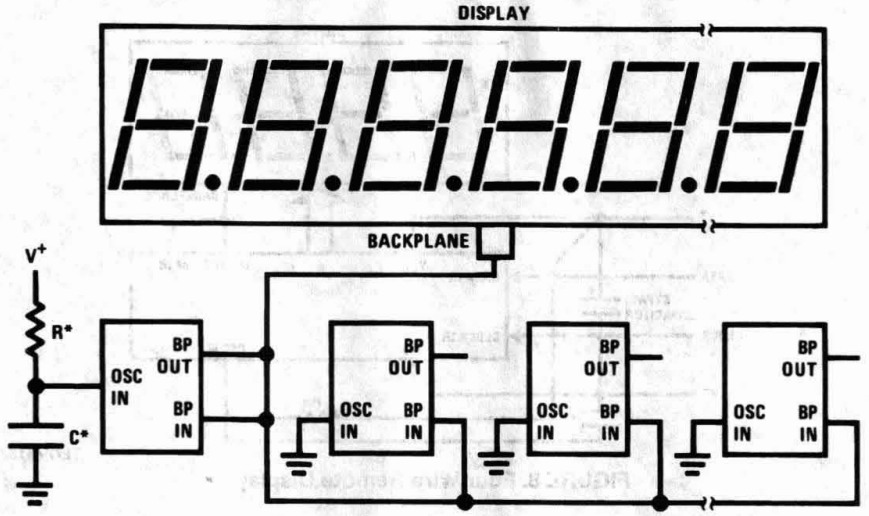


TL/F/6137–6

Consult LCD manufacturer's data sheet for specific pinouts.

FIGURE 5. Typical 4½-Digit Display Application

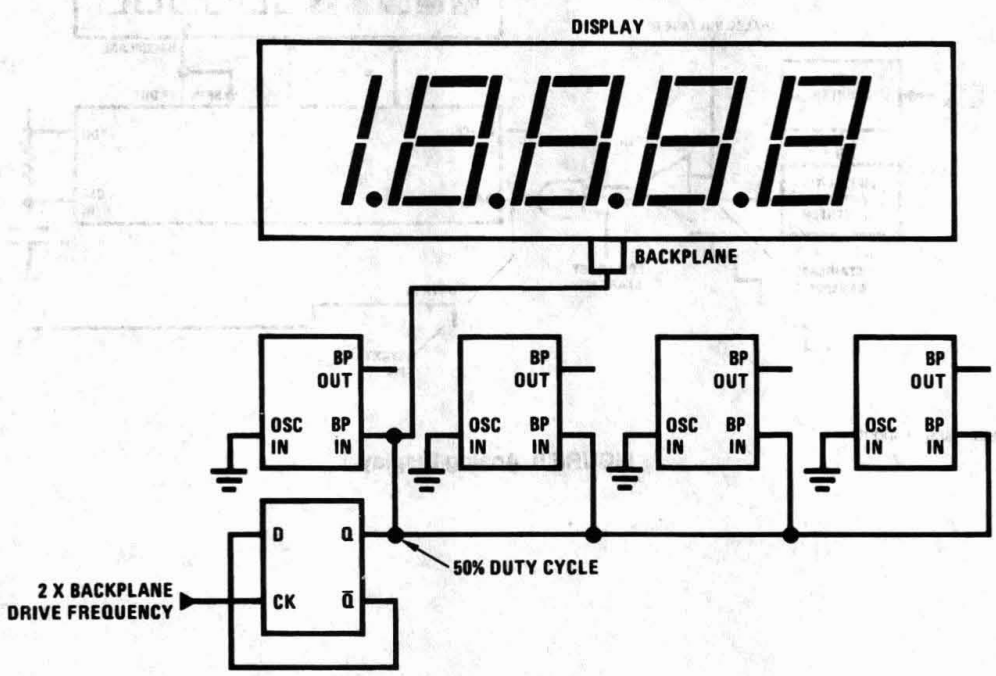
Functional Description (Continued)



TL/F/6137–7

*The minimum recommended value for R for the oscillator input is 9 kΩ. An RC time constant of approximately 4.91×10^{-4} should produce a backplane frequency between 30 Hz and 150 Hz.

FIGURE 6. Parallel Backplane Outputs



TL/F/6137–8

FIGURE 7. External Backplane Clock

Figure 8 shows a four wire remote display that takes advantage of the device's serial input to move many bits of display information on a few wires.

USING AN EXTERNAL CLOCK

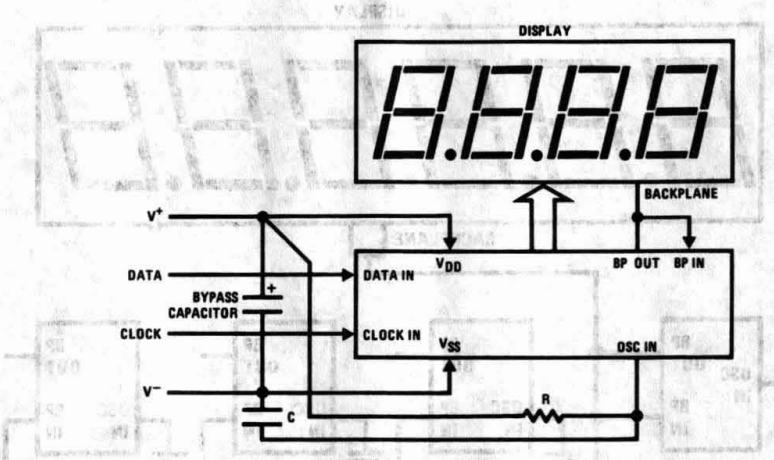
The MM5452/MM5453 LCD Drivers can be used with an externally supplied clock, provided it has a duty cycle of 50%. Deviations from a 50% duty cycle result in an offset voltage on the LCD. In *Figure 7,* a flip-flop is used to assure a 50% duty cycle. The oscillator input is grounded to prevent oscillation and reduce current consumptions in the chips. The oscillator is not used.

Using an external clock allows synchronizing the display drive with AC power, internal clocks, or DVM integration time to reduce interference from the display.

Figure 9 is a general block diagram that shows how the device's serial input can be used to advantage in an analog display. The analog voltage input is compared with a staircase voltage generated by a counter and a digital-to-analog converter or resistor array. The result of this comparison is clocked into the MM5452, MM5453. The next clock pulse increments the staircase and clocks the new data in.

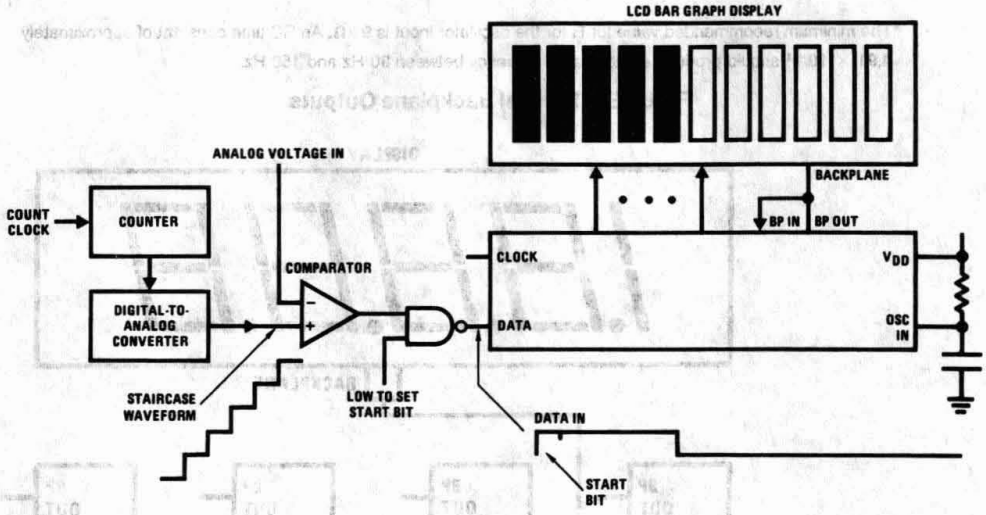
With a buffer amplifier, the same staircase waveform can be used for many displays. The digital-to-analog converter need not be linear; logarithmic or other non-linear functions can be displayed by using weighted resistors or special DACs. This system can be used for status indicators, spectrum analyzers, audio level and power meters, tuning indicators, and other applications.

Functional Description (Continued)



TL/F/6137–9

FIGURE 8. Four Wire Remote Display



TL/F/6137–10

Data is high until staircase > input

FIGURE 9. Analog Display

National Semiconductor

MM5480 LED Display Driver

General Description

The MM5480 is a monolithic MOS integrated circuit utilizing N-channel metal gate low threshold, enhancement mode and ion-implanted depletion mode devices. It utilizes the MM5451 die packaged in a 28-pin package making it ideal for a 3½ digit display. The MM5480 is designed to drive common anode-separate cathode LED displays. A single pin controls the LED display brightness by setting a reference current through a variable resistor connected either to V_{DD} or to a separate supply of 11V maximum.

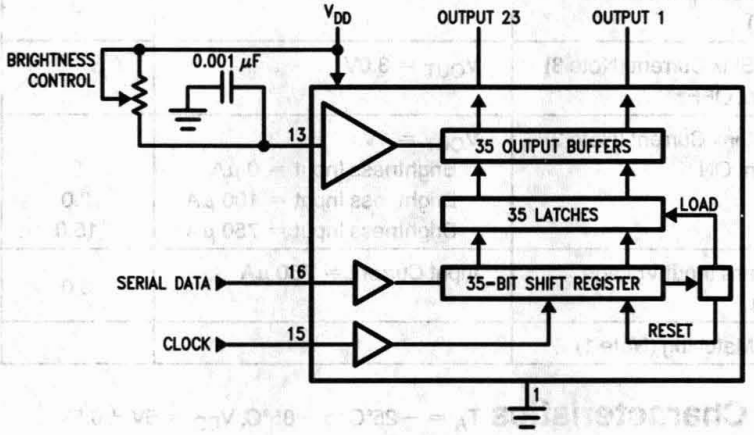
Features

- Continuous brightness control
- Serial data input
- No load signal required
- Wide power supply operation
- TTL compatibility
- Alphanumeric capability
- 3½ digit displays

Applications

- COPS™ microcontrollers or microprocessor displays
- Industrial control indicator
- Relay driver
- Digital clock, thermometer, counter, voltmeter
- Instrumentation readouts

Block Diagram

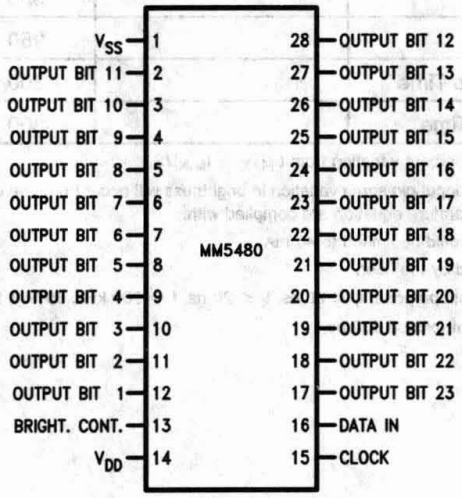


TL/F/6138–1

FIGURE 1

Connection Diagram

Dual-In-Line Package



Order Number MM5480N
See NS Package Number N28B

TL/F/6138–2

Top View
FIGURE 2

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Voltage at Any Pin	$V_{SS} - 0.3V$ to $V_{SS} + 12V$
Storage Temperature	−65°C to +150°C

Power Dissipation at 25°C	
Molded DIP Package, Board Mount	2.4W*
Molded DIP Package, Socket Mount	2.1W**
Junction Temperature	150°C
Lead Temperature (Soldering, 10 sec.)	300°C

*Molded DIP Package, Board Mount, θ_{JA} = 52°C/W, Derate 19.2 mW/°C above 25°C.

**Molded DIP Package, Socket Mount, θ_{JA} = 58°C/W, Derate 17.2 mW/°C above 25°C.

Electrical Characteristics

$T_A = -25°C$ to $+85°C$, $V_{DD} = 4.75V$ to $11.0V$, $V_{SS} = 0V$ unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{DD}	Power Supply		4.75		11	V
I_{DD}	Power Supply Current	Excluding Output Loads			7	mA
V_{IL}	Input Voltage Logical "0" Level	±10 μA Input Bias	−0.3		0.8	V
V_{IH}	Input Voltage Logical "1" Level	$4.75V \le V_{DD} \le 5.25V$	2.2		V_{DD}	V
		$V_{DD} > 5.25V$	$V_{DD} - 2$		V_{DD}	V
I_{BR}	Brightness Input Current (Note 2)		0		0.75	mA
I_{OH}	Output Sink Current (Note 3) Segment OFF	$V_{OUT} = 3.0V$			10.0	μA
I_{OL}	Output Sink Current (Note 3) Segment ON	$V_{OUT} = 1V$				
		Brightness Input = 0 μA	0		10.0	μA
		Brightness Input = 100 μA	2.0	2.7	4.0	mA
		Brightness Input = 750 μA	15.0		25.0	mA
V_{IBR}	Brightness Input Voltage (Pin 13)	Input Current = 750 μA	3.0		4.3	V
OM	Output Matching (Note 1)				±20	%

AC Electrical Characteristics $T_A = -25°C$ to $+85°C$, $V_{DD} = 5V \pm 0.5V$

Symbol	Parameter	Conditions	Min	Typ	Max	Units
f_C	Clock Input Frequency	(Notes 5 and 6)	DC		500	kHz
t_h	High Time		950			ns
t_l	Low Time		950			ns
t_{DS}	Data Input Set-Up Time		300			ns
t_{DH}	Data Input Hold Time		300			ns

Note 1: Output matching is calculated as the percent variation from $(I_{MAX} + I_{MIN})/2$.

Note 2: With a fixed resistor on the brightness input pin some variation in brightness will occur from one device to another. Maximum brightness input current can be 2 mA as long as Note 3 and junction temperature equation are complied with.

Note 3: Absolute maximum for each output should be limited to 40 mA.

Note 4: The V_{OUT} voltage should be regulated by the user.

Note 5: AC input waveform specification for test purpose: $t_r \le 20$ ns, $t_f \le 20$ ns, f = 500 kHz, 50% ±10% duty cycle.

Note 6: Clock input rise and fall times must not exceed 300 ns.

Functional Description

The MM5480 is specifically designed to operate 3½-digit alphanumeric displays with minimal interface with the display and the data source. Serial data transfer from the data source to the display driver is accomplished with 2 signals, serial data and clock. Using a format of a leading "1" followed by the 35 data bits allows data transfer without an additional load signal. The 35 data bits are latched after the 36th bit is complete, thus providing non-multiplexed, direct drive to the display. Outputs change only if the serial data bits differ from the previous time. Display brightness is determined by control of the output current for LED displays. A 0.001 μF ceramic or mica disc capacitor should be connected to brightness control, pin 13, to prevent possible oscillations.

A block diagram is shown in *Figure 1*. The output current is typically 20 times greater than the current into pin 13, which is set by an external variable resistor. There is an internal limiting resistor of 400Ω nominal value.

Figure 4 shows the input data format. A start bit of logical "1" precedes the 35 bits of data. At the 36th clock a LOAD signal is generated synchronously with the high state of the clock, which loads the 35 bits of the shift registers into the latches. At the low state of the clock a RESET signal is generated which clears all the shift registers for the next set of data. The shift registers are static master-slave configuration. There is no clear for the master portion of the first shift register, thus allowing continuous operation.

There must be a complete set of 36 clocks or the shift registers will not clear.

When the chip first powers ON an internal power ON reset signal is generated which resets all registers and all latches. The START bit and the first clock return the chip to its normal operation.

Figure 5 shows the Output Data Format for the 5480. Because it uses only 23 of the possible 35 outputs, 12 of the bits are 'Don't Cares'.

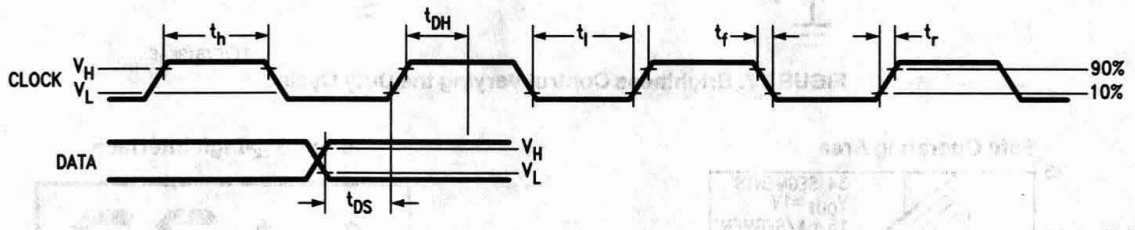
Figure 3 shows the timing relationships between data and clock. A maximum clock frequency of 0.5 MHz is assumed.

For applications where a lesser number of outputs are used, it is possible to either increase the current per output, or operate the part at higher than 1V V_{OUT}. The following equation can be used for calculations.

$$T_j = (V_{OUT})\,(I_{LED})\,(\text{No. of segments})\,(\theta_{JA}) + T_A$$

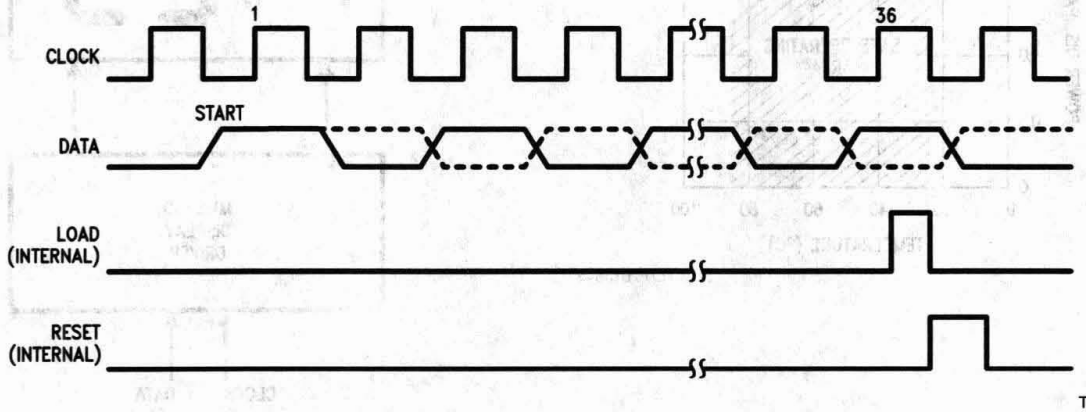
where:

T_j = junction temperature, 150°C max.
V_{OUT} = the voltage at the LED driver outputs
I_{LED} = the LED current
θ_{JA} = thermal coefficient of the package
T_A = ambient temperature
θ_{JA} (Socket Mount) = 58°C/W
θ_{JA} (Board Mount) = 52°C/W



TL/F/6138–3

FIGURE 3



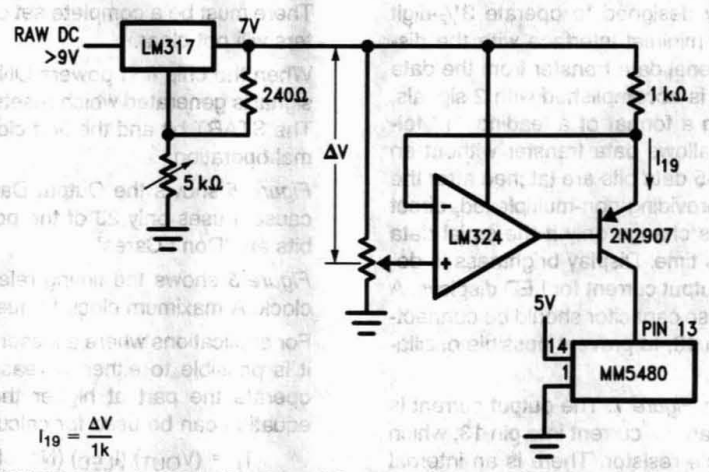
TL/F/6138–4

FIGURE 4. Input Data Format

START	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	5451
START	X	1	2	3	4	5	6	7	X	X	X	8	9	10	11	X	X	X	X	12	13	14	15	16	17	X	18	X	X	19	20	21	22	23	X	5480

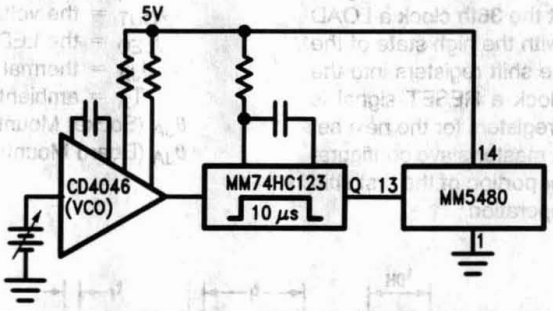
FIGURE 5. Output Data Format

Functional Description (Continued)



TL/F/6138–5

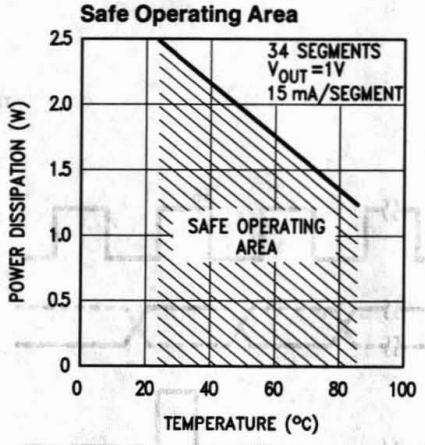
FIGURE 6. Typical Application of Constant Current Brightness Control



TL/F/6138–6

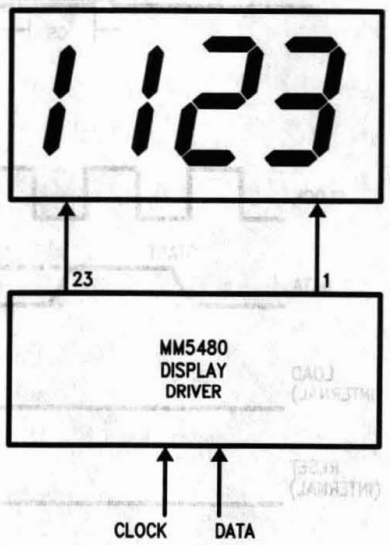
FIGURE 7. Brightness Control Varying the Duty Cycle

Safe Operating Area



TL/F/6138–7

Basic 3½-Digit Interface



TL/F/6138–8

National Semiconductor

MM5481 LED Display Driver

General Description

The 5481 is a monolithic MOS integrated circuit utilizing N-channel metal gate low threshold, enhancement mode and ion-implanted depletion mode devices. It utilizes the MM5450 die packaged in a 20-pin package making it ideal for a 2 digit display. The MM5481 is designed to drive common anode-separate cathode LED displays. A single pin controls the LED display brightness by setting a reference current through a variable resistor connected either to V_{DD} or to a separate supply of 11V maximum.

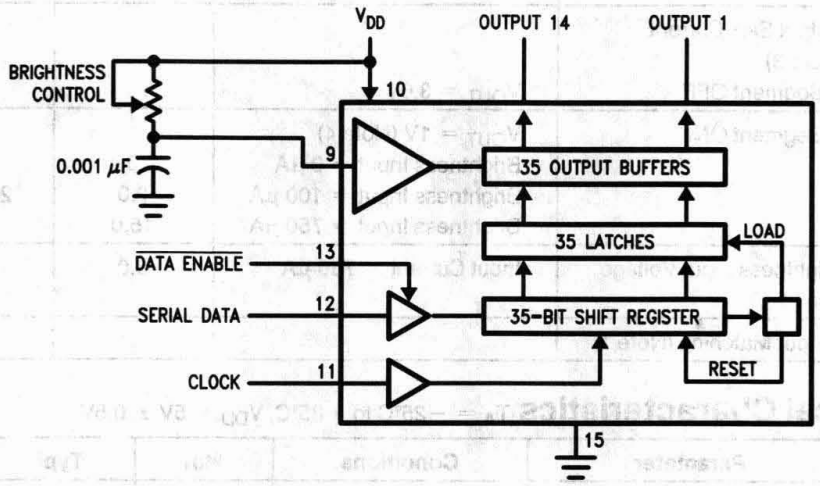
Features

- Continuous brightness control
- Serial data input
- No load signal required
- Data enable
- Wide power supply operation
- TTL compatibility
- Alphanumeric capability
- 2 digit LED driver

Applications

- COPS or microprocessor displays
- Industrial control indicator
- Relay driver
- Instrumentation readouts

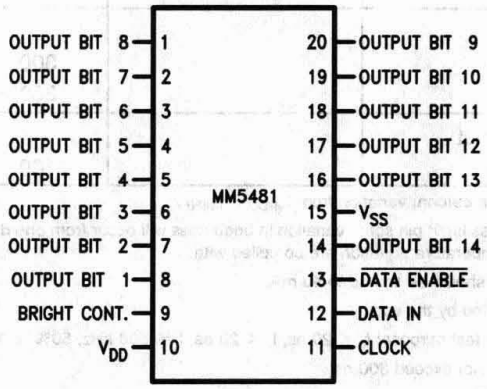
Block and Connection Diagrams



TL/F/6139–1

FIGURE 1

Dual-In-Line Package


OUTPUT BIT 8 — 1
OUTPUT BIT 7 — 2
OUTPUT BIT 6 — 3
OUTPUT BIT 5 — 4
OUTPUT BIT 4 — 5
OUTPUT BIT 3 — 6
OUTPUT BIT 2 — 7
OUTPUT BIT 1 — 8
BRIGHT CONT. — 9
V_{DD} — 10
MM5481
20 — OUTPUT BIT 9
19 — OUTPUT BIT 10
18 — OUTPUT BIT 11
17 — OUTPUT BIT 12
16 — OUTPUT BIT 13
15 — V_{SS}
14 — OUTPUT BIT 14
13 — DATA ENABLE
12 — DATA IN
11 — CLOCK

TL/F/6139–2

Top View
FIGURE 2

Order Number MM5481N
See NS Package Number N20A

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Voltage at Any Pin	V_{SS} to V_{SS} + 12V
Storage Temperature	−65°C to +150°C
Power Dissipation at 25°C	
Molded DIP Package, Board Mount	2W*
Molded DIP Package, Socket Mount	1.8W**
Junction Temperature	+150°C
Lead Temperature (Soldering, 10 sec.)	300°C

*Molded DIP Package, Board Mount, θ_{JA} = 61°C/W, Derate 16.4 mW/°C above 25°C.

**Molded DIP Package, Socket Mount, θ_{JA} = 67°C/W, Derate 14.9 mW/°C above 25°C.

Electrical Characteristics

T_A = −25°C to +85°C, V_{DD} = 4.75V to 11.0V, V_{SS} = 0V unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{DD}	Power Supply		4.75		11	V
I_{DD}	Power Supply Current	Excluding Output Loads			7	mA
V_{IL}	Input Voltages Logical "0" Level	±10 μA Input Bias	−0.3		0.8	V
V_{IH}	Logical "1" Level	4.75 ≤ V_{DD} ≤ 5.25	2.2		V_{DD}	V
		V_{DD} > 5.25	V_{DD} − 2		V_{DD}	V
I_{BR}	Brightness Input Current (Note 2)		0		0.75	mA
I_{OH}	Output Sink Current (Note 3) Segment OFF	V_{OUT} = 3.0V			10.0	μA
I_{OL}	Segment ON	V_{OUT} = 1V (Note 4) Brightness Input = 0 μA Brightness Input = 100 μA Brightness Input = 750 μA	 0 2.0 15.0	 2.7	 10.0 4.0 25.0	 μA mA mA
V_{IBR}	Brightness Input Voltage (Pin 9)	Input Current = 750 μA	3.0		4.3	V
OM	Output Matching (Note 1)				±20	%

AC Electrical Characteristics T_A = −25°C to +85°C, V_{DD} = 5V ± 0.5V

Symbol	Parameter	Conditions	Min	Typ	Max	Units
f_C	Clock Input Frequency	(Notes 5 and 6)	DC		500	kHz
t_h	High Time		950			ns
t_l	Low Time		950			ns
	Data Input					
t_{DS}	Set-Up Time		300			ns
t_{DH}	Hold Time		300			ns
t_{DES}	Data Enable Input Set-Up Time		100			ns

Note 1: Output matching is calculated as the percent variation from $I_{MAX} + I_{MIN}/2$.

Note 2: With a fixed resistor on the brightness input pin some variation in brightness will occur from one device to another. Maximum brightness input current can be 2 mA as long as Note 3 and junction temperature equation are compiled with.

Note 3: Absolute maximum for each output should be limited to 40 mA.

Note 4: The V_{OUT} voltage should be regulated by the user.

Note 5: AC input waveform specification for test purpose: $t_r \leq 20$ ns, $t_f \leq 20$ ns, f = 500 kHz, 50% ± 10% duty cycle.

Note 6: Clock input rise and fall times must not exceed 300 ns.

Functional Description

The MM5481 uses the MM5450 die which is packaged to operate 2-digit alphanumeric displays with minimal interference to the display and the data source. Serial data transfer from the data source to the display driver is accomplished with 2 signals, serial data and clock. Using a format of a leading "1" followed by the 35 data bits allows data transfer without an additional load signal. The 35 data bits are latched after the 36th bit is complete, thus providing non-multiplexed, direct drive to the display. Outputs change only if the serial data bits differ from the previous time. Display brightness is determined by control of the output current for LED displays. A 0.001 μF capacitor should be connected to brightness control, pin 9, to prevent possible oscillations.

A block diagram is shown in *Figure 1*. The output current is typically 20 times greater than the current into pin 9, which is set by an external variable resistor. There is an internal limiting resistor of 400Ω nominal value.

Figure 4 shows the input data format. A start bit of logical "1" precedes the 35 bits of data. At the positive-going-edge of the 36th clock a LOAD signal is generated synchronously with the high state of the clock, which loads the 35 bits of the shift registers into the latches. At the low state of the clock a RESET signal is generated which clears all the shift registers for the next set of data. The shift registers are a static master-slave configuration. There is no clear for the master portion of the first shift register, thus allowing continous operation.

There must be a complete set of 36 clocks (high/low edges) or the shift registers will not clear.

Data Enable

This active low signal enables the data input pin. If high, the shift register sees zeroes clocked in.

To blank the display at any time, (i.e., power on), clock in 36 or more zeroes, followed by a 'one' (start bit), followed by 36 or more zeroes.

Figure 5 shows the Output Data Format for the MM5481. Because it uses only 14 of the possible 34 outputs, 20 of the bits are 'Don't Cares'. Note that only alternate groups of 4 outputs are used.

Figure 3 shows the timing relationships between data, clock, and data enable. A maximum clock frequency of 0.5 MHz is assumed.

For applications where a lesser number of outputs are used, it is possible to either increase the current per output, or operate the part at higher than 1V V_{OUT}. The following equation can be used for calculations.

$T_j = (V_{OUT})\ (I_{LED})\ (\text{No. of segments})\ (\theta_{JA}) + T_A$

where:

T_j = junction temperature, 150°C max.

V_{OUT} = the voltage at the LED driver outputs

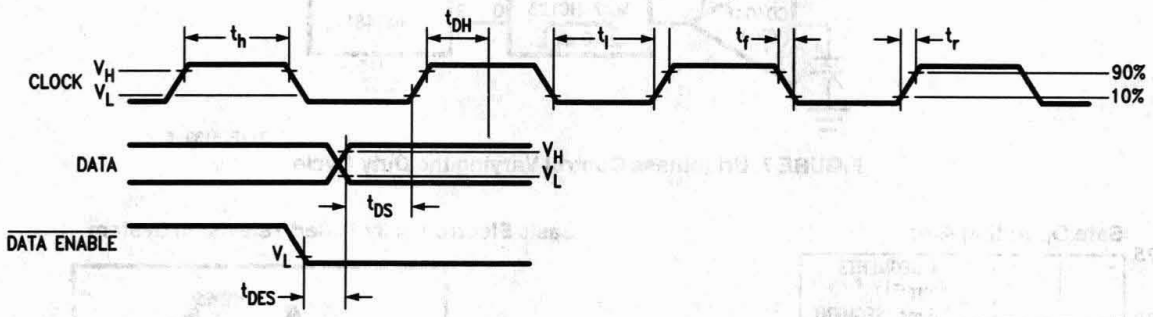
I_{LED} = the LED current

θ_{JA} = thermal coefficient of the package

T_A = ambient temperature

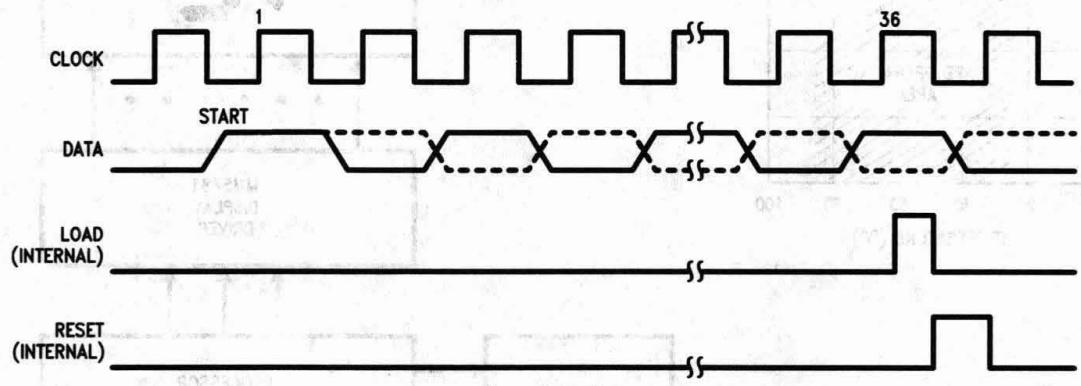
θ_{JA} (Socket Mount) = 67°C/W

θ_{JA} (Board Mount) = 61°C/W



TL/F/6139–3

FIGURE 3. Timing



TL/F/6139–4

FIGURE 4. Input Data Format

Functional Description (Continued)

START	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	5450
START	X	X	X	X	1	2	3	4	X	X	X	X	5	6	7	8	X	X	X	X	9	10	11	12	X	X	X	X	13	14	X	X	X	X	5481

FIGURE 5. Output Data Format

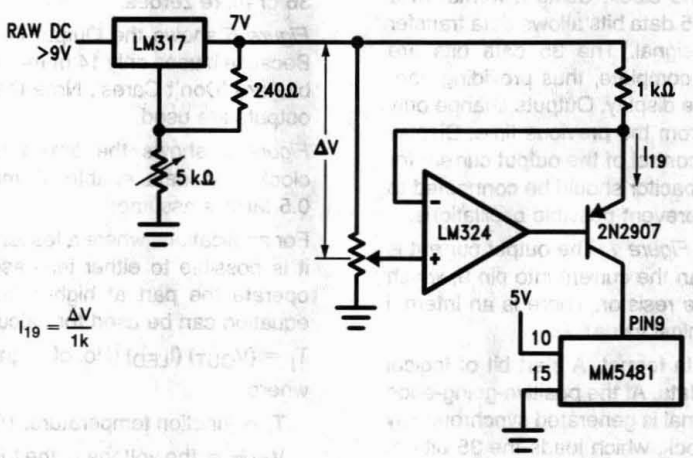


FIGURE 6. Typical Application of Constant Current Brightness Control

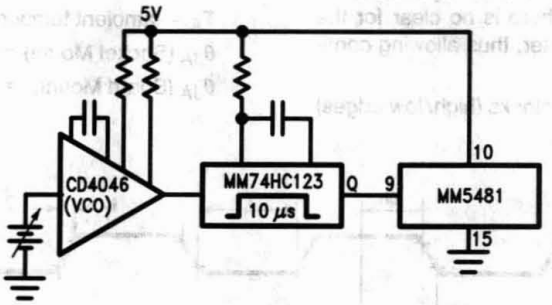
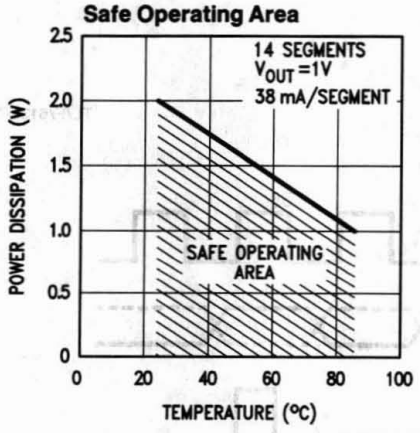
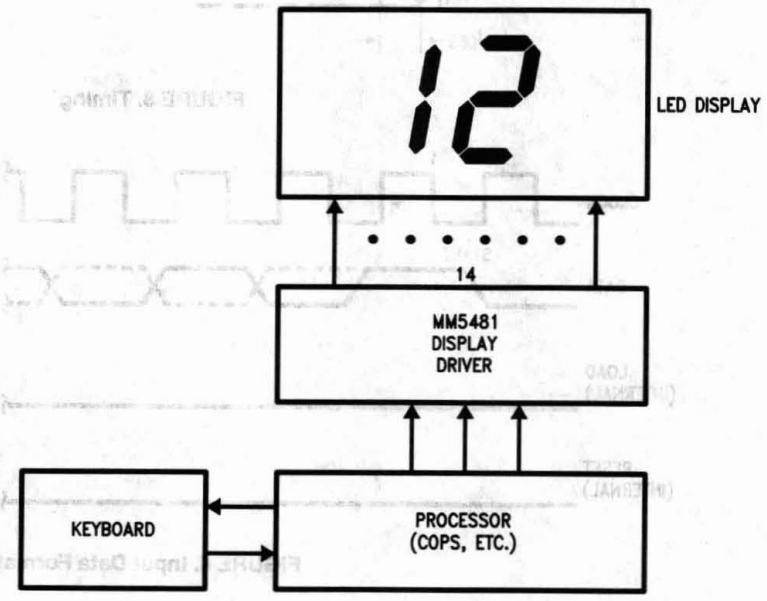


FIGURE 7. Brightness Control Varying the Duty Cycle

Safe Operating Area



Basic Electronically Tuned Television System



National Semiconductor

MM5483 Liquid Crystal Display Driver

General Description

The MM5483 is a monolithic integrated circuit utilizing CMOS metal-gate low-threshold enhancement mode devices. It is available in a 40-pin molded package. The chip can drive up to 31 segments of LCD and can be cascaded to increase this number. This chip is capable of driving a 4½-digit 7-segment display with minimal interface between the display and the data source.

The MM5483 stores the display data in latches after it is latched in, and holds the data until another load pulse is received

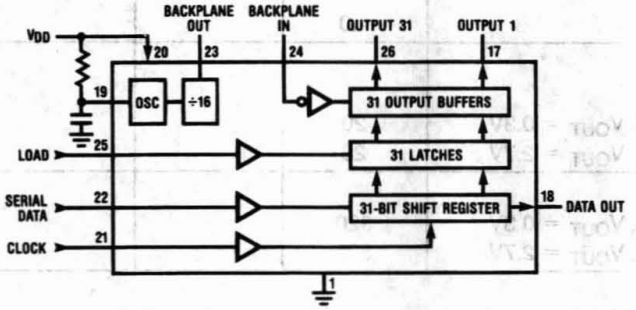
Features

- Serial data input
- Serial data output
- Wide power supply operation
- TTL compatibility
- 31 segment outputs
- Alphanumeric and bar graph capability
- Cascade capability

Applications

- COPS™ or microprocessor displays
- Industrial control indicator
- Digital clock, thermometer, counter, voltmeter
- Instrumentation readouts
- Remote displays

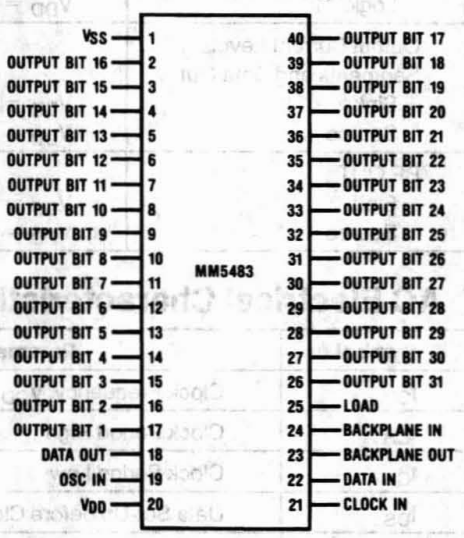
Block and Connection Diagrams



TL/F/6140–1

FIGURE 1

Dual-In-Line Package

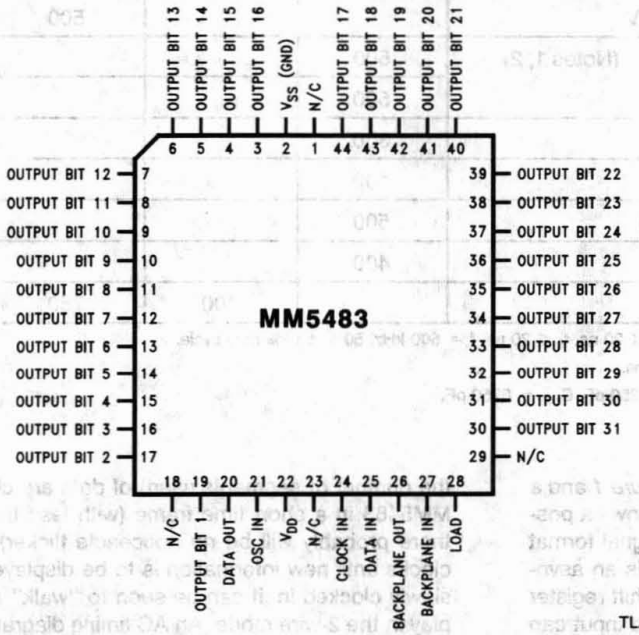


TL/F/6140–2

Top View

FIGURE 2

Order Number MM5483MS or MM5483N
See SSOP Package Number MS40A
See NS Package Number N40A



TL/F/6140–7

Order Number MM5483V
See NS Package Number V44A

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Voltage at Any Pin	V_{SS} to V_{SS} + 10V
Operating Temperature	−40°C to +85°C
Storage Temperature	−65°C to +150°C
Power Dissipation	300 mW at +85°C 350 mW at +25°C
Junction Temperature	+150°C
Lead Temperature (Soldering, 10 seconds)	300°C

DC Electrical Characteristics

T_A within operating range, V_{DD} = 3.0V to 10V, V_{SS} = 0V, unless otherwise specified

Parameter	Conditions	Min	Typ	Max	Units
Power Supply		3.0		10	V
Power Supply Current	R = 1M, C = 470 pF, Outputs Open				
	V_{DD} = 3.0V		9	15	μA
	V_{DD} = 5.0V		17	25	μA
	V_{DD} = 10.0V		35	45	μA
	OSC = 0V, Outputs Open, BPIN = 32 Hz, V_{DD} = 3.0V		1.5	2.5	μA
Input Voltage Levels	Load, Clock, Data				
Logic "0"	V_{DD} = 5.0V			0.9	V
Logic "1"	V_{DD} = 5.0V	2.4			V
Logic "0"	V_{DD} = 3.0V			0.4	V
Logic "1"	V_{DD} = 3.0V	2.0			V
Output Current Levels Segments and Data Out					
Sink	V_{DD} = 3.0V, V_{OUT} = 0.3V	20			μA
Source	V_{DD} = 3.0V, V_{OUT} = 2.7V	20			μA
BP OUT					
Sink	V_{DD} = 3.0V, V_{OUT} = 0.3V	320			μA
Source	V_{DD} = 3.0V, V_{OUT} = 2.7V	320			μA

AC Electrical Characteristics $V_{DD} \geq 4.7V$, V_{SS} = 0V unless otherwise specified

Symbol	Parameter		Min	Typ	Max	Units
f_C	Clock Frequency, V_{DD} = 3V				500	kHz
t_{CH}	Clock Period High	(Notes 1, 2)	500			ns
t_{CL}	Clock Period Low		500			ns
t_{DS}	Data Set-Up before Clock		300			ns
t_{DH}	Data Hold Time after Clock		100			ns
t_{LW}	Minimum Load Pulse Width		500			ns
t_{LTC}	Load to Clock		400			ns
t_{CDO}	Clock to Data Valid			400	750	ns

Note 1: AC input waveform specification for test purpose: $t_r \leq 20$ ns, $t_f \leq 20$ ns, f = 500 kHz, 50% ±10% duty cycle.

Note 2: Clock input rise and fall times must not exceed 300 ns.

Note 3: Output offset voltage is ±50 mV with $C_{SEGMENT}$ = 250 pF, C_{BP} = 8750 pF.

Functional Description

A block diagram for the MM5483 is shown in *Figure 1* and a package pinout is shown in *Figure 2*. *Figure 3* shows a possible 3-wire connection system with a typical signal format for *Figure 3*. Shown in *Figure 4*, the load input is an asynchronous input and lets data through from the shift register to the output buffers any time it is high. The load input can be connected to V_{DD} for 2-wire control as shown in *Figure 5*. In the 2-wire control mode, 31 bits (or less depending on the number of segments used) of data are clocked into the MM5483 in a short time frame (with less than 0.1 second there probably will be no noticeable flicker) with no more clocks until new information is to be displayed. If data was slowly clocked in, it can be seen to "walk" across the display in the 2-wire mode. An AC timing diagram can be seen in *Figure 6*. It should be noted that data out is not a TTL-compatible output.

Functional Description (Continued)

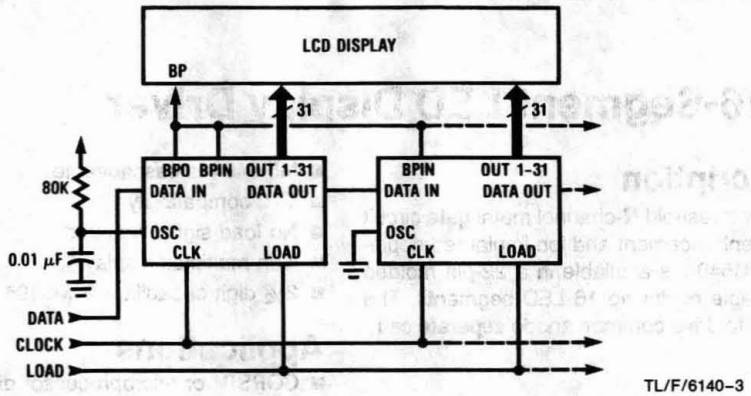


FIGURE 3. Three-Wire Control Mode

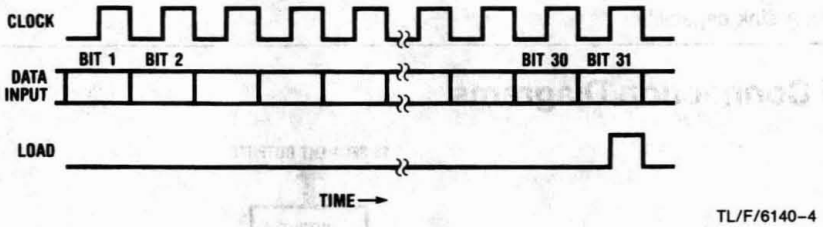


FIGURE 4. Data Format Diagram

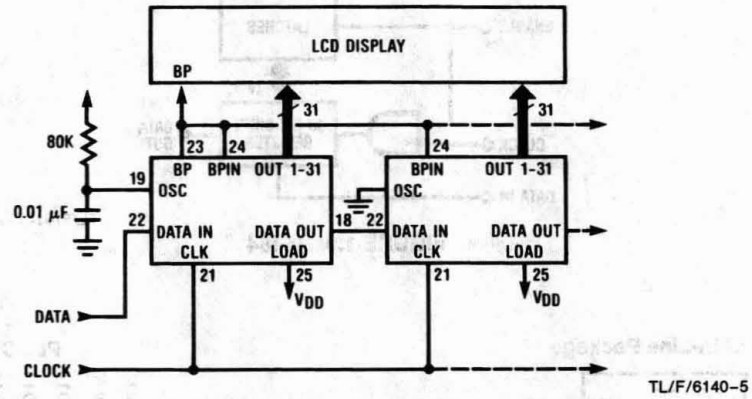


FIGURE 5. Two-Wire Control Mode

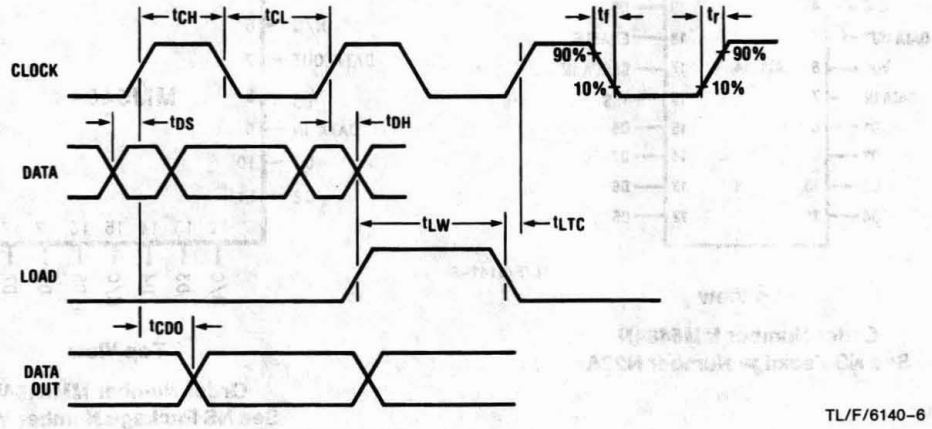


FIGURE 6. Timing Diagram

National Semiconductor

MM5484 16-Segment LED Display Driver

General Description

The MM5484 is a low threshold N-channel metal gate circuit using low threshold enhancement and ion implanted depletion devices. The MM5484 is available in a 22-pin molded package and is capable of driving 16 LED segments. The MM5484 is designed to drive common anode separate cathode LED displays.

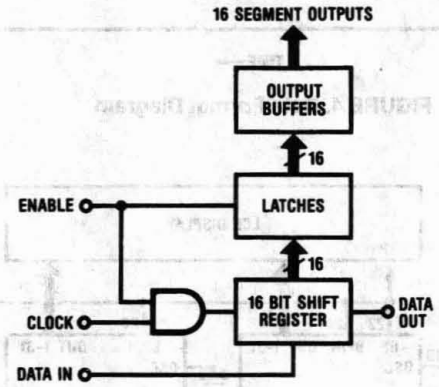
Features

- Serial data input
- Wide power supply operation
- 16 output, 15 mA sink capability
- MM5484 is cascadeable
- TTL compatibility
- No load signal required
- Non multiplex display
- 2½ digit capability—MM5484

Applications

- COPS™ or microprocessor displays
- Instrumentation readouts
- Industrial control indicator
- Relay driver

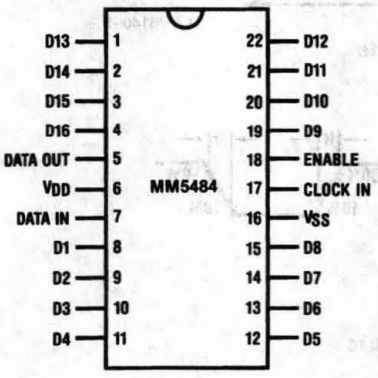
Block and Connection Diagrams



TL/F/6141–1

FIGURE 1. MM5484

Dual-In-Line Package

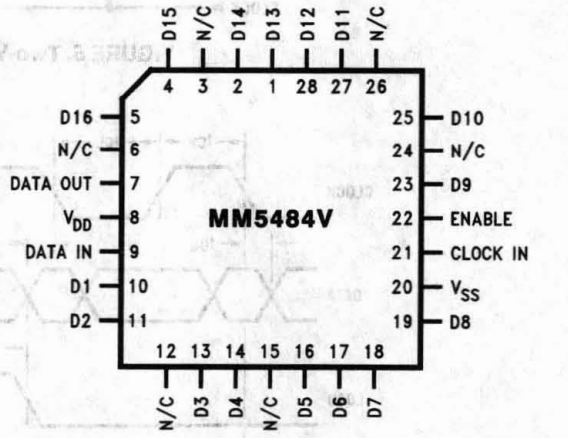


TL/F/6141–3

Top View

Order Number MM5484N
See NS Package Number N22A

PLCC



TL/F/6141–6

Top View

Order Number MM5484V
See NS Package Number V28A

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Voltage at LED Outputs	$V_{SS} - 0.5V$ to $V_{SS} + 12V$
Voltage at Other Pins	$V_{SS} - 0.5V$ to $V_{SS} + 10V$
Operating Temperature	−40°C to +85°C
Storage Temperature	−40°C to +150°C
Power Dissipation at 25°C	
Molded DIP Package, board mount	2W*
Molded DIP Package, socket mount	1.8W**

*Molded DIP Package, board mount, $\theta_{JA} = 63°C/W$, derate 15.8m W/°C above 25°C.

**Molded DIP Package, socket mount, $\theta_{JA} = 69°C/W$, derate 14.5m W/°C above 25°C.

Lead Temperature (Soldering, 10 sec.) 300°C

DC Electrical Characteristics

$V_{DD} = 4.5V$ to 9V, $T_A = -40°C$ to +85°C unless otherwise specified

Parameter	Conditions	Min	Typ	Max	Units
Supply Voltage		4.5		9	V
Supply Current			5	10	mA
Logic One					
Input High Level V_{IH}		2.4		$V_{DD} + 0.5$	V
Logic Zero					
Input Low Level V_{IL}		0		0.8	V
Input Current	High or Low Level			±1	μA
Input Capacitance				7.5	pF
OUTPUTS					
Data Output Voltage					
High Level V_{OH}	$I_{OUT} = 0.1$ mA	$V_{DD} - 0.5$			V
Low Level V_{OL}	$I_{OUT} = -0.1$ mA			0.5	V
Segment Off	$V_{OUT} = 12V$			50	μA
(Logic Zero on Input)	$R_{EXT} = 400\Omega$				
Output Current Segment On (Logic One on Input) Output Voltage	$I_{OUT} = 15$ mA, $V_{DD} \geq 6V$		0.5	1.0	V

AC Electrical Characteristics

(See *Figure 3.*) $V_{DD} = 4.5V$ to 9V, $T_A = -40°C$ to +85°C unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Units
f_C	Clock Frequency				0.5	MHz
t_h	High Time		0.95			μs
t_l	Low Time		0.95			μs
t_{S1}	Data Setup Time		0.5			μs
t_{H1}	Data Hold Time		0.5			μs
t_{S2}	Enable Setup Time		0.5			μs
t_{H2}	Enable Hold Time		0.5			μs
t_{pd}	Data Out Delay				0.5	μs

Note 1: Under no condition should the power dissipated by the segment driver exceed 50 mW nor the entire chip power dissipation exceed 500 mW.

Note 2: AC input waveform specification for test purpose: $t_r \leq 20$ ns, $t_f \leq 20$ ns, f = 500 kHz, 50% ±10% duty cycle.

Note 3: Clock input rise and fall times must not exceed 500 ns.

Functional Description

The MM5484 is designed to drive LED displays directly. Serial data transfer from the data source to the display driver is accomplished with 3 signals, DATA IN, CLOCK and ENABLE. The signal ENABLE acts as an envelope and only while this signal is at a logic '1' do the circuits recognize the clock signal.

While ENABLE is high, data on the serial data input is transferred and shifted in the internal shift register on the rising clock edge, i.e. a logic '0' to logic '1' transition.

When the ENABLE signal goes to a low (logic zero state), the contents of the shift register is latched and the display will show the new data. While new data is being loaded into the SR the display will continue to show the old data.

For the MM5484, data is output from the serial DATA OUT pin on the falling edge of clock so cascading is made simple with race hazards eliminated.

When the chip first powers on, an internal power on reset signal is generated which resets the SR and latches to zero so that the display will be off.

Timing Diagram

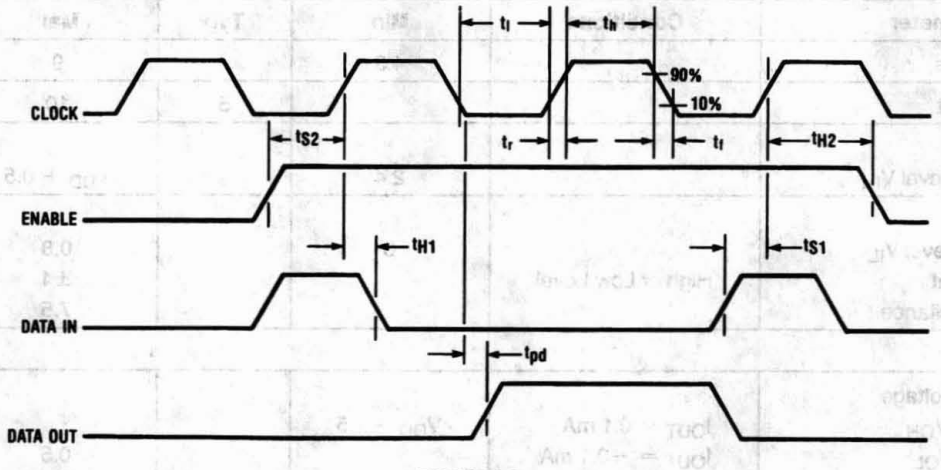


FIGURE 3

National Semiconductor

MM5486 LED Display Driver

General Description

The MM5486 is a monolithic MOS integrated circuit utilizing N-channel metal-gate low-threshold, enhancement mode and ion-implanted depletion mode devices. It is available in a 40-pin molded dual-in-line package. The MM5486 is designed to drive common anode-separate cathode LED displays. A single pin controls the LED display brightness by setting a reference current through a variable resistor connected to V_{DD}.

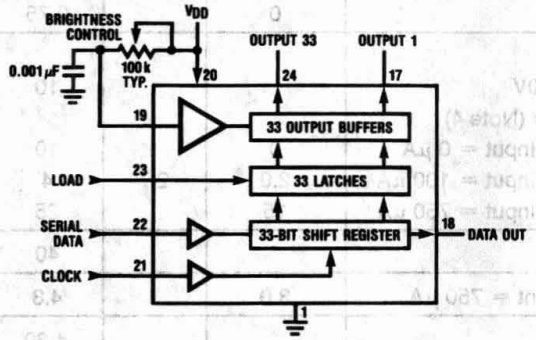
Features

- Continuous brightness control
- Serial data input/outut
- External load input
- Cascaded operation capability
- Wide power supply operation
- TTL compatibility
- 33 outputs, 15 mA sink capability
- Alphanumeric capability

Applications

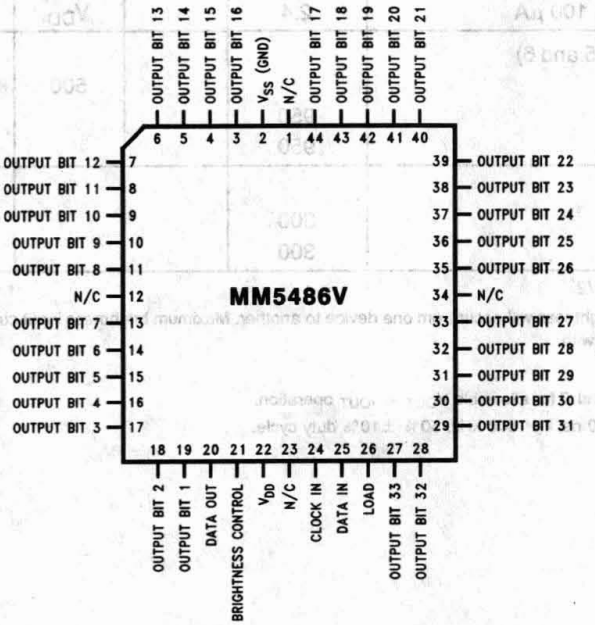
- COPS™ or microprocessor displays
- Industrial control indicator
- Relay driver
- Digital clock, thermometer, counter, voltmeter
- Instrumentation readouts

Block and Connection Diagrams



TL/F/6142–1

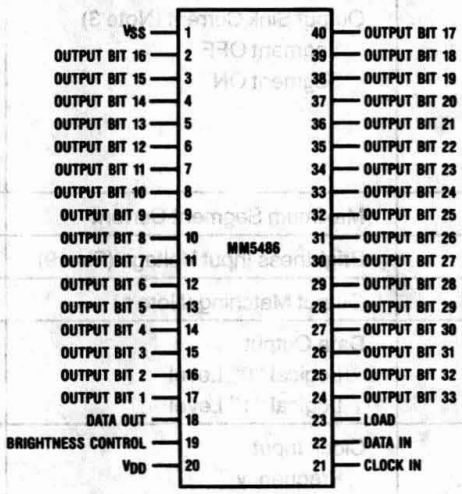
FIGURE 1



TL/F/6142–13

Order Number MM5486V
See NS Package Number V44A

Dual-In-Line Package



TL/F/6142–2

Top View

Order Number MM5486N
See NS Package Number N40A

FIGURE 2

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Voltage at Any Pin	V_{SS} to V_{SS} +12V
Operating Temperature	−25°C to +85°C
Storage Temperature	−65°C to +150°C

Power Dissipation at 25°C	
Molded DIP Package, Board Mount	2.5W*
Molded DIP Package, Socket Mount	2.3W**
Junction Temperature	+150°C
Lead Temperature (Soldering, 10 seconds)	300°C

*Molded DIP Package, Board Mount, θ_{JA} = 49°C/W, Derate 20.4 mW/°C above 25°C.

**Molded DIP Package, Socket Mount, θ_{JA} = 54°C/W, Derate 18.5 mW/°C above 25°C.

Electrical Characteristics

T_A within operating range, V_{DD} = 4.75V to 11.0V, V_{SS} = 0V, unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{DD}	Power Supply		4.75		11	V
I_{DD}	Power Supply Current	Excluding Output Loads			7	mA
	Input Voltages					
V_{IL}	Logic "0" Level	±10 μA Input Bias	−0.3		0.8	V
V_{IH}	Logic "1" Level	4.75 ≤ V_{DD} ≤ 5.25	2.2		V_{DD}	V
		V_{DD} > 5.25	V_{DD}−2		V_{DD}	V
I_{BR}	Brightness Input (Note 2)		0		0.75	mA
	Output Sink Current (Note 3)					
I_{OH}	Segment OFF	V_{OUT} = 3.0V			10	μA
I_{OL}	Segment ON	V_{OUT} = 1V (Note 4)				
		Brightness Input = 0 μA	0		10	μA
		Brightness Input = 100 μA	2.0	2.7	4	mA
		Brightness Input = 750 μA	15		25	mA
I_O	Maximum Segment Current				40	mA
V_{IBR}	Brightness Input Voltage (Pin 19)	Input Current = 750 μA	3.0		4.3	V
OM	Output Matching (Note 1)				±20	%
	Data Output					
V_{OL}	Logical "0" Level	I_{OUT} = 0.5 mA	V_{SS}		0.4	V
V_{OH}	Logical "1" Level	I_{OUT} = 100 μA	2.4		V_{DD}	V
	Clock Input	(Notes 5 and 6)				
f_C	Frequency				500	kHz
t_h	High Time		950			ns
t_l	Low Time		950			ns
	Data Input					
t_{DS}	Set-Up Time		300			ns
t_{DH}	Hold Time		300			ns

Note 1: Output matching is calculated as the percent variation $(I_{MAX} + I_{MIN})/2$.

Note 2: With a fixed resistor on the brightness input pin, some variation in brightness will occur from one device to another. Maximum brightness input current can be 2 mA as long as Note 3 and junction temperature equation are complied with.

Note 3: Absolute maximum for each output should be limited to 40 mA.

Note 4: The V_{OUT} voltage should be regulated by the user. See *Figures 6* and *7* for allowable V_{OUT} vs I_{OUT} operation.

Note 5: AC input waveform specification for test purpose: $t_r \leq 20$ ns, $t_f \leq 20$ ns, f = 500 kHz, 50% ±10% duty cycle.

Note 6: Clock input rise and fall times must not exceed 300 ns.

Functional Description

The MM5486 is specifically designed to operate four-digit alphanumeric displays with minimal interface with the display and the data source. Serial data transfer from the data source to the display driver is accomplished with 3 signals, serial data, clock, and load. The data bits are latched by a positive-level load signal, thus providing non-multiplexed, direct drive to the display. When load is high, the data in the shift registers is displayed on the output drivers. Outputs change only if the serial data bits differ from the previous time. Display brightness is determined by control of the output current for LED displays. A 0.001 μF capacitor should be connected to brightness control, pin 19, to prevent possible oscillations. The output current is typically 20 times greater than the current into pin 19, which is set by an external variable resistor. There is an internal limiting resistor of 400Ω nominal value.

A block diagram is shown in *Figure 1*.

Figure 4 shows the input data format. Bit "1" is the first bit into the data input pin and it will appear on pin 17. A logical "1" at the input will turn on the appropriate LED. The load signal latches the 33 bits of the shift register into the latches. The data out pin allows for cascading the shift registers for more than 33 output drivers.

When the chip first powers ON, an internal power ON reset signal is generated which resets all registers and latches. The leading clock returns the chip to its normal operation.

Figure 3 shows the timing relationship between data, clock and data enable. A maximum clock frequency of 0.5 MHz is assumed.

For applications where a lesser number of outputs are used, it is possible to either increase the current per output, or operate the part at higher than 1V V_{OUT}. The following equation can be used for calculations:

$$T_J = (V_{OUT})\,(I_{LED})\,(\text{No. of segments})\,(\theta_{JA}) + T_A$$

where:

T_J = junction temperature, 150°C max.

V_{OUT} = the voltage at the LED driver outputs

I_{LED} = the LED current

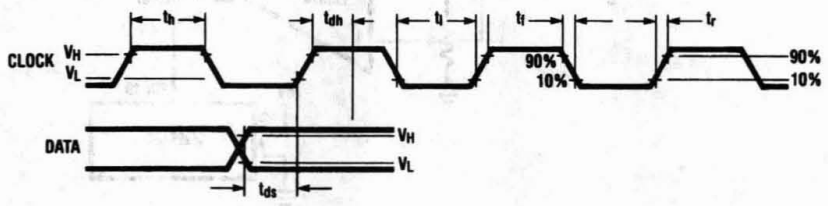
θ_{JA} = thermal coefficient of the package

T_A = ambient temperature

θ_{JA} (Socket Mount) = 54°C/W

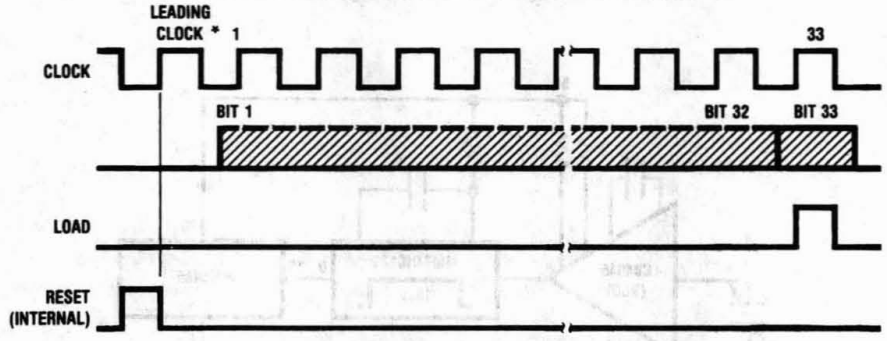
θ_{JA} (Board Mount) = 49°C/W

The above equation was used to plot *Figure 6, Figure 7,* and *Figure 8*.



TL/F/6142–3

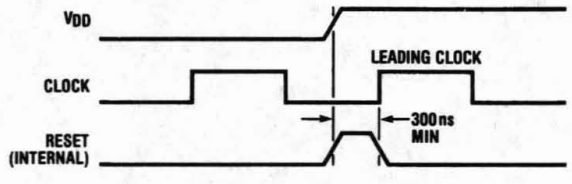
FIGURE 3



TL/F/6142–4

*This leading clock is necessary only after power ON.

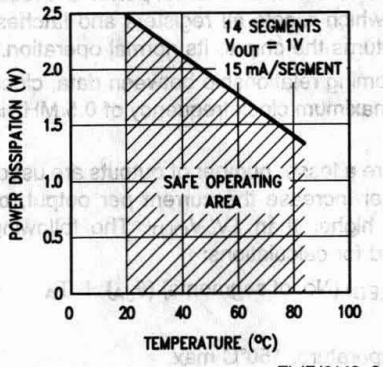
FIGURE 4. Input Data Format



TL/F/6142–5

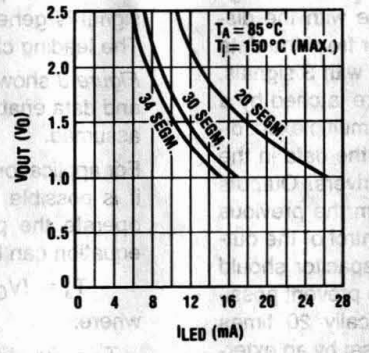
FIGURE 5

Typical Applications



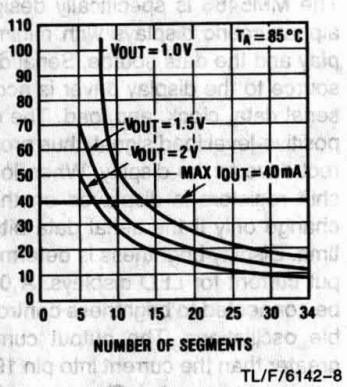
TL/F/6142–6

FIGURE 6



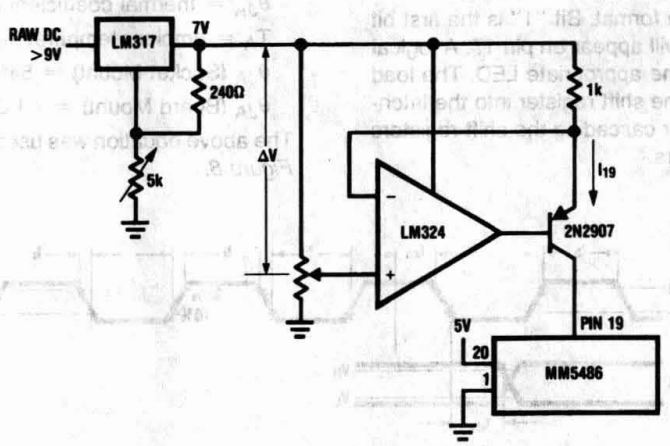
TL/F/6142–7

FIGURE 7



TL/F/6142–8

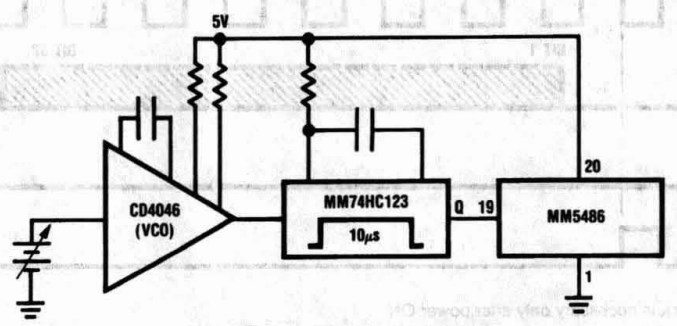
FIGURE 8



TL/F/6142–9

$$I_{19} = \frac{\Delta V}{1k}$$

FIGURE 9. Constant Current Brightness Control

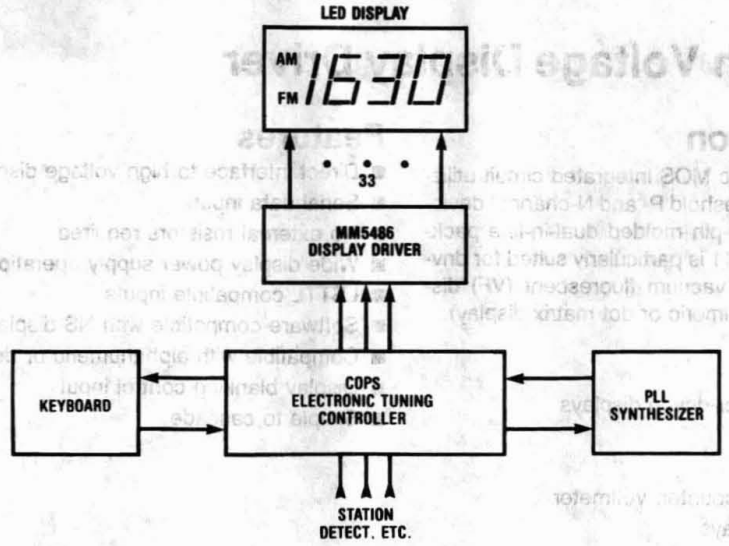


TL/F/6142–10

FIGURE 10. Brightness Control Varying the Duty Cycle

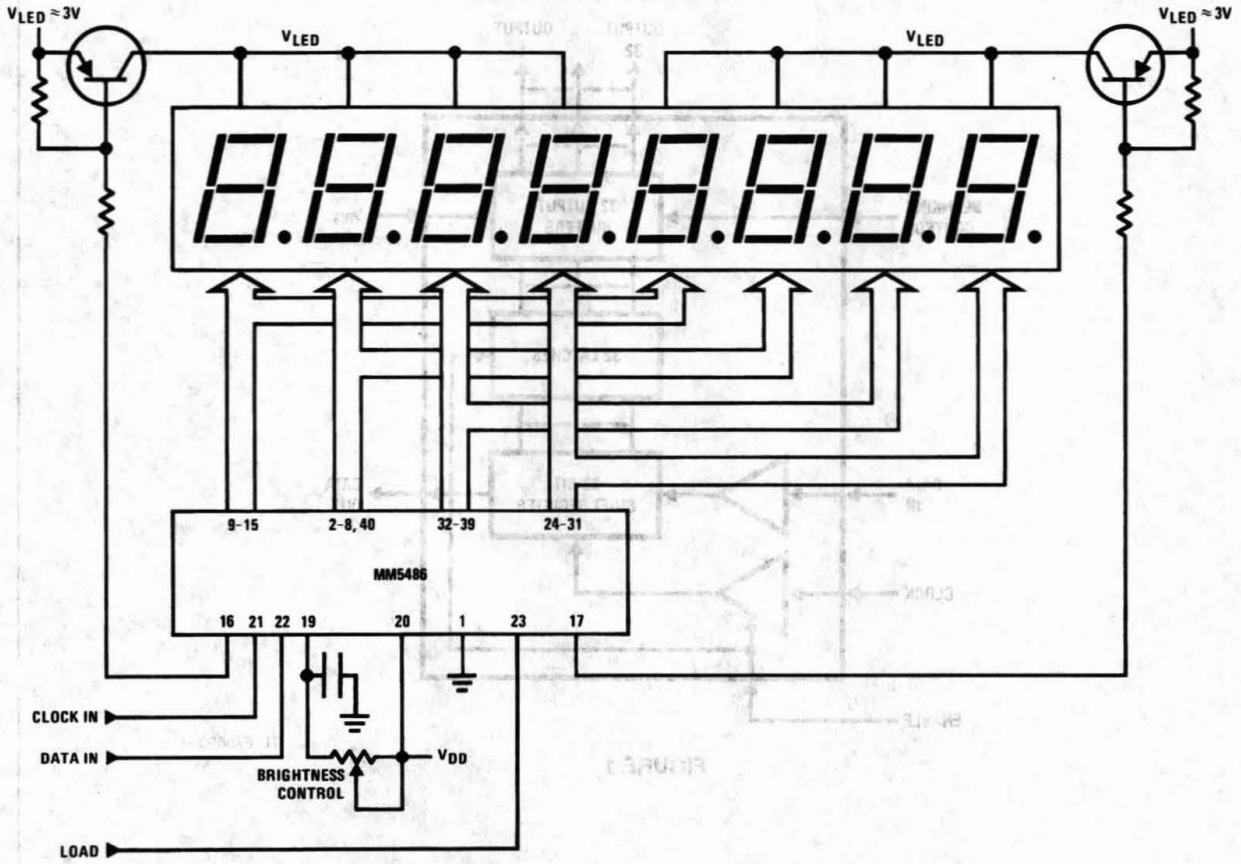
Typical Applications (Continued)

Basic Electronically Tuned Radio System



TL/F/6142–11

Duplexing 8 Digits with One MM5486



TL/F/6142–12

*This driver has 7 segments only.

National Semiconductor

MM58241 High Voltage Display Driver

General Description

The MM58241 is a monolithic MOS integrated circuit utilizing CMOS metal gate low threshold P- and N-channel devices. It is available both in 40-pin molded dual-in-line packages or as dice. The MM58241 is particularly suited for driving high voltage (60V max) vacuum fluorescent (VF) displays (e.g., a 32-digit alphanumeric or dot matrix display).

Applications

- COPS™ or microprocessor-driven displays
- Instrumentation readouts
- Industrial control indicator
- Digital clock, thermostat, counter, voltmeter
- Word processor text displays
- Automotive dashboards

Features

- Direct interface to high voltage display
- Serial data input
- No external resistors required
- Wide display power supply operation
- LSTTL compatible inputs
- Software compatible with NS display driver family
- Compatible with alphanumeric or dot matrix displays
- Display blanking control input
- Simple to cascade

Block Diagram

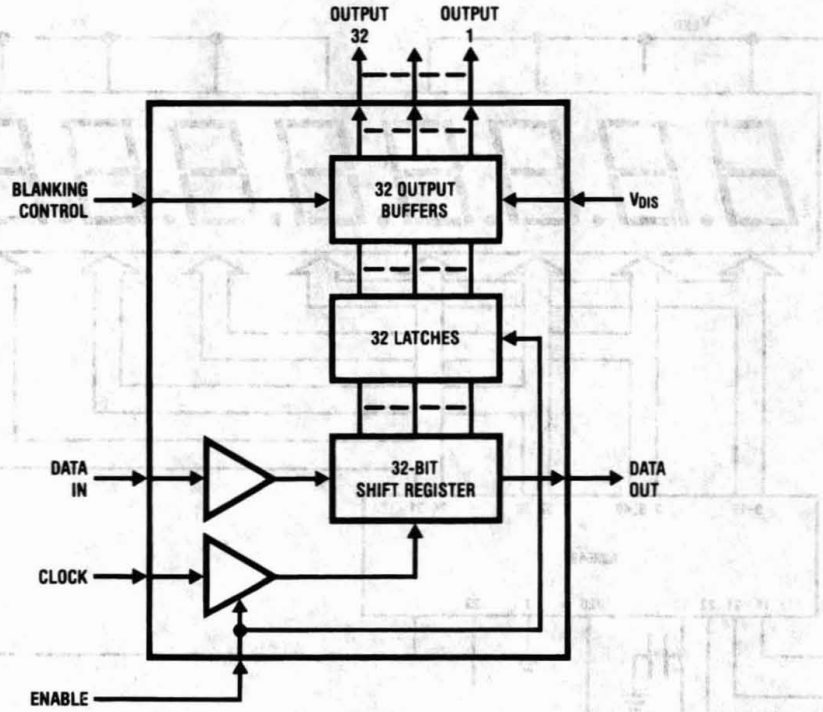


FIGURE 1

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Voltage at Any Input Pin	$V_{DD} + 0.3V$ to $V_{SS} - 0.3V$
Voltage at Any Display Pin	V_{DD} to $V_{DD} - 62.5V$
$V_{DD} + \lvert V_{DIS} \rvert$	62.5V
Storage Temperature	−65°C to +150°C
Power Dissipation at +25°C	
Molded DIP Package, Board Mount	2.28W*
Molded DIP Package, Socket Mount	2.05W**
Junction Temperature	130°C
Lead Temperature (Soldering, 10 sec.)	260°C

*Molded DIP Package, Board Mount, θ_{JA} = 46°C/W, Derate 21.7 mW/°C above +25°C.

**Molded DIP Package, Socket Mount, θ_{JA} = 51°C/W, Derate 19.6 mW/°C above +25°C.

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{DD}) V_{SS} = 0V	4.5	5.5	V
Display Voltage (V_{DIS})	−55	−25	V
Temperature Range	−40	+85	°C

DC Electrical Characteristics

T_A = −40°C to +85°C, V_{DD} = 5V ±0.5V, V_{SS} = 0V unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Units
I_{DD}	Power Supply Currents	$V_{IN} = V_{SS}$ or V_{DD}, V_{SS} = 0V, V_{DIS} Disconnected			150	µA
I_{DIS}		V_{DD} = 5.5V, V_{SS} = 0V, V_{DIS} = −55V All Outputs Low			10	mA
	Input Logic Levels DATA IN, CLOCK ENABLE, BLANK					
V_{IL}	Logic '0'				0.8	V
V_{IH}	Logic '1'	(Note 1)	2.4			V
	Data Output Logic Levels					
V_{OL}	Logic '0'	I_{OUT} = 400 µA			0.4	V
V_{OH}	Logic '1'	I_{OUT} = −10 µA	$V_{DD} - 0.5$			V
V_{OH}	Logic '1'	I_{OUT} = −500 µA	2.8			V
I_{IN}	Input Currents DATA IN, CLOCK ENABLE, BLANK	V_{IN} = 0V or V_{DD}	−10		10	µA
C_{IN}	Input Capacitance DATA IN, CLOCK ENABLE, BLANK				15	pF
	Display Output Impedances	V_{DD} = 5.5V, V_{SS} = 0V				
R_{OFF}	Output Off *(Figure 3a)*	V_{DIS} = −25V	60		400	kΩ
		V_{DIS} = −40V	70		550	kΩ
		V_{DIS} = −55V	80		650	kΩ
R_{ON}	Output On *(Figure 3b)*	V_{DIS} = −25V		3.0	4.0	kΩ
		V_{DIS} = −40V		2.6	3.7	kΩ
		V_{DIS} = −55V		2.3	3.4	kΩ
V_{DOL}	Display Output Low Voltage	V_{DD} = 5.5V, I_{OUT} = Open Circuit, −55V ≤ V_{DIS} ≤ −25V	V_{DIS}		$V_{DIS} + 4$	V

Note 1: 74LSTTL V_{OH} = 2.7V @ I_{OUT} = −400 µA, TTL V_{OH} = 2.4V @ I_{OUT} = −400 µA.

AC Electrical Characteristics $T_A = -40°C$ to $+85°C$, $V_{DD} = 5V \pm 0.5V$

Symbol	Parameter	Conditions	Min	Typ	Max	Units
	Clock Input	(Notes 3 and 4)				
f_C	Frequency				800	kHz
t_H	High Time		300			ns
t_L	Low Time		300			ns
	Data Input					
t_{DS}	Set-Up Time		100			ns
t_{DH}	Hold Time		100			ns
	Enable Input					
t_{ES}	Set-Up Time		100			ns
t_{EH}	Hold Time		100			ns
	Data Output	$C_L = 50$ pF				
t_{CDO}	CLOCK Low to Data Out Time				500	ns

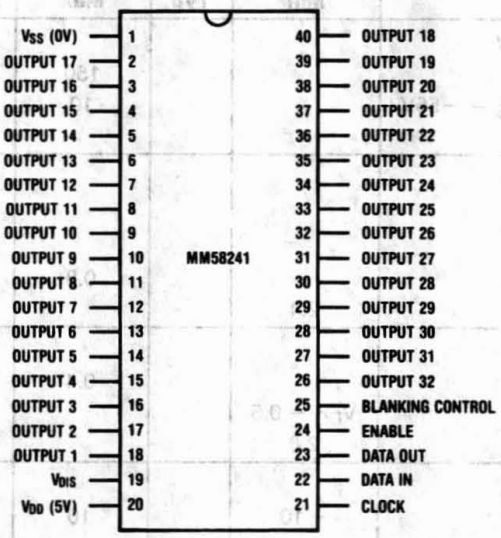
Note 2: For timing purposes, the signals ENABLE and BLANK can be considered to be totally independent of each other.

Note 3: AC input waveform specification for test purposes: t_r, $t_f \leq 20$ ns, f = 800 kHz, 50% ±10% duty cycle.

Note 4: Clock input rise and fall times must not exceed 5 μs.

Connection Diagrams

Dual-In-Line Package



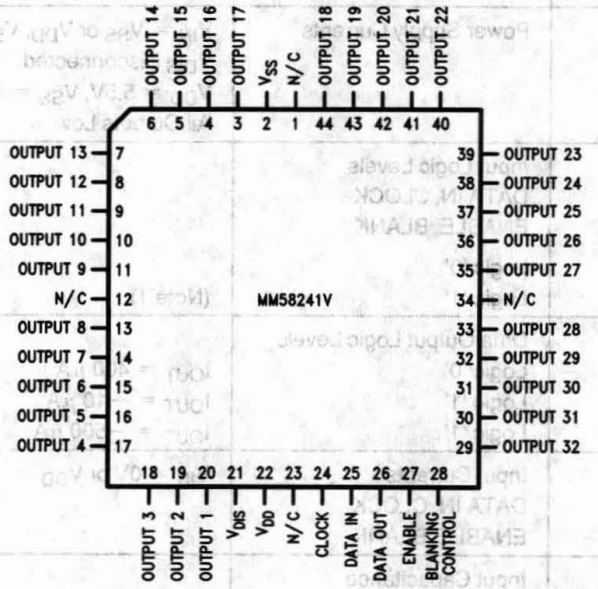
TL/F/5600–2

Top View

FIGURE 2

Order Number MM58241N or MM58241V
See NS Package Number N40A or V44A

Plastic Chip Carrier



TL/F/5600–8

Top View

Functional Description

This product is specifically designed to drive multiplexed or non-multiplexed high voltage alphanumeric or dot matrix vacuum fluorescent (VF) displays. Character generation is done externally in the microprocessor, with a serial data path to the display driver. The MM58421 uses three signals, DATA IN, CLOCK and ENABLE, where ENABLE acts as an external load signal. Display blanking can be achieved by means of the BLANKING CONTROL input, and a logic '1' will turn off all sections of the display. A block diagram of the MM58241 is shown in *Figure 1.*

Figure 2 shows the pinout of the MM58241 device, where output 1 (pin 18) is equivalent to bit 1, i.e., the first bit of data to be loaded into the shift register following ENABLE high. A logic '1' at the input will turn on the corresponding display digit/segment/dot output.

A significant reduction in discrete board components can be achieved by use of the MM58241, because external pull-down resistors are not required. Due to the nature of the output stage, both its on and off impedance values vary as a function of the display voltage applied. However, *Figures 3a* and *3b* show that this output impedance will remain constant for a fixed value of display voltage.

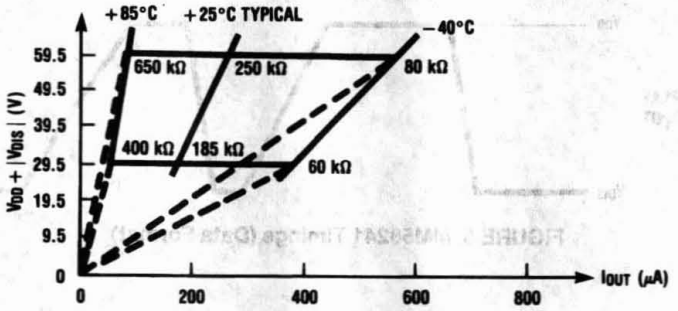
Functional Description (Continued)

Figure 4 demonstrates the critical timing requirements between CLOCK and DATA IN for the MM58241.

To clear (reset) the display driver at power on or any time, the following flushing routine may be used. With the enable signal high, clock in 32 zeroes. Drive the enable signal low and the display will be blank. It is recommended to clear the driver at power on.

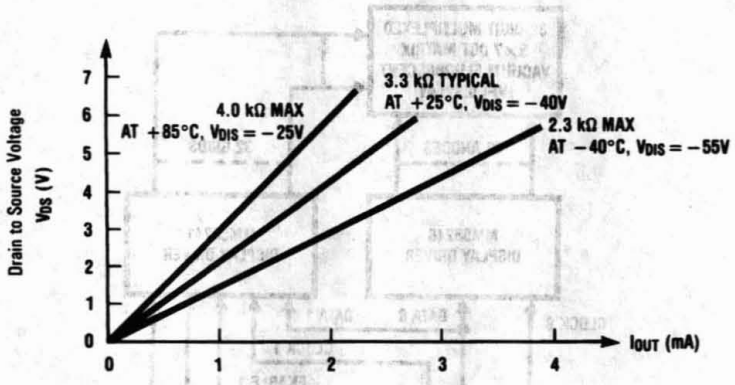
In *Figure 5,* the ENABLE signal acts as an envelope, and only while this signal is at a logic '1' does the circuit accept CLOCK input signals. Data is transferred and shifted in the internal shift register on the rising clock edge, i.e., '0'–'1' transition. When the ENABLE signal goes low, the contents of the shift registers are latched, and the display will show new data. During data transfer, the display will show old data. DATA OUT is also provided on the MM58241, being output on the falling edge. At any time, the display may be blanked under processor control, using the BLANKING CONTROL input.

Figure 6 shows a schematic diagram of a microprocessor-based system where the MM58241 is used to provide the grid drive for a 32-digit 5 x 7 dot matrix vaccum fluorescent (VF) display. The anode drive in this example is provided by another member of the high voltage display driver family, namely the MM58248, which does not require an externally generated load signal.



TL/F/5600–3

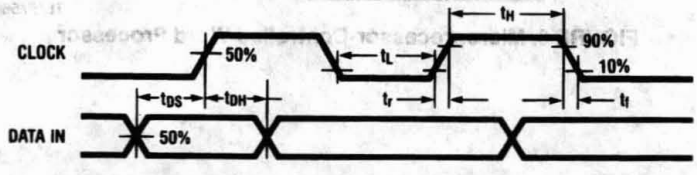
FIGURE 3a. Output Impedance Off



TL/F/5600–4

FIGURE 3b. Output Impedance On

Timing Diagrams

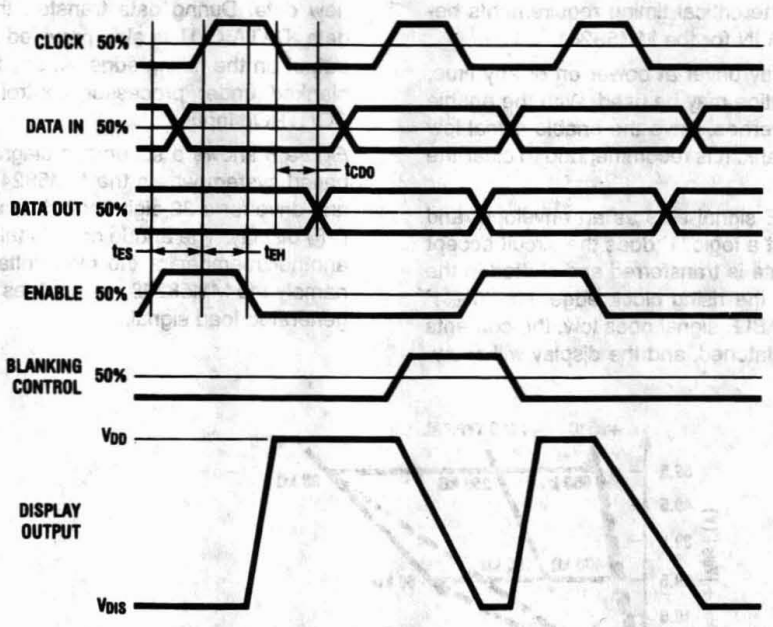


TL/F/5600–5

For the purposes of AC measurements, V_{IH} = 2.4V, V_{IL} = 0.8V.

FIGURE 4. Clock and Data Timings

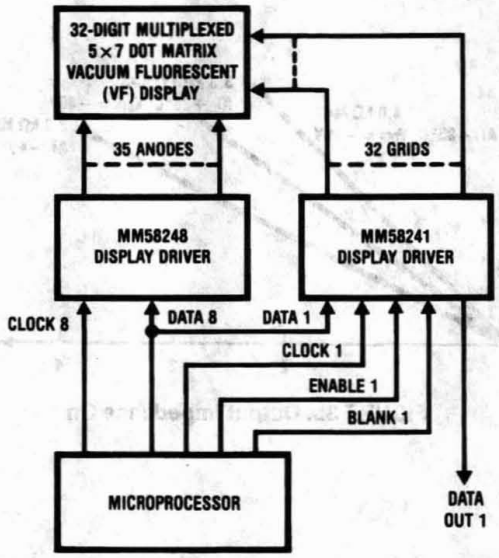
Timing Diagrams (Continued)



TL/F/5600–6

FIGURE 5. MM58241 Timings (Data Format)

Typical Application



TL/F/5600–7

FIGURE 6. Microprocessor-Controlled Word Processor

National Semiconductor

MM58341 High Voltage Display Driver

General Description

The MM58341 is a monolithic MOS integrated circuit utilizing CMOS metal gate low threshold P and N-channel devices. It is available both in 40-pin molded dual-in-line packages or as dice. The MM58341 is particularly suited for driving high voltage (35V max) vacuum fluorescent (VF) displays, (e.g., a 32-digit alphanumeric or dot matrix display).

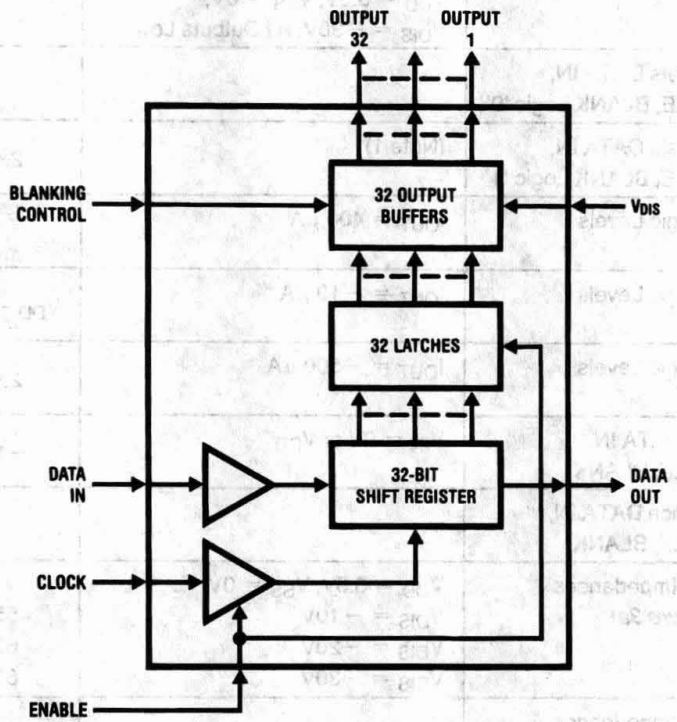
Applications

- COPS™ or microprocessor-driven displays
- Instrumentation readouts
- Industrial control indicator
- Digital clock, thermostat, counter, voltmeter
- Word processor text displays
- Automotive dashboards

Features

- Direct interface to high voltage display
- Serial data input
- No external resistors required
- Wide display power supply operation
- LSTTL compatible inputs
- Software compatible with NS display driver family
- Compatible with alphanumeric or dot matrix displays
- Display blanking control input
- Simple to cascade

Block Diagram



TL/F/5603–1

FIGURE 1

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Voltage at Any Input Pin	$V_{DD} + 0.3V$ to $V_{SS} - 0.3V$
Voltage at Any Display Pin	V_{DD} to $V_{DD} - 36.5V$
$V_{DD} + \lvert V_{DIS} \rvert$	36.5V
Storage Temperature	−65°C to +150°C
Power Dissipation at 25°C	
Molded DIP Package, Board Mount	2.28W*
Molded DIP Package, Socket Mount	2.05W**
*Molded DIP Package, Board Mount, Derate 21.7 mW°C Above 25°C	$\theta_{JA} = 46°C/W$
**Molded DIP Package, Socket Mount, Derate 19.6 mW/°C Above 25°C	$\theta_{JA} = 51°C/W$
Junction Temperature	130°C
Lead Temperature (Soldering, 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{DD}) $V_{SS} = 0V$	4.5	5.5	V
Display Voltage (V_{DIS})	−30	−10	V
Temperature Range	−40	+85	°C

DC Electrical Characteristics

$T_A = -40°C$ to $+85°C$, $V_{DD} = 5V \pm 0.5V$, $V_{SS} = 0V$ unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Units
I_{DD}	Power Supply Currents	$V_{IN} = V_{SS}$ or V_{DD}, $V_{SS} = 0V$, V_{DIS} Disconnected			150	μA
I_{DIS}		$V_{DD} = 5.5V$, $V_{SS} = 0V$, $V_{DIS} = -30V$, All Outputs Low			10	mA
V_{IL}	Input Logic Levels DATA IN, CLOCK ENABLE, BLANK Logic '0'				0.8	V
V_{IH}	Input Logic Levels DATA IN, CLOCK ENABLE, BLANK Logic '1'	(Note 1)	2.4			V
V_{OH}	Data Output Logic Levels Logic '0'	$I_{OUT} = 400\ \mu A$			0.4	V
V_{OH}	Data Output Logic Levels Logic '1'	$I_{OUT} = -10\ \mu A$	$V_{DD} - 0.5$			V
V_{OH}	Data Output Logic Levels Logic '1'	$I_{OUT} = -500\ \mu A$	2.8			V
I_{IN}	Input Currents DATA IN, CLOCK ENABLE, BLANK	$V_{IN} = 0V$ or V_{DD}	−10		10	μA
C_{IN}	Input Capacitance DATA IN, CLOCK ENABLE, BLANK				15	pF
R_{OFF}	Display Output Impedances Output Off *(Figure 3a)*	$V_{DD} = 5.5V$, $V_{SS} = 0V$				
		$V_{DIS} = -10V$	55		250	kΩ
		$V_{DIS} = -20V$	60		300	kΩ
		$V_{DIS} = -30V$	65		400	kΩ
R_{ON}	Display Output Impedances Output On *(Figure 3b)*					
		$V_{DIS} = -10V$		700	800	Ω
		$V_{DIS} = -20V$		600	750	Ω
		$V_{DIS} = -30V$		500	680	Ω
V_{DOL}	Display Output Low Voltage	$V_{DD} = 5.5V$, I_{OUT} = Open Circuit, $-30V \le V_{DIS} \le -10V$	V_{DIS}		$V_{DIS} + 2$	V

Note 1: 74LSTTL $V_{OH} = 2.7V$ @ $I_{OUT} = -400\ \mu A$, TTL $V_{OH} = 2.4V$ @ $I_{OUT} = -400\ \mu A$.

AC Electrical Characteristics $T_A = -40°C$ to $+85°C$, $V_{DD} = 5V \pm 0.5V$

Symbol	Parameter	Conditions	Min	Typ	Max	Units
f_C	Clock Input Frequency	(Notes 3, 4)			800	kHz
t_H	Clock Input High Time		300			ns
t_L	Clock Input Low Time		300			ns
t_{DS}	Data Input Setup Time		100			ns
t_{DH}	Data Input Hold Time		100			ns
t_{ES}	Enable Input Setup Time		100			ns
t_{EH}	Enable Input Hold Time		100			ns
t_{CDO}	Data Output Clock Low to Data Out Time	$C_L = 50$ pF			500	ns

Note 2: Note that, for timing purposes, the signals ENABLE and BLANK can be considered to be totally independent of each other.

Note 3: AC input waveform specification for test purpose: $t_r \leq 20$ ns, $t_f \leq 20$ ns, f = 800 kHz, 50% ±10% duty cycle.

Note 4: Clock input rise and fall times must not exceed 5 μs.

Connection Diagrams

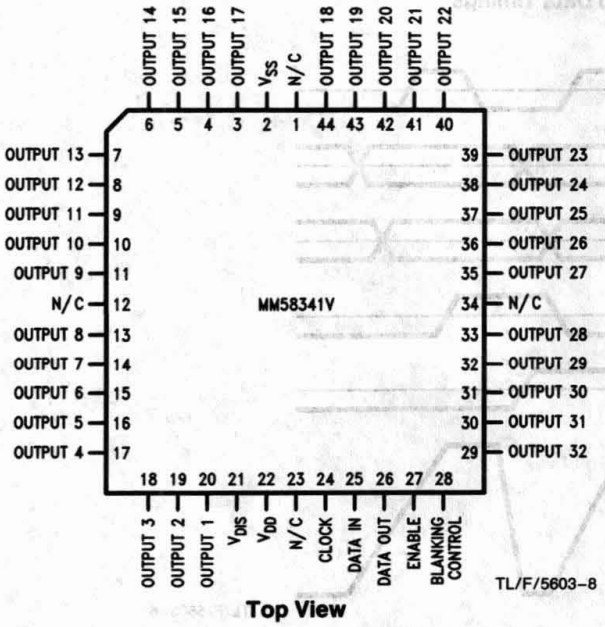
Dual-In-Line Package

TL/F/5603–2

Top View

Order Number MM58341N
See NS Package Number N40A

Plastic Chip Carrier



TL/F/5603–8

Top View

Order Number MM58341V
See NS Package Number V44A

Functional Description

This product is specifically designed to drive multiplexed or non-multiplexed high voltage alphanumeric or dot matrix vacuum fluorescent (VF) displays. Character generation is done externally in the microprocessor, with a serial data path to the display driver. The MM58341 uses three signals, DATA IN, CLOCK and ENABLE, where ENABLE acts as an external load signal. Display blanking can be achieved by means of the BLANKING CONTROL input, and a logic '1' will turn off all sections of the display. A block diagram of the MM58341 is shown in *Figure 1.*

Figure 2 shows the pinout of the MM58341 device, where output 1 (pin 18) is equivalent to bit 1 (i.e., the first bit of data to be loaded into the shift register following ENABLE high). A logic '1' at the input will turn on the corresponding display digit/segment/dot output.

A significant reduction in discrete board components can be achieved by use of the MM58341, because external pull-down resistors are not required. Due to the nature of the output stage, both its on and off impedance values vary as a function of the display voltage applied. However, *Figures 3a* and *3b* show that this output impedance will remain constant for a fixed value of display voltage.

Figure 4 demonstrates the critical timing requirements between CLOCK and DATA IN for the MM58341.

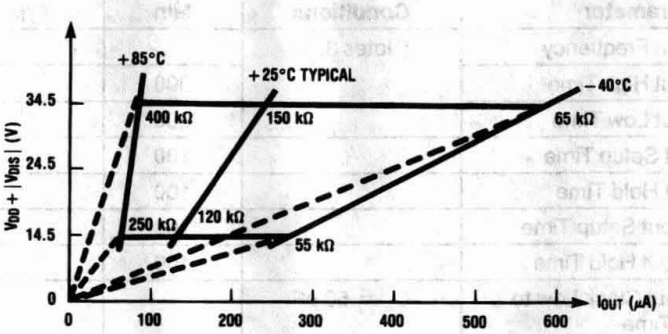
To clear (reset) the display driver at power on or any time, the following flushing routine may be used. With the enable signal high, clock in 32 zeroes. Drive the enable signal low and the display will be blank. It is recommended to clear the driver at power on.

In *Figure 5,* the ENABLE signal acts as an envelope, and only while this signal is at a logic '1' does the circuit accept CLOCK input signals. Data is transferred and shifted in the internal shift register on the rising clock edge, i.e., '0'–'1' transition. When the ENABLE signal goes low, the contents of the shift registers are latched, and the display will show new data. During data transfer, the display will show old data. DATA OUT is also provided on the MM58341, being output on the falling edge. At any time, the display may be blanked under processor control, using the BLANKING CONTROL input.

Figure 6 shows a schematic diagram of a microprocessor-based system where the MM58341 is used to provide the grid drive for a 32-digit 5 x 7 dot matrix vacuum fluorescent (VF) display. The anode drive in this example is provided by another member of the high voltage display driver family, namely the MM58348, which does not require an externally generated load signal.

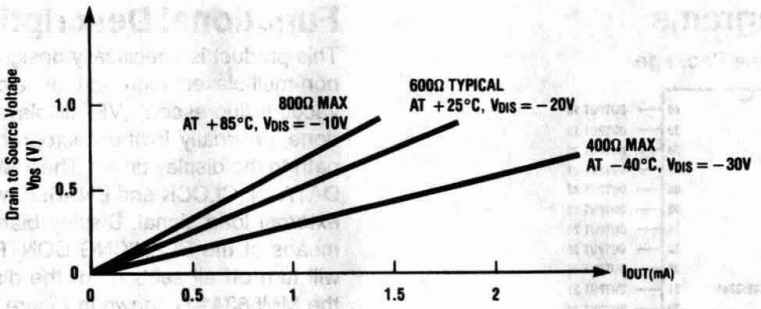
4

Functional Decription (Continued)



TL/F/5603–3

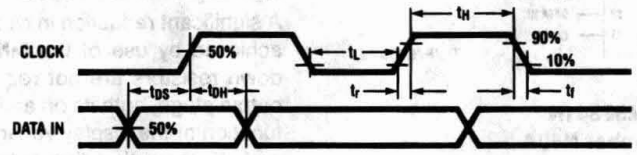
FIGURE 3a. Output Impedance Off



TL/F/5603–4

FIGURE 3b. Output Impedance On

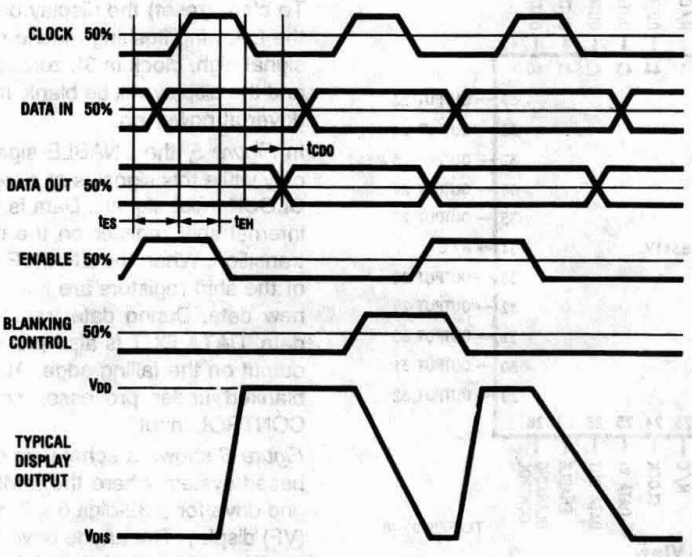
Timing Diagrams



TL/F/5603–5

For the purposes of AC measurements, V_{IH} = 2.4V, V_{IL} = 0.8V.

FIGURE 4. Clock and Data Timings



TL/F/5603–6

FIGURE 5. MM58341 Timings (Data Format)

Typical Application

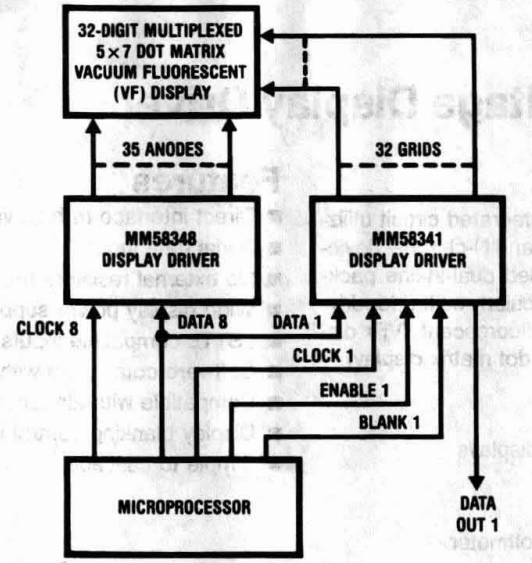


FIGURE 6. Microprocessor-Controlled Word Processor

National Semiconductor

MM58342 High Voltage Display Driver

General Description

The MM58342 is a monolithic MOS integrated circuit utilizing CMOS metal gate low threshold P- and N-channel devices. It is available both in 28-pin molded dual-in-line packages or as dice. The MM58342 is particularly suited for driving high voltage (35V max) vacuum fluorescent (VF) displays (e.g., a 20-digit alphanumeric or dot matrix display).

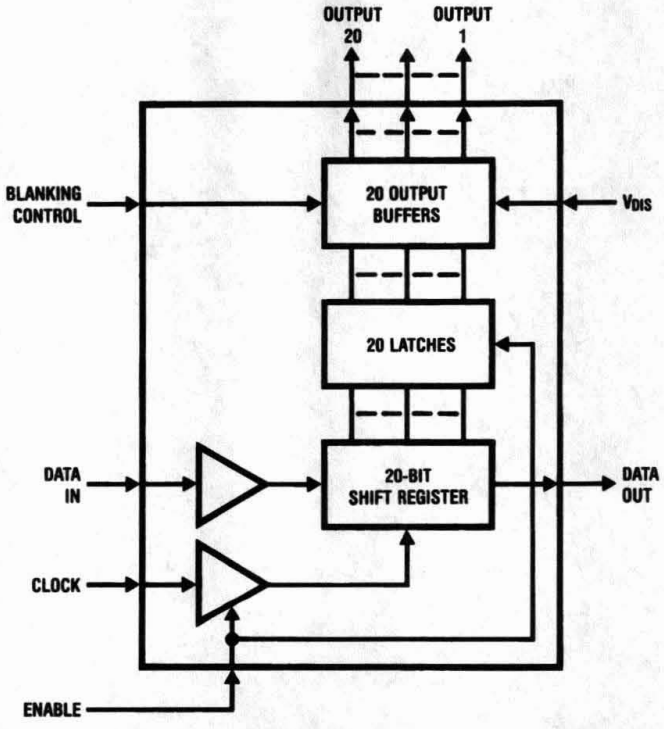
Applications

- COPS™ or microprocessor-driven displays
- Instrumentation readouts
- Industrial control indicator
- Digital clock, thermostat, counter, voltmeter
- Word processor text displays
- Automotive dashboards

Features

- Direct interface to high voltage display
- Serial data input
- No external resistors required
- Wide display power supply operation
- LSTTL compatible inputs
- Software compatible with NS display driver family
- Compatible with alphanumeric or dot matrix displays
- Display blanking control input
- Simple to cascade

Block Diagram



TL/F/7925–1

FIGURE 1

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Voltage at Any Input Pin	$V_{DD} + 0.3V$ to $V_{SS} - 0.3V$
Voltage at Any Display Pin	V_{DD} to $V_{DD} - 36.5V$
$V_{DD} + \lvert V_{DIS} \rvert$	36.5V
Storage Temperature	−65°C to +150°C
Power Dissipation at 25°C	
Molded DIP Package, Board Mount	2.03W*
Molded DIP Package, Socket Mount	1.83W**
Junction Temperature	130°C
Lead Temperature (Soldering, 10 sec.)	260°C

*Molded DIP Package, Board Mount, $\theta_{JA} = 52°C/W$, derate 19.2 mW/°C above 25°C.

**Molded DIP Package, Socket Mount, $\theta_{JA} = 58°C/W$, derate 17.2 mW/°C above 25°C.

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{DD}) $V_{SS} = 0V$	4.5	5.5	V
Display Voltage (V_{DIS})	−30	−10	V
Temperature Range	−40	+85	°C

DC Electrical Characteristics

$T_A = -40°C$ to $+85°C$, $V_{DD} = 5V \pm 0.5V$, $V_{SS} = 0V$ unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Units
	Power Supply Currents					
I_{DD}		$V_{IN} = V_{SS}$ or V_{DD}, $V_{SS} = 0V$, V_{DIS} Disconnected			150	μA
I_{DIS}		$V_{DD} = 5.5V$, $V_{SS} = 0V$, $V_{DIS} = -30V$ All Outputs Low			10	mA
	Input Logic Levels DATA IN, CLOCK ENABLE, BLANK					
V_{IL}	Logic '0'				0.8	V
V_{IH}	Logic '1'	(Note 1)	2.4			V
	Data Output Logic Levels					
V_{OL}	Logic '0'	$I_{OUT} = 400\ \mu A$			0.4	V
V_{OH}	Logic '1'	$I_{OUT} = -10\ \mu A$	$V_{DD} - 0.5$			V
V_{OH}	Logic '1'	$I_{OUT} = -500\ \mu A$	2.8			V
I_{IN}	Input Currents DATA IN, CLOCK ENABLE, BLANK	$V_{IN} = 0V$ or V_{DD}	−10		10	μA
C_{IN}	Input Capacitance DATA IN, CLOCK ENABLE, BLANK				15	pF
	Display Output Impedances	$V_{DD} = 5.5V$, $V_{SS} = 0V$				
R_{OFF}	Output Off *(Figure 3a)*	$V_{DIS} = -10V$	55		250	kΩ
		$V_{DIS} = -20V$	60		300	kΩ
		$V_{DIS} = -30V$	65		400	kΩ
R_{ON}	Output On *(Figure 3b)*	$V_{DIS} = -10V$		700	800	Ω
		$V_{DIS} = -20V$		600	750	Ω
		$V_{DIS} = -30V$		500	680	Ω
V_{DOL}	Display Output Low Voltage	$V_{DD} = 5.5V$, I_{OUT} = Open Circuit, $-30V \le V_{DIS} \le -10V$	V_{DIS}		$V_{DIS} + 2$	V

Note 1: 74LSTTL $V_{OH} = 2.7V$ @ $I_{OUT} = -400\ \mu A$, TTL $V_{OH} = 2.4V$ @ $I_{OUT} = -400\ \mu A$.

4

AC Electrical Characteristics $T_A = -40°C$ to $+85°C$, $V_{DD} = 5V \pm 0.5V$

Symbol	Parameter	Conditions	Min	Typ	Max	Units
	Clock Input	(Notes 3 and 4)				
f_C	Frequency				800	kHz
t_H	High Time		300			ns
t_L	Low Time		300			ns
	Data Input					
t_{DS}	Set-Up Time		100			ns
t_{DH}	Hold Time		100			ns
	Enable Input	(Note 2)				
t_{ES}	Set-Up Time		100			ns
t_{EH}	Hold Time		100			ns
	Data Output	$C_L = 50$ pF				
	CLOCK Low to Data Out				500	ns
t_{CDO}	Time					

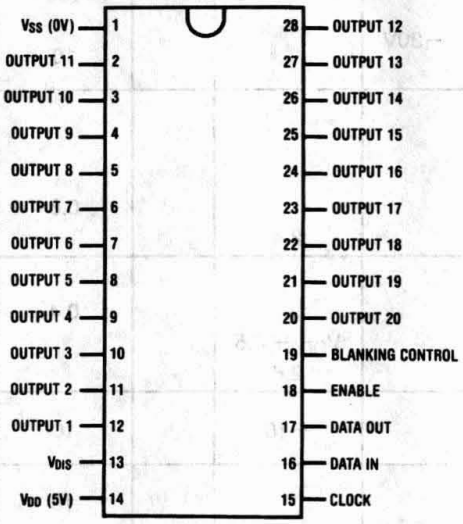
Note 2: For timing purposes, the signals ENABLE and BLANK can be considered to be totally independent of each other.

Note 3: AC input waveform specification for test purposes: t_r, $t_f \leq 20$ ns, $f = 800$ kHz, 50% $\pm 10\%$ duty cycle.

Note 4: Clock input rise and fall times must not exceed 5 μs.

Connection Diagrams

Dual-In-Line Package



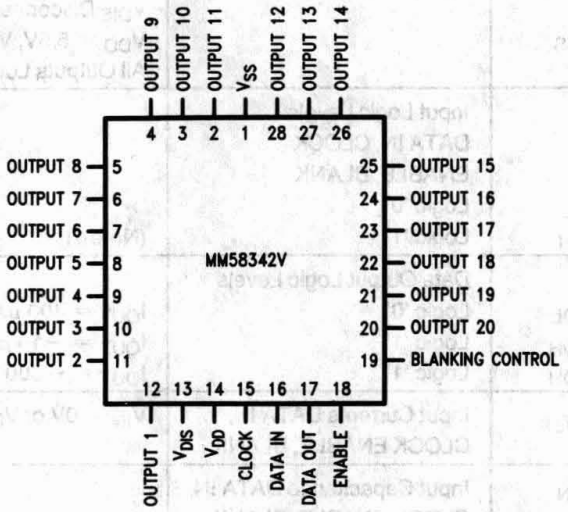
TL/F/7925–2

Top View

FIGURE 2

Order Number MM58342N
See NS Package Number N28B

Plastic Chip Carrier



TL/F/7925–8

Top View
Order Number MM58342V
See NS Package Number V28A

Functional Description

This product is specifically designed to drive multiplexed or non-multiplexed high voltage alphanumeric or dot matrix vacuum fluorescent (VF) displays. Character generation is done externally in the microprocessor, with a serial data path to the display driver. The MM58342 uses three signals, DATA IN, CLOCK and ENABLE, where ENABLE acts as an external load signal. Display blanking can be achieved by means of the BLANKING CONTROL input, and a logic '1' will turn off all sections of the display. A block diagram of the MM58342 is shown in *Figure 1*.

Figure 2 shows the pinout of the MM58342 device, where output 1 (pin 12) is equivalent to bit 1 (i.e., the first bit of data to be loaded into the shift register following ENABLE high). A logic '1' at the input will turn on the corresponding display digit/segment/dot output.

A significant reduction in discrete board components can be achieved by use of the MM58342, because external pull-down resistors are not required. Due to the nature of the output stage, both its on and off impedance values vary as a function of the display voltage applied. However, *Figures 3a*

Functional Description (Continued)

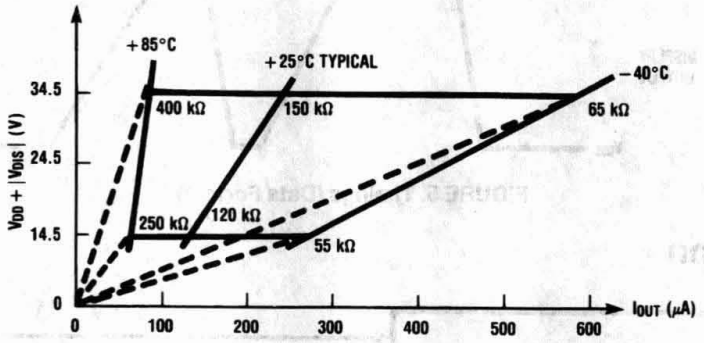
and *3b* show that this output impedance will remain constant for a fixed value of display voltage.

Figure 4 demonstrates the critical timing requirements between CLOCK and DATA IN for the MM58342.

To clear (reset) the display driver at power on or any time, the following flushing routine may be used. With the enable signal high, clock in 20 zeroes. Drive the enable signal low and the display will be blank. It is recommended to clear the driver at power on.

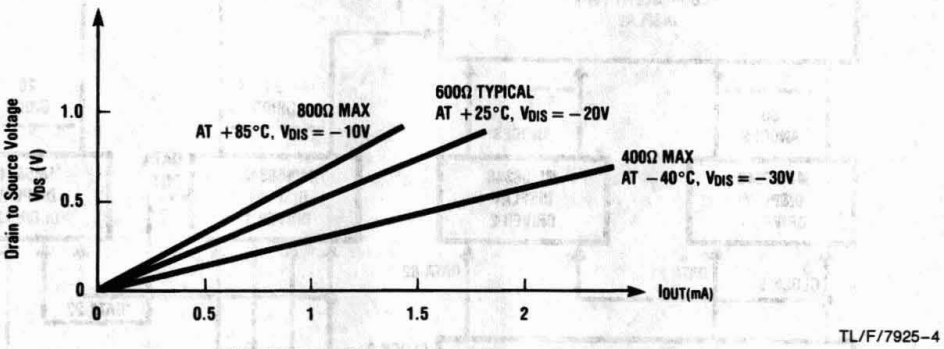
In *Figure 5*, the ENABLE signal acts as an envelope, and only while this signal is at a logic '1' does the circuit accept CLOCK input signals. Data is transferred and shifted in the internal shift register on the rising clock edge, i.e., '0'–'1' transition. When the ENABLE signal goes low, the contents of the shift registers are latched, and the display will show new data. During data transfer, the display will show old data. DATA OUT is also provided on the MM58342 being output on the falling edge. At any time, the display may be blanked under processor control, using the BLANKING CONTROL input.

Figure 6 shows a schematic diagram of a microprocessor-based system where the MM58342 is used to provide the grid drive for a 40-digit 2 line 5 x 7 multiplexed vacuum fluorescent (VF) display. The anode drive in this example is provided by another member of the high voltage display driver family, namely the MM58348, which does not require an externally generated load signal.



TL/F/7925–3

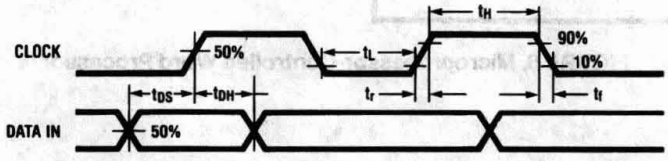
FIGURE 3a. Output Impedance Off



TL/F/7925–4

FIGURE 3b. Output Impedance On

Timing Diagrams

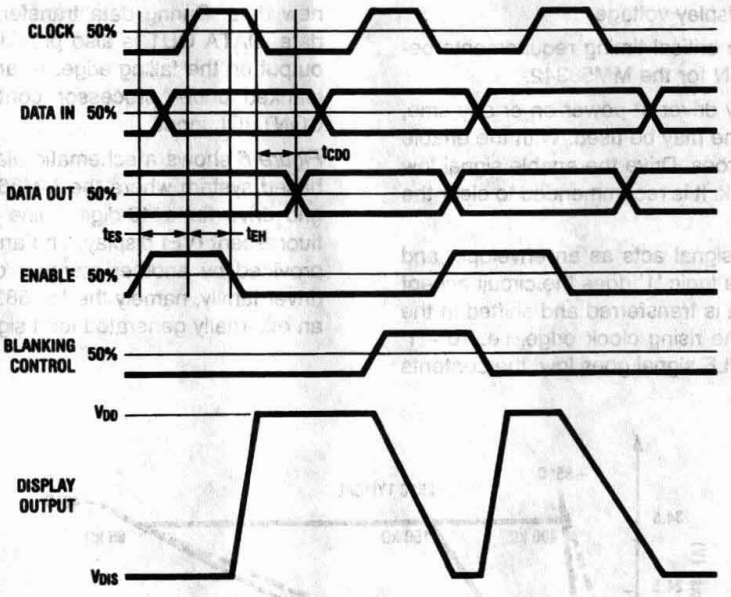


TL/F/7925–5

For the purposes of AC measurement, V_{IH} = 2.4V, V_{IL} = 0.8V.

FIGURE 4. Clock and Data Timings

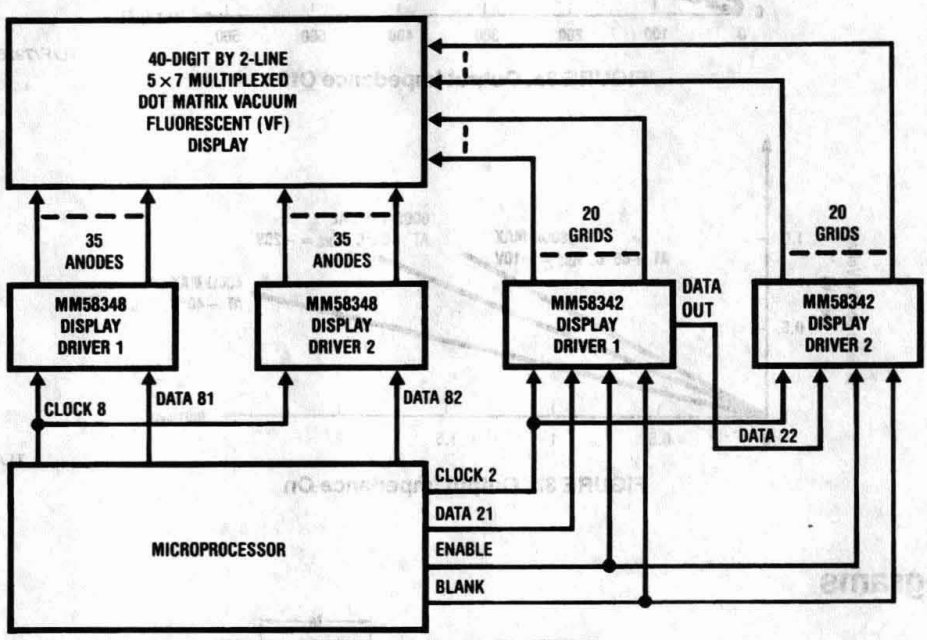
Timing Diagrams (Continued)



TL/F/7925–6

FIGURE 5. Timings (Data Format)

Typical Application



TL/F/7925–7

FIGURE 6. Microprocessor-Controlled Word Processor

National Semiconductor

LM565/LM565C Phase Locked Loop

General Description

The LM565 and LM565C are general purpose phase locked loops containing a stable, highly linear voltage controlled oscillator for low distortion FM demodulation, and a double balanced phase detector with good carrier suppression. The VCO frequency is set with an external resistor and capacitor, and a tuning range of 10:1 can be obtained with the same capacitor. The characteristics of the closed loop system—bandwidth, response speed, capture and pull in range—may be adjusted over a wide range with an external resistor and capacitor. The loop may be broken between the VCO and the phase detector for insertion of a digital frequency divider to obtain frequency multiplication.

The LM565H is specified for operation over the −55°C to +125°C military temperature range. The LM565CN is specified for operation over the 0°C to +70°C temperature range.

Features

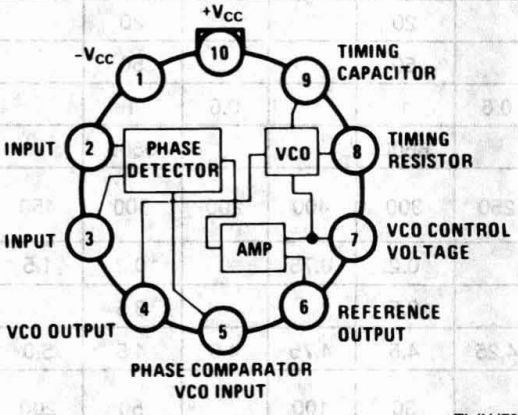
- 200 ppm/°C frequency stability of the VCO
- Power supply range of ±5 to ±12 volts with 100 ppm/% typical
- 0.2% linearity of demodulated output
- Linear triangle wave with in phase zero crossings available
- TTL and DTL compatible phase detector input and square wave output
- Adjustable hold in range from ±1% to > ±60%

Applications

- Data and tape synchronization
- Modems
- FSK demodulation
- FM demodulation
- Frequency synthesizer
- Tone decoding
- Frequency multiplication and division
- SCA demodulators
- Telemetry receivers
- Signal regeneration
- Coherent demodulators

Connection Diagrams

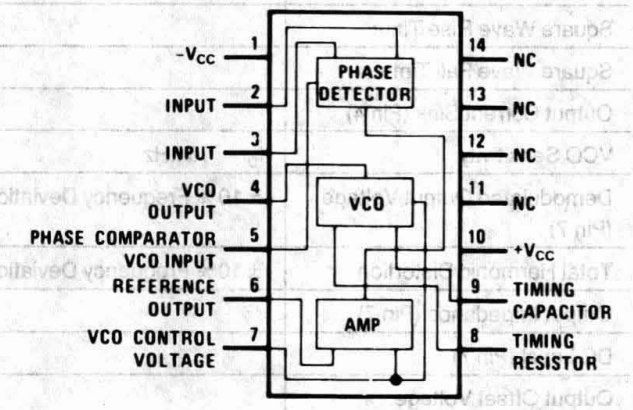
Metal Can Package



TL/H/7853–2

Order Number LM565H
See NS Package Number H10C

Dual-In-Line Package



TL/H/7853–3

Order Number LM565CN
See NS Package Number N14A

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	±12V
Power Dissipation (Note 1)	1400 mW
Differential Input Voltage	±1V
Operating Temperature Range	
LM565H	−55°C to +125°C
LM565CN	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec.)	260°C

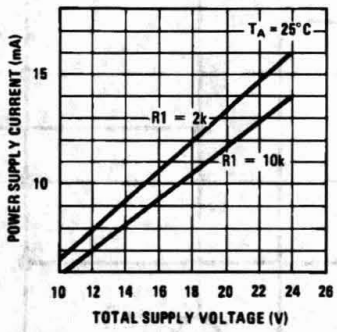
Electrical Characteristics AC Test Circuit, $T_A = 25°C$, $V_{CC} = \pm 6V$

Parameter	Conditions	LM565			LM565C			Units
		Min	Typ	Max	Min	Typ	Max	
Power Supply Current			8.0	12.5		8.0	12.5	mA
Input Impedance (Pins 2, 3)	$-4V < V_2, V_3 < 0V$	7	10			5		kΩ
VCO Maximum Operating Frequency	$C_o = 2.7$ pF	300	500		250	500		kHz
VCO Free-Running Frequency	$C_o = 1.5$ nF $R_o = 20$ kΩ $f_o = 10$ kHz	−10	0	+10	−30	0	+30	%
Operating Frequency Temperature Coefficient			−100			−200		ppm/°C
Frequency Drift with Supply Voltage			0.1	1.0		0.2	1.5	%/V
Triangle Wave Output Voltage		2	2.4	3	2	2.4	3	V_{p-p}
Triangle Wave Output Linearity			0.2			0.5		%
Square Wave Output Level		4.7	5.4		4.7	5.4		V_{p-p}
Output Impedance (Pin 4)			5			5		kΩ
Square Wave Duty Cycle		45	50	55	40	50	60	%
Square Wave Rise Time			20			20		ns
Square Wave Fall Time			50			50		ns
Output Current Sink (Pin 4)		0.6	1		0.6	1		mA
VCO Sensitivity	$f_o = 10$ kHz		6600			6600		Hz/V
Demodulated Output Voltage (Pin 7)	±10% Frequency Deviation	250	300	400	200	300	450	mV_{p-p}
Total Harmonic Distortion	±10% Frequency Deviation		0.2	0.75		0.2	1.5	%
Output Impedance (Pin 7)			3.5			3.5		kΩ
DC Level (Pin 7)		4.25	4.5	4.75	4.0	4.5	5.0	V
Output Offset Voltage $\lvert V_7 - V_6 \rvert$			30	100		50	200	mV
Temperature Drift of $\lvert V_7 - V_6 \rvert$			500			500		μV/°C
AM Rejection		30	40			40		dB
Phase Detector Sensitivity K_D			.68			.68		V/radian

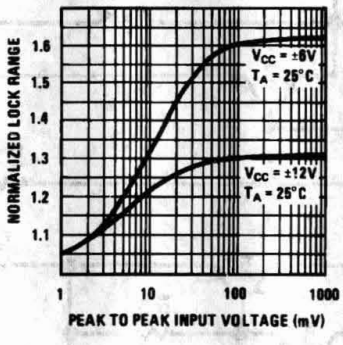
Note 1: The maximum junction temperature of the LM565 and LM565C is +150°C. For operation at elevated temperatures, devices in the TO-5 package must be derated based on a thermal resistance of +150°C/W junction to ambient or +45°C/W junction to case. Thermal resistance of the dual-in-line package is +85°C/W.

Typical Performance Characteristics

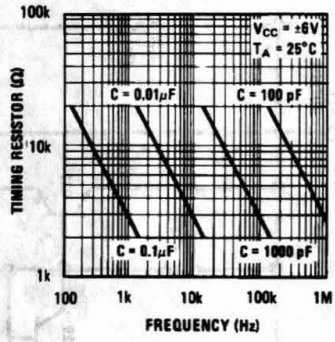
Power Supply Current as a Function of Supply Voltage



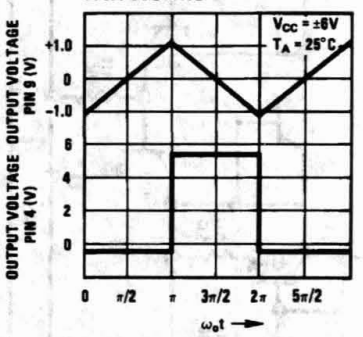
Lock Range as a Function of Input Voltage



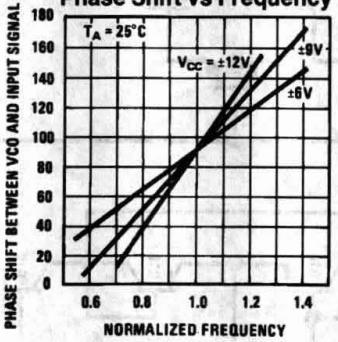
VCO Frequency



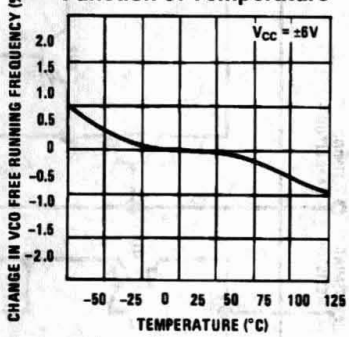
Oscillator Output Waveforms



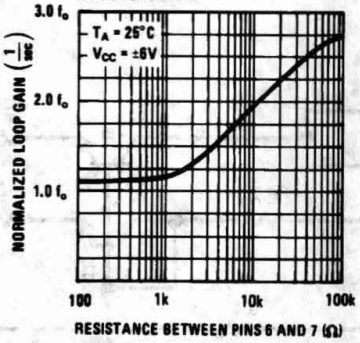
Phase Shift vs Frequency



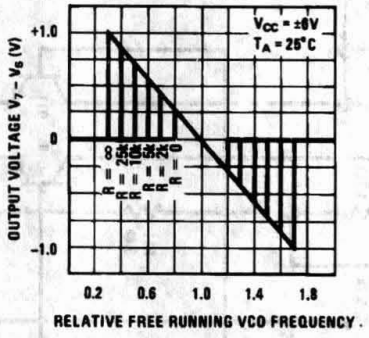
VCO Frequency as a Function of Temperature



Loop Gain vs Load Resistance

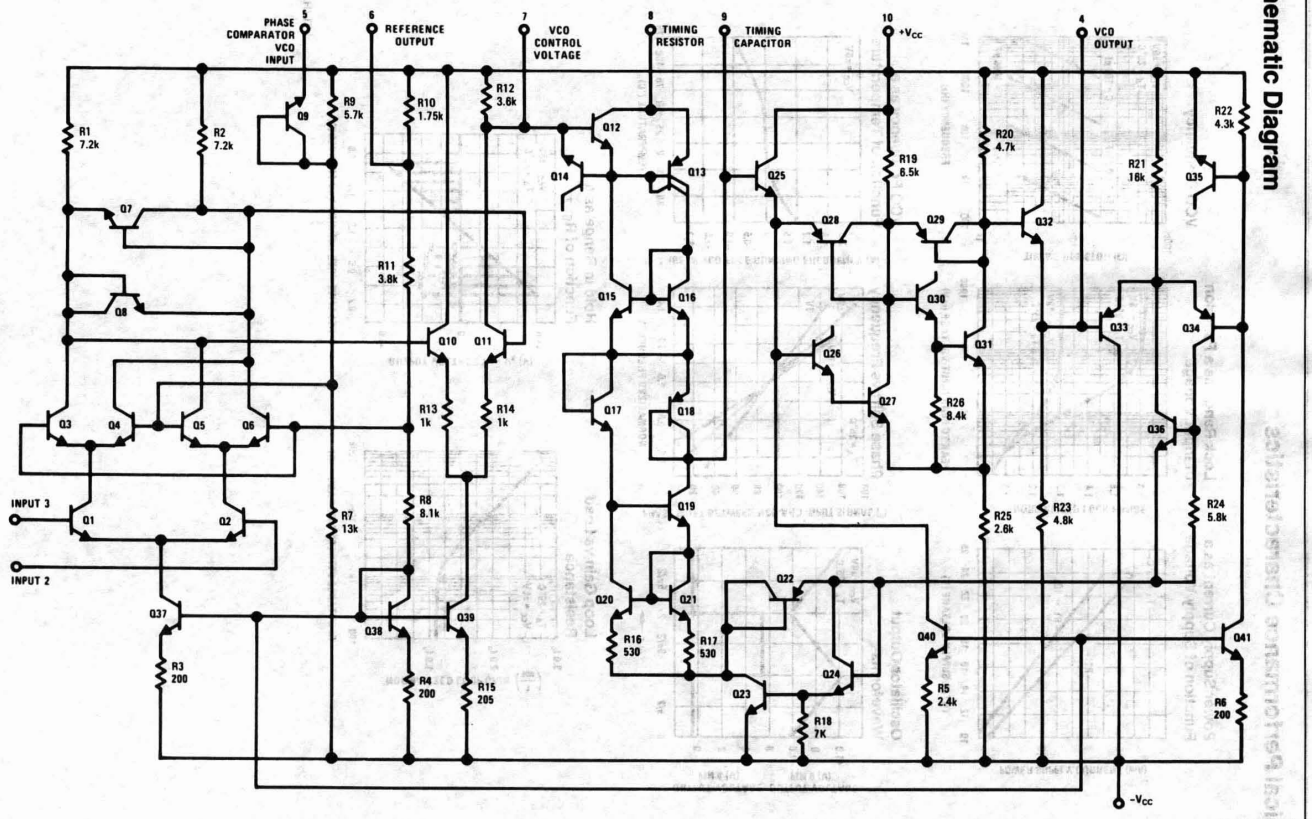


Hold in Range as a Function of R_{6-7}



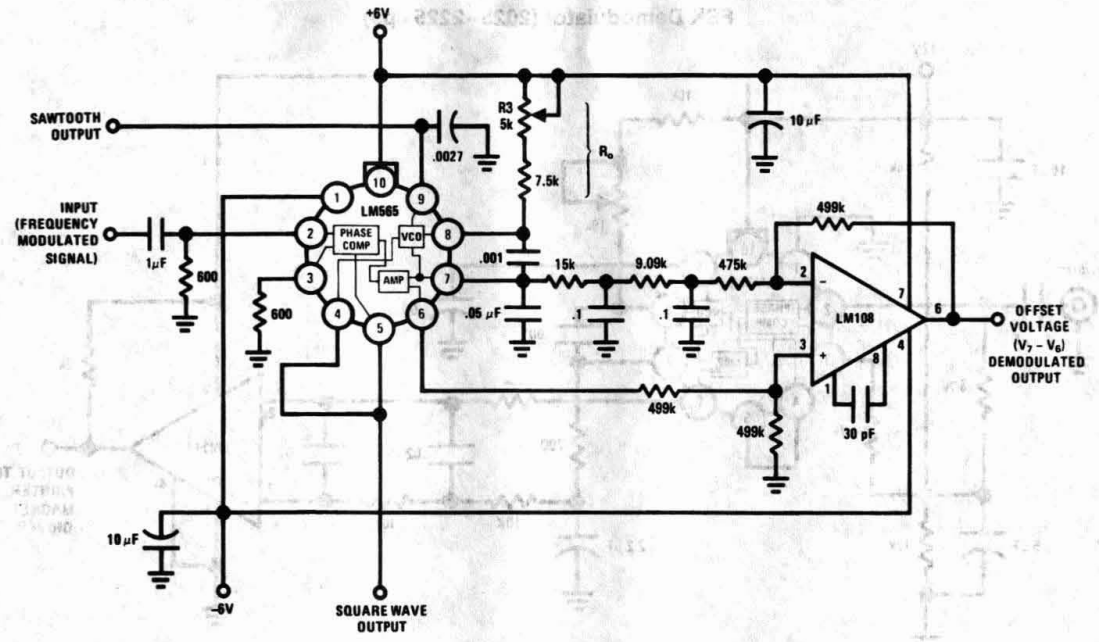
TL/H/7853–4

Schematic Diagram



TL/H/7853–1

AC Test Circuit

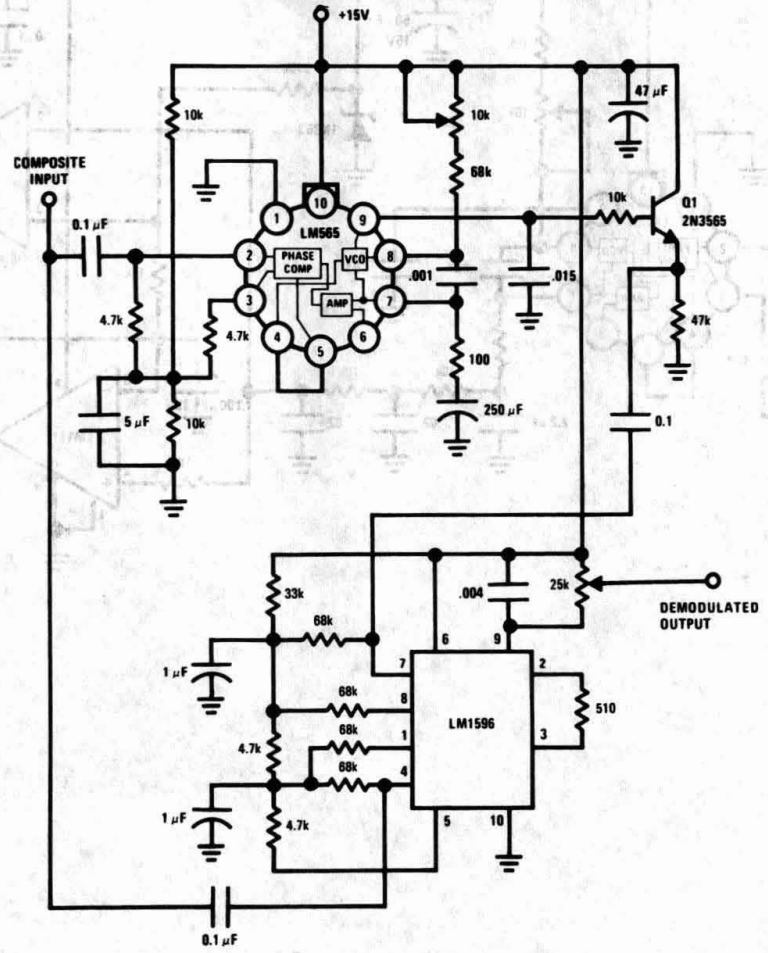


TL/H/7853–5

Note: S_1 open for output offset voltage ($V_7 - V_6$) measurement.

Typical Applications

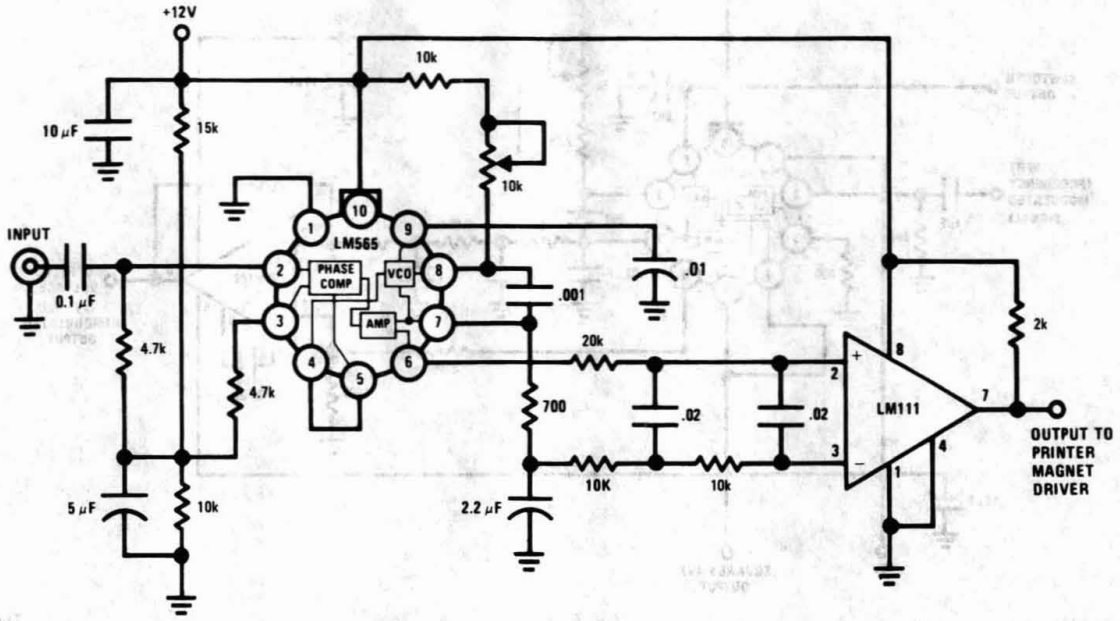
2400 Hz Synchronous AM Demodulator



TL/H/7853–6

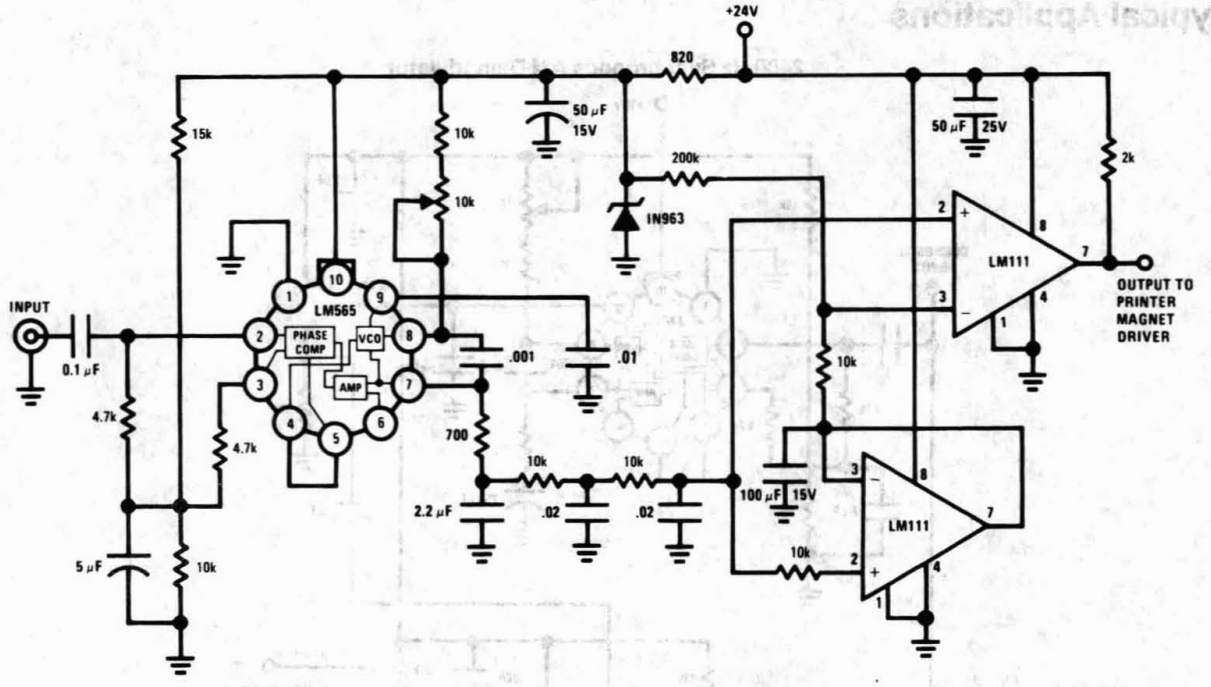
Typical Applications (Continued)

FSK Demodulator (2025–2225 cps)



TL/H/7853–7

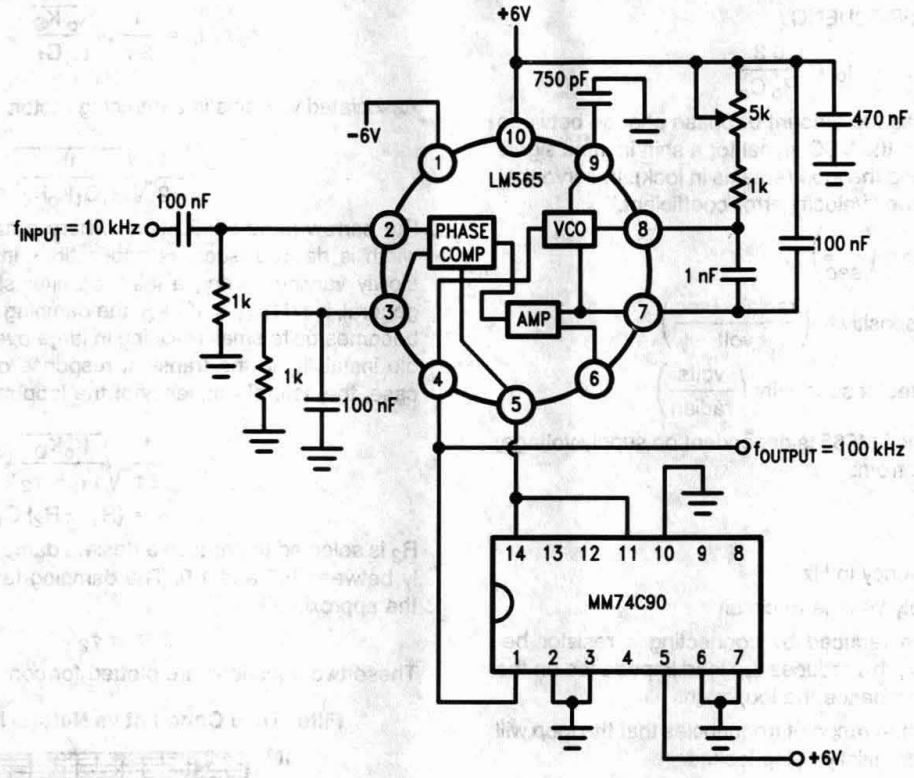
FSK Demodulator with DC Restoration



TL/H/7853–8

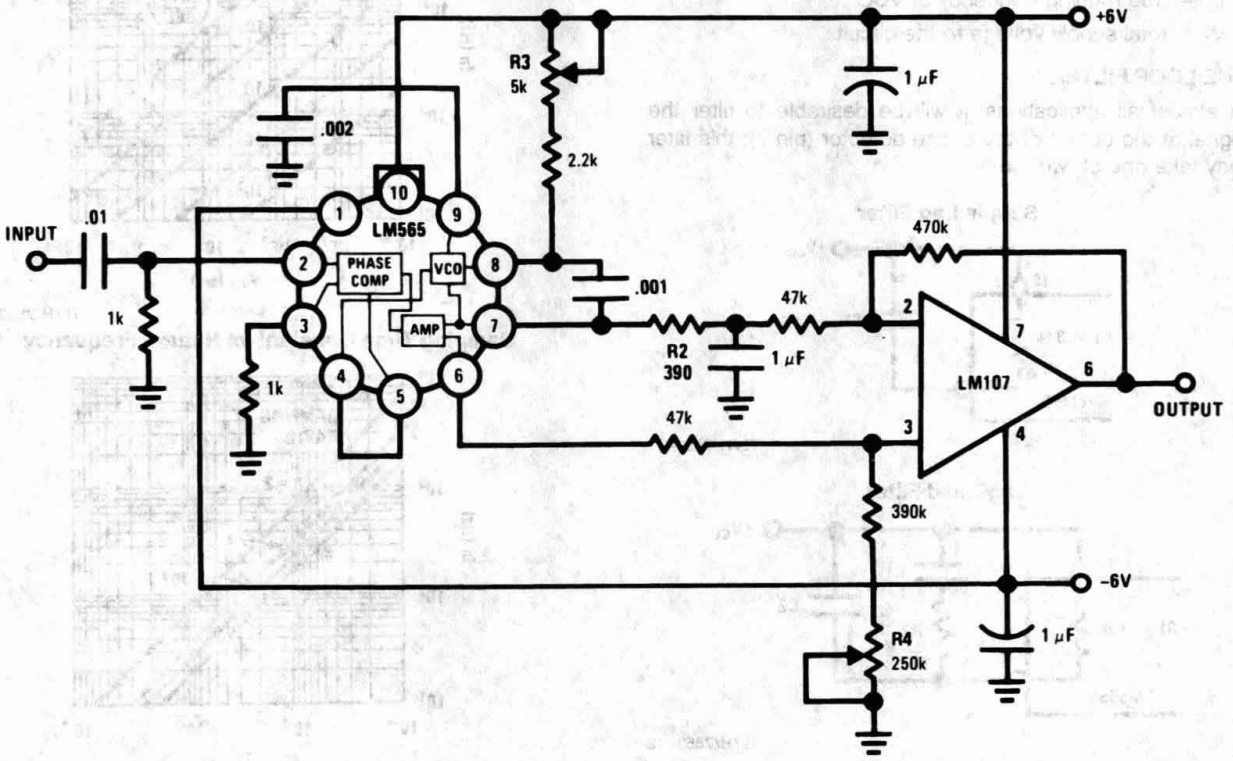
Typical Applications (Continued)

Frequency Multiplier (×10)



TL/H/7853–9

IRIG Channel 13 Demodulator



TL/H/7853–10

Applications Information

In designing with phase locked loops such as the LM565, the important parameters of interest are:

FREE RUNNING FREQUENCY

$$f_o \cong \frac{0.3}{R_o C_o}$$

LOOP GAIN: relates the amount of phase change between the input signal and the VCO signal for a shift in input signal frequency (assuming the loop remains in lock). In servo theory, this is called the "velocity error coefficient."

$$\text{Loop gain} = K_o K_D \left(\frac{1}{\text{sec}}\right)$$

K_o = oscillator sensitivity $\left(\frac{\text{radians/sec}}{\text{volt}}\right)$

K_D = phase detector sensitivity $\left(\frac{\text{volts}}{\text{radian}}\right)$

The loop gain of the LM565 is dependent on supply voltage, and may be found from:

$$K_o K_D = \frac{33.6\, f_o}{V_c}$$

f_o = VCO frequency in Hz

V_c = total supply voltage to circuit

Loop gain may be reduced by connecting a resistor between pins 6 and 7; this reduces the load impedance on the output amplifier and hence the loop gain.

HOLD IN RANGE: the range of frequencies that the loop will remain in lock after initially being locked.

$$f_H = \pm\frac{8\, f_o}{V_c}$$

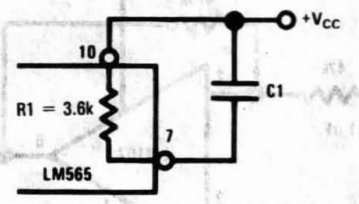
f_o = free running frequency of VCO

V_c = total supply voltage to the circuit

THE LOOP FILTER

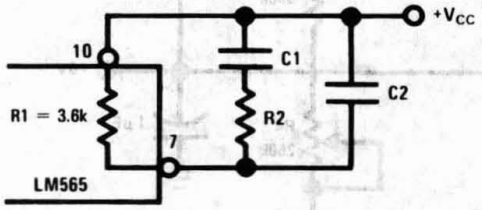
In almost all applications, it will be desirable to filter the signal at the output of the phase detector (pin 7); this filter may take one of two forms:

Simple Lag Filter



TL/H/7853–11

Lag-Lead Filter



TL/H/7853–12

A simple lag filter may be used for wide closed loop bandwidth applications such as modulation following where the frequency deviation of the carrier is fairly high (greater than 10%), or where wideband modulating signals must be followed.

The natural bandwidth of the closed loop response may be found from:

$$f_n = \frac{1}{2\pi}\sqrt{\frac{K_o K_D}{R_1 C_1}}$$

Associated with this is a damping factor:

$$\delta = \frac{1}{2}\sqrt{\frac{1}{R_1 C_1 K_o K_D}}$$

For narrow band applications where a narrow noise bandwidth is desired, such as applications involving tracking a slowly varying carrier, a lead lag filter should be used. In general, if $1/R_1C_1 < K_o K_D$, the damping factor for the loop becomes quite small resulting in large overshoot and possible instability in the transient response of the loop. In this case, the natural frequency of the loop may be found from

$$f_n = \frac{1}{2\pi}\sqrt{\frac{K_o K_D}{\tau_1 + \tau_2}}$$

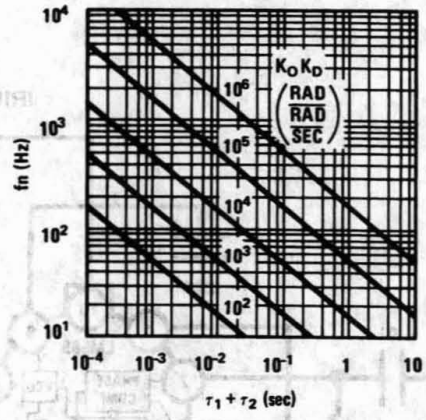
$$\tau_1 + \tau_2 = (R_1 + R_2)\, C_1$$

R_2 is selected to produce a desired damping factor δ, usually between 0.5 and 1.0. The damping factor is found from the approximation:

$$\delta \approx \pi\, \tau_2 f_n$$

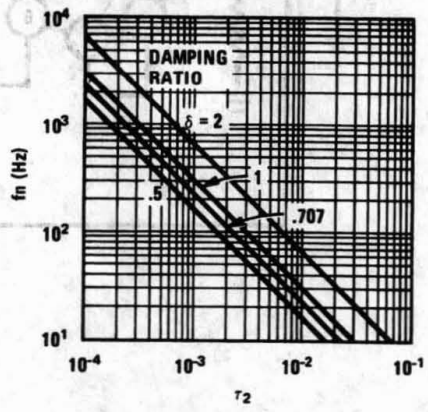
These two equations are plotted for convenience.

Filter Time Constant vs Natural Frequency



TL/H/7853–13

Damping Time Constant vs Natural Frequency



TL/H/7853–14

Capacitor C_2 should be much smaller than C_1 since its function is to provide filtering of carrier. In general $C_2 \leq 0.1\, C_1$.

National Semiconductor

LM567/LM567C Tone Decoder

General Description

The LM567 and LM567C are general purpose tone decoders designed to provide a saturated transistor switch to ground when an input signal is present within the passband. The circuit consists of an I and Q detector driven by a voltage controlled oscillator which determines the center frequency of the decoder. External components are used to independently set center frequency, bandwidth and output delay.

Features

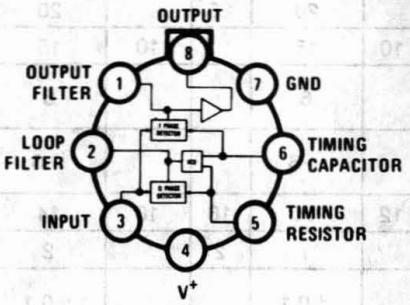
- 20 to 1 frequency range with an external resistor
- Logic compatible output with 100 mA current sinking capability
- Bandwidth adjustable from 0 to 14%
- High rejection of out of band signals and noise
- Immunity to false signals
- Highly stable center frequency
- Center frequency adjustable from 0.01 Hz to 500 kHz

Applications

- Touch tone decoding
- Precision oscillator
- Frequency monitoring and control
- Wide band FSK demodulation
- Ultrasonic controls
- Carrier current remote controls
- Communications paging decoders

Connection Diagrams

Metal Can Package

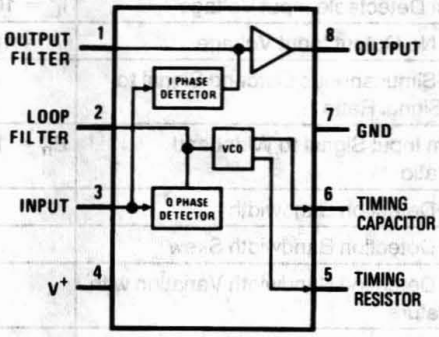


TL/H/6975–1

Top View

Order Number LM567H or LM567CH
See NS Package Number H08C

Dual-In-Line and Small Outline Packages



TL/H/6975–2

Top View

Order Number LM567CM
See NS Package Number M08A
Order Number LM567CN
See NS Package Number N08E

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage Pin	9V
Power Dissipation (Note 1)	1100 mW
V_8	15V
V_3	−10V
V_3	V_4 + 0.5V
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	
LM567H	−55°C to +125°C
LM567CH, LM567CM, LM567CN	0°C to +70°C

Soldering Information

Dual-In-Line Package	
Soldering (10 sec.)	260°C
Small Outline Package	
Vapor Phase (60 sec.)	215°C
Infrared (15 sec.)	220°C

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.

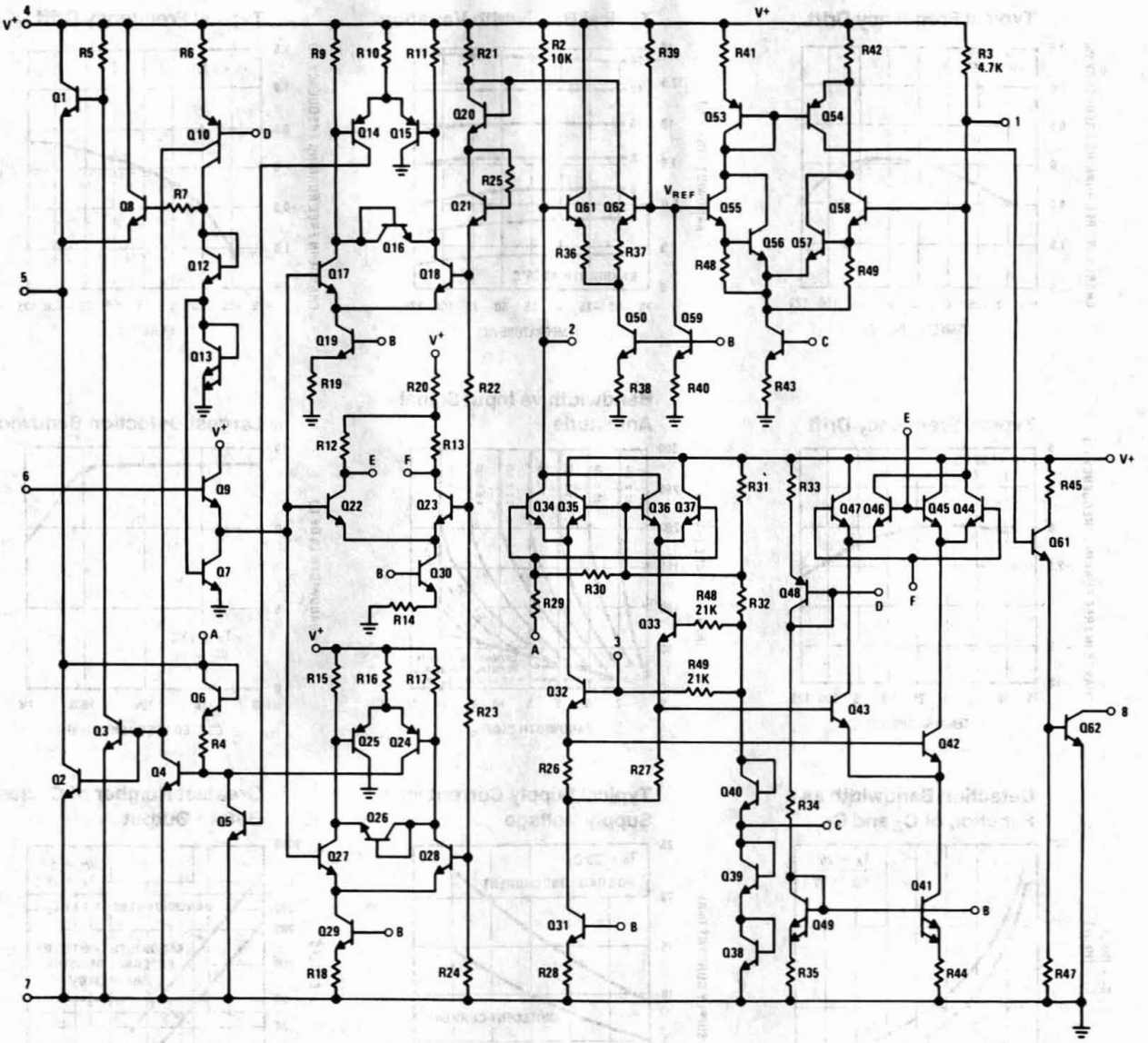
Electrical Characteristics AC Test Circuit, T_A = 25°C, V^+ = 5V

Parameters	Conditions	LM567			LM567C/LM567CM			Units
		Min	Typ	Max	Min	Typ	Max	
Power Supply Voltage Range		4.75	5.0	9.0	4.75	5.0	9.0	V
Power Supply Current Quiescent	R_L = 20k		6	8		7	10	mA
Power Supply Current Activated	R_L = 20k		11	13		12	15	mA
Input Resistance		18	20		15	20		kΩ
Smallest Detectable Input Voltage	I_L = 100 mA, $f_i = f_o$		20	25		20	25	mVrms
Largest No Output Input Voltage	I_C = 100 mA, $f_i = f_o$	10	15		10	15		mVrms
Largest Simultaneous Outband Signal to Inband Signal Ratio			6			6		dB
Minimum Input Signal to Wideband Noise Ratio	B_n = 140 kHz		−6			−6		dB
Largest Detection Bandwidth		12	14	16	10	14	18	% of f_o
Largest Detection Bandwidth Skew			1	2		2	3	% of f_o
Largest Detection Bandwidth Variation with Temperature			±0.1			±0.1		%/°C
Largest Detection Bandwidth Variation with Supply Voltage	4.75 − 6.75V		±1	±2		±1	±5	%V
Highest Center Frequency		100	500		100	500		kHz
Center Frequency Stability (4.75–5.75V)	$0 < T_A < 70$ $-55 < T_A < +125$		35 ± 60 35 ± 140			35 ±60 35 ± 140		ppm/°C ppm/°C
Center Frequency Shift with Supply Voltage	4.75V − 6.75V 4.75V − 9V		0.5	1.0 2.0		0.4	2.0 2.0	%/V %/V
Fastest ON-OFF Cycling Rate			f_o/20			f_o/20		
Output Leakage Current	V_8 = 15V		0.01	25		0.01	25	μA
Output Saturation Voltage	e_i = 25 mV, I_8 = 30 mA e_i = 25 mV, I_8 = 100 mA		0.2 0.6	0.4 1.0		0.2 0.6	0.4 1.0	V
Output Fall Time			30			30		ns
Output Rise Time			150			150		ns

Note 1: The maximum junction temperature of the LM567 and LM567C is 150°C. For operating at elevated temperatures, devices in the TO-5 package must be derated based on a thermal resistance of 150°C/W, junction to ambient or 45°C/W, junction to case. For the DIP the device must be derated based on a thermal resistance of 110°C/W, junction to ambient. For the Small Outline package, the device must be derated based on a thermal resistance of 160°C/W, junction to ambient.

Note 2: Refer to RETS567X drawing for specifications of military LM567H version.

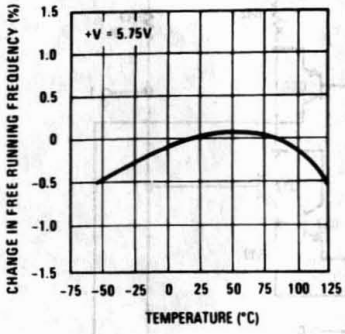
Schematic Diagram



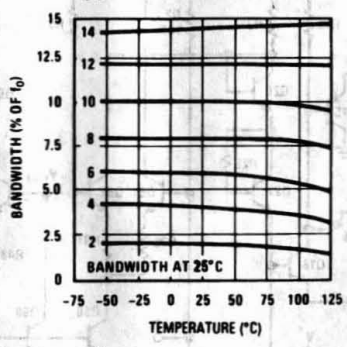
TL/H/6975-3

Typical Performance Characteristics

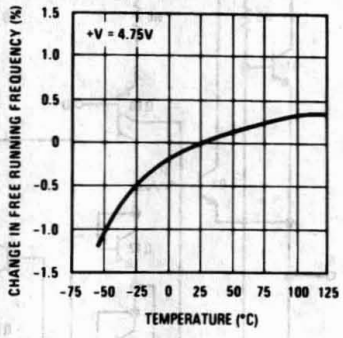
Typical Frequency Drift



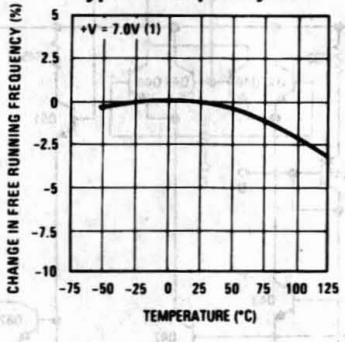
Typical Bandwidth Variation



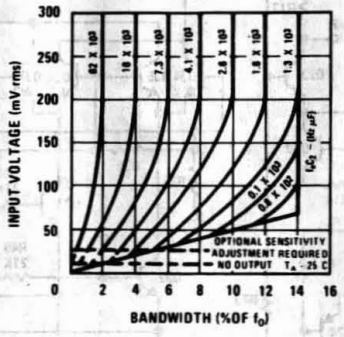
Typical Frequency Drift



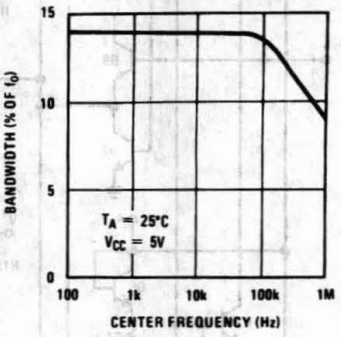
Typical Frequency Drift



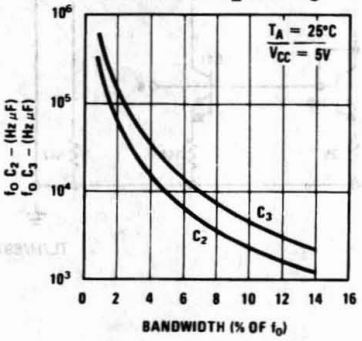
Bandwidth vs Input Signal Amplitude



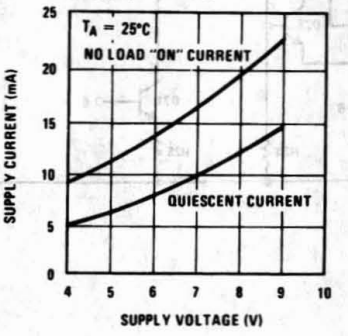
Largest Detection Bandwidth



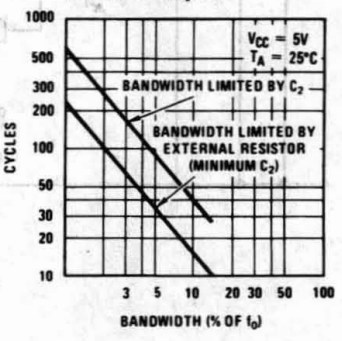
Detection Bandwidth as a Function of C_2 and C_3



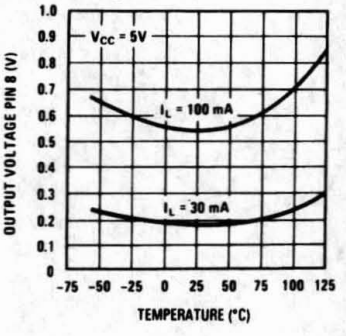
Typical Supply Current vs Supply Voltage



Greatest Number of Cycles Before Output



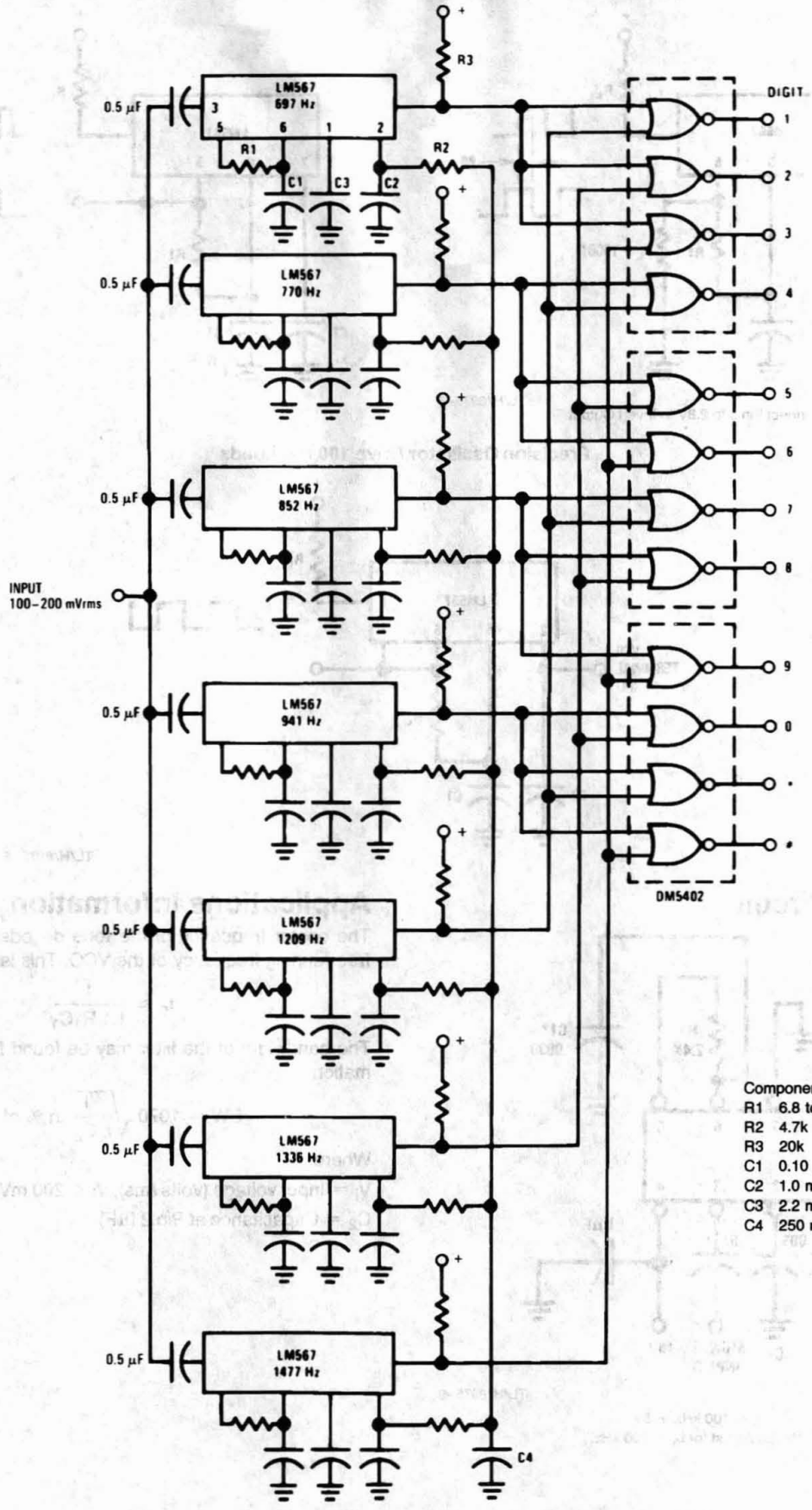
Typical Output Voltage vs Temperature



TL/H/6975–4

Typical Applications

Touch-Tone Decoder



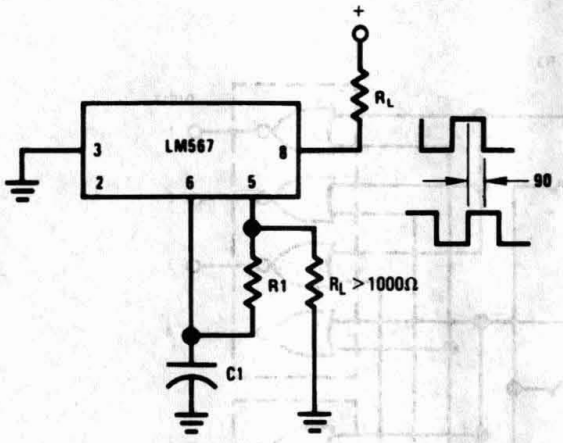
Component values (typ)

R1	6.8 to 15k
R2	4.7k
R3	20k
C1	0.10 mfd
C2	1.0 mfd 6V
C3	2.2 mfd 6V
C4	250 mfd 6V

TL/H/6975–5

Typical Applications (Continued)

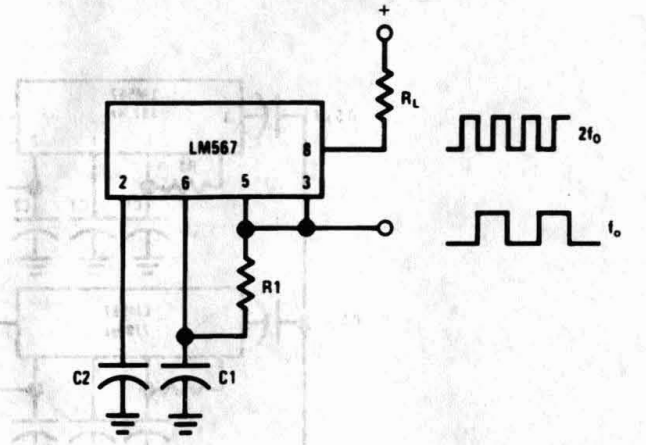
Oscillator with Quadrature Output



TL/H/6975–6

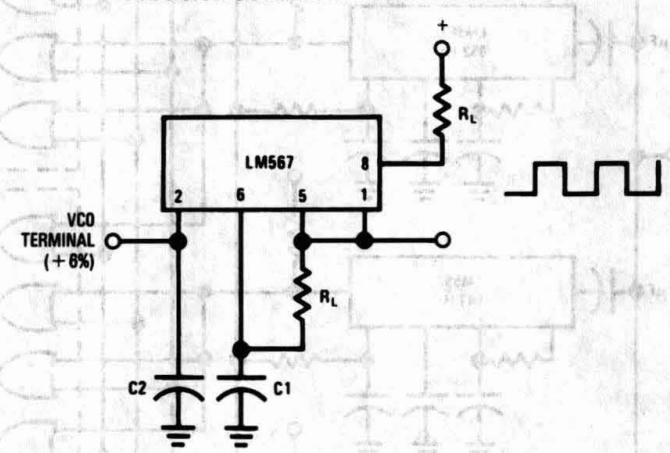
Connect Pin 3 to 2.8V to Invert Output

Oscillator with Double Frequency Output



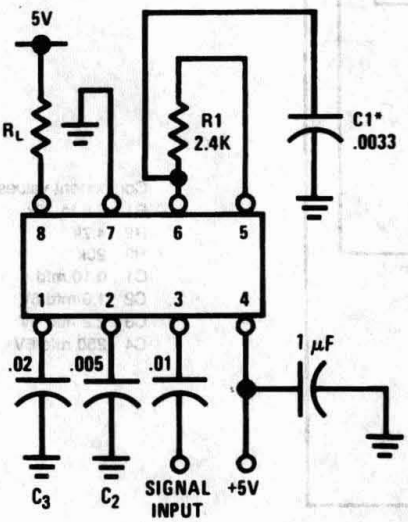
TL/H/6975–7

Precision Oscillator Drive 100 mA Loads



TL/H/6975–8

AC Test Circuit



TL/H/6975–9

f_i = 100 kHz + 5V

***Note:** Adjust for f_o = 100 kHz.

Applications Information

The center frequency of the tone decoder is equal to the free running frequency of the VCO. This is given by

$$f_o \cong \frac{1}{1.1\ R_1 C_1}$$

The bandwidth of the filter may be found from the approximation

$$BW = 1070 \sqrt{\frac{V_i}{f_o C_2}} \text{ in \% of } f_o$$

Where:

V_i = Input voltage (volts rms), $V_i \leq 200$ mV

C_2 = Capacitance at Pin 2 (μF)

National Semiconductor

LM1596/LM1496 Balanced Modulator-Demodulator

General Description

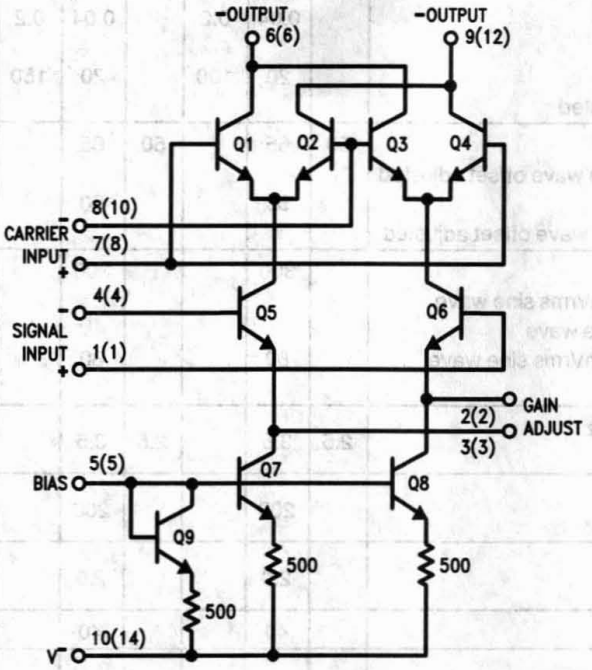
The LM1596/LM1496 are doubled balanced modulator-demodulators which produce an output voltage proportional to the product of an input (signal) voltage and a switching (carrier) signal. Typical applications include suppressed carrier modulation, amplitude modulation, synchronous detection, FM or PM detection, broadband frequency doubling and chopping.

The LM1596 is specified for operation over the −55°C to +125°C military temperature range. The LM1496 is specified for operation over the 0°C to +70°C temperature range.

Features

- Excellent carrier suppression
  65 dB typical at 0.5 MHz
  50 dB typical at 10 MHz
- Adjustable gain and signal handling
- Fully balanced inputs and outputs
- Low offset and drift
- Wide frequency response up to 100 MHz

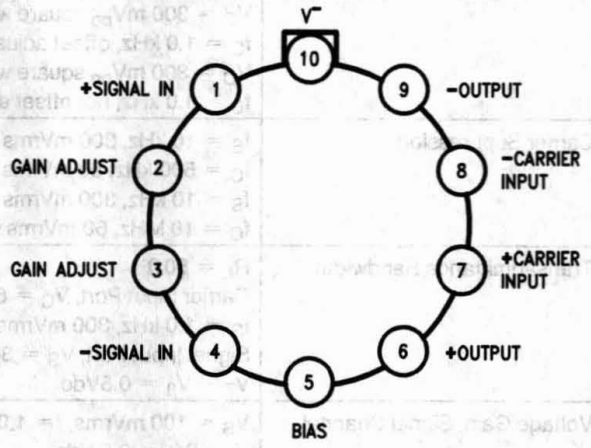
Schematic and Connection Diagrams



TL/H/7887–1

Numbers in parentheses show DIP connections.

Metal Can Package



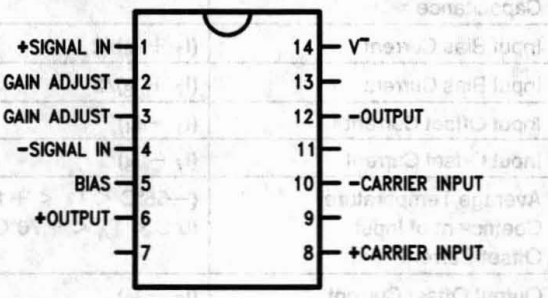
TL/H/7887–2

Top View

Note: Pin 10 is connected electrically to the case through the device substrate.

Order Number LM1496H or LM1596H
See NS Package Number H08C

Dual-In-Line and Small Outline Packages



TL/H/7887–3

Order Number LM1496M or LM1496N
See NS Package Number M14A or N14A

4

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Internal Power Dissipation (Note 1)	500 mW
Applied Voltage (Note 2)	30V
Differential Input Signal ($V_7 - V_8$)	±5.0V
Differential Input Signal ($V_4 - V_1$)	$\pm(5+I_5R_0)$V
Input Signal ($V_2 - V_1$, $V_3 - V_4$)	5.0V
Bias Current (I_5)	12 mA
Operating Temperature Range LM1596	−55°C to +125°C
LM1496	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Soldering Information

- Dual-In-Line Package
  - Soldering (10 seconds) 260°C
- Small Outline Package
  - Vapor Phase (60 seconds) 215°C
  - Infrared (15 seconds) 220°C

See AN-450 "Surface Mounting Methods and their effects on Product Reliability" for other methods of soldering surface mount devices.

Electrical Characteristics (T_A = 25°C, unless otherwise specified, see test circuit)

Parameter	Conditions	LM1596			LM1496			Units
		Min	Typ	Max	Min	Typ	Max	
Carrier Feedthrough	V_C = 60 mVrms sine wave f_C = 1.0 kHz, offset adjusted		40			40		μVrms
	V_C = 60 mVrms sine wave f_C = 10 kHz, offset adjusted		140			140		μVrms
	V_C = 300 mV_{pp} square wave f_C = 1.0 kHz, offset adjusted		0.04	0.2		0.04	0.2	mVrms
	V_C = 300 mV_{pp} square wave f_C = 1.0 kHz, not offset adjusted		20	100		20	150	mVrms
Carrier Suppression	f_S = 10 kHz, 300 mVrms f_C = 500 kHz, 60 mVrms sine wave offset adjusted	50	65		50	65		dB
	f_S = 10 kHz, 300 mVrms f_C = 10 MHz, 60 mVrms sine wave offset adjusted		50			50		dB
Transadmittance Bandwidth	R_L = 50Ω Carrier Input Port, V_C = 60 mVrms sine wave		300			300		MHz
	f_S = 1.0 kHz, 300 mVrms sine wave Signal Input Port, V_S = 300 mVrms sine wave $V_7 - V_8$ = 0.5Vdc		80			80		MHz
Voltage Gain, Signal Channel	V_S = 100 mVrms, f = 1.0 kHz $V_7 - V_8$ = 0.5 Vdc	2.5	3.5		2.5	3.5		V/V
Input Resistance, Signal Port	f = 5.0 MHz $V_7 - V_8$ = 0.5 Vdc		200			200		kΩ
Input Capacitance, Signal Port	f = 5.0 MHz $V_7 - V_8$ = 0.5 Vdc		2.0			2.0		pF
Single Ended Output Resistance	f = 10 MHz		40			40		kΩ
Single Ended Output Capacitance	f = 10 MHz		5.0			5.0		pF
Input Bias Current	$(I_1 + I_4)/2$		12	25		12	30	μA
Input Bias Current	$(I_7 + I_8)/2$		12	25		12	30	μA
Input Offset Current	$(I_1 - I_4)$		0.7	5.0		0.7	5.0	μA
Input Offset Current	$(I_7 - I_8)$		0.7	5.0		5.0	5.0	μA
Average Temperature Coefficient of Input Offset Current	(−55°C < T_A < +125°C) (0°C < T_A < +70°C)		2.0			2.0		nA/°C nA/°C
Output Offset Current	$(I_6 - I_9)$		14	50		14	60	μA
Average Temperature Coefficient of Output Offset Current	(−55°C < T_A < +125°C) (0°C < T_A < +70°C)		90			90		nA/°C nA/°C

Electrical Characteristics (T_A = 25°C, unless otherwise specified, see test circuit) (Continued)

Parameter	Conditions	LM1596			LM1496			Units
		Min	Typ	Max	Min	Typ	Max	
Signal Port Common Mode Input Voltage Range	f_S = 1.0 kHz		5.0			5.0		V_{p-p}
Signal Port Common Mode Rejection Ratio	$V_7 - V_8$ = 0.5 Vdc		−85			−85		dB
Common Mode Quiescent Output Voltage			8.0			8.0		Vdc
Differential Output Swing Capability			8.0			8.0		V_{p-p}
Positive Supply Current	$(I_6 + I_8)$		2.0	3.0		2.0	3.0	mA
Negative Supply Current	(I_{10})		3.0	4.0		3.0	4.0	mA
Power Dissipation			33			33		mW

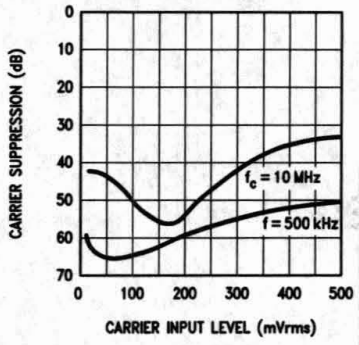
Note 1: LM1596 rating applies to case temperatures to +125°C; derate linearly at 6.5 mW/°C for ambient temperature above 75°C. LM1496 rating applies to case temperatures to +70°C.

Note 2: Voltage applied between pins 6-7, 8-1, 9-7, 9-8, 7-4, 7-1, 8-4, 6-8, 2-5, 3-5.

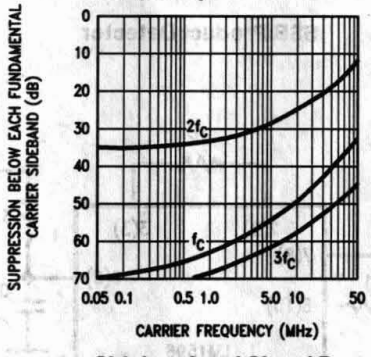
Note 3: Refer to rets1596x drawing for specifications of military LM1596H versions.

Typical Performance Characteristics

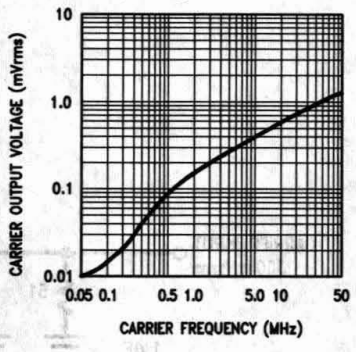
Carrier Suppression vs Carrier Input Level



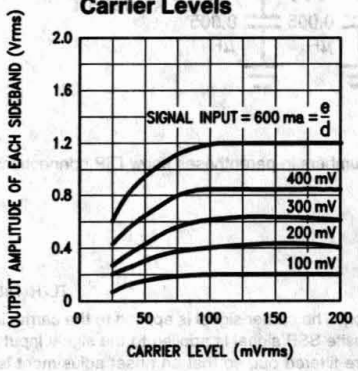
Carrier Suppression vs Frequency



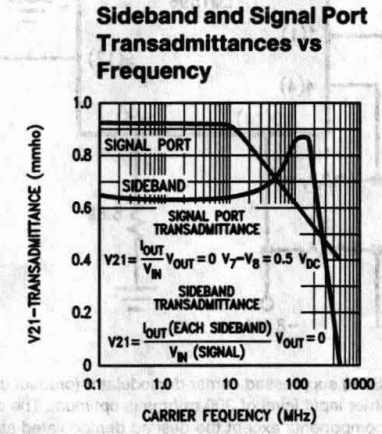
Carrier Feedthrough vs Frequency



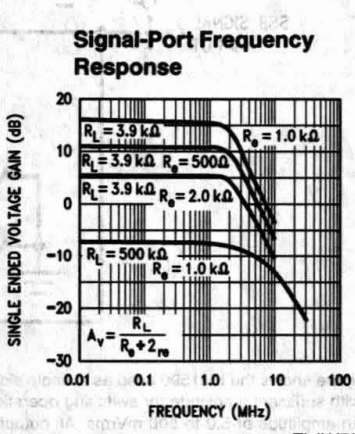
Sideband Output vs Carrier Levels



Sideband and Signal Port Transadmittances vs Frequency



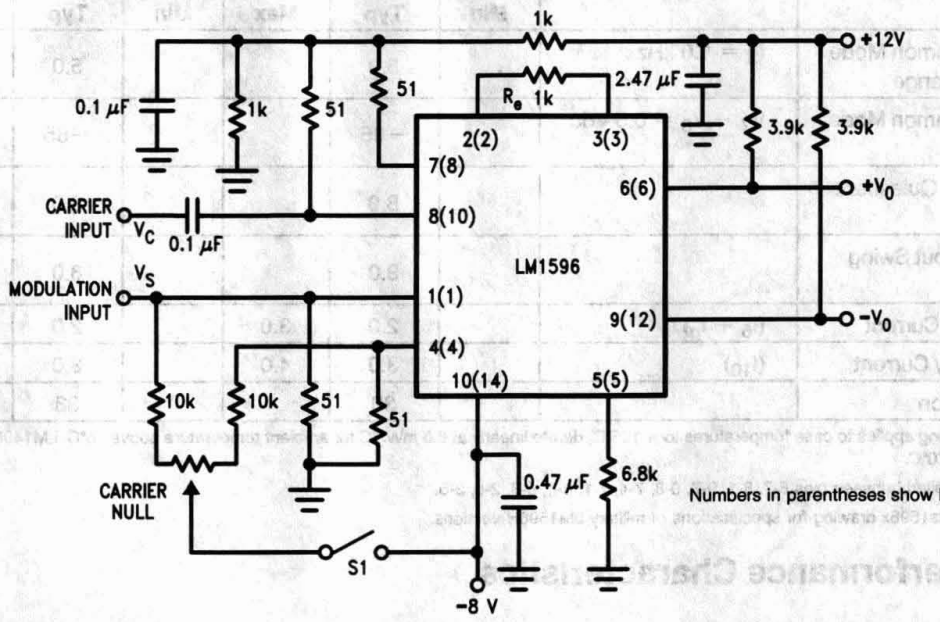
Signal-Port Frequency Response



TL/H/7887–5

Typical Application and Test Circuit

Suppressed Carrier Modulator

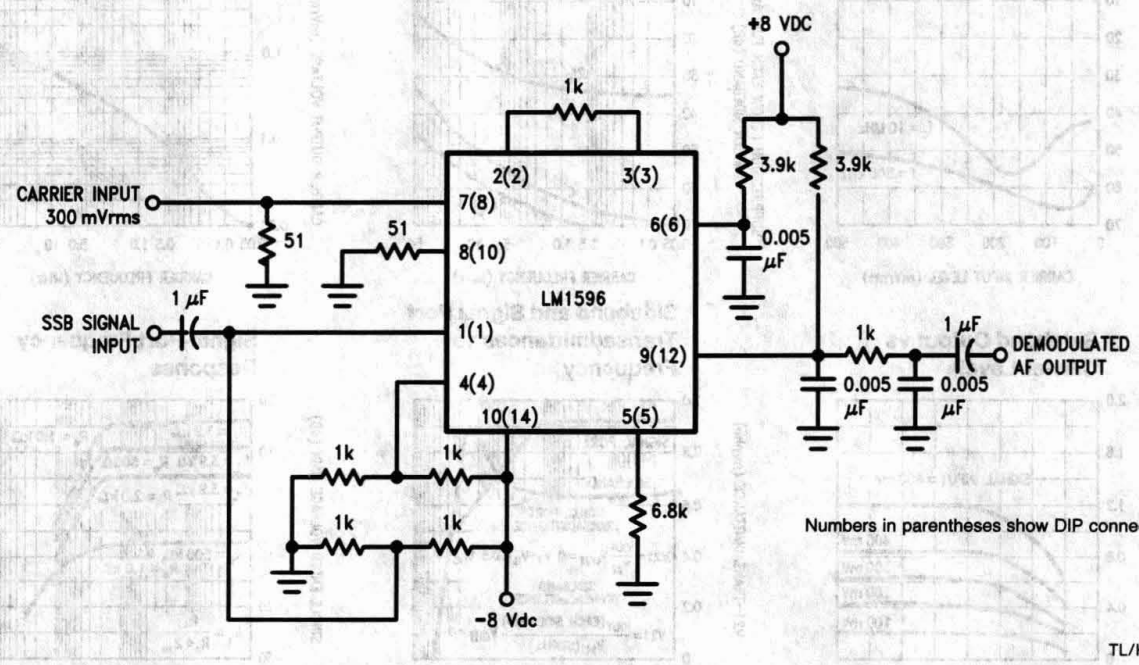


Numbers in parentheses show DIP connections.

TL/H/7887–4

Note: S_1 is closed for "adjusted" measurements.

SSB Product Detector



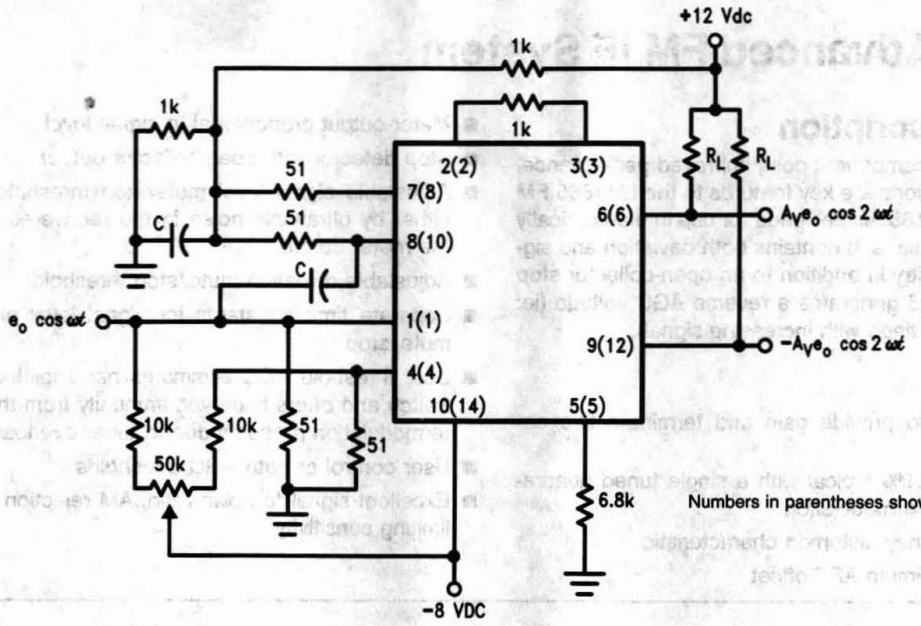
Numbers in parentheses show DIP connections.

TL/H/7887–6

This figure shows the LM1596 used as a single sideband (SSB) suppressed carrier demodulator (product detector). The carrier signal is applied to the carrier input port with sufficient amplitude for switching operation. A carrier input level of 300 mVrms is optimum. The composite SSB signal is applied to the signal input port with an amplitude of 5.0 to 500 mVrms. All output signal components except the desired demodulated audio are filtered out, so that an offset adjustment is not required. This circuit may also be used as an AM detector by applying composite and carrier signals in the same manner as described for product detector operation.

Typical Applications (Continued)

Broadband Frequency Doubler

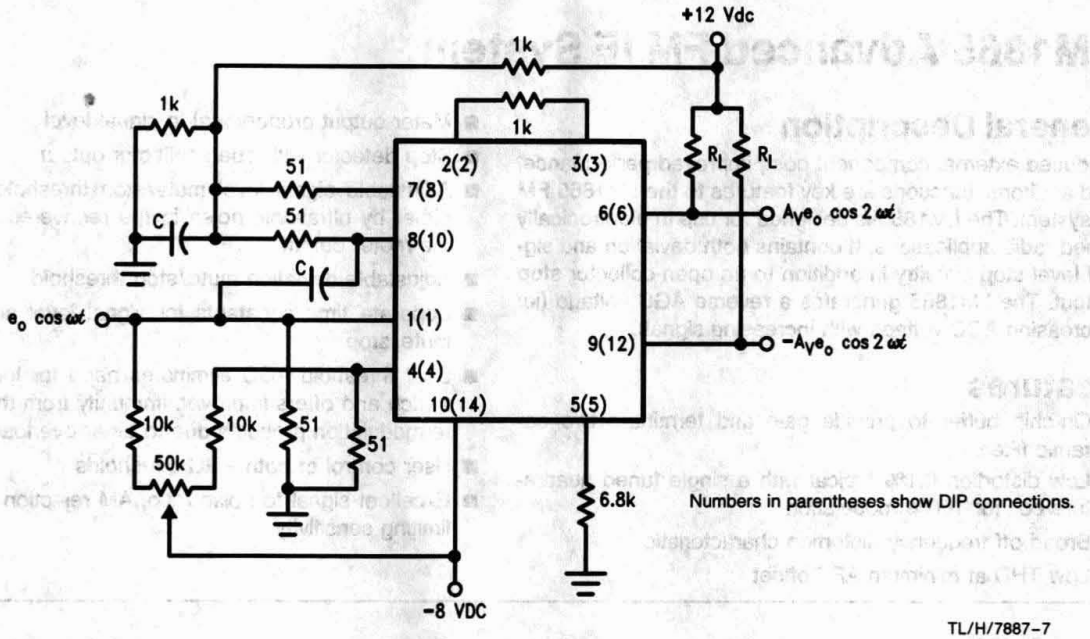


TL/H/7887–7

The frequency doubler circuit shown will double low-level signals with low distortion. The value of C should be chosen for low reactance at the operating frequency. Signal level at the carrier input must be less than 25 mV peak to maintain operation in the linear region of the switching differential amplifier. Levels to 50 mV peak may be used with some distortion of the output waveform. If a larger input signal is available a resistive divider may be used at the carrier input, with full signal applied to the signal input.

Typical Applications (Continued)

Broadband Frequency Doubler



TL/H/7887–7

The frequency doubler circuit shown will double low-level signals with low distortion. The value of C should be chosen for low reactance at the operating frequency. Signal level at the carrier input must be less than 25 mV peak to maintain operation in the linear region of the switching differential amplifier. Levels to 50 mV peak may be used with some distortion of the output waveform. If a larger input signal is available a resistive divider may be used at the carrier input, with full signal applied to the signal input.

National Semiconductor

LM1865 Advanced FM IF System

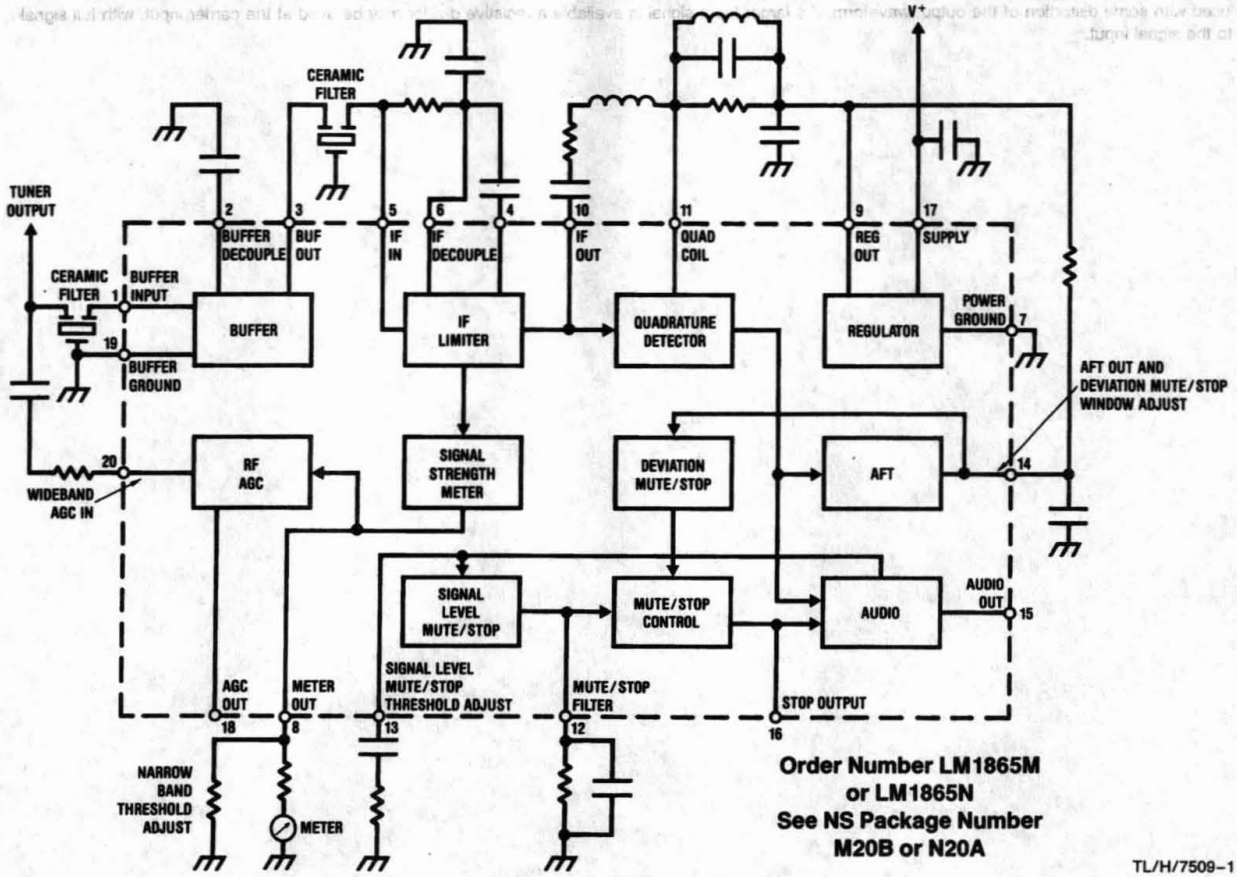
General Description

Reduced external component cost, improved performance, and additonal functions are key features to the LM1865 FM IF system. The LM1865 is designed for use in electronically tuned radio applications. It contains both deviation and signal level stop circuitry in addition to an open-collector stop output. The LM1865 generates a reverse AGC voltage (ie: decreasing AGC voltage with increasing signal).

Features

- On-chip buffer to provide gain and terminate two ceramic filters
- Low distortion 0.1% typical with a single tuned quadrature coil for 100% modulation.
- Broad off frequency distortion characteristic
- Low THD at minimum AFT offset
- Meter output proportional to signal level
- Stop detector with open-collector output
- Adjustable signal level mute/stop threshold, controlled either by ultrasonic noise in the recovered audio or by the meter output
- Adjustable deviation mute/stop threshold
- Separate time constants for signal level and deviation mute/stop
- Dual threshold AGC eliminates need for local/distance switch and offers improved immunity from third order intermodulation products due to tuner overload
- User control of both AGC thresholds
- Excellent signal to noise ratio, AM rejection and system limiting sensitivity

Block Diagram



Order Number LM1865M or LM1865N
See NS Package Number M20B or N20A

TL/H/7509–1

FIGURE 1

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage, Pin 17	16V
Package Dissipation (Note 1)	2.0W
Storage Temperature Range	−55°C to +150°C
Operating Temperature Range	−20°C to +85°C
Max Voltage on Pin 16 (Stop Output)	16V

Soldering Information

Dual-In-Line Package	
Soldering (10 seconds)	260°C
Small Outline Package	
Vapor Phase (60 seconds)	215°C
Infrared (15 seconds)	220°C

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.

Electrical Characteristics

Test Circuit, T_A = 25°C, V^+ = 12V; S1 in position 2; S2 in position 1; and S3 in position 2 unless indicated otherwise

Parameter	Conditions	Min	Typ	Max	Units
STATIC CHARACTERISTICS					
Supply Current			33	45	mA
Pin 9, Regulator Voltage			5.7		V
Operating Voltage Range	(See Note 2)	7.3		16	V
Pin 18, Output Leakage Current	Pin 20 Open, V_{IF} = 0, S3 in Position 1		0.1		μA
Pin 16, Stop Low Output Voltage	S1 in Position 1, S2 in Position 3		0.3		V
Pin 16, Stop High Output Leakage Current	S2 in Position 2, V14 = V9		0.1		μA
Pin 15, Audio Output Resistance			4.7		kΩ
Pin 1, Buffer Input Resistance	Measured at DC		350		Ω
Pin 3, Buffer Output Resistance	Measured at DC		350		Ω
Pin 20, Wide Band Input Resistance	Measured at DC		2		Ω
Pin 8, Meter Output Resistance			1		kΩ
DYNAMIC CHARACTERISTICS f_{MOD} = 400 Hz, f_o = 10.7 MHz, Deviation = ±75 kHz					
−3 dB Limiting Sensitivity	IF Only (See Note 3)		60	120	μVrms
Buffer Voltage Gain	V_{IN} Pin 1 = 10 mVrms at 10.7 MHz	19	22	25	dB
Recovered Audio	V_{IF} = 10 mVrms, V14 = V9	275	320	470	mVrms
Signal-to-Noise	V_{IF} = 10 mVrms, V14 = V9 (See Note 4)	70	84		dB
AM Rejection	V14 = V9				
	V_{IF} = 1 mV, 30% AM Mod	50	60		dB
	V_{IF} = 10 mV, 30% AM Mod	50	60		dB
Minimum Total Harmonic Distortion	V_{IF} = 10 mV		0.1	0.35	%
THD at Frequency where V14 = V9 (Zero AFT Offset)	V_{IF} = 10 mV, Tune until V14 = V9		0.1	0.45	%
THD ± 10 kHz from Frequency where V14 = V9	V_{IF} = 10 mV		0.15		%
AFT Offset Frequency for Low Stop Output at Pin 16	V_{IF} = 10 mV, S2 in Position 3, f_{MOD} = 0 Offset = (Frequency for Pin 16 Low) − (Frequency where V14 = V9)		±50		kHz
Ultrasonic Mute/Stop Level Threshold	V14 = V9, S1 in Position 3 (See Note 5) V_{IF} = 10 mV f_{MOD} = 100 kHz S2 in Position 3 Amount of Deviation where V16 → Low		60		kHz

Electrical Characteristics Test Circuit, $T_A = 25°C$, $V^+ = 12V$; S1 in position 2; S2 in position 1; and S3 in position 2 unless indicated otherwise (Continued)

Parameter	Conditions	Min	Typ	Max	Units
DYNAMIC CHARACTERISTICS $f_{MOD} = 400$ Hz, $f_o = 10.7$ MHz, Deviation $= \pm 75$ kHz (Continued)					
Pin 13 Mute/Stop Threshold Voltage	V14 = V9, S1 in Position 4 S2 in Position 3 V13 where V16 → Low		220		mV
Amount of Muting (LM1965 Only)	S2 in Position 4, S1 in Position 1, $V_{IF} = 10$ mV		66		dB
Amount of Muting with Pin 13 and Pin 16 Grounded	S1 in Position 1 V14, = V9, $V_{IF} = 10$ mV		0		dB
Narrow Band AGC Threshold	Increase IF Input until $I_{AGC} = 0.1$ mA Pin 20 = 30 mVrms	100	210	300	μVrms
Wide Band AGC Threshold	$V_{IF} = 100$ mVrms Increase Signal to Pin 20 until $I_{AGC} = 0.1$ mA	5	12	22	mVrms
Pin 18, Low Output Voltage (LM1865 and LM1965 only)	V_{IN} Pin 20 = 100 mV, $V_{IF} = 100$ mVrms		0.2	0.5	V
Pin 18, High Output Voltage (LM2065 only)	V_{IN} Pin 20 = 100 mV, $V_{IF} = 100$ mVrms, (See Note 6)		11.7		V
Pin 8, Meter Output Voltage	$V_{IF} = 10$ μV $V_{IF} = 300$ μV $V_{IF} = 3$ mV		0.1 1.1 2.6		V V V

Note 1: Above $T_A = 25°C$ derate based on $T_{J(max)} = 150°C$ and $\theta_{JA} = 60°C/W$.

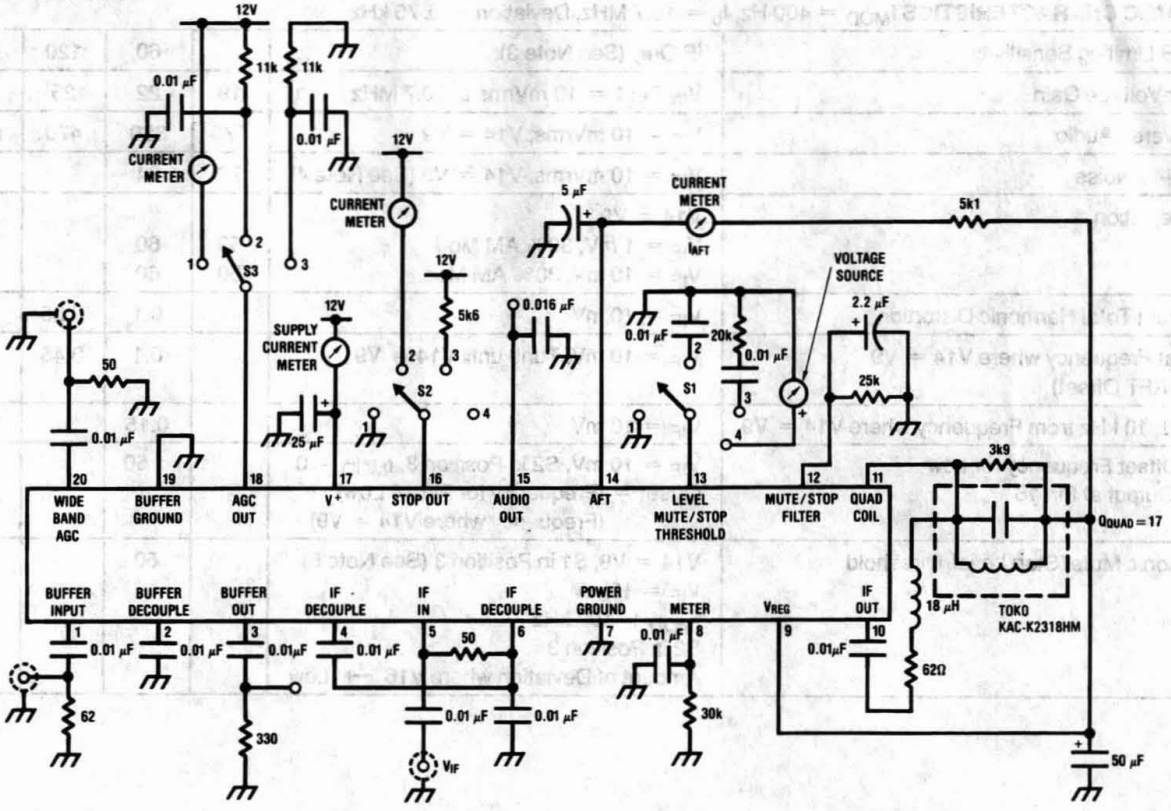
Note 2: All data sheet specifications are for $V^+ = 12V$ may change slightly with supply.

Note 3: When the IF is preceded by 22 dB gain in the buffer, excellent system sensitivity is achieved.

Note 4: Measured with a notch at 60 Hz and 20 Hz to 100 kHz bandwidth.

Note 5: FM modulate RF source with a 100 kHz audio signal and find what modulation level, expressed as kHz deviation, results in V16 → 12V.

Test Circuit

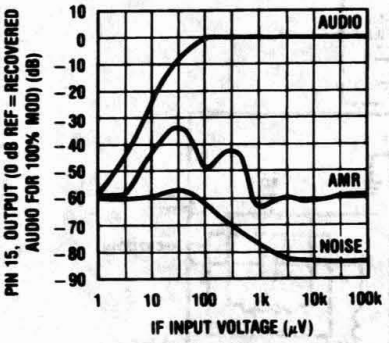


TL/H/7509–2

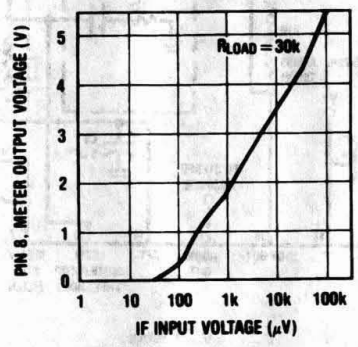
FIGURE 2

Typical Performance Characteristics (from Test Circuit)

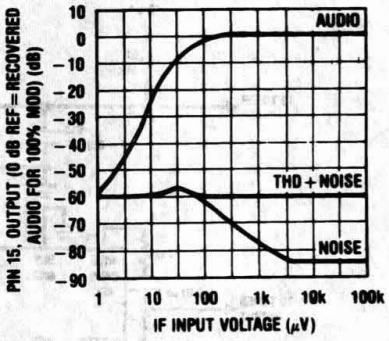
FM Limiting Characteristics and AM Rejection



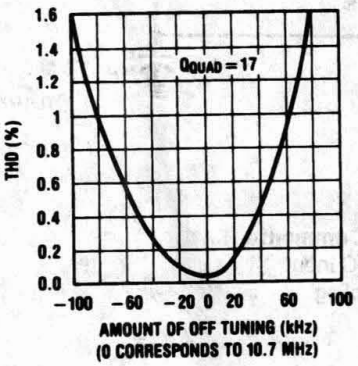
Pin 8, Meter Output Voltage vs IF Input Level



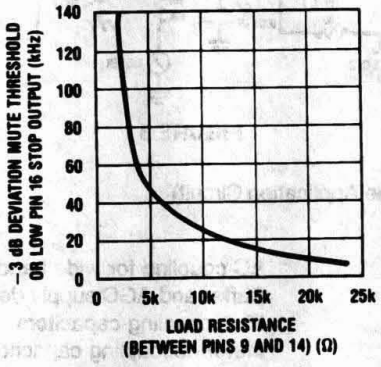
FM Limiting Characteristics + THD



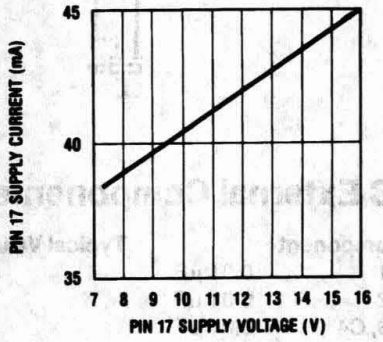
% THD vs OFF Tuning (Single Tuned Quadrature Coil)



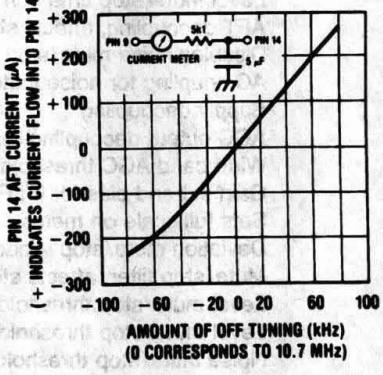
Deviation Mute/Stop Threshold as a Function of AFT Load Resistor



Supply Current vs Supply Voltage



Pin 14, AFT Current vs Tuning

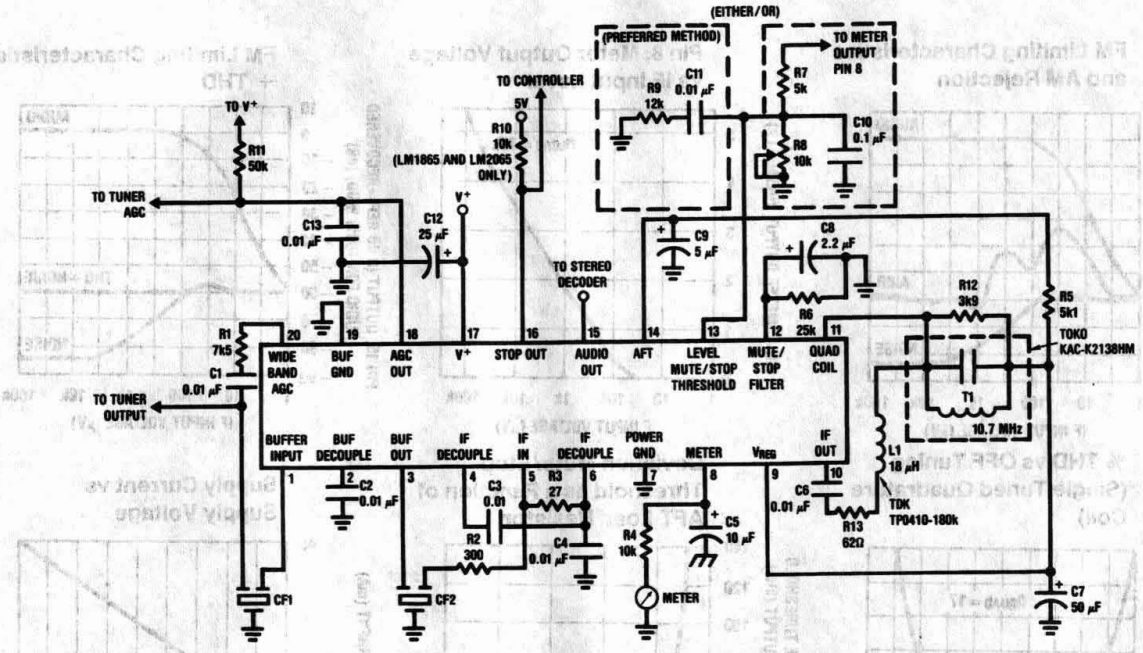


TL/H/7509–3

Coils and ceramic filters are available from:

Toko America	Murata
1250 Feehanville Drive	2200 Lake Park Drive
Mount Prospect, IL 60056	Smyrna, GA 30080
(312) 297-0070	(404) 436-1300

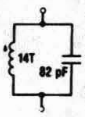
Application Circuit



TL/H/7509–4

FIGURE 3

IC External Components (See Application Circuit)

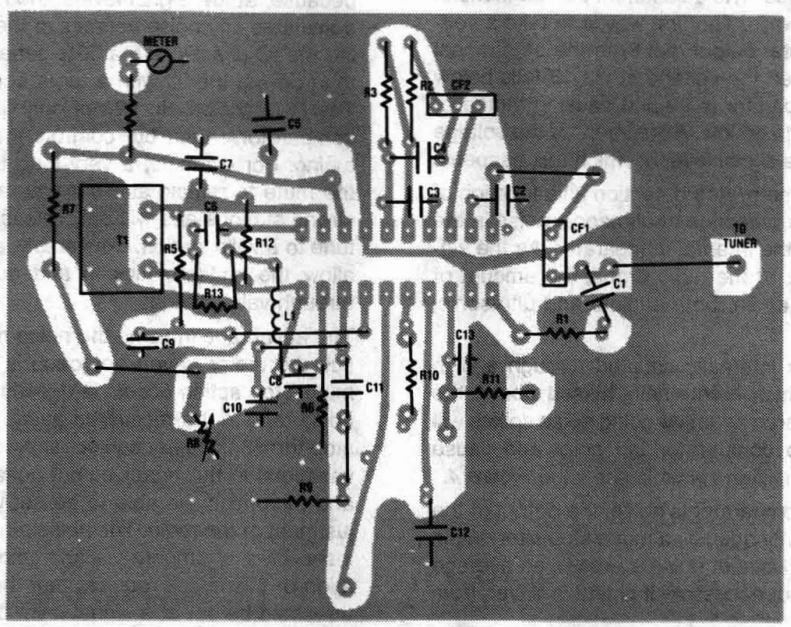
Component	Typical Value	Comments
C1	0.01 µF	AC coupling for wide band AGC input
C2	0.01 µF	Buffer and AGC supply decoupling
C3, C4	0.01 µF	IF decoupling capacitors
C5	10 µF	Meter decoupling capacitor
C6	0.01 µF	AC coupling for IF output
C7	50 µF	Regulator decoupling capacitor, affects S/N floor
C8	2.2 µF	Level mute/stop time constant
C9	5 µF	AFT decoupling, affects stop time
C10	0.1 µF	Disables noise mute/stop
C11	0.01 µF	AC coupling for noise mute/stop threshold adjust
C12	25 µF	Supply decoupling
C13	0.01 µF	AGC output decoupling capacitor
R1	Tuner Dependent	Wide band AGC threshold adjust
R2, R3	Tuner Dependent	Gain set and bias for IF; R2 + R3 = 330Ω to terminate ceramic filter
R4	Meter Dependent	Sets full-scale on meter
R5	5k1	Deviation mute/stop window adjustment
R6	25k	Mute/stop filter, affects stop time
R7	5k	Level mute/stop threshold adjustment
R8	10k Pot	Level mute/stop threshold adjustment
R9	12k	Noise mute/stop threshold adjustment, decrease resistor for lower S/N at threshold, for optimum performance over temp. and gain variation, set this resistor value so that the signal level mute/stop threshold occurs in the radio at 45dB S/N (±3 dB) in mono.
R10	10k	Load for open-collector stop output
R11	50k	AGC output load resistor for open-collector output
R12	3k9	Sets Q of quadrature coil affecting THD, S/N and recovered audio
R13	62Ω	Optimises minimum THD
L1	18 µH Q_u > 50 @ 10.7 MHz TDK Electronics TPO410-180K or equivalent	Sets signal swing across quadrature coil, High Q is important to minimize effect variation of Q has on both minimum THD and AFT offset.
T1	 TL/H/7509–5 Q_u > 70 @ 10.7 MHz, L to resonate w/82 pF @ 10.7 MHz TOKO KAC-K2318HM or equivalent	10.7 MHz quadrature coil: Q_{UL} > 70
CF1, CF2	Murata SFE10.7ML or equivalent	10.7 MHz ceramic resonators provide selectivity; good group delay characteristics important for low THD of system

Typical Application

LAYOUT CONSIDERATIONS

Although the pinout of the LM1865 has been chosen to minimize layout problems, some care is required to insure stability. The ground terminal on CF1 should return to both the input signal ground and the buffer ground, pin 19. The ground terminal on CF2 should return to the ground side of C4. The quadrature coil T1 and inductor L1 should be separated from the input circuitry as far as possible.

PC Layout (Component Side)

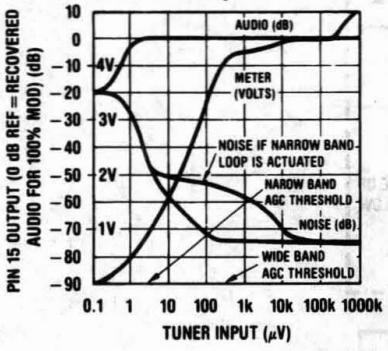


TL/H/7509–6

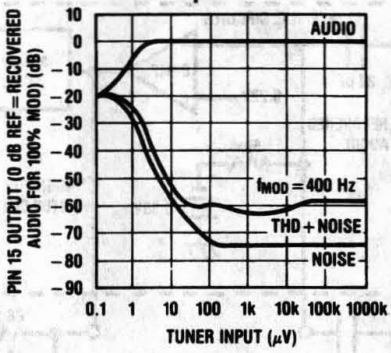
PERFORMANCE CHARACTERISTICS OF TYPICAL APPLICATION WITH TUNER

The following data was taken using the typical application circuit in conjunction with an FM tuner with 43 dB of gain, a 5.5 dB noise figure, and 30 dB of AGC range. The tuner was driven from a 50Ω source. 75 μs of de-emphasis was used on the audio output, pin 15. The 0 dB reference is for ±75 kHz deviation at 400 Hz modulation.

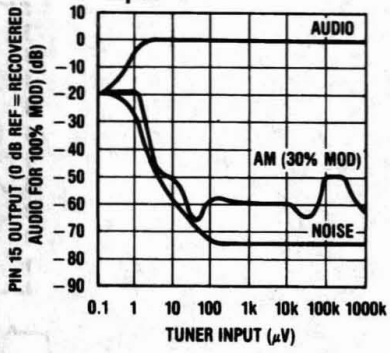
Meter Output and Signal-to-Noise vs Tuner Input



Total Harmonic Distortion vs Tuner Input



AM Rejection vs Tuner Input



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−3 dB limiting = 0.9 μV

30 dB quieting = 1.4 μV

Level stop/mute threshold = 1.4 μV

Deviation mute window (−3 dB) = ±45 kHz

Application Notes

ADJUSTABLE MUTE/STOP THRESHOLD

The threshold adjustments for the mute and stop functions are controlled by the same pins. Thus, the term mute/stop will be used to designate either function.

The adjustable mute/stop threshold in the LM1865 allows for user programming of the signal level at which muting or stop indication takes place. The adjustment can be made in two mutually exclusive ways. The first way is to take a voltage divider from the meter output (pin 8) to the off channel mute input (pin 13). When the voltage at pin 13 falls below 0.22V, an internal comparator is tripped causing muted or causing the stop output to go low. Adjustment of the voltage divider ratio changes the signal level at which this happens.

The second method of mute/stop detection as a function of signal level is to use the presence of ultrasonic noise in the recovered audio to trip the internal comparator. As the signal level at the antenna of the radio drops, the amount of noise in the recovered audio, both audible and ultrasonic, increases.

The recovered audio is internally coupled through a high pass filter to pin 13 which is internally biased above the comparator trip point. Large negative-going noise spikes will drive pin 13 below the comparator trip point and cause mute/stop action. A simplified circuit is shown in *Figure 4*.

Since the input to the comparator is noise, the output of the comparator is noise. Consequently, a mute/stop filter on pin 12 is required to convert output noise spikes to an average DC value. This filter is not necessary if pin 13 is driven from the meter.

Adjustment of the mute/stop threshold in the noise mode is accomplished by adjusting the pole of the high pass filter coupled to the comparator input. This is done with a series capacitor/resistor combination, R9 C11, from pin 13 to ground. As the pole is moved higher in frequency (i.e., R9 gets smaller) more ultrasonic noise is required in the recovered audio in order to initiate mute/stop action. This corresponds to a weaker signal at the antenna of the radio. In choosing the correct value for R9 it is important to make sure that recovered audio below 75 kHz is not sufficient to cause mute/stop action. This is because stereo and SCA information are contained in the audio signal up to 75 kHz. Also note that the ultrasonic mute/stop circuit will not operate properly unless a tuner is connected to the IF. This is because, at low signal levels, the noise at the tuner output dominates any noise sources in the IC. Consequently, driving the IC directly with a 50Ω generator is much less noisy than driving the IC with a tuner and therefore not realistic. The RC filter on pin 12 not only filters out noise from the comparator output but controls the "feel" when manually tuning. For example, a very long time constant will cause the mute to remain active if you rapidly tune through valid strong stations and will only release the mute if you slowly tune to a valid station. Conversely, a short time constant will allow the mute to kick in and out as one tunes rapidly through valid stations.

The advantage in using the noise mute/stop approach versus the meter driven approach is that the point at which mute/stop action occurs is directly related to the signal-to-noise ratio in the recovered audio. Furthermore, the mute/stop threshold is not subject to production and temperature variations in the meter output voltage at low signal levels, and thus might be able to be set without a production adjustment of the radio. The noise mute/stop threshold is very insensitive to temperature and gain variations. Proper operation of this circuit requires that the signal level mute/stop threshold be set at a signal level that achieves 45 dB S/N (±3 dB) in mono. in a radio. In an electronically tuned radio, the signal level stop threshold can be set to a much larger level by gain reducing the tuner (ie. pulling the AGC line) in scan mode and then releasing the AGC once the radio stops on a station. In an environment where temperature variations are minimal and manual adjustment of the signal level mute/stop threshold is desired, then the meter driven approach is the best alternative.

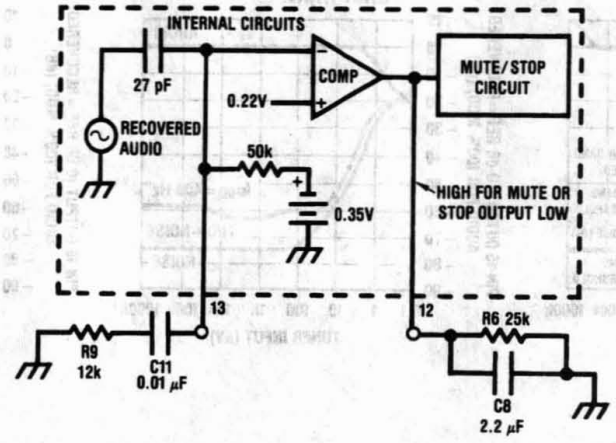

FIGURE 4. Simplified Level Mute/Stop Circuit

Application Notes (Continued)

STOP TIME

An electronically tuned radio (ETR) pauses at fixed intervals across the FM band and awaits the stop indication from the LM1865. If within a predetermined period of time, no stop indication is forthcoming, the controller circuit concludes that there is no valid station at that frequency and will tune to the next interval. There are several time constants that can affect the amount of time it takes the LM1865 to output a valid stop indication on pin 16. In this section each time constant will be discussed.

Deviation Stop Time Constant

An offset voltage is generated by the AFT if the LM1865 is tuned to either side of a station. Since deviation stop detection in the LM1865 is detected by the voltage at pin 14, it is important that this voltage move fast enough to make the deviation stop decision within the time allowed by the controller. The speed at which the voltage at pin 14 moves is governed by the RC time constant, R5 C9. This time constant must be chosen long enough to remove recovered audio from pin 14 and short enough to allow for reasonable stop detection time.

Signal Level Stop Using Ultrasonic Noise Detection

As previously mentioned, the R6 C8 time constant on pin 12 is necessary to filter the noise spikes on the output of the internal comparator in the LM1865. This time constant also determines the level stop time. When the voltage at pin 12 is above a threshold voltage of about 0.6V, the stop output is low. The maximum voltage at pin 12 is about 0.8V. The level stop time is dominated by the amount of time it takes the voltage at pin 12 to fall from 0.8V to 0.6V. The voltage at pin 12 follows an exponential decay with RC time constant given by R6 C8. For example if R6 = 25k and C8 = 2.2 μF the stop time is given by

$$t = -(24k)\,(2.2\ \mu F)\ \ell n\left(\frac{0.6}{0.8}\right)$$

which yields t = 15 ms. It should be noted that the 0.6V threshold at pin 12 has a high temperature dependence and can move as much as 100 mV in either direction.

Signal Level Stop Using the Meter Output, Pin 8

As mentioned previously, R6 C8 is not necessary when the meter output is used to drive pin 13. Consequently, this time constant is not a factor in determining the stop time. However, the speed at which the meter voltage can move may become important in this regard. This speed is a function of the resistive load on pin 8 and filter capacitance, C5.

AGC Time Constant

In tuning from a strong station to a weaker station above the level stop threshold, the AGC voltage will move in order to try to maintain a constant tuner output. The AGC voltage must move sufficiently fast so that the tuner is gain increased to the point that the level stop indicates a valid station. This time constant is controlled by R11 and C13.

DISTORTION COMPENSATION CIRCUIT

The quadrature detector of the LM1865 has been designed with a special circuit that compensates for distortion generated by the non-linear phase characteristic of the quadrature coil. This circuit not only has the effect of reducing distortion, but also desensitizes the distortion as a function of tuning characteristic. As a result, low distortion is achieved with a single tuned quad coil without the need for a double tuned coil which is costly and difficult to adjust on a production basis. The lower distortion has been achieved without any degradation of the noise floor of the audio output. Futhermore, the compensation circuit first-order cancels the effect of quadrature coil Q on distortion.

When measuring the total harmonic distortion (THD) of the LM1865, it is imperative that a low distortion RF generator be used. In the past it has been possible to cancel out distortion in the generator by adjustment of the quadrature coil. This is because centering the quadrature coil at other than the point of inflection on the S-curve introduces 2nd harmonic distortion which can cancel 2nd harmonic distortion in the generator. Thus low THD numbers may have been obtained wrongly. Large AFT offsets asymmetrical off tuning characteristic, and less than minimum THD will be observed if alignment of the quadrature coil is done with a high distortion RF generator.

Care must also be taken in choosing ceramic filters for the LM1865. It is important to use filters with good group delay characteristics and wide enough bandwidth to pass enough FM sidebands to achieve low distortion.

Application Notes (Continued)

The LM1865 has been carefully designed to insure low AFT offset current at the point of minimum THD. AFT offset current will cause a non-symmetric deviation mute/stop window about the point of minimum THD. No external AFT offset adjustment should be necessary with the LM1865. The amount of resistance in series with the 18 μH quadrature coil drive inductor, L1, has a significant effect on the minimum THD. This series resistance is contributed not only by R13 but also by the Q of L1. The Q of L1 should be as high as possible (ie: Q>50) in order to avoid production problems with the Q variation of L1. Once R13 has been optimized for minimum THD, adjustment on a radio by radio basis should be un-necessary.

DUAL THRESHOLD AGC (AUTOMATIC LOCAL/DISTANCE SWITCH)

There is a well recognized need in the field for gain reducing (AGCing) the front end (tuner) of an FM receiver. This gain reduction is important in preventing overload of the front end which might occur for large signal inputs. Overloading the front end with two out-of-band signals, one channel spacing apart and one channel spacing from center frequency, or, two channel spacings apart and two channel spacings from center frequency, will produce a third order intermodulation product (IM_3) which falls inband. This IM_3 product can completely block out a weaker desired station. The AGC in the LM1865 has been specially designed to deal with the problem of IM_3.

With the LM1865 system, a low AGC threshold is achieved whenever there are strong out-of-band signals that might generate an interfering IM_3 product, and a high AGC threshold is achieved if there are no strong out-of-band signals. The high AGC threshold allows the receiver to obtain its best signal-to-noise performance when there is no possibility of an IM_3 product. The low AGC threshold allows for weaker desired stations to be received without gain-reducing the tuner. It should be noted that when the AGC threshold is set low, there will be a signal-to-noise compromise, but is assumed that it is more desirable to listen to a slightly noisy station than to listen to an undesired IM_3 product. The simplified circuit diagram (*Figure 5*) of the AGC system shows how the dual AGC thresholds are achieved.

V_m = 1V corresponds to a fixed in-band signal level (defined as V_{NB}) at the tuner output. V_{NB} will be referred to as the "narrow band threshold". V_{WB} also corresponds to a fixed tuner output which can either be an in-band or out-of-band signal. This fixed tuner output will be called the "wide band threshold". Always $V_{WB} > V_{NB}$. R11 and C13 define the AGC time constant. A reverse AGC system is shown. This means that V_{AGC} decreases to gain-reduce the tuner. The LM1865 AGC output is an open-collector current source capable of sinking at least 1 mA.

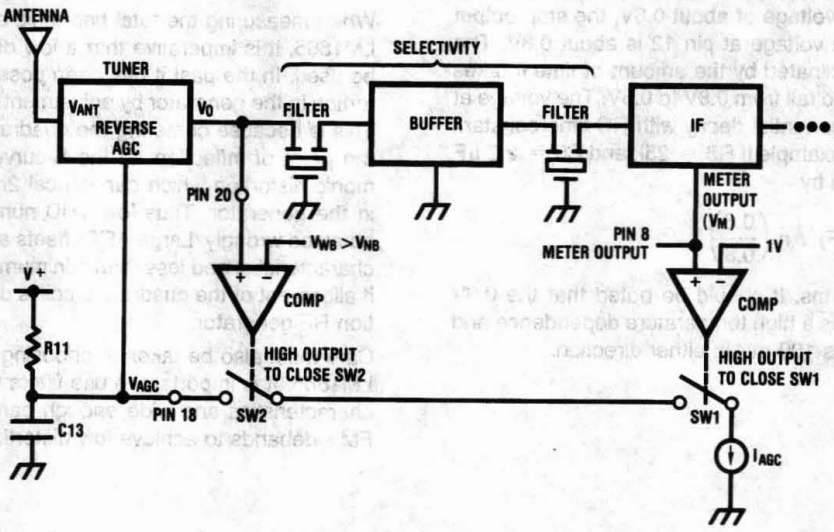

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FIGURE 5. Dual Threshold AGC

$I_1 = GM_1 V_m$ only if $V_m > 1V$
otherwise $I_1 = 0$

Gm_1, V_{WB} = constants

$I_{AGC} = Gm_2 V_o$ where $Gm_2 = I_1/26$ mV *and*
$V_o > V_{WB}$ otherwise $I_{AGC} = 0$

Application Notes (Continued)

First examine what happens with a single in-band signal as we vary the strength of this signal. *Figures 6 and 7* illustrate what happens at the tuner and AGC outputs.

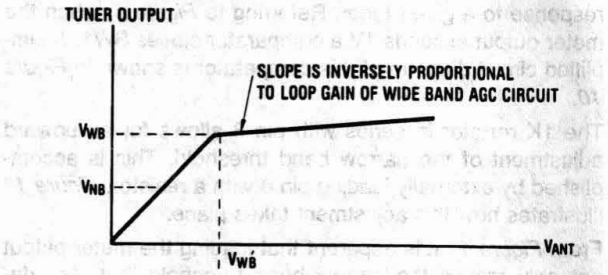

FIGURE 6

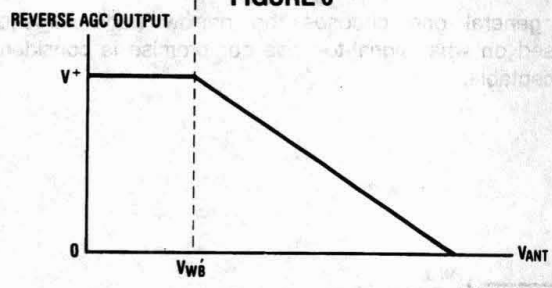

FIGURE 7

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In *Figure 7* there is no AGC output until the tuner output equals the wide band threshold. At this point both SW2 and SW1 are closed and the AGC holds the tuner output in *Figure 6* relatively constant.

Another simple case to examine is that of the single out-of-band signal. Here there is no AGC output even if the signal exceeds V_{WB}. There is no output because the ceramic filters prevent the out-of-band signal from getting to the input of the IF. With no signal at the IF input there is no meter output and SW1 is open, which means No AGC.

Figures 8 and 9 illustrate what happens at the tuner and AGC outputs when the strength of an in-band signal is varied in the presence of a strong out-of-band signal (i.e., greater than V_{WB}) which is held constant at the tuner input. For this example, the in-band signal at the tuner output will be referred to as V_D (desired signal), and the out-of-band signal as V_{UD} (undesired signal).

In *Figure 9*, we see that there is no AGC output until the tuner output exceeds the narrow band threshold, V_{NB}. At this point $V_m > 1V$ and SW1 closes. Further increase of the desired signal at the tuner input results in an AGC current that tries to hold the desired signal at the tuner output constant. This gain reduction of the tuner forces the undesired signal at the tuner output to fall. At the point that V_{UD} reaches the wide band threshold, no further gain reduction can occur as V_o would fall below V_{WB} (refer to *Figure 5*). At this point, control of the AGC shifts from the meter output (narrow band loop) to the out-of-band signal (wide band loop). Here V_{UD} is held constant along with the AGC

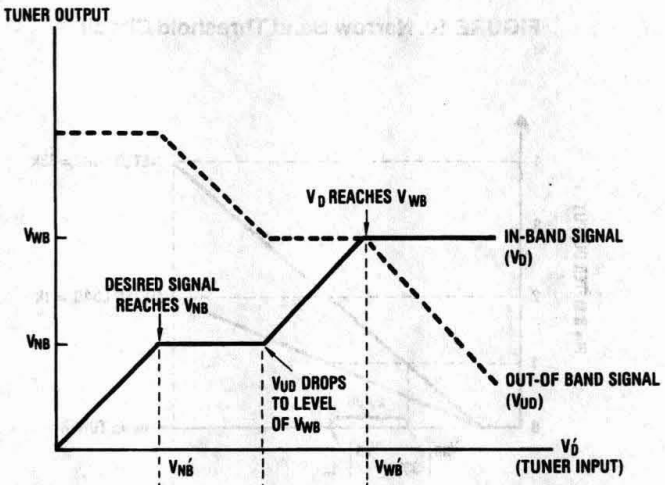
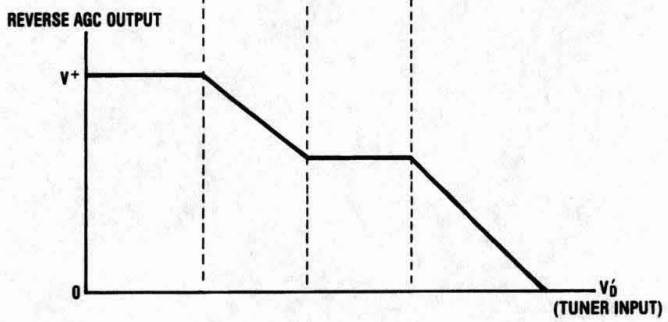


FIGURE 8



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Prime indicates referenced to tuner input

FIGURE 9

Application Notes (Continued)

voltage, while V_D is allowed to increase. V_D will increase until it reaches the level of the wide band threshold at the tuner output. When this occurs V_{UD} is no longer needed to keep $V_o > V_{WB}$ as V_D takes over the job. Thus V_{UD} will drop as the amount of AGC increases, while V_D is held constant by the AGC.

When compared to the simple case of a single in-band signal, we see that because of the presence of a strong out-of-band signal, AGC action has occurred earlier. For the simple case, AGC started when $V_D \geq V_{WB}$. For the two signal case above, AGC started when $V_D \geq V_{NB}$. Thus, the LM1865 achieves an early AGC when there are strong adjacent channels that might cause IM_3, and a later AGC when these signals aren't present.

For the range of signal levels that the tuner was gain-reduced and $V_D < V_{WB}$ there was loss in signal-to-noise in the recovered audio as compared to the case where there was no gain reduction in this interval. *Note, however, that the tuner is not desensitized by the AGC to weak desired stations below the narrow band threshold.*

NARROW BAND AGC THRESHOLD ADJUSTMENT

Both the narrow band and wide band AGC thresholds are user adjustable. This allows the user to optimize the AGC response to a given tuner. Referring to *Figure 5*, when the meter output exceeds 1V a comparator closes SW1. A simplified circuit diagram of this comparator is shown in *Figure 10*.

The 1K resistor in series with pin 8 allows for an upward adjustment of the narrow band threshold. This is accomplished by externally loading pin 8 with a resistor. *Figure 11* illustrates how this adjustment takes place.

From *Figure 11* it is apparent that loading the meter output not only moves the narrow band threshold, but also decreases the meter output for a given input.

In general one chooses the narrow band threshold based on what signal-to-noise compromise is considered acceptable.

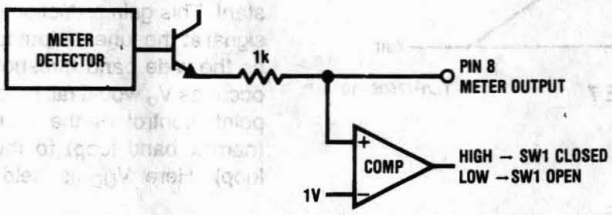

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FIGURE 10. Narrow Band Threshold Circuit

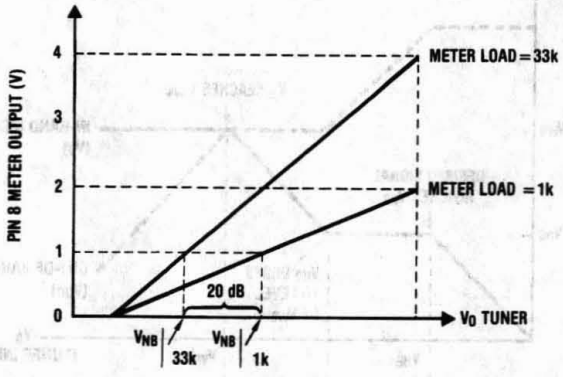

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FIGURE 11. Affect of Meter Load on Narrow Band Threshold

Application Notes (Continued)

WIDE BAND AGC THRESHOLD ADJUSTMENT

There are a number of criteria that determine where the wide band threshold should be set. If the threshold is set too high, protection against IM_3 will be lost. If the threshold is set too low, the front end, under certain input conditions, may be needlessly gain-reduced, sacrificing signal-to-noise performance. Ideally, the wide band threshold should be set to a level that will insure AGC operation whenever there are out-of-band signals strong enough to generate an IM_3 product of sufficient magnitude to exceed the narrow band threshold. Ideally, this level should be high enough to allow for a single in-band desired station to AGC the tuner, only after the maximum signal-to-noise has been achieved.

In order to insure that the wide band loop is activated whenever the IM_3 exceeds the narrow band threshold, V_{NB}, determine the minimum signal levels for two out-of-band signals necessary to produce an IM_3 equal to V_{NB}. Then, arrange for the wide band loop to be activated whenever the tuner output exceeds the rms sum of these signals. There are many combinations of two out-of-band signals that will produce an IM_3 of a given level. However, there is only one combination whose rms sum is a minimum at the tuner output. IM_3 at the tuner output is given according to the equation:

$$IM_3 = aV_{UD1}{}^2 V_{UD2} \text{ (assuming no gain reduction)} \quad (1)$$

where a = constant dependent on the tuner;

V_{UD1} = out-of-band signal 400 kHz from center frequency, applied to tuner input;

V_{UD2} = out-of-band signal 800 kHz from center frequency and 400 kHz away from V_{UD1}, applied to tuner input.

In general, due to tuned circuits within the tuner, the tuner gain is not constant with frequency. Thus, if the tuner is kept fixed at one frequency while the input frequency is changed, the output level will not remain constant. *Figure 12* illustrates this.

It can be shown that for a given IM_3, the combination of V_{UD1} and V_{UD2} that produces the smallest rms sum at the tuner output is given by the equations:

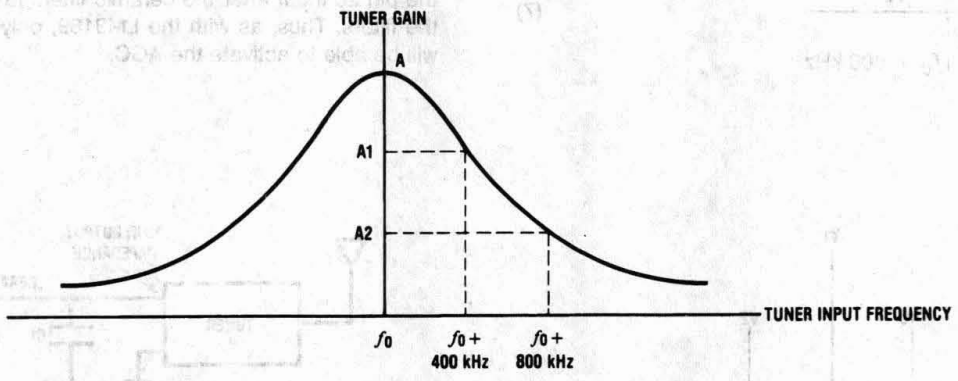
$$V_{UD1} = 1.12\left(\frac{A2}{A1}\frac{IM_3}{a}\right)^{1/3} \quad (2)$$

$$V_{UD2} = 0.794\left(\frac{A1^2}{A2^2}\frac{IM_3}{a}\right)^{1/3} \quad (3)$$

Therefore, in order to guarantee that the AGC will be keyed for an $IM_3 = V_{NB}$ we need only satisfy the condition:

$$V_{WB} \leq \sqrt{V_{NB}^2 + \left[(A1)(1.12)\left(\frac{A2}{A1}\frac{V_{NB}}{a}\right)^{1/3}\right]^2 + \left[A2(0.794)\left(\frac{A1^2}{A2^2}\frac{V_{NB}}{a}\right)^{1/3}\right]^2} \quad (4)$$

The right hand term of equation (4) defines an upper limit for V_{WB} called V_{WBUL}. V_{WBUL} is the rms sum of all the signals at the tuner output for two out-of-band signals, V_{UD1} and V_{UD2} [as expressed in equations (2) and (3)], applied to the tuner input.



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Define A = tuner gain at center frequency
A1 = tuner gain at f_0 + 400 kHz
A2 = tuner gain at f_0 + 800 kHz

FIGURE 12

Application Notes (Continued)

In order to make the calculation in equation (4), the constants a, A1, A2 must first be determined. This is done by the following procedure:

1. Connect together two RF generators and apply them to the tuner input. Since the generators will terminate each other, remove the 50Ω termination at the tuner input.
2. Connect a spectrum analyzer to the tuner output. Most spectrum analyzers have 50Ω input impedances. To make sure that this impedance does not load the tuner output use a FET probe connected to the spectrum analyzer. The tuner output should be terminated with a ceramic filter.
3. Disconnect the AGC line to the tuner. Make sure that the tuner is not gain-reduced.
4. Adjust the two RF generators for about 1 mV input and to frequencies 400 kHz and 800 kHz away from center frequency (*Figure 13*).
5. Note the three output levels in volts.
6. Knowing the tuner input levels for V_{UD1} and V_{UD2} and the resulting IM_3 just measured, "a" is calculated from the formula:

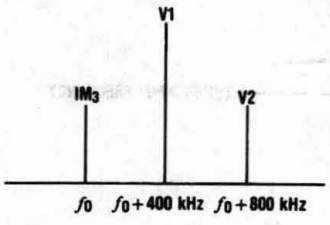
$$a = \frac{IM_3}{V_{UD1}{}^2\, V_{UD2}} \quad (5)$$

where all levels are in volts rms. A typical value for "a" might be 2×10^6.

7. A1 and A2 are calculated according to the following formulas

$$A1 = \frac{V1}{V_{IN}\Big|_{f_o + 400\ kHz}} \quad (6)$$

$$A2 = \frac{V2}{V_{IN}\Big|_{f_o + 800\ kHz}} \quad (7)$$



$f_o = 10.7$ MHz

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FIGURE 13. Spectrum Analyzer Display of Tuner Output

If the wide band threshold was set to V_{WBUL}, then when a single in-band station reached the level V_{WBUL} at the tuner output, AGC action would start to take place. For this reason it is hoped that V_{WBUL} is above the level that will allow for maximum signal-to-noise. If, however, this is not the case, consideration might be given to improving the intermodulation performance of the tuner.

The lower limit for V_{WB} is the minimum tuner output that achieves the best possible signal-to-noise ratio in the recovered audio. In general, it is desirable to set V_{WB} closer to the upper limit rather than the lower limit. This is done to prevent AGC action within the narrow band loop except when there is a possibility of an IM_3 greater than V_{NB}.

The wide band threshold at the pin 20 input to the LM1865 is fixed at 12 mVrms. Generally speaking, if pin 20 were driven directly from the tuner output. V_{WB} would be too low. Therefore, in general, pin 20 is not connected directly to the tuner output. Instead the tuner output is attenuated and then applied to pin 20. Increasing attenuation increases the wide band threshold, V_{WB}.

Pin 20 has an input impedance at 10.7 MHz that can be modeled as a 500Ω resistor in series with a 19 pF capacitor, giving a total impedance of $940\Omega \angle -58°$. Thus an easy way to attenuate the input to pin 20 is with the arrangement shown in *Figure 14*.

Notice that pin 20 must be AC coupled to the tuner output and that C1 is a bypass capacitor. R1 adjusts the amount of attenuation to pin 20. The wide band threshold will roughly increase by a factor of (R1 + 940Ω)/940Ω.

AGC CIRCUIT USED AS A CONVENTIONAL AGC

If for some reason the dual AGC thresholds are not desired, it is easy to use the LM1865 as a more conventional LM3189 type of AGC. This is accomplished by AC coupling the pin 20 input after the ceramic filters rather than before the filters. Thus, as with the LM3189, only in-band signals will be able to activate the AGC.

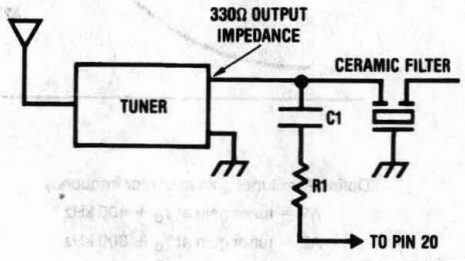

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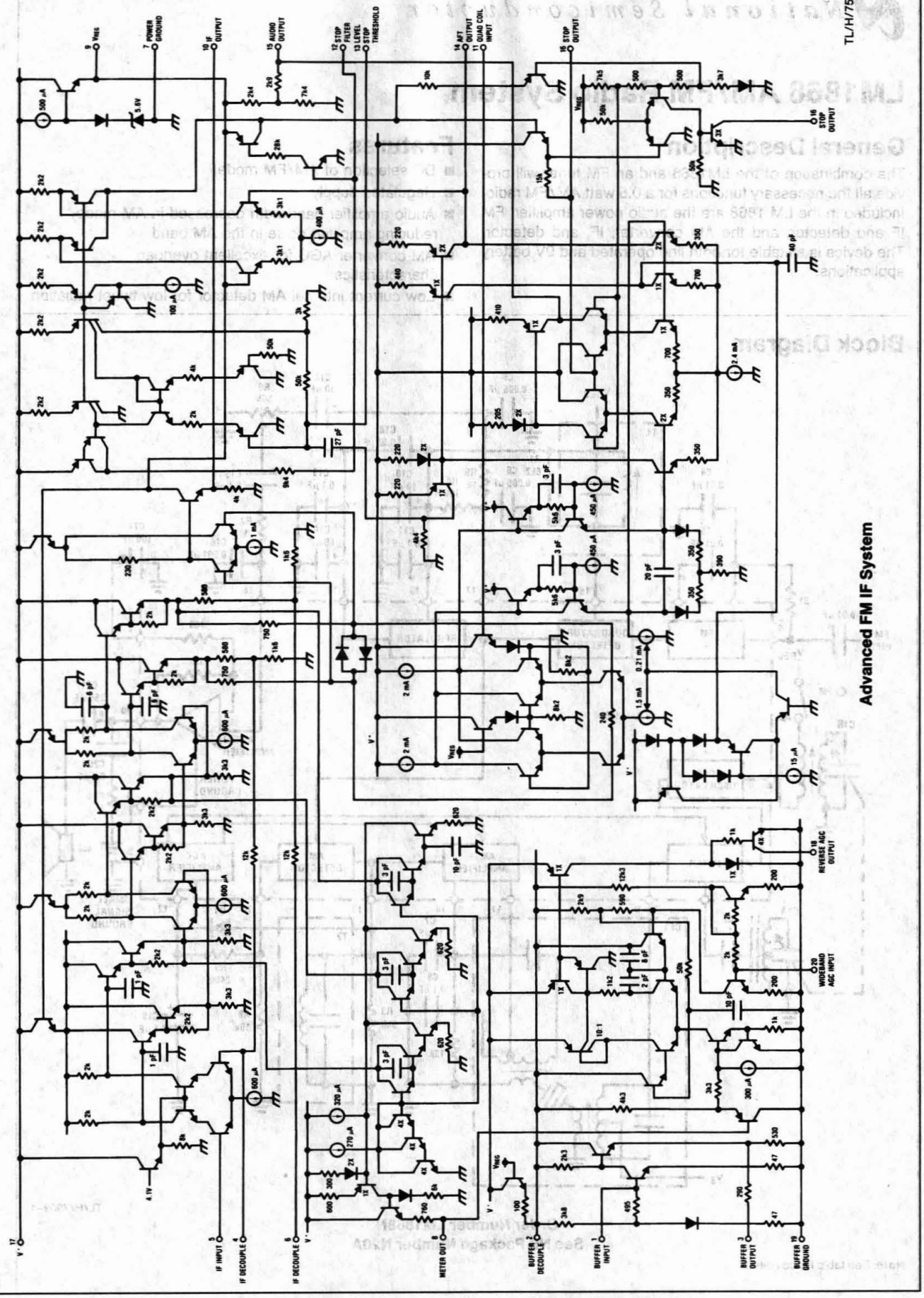
FIGURE 14. Wide Band Threshold Adjustment

Simplified Diagram



National Semiconductor

LM1868 AM/FM Radio System

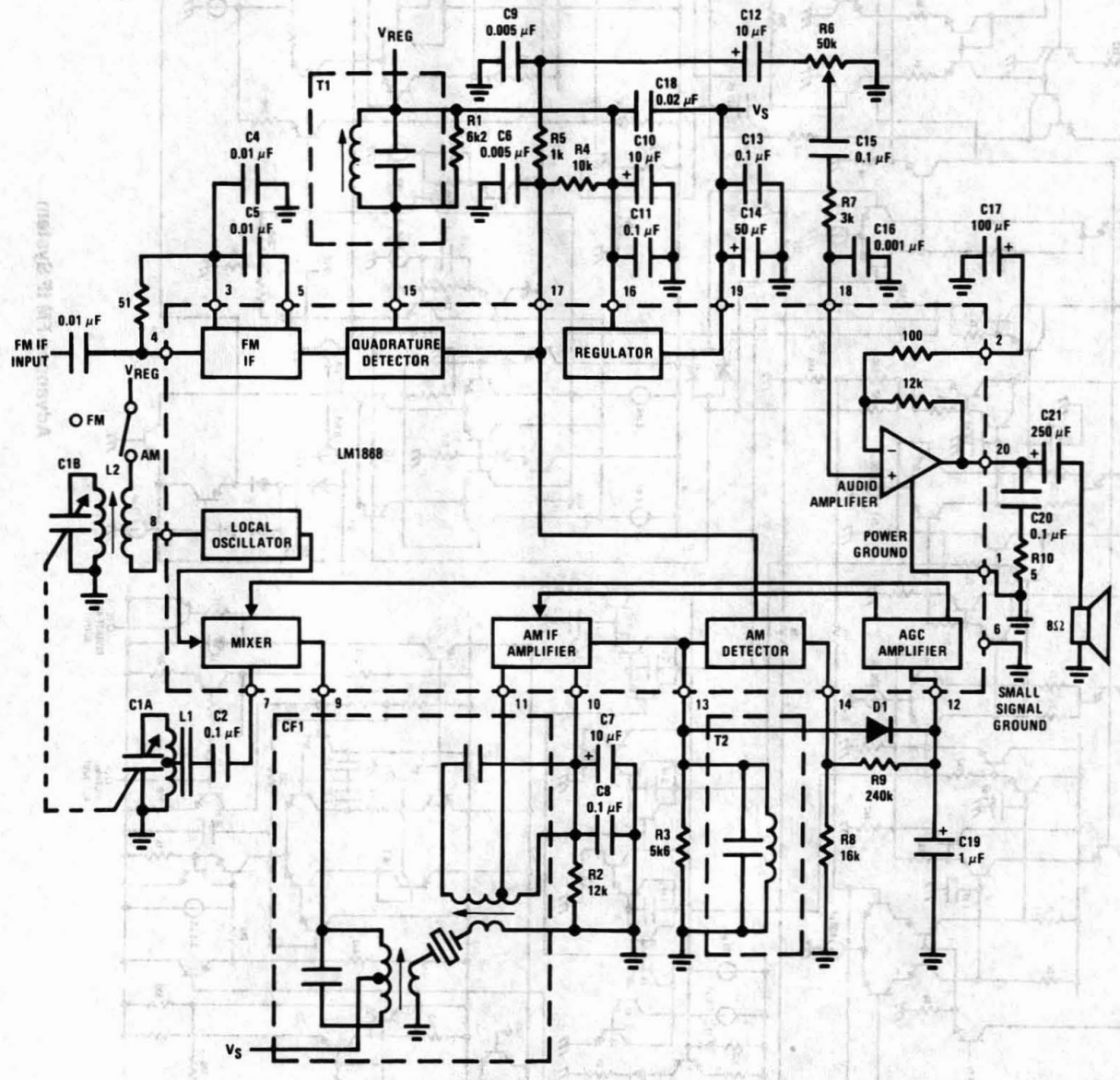
General Description

The combination of the LM1868 and an FM tuner will provide all the necessary functions for a 0.5 watt AM/FM radio. Included in the LM 1868 are the audio power amplifier, FM IF and detector, and the AM converter, IF, and detector. The device is suitable for both line operated and 9V battery applications.

Features

- DC selection of AM/FM mode
- Regulated supply
- Audio amplifier bandwidth decreased in AM mode, reducing amplifier noise in the AM band
- AM converter AGC for excellent overload characteristics
- Low current internal AM detector for low tweet radiation

Block Diagram



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Order Number LM1868N
See NS Package Number N20A

Note: See table for coil data

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (Pin 19)	15V
Package Dissipation	2.0W
Above T_A = 25°C, Derate Based on $T_{J(MAX)}$ = 150°C and θ_{JA} = 60°C/W	
Storage Temperature Range	−55°C to +150°C
Operating Temperature Range	0°C to +70°C
Lead Temperature (Soldering, 10 sec.)	260°C

Electrical Characteristics

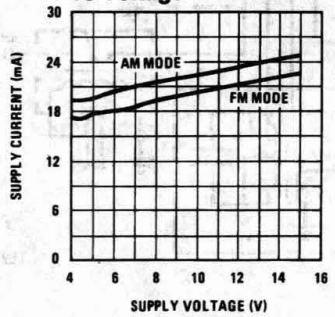
Test Circuit, T_A = 25°C, V_S = 9V, R_L = 8Ω (unless otherwise noted)

Parameter	Conditions	Min	Typ	Max	Units
STATIC CHARACTERISTICS e_{AM} = 0, e_{FM} = 0					
Supply Current	AM Mode, S1 in Position 1		22	30	mA
Regulator Output Voltage (Pin 16)		3.5	3.9	4.8	V
Operating Voltage Range		4.5		15	
DYNAMIC CHARACTERISTICS—AM MODE f_{AM} = 1 MHz, f_{mod} = 1 kHz, 30% Modulation, S1 in Position 1, P_O = 50 mW unless noted					
Maximum Sensitivity	Measure e_{AM} for P_O = 50 mW, Maximum Volume	8		16	μV
Signal-to-Noise	e_{AM} = 10 mV	40	50		dB
Detector Output	e_{AM} = 1 mV Measure at Top of Volume Control	40	60	85	mV
Overload Distortion	e_{AM} = 50 mV, 80% Modulation		2	10	%
Total Harmonic Distortion (THD)	e_{AM} = 10 mV		1.1	2	%
DYNAMIC CHARACTERISTICS—FM MODE f_{FM} = 10.7 MHz, f_{mod} = 400 Hz, Δf = ±75 kHz, P_O = 50 mW, S1 in Position 1					
−3 dB Limiting Sensitivity			15	45	μV
Signal-to-Noise Ratio	e_{FM} = 10 mV	50	64		dB
Detector Output	e_{FM} = 10 mV, Δf = ±22.5 kHz Measure at Top of Volume Control	40	60	85	mV
AM Rejection	e_{FM} = 10 mV, 30% AM Modulation	40	50		dB
Total Harmonic Distortion (THD)	e_{FM} = 10 mV		1.1	2	%
DYNAMIC CHARACTERISTICS—AUDIO AMPLIFIER ONLY f = 1 kHz, e_{AM} = 0, e_{FM} = 0, S1 in Position 2					
Power Output	THD = 10%, R_L 8Ω				
	V_S = 6V	250	325		mW
	V_S = 9V	500	700		mW
Bandwidth	AM Mode, P_O = 50 mW		11		kHz
	FM Mode, P_O = 50 mW		22		kHz
Total Harmonic Distortion (THD)	P_O = 50 mW, FM Mode		0.2		%
Voltage Gain			41		dB

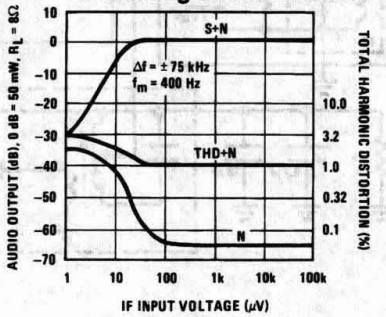
Typical Performance Characteristics

(Test Circuit) All curves are measured at audio output

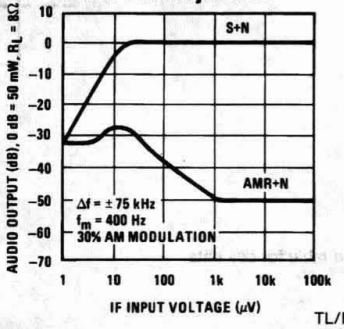
Quiescent Supply Current vs Voltage



FM Limiting Characteristics



FM IF AM Rejection

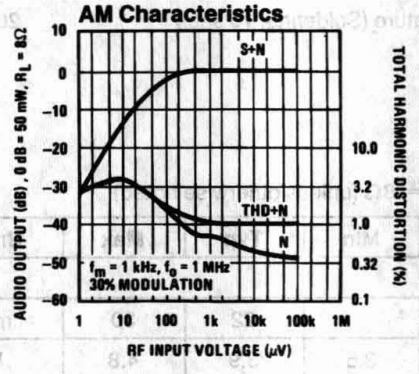


TL/H/7909–2

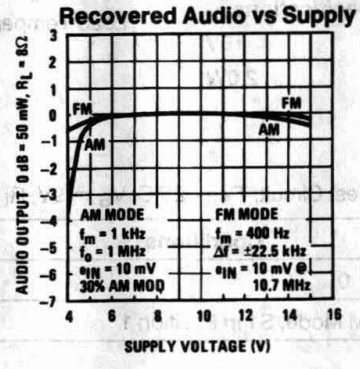
Typical Performance Characteristics (Continued)

All curves are measured at audio output (Test Circuit)

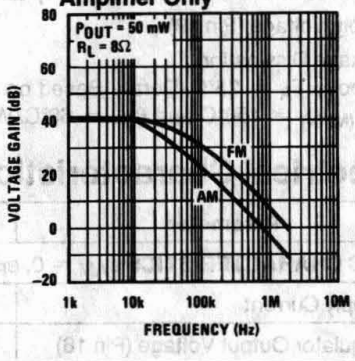
AM Characteristics



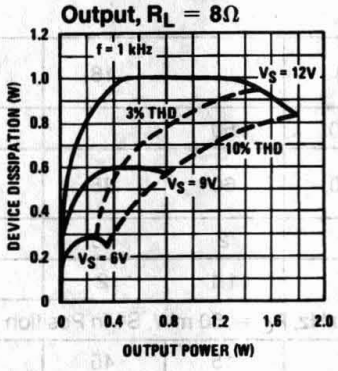
Recovered Audio vs Supply



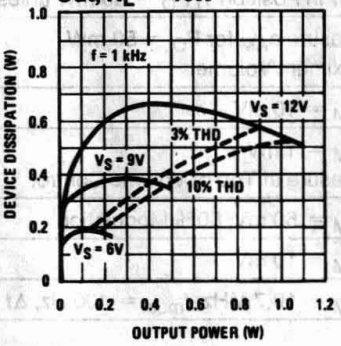
Gain vs Frequency Audio Amplifier Only



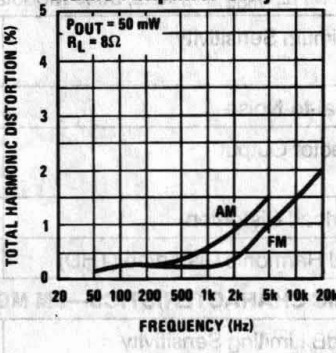
Power Dissipation vs Power Output, R_L = 8Ω



Power Dissipation vs Power Out, R_L = 16Ω



Distortion vs Frequency Audio Amplifier Only



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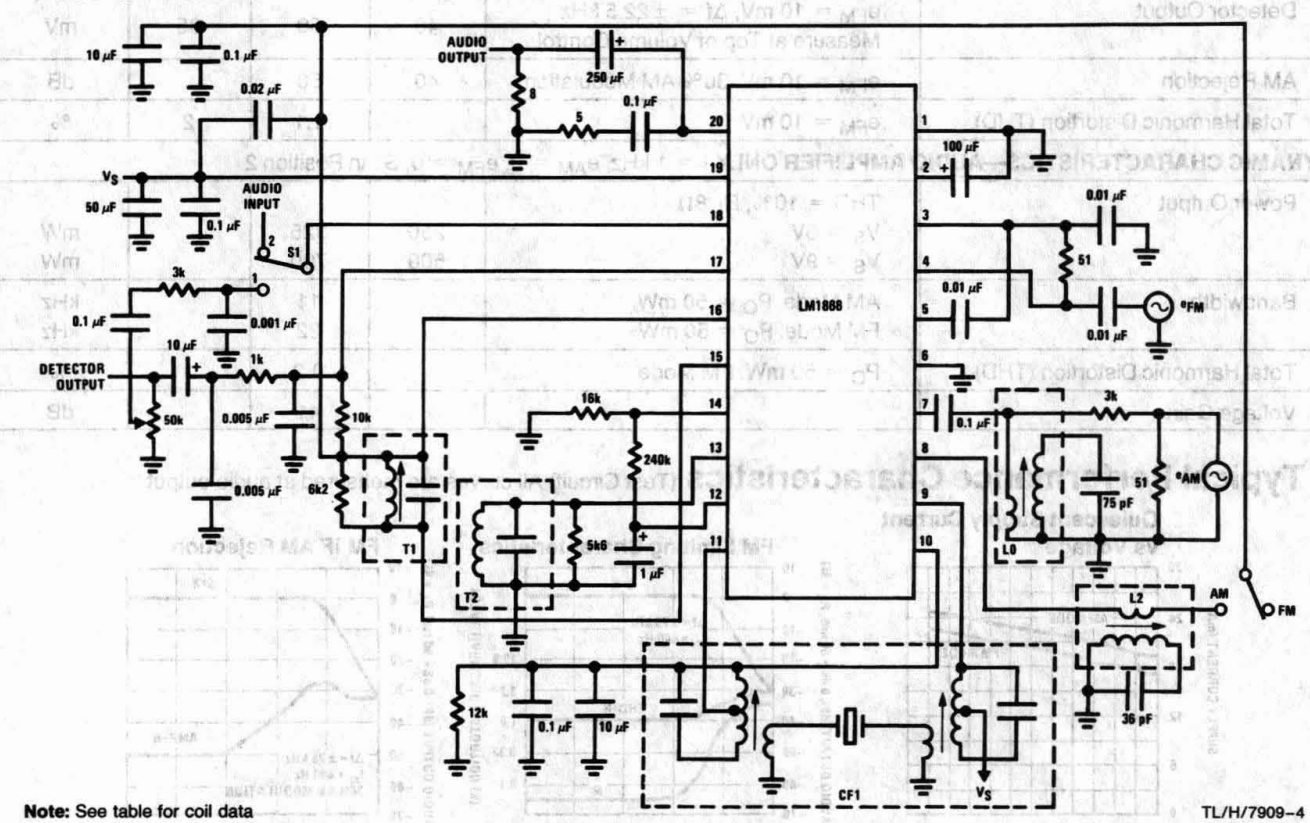
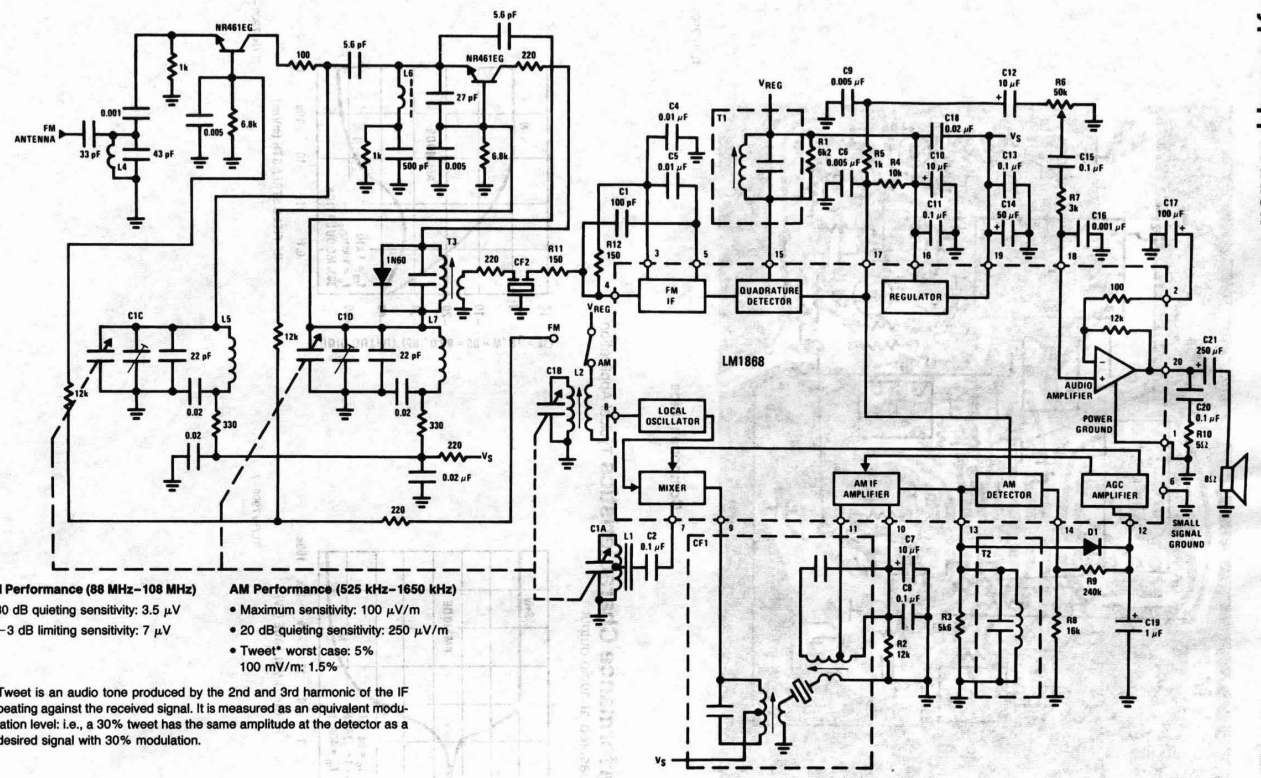
Test Circuit



Note: See table for coil data

TL/H/7909–4

Typical Application



FM Performance (88 MHz–108 MHz)

- 30 dB quieting sensitivity: 3.5 μV
- −3 dB limiting sensitivity: 7 μV

AM Performance (525 kHz–1650 kHz)

- Maximum sensitivity: 100 μV/m
- 20 dB quieting sensitivity: 250 μV/m
- Tweet* worst case: 5%
  100 mV/m: 1.5%

*Tweet is an audio tone produced by the 2nd and 3rd harmonic of the IF beating against the received signal. It is measured as an equivalent modulation level: i.e., a 30% tweet has the same amplitude at the detector as a desired signal with 30% modulation.

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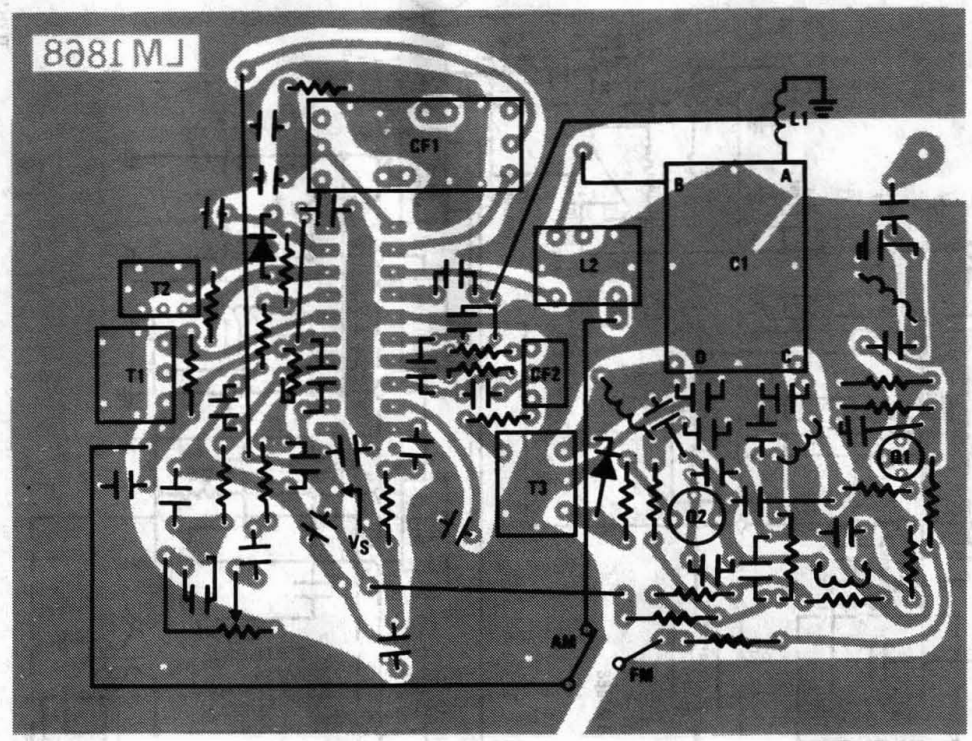
PC Board Layout



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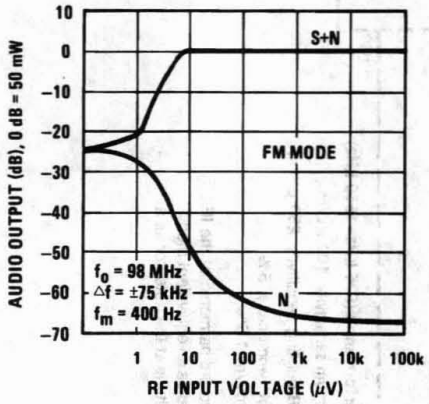
Component Side

Typical Performance Characteristics Typical Application

All curves are measured at audio output



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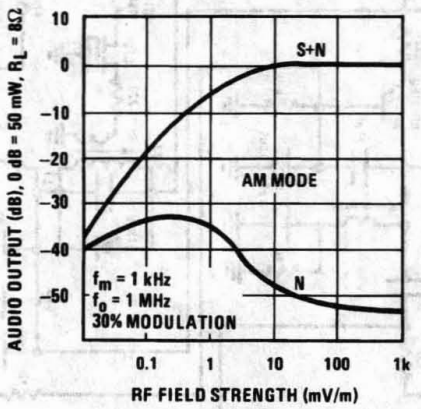


TL/H/7909–8

IC External Components (Application Circuit)

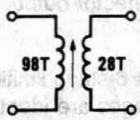
Component	Typical Value	Comments
C1	100 pF	Removes tuner LO from IF input
C2	0.1 μF	Antenna coupling capacitor
C4, C5	0.01 μF	FM IF decoupling capacitors
C6, C9	0.005 μF	AM smoothing/FM de-emphasis network, de-emphasis pole is given by. $f1 \cong \frac{1}{2\pi\,(C6 + C9)\left(\frac{R4\ \ R6}{R4 + R6}\right)}$
R5	1k	
C10	10 μF	Regulator decoupling capacitor
C11	0.1 μF	Regulator decoupling capacitor
C12	10μF	AC coupling to volume control
C13	0.1 μF	Power supply decoupling
C14	50 μF	Power supply decoupling
C15	0.1 μF	Audio amplifier input coupling
R7	3k	Roll off signals from detector in the AM band to prevent radiation
C16	0.001 μF	
C17	100 μF	Power amplifier feedback decoupling, sets low frequency supply rejection
R8	16k	AM detector bias resistor
R9	240k	Set AGC time constant
C19	1 μF	
C7	10 μF	IF coupling
C8	0.1 μF	IF coupling
C20	0.1 μF	High frequency load for audio amplifier, required to stabilize audio amplifier
R10	5Ω	
C21	250 μF	Output coupling capacitor
R1	6k2	Sets Q of quadrature coil, determining FM THD and recovered audio
R2	12k	IF amplifier bias R
R3	5k6	Sets gain of AM IF and Q of AM IF output tank
R4	10k	Detector load resistor
R6	50k	Volume control
C18	0.02 μF	Power supply decoupling
R11, R12	150Ω	Terminates the ceramic filter, biases FM IF input stage
D1	1N4148	Optional. Quickens the AGC response during turn on

Coil and Tuning Capacitor Specifications

C1 — AM ANT 140 pF max 5.0 pF min; AM OSC 82 pF max 5.0 pF min; Trimmers 5 pF — FM 20 pF max 4.5 pF min; TOKO CY2-22124PT

L1 — 640 μH, Q_u = 200; R_P = 3k5 @ F = 796 kHz (At secondary) — AM antenna; 1 mV/meter induces approximately 100 μV open circuit at the secondary

L0, L2 — 360 μH, Q_U > 80 @ F = 796 kHz — TOKO RWO-6A5105 or equivalent



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Toko America
1250 Feehanville Drive
Mount Prospect, IL 60056
(312) 297-0070

L4 — SWG #20, N = 3½T, inner diameter = 5 mm

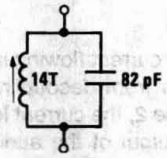
L5 — SWG #20, N = 3½T, inner diameter = 5 mm

L6 — L = 0.44 μH, N = 4 ½T, Qu = 70

L7 — SWG #20, N = 2 ½T, inner diameter = 5 mm

CF2 — 10.7 MHz ceramic filter MURATA SFE 10.7 mA or equivalent — Murata
2200 Lake Park Drive
Smyrna, GA 30080
(404) 436-1300

T1 — Q_u > 70 @ 10.7 MHz, L to resonate w/82 pF @ 10.7 MHz TOKO KAC-K2318 or equivalent



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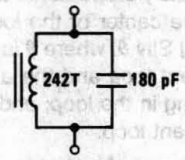
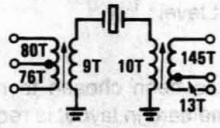
T2 — Q_u > 14 @ 455 kHz, L to resonate w/180 pF @ 455 kHz TOKO 159GC-A3785 or equivalent



TL/H/7909–11

CF1 — TOKO CFU-090D or equivalent BW > 4.8 kHz @ 455 kHz



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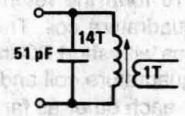
T3 — Apollo Electronics NS-107C or equivalent



TL/H/7909–13

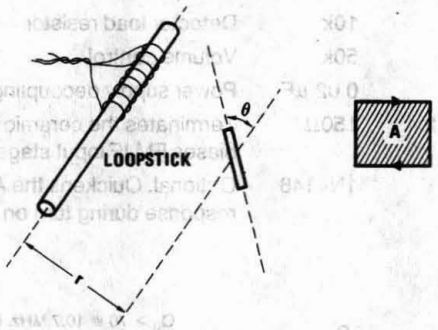
Layout Considerations

AM SECTION

Most problems in an AM radio design are associated with radiation of undesired signals to the loopstick. Depending on the source, this radiation can cause a variety of problems including tweet, poor signal-to-noise, and low frequency oscillation (motor boating). Although the level of radiation from the LM1868 is low, the overall radio performance can be degraded by improper PCB layout. Listed below are layout considerations association with common problems.

1. **Tweet:** Locate the loopstick as far as possible from detector components C6, C9, R4, and R5. Orient C6, C9, R4, and R5 parallel to the axis of the loopstick. Return R8, C6, C9, and C19 to a separate ground run (see Typical Application PCB).

2. **Poor Signal-to-Noise/Low Frequency Oscillation:** Twist speaker leads. Orient R10 and C20 parallel to the axis of the loopstick. Locate C11 away from the loopstick.



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In general, radiation results from current flowing in a loop. In case 1 this current loop results from decoupling detector harmonics at pin 17; while in case 2, the current loop results from decoupling noise at the output of the audio amplifier and the output of the regulator. The level of radiation picked up by the loopstick is approximately proportional to: 1) $1/r^3$; where r is the distance from the center of the loopstick to the center of the current loop; 2) SIN θ, where θ is the angle between the plane of the current loop and the axis of the loopstick; 3) I, the current flowing in the loop; and 4) A, the cross-sectional area of the current loop.

Pickup is kept low by short leads (low A), proper orientation ($\theta \cong 0$ so SIN $\theta \cong 0$), maximizing distance from sources to loopstick, and keeping current levels low.

FM SECTION

The pinout of the LM1868 has been chosen to minimize layout problems, however some care in layout is required to insure stability. The input source ground should return to C4 ground. Capacitors C13 and C18 form the return path for signal currents flowing in the quadrature coil. They should connect directly to the proper pins with short PC traces (see Typical Application PCB). The quadrature coil and input circuitry should be separated from each other as far as possible.

AUDIO AMPLIFIER

The standard layout considerations for audio amplifiers apply to the LM1868, that is: positive and negative inputs should be returned to the same ground point, and leads to the high frequency load should be kept short. In the case of the LM1868 this means returning the volume control ground (R6) to the same ground point as C17, and keeping the leads to C20 and R10 short.

Circuit Description (See Equivalent Schematic)

AM SECTION

The AM section consists of a mixer stage, a separate local oscillator, an IF gain block, an envelope detector, AGC circuits for controlling the IF and mixer gains, and a switching circuit which disables the AM section in the FM mode.

Signals from the antenna are AC-coupled into pin 7, the mixer input. This stage consists of a common-emitter amplifier driving a differential amp which is switched by the local oscillator. With no mixer AGC, the current in the mixer is 330 μA; as the AGC is applied, the mixer current drops, decreasing the gain, and also the input impedance drops, reducing the signal at the input. The differential amp connected to pin 8 forms the local oscillator. Bias resistors are arranged to present a negative impedance at pin 8. The frequency of oscillation is determined by the tank circuit, the peak-to-peak amplitude is approximately 300 μA times the impedance at pin 8 in parallel with 8k2.

After passing through the ceramic filter, the IF signals are applied to the IF input. Signals at pin 11 are amplified by two AGC controlled common-emitter stages and then applied to the PNP output stage connected to pin 13. Biasing is arranged so that the current in the first two stages is set by the difference between a 250 μA current source and the Darlington device connected to pin 12.

When the AGC threshold is exceeded, the Darlington device turns ON, steering current away from the IF into ground, reducing the IF gain. Current in the IF is monitored by the mixer AGC circuit. When the current in the IF has dropped to 30 μA, corresponding to 30 dB gain reduction in the IF, the mixer AGC line begins to draw current. This causes the mixer current and input impedance to drop, as previously described.

The IF output is level shifted and then peak detected at detector cap C1. By loading C1 with only the base current of the following device, detector currents are kept low. Drive from the AGC is taken at pin 14, while the AM detector output is summed with the FM detector output at pin 17.

FM SECTION

The FM section is composed of a 6-stage limiting IF driving a quadrature detector. The IF stages are identical with the exceptions of the input stage, which is run at higher current to reduce noise, and the last stage, which is switched OFF in the AM mode. The quadrature detector collectors drive a level shift arrangement which allows the detector output load to be connected to the regulated supply.

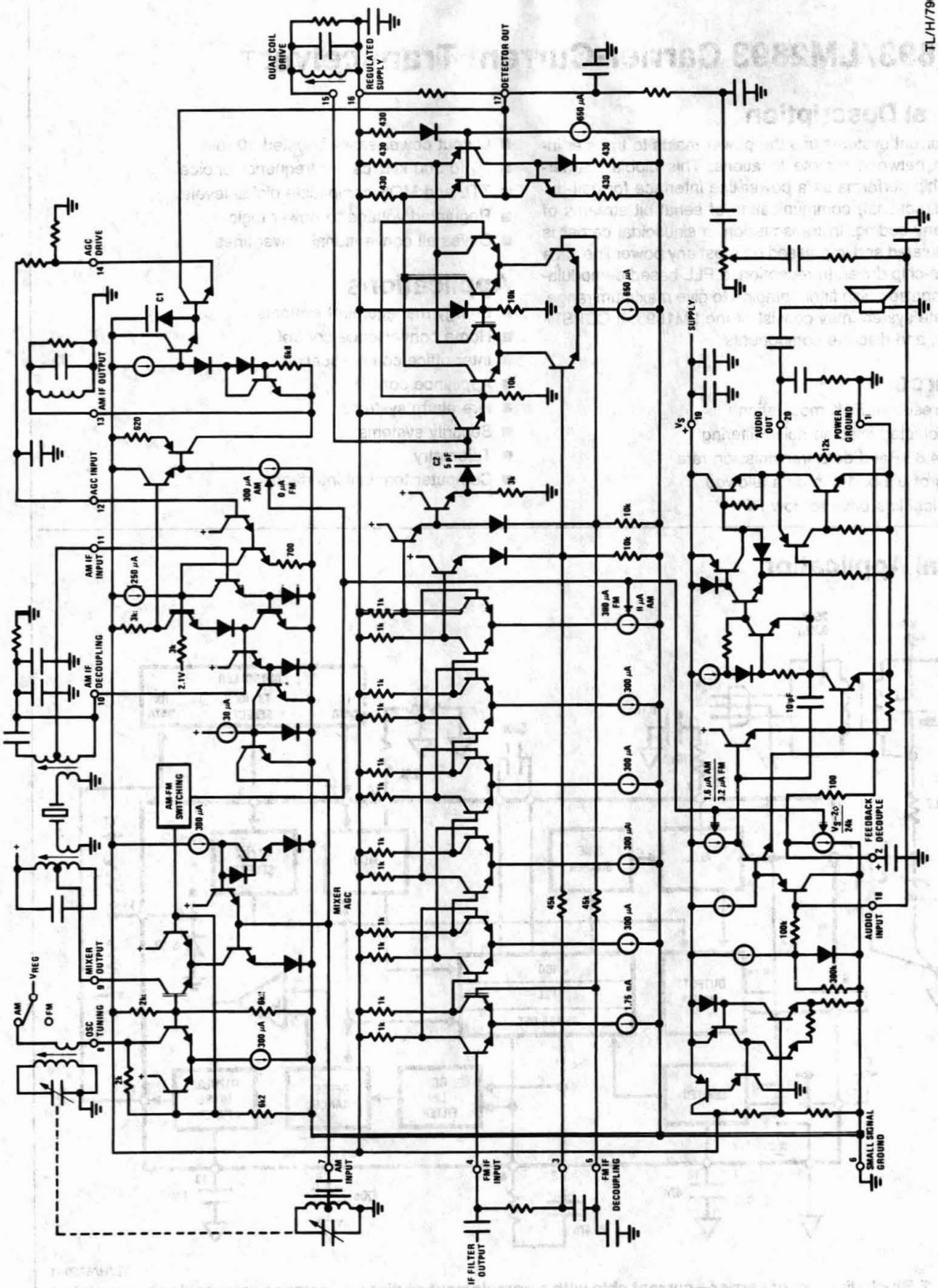
AUDIO AMPLIFIER

The audio amplifier has an internally set voltage gain of 120. The bandwidth of the audio amplifier is reduced in the AM mode so as to reduce the output noise falling in the AM band. The bandwidth reduction is accomplished by reducing the current in the input stage.

REGULATOR

A series pass regulator provides biasing for the AM and FM sections. Use of a PNP pass device allows the supply to drop to within a few hundred millivolts of the regulator output and still be in regulation.

Equivalent Schematic



National Semiconductor

LM1893/LM2893 Carrier-Current Transceiver†

General Description

Carrier-current systems use the power mains to transfer information between remote locations. This bipolar carrier-current chip performs as a power line interface for half-duplex (bi-directional) communication of serial bit streams of virtually any coding. In transmission, a sinusoidal carrier is FSK modulated and impressed on most any power line via a rugged on-chip driver. In reception, a PLL-based demodulator and impulse noise filter combine to give maximum range. A complete system may consist of the LM1893, a COPS™ controller, and discrete components.

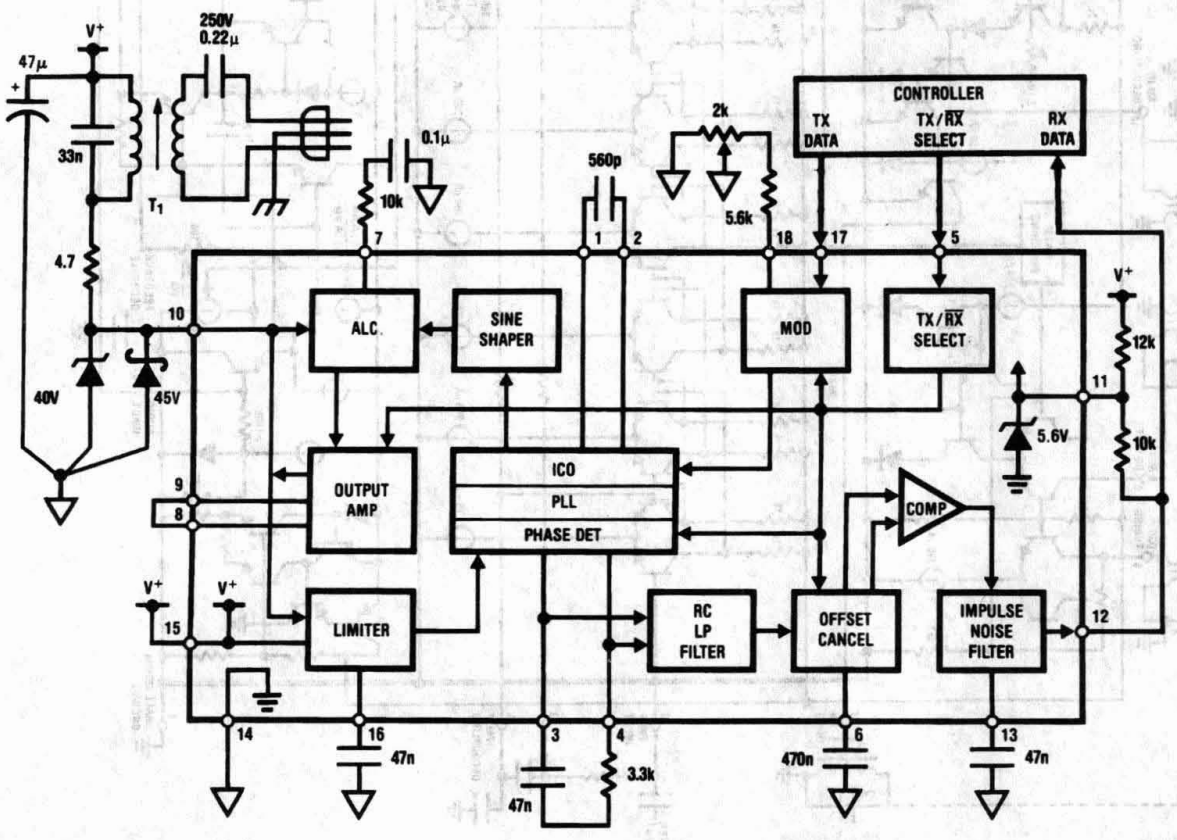
Features

- Noise resistant FSK modulation
- User-selected impulse noise filtering
- Up to 4.8 kBaud data transmission rate
- Strings of 0's or 1's in data allowed
- Sinusoidal line drive for low RFI
- Output power easily boosted 10-fold
- 50 to 300 kHz carrier frequency choice
- TTL and MOS compatible digital levels
- Regulated voltage to power logic
- Drives all conventional power lines

Applications

- Energy management systems
- Home convenience control
- Inter-office communication
- Appliance control
- Fire alarm systems
- Security systems
- Telemetry
- Computer terminal interface

Typical Application



TL/H/6750–1

FIGURE 1. Block diagram of carrier—current chip with a complement of discrete components making a complete $F_O = 125$ kHz, $f_{DATA} = 360$ Baud transceiver. Use caution with this circuit—dangerous line voltage is present.

†Carrier-Current Transceivers are also called Power Line Carrier (PLC) transceivers.

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply voltage		30 V
Voltage on pin 12		55 V
Voltage on pin 10 (Note 1)		41 V
Voltage on pins 5 and 17		40 V
5.6 V DC zener current		100 mA
Junction temperature:	transmit mode	150°C
	receive mode	125°C
Electro-Static Discharge (120 pF, 1500Ω)		1KV

Maximum continuous dissipation, $T_A = 25°C$,		
plastic DIP N (Note 2):	transmit mode	1.66 W
	receive mode	1.33 W
Operating ambient temp. range		−40 to 85°C
Storage temperature range		−65 to 150°C
Lead temp., soldering, 7 seconds		260°C

Note: *Absolute maximum ratings indicate limits beyond which damage to the device may occur. Electrical specifications are not ensured when operating the device above guaranteed limits but below absolute maximum limits, but there will be no device degradation.*

General Electrical Characteristics

(Note 3). The test conditions are: $V^+ = 18V$ and $F_O = 125$ kHz, unless otherwise noted.

#	Parameter	Conditions	Typical	Test Limit (Note 4)	Design Limit (Note 5)	Limit Units
1	5.6 V Zener voltage, V_Z	Pin 11, $I_Z = 2$ mA	5.6	5.2 5.9		V min. V max.
2	5.6 V Zener resistance, R_Z	Pin 11, $R_Z = (V_Z@10\text{ mA} - V_Z@1\text{ mA})/(10\text{ mA} - 1\text{ mA})$	5			Ω
3	Carrier I/O peak survivable transient voltage, V_{OT}	Pin 10, discharge 1 μF cap. charged to V_{OT} thru <1Ω	80	60		V max.
4	Carrier I/O clamp voltage, V_{OC}	Pin 10, $I_{OC} = 10$ mA, RX mode 2N2222 diode pin 8 to 9	44	41 50		V min. V max.
5	Carrier I/O clamp resistance, R_{10}	Pin 10, $I_{OC} = 10$ mA	20			Ω
6	TX/$\overline{RX}$ low input voltage, V_{IL}	Pin 5	1.8	0.8		V max.
7	TX/$\overline{RX}$ high input voltage, V_{IH}	Pin 5 (Note 9)	2.2	2.8		V min.
8	TX/$\overline{RX}$ low input current, I_{IL}	Pin 5 at 0.8 V	−2	−20 1		μA min. μA max.
9	TX/$\overline{RX}$ high input current, I_{IH}	Pin 5 at 40 V	10^{-4}	−1 10	**0**	μA min. μA max.
10	RX−TX switch-over time, T_{RT}	Time to develop 63% of full current drive thru pin 10	10			μs
11	TX−RX switch-over time, T_{TR}	1 bit time, $T_B = 1/(2F_{DATA})$. Time T_{TR} is user controlled with C_M, see Apps. Info.	2			bit
12	ICO initial accuracy of F_O	TX mode, $R_O = 6.65$ kΩ, $C_O = 560$ pF $F_0 = (F_1 + F_2)/2$	125	113 137		kHz min. kHz max.
13	ICO temperature coefficient of F_O	TX or RX mode, $(F_{OMAX} - F_{OMIN})/(T_{JMAX} - T_{JMIN})$	**−100**			PPM/°C
14	Temperature drift of F_O	TX or RX mode, $-40 \le T_J \le T_{JMAX}$	**±2.0**		**±5.0**	% max.

Transmitter Electrical Characteristics

(Note 3). The test conditions are: $V^+ = 18$ V and $F_O = 125$ kHz unless otherwise noted. The transmit center frequency is F_O, FSK low is F_1, and FSK high is F_2.

#	Parameter	Conditions	Typical	Test Limit (Note 4)	Design Limit (Note 5)	Limit Units
15	Supply voltage, V^+, range	Meets test 17 spec. at $T_J = 25°C$ and: $\lvert(F_1[14V] - F_1[18V])/F_1[18V]\rvert < 0.01$ $\lvert(F_1[24V] - F_1[18V])/F_1[18V]\rvert < 0.01$	**13** **40**	14 24	**15** **23**	V min. V max.
16	Total supply current, I_{QT}	Pin 15. Pin 12 high. I_{QT} is I_Q through pin 15 and the average current I_{ODC} of the Carrier I/O through pin 10	52	79		mA max.
17	Carrier I/O output current, I_O	100Ω load on pin 10	70	45		mApp min.
18	Carrier I/O lower swing limit, V_{ALC}	Pin 10. Set internally be ALC. 2N2222 diode pin 8 to 9	4.7	4.0 5.7		V min. V max.
19	THD of I_O (Note 6)	Q of 10 tank driving 10Ω line 100Ω load, no tank	0.6 5.5		**5.0** 9	% max. % max.
20	FSK deviation, $F_2 - F_1$	$(F_2 - F_1)/([F_2 + F_1]/2)$	4.4	3.7 5.2		% min. % max.
21	Data In. low input voltage, V_{IL}	Pin 17	1.7	0.8		V max.
22	Data In. high input voltage, V_{IH}	Pin 17 (Note 9)	2.1	2.8		V min.
23	Data In. low input current, I_{IL}	Pin 17 at 0.8 V	−1	−10 1		μA min. μA max.
24	Data In. high input current, I_{IH}	Pin 17 at 40 V	10^{-4}	−1 10	**0**	μA min. μA max.

Receiver Electrical Characteristics (Note 3). The test conditions are: $V^+ = 18$ V, $F_O = 125$ kHz, ±2.2% deviation FSK, $F_{DATA} = 2.4$ kHz, $V_{IN} = 100$ mVpp, in the receive mode, unless otherwise noted.

#	Parameter	Conditions	Typical	Test Limit (Note 4)	Design Limit (Note 5)	Limit Units
25	Supply voltage, V^+, range	Functional receiver (Note 7)	**12** **37**	13 30	**13.5** **28**	V min. V max.
26	Supply current, I_{QT}	I_{QT} is pin 15 (V^+) plus pin 10 (Carrier I/O) current. 2.4 kΩ Pin 13 to GND.	11	5 14		mA min. mA max.
27	Carrier I/O input resistance, R_{10}	Pin 10	19.5	14 30		kΩ min. kΩ max.
28	Max. data rate, F_{MD}	Functional receiver (Note 7), C_F = 100 pF, R_F = 0Ω, no tank, 2.4 kHz = 4.8 kBaud	10	4.8	**2.4**	kBaud
29	PLL capture range, F_C	C_F = 100 pF, R_F = 0 Ω	±40	±15	±**10**	% min.
30	PLL lock range, F_L	C_F = 100 pF, R_F = 0 Ω	±45	±15		% min.
31	Receiver input sensitivity, S_{IN}	For a functional receiver (Note 8) Referred to chip side (pin 10) of the line-coupling XFMR: F_O = 50 kHz F_O = 300 kHz Referred to line side of XFMR: (assuming a 7.07:1 XFMR) F_O = 50 kHz F_O = 300 kHz	 1.8 2.0 1.4 0.26 0.29 0.20	 10	 **12**	 mV_{RMS} mV_{RMS} mV_{RMS} mV_{RMS} mV_{RMS} mV_{RMS}
32	Tolerable input dc voltage offset range, V_{INDC}	Pin 10 lower than pin 15 by V_{INDC}	2	0.1		V max.
33	Data Out. breakdown voltage	Pin 12, leakage I ≤ 20 μA	70	55		V min.
34	Data Out. low output, V_{OL}	Pin 12, sat. voltage at I_{OL} = 2 mA	0.15	0.4		V max.
35	Impulse noise filter current, I_I	Pin 13 charge and discharge current	±55	±45 ±85		μA min. μA max.
36	Offset hold cap. bias voltage, V_{CM}	Pin 6	2.0	1.3 3.5		V min. V max.
37	Offset hold capacitor max. drive current, I_{MCM}	Pin 6. V(pin 3) − V(pin 4) = ±250 mV	±55	±25 ±80		μA min. μA max.
38	Offset hold bias current, I_{OHB}	Pin 6, TX mode. Bias pin 6 as it self-biased during test 31.	−0.5	−20	−**40** **40**	nA min. nA max.
39	Phase comparator current, I_{PC}	Bias pins 3 and 4 at 8.5 V I_{PC} = I(pin 3) + I(pin 4), TX mode	100	50 200		μA min. μA max.
40	Phase detector output resistance, R_{PD}	Pins 3 and 4. R_{PD} = (V@100μA − V@50μA)/(50μA)	10	6 18		kΩ min. kΩ max.
41	Phase detector demodulated output voltage, V_{PD}	Pin 3 to 4, measured after filtering out the $2F_O$ component	100	60 180		mVpp min. mVpp max.
42	Fast offset cancel voltage "window" -to-V_{PD} ratio, V_W/V_{PD}	$V_{PIN3} - V_{PIN4} = \pm V_{WINDOW}$ + DC offset Drive for ±1 μA pin 6 current	0.95	0.70 1.20		V/V min. V/V max.
43	Power supply rejection, PSRR	C_L = 0.1 μF. PSRR = CMRR. 120 Hz	80			dB min.

Note 1: More accurately, the maximum voltage allowed on pin 10 is V_{OC}, and V_{OC} ranges from 41 to 50V. Also, transients may reach above 60V; see the transient peak voltage characteristic curve.

Note 2: The maximum power dissipation rating should be derated for device operation above 25°C to insure that the junction temperature remains below the maximum rating. Use a θ_{JA} of 75°C/W for the N package using a socket in still air (which is the worst case). Consult the Application Information section for more detail.

Note 3: The **boldface** values apply over the full junction temperature range for the specified supply voltage range. All other numbers apply at $T_A = T_J = 25$°C. Pin numbers refer to LM1893. LM2893 tested by shorting Carrier In to Carrier Out and testing it as an LM1893.

Note 4: Guaranteed and 100% production tested.

Note 5: Guaranteed (but not 100% production tested) over the temperature and supply voltage ranges. These limits are not used to calculate outgoing quality levels.

Note 6: Total harmonic distortion is measured using THD = [I_{RMS} (all components at or above $2F_O$)]/[I_{RMS} (fundamental)].

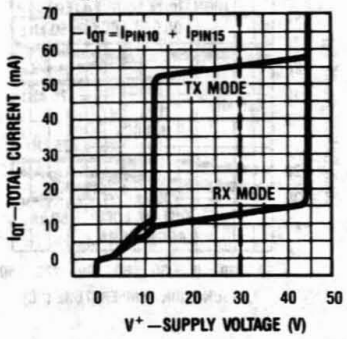
Note 7: Receiver function is defined as the error-free passage of 1 cycle of 50% duty-cycle 2.4 kHz square-wave data (2 sequential 208 μS bits), with the first bit being a "1." All of the data transitions (edges) must fall within ±10% (±20.8 μs) of their noise-free positions. RX time delay is minimized by using no impulse noise filter cap. C_I for this test.

Note 8: During the sensitivity check, note 7 requirements are followed with these exceptions: (1) data rate $F_{DATA} = 1.2$ kHz, (2) all of the data transitions must fall within ±20% (±41.6 μs) of their noise-free positions, and (3), a time-domain filter capacitor (C_I) is used. The time delay of C_I is ½ bit, or 208 μs. (C_I is approximately 6200 pF).

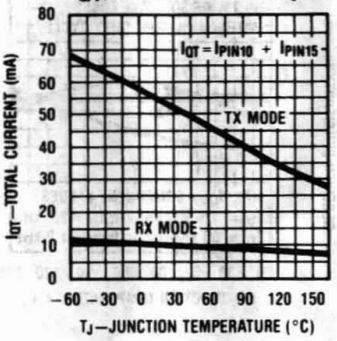
Note 9: For TTL compatibility use a pull-up resistor to increase min. V_{OH} to above 2.8 V.

Typical Performance Characteristics ($V^+ = 18V$, $F_O = 125$ kHz, circuit of *Figure 1*, pin numbers for LM1893)

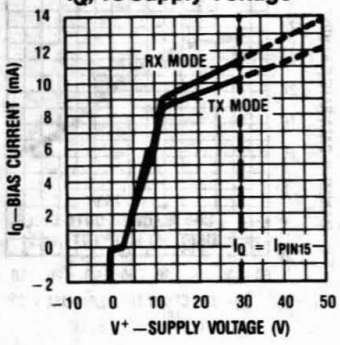
Total Current Consumption, I_{QT}, vs Supply Voltage



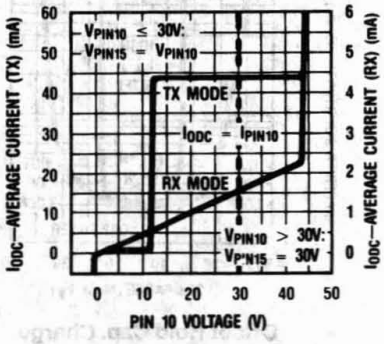
Total Current Consumption, I_{QT}, vs Junction Temperature



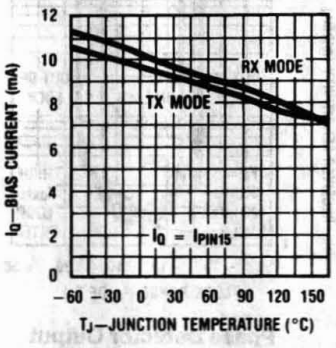
Chip Bias Current, I_Q, vs Supply Voltage



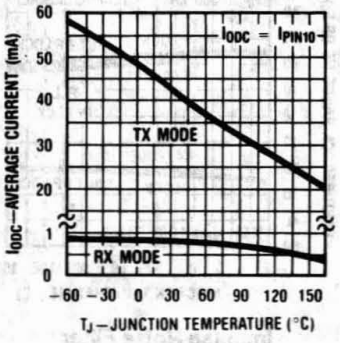
Chip Bias Current, I_Q, vs Junction Tempurature



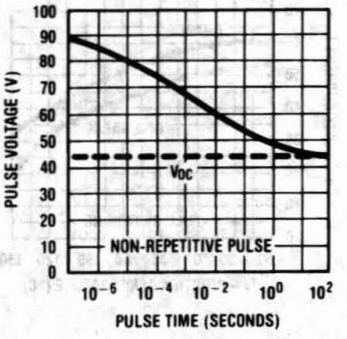
Output Stage DC Current, I_{ODC}, vs Output Voltage



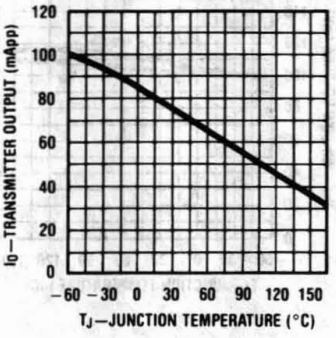
Output Stage DC Current, I_{ODC}, vs Junction Temperature



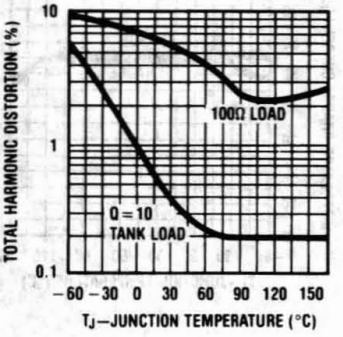
Transient Voltage Survival vs Pulse Time



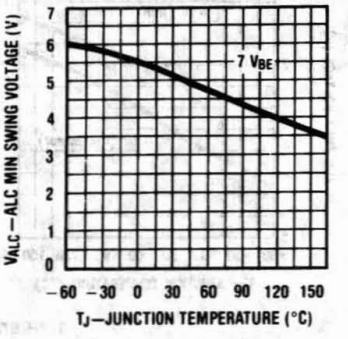
Transmitter AC Output Current vs Junction Temperature



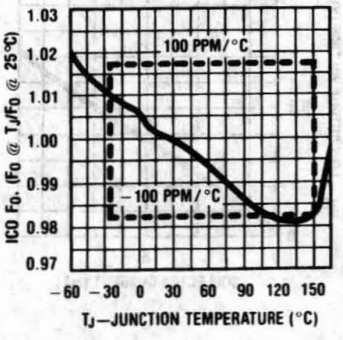
Transmitter Sinusoid THD vs Junction Temperature



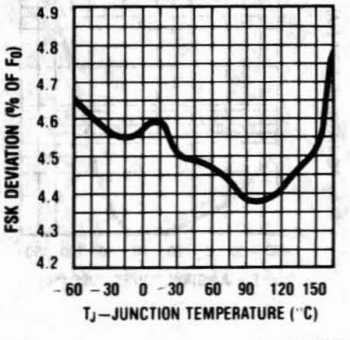
ALC Voltage vs Junction Temperature



ICO Frequency vs Junction Temperature



Transmitter FSK Deviation vs Junction Temperature



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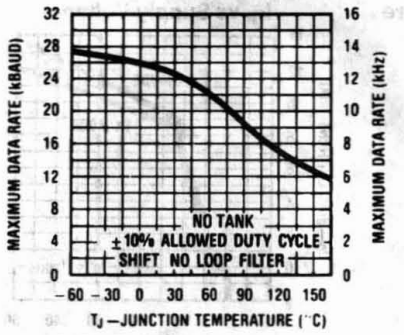
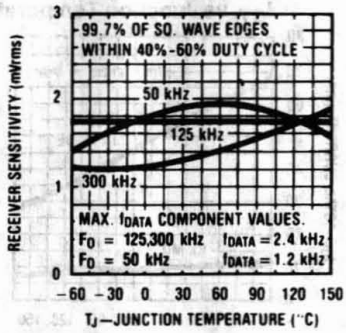
Typical Performance Characteristics (Continued)

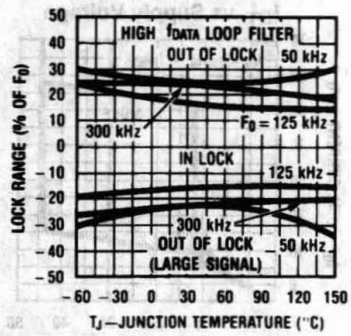
Maximum Data Rate vs Junction Temperature


MAXIMUM DATA RATE (kBAUD)
MAXIMUM DATA RATE (kHz)
NO TANK
±10% ALLOWED DUTY CYCLE SHIFT NO LOOP FILTER
TJ—JUNCTION TEMPERATURE (°C)

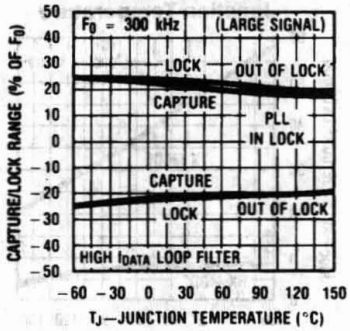
Receiver Sensitivity vs Junction Temperature


99.7% OF SQ. WAVE EDGES WITHIN 40%-60% DUTY CYCLE
50 kHz
125 kHz
300 kHz
MAX. fDATA COMPONENT VALUES.
F0 = 125,300 kHz fDATA = 2.4 kHz
F0 = 50 kHz fDATA = 1.2 kHz
RECEIVER SENSITIVITY (mVrms)
TJ—JUNCTION TEMPERATURE (°C)

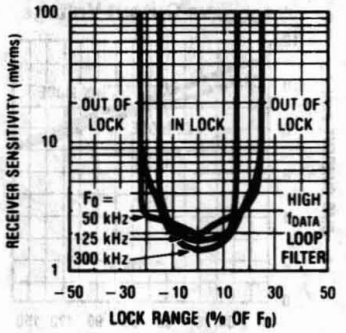
PLL Lock Range vs Junction Temperature and F_O



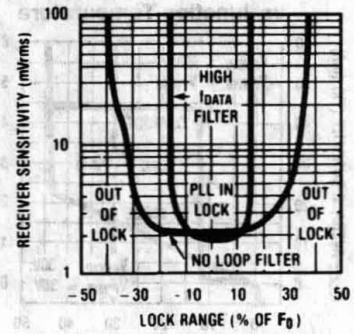
PLL Capture & Lock Range vs Junction Temperature



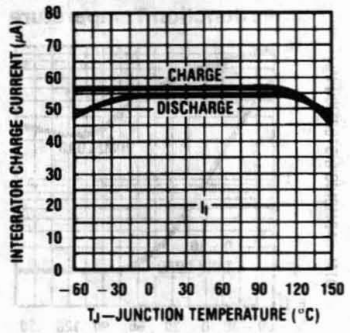
Receiver Sensitivity vs PLL Lock Range and F_O



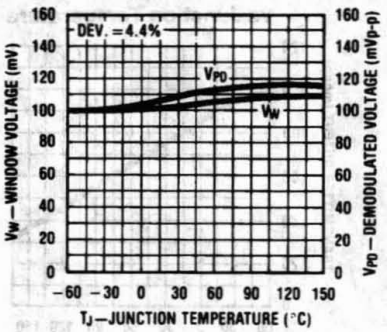
Receiver Sensitivity vs PLL Lock Range and Loop Filter



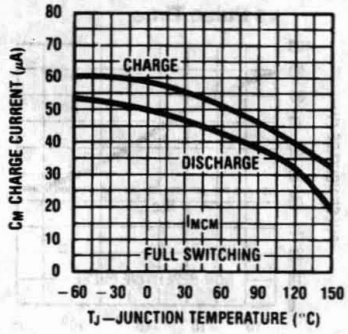
Impulse Noise Filter Current vs Junction Temperature



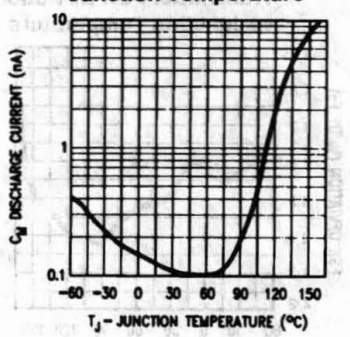
Phase Detector Output Voltage vs Junction Temperature



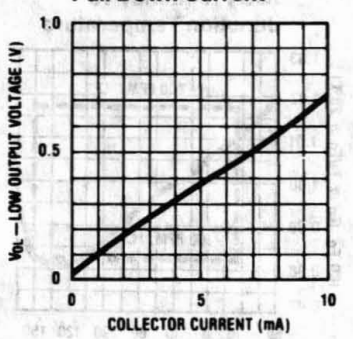
Offset Hold Cap. Charge Currents vs Junction Temperature



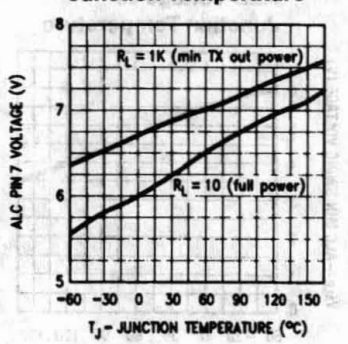
Offset Hold Cap. Bias Current vs Junction Temperature



Data Out. Low Voltage vs Pull Down Current



Pin 7 Bias Voltage vs Junction Temperature



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Application Information*

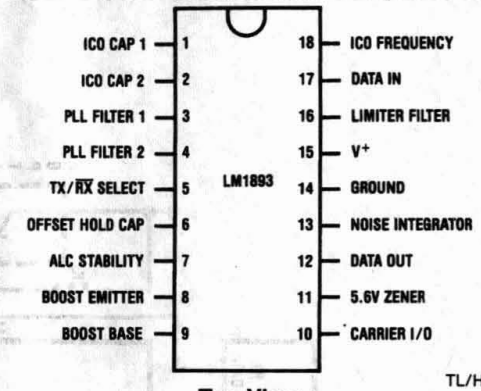
THE DATA PATH

The BI-LINE™ chip serves as a power line interface in the carrier-current transceiver (CCT) system of *Figure 3*. *Figure 4* shows the interface circuit now discussed. The controller may select either the transmit (TX) or receive (RX) mode. Serial data from the controller is used to generate a FSK-modulated 50 to 300 kHz carrier on the line in the TX mode. In the RX mode line signal passes through the coupling transformer into the PLL-based receiver. The recreated serial bit stream drives the controller.

With the IC in the TX mode (pin 5 a logic high), baseband data to 5 kHz drive the modulator's Data In pin to generate a switched 0.978I/1.022I control current to drive the low TC, triangle-wave, current-controlled oscillator to ±2.2% deviation. The tri-wave passes through a differential attenuator and sine shaper which deliver a current sinusoid through an automatic level control (ALC) circuit to the gain of 200 current output amplifier. Drive current from the Carrier I/O develops a voltage swing on T_1's (*Figure 4*) resonant tank proportional to line impedance, then passes through the step-down transformer and coupling capacitor C_C onto the line. Progressively smaller line impedances cause reduced signal swing, but never clipping-thus avoiding potential radio frequency interference. When large line impedances threaten to allow excessive output swing on pin 10, the ALC shunts current away from the output amplifier, holding the voltage swing constant and within the amp's compliance limit. The amplifier is stable with a load of any magnitude or phase angle.

In the RX mode (pin 5 a logic low), the TX sections on the chip are disabled. Carrier signal, broad-band noise, transient spikes, and power line component impinge of the receiver's input highpass filter, made up of C_C and T_1, and the tank bandpass filter. In-band carrier signal, band-limited noise, heavily attenuated line frequency component, and attenuated transient energy pass through to produce voltage swing on the tank, swinging about the positive supply to drive the Carrier I/O receiver input. The balanced Norton-input limiter amplifier removes DC offsets, attenuates line frequency, performs as a bandpass filter, and limits the signal to drive the PLL phase detector differentially. The differential demodulated output signal from the phase detector, containing AC and DC data signal, noise, system DC offsets, and a large twice-the-carrier-frequency component, passes through a 3-stage RC lowpass filter to drive the offset cancel circuit differentially. The offset cancelling circuit works by insuring that the (fixed) ±50 mV signal delivered to the data squaring ("slicing") comparator is centered around the 0 mV comparator switch point. Whenever the comparator signal plus DC offset and noise moves outside the carefully matched ±50 mV voltage "window" of the offset cancel circuit, it adjusts its DC correction voltage in series with the differential signal to force the signal back into the window. While the signal is within the ±50 mV window, the DC offset is stored on capacitor C_M. By grace of the highly non-linear offset hold capacitor charging during offset cancelling, the DC cancellation is done much more quickly than with an AC coupling capacitor normally used in place of the offset cancel circuit. Since impulse noise spikes normally ring the signal symmetrically around 0 V, the fully bilateral offset cancel topology affords excellent noise rejection. The switched current output of the comparator drives the impulse noise filter integrator capacitor that rejects all data pulses of less than the integrator charge time. Noise appears as duty-cycle jitter at the open collector serial data output.

Dual-In-Line Package

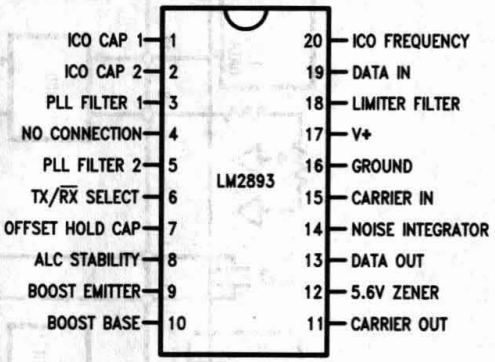


TL/H/6750–2

Top View

Order Number LM1893N
See NS Package Number N18A

Small Outline & Dual-In-Line Package

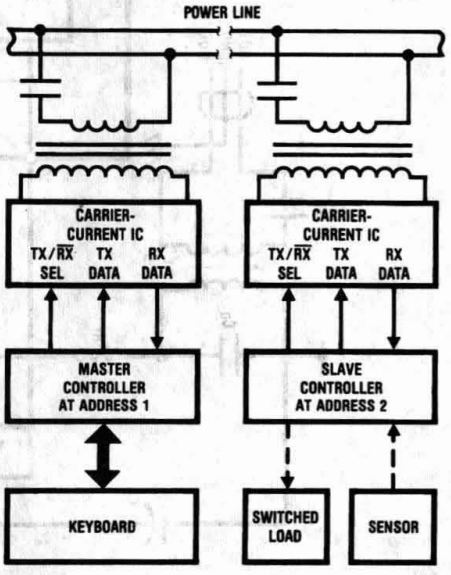


TL/H/6750–41

Top View

Order Number LM2893M or LM2893N
See NS Package Number M20B or N20A

FIGURE 2. Connection Diagrams

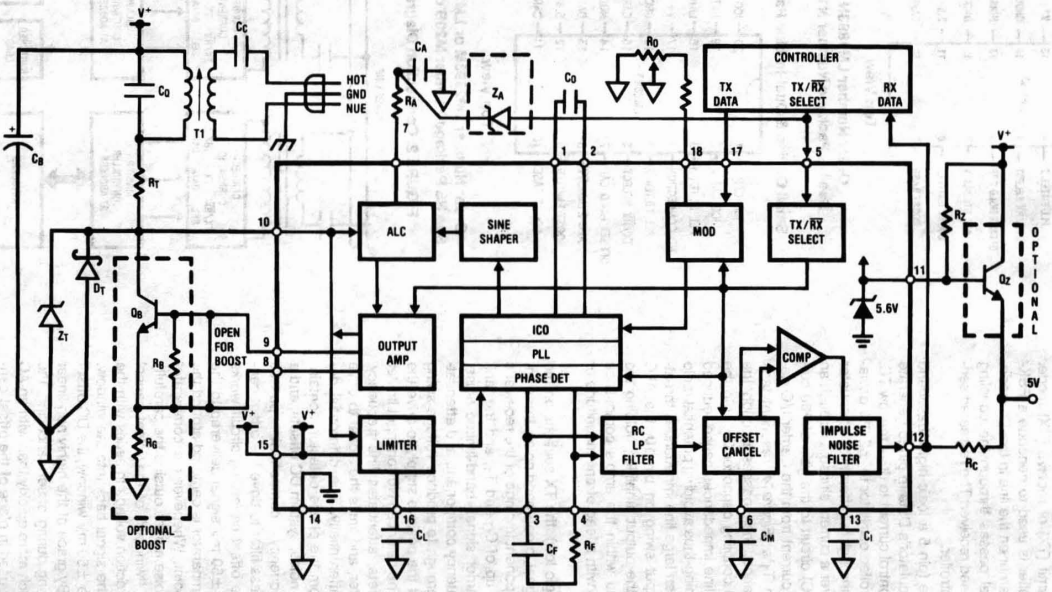


TL/H/6750–3

FIGURE 3. The block diagram of a carrier-current system using the Bi-Line chip to interface digital controllers via the power line

*Unless otherwise noted, all pin references refer to LM1893, but hold true for equivalent LM2893 pin.

Application Information (Continued)



TL/H/6750–4

FIGURE 4. Block diagram of a CCT system with the boost and 5V supply options shown in dashed boxes

Application Information (Continued)

#	Recommended Value	Purpose	Effect of making the component value: Smaller	Effect of making the component value: Larger	Notes
C_O R_O	560 pF 6.2 kΩ	Together, C_O and R_O set ICO F_O.	Increases F_O Increases F_O <5.6 k not recommended.	Decreases F_O Decreases F_O >7.6 k not recommended.	±5% NPO ceramic. Use low TC 2 k pot and 5.6 k fixed R. Poor F_O TC with <5.6 k R_O.
C_F R_F	0.047 μF 3.3 kΩ	PLL loop filter pole PLL loop filter zero	Less noise immune, higher f_{DATA}, more PLL stability. PLL less stable, allows less C_F. Less ringing.	More noise immune, lower f_{DATA}, less PLL stability. PLL more stable, allows more C_F. More ringing.	Depending on R_F value and F_O, PLL unstable with large C_F. See Apps. Info. C_F and R_F values not critical.
C_C	0.22 μF	Couples F_O to line, C_C and T_1 low-pass attenuates 60 Hz.	Low TX line amplitude. Less 60 Hz T_1 current. Less stored charge.	Drives lower line Z. More 60 Hz T_1 current. More stored charge.	≥250 V non-polar. Use $2C_C$ on hot and neutral for max. line isolation, safety.
C_Q T_1	0.033 μF Use recommended XFMR	Tank matches line Z, bandpass filters, isolates from line, and attenuates transients.	Tank F_O up or increase L of T_1 for constant F_O. Smaller L: higher F_O or increase C_C; decreased F_O line pull.	Tank F_O down or decrease L of T_1 for constant F_O. Larger L: lower F_O or decrease C_C; increased F_O line pull.	100 V nonpolar, low TC, ±10% High large-signal Q needed. Optimize for low F_O line pull with control of F_O TC and Q.
C_A R_A	0.1 μF 10 kΩ	ALC pole ALC zero	Noise spikes turn ALC off. Less stable ALC.	Slower ALC response. More stable ALC.	R_A optional. ALC stable for C_A≥100 pF.
C_L	0.047 μF	Limiter 50 kHz pole, 60 Hz rejection.	Higher pole F, more 60 Hz reject. F_O attenuation?	Lower pole F, less 60 Hz reject, more noise BW.	Any reasonably low TC cap. 300 pF guarantees stability.
C_M	0.47 μF	Holds RX path V_{OS}	Less noise immune, shorter V_{OS} hold, faster V_{OS} aquisition, shorter preamble.	More noise immune, longer V_{OS} hold, slower V_{OS} aquisition, longer preamble.	Low leakage ±20% cap. Scale with f_{DATA}.
C_I	0.047 μF	Rejects short pulses like impulse noise.	Less impulse reject, less delay, more pulse jitter.	More impulse reject, more delay, less pulse jitter.	C_I charge time ½ bit nom. Must be <1 bit worst-case.
R_C	10 kΩ	Open-col. pull-up	Less available sink I.	Less available source I.	R_C≥1.5 kΩ on 5.6 V
R_Z	12 kΩ	5.6 V Zener bias	Larger shunt current, more chip dissipation.	Smaller shunt current, less V^+ current draw.	1<I_Z<30 mA recommended. (Chip power-up needs 5.6 V)
Z_T R_T D_T	≥44 V BV <60 V peak 4.7 Ω ≥44V BV	Transient clamp Transient I limit Over-drive Clamp	Z_T failure, higher series R-excess peak V, Zener and chip damage, less ruggedness. Damage Z_T, pull up V^+. Failure on Transient	Z_T costly, lower series R gives enhanced transient clamp, more ruggedness. Excessive TX attenuation. Costly	Recommend Zener rated for ≥500 W for 1 ms. Carbon comp. recommended. IRF 11DQ05 or 1N5819
R_B Q_B R_G	180 Ω Power NPN 1.1 Ω	Base bleed Boost gain device Current setting R	Faster, lower THD I_O. Excessive T_J and V_{SAT}. More I_O, need higher h_{fe}.	Inadequate turn-off speed. More rugged, but costly. Less I_O, lower min. h_{fe}.	Boost optional. Q_B F(−3 dB) of >200 MHz. R_B > 24 Ohm. $I_O = 70[(10+R_G)/R_G]$ mApp.
C_B	≥47 μF	Supply bypass	Transients destroy chip.	Less supply spike.	V^+ never over abs. max.
Z_A	5.1V	Stop ALC charge in RX mode	Excess ALC current flow	ALC RX charging not inhibited over T_J	Z_A optional - 5.1V ±20% low leakage type

FIGURE 5. A quick explanation of the external component function using the circuit of *Figure 4*. Values given are for V^+ = 18 V, F_O = 125 kHz, f_{DATA} = 360 Baud (180 Hz), using a 115 V 60 Hz power line

Component Selection

Assuming the circuit of *Figure 4* is used with something other than the nominal 125 kHz carrier frequency, 180 Hz data rate, 18V supply voltage, etcetera, the component values listed in *Figure 5* will need changing. This section will help direct the CCT designer in finding the required component values with emphasis placed on look-up tables and charts. It is assumed that the designer has selected values for carrier center frequency, F_O; data rate, f_{DATA}; supply voltage, V^+; power line voltage, V_L; and power line frequency, F_L. If one or more of those parameters is not defined, one may read the data sheet and make an educated guess.

Maxims to keep in mind, based on CCT electrical performance considerations only, are: 1) the higher the F_O the better, 2) the lower the maximum data rate the better, and 3) the more time and frequency filtering the better.

Use *Figure 5* as a quick reference to the external component function.

THE TRANSMITTER

C_O

Central to chip operation is the low TC of F_O emitter-coupled oscillator. With proper C_O, the F_O of the $2V_{BE}$ amplitude triangle-wave oscillator output may vary from near DC to above 300 kHz. While C_O may have any value, C_O should

Component Selection (Continued)

be made above 10 pF so that parasitic capacitance is not dominant. Excessive or unbalanced common-mode-to-ground capacitance should be avoided. A low temperature coefficient (TC) of capacitance (<100 PPM/°C), such as a monolithic NPO ceramic multilayer type, preserves low TC of F_O. *Figure 6* finds a C_O value given F_O.

R_O

Resistor R_O is used by the IC to generate a V_{BE}/R related current that is multiplied by 2 to produce the 200 μA ICO control current that sets F_O. The control current TC "bucks" the V_{BE} related tri-wave amplitude across C_O to effect a low TC of F_O. Vary R_O to trim F_O, within limits. Raising F_O more than 20% above its untrimmed value by means of decreasing R_O more than 20% is not recommended. Low R_O, and so high control current, risks ICO saturation and poor TC under worst-case conditions. Raising R_O reduces the demodulated signal amplitude from the phase detector; raising R_O by more than a factor of 2 (1 octave) is not recommended.

Since lower TC pots are relatively costly, it is recommended that R_O be made up of a 5.6 k fixed (<100 PPM/°C) resistor with a 2 kΩ (<250 PPM/°C) series pot.

C_A and R_A

Components C_A and R_A control the dynamic characteristics of the transmitter output envelope. Their values are not critical. Use the values given in *Figure 5*. C_A and R_A are functions of loaded T_1 tank Q, R_O, f_{DATA}, and line impulse noise. Any changes made in C_A and R_A should be made based on empirical measurements of a CCT on the line. Roughly, C_A acts as an ALC pole and R_A an ALC zero.

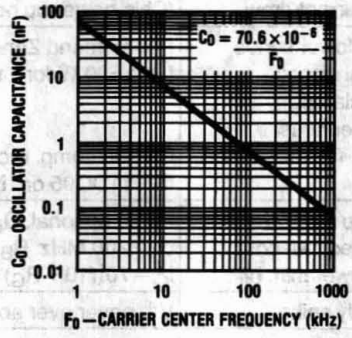
T_1

At this point, the CCT system designer may choose to use one of the recommended transformers or to design custom T_1. Consult "The Coupling Transformer" section to help with the design of T_1 if a new or boost-capable transformer is needed. The recommended 125 kHz transformer functions with an I_O of up to 600 mApp.

It is recommended that CCT systems use the recommended transformers, described in *Figure 7*, for T_1. The 3 transformers are optimized for use in the ranges of 50–100 kHz, 100–200 kHz, and 200–400 kHz with unloaded Q's (Q_U) of about 35, and loaded Q's (Q_L) of about 12. Three secondary taps are supplied with nominal 7.07, 10, and 14.1 turns ratios (N) to drive industrial and residential power line impedances of 3.5, 7, and 14Ω respectively. All are inexpensive, all have the same pin-outs for easy exchange in a PC board, and all are small - on the order of 10 mm diameter at the base.

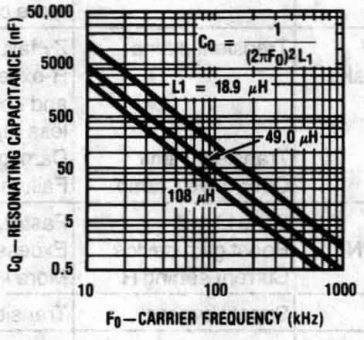
C_Q

Tank resonant frequency F_Q must be correct to allow passage of transmitter signal to the line. Use *Figure 8* to find C_Q's value. Trimming F_Q to equal F_O is done with T_1's trimming slug. The inductance of T_1 has a TC of +150 PPM/°C which may be cancelled by using a −150 PPM/°C cap such as polystyrene. Since circulating current in the tank is ¼ A_{RMS}, C_Q should have a low series resistance (a 1 Ω series resistance is too much). Polypropelene caps are excellent, "orange drop" mylars are adequate, while many other mylars are inadequate. A 100V rating is needed for transient protection.



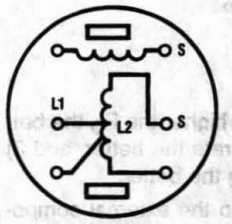
TL/H/6750–5

FIGURE 6. Find C_O's value knowing F_O

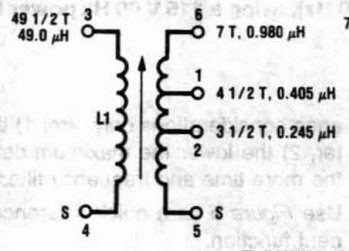


TL/H/6750–10

FIGURE 8. Find C_O's value given F_O

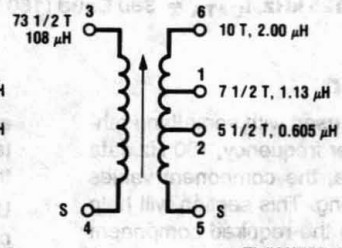


TL/H/6750–6



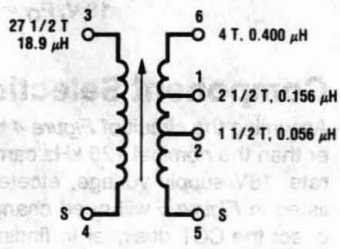
TL/H/6750–7

125 kHz
Toko 707VX-A042YUK



TL/H/6750–8

50 kHz
Toko 707VX-A043YUK



TL/H/6750–9

300 kHz
Toko 161XN-A207YUK

FIGURE 7. The recommended T_1 transformers, available through:
Toko America, 1250 Feehanville Drive, Mount Prospect, IL, 60056, (312) 297-0070

Component Selection (Continued)

C_C

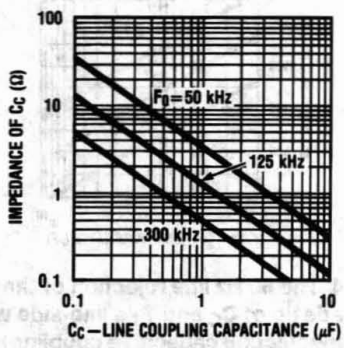
Capacitor C_C's primary function is to block the power line voltage from T_1's line-side winding. Also, C_C and T_1's line-side winding comprise a LC highpass filter. The self-inductance of T_1 is far too low to support a direct line connection. C_C must have a low enough impedance at F_O to allow T_1 to drive transmitted energy onto the line. To drive a 14Ω power line, the impedance of C_C should be below 14Ω.

Use *Figure 9* to find the reactive impedance of C_C to check that it is less than the line impedance. Then check *Figure 10* to see that the power line current is small enough to keep T_1 well out of saturation; the recommended transformers can withstand a 10 Amp-turn magnetizing force (1 Amp through the worst-case 10 turn line-side winding).

Caution is required when choosing C_C to avoid series resonance of the series combination of C_C, the transformer inductance, and the reflected tank impedance. The low resistance of the network under series resonance will load the line, possibly decreasing range. For your particular line coupling circuit, measure for series resonance using some expected line impedance load.

R_B

This base-bleed resistor turns Q_B off quickly - important since the amplifier output swing is about 200V/μs. An R_B below about 24Ω will conduct excessive current and overload the chip amplifier and is not recommended.



TL/H/6750–11

FIGURE 9. C_C's impedance should be, as a rule-of-thumb, smaller than the lowest expected line impedance

R_G

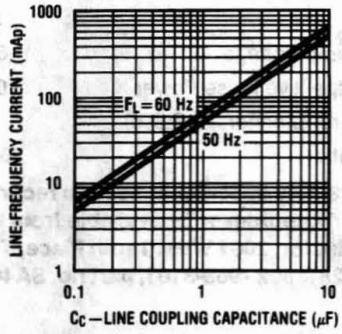
This resistor, in parallel with the internal 10Ω resistor, fixes the current gain of the output amplifier, and so the output current amplitude. *Figure 11* gives output current and minimum AC current gain h_{fe} for Q_B when R_G is used to boost output current.

Q_B

The boost gain transistor Q_B must be fast. Double-diffused devices with 50 MHz F_T's work, slower transistors (epi-base types) do not preserve a sinusoidal waveform when F_O is high or will cause the output amp. to oscillate. Q_B must have a certain minimum h_{fe} for given boost levels, as shown in *Figure 11*. *Figure 12* shows the power Q_B must dissipate continuously operating with a shorted output. BV_{CER} ($R = R_B$) must be 60V or greater and Q_B must have adequate SOA for transient survival.

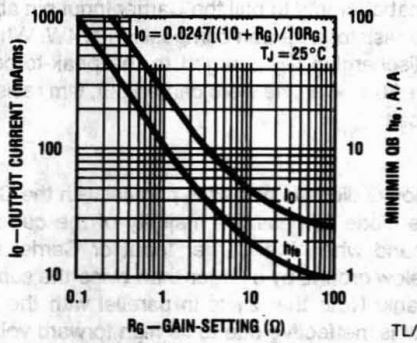
Z_T

Unfortunately, potentially damaging transient energy passes through transformer T_1 onto the Carrier I/O pin (instantaneous power of greater than 1 kW has been measured using the recommended transformers). For self protection, the Carrier I/O has an internal 44V voltage clamp with a 20Ω series resistance. A parallel low impedance 44V external transient suppression diode will then conduct the lion's share of any current when transients force the Carrier I/O to a high voltage.



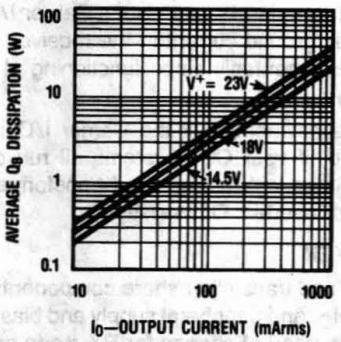
TL/H/6750–12

FIGURE 10. The AC line-induced current passed by C_C



TL/H/6750–13

FIGURE 11. Output amplifier current and required min. Q_B h_{fe} versus gain-setting resistor R_G



TL/H/6750–14

FIGURE 12. Boost transistor power dissipation versus amplifier output current

Z_T must be used unless some precaution is taken to protect the Carrier I/O pin from line transients or transients caused when stored line energy in C_C is discharged by the random phase of power line connection and disconnection. Worst case, C_C may discharge a full peak-to-peak line voltage into the tuned circuit. Another way to reduce the need for Z_T is by placing another magnetic circuit in the signal path that relies on a high, but easily saturated, permeability to couple a primary and secondary winding - a toroidal transformer for example. Toroids cost more than Z_T.

Use an avalanche diode designed specifically for transient suppression — they have orders of magnitude higher pulse

4

Component Selection (Continued)

power capability than standard avalanche diodes rated for equal DC dissipation. Metal oxide varistors have not proven useful because of their inferior clamping coefficient and are not recommended. Specifications for an example minimum diode are given in *Figure 13*.

Breakdown Voltage	44–49V @ 1 mA
Maximum Leakage	1 μA @ 40V
Capacitance	300 pF @ BV
Maximum Clamp Voltage	64.5V @ 7.8A
Peak Non-Repetitive Pulse Power (REA Standard Exponential Pulse)	10 kW for 1 μs
Surge Current	70A for 1/120s

FIGURE 13. Key specifications for a recommended transient suppressor Z_T available from General Semiconductor, 2001 West Tenth Place, Tempe, AZ 85281, 602–968-3101, part no. SA40A

R_T

R_T acts as a voltage divider with Z_T, absorbing transient energy that attempts to pull the Carrier Input pin above 44V. Make the resistor a carbon composition 1/4W. When experiments discharging C_C charged to the peak-to-peak 620V AC thru a 1Ω power line were carried out, film resistors blew open-circuit.

D_T

This Schottky diode is placed in parallel with the CCT chip's substrate diode to pass the majority of the current drawn from ground when the Carrier Input or Carrier Output is pulled below ground by a larger-than-twice-the supply-swing on the tank. Note that Z_T is in parallel with the substrate diode, but is ineffective due to its high forward voltage drop and high diffusion capacitance caused by its low forward speed. Tests proved that a 1N5818 kept a receive-path functional with a 20X boost transmitter with a 7:1 transformer attempted to swing the receiver's Carrier I/O to ±100V (300 mA peak ground current in the receiver). Without D_T, the receiver momentarily stops functioning at a 100 times lower ground current.

This diode is not needed if the Carrier I/O never swings below ground. If your CCT systems all run on the same regulated voltage with all matched transformers and turns ratios, it is not needed. Otherwise, it is.

THE RECEIVER

The receiver and transmitter share components C_C, T_1, C_Q, R_T, Z_T, C_O, R_O, and peripheral supply and bias components that are not in need of change for RX mode operation. Values for the balance of the components are now found.

Line-Frequency Rejection

To use the ultimate sensitivity of the device, fully 110 dB of 115 V, 60 Hz attenuation is required between the line and the limiter amplifier output. Using the circuit topology of *Figure 4*, the combined attenuation of the C_C/T_1 highpass, the tuned transformer, and the bandpass filter attenuation of the limiter amplifier give far more line rejection than the above-stated minimum. However, if some other CCT line coupling circuit is used, line rejection will become important to the system designer.

Receiver input power supply rejection (PSRR) and common-mode rejection (CMRR) are one-in-the-same using the supply-referenced signal input of *Figure 4*. Ripple swings both differential inputs of the Norton amp. equally, while the single-ended input signal swings only the positive input. Overall PSRR consists of the input CMRR (set by the input stage component matching) and the ripple-frequency attenuation of the input amplifier bandpass response that passes carrier frequency but stops low frequencies. A typical 1% resistor and 1 mV n-p-n mirror offsets give 26 dB of attenuation, the bandpass gives 54 dB 120 Hz attenuation, for an overall 80 dB PSRR to allow tens of volts of ripple before impacting ultimate sensitivity.

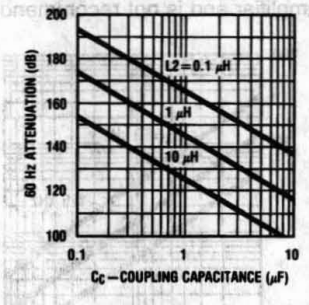
C_C

A value was chosen earlier. Knowing T_1's secondary inductance allows a check of LC line attenuation using *Figure 14*.

C_L

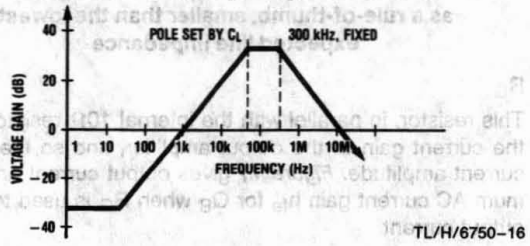
The Norton input limiter amplifier has a bandpass filter for enhanced receiver selectivity, noise immunity, and line frequency rejection. The nominal response curve for F_O = 50 kHz is shown in *Figure 15*. The 300 kHz pole is fixed. The 50 kHz pole is set by C_L's value. After C_L is found, the resulting line frequency attenuation is found for the bandpass filter.

Use *Figure 15* to find a C_L value given for F_O. The approximate line frequency attenuation of the bandpass filter may then be found in *Figure 16*. *Figure 15* returns a value for C_L 33% larger than nominal, giving a low frequency pole 33% low to allow for component tolerances.

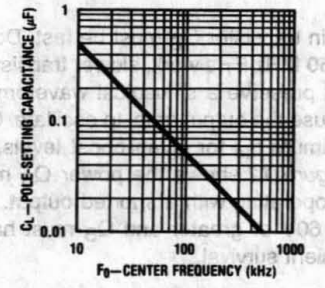


TL/H/6750–15

FIGURE 14. The 60 Hz line rejection of the highpass filter made up of C_C and T_1's line-side winding (neglecting capacitive coupling)



TL/H/6750–16



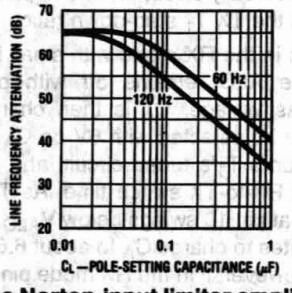
TL/H/6750–17

FIGURE 15. Given F_O, C_L is found. Also shown is the input amplifier's small signal amplitude response

Component Selection (Continued)

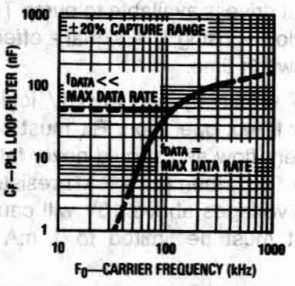
C_F and R_F

These phase-locked loop (PLL) loop filter components remove some of the noise and most of the $2F_O$ components present in the demodulated differential output voltage signal from the phase detector. They affect the PLL capture range, loop bandwidth, damping, and capture time. Because the PLL has an inherent loop pole due to the integrator action of the ICO (via C_O), the loop pole set by C_F and the zero set by R_F gives the loop filter a classical 2nd-order response.



TL/H/6750–18

FIGURE 16. The Norton-input limiter amplifier bandpass filter line-frequency signal attenuation given C_L



TL/H/6750–19

FIGURE 17. Find C_F given F_O. *Figure 19* gives the maximum data rate

No C_F and R_F give the most stable PLL with the fastest response. Large C_F's with a too-small R_F cause PLL loop instability leading to poor capture range and poor step response or oscillation.

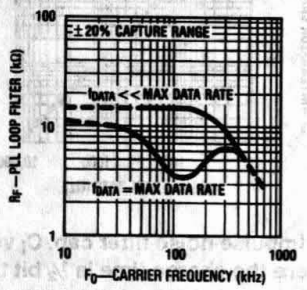
Calculation of C_F and R_F is quite difficult, involving not only the 2nd-order loop step response, but also the PLL nondominant poles, the tuned transformer stepped-frequency response, and the RC lowpass step response (for data rates approaching 1 kHz). C_F and R_F values are best found empirically. Tolerance is not critical. Component values are selected to give the best possible impulse noise rejection while preserving a ±20% capture range and wide stability margin. *Figures 17* and *18* give C_F and R_F values versus F_O, where "f_{DATA} << MAX DATA RATE" means that f_{DATA} should be less than the maximum data rate, in kHz, from *Figure 19* divided by 10.

Note that C_F and R_F are a function of data rate only for high data rates and are not plotted against data rate - as one might expect. The reason for this is important to understand if the CCT system designer wishes to find C_F and R_F empirically. Data signal is, loosely speaking, passed through the PLL loop and is therefore potentially attenuated if the loop bandwidth is on the order of the 3rd harmonic of the data rate, or less. Overall loop bandwidth is held as low as possible for maximum noise rejection while passing the data. Loop bandwidth is roughly proportional to the geometric mean of the unfiltered loop bandwidth and the filter pole set by C_F. Therefore, C_F is related to data rate. Unfortunately, the loop capture range falls to critically low values when large enough values of C_F are used to reduce loop bandwidth down to the 100's of Hz range, for low data rates. The obvious way out is to then reduce the unfiltered loop bandwidth. That bandwidth is approximately proportional to the value of C_O. For a fixed F_O, unfiltered loop bandwidth reduction requires a larger C_O and larger control current. With this chip, changing the control current is not allowed. So one is forced to choose a C_F/R_F combination with some minimum capture range, say ±20%, that is within some guardband from the point of loop instability. Happily, impulse noise tends to last only fractions of a millisecond so that the lack of low bandwidth loop response with low data rates is not a heavy penalty. As long as there is adequate capture range, the impulse noise filter performs admirably. Note that reducing F_O will reduce the no-filter loop bandwidth, and indeed the maximum data rate falls below the limit set by the RC lowpass filter as F_O falls below 100 kHz (*Figure 19*).

The tuned transformer characteristics will affect the demodulated data waveform more than C_F and R_F at low data rates. Tank Q and off-tuning will affect overshoot during the FSK frequency steps. This is a property of tuned circuits. The maximum data rate of *Figure 19* is measured from the receiver input to the Data Out and does not include the data bandwidth reducing effects of T_I.

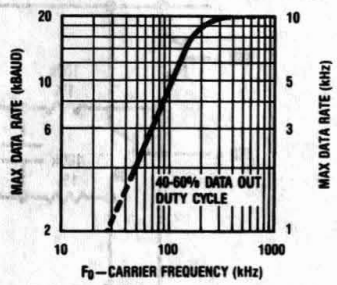
C_M

Capacitor C_M stores a voltage corresponding to a correction factor required to cancel the phase detector differential output DC offsets. The stored voltage is 5/6 of the DC offset plus some bias level of about 2.2 V. A large C_M value increases the time required to bias-up the receive path at the beginning of transmission. A large C_M does filter well and store its bias voltage long. Because of the initial random charge of C_M, the receiver must be given a data transition to charge to the proper bias voltage. Therefore, reducing C_M's value to one that may be charged in less than 2 bit-times will not save biasing time and is not recommended.



TL/H/6750–20

FIGURE 18. Find R_F given F_O with F_{DATA} a parameter

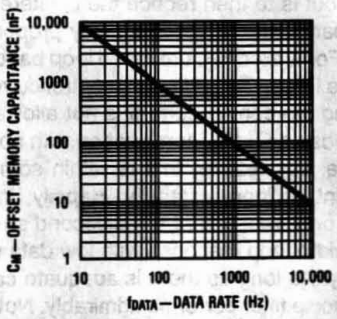


TL/H/6750–21

FIGURE 19. The maximum data rate versus F_O using loop filter components optimized for max. noise performance while retaining a min. ±20% capture range (large signal)

Use *Figure 20* to find C_M's value knowing f_{DATA}, assuming the standard 2 bit receive charge time is desired. The cap. value and TC are not critical, but the capacitor should have low leakage.

Component Selection (Continued)



TL/H/6750–22

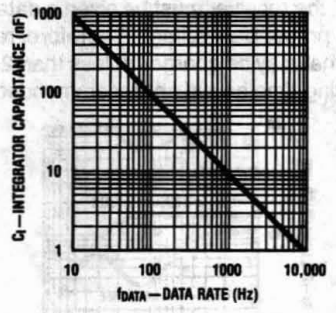
FIGURE 20. Size C_M assuming a 2 bit-time receive bias time

C_I

The impulse noise filter integrator capacitor C_I is used to disallow the passage of any pulse shorter than the integrator charge time. That charge time, set to a nominal ½ bit time, is the time required for a ±50 μA charge current to swing C_I over a 2 V_{BE} range. Charge time under worst case conditions must never be greater than a bit time since no signal could then pass. Using a ±10% capacitor, full junction temperature range, and full specified current range, a maximum nominal charge time of ½ bit is recommended. *Figure 21* gives C_I versus data rate under those conditions.

R_C

The collector pull-up resistor is sized to supply adequate pull-up current drive and speed while preserving adequate output low current drive.



TL/H/6750–24

FIGURE 21. Impulse noise filter cap. C_I versus F_{DATA} where the charge time is ½ bit time

Z_A

The 5.1V silicon zener diode Z_A is required when a short RX-to-TX switch-over time is needed at the same time that the chip is operating in the RX mode with a pin 10 input signal swing approaching or exceeding twice the supply voltage. Predominant causes of these large swings impinging on the RX input are: 1) a transmitter's supply voltage higher than the receiver's supply voltage, 2) a TX and RX pair that are electrically close, or, 3) a higher RX T_1 step-up turns ratio than the TX T_1 step-down ratio.

Normally, when in the RX mode with small incoming signal on pin 10, the ALC remains off with pin 7 at a 6V ($V_Z - 2V_{BE}$) bias voltage. C_A is then charged to 6V. TX mode may then be selected with 6V on C_A allowing 100% TX power to pump T_1's tuned circuit, and so the AC line, quickly for fast RX-to-TX switch time. As TX output swing increases so that pin 10 swings below V_{ALC} (4.7V typically), that ALC activates to charge C_A to about 6.6V to reduce TX output drive. However, if in the RX mode pin 10 ever swings below V_{ALC}, C_A will charge to above 6.6V. Now, when the TX mode is selected with C_A at 6.6V, somewhere from 0 to 100% TX output drive is available to pump T_1's tuned circuit resulting in a slower rising line signal - effectively reducing the RX-to-TX switch time.

Use a 5.1V Z_A driven by a 0 to 0.8V logic low signal to guarantee over-temp. operation. R_A must be in series with Z_A to limit current flow and should never fall below 1 kΩ. If R_A is less than 1 kΩ, then put a 2 kΩ resistor in series with Z_A. Logic high voltages above 10V will cause current flow into pin 7 that must be limited to 1 mA (with R_A or a series R).

Breadboarding Tips

During CCT system evaluation, some techniques listed below will simplify certain measurements.

— Use caution when working on this circuit - dangerous line voltages may be present.

— When evaluating PLL operation, offset cancel circuit operation, and loop filter values, use the filter of *Figure 22* to view the demodulated signal minus the $2F_O$ and noise components. This filter models the RC lowpass filter on chip.

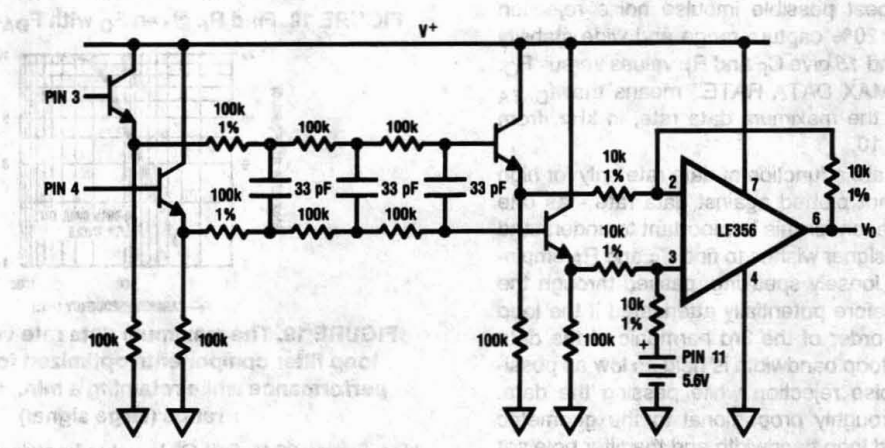


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FIGURE 22. Circuit to view the differential demodulated data signal, minus the noise and $2F_O$ components, conveniently with a single-ended gain-of-one output

Breadboarding Tips (Continued)

— When evaluating CCT system noise performance on a real power line, it is desirable to vary the signal amplitude to the receiver. This is not easy. An in-line line-proof L-pad is fine except that the line impedance is unknown and variable and so the L-pad will rarely match. Instead, the power output of a chip transmitter may be controlled using the circuit of *Figure 23*. This circuit controls the ALC.

— It is sometimes desirable to place impulse noise on the line. A simple light dimmer with a 100 W light bulb load produces representative impulse noise.

— Do not allow peak currents of over 1 A through the 5.6 V Zener. In other words, don't short charged capacitors into this low-impedance device. Take care not to momentarily short pins 10 and 11 - chip damage may result.

— *Figure 24* shows some typical signals beginning with serial data transmitted to received signal.

Tuning Procedure

This procedure applies to circuits similar to *Figure 4* LM1893 or LM2893 circuit.

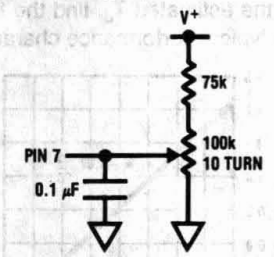
First, trim F_O by putting the chip in the TX mode, setting a logical high data input, and measuring the TX high frequency, 1.022 F_O, on the Carrier I/O using these steps:

1. Take pin 17 to a logic low.
2. Take pin 5 to a logic high.
3. Place a counter on pin 10.
4. Adjust R_O on pin 18 for $F = 1.022F_O$.

Second, the line transformer is tuned. The chip is placed in the TX mode, a resistive line load is connected to disable the ALC by reducing tank voltage swing below its limit. FSK data is then passed through the tank so that the tank envelope may be adjusted for equal amplitude for high and low data frequency.

1. Take pin 5 to a logic high.
2. Place a logic-level square wave at or below the receiver's maximum data rate on pin 17.
3. Temporarily place a 330 Ω resistor across the tank.
4. Place a scope on pin 10.
5. Adjust the transformer slug for the least envelope modulation.

In lieu of the 330 Ω resistive load, T_1 may be coupled to the power line to better simulate actual load and tank pull conditions during tank tuning. Alternatively, a passive network representing an average line impedance may be connected to the line side of T_1. The circuit of *Figure 23* should then be used to defeat the leveling effect of the ALC.



TL/H/6750–26

FIGURE 23. A means of transmitter output amplitude control is shown

Thermal Considerations

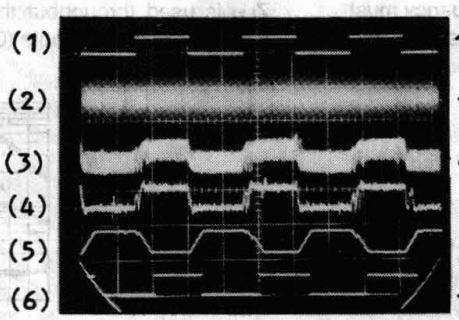
It is desirable to place the largest possible signal on the power line for maximum range, limited only by the chip power dissipation and maximum junction temperature T_J. The falling output power at elevated T_J allows a more optimal power output - high power at low T_J and lower power at high T_J for chip self-protection. However, it is still possible to exceed the maximum T_J within the specified ambient temperature limit (T_A = 85°C) under worst case conditions of 100% TX duty cyle, high supply, shorted load, poor PC board layout (with small copper foil area), and an above nominal current part. Under those conditions, a part may dissipate 2140 mW, reaching a T_J = 170°C worst-case (admittedly a rare occurrence). Proper system design includes the measurement or calculation of T_J max. to guarantee function under worst-case operation. Like all devices with failure modes modeled by the Arrhenius model, the high chip reliability is further enhanced by keeping the die temperature mercifully below the absolute maximum rating.

A direct method of measuring operating junction temperature is to measure the V_{BE} voltage on pin 18, which is always available under all operating modes. The graph of *Figure 25* may be used to find T_J, knowing V_{BE} at the operating point in question and V_{BE} at $T_A = T_J = 25°C$. V_{BE} is found by powering up a chip (in RX mode) that has been dissipating zero power at some T_A for some time and measuring V_{BE} in less than 1 s (for better than 5°C accuracy).

Alternately, T_J may be calculated using:

$$T_J = T_A + \theta_{JA}P_D \quad (1)$$

where θ_{JA} is 75°C/W for the plastic (N) package using a socket. That θ_{JA} value is for a high confidence level; nomi-



TL/H/6750–23

FIGURE 24. Oscillogram revealing signals at several important nodes under weak signal (0.5 mV_{RMS}) conditions with SCR spikes on an otherwise quiet 115 V, 60 Hz power line. The signals are: 1) transmitted data, 2) RX carrier on the tuned transformer, 3) demodulated signal from the PLL after passing thru circuit of *Figure 22*, 4) signal after RC lowpass, 5) data at impulse noise filter integrator, and 6) received data. Horizontal scale is 10 ms per div.

Thermal Considerations (Continued)

nal θ_{JA} for an N package is 60°C/W, lower with good PC board layout. Since P_D is a relatively strong function of T_J, an iterative solution process starting with an initial guess for T_J is used. With the estimated T_J, find the total supply current found in the typical performance characteristics.

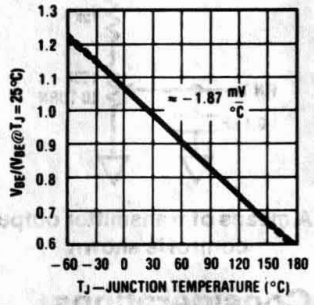


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FIGURE 25. T_J may be found by using the temperature coefficient of pin 18 V_{BE} if V_{BE} is known at 25°C

Transmit-To-Receive Switch-Over Time

An important figure-of-merit for a half-duplex CCT link, affecting effective data rate, is the TX-to-RX switch time T_{TR}. Using the recommended component values gives this part a nominal 2 bit-time (1 bit time = $1/[2f_{DATA}]$) over a wide range of operating conditions, where the receiver requires 1 data transition. T_{TR} cannot be decreased significantly but does increase as noise filtering, especially via C_M, is increased. Impulse noise at switch, signals near the limiting sensitivity, poor F_O match between receiver and transmitter because of poor trim or worst-case conditions, and the statistical nature of PLL signal acquisition may all contribute to increase T_{TR} to possibly 4 bit-times.

T_{TR} is lower when a pair of LM1893's handshake rapidly. The receiver was designed to "remember" the RX-mode DC operating points on C_M and C_F while in the TX mode. Under noisy worst case conditions, C_M will discharge to the point of false operation after 35 bit-times in the TX mode (1400 bit times with no noise and a nominal part, f_{DATA} = 180 Hz). T_{TR} is about 0.8 ms (proportional to the selected F_O) plus ½ bit-time.

The major components of T_{TR} are described below for a nominal 125 kHz F_O, 180 Hz f_{DATA}, lightly-loaded tank with a Q of 20, and the circuit of *Figure 4*. The remote CCT has been operating in the TX mode with a 26.6 V_{PP} tank swing and is now selected as a receiver. An incoming signal requiring the ultimate receiver sensitivity immediately is placed on the line.

First, the tank stored energy at the transmit frequency must decay to a level below the 2.8 mV_{PP} swing caused by the 0.14 mV_{RMS} incoming line signal containing the information to be received.

$$\text{decay time} = \frac{Q}{\pi F_O} \ln\left(\frac{V_1}{V_O}\right) =$$

$$\frac{20}{\pi \times 125\,000} \ln\left(\frac{26.6}{0.0028}\right) = 0.466 \text{ ms} \qquad (2)$$

That is 0.47 ms of delay (proportional to $1/F_O$ and Q).

Second, the PLL must acquire the signal; it must lock and settle. Acquisition time is statistical and may take any length of time, but average acquisition time depends on the loop filter components C_F and R_F and the difference in center frequencies, ΔF_O, of the TX/RX pair. Using the recommended C_F and R_F (47 nF and 6.2 kΩ) with a ±4.4% ΔF_O (a ± 100 mV DC offset on C_F and R_F), lock was measured to take less than 50 cycles of F_O. That is a 0.40 ms delay (proportional to $1/F_O$).

Acquisition is incomplete until the second order PLL loop settles. For the above-mentioned C_F and R_F, the loop natural frequency F_N and damping factor are found to be 2.3 kHz and 1.0 respectively. Settling to within ±25 mV of the ±100 mV DC offset change requires 2.7 periods of F_N, or 1.2 ms (a function of C_F and R_F).

Third, the RC lowpass filter introduces a 0.12 ms delay.

Fourth, C_M must charge up to ±(5/6)100 = 83 mV depending on the polarity of F_O. Borderline data squaring with zero noise immunity is possible with only ±(5/6) 50 mV of charging. C_M charge current is an asymptotic function approximated by assuming a 50 μA charge current and the full 83 mV charge voltage. C_M charge time is then 1.7 ms (proportional to $1/f_{DATA}$).

Fifth, the impulse noise filter adds a ½ bit-time delay. Total T_{TR} is 3.9 ms plus ½ bit-time for a total of 1.9 bit-times at 360 Baud.

Receive-To-Transmit Switch-Over Time

Assume the chip has been in the RX mode and the TX mode is now selected. In less than 10 μs, full output current is exponentially building tank swing. 50% of full swing is achieved in less than 10 cycles - or under 80 μs at 125 kHz. In the same 10 μs that the output amp went on, the phase detector and loop filter are disconnected and the modulator input is enabled. FSK modulation is produced in 10 μs after switching to TX mode.

Power Line Impedance

Irrespective of how wide the limits on power line impedance Z_L are placed, there are no guarantees. However, since the CCT design requires an estimate of the lowest expected line impedance Z_{LN} encountered for the most efficient transmitter-to-line coupling, line impedance should be measured and Z_L limits fixed to a given confidence level. Reasonable values for T_1 turns ratio, loaded Q, and tank resonant frequency pull F_Q may be found to enable a CCT system design that functions with the overwhelming majority of power lines.

A limited sampling of Z_L was made, during the LM1893 design, of residential and commercial 115V 60 Hz power line. Data was also drawn from the research of Nicholson and Malack (reference 1), among others, to produce *Figures 26* and *27*. All measured impedances are contained within the shaded portions of *Figure 27*. A nominal 3.5, 7.0 and 14 Ω Z_{LN} is used throughout the application information with a nominal 45° phase angle (0° is sometimes used for simplicity).

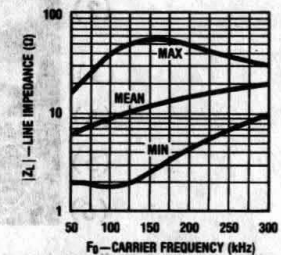

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FIGURE 26. Measured line impedance range for residential and commercial 115V, 60 Hz lines

Power Line Impedance (Continued)

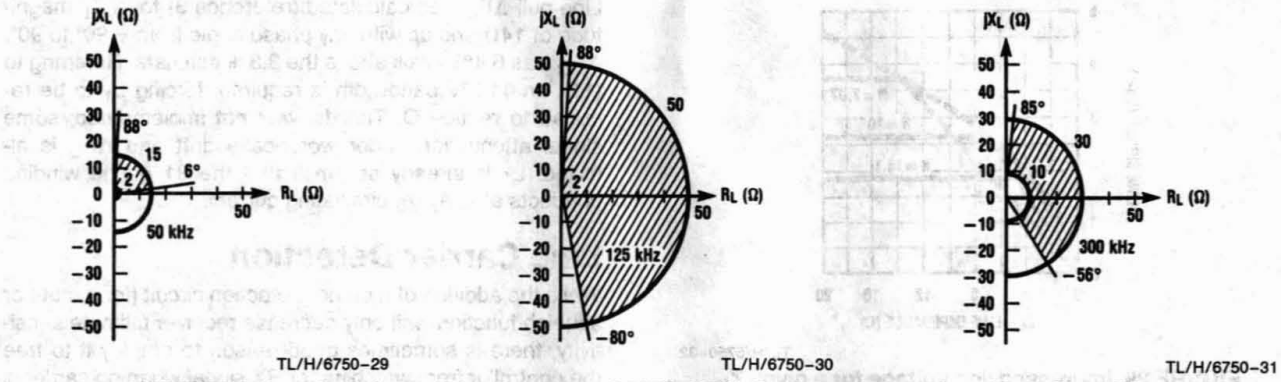

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FIGURE 27. Complex-plane plots of measured 115V, 60 Hz line impedance where $Z_L = R_L + jX_L$

Power Line Attenuation

The wiring in most US buildings is a flat 3 conductor cable called Amerflex, BX, or Romex. All referenced line impedances refer to hot-to-neutral impedances with a grounded center conductor. The cable has a 100 Ω characteristic impedance, a 125 kHz quarter-wavelength of 600 m (250 m at 300 kHz), and a measured 7 dB attenuation for a 50 m run with a 10 Ω termination. Generally, line loads may be treated as lumped impedances. Instrument line cords exhibit about 0.7 μH and 30 pF per meter.

Limited tests of CCT link range using this chip show extensive coverage while remaining on one phase of a distribution transformer (100's of m), with link failure often occuring across transformer phases or through transformers unless coupling networks are utilized. Total line attenuation allowed from full signal to limiting sensitivity is more than 70 dB. Typically, signal is coupled across transformer phases by parasitic winding capacitance, typically giving 40 dB attenuation between phased 115 V windings. Coupling capacitors may be installed for improved link operation across phases. Power factor correcting capacitor banks on industrial lines or filter capacitors across the power lines of some electronic gear short carrier signal and should be isolated with inductors. Increasing range is sometimes accomplished by electing to install the isolating inductors (*Figure 28*) and coupling capacitors, as well as by electing to use the boost option. Frequency translating or time division multiplexed repeaters will also increase range.

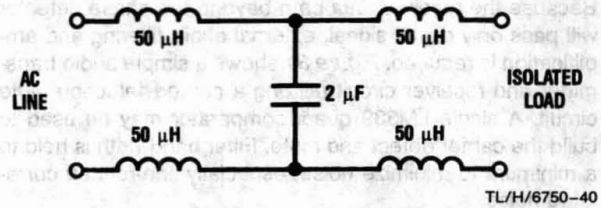

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FIGURE 28. An isolation network to prevent: 1) noise from some device from polluting the AC line, and 2) to stop some low impedance device (measured at F_O) from shorting carrier signal. Component values given as an example for $F_O = 125$ kHz on residential power lines

The Coupling Transformer

The design arrived at for T_1 is the result of an unhappy compromise - but a workable one. The goals of 1) building T_1 with a stable resonant frequency, F_Q, that is little affected by the de-tuning effect of the line impedance Z_L, and of 2) building a tightly line-coupled transformer for transmitted carrier with loose coupling for transients, are somewhat mutually exclusive. The tradeoffs are exposed in the following example for the CCT designer attempting a new boost-capable, or different core, transformer design.

The compromises are eased by separating the TX output and RX input in the LM2893. An untuned TX coupling transformer with only core coupling (not air-coupled solenoid windings) would employ a high permeability, high magnetic field, low loss, square saturating, toroidal core. The resonant RX path would be isolated from line-pull problems by a unilateral amplifier that operates at line voltages with much more than 110 dB of dynamic range, or by a capacitively coupled pulse transformer driving a unilateral amplifier and filter, for increased selectivity. See the LM2893-specific applications section.

For a LM1893-style transformer application, first, choose the turns ratio N based on an estimated lowest Z_L likely encountered, Z_{LN}. *Figure 29* shows graphically how N affects line signal. N should be as large as possible to drive Z_{LN} with full signal. If T_1 has an unloaded Q, Q_U, of well less than 35, a guess of N somewhat high should be used and later checked for accuracy. The recommended transformers have secondary taps giving a choice of N = 7.07, 10, and 14.1 (nominally) for driving Z_{LN}'s of 14, 7.0, and 3.5 Ω respectively (at $T_J = 25°C$, $V+ = 18V$, and $Q_U = 35$).

The resonating inductance of the tuned primary, L_1, is sought. Note that, while standard transformer design gives a transformer self-inductance with an impedance at operating frequency well above load impedance, the tuned transformer requires a low L_1 for adequate Q_U and minimum line pull. Result: relatively poor mutual coupling.

$$L_1 = \frac{R}{2\pi F_O Q} \quad (3)$$

It is known that resonant frequency $F_Q = F_O$ and some minimum bandwidth, or maximum Q, will be required to pass signal under full load conditions.

$$L_1 = \frac{R_Q \parallel |Z_{LN}|'}{2\pi F_O Q_L} \quad (4)$$

$|Z_{LN}|'$ is the reflected Z_{LN}, Q_L is the loaded Q, and parallel resistance R_Q models all transformer losses and sets Q_O.

$R_Q \parallel |Z_{LN}|'$ is found knowing that it absorbs full rated power.

The Coupling Transformer (Continued)

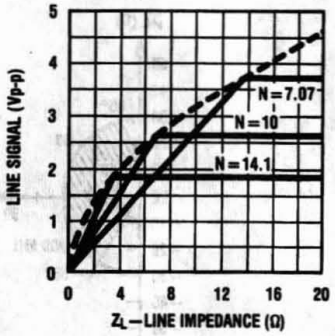

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FIGURE 29. Impressed line voltage for a given Z_L for each of the 3 taps available on the recommended transformers

$$P_O = I_O V_O = \frac{I_{OPP}}{2\sqrt{2}}\left[\frac{2(-V_{ALC}+V_+)}{2\sqrt{2}}\right] = \frac{(-4.7+V_+)I_O}{4} \quad (5)$$

where I_O is in amps peak-to-peak at an elevated T_J

$$P_O = \frac{(18 - 4.7)\,0.06}{4} = 0.200\ W \quad (6)$$

$$R_Q \| |Z_{LN}|' = \frac{V_O^2}{P_O} = \frac{(-V_{ALC} + V_+)\sqrt{2}}{I_O} = 442\ \Omega \quad (7)$$

R_Q is found using Z_{LN} and the value for N found when assuming $Q_U = 35$.

$$|Z_{LN}|' = N^2 Z_{LN} = (7.07)^2\,13.9 = 695\ \Omega \quad (8)$$

$$R_Q = \frac{1}{\frac{1}{R_Q \| |Z_{LN}|'} - \frac{1}{|Z_{LN}|'}} = \frac{1}{\frac{1}{442} - \frac{1}{695}} = 1210\ \Omega \quad (9)$$

$$R_{QS} = \frac{R_Q}{1 + Q_U^2} = \frac{1210}{1 + 35^2} = 1\ \Omega \quad (10)$$

Only Q_L remains to be found to calculate L_1. Q_L is related to the −3 dB (half-power) bandwidth by

$$Q_L = \frac{1}{BW\ (\%\ of\ F_O)} \quad (11)$$

An iterative solution is forced where line pull, ΔF_Q, must be guessed to find Q_L and L_1. L_1 is then used to check the line pull guess; a large error requires a new guess. Try a BW of 8.7% - that is 4.4% for deviation, 1% for TC of F_O, and 3.3% for ΔF_Q - giving $Q_L = 11.5$.

$$L_1 = \frac{442}{2\pi \times 125\,000 \times 11.5} = 49.0\ \mu H \quad (12)$$

Knowing the core inductance per turn, L, and L_1, the number of turns is found.

$$T_1 = \sqrt{\frac{L_1}{L}} = \sqrt{\frac{49.0\ \mu H}{20\ nH/T}} = 49\ \tfrac{1}{2}\ turns \quad (13)$$

T is normally an integer, but these transformers require so few turns that half-turns are specified, remembering that the remaining ½ turn is completed on the P.C. board and is loosely coupled. The secondary turns are calculated

$$T_2 = \frac{T_1}{N} = \frac{49.5}{7.07} = 7.00 = 7\ turns \quad (15)$$

giving an L_2 of 0.98 μH. Note that the recommended 125 kHz transformer mirrors these specifications. The resonating capacitor is

$$C_Q = \frac{1}{(2\pi F_Q)^2 L_1} = 33.1 \times 10^{-9} = 33\ nF \quad (16)$$

Line pull ΔF_Q was calculated (reference 3) for a Z_L magnitude of 14Ω and up with any phase angle from −90° to 90°. ΔF_Q was 6.4% - well above the 3.3% estimate. Referring to (11), an 11.8% bandwidth is required, forcing L_1 to be reduced to reduce Q. That fix was not implemented; some signal attenuation under worst-case drift and ΔF_Q is allowed. L_1 is already so small that the 31 gauge winding conducts a ¼ A_{RMS} circulating current.

Line Carrier Detection

While the addition of a carrier detection circuit (for a mute or squelch function) will only decrease receiver ultimate sensitivity, there is sometimes good reason to employ it to free the controller from watching for RX signal when no carrier is incoming, or to employ it to reduce the probability of line collisions (when multiple transmitters operate simultaneously to cause one or more transmissions to fail). Unless the detector is heavily filtered or uses a high carrier amplitude threshold, there will be false outputs that force the controller to have Data Out data checking capability just as is required when using no carrier detector. If false triggering is minimized, the probability of line collisions is increased due to the inability to sense low carrier amplitudes and because of sense delay. The property of the LM1893 to change output state infrequently (although the polarity is undefined) when in the RX mode, with no incoming carrier, reduces the desire to implement carrier detection and preserves the full ultimate sensitivity. Also, many impulse-noise insensitive transmission schemes, like handshaking, are easily modified to recover from line collisions.

Regarding this, it should be stated that for very complicated industrial systems with long signal runs and high line noise levels, it is probably wise to use a protocol which is inherently collision free so that no carrier detect hardware or software is needed. A token passing protocol is an example of such a system.

Figure 30 shows a low cost carrier amplitude detection circuit.

Audio Transmission

The LM1893 is designed to allow analog data transmission and reception. Base-band audio-bandwidth signals FM modulate the carrier passing through the tuned transformer (placing a limit on the usable percent modulation) onto the power line to be linearly demodulated by the receiver PLL. Because the receiver data path beyond the phase detector will pass only digital signal, external audio filtering and amplification is required. *Figure 31* shows a simple audio transmitter and receiver circuit utilizing a carrier detection mute circuit. A single LM339 quad. comparator may be used to build the carrier detect and mute. Filter bandwidth is held to a minimum to minimize noise, especially line-related correlated noise.

Communication and System Protocols

The development of communication and system protocols has historically been the single most time consuming element in design of carrier current systems. The protocols are defined as the following:

1. *Communication protocol*: a software method of encoding and decoding data that remains constant for every transmis-

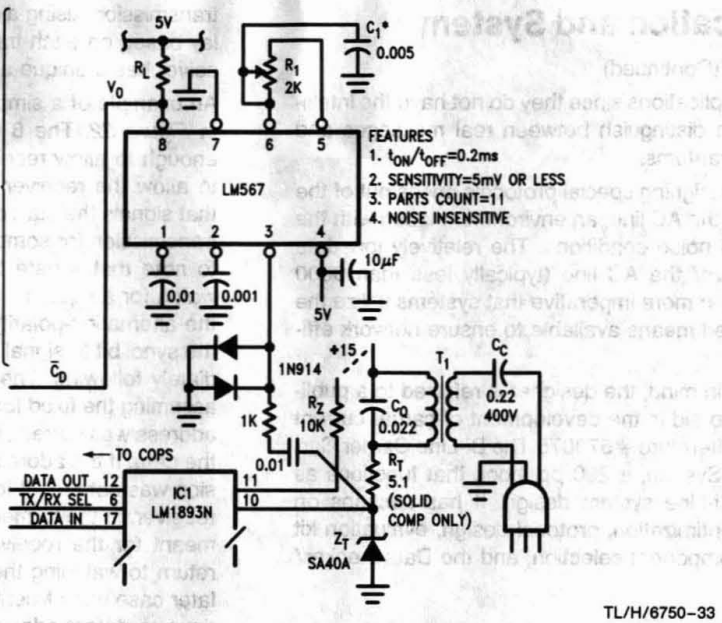

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FIGURE 30. A simple carrier amplitude detector with output low when carrier is detected

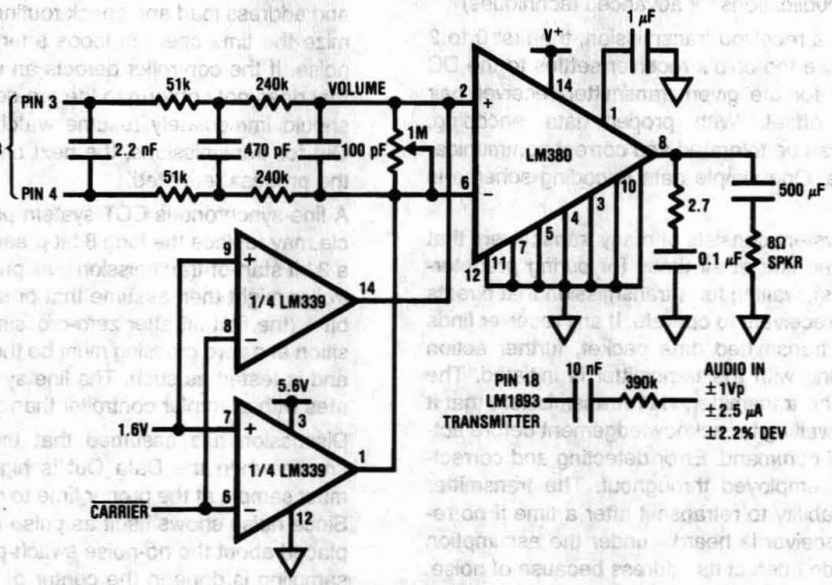

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FIGURE 31. A simple linear analog audio transmitter and receiver are shown. The carrier and 1.6V inputs are derived from the carrier detector of *Figure 30*. The remaining 2 LM339 comparators may be used to build the carrier detector circuit.

Communication and System Protocols (Continued)

sion in a system. Its first purpose is to put data in a baseband digital form that is more easily recognized as a real message at the receive end. Secondly, it incorporates encoding techniques to ensure that noise induced errors do not easily occur; and when they do, they can always be detected. Lastly, the software algorithms that are used on the receive end to decode incoming data prevent the reception of noise induced "phantom" messages, and insure the recovery of real messages from an incoming bit stream that has been altered by noise.

2. *System protocol*: the manner in which messages are coordinated between nodes in a system. Its first purpose is to ensure message retransmission to correct errors (handshake). Secondly it coordinates messages for maximum utilization and efficiency on the network. Lastly, it ensures that messages do not collide on the network. Common system protocols include master-slave, carrier detect multiple access, and token passing. Token passing and master slave have been found to be the most useful since they are inherently collision free.

Both protocols usually reside as software in a single microcontroller that is connected to the LM1893/2893 I/O. In any case, some sort of intelligence is needed to process incoming and outgoing messages. UARTs have no usefulness in

Communication and System Protocols (Continued)

carrier current applications since they do not have the intelligence needed to distinguish between real messages and noise induced phantoms.

The difficulty in designing special protocols arises out of the special nature of the AC line, an environment laden with the worst imaginable noise conditions. The relatively low data rates possible over the AC line (typically less than 9600 baud) make it even more imperative that systems utilize the most sophisticated means available to ensure network efficiency.

With these facts in mind, the designer is referred to a publication intended to aid in the development of carrier current systems. This is literature #570075 The Bi-Line Carrier Current Networking System, a 200 pp. book that functions as the "bible" of Bi-Line system design. It has sections on LM1893 circuit optimization, protocol design, evaluation kit usage, critical component selection, and the Datachecker/DTS case study.

Basic Data Encoding (please refer to the previously mentioned publications for advanced techniques)

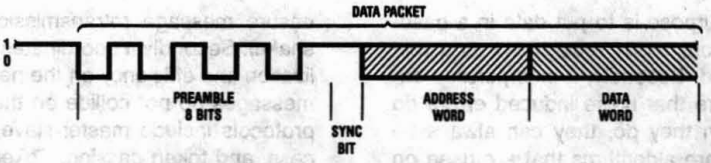
At the beginning of a received transmission, the first 0 to 2 bits may be lost while the chip's receiver settles to the DC bias point required for the given transmitter/receiver pair carrier frequency offset. With proper data encoding, dropped start bits can be tolerated and correct communication can take place. One simple data encoding scheme is now discussed.

Generally, a CCT system consists of many transceivers that normally listen to the line at all times (or during predetermined time windows), waiting for a transmission that directs one or more of the receivers to operate. If any receiver finds its address in the transmitted data packet, further action such as handshaking with the transmitter is initiated. The receiver might tell the transmitter, via retransmission, that it received this data, waiting for acknowledgement before acting on the received command. Error detecting and correcting codes may be employed throughout. The transmitter must have the capability to retransmit after a time if no response from the receiver is heard - under the assumption that the receiver didn't detect its address because of noise, or that the response was missed because of noise or a line collision. (A line collision happens when more than 1 transmitter operates at one time - causing one or more of the communications to fail). After many re-transmissions the transmitter might choose to give up. Collision recovery is achieved by waiting some variable amount of time before retransmission, using a random number of bits delay or a delay based on each transmitter's address, since each transceiver has a unique address.

An example of a simple transmission data packet is shown in *Figure 32*. The 8 bit 50% duty-cycle preamble is long enough to allow receiver biasing with enough bits left over to allow the receiver controller to detect the square-wave that signals the start of a transmission. If there had been no transmission for some time, the receiver would simply need to note that a data transition had occurred and begin its watch for a square-wave. If the receive controller detected the alternating-polarity data square-wave it would then use the sync. bit to signal that the address and data were immediately following. The address data would then be loaded, assuming the fixed format, and tested against its own. If the address was correct, the receiver would then load and store the data. If the address was not correct, either the transmission was not meant for this receiver or noise has fooled the receiver. In the former case, when the transmission was not meant for the receiver, the controller should immediately return to watching the incoming data for its address. If the later case were true, then the receive controller would continue to detect edges, tieing itself up by loading false data and being forced to handshake. The square-wave detection and address load and check routines should be fast to minimize the time spent in loops after being false-triggered by noise. If the controller detects an error (a received data bit that does not conform to the pre-defined encoding format) it should immediately resume watching the LM1893's Data Out for transmissions, the next bit would be shifted in and the process repeated.

A line-synchronous CCT system passing 3 bits per half-cycle may replace the long 8 bit preamble and sync pulse with a 2 bit start-of-transmission bias preamble. The receive controller might then assume that preamble always starts after bit 1 (the first bit after zero-crossing) so that any data transition at a zero crossing must be the start of the address bits and is tested as such. The line synchronous receiver operates with a simpler controller than an asynchronous system.

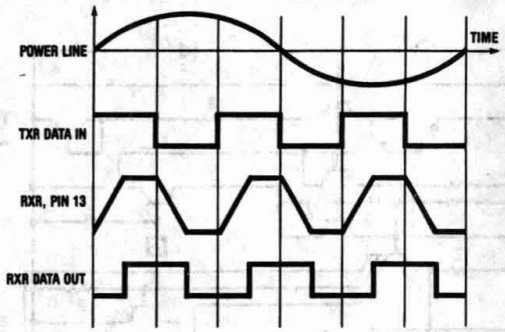
Discussion has assumed that the controller has always known when the Data Out is high or low. The controller must sample at the proper time to check the Data Out state. Since noise shows itself as pulse width jitter, symmetrically placed about the no-noise switch-points, optimum Data Out sampling is done in the center of the received data pulse. The receive data path has a time delay that, at low data rates, is dominated by the impulse noise filter integrator and is nominally ½ bit. At a 2 kHz data rate, an additional delay of approximately $1/_{10}$ bit is added because of the cumulative delay of the remainder of the receiver. *Figure 33* shows that Data Out sampling occurs conveniently at the transmitted



TL/H/6750–35

FIGURE 32. A simple encoded data packet, generated by the transmit controller is shown. The horizontal axis is time where 1 bit time is $1/(2f_{DATA})$

Basic Data Encoding (Continued)



TL/H/6750–36

FIGURE 33. Operating waveforms of a line-synchronized transceiver pair are shown. The diagram shows how the transmitted data transitions may be used as received data sampling points

data edges for the line synchronous data transmission scheme mentioned in the previous paragraph. With the asynchronous system suggested, the receive controller must sample the Data Out pin often to determine, with several bits of accuracy, where the square-wave data transitions take place, average their positions assuming a known data rate, and calculate where the center of the data bits are and will continue to be as the address and data are read. A long preamble is helpful. Software that continuously updates the center-of-bit time estimate, as address and data are received, works even better. Alternatively, a coding scheme employing an embedded clock can be used.

LM2893 Application Hints

The LM2893 is intended for advanced applications where special circuitry is used in the transmit and receive paths. The LM2893 makes this possible by featuring separate transmit output and receive input pins.

Examples of enhancements that can be added to the basic LM1893/2893 circuit include separate transmit and receive windings on the coupling transformer, high quality ceramic or LC filters in the receive path, and simple impulse noise blanking circuits.

In many applications, the additional performance to be gained outweighs the extra cost of the additional circuitry. More than likely, high performance industrial applications such as building energy management will fit into this category, since they require the utmost in reliability.

Because of the specialized nature of individual LM2893 applications, it is not possible to give one circuit that will satisfy all requirements for performance and cost effectiveness. Therefore no specific application examples will be given. Instead the subsequent text describes in general terms the types of circuits that can be used to increase performance along with their advantages and disadvantages. It is intended to be a springboard for ideas.

LM2893 COUPLING NETWORKS

The main disadvantages of the typical LM1893 coupling network are that it functions as the bandpass filter, has loose coupling between primary and secondary, and has a single secondary. The LM1893 coupling network was designed this way mainly because of the restraint that the carrier input and output are tied together.

Because the coupling transformer is used as a filter, the LM1893 circuit is susceptible to pulling of the center frequency under conditions of changing line impedances or when several LM1893 circuits are close in proximity on the AC line. Because the tuned transformer has a high value of "Q", ringing also occurs in the presence of impulsive noise. This ringing occurs at the center frequency and increases the error rate of transmissions, especially at relatively high data rates (>2000 baud). Because it is the only tuned circuit in the system, the selectivity characteristics leave a lot to be desired.

The LM2893, having separate receive input and transmit output pins, removes the limitations on coupling transformer design, allowing the design of circuits devoid of the previous limitations.

The first enhancement that can be made with the LM2893 circuit is the use of a high permeability ferrite toroid for line coupling along with a separate filter. The transformer would be of broadband design (untuned) with two secondaries, one for coupling to the transmit output and one for coupling to the receive input. This allows impedance matching of both the transmitter and receiver, with the result of quite a bit more receive sensitivity.

Because of the increased signal and separate receive signal path, a 3 or 6 db pad can be used before the selective stages to eliminate pulling of the center frequency due to changes in line impedance.

Another advantage of the toroidal transformer is that it can be designed for use at very low line impedances due to its inherent tight coupling.

SEPARATE FILTER

Because of the separate receive path of the LM2893, a relatively high quality bandpass filter can be used for selectivity. Inexpensive ceramic filters are available that have bandpass and center frequency characteristics compatible with carrier current operation. Futhermore, the use of these filters allows multichannel operation, previously made difficult by the single tuned network of the LM1893. These filters are easily cascaded for even more off-frequency rejection. If the pad is added before the filter, there will be negligible pulling due to changes in line impedance reflected through the coupling transformer.

Alternatively, a Butterworth/Chebyshev bandpass LC filter or an active filter can be used in place of the ceramic filter.

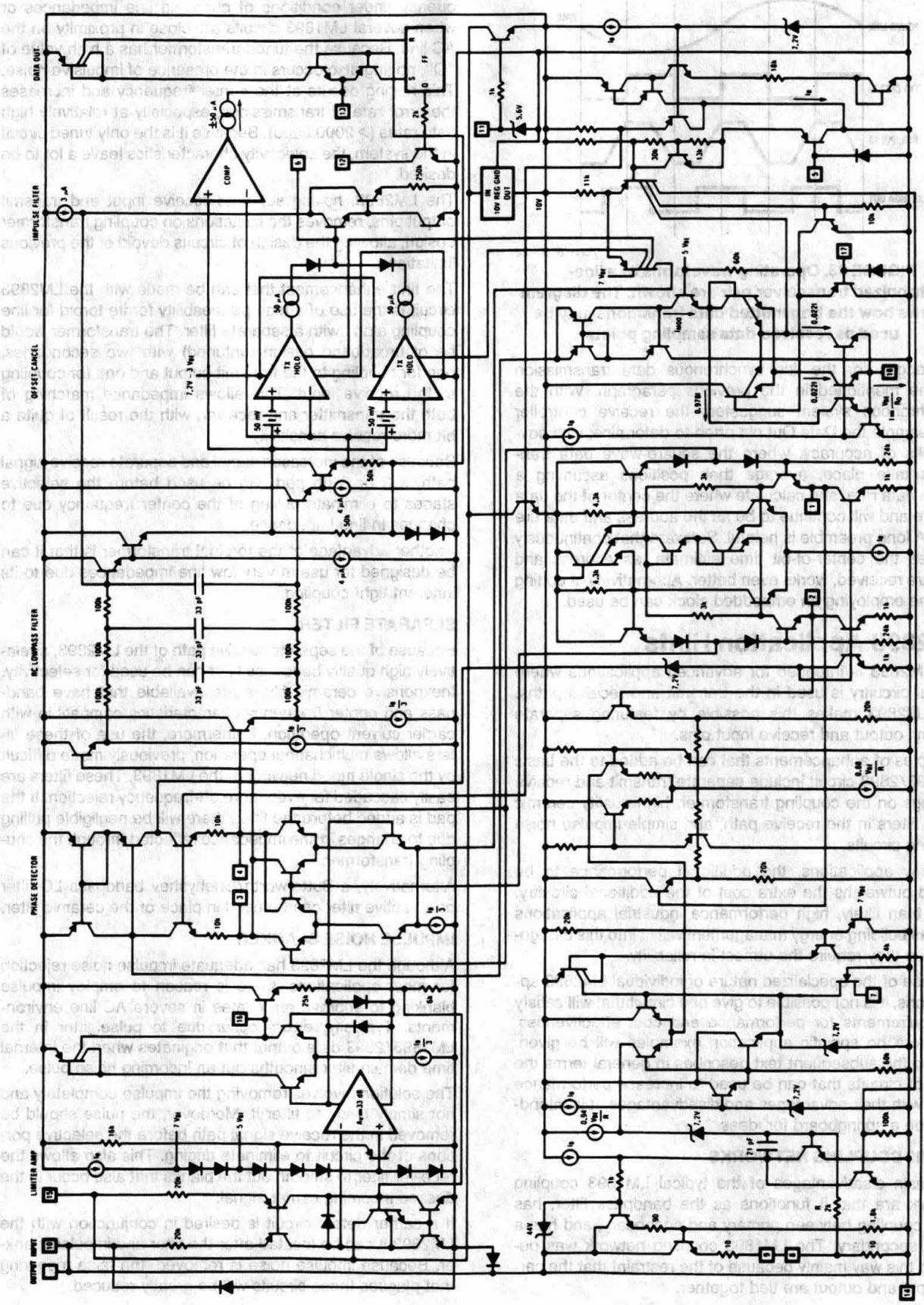
IMPULSE NOISE BLANKER

Although the LM2893 has adequate impulse noise rejection for most applications, there is reason to employ impulse blanking to improve error rates in severe AC line environments. Typically, errors occur due to pulse jitter in the LM1893/2893 data output that originates when the internal time domain filter smooths out an incoming noise pulse.

The solution involves removing the impulse completely and not simply trying to filter it. Moreover, the pulse should be removed in the receive signal path before the selective portions of the circuit to eliminate ringing. This also allows the receiver filter to smooth out the blanks that also occur in the desired incoming carrier signal.

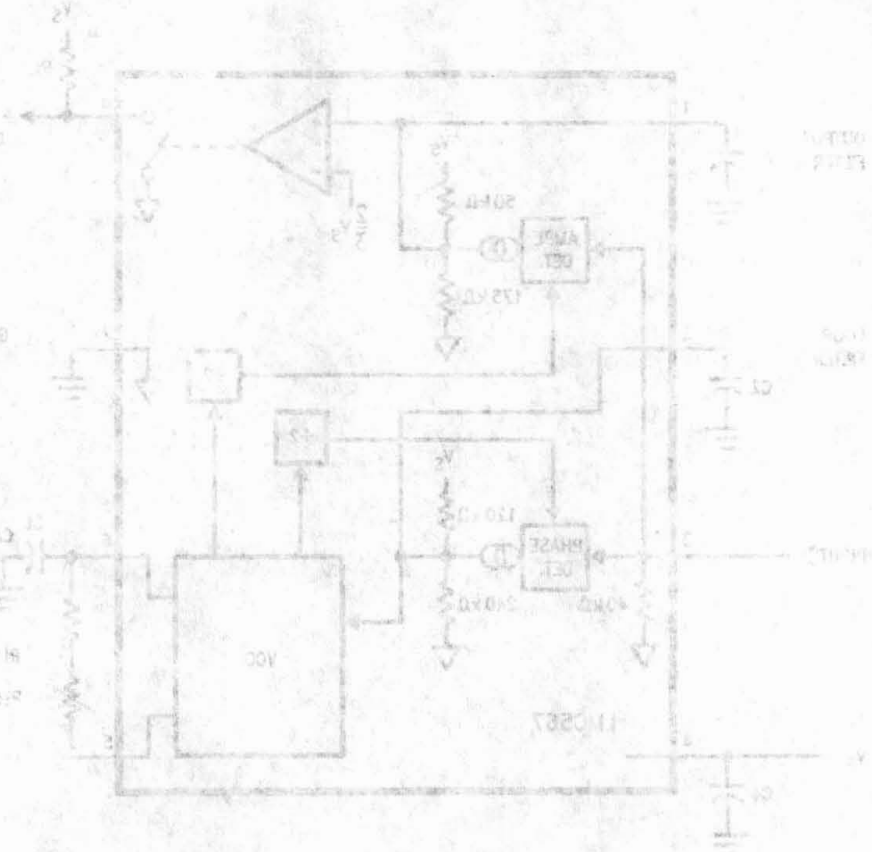
If a carrier detect circuit is desired in conjunction with the LM2893 it can be located after the filter and impulse blanker. Because impulse noise is removed, the false triggering that plagues these circuits will be greatly reduced.

Simplified Schematic



References

1. Nicholson, J.R. and J.A. Malack; "RF Impedance of Power Lines and Line Impedance Stabilization Network in Conducted Interference Measurements;" IEEE Transactions on Electromagnetic Compatibility; May 1973; (line impedance data)
2. Southwick, R.A.; "Impedance Characteristics of Single-Phase Power Lines;" Conference Rec.; 1973 IEEE Int. Symp. on Electromagnetic Compatibility; (line impedance data)
3. Hayt, William H. Jr. and Jack E. Kemmerly; "Engineering Circuit Analysis;" McGraw-Hill Books; 1971; pp. 447–453; (linear transformer reflected impedance)
4. FCC, "Notice of Proposed Rule Making," Docket 20780, adopted Apr. 14, 1976, (Proposed regulation)
5. Monticelli, Dennis M. and Michael E. Wright; "A Carrier Current Transceiver IC for Data Transmission Over the AC Power Lines;" IEEE J. Solid-State Circuits; vol. SC-17; Dec. 1982; pp. 1158-1165; (LM1893 circuit description)
6. Lee, Mitchell; "A New Carrier Current Transceiver IC;" IEEE Trans. on Consumer Electronics; vol. CE-28; Aug. 1982; pp. 409–414; (Application of LM1893)



National Semiconductor

LMC567 Low Power Tone Decoder

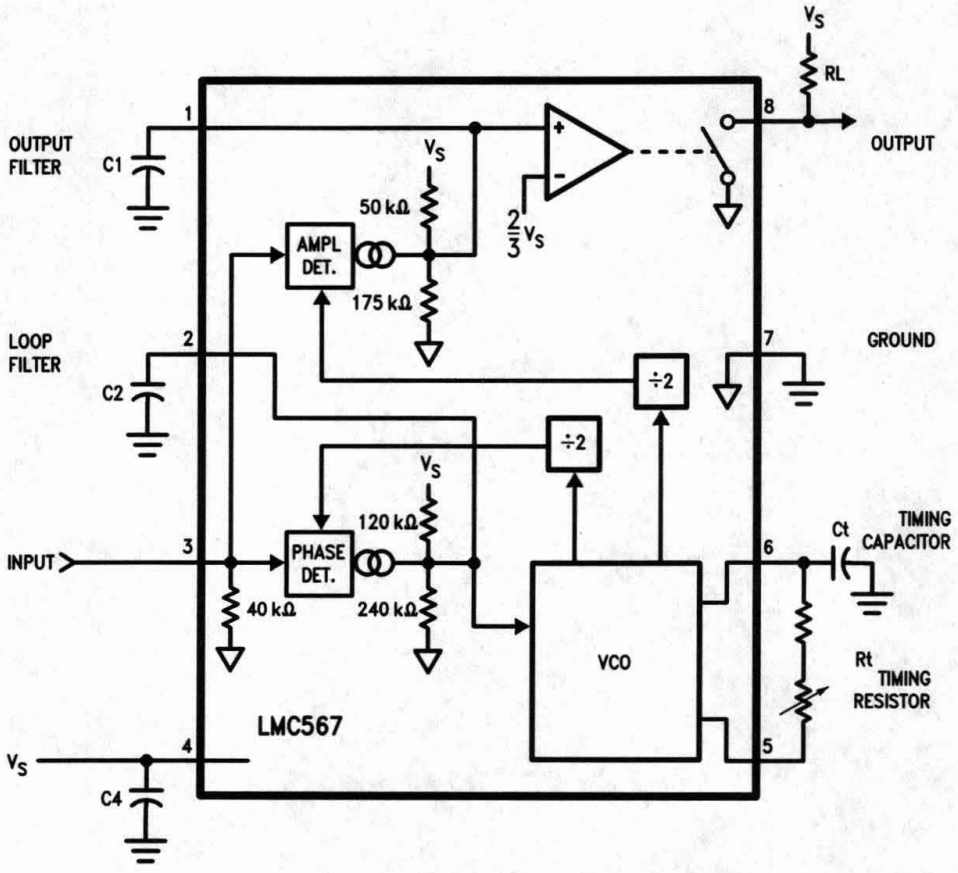
General Description

The LMC567 is a low power general purpose LMCMOS™ tone decoder which is functionally similar to the industry standard LM567. It consists of a twice frequency voltage-controlled oscillator (VCO) and quadrature dividers which establish the reference signals for phase and amplitude detectors. The phase detector and VCO form a phase-locked loop (PLL) which locks to an input signal frequency which is within the control range of the VCO. When the PLL is locked and the input signal amplitude exceeds an internally pre-set threshold, a switch to ground is activated on the output pin. External components set up the oscillator to run at twice the input frequency and determine the phase and amplitude filter time constants.

Features

- Functionally similar to LM567
- 2V to 9V supply voltage range
- Low supply current drain
- No increase in current with output activated
- Operates to 500 kHz input frequency
- High oscillator stability
- Ground-referenced input
- Hysteresis added to amplitude comparator
- Out-of-band signals and noise rejected
- 20 mA output current capability

Block Diagram (with External Components)



TL/H/8670–1

Order Number LMC567CM or LMC567CN
See NS Package Number M08A or N08E

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Input Voltage, Pin 3	2 V_{p-p}
Supply Voltage, Pin 4	10V
Output Voltage, Pin 8	13V
Voltage at All Other Pins	Vs to Gnd
Output Current, Pin 8	30 mA
Package Dissipation	500 mW
Operating Temperature Range (T_A)	−25°C to +125°C
Storage Temperature Range	−55°C to +150°C
Soldering Information	
Dual-In-Line Package	
Soldering (10 sec.)	260°C
Small Outline Package	
Vapor Phase (60 sec.)	215°C
Infrared (15 sec.)	220°C

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.

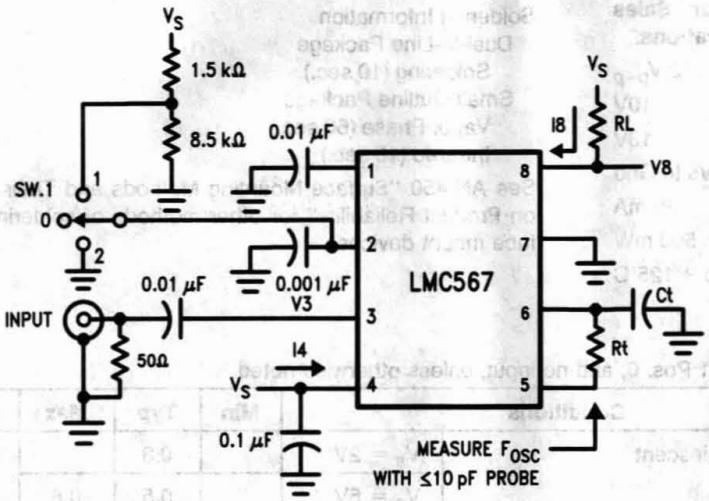
Electrical Characteristics

Test Circuit, T_A = 25°C, V_S = 5V, RtCt #2, Sw. 1 Pos. 0, and no input, unless otherwise noted.

Symbol	Parameter	Conditions		Min	Typ	Max	Units
I4	Power Supply Current	RtCt #1, Quiescent or Activated	V_S = 2V		0.3		mAdc
			V_S = 5V		0.5	0.8	
			V_S = 9V		0.8	1.3	
V3	Input D.C. Bias				0		mVdc
R3	Input Resistance				40		kΩ
I8	Output Leakage				1	100	nAdc
f_0	Center Frequency, $F_{osc} \div 2$	RtCt #2, Measure Oscillator Frequency and Divide by 2	V_S = 2V		98		kHz
			V_S = 5V	92	103	113	
			V_S = 9V		105		
Δf_0	Center Frequency Shift with Supply	$\frac{f_0\|_{9V} - f_0\|_{2V}}{7\, f_0\|_{5V}} \times 100$			1.0	2.0	%/V
V_{in}	Input Threshold	Set Input Frequency Equal to f_0 Measured Above, Increase Input Level Until Pin 8 Goes Low.	V_S = 2V	11	20	27	mVrms
			V_S = 5V	17	30	45	
			V_S = 9V		45		
ΔV_{in}	Input Hysteresis	Starting at Input Threshold, Decrease Input Level Until Pin 8 goes High.			1.5		mVrms
V8	Output 'Sat' Voltage	Input Level > Threshold Choose RL for Specified I8	I8 = 2 mA		0.06	0.15	Vdc
			I8 = 20 mA		0.7		
L.D.B.W.	Largest Detection Bandwidth	Measure F_{osc} with Sw. 1 in Pos. 0, 1, and 2; L.D.B.W = $\frac{F_{osc\|P2} - F_{osc\|P1}}{F_{osc\|P0}} \times 100$	V_S = 2V	7	11	15	%
			V_S = 5V	11	14	17	
			V_S = 9V		15		
ΔBW	Bandwidth Skew	Skew = $\left(\frac{F_{osc\|P2} + F_{osc\|P1}}{2\, F_{osc\|P0}} - 1\right) \times 100$			0	±1.0	%
f_{max}	Highest Center Freq.	RtCt #3, Measure Oscillator Frequency and Divide by 2			700		kHz
V_{in}	Input Threshold at f_{max}	Set Input Frequency Equal to f_{max} measured Above, Increase Input Level Until Pin 8 goes Low.			35		mVrms

Test Circuit

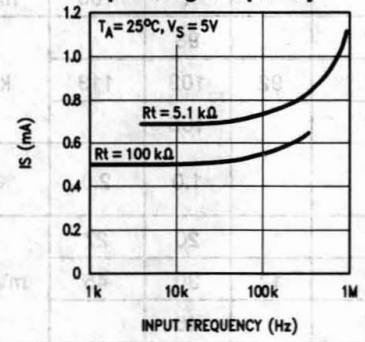
RtCt	Rt	Ct
#1	100k	300 pF
#2	10k	300 pF
#3	5.1k	62 pF



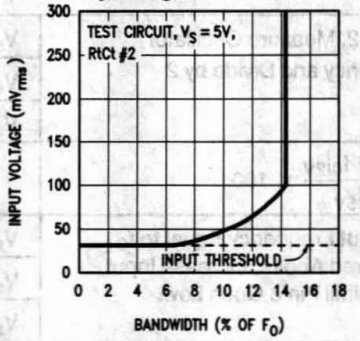
TL/H/8670–2

Typical Performance Characteristics

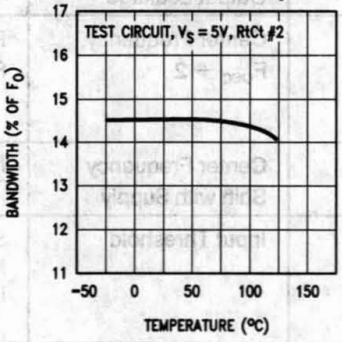
Supply Current vs. Operating Frequency



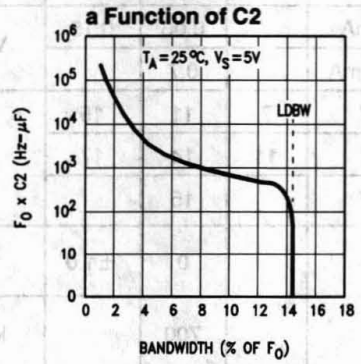
Bandwidth vs. Input Signal Level



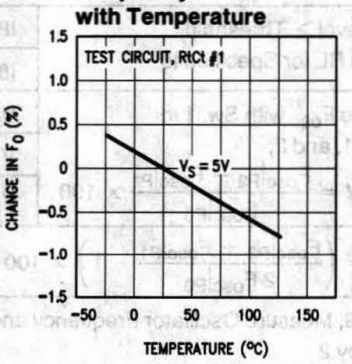
Largest Detection Bandwidth vs. Temp.



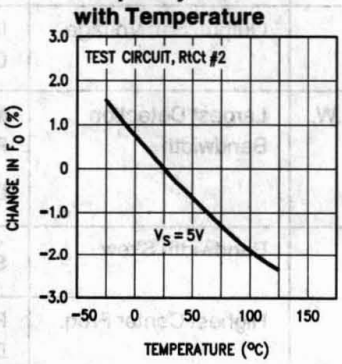
Bandwidth as a Function of C2



Frequency Drift with Temperature



Frequency Drift with Temperature



TL/H/8670–3

Applications Information (refer to Block Diagram)

GENERAL

The LMC567 low power tone decoder can be operated at supply voltages of 2V to 9V and at input frequencies ranging from 1 Hz up to 500 kHz.

The LMC567 can be directly substituted in most LM567 applications with the following provisions:

1. Oscillator timing capacitor Ct must be halved to double the oscillator frequency relative to the input frequency (See OSCILLATOR TIMING COMPONENTS).
2. Filter capacitors C1 and C2 must be reduced by a factor of 8 to maintain the same filter time constants.
3. The output current demanded of pin 8 must be limited to the specified capability of the LMC567.

OSCILLATOR TIMING COMPONENTS

The voltage-controlled oscillator (VCO) on the LMC567 must be set up to run at twice the frequency of the input signal tone to be decoded. The center frequency of the VCO is set by timing resistor Rt and timing capacitor Ct connected to pins 5 and 6 of the IC. The center frequency as a function of Rt and Ct is given by:

$$F_{osc} \cong \frac{1}{1.4\ Rt\ Ct}\ Hz$$

Since this will cause an input tone of half F_{osc} to be decoded,

$$F_{input} \cong \frac{1}{2.8\ Rt\ Ct}\ Hz$$

This equation is accurate at low frequencies; however, above 50 kHz (F_{osc} = 100 kHz), internal delays cause the actual frequency to be lower than predicted.

The choice of Rt and Ct will be a tradeoff between supply current and practical capacitor values. An additional supply current component is introduced due to Rt being switched to V_S every half cycle to charge Ct:

$$I_S \text{ due to } Rt = V_S/(4Rt)$$

Thus the supply current can be minimized by keeping Rt as large as possible (see supply current vs. operating frequency curves). However, the desired frequency will dictate an RtCt product such that increasing Rt will require a smaller Ct. Below Ct = 100 pF, circuit board stray capacitances begin to play a role in determining the oscillation frequency which ultimately limits the minimum Ct.

To allow for I.C. and component value tolerances, the oscillator timing components will require a trim. This is generally accomplished by using a variable resistor as part of Rt, although Ct could also be padded. The amount of initial frequency variation due to the LMC567 itself is given in the electrical specifications; the total trim range must also accommodate the tolerances of Rt and Ct.

SUPPLY DECOUPLING

The decoupling of supply pin 4 becomes more critical at high supply voltages with high operating frequencies, requiring C4 to be placed as close as possible to pin 4.

INPUT PIN

The input pin 3 is internally ground-referenced with a nominal 40 kΩ resistor. Signals which are already centered on 0V may be directly coupled to pin 3; however, any d.c. potential must be isolated via a coupling capacitor. Inputs of multiple LMC567 devices can be paralleled without individual d.c. isolation.

LOOP FILTER

Pin 2 is the combined output of the phase detector and control input of the VCO for the phase-locked loop (PLL). Capacitor C2 in conjunction with the nominal 80 kΩ pin 2 internal resistance forms the loop filter.

For small values of C2, the PLL will have a fast acquisition time and the pull-in range will be set by the built in VCO frequency stops, which also determine the largest detection bandwidth (LDBW). Increasing C2 results in improved noise immunity at the expense of acquisition time, and the pull-in range will begin to become narrower than the LDBW (see Bandwidth as a Function of C2 curve). However, the maximum hold-in range will always equal the LDBW.

OUTPUT FILTER

Pin 1 is the output of a negative-going amplitude detector which has a nominal 0 signal output of 7/9 V_S. When the PLL is locked to the input, an increase in signal level causes the detector output to move negative. When pin 1 reaches 2/3 V_S the output is activated (see OUTPUT PIN).

Capacitor C1 in conjunction with the nominal 40 kΩ pin 1 internal resistance forms the output filter. The size of C1 is a tradeoff between slew rate and carrier ripple at the output comparator. Low values of C1 produce the least delay between the input and output for tone burst applications, while larger values of C1 improve noise immunity.

Pin 1 also provides a means for shifting the input threshold higher or lower by connecting an external resistor to supply or ground. However, reducing the threshold using this technique increases sensitivity to pin 1 carrier ripple and also results in more part to part threshold variation.

OUTPUT PIN

The output at pin 8 is an N-channel FET switch to ground which is activated when the PLL is locked and the input tone is of sufficient amplitude to cause pin 1 to fall below 2/3 V_S. Apart from the obvious current component due to the external pin 8 load resistor, no additional supply current is required to activate the switch. The on resistance of the switch is inversely proportional to supply; thus the 'sat' voltage for a given output current will increase at lower supplies.

National Semiconductor

LMC568 Low Power Phase-Locked Loop

General Description

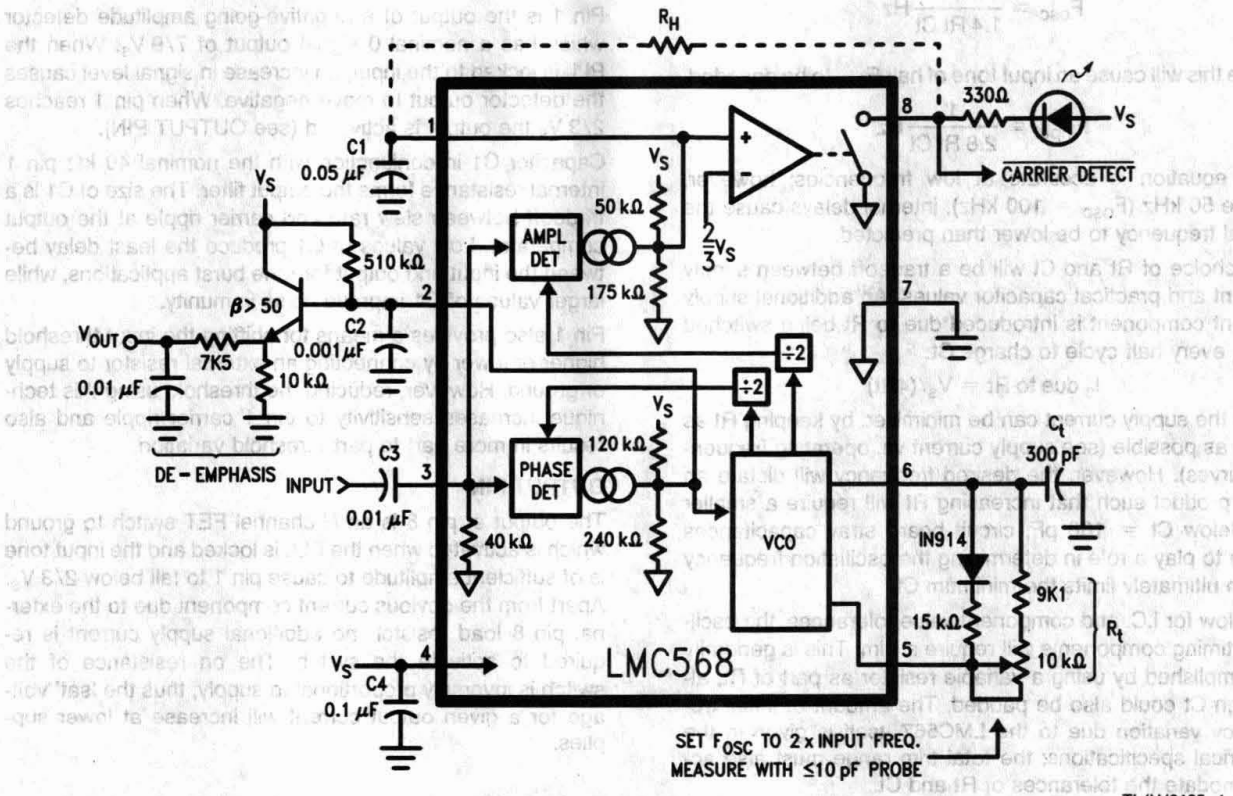
The LMC568 is an amplitude-linear phase-locked loop consisting of a linear VCO, fully balanced phase detectors, and a carrier detect output. LMCMOS™ technology is employed for high performance with low power consumption.

The VCO has a linearized control range of ±30% to allow demodulation of FM and FSK signals. Carrier detect is indicated when the PLL is locked to an input signal greater than 26 mVrms. LMC568 applications include FM SCA and TV second audio program decoders, FSK data demodulators, and voice pagers.

Features

- Demodulates ±15% deviation FM/FSK signals
- Carrier Detect Output with hysteresis
- Operation to 500 kHz input frequency
- Low THD—0.5% typ. for ±10% deviation
- 2V to 9V supply voltage range
- Low supply current drain

Typical Application (100 kHz input frequency, refer to notes pg. 4-194)



Order Number LMC568CM or LMC568CN
See NS Package Number M08A or N08E

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Input Voltage, Pin 3	2 V_{p-p}
Supply Voltage, Pin 4	10V
Output Voltage, Pin 8	13V
Voltage at All Other Pins	V_S to Gnd
Output Current, Pin 8	30 mA
Package Dissipation	500 mW
Operating Temperature Range (T_A)	−25°C to +125°C
Storage Temperature Range	−55°C to +150°C
Soldering Information	
Dual-In-Line Package	
Soldering (10 seconds)	260°C
Small Outline Package	
Vapor Phase (60 seconds)	215°C
Infrared (15 seconds)	220°C

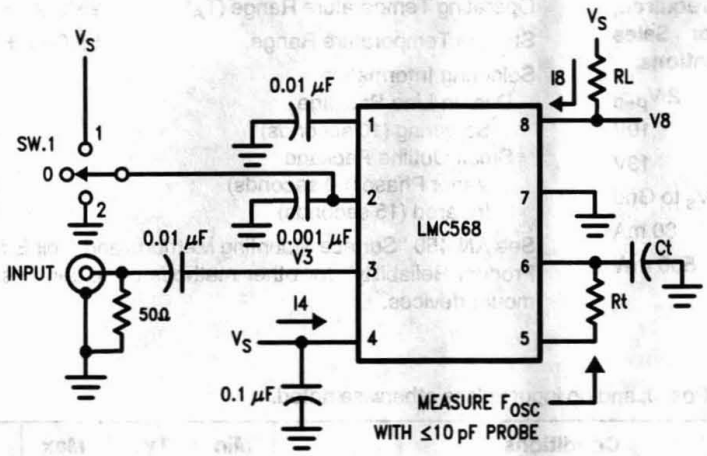
See AN-450 "Surface Mounting Methods and their Effect on Product Reliability" for other methods of soldering surface mount devices.

Electrical Characteristics

Test Circuit, T_A = 25°C, V_S = 5V, RtCt #2, Sw. 1 Pos. 0; and no input unless otherwise noted.

Symbol	Parameter	Conditions		Min	Typ	Max	Units
I4	Power Supply Current	RtCt #1, Quiescent or Activated	V_S = 2V		0.35		mAdc
			V_S = 5V		0.75	1.5	
			V_S = 9V		1.2	2.4	
V3	Input D.C. Bias				0		mVdc
R3	Input Resistance				40		kΩ
I8	Output Leakage				1	100	nAdc
f_0	Center Frequency $F_{osc} \div 2$	RtCt #2, Measure Oscillator Frequency and Divide by 2	V_S = 2V		98		kHz
			V_S = 5V	90	103	115	
			V_S = 9V		105		
Δf_0	Center Frequency Shift with Supply	$\frac{f_0\|_{9V} - f_0\|_{2V}}{7\, f_0\|_{5V}} \times 100$			1.0	2.0	%/V
V_{in}	Input Threshold	Set Input Frequency Equal to f_0 Measured Above, Increase Input Level until Pin 8 Goes Low.	V_S = 2V	8	16	25	mVrms
			V_S = 5V	15	26	42	
			V_S = 9V		45		
ΔV_{in}	Input Hysteresis	Starting at Input Threshold, Decrease Input Level until Pin 8 Goes High.			1.5		mVrms
V8	Output 'Sat' Voltage	Input Level > Threshold Choose RL for Specified I8	I8 = 2 mA		0.06	0.15	Vdc
			I8 = 20 mA		0.7		
L.D.B.W.	Largest Detection Bandwidth	Measure F_{osc} with Sw. 1 in Pos. 0, 1, and 2; L.D.B.W. $= \frac{F_{osc}\|_{P2} - F_{osc}\|_{P1}}{F_{osc}\|_{P0}} \times 100$	V_S = 2V		30		%
			V_S = 5V	40	55		
			V_S = 9V		60		
ΔBW	Bandwidth Skew	Skew $= \left(\frac{F_{osc}\|_{P2} + F_{osc}\|_{P1}}{2\, F_{osc}\|_{P0}} - 1\right) \times 100$			1	±5	%
V_{out}	Recovered Audio	Typical Application Circuit Input = 100 mVrms, F = 100 kHz F_{mod} = 400 Hz, ±10 kHz Dev.	V_S = 2V		170		mVrms
			V_S = 5V		270		
			V_S = 9V		400		
THD	Total Harmonic Distortion	Typical Application Circuit as Above, Measure V_{out} Distortion.			0.5		%
$\frac{S+N}{N}$	Signal to Noise Ratio	Typical Application Circuit Remove Modulation, Measure V_n $(S + N)/N = 20 \log (V_{out}/V_n)$.			65		dB
f_{max}	Highest Center Freq.	RtCt #3, Measure Oscillator Frequency and Divide by 2			700		kHz

Test Circuit



RtCt	Rt	Ct
#1	100k	300 pF
#2	10k	300 pF
#3	5.1k	62 pF

TL/H/9135–3

Notes to Typical Application

SUPPLY DECOUPLING

The decoupling of supply pin 4 becomes more critical at high supply voltages with high operating frequencies, requiring C4 to be placed as close to possible to pin 4. Also, due to pin voltages tracking supply, a large C4 is necessary for low frequency PSRR.

OSCILLATOR TIMING COMPONENTS

The voltage-controlled oscillator (VCO) on the LMC568 must be set up to run at twice the frequency of the input signal. The components shown in the typical application are for F_{osc} = 200 kHz (100 kHz input frequency). For operation at lower frequencies, increase the capacitor value; for higher frequencies proportionally reduce the resistor values.

If low distortion is not a requirement, the series diode/resistor between pins 6 and 5 may be omitted. This will reduce VCO supply dependence and increase V_{out} by approximately 2 dB with THD = 2% typical. The center frequency as a function of Rt and Ct is given by:

$$F_{osc} \cong \frac{1}{1.4\ Rt\ Ct}\ Hz$$

To allow for I.C. and component value tolerences, the oscillator timing components will require a trim. This is generally accomplished by using a variable resistor as part of Rt, although Ct could also be padded. The amount of initial frequency variation due to the LMC568 itself is given in the electrical specifications; the total trim range must also accommodate the tolerances of Rt and Ct.

INPUT PIN

The input pin 3 is internally ground-referenced with a nominal 40 kΩ resistor. Signals that are centered on 0V may be directly coupled to pin 3; however, any d.c. potential must be isolated via C3.

OUTPUT TAKEOFF

The output signal is taken off the loop filter at pin 2. Pin 2 is the combined output of the phase detector and control input of the VCO for the phase-locked loop (PLL). The nominal pin 2 source resistance is 80 kΩ, requiring the use of an external buffer transistor to drive nominal loads.

For small values of C2, the PLL will have a fast acquisition time and the pull-in range will be set by the built-in VCO frequency stops, which also determine the largest detection bandwidth (LDBW). Increasing C2 results in improved noise immunity at the expense of acquisition time, and the pull-in range will become narrower than the LDBW. However, the maximum hold-in range will always equal the LDBW. The 2 kHz de-emphasis pole shown may be modified or omitted as required by the application.

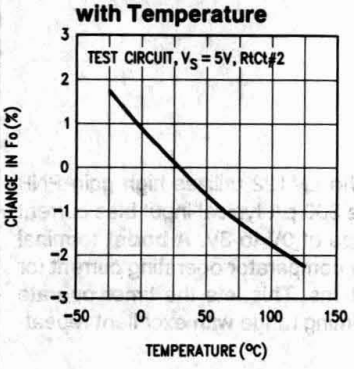
CARRIER DETECT

Pin 1 is the output of a negative-going amplitude detector which has a nominal 0 signal output of 7/9 V_S. The output at pin 8 is an N-channel FET switch to ground which is activated when the PLL is locked and the input is of sufficient amplitude to cause pin 1 to fall below 2/3 V_S. The carrier detect threshold is internally set to 26 mVrms typical on a 5V supply.

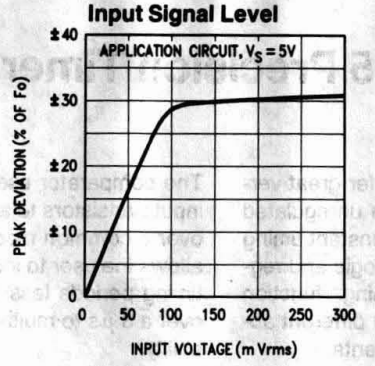
Capacitor C1 in conjunction with the nominal 40 kΩ pin 1 internal resistance forms the output filter. The size of C1 is a tradeoff between slew rate and carrier ripple at the output comparator. Optional resistor R_H increases the hysteresis in the pin 8 output for applications such as audio mute control. The minimum allowable value for R_H is 330 kΩ.

LMC568 Typical Performance Characteristics

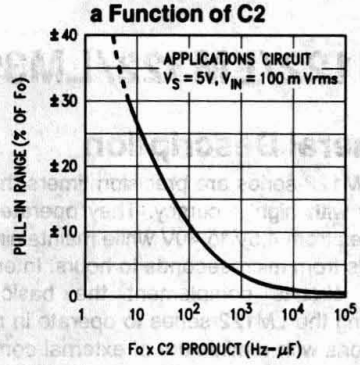
Frequency Drift with Temperature



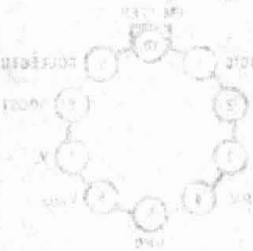
Peak Deviation vs Input Signal Level



Pull-In Range as a Function of C2



TL/H/9135–2



National Semiconductor

LM122/LM322/LM3905 Precision Timers

General Description

The LM122 series are precision timers that offer great versatility with high accuracy. They operate with unregulated supplies from 4.5V to 40V while maintaining constant timing periods from microseconds to hours. Internal logic and regulator circuits complement the basic timing function enabling the LM122 series to operate in many different applications with a minimum of external components.

The output of the timer is a floating transistor with built in current limiting. It can drive either ground referred or supply referred loads up to 40V and 50 mA. The floating nature of this output makes it ideal for interfacing, lamp or relay driving, and signal conditioning where an open collector or emitter is required. A "logic reverse" circuit can be programmed by the user to make the output transistor either "on" or "off" during the timing period.

The **trigger** input to the LM122 series has a threshold of 1.6V independent of supply voltage, but it is fully protected against inputs as high as ±40V—even when using a 5V supply. The circuitry reacts only to the rising edge of the trigger signal, and is immune to any trigger voltage during the timing periods.

An internal 3.15V regulator is included in the timer to reject supply voltage changes and to provide the user with a convenient reference for applications other than a basic timer. External loads up to 5 mA can be driven by the regulator. An internal 2V divider between the reference and ground sets the timing period to 1 RC. The timing period can be voltage controlled by driving this divider with an external source through the V_{ADJ} pin. Timing ratios of 50:1 can be easily achieved.

The comparator used in the LM122 utilizes high gain PNP input transistors to achieve 300 pA typical input bias current over a common mode range of 0V to 3V. A **boost** terminal allows the user to increase comparator operating current for timing periods less than 1 ms. This lets the timer operate over a 3 μs to multi-hour timing range with excellent repeatability.

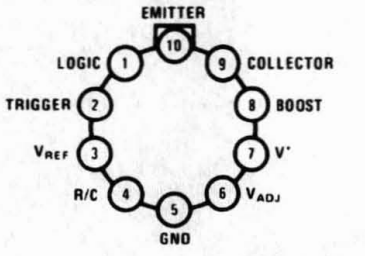
The LM122 operates over a temperature range of −55°C to +125°C. An electrically identical LM322 is specified from 0°C to +70°C. The LM3905 is identical to the LM122 series except that the **boost** and V_{ADJ} pin options are not available, limiting minimum timing period to 1 ms.

Features

- Immune to changes in trigger voltage during timing interval
- Timing periods from microseconds to hours
- Internal logic reversal
- Immune to power supply ripple during the timing interval
- Operates from 4.5V to 40V supplies
- Input protected to ±40V
- Floating transistor output with internal current limiting
- Internal regulated reference
- Timing period can be voltage controlled
- TTL compatible input and output

Connection Diagrams

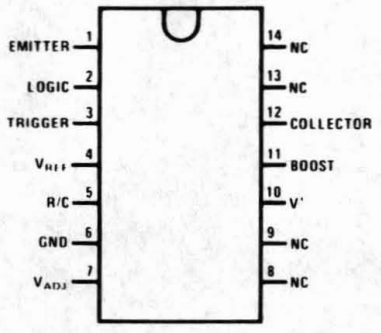
Metal Can Package



TL/H/7768–6

Top View
Order Number LM122H
See NS Package Number H10C

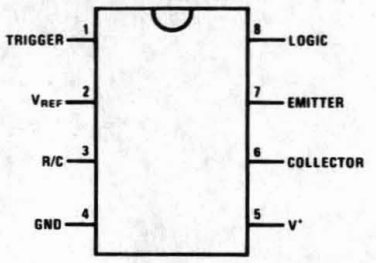
Dual-In-Line Package



TL/H/7768–7

Top View
Order Number LM322N
See NS Package Number N14A

Dual-In-Line Package



TL/H/7768–8

Top View
Order Number LM3905N
See NS Package Number N08E

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Power Dissipation	500 mW
V^+ Voltage	40V
Collector Output Voltage	40V
V_{REF} Current	5 mA
Trigger Voltage	±40V
V_{ADJ} Voltage (Forced)	5V
Logic Reverse Voltage	5.5V
Output Short Circuit Duration (Note 1)	
Lead Temperature (Soldering, 10 sec.)	260°C
Operating Temperature Range	
LM122	$-55°C \le T_A \le +125°C$
LM322	$0°C \le T_A \le +70°C$
LM3905	$0°C \le T_A \le +70°C$

Electrical Characteristics (Note 2)

Parameter	Conditions	LM122			LM322			LM3905			Units
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Timing Ratio	$T_A = 25°C$, $4.5V \le V^+ \le 40V$	0.626	0.632	0.638	0.620	0.632	0.644	0.620	0.632	0.644	
	Boost Tied to V^+, (Note 3)	0.620	0.632	0.644	0.620	0.632	0.644				
Comparator Input Current	$T_A = 25°C$, $4.5V \le V^+ \le 40V$		0.3	1.0		0.3	1.5		0.5	1.5	nA
	Boost Tied to V^+		30	100		30	100				nA
Trigger Voltage	$T_A = 25°C$, $4.5V \le V^+ \le 40V$	1.2	1.6	2	1.2	1.6	2	1.2	1.6	2	V
Trigger Current	$T_A = 25°C$, $V_{TRIG} = 2V$		25			25			25		μA
Supply Current	$T_A \ge 25°C$, $4.5V \le V^+ \le 40V$		2.5	4		2.5	4.5		2.5	4.5	mA
Timing Ratio	$4.5V \le V^+ \le 40V$	0.62		0.644	0.61		0.654	0.61		0.654	
	Boost Tied to V^+	0.62		0.644	0.61		0.654				
Comparator Input Current	$4.5V \le V^+ \le 40V$	−5		5	−2		2	−2.5		2.5	nA
	Boost Tied to V^+, (Note 4)			100			150				nA
Trigger Voltage	$4.5V \le V^+ \le 40V$	0.8		2.5	0.8		2.5	0.8		2.5	V
Trigger Current	$V_{TRIG} = 2.5V$			200			200			200	μA
Output Leakage Current	$V_{CE} = 40V$			1			5			5	μA
Capacitor Saturation Voltage	$R_t \ge 1\ M\Omega$		2.5			2.5			2.5		mV
	$R_t = 10\ k\Omega$		25			25			25		mV
Reset Resistance			150			150			150		Ω
Reference Voltage	$T_A = 25°C$	3	3.15	3.3	3	3.15	3.3	3	3.15	3.3	V
Reference Regulation	$0 \le I_{OUT} \le 3\ mA$		20	50		20	50		20	50	mV
	$4.5V \le V^+ \le 40V$		6	25		6	25		6	25	mV
Collector Saturation Voltage	$I_L = 8\ mA$		0.25	0.4		0.25	0.4		0.25	0.4	V
	$I_L = 50\ mA$		0.7	1.4		0.7	1.4		0.7	1.4	V
Emitter Saturation Voltage	$T_A = 25°C$, $I_L = 3\ mA$		1.8	2.2		1.8	2.2		1.8	2.2	V
	$T_A = 25°C$, $I_L = 50\ mA$		2.1	3		2.1	3		2.1	3	V
Average Temperature Coefficient of Timing Ratio			0.003			0.003			0.003		%/°C
Minimum Trigger Width	$V_{TRIG} = 3V$		0.25			0.25			0.25		μs

Note 1: Continuous output shorts are not allowed. Short circuit duration at ambient temperatures up to 40°C may be calculated from $t = 120/V_{CE}$ seconds, where V_{CE} is the collector to emitter voltage across the output transistor during the short.

Note 2: These specifications apply for $T_{AMIN} \le T_A \le T_{AMAX}$ unless otherwise noted.

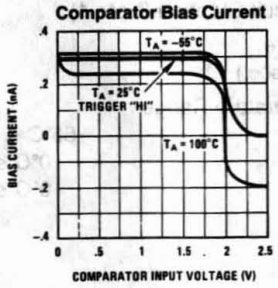
Note 3: Output pulse width can be calculated from the following equation: $t = (R_t)(C_t)[1 - 2(0.632 - r) - V_C/V_{REF})$ where r is timing ratio and V_C is capacitor saturation voltage. This reduces to $t = (R_t)(C_t)$ for all but the most critical applications.

Note 4: Sign reversal may occur at high temperatures (> 100°C) where comparator input current is predominately leakage. See typcial curves.

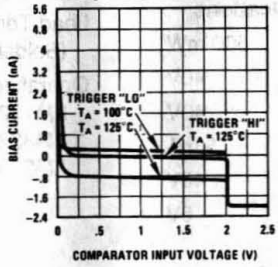
Note 5: Refer to RETS122X drawing of military LM122H version for specifications.

Typical Performance Characteristics

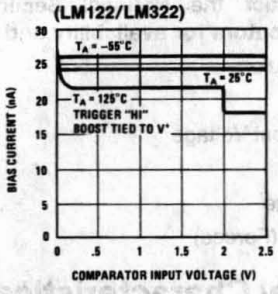
Comparator Bias Current



Comparator Bias Current

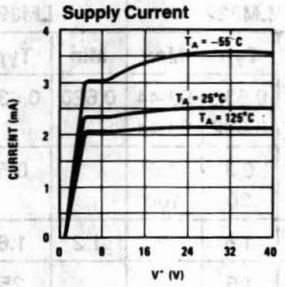


Comparator Bias Current (LM122/LM322)

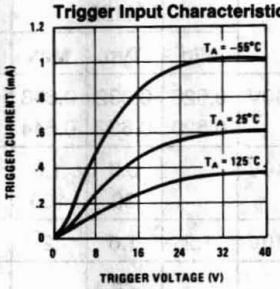


TL/H/7768–3

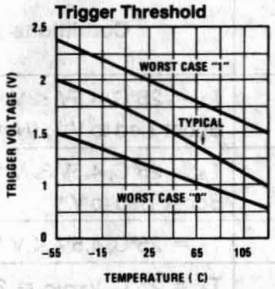
Supply Current



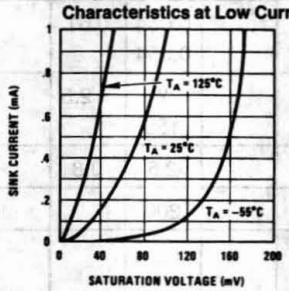
Trigger Input Characteristics



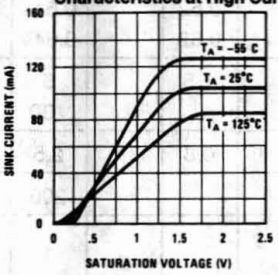
Trigger Threshold



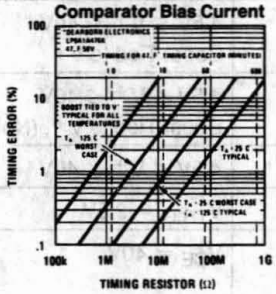
Output Transistor Saturation Characteristics at Low Currents



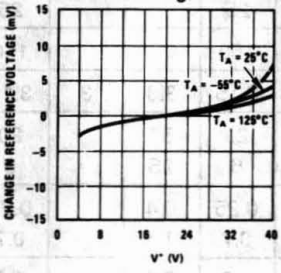
Collector Output Saturation Characteristics at High Current



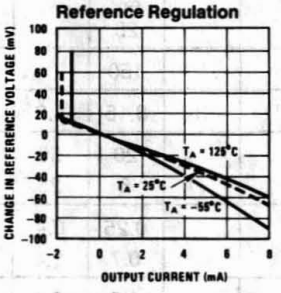
Timing Error Due to Comparator Bias Current


TIMING ERROR (%)
TIMING RESISTOR (Ω)
BOOST TIED TO V+ TYPICAL FOR ALL TEMPERATURES
T_A 125°C WORST CASE
T_A 25°C TYPICAL
T_A 25°C WORST CASE
T_A 125°C TYPICAL

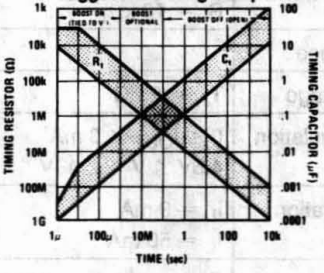
Reference Regulation



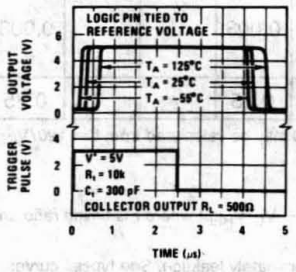
Reference Regulation



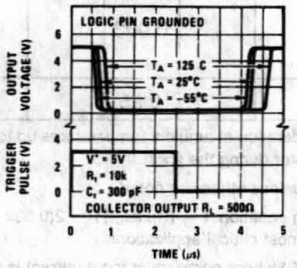
Suggested Timing Components



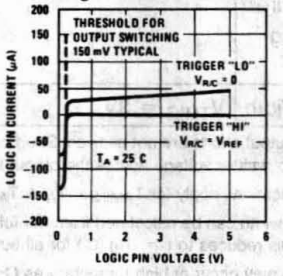
Short Output Pulse (LM122/LM322)



Short Output Pulse (LM122/LM322)

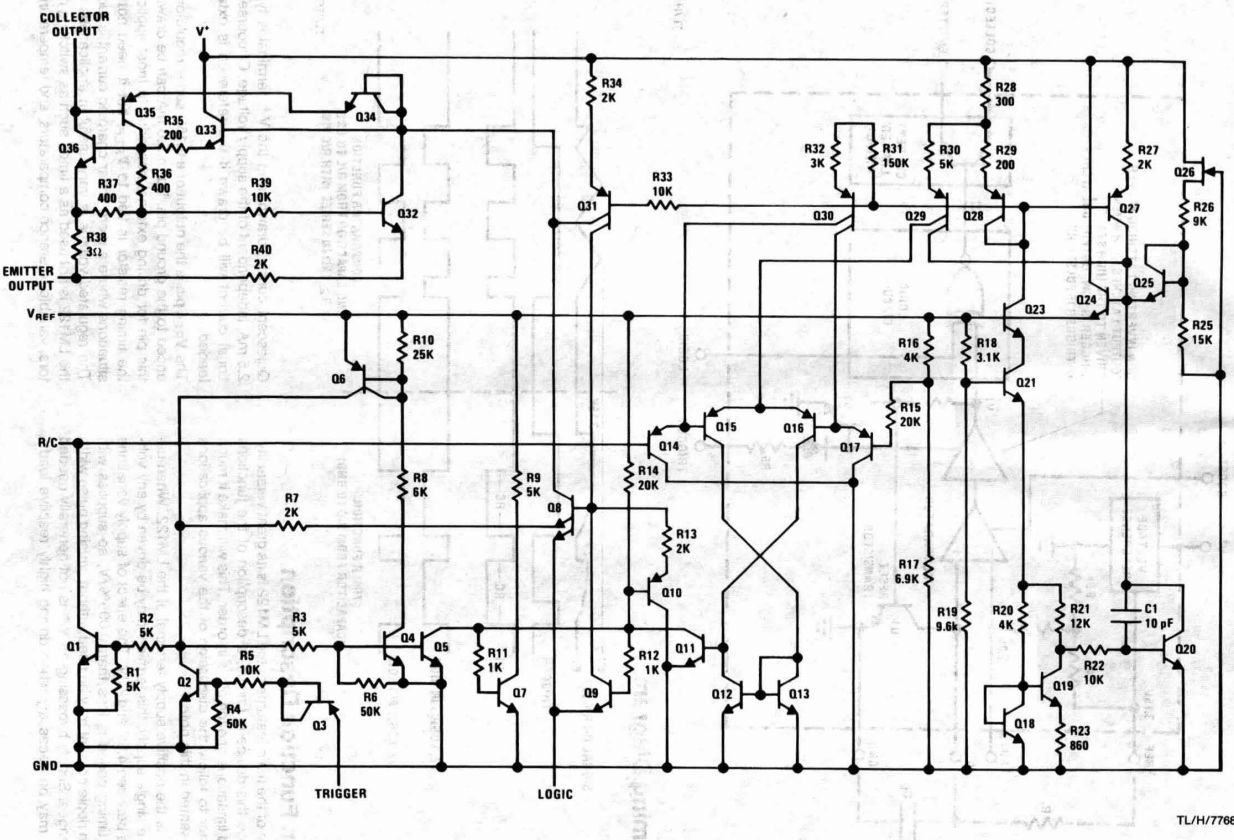


Logic Pin Characteristics



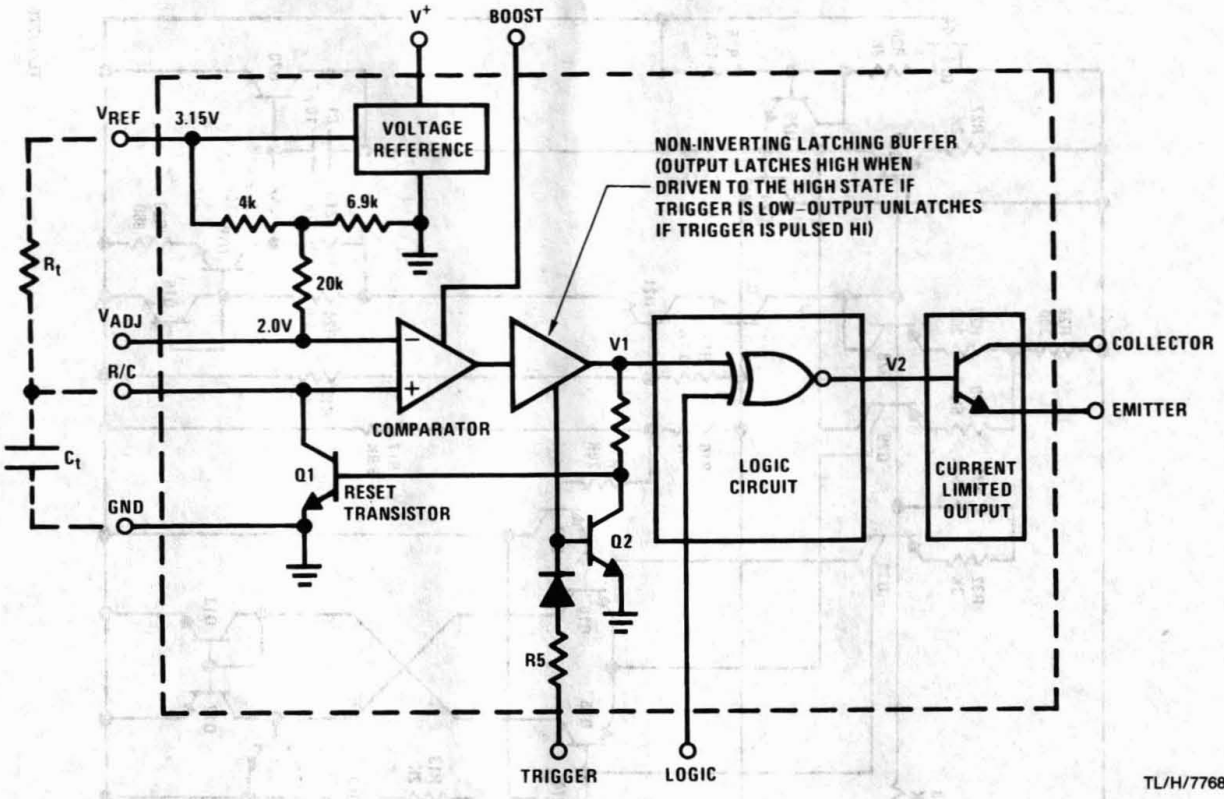
TL/H/7768–4

Schematic Diagram



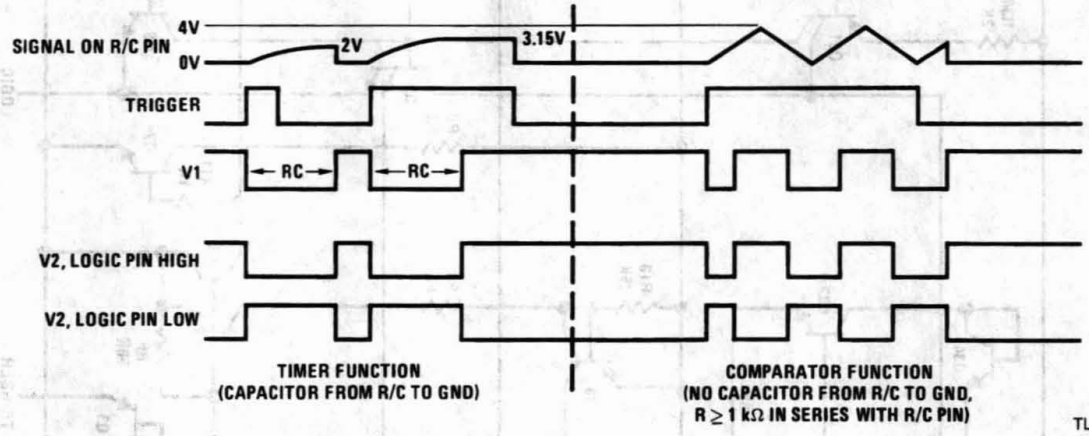
TL/H/7768–5

Functional Diagram



TL/H/7768–9

Timing Diagram



TL/H/7768–10

Pin Function Description

One of the main features of the LM122 is its great versatility. Since this device is unique, a description of the functions and limitations of each pin is in order. This will make it much easier to follow the discussion of the various applications presented in this note.

V^+ is the positive supply terminal of the LM122. When using a single supply, this terminal may be driven by any voltage between 4.5V and 40V. The effect of supply variations on timing period is less than 0.005%/V, so supplies with high ripple content may be used without causing pulse width changes. Supply bypassing on V^+ is not generally needed but may be necessary when driving highly reactive loads. Quiescent current drawn from the V^+ terminal is typically 2.5 mA, independent of the supply voltage. Of course, additional current will be drawn if the reference is externally loaded.

The V_{REF} pin is the output of a 3.15V series regulator referenced to the ground pin. Up to 5.0 mA can be drawn from this pin for driving external networks. In most applications the timing resistor is tied to V_{REF}, but it need not be in situations where a more linear charging current is required. The regulated voltage is very useful in applications where the LM122 is not used as a timer; such as switching regulators, variable reference comparators, and temperature con-

Pin Function Description (Continued)

trollers. Typical temperature drift of the reference is less than 0.01%/°C.

The **trigger** terminal is used to start a timing cycle (see functional diagram). Initially, Q1 is saturated, C_t is discharged and the latching buffer output (V1) is latched high. A trigger pulse unlatches the buffer, V1 goes low and turns Q1 off. The timing capacitor C_t connected from R/C to GND will begin to charge. When the voltage at the R/C terminal reaches the 2.0V threshold of the comparator, the comparator toggles, latching the buffer output (V1) in the high state. This turns on Q1, discharges the capacitor C_t and the cycle is ready to begin again.

If the **trigger** is held high as the timing period ends, the comparator will toggle and V1 will go high exactly as before. However, V1 will not be latched and the capacitor will not discharge until the trigger again goes low. When the trigger goes low, V1 remains high but is now latched.

Trigger threshold is typically 1.6V at 25°C and has a temperature dependence of −5.0 mV/°C. Current drawn from the **trigger** source is typically 20 μA at threshold, rising to 600 μA at 30V, then leveling off due to FET action of the series resistor, R5. For negative input trigger voltages, the only current drawn is leakage in the nA region. The **trigger** can be driven from supplies as high as ±40V, even when device supply voltage is only 5V.

The **R/C** pin is tied to the non-inverting side of the comparator and to the collector of Q1. Timing ends when the voltage on this pin reaches 2.0V (1 RC time constant referenced to the 3.15V regulator). Q1 turns on only if the trigger voltage has dropped below threshold. In comparator or regulator applications of the timer, the trigger is held permanently high and the **R/C** pin acts just like the input to an ordinary comparator. The maximum voltages which can be applied to this pin are +5.5V and −0.7V. Current from the **R/C** pin is typically 300 pA when the voltage is negative with respect to the V_{ADJ} terminal. For higher voltages, the current drops to leakage levels. In the boosted mode, input current is typically 30 nA. Gain of the comparator is very high, 200,000 or more, depending on the state of the logic reverse pin and the connection of the output transistor.

The **ground** pin of the LM122 need not necessarily be tied to system ground. It can be connected to any positive or negative voltage as long as the supply is negative with respect to the V^+ terminal. Level shifting may be necessary for the input **trigger** if the **trigger** voltage is referred to system ground. This can be done by capacitive coupling or by actual resistive or active level shifting. One point must be kept in mind; the emitter output must not be held above the **ground** terminal with a low source impedance. This could occur, for instance, if the emitter were grounded when the **ground** pin of the LM122 was tied to a negative supply.

The terminal labled V_{ADJ} is tied to one side of the comparator and to a voltage divider between V_{REF} and **ground**. The divider voltage is set at 63.2% of V_{REF} with respect to ground—exactly one RC time constant. The impedance of the divider is increased to about 30k with a series resistor to present a minimum load on external signals tied to V_{ADJ}. This resistor is a pinched type with a typical variation in nominal value of −50%, +100% and a TC of 0.7%/°C. For this reason, external signals (typically a pot between V_{REF} and **ground**) connected to V_{ADJ} should have a source resistance as low as possible. For small changes in V_{ADJ}, up to several kΩ is all right, but for large variations, 250Ω or less should be maintained. This can be accomplished with a 1k pot, since the maximum impedance from the wiper is 250Ω. If a voltage is forced on V_{ADJ} from a hard source, voltage should be limited to −0.5, and +5.0V, or current limited to ±1.0 mA. This includes capacitively coupled signals because even small values of capacitors contain enough energy to degrade the input stage if the capacitor is driven with a large, fast slewing signal. The V_{ADJ} pin may be used to abort the timing cycle. Grounding this pin during the timing period causes the timer to react just as if the capacitor voltage had reached its normal RC trigger point; the capacitor discharges and the output charges state. An exception to this occurs if the trigger pin is held high, when the V_{ADJ} pin is grounded. In this case, the output changes state, but the capacitor does not discharge.

If the trigger drops while V_{ADJ} is being held low, discharge will occur immediately and the cycle will be over. If the trigger is still high when V_{ADJ} is released, the output may or may not change state, depending on the voltage across the timing capacitor. For voltages below 2.0V across the timing capacitor, the output will change state immediately, then once more as the voltage rises past 2.0V. For voltages above 2.0V, no change will occur in the output. This pin is not available on the LM2905/LM3905.

In noisy environments or in comparator-type applications, a bypass capacitor on the V_{ADJ} terminal may be needed to eliminate spurious outputs because it is high impedance point. The size of the cap will depend on the frequency and energy content of the noise. A 0.1 μF will generally suffice for spike suppression, but several μF may be used if the timer is subjected to high level 60 Hz EMI.

The **emitter** and the **collector** outputs of the timer can be treated just as if they were an ordinary transistor with 40V minimum collector-emitter breakdown voltage. Normally, the **emitter** is tied to the **ground** pin and the signal is taken from the **collector**, or the **collector** is tied to V^+ and the signal is taken from the **emitter**. Variations on these basic connections are possible. The **collector** can be tied to any positive voltage up to 40V when the signal is taken from the **emitter**. However, the **emitter** will not be pulled higher than the supply voltage on the V^+ pin. Connecting the **collector** to a voltage less than the V^+ voltage is allowed. The **emitter** should not be connected to a low impedance load other than that to which the ground pin is tied. The transistor has built-in current limiting with a typical knee current of 120 mA. Temporary short circuits are allowed; even with **collector-emitter** voltages up to 40V. The power x time product, however, must not exceed 15 watt-seconds for power levels above the maximum rating of the package. A short to 30V,

Pin Function Description (Continued)

for instance, cannot be held for more than 4 seconds. These levels are based on 40°C maximum initial chip temperature. When driving inductive loads, always use a clamp diode to protect the transistor from inductive kick-back.

A **boost** pin is provided on the LM122 to increase the speed of the internal comparator. The comparator is normally operated at low current levels for lowest possible input current.

For timing periods less than 1 ms, where low input current is not needed, comparator operating current can be increased several orders of magnitude. Shorting the boost terminal to **V**+ increases the emitter current of the vertical PNP drivers in the differential stage from 25 nA to 5 μA. This pin is not available on the LM3905.

With the timer in the unboosted state, timing periods are accurate down to about 1 ms. In the boosted mode, loss of accuracy due to comparator speed is only about 800 ns, so timing periods of several microseconds can be used. The 800 ns error is relatively insensitive to temperature, so temperature coefficient of pulse width is still good.

The **Logic** pin is used to reverse the signal appearing at the output transistor. An open or "high" condition on the **logic** pin programs the output transistor to be "off" during the timing period and "on" all other times. Grounding the **logic** pin reverses the sequence to make the transistor "on" during the timing period. Threshold for the **logic** pin is typically 100 mV with 150 μA flowing out of the terminal. If an active drive to the **logic** pin is desired, a saturated transistor drive is recommended, either with a discrete transistor or the open collector output of integrated logic. A maximum V_{SAT} of 25 mV at 200 μA is required. Minimum and maximum voltages that may appear on the **logic** pin are 0 and +5.0, respectively.

Typical Applications

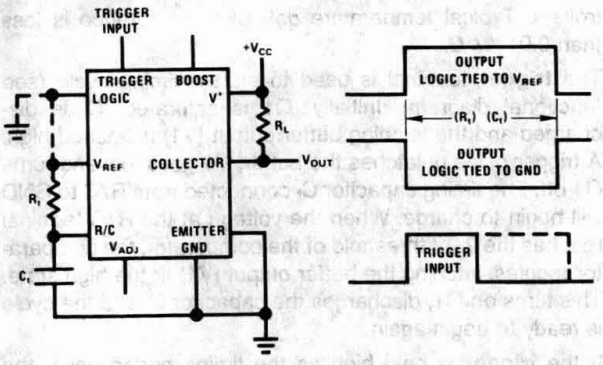
Basic Timers

Figure 1 is a basic timer using the collector output. R_t and C_t set the time interval with R_L as the load. During the timing interval the output may be either high or low depending on the connection of the logic pin. Timing waveforms are shown in the sketch along side *Figure 1*. Note that the trigger pulse may be either shorter or longer than the output pulse width.

Figure 2 is again a basic timer, but with the output taken from the emitter of the output transistor. As with the collector output, either a high or low condition may be obtained during the timing period.

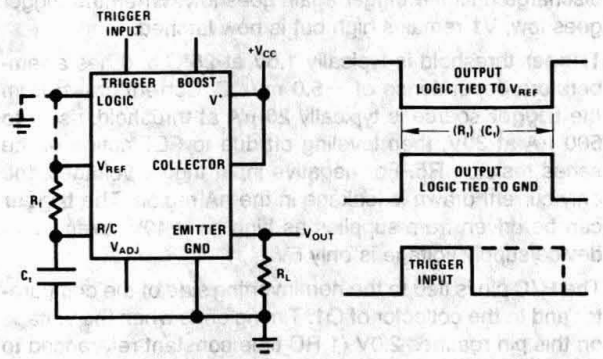
Simulating a Thermal Delay Relay

Figure 3 is an application where the LM122 is used to simulate a thermal delay relay which prevents power from being applied to other circuitry until the supply has been on for some time. The relay remains de-energized for R_t C_t seconds after V_{CC} is applied, then closes and stays energized until V_{CC} is turned off. *Figure 4* is a similar circuit except that the relay is energized as soon as V_{CC} is applied. R_t C_t seconds later, the relay is de-energized and stays off until the V_{CC} supply is recycled.



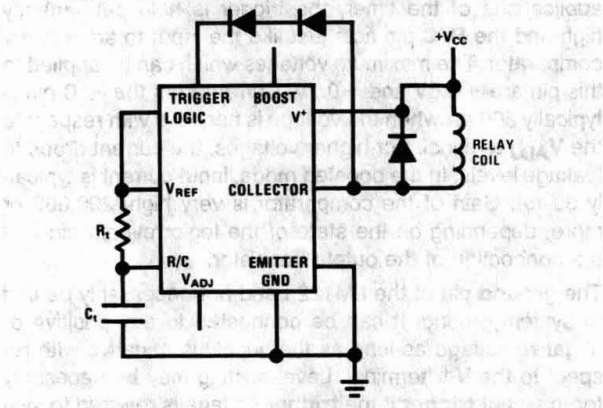
TL/H/7768–11

FIGURE 1. Basic Timer-Collector Output and Timing Chart



TL/H/7768–12

FIGURE 2. Basic Timer-Emitter Output and Timing Chart



TL/H/7768–13

FIGURE 3. Time Out on Power Up (Relay Energized R_t C_t Seconds after V_{CC} is Applied)

+5V Supply Driving 28V Relay

Figure 5 shows the timer interfacing 5V logic to a high voltage relay. Although the V+ terminal could be tied to the +28V supply, this may be an unnecessary waste of power in the IC or require extra wiring if the LM122 is on a logic card. In either case, the threshold for the trigger is 1.6V.

Typical Applications (Continued)

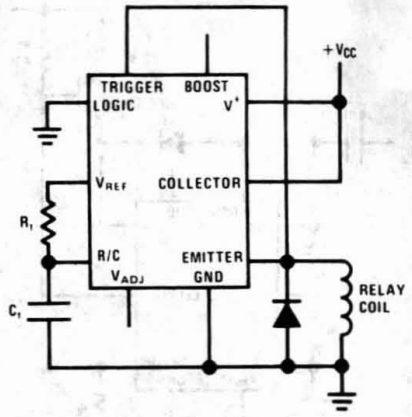


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FIGURE 4. Time Out on Power Up (Relay Energized *Until* R_t C_t Seconds After V_{CC} is Applied)

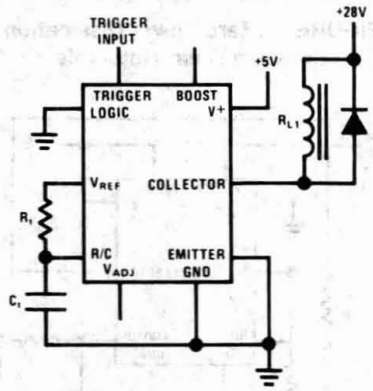

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FIGURE 5. 5V Logic Supply Driving 28V Relay

30V Supply Interfacing with 5V Logic

Figure 6 indicates the ability of the timer to interface to digital logic when operating off a high supply voltage. V_{OUT} swings between +5V and ground with a minimum fanout of 5 for medium speed TTL. If the logic is sensitive to rise/fall time of the trailing edge of the output pulse, the trigger pin should be low at that time.

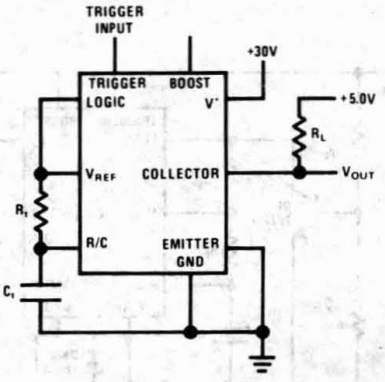

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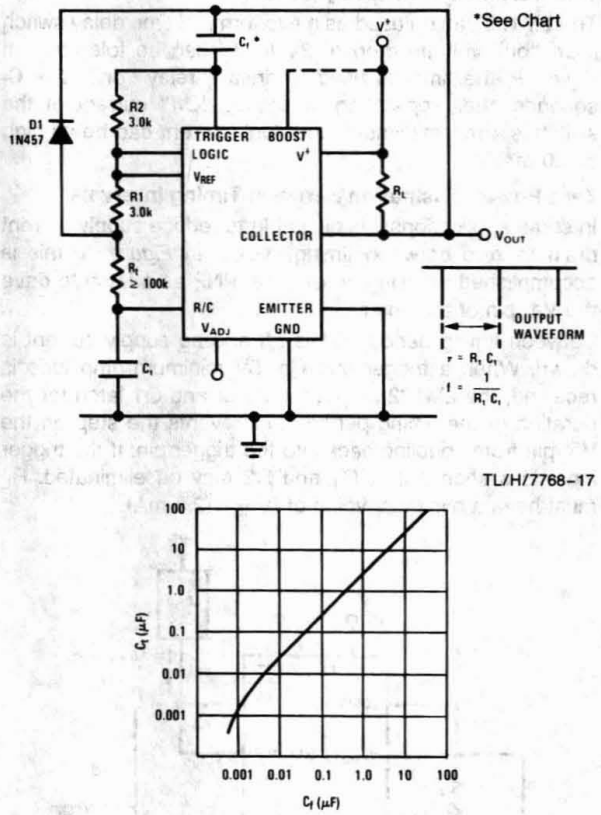
FIGURE 6. 30V Supply Interfacing with 5V Logic

Astable Operation

The LM122 can be made into a self-starting oscillator by feeding the output back to the trigger input through a capacitor as shown in *Figure 7*. Operating frequency is $1/(R_t + R_1)(C_t)$. The output is a narrow negative pulse whose width is approximately $2R_2$ C_f. For optimum frequency stability, C_f should be as small as possible. The minimum value is determined by the time required to discharge C_t through the internal discharge transistor. A conservative value for C_f can be chosen from the graph included with *Figure 20*. For frequencies below 1 kHz, the frequency error introduced by C_f is a few tenths of one percent or less for $R_t \geq 500k$.



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TL/H/7768–18

FIGURE 7. Oscillator

One Hour Timer with Reset and Manual Cycle End

Figure 8 shows the LM122 connected as a one hour timer with manual controls for start, reset, and cycle end. S1 starts timing, but has no effect after timing has started. S2 is a center off switch which can either end the cycle prematurely with the appropriate change in output state and discharging of C_t, or cause C_t to be reset to 0V without a change in output. In the latter case, a new timing period starts as soon as S2 is released.

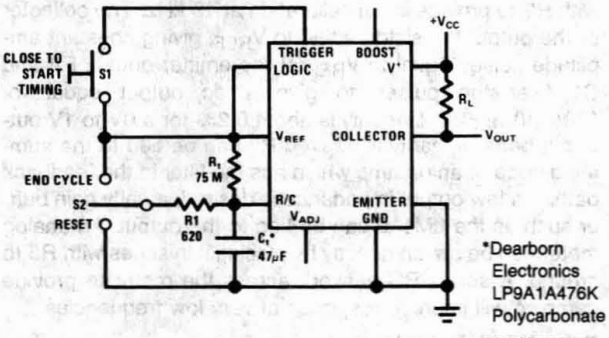

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FIGURE 8. One Hour Timer with Reset and Manual Cycle End

Typical Applications (Continued)

The average charging current through R_t is about 30 nA, so some attention must be paid to parts layout to prevent stray leakage paths. The suggested timing capacitor has a typical self time constant of 300 hours and a guaranteed minimum of 25 hours at +25°C. Other capacitor types may be used if sufficient data is available on their leakage characteristics.

Two Terminal Time Delay Switch

The LM122 can be used as a two terminal time delay switch if an "on" voltage drop of 2V to 3V can be tolerated. In *Figure 9*, the timer is used to drive a relay "on" $R_t \bullet C_t$ seconds after application of power. "Off" current of the switch is 4 mA maximum, and "on" current can be as high as 50 mA.

Zero Power Dissipation Between Timing Intervals

In some applications it is desirable to reduce supply current drain to zero between timing cycles. In *Figure 10* this is accomplished by using an external PNP as a latch to drive the V^+ pin of the timer.

Between timing periods Q1 is off and no supply current is drawn. When a trigger pulse of 5V minimum amplitude is received, the LM122 output transistor and Q1 latch for the duration of the timing period. D1 prevents the step on the V^+ pin from coupling back into the trigger pin. If the trigger input is a short pulse, C1 and R2 may be eliminated. R_L must have a minimum value of $(V_{CC})/(2.5\ mA)$.

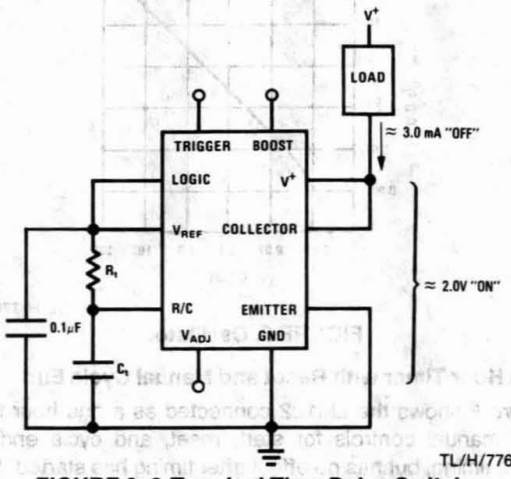

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FIGURE 9. 2-Terminal Time Delay Switch

Frequency to Voltage Converter

An accurate frequency to voltage converter can be made with the LM122 by averaging output pulses with a simple one pole filter as shown in *Figure 11*. Pulse width is adjusted with R2 to provide initial calibration at 10 kHz. The collector of the output transistor is tied to V_{REF}, giving constant amplitude pulses equal to V_{REF} at the emitter output. R4 and C1 filter the pulses to give a dc output equal to, $(R_t)(C_t)(V_{REF})(f)$. Linearity is about 0.2% for a 0V to 1V output. If better linearity is desired R5 can be tied to the summing node of an op amp which has the filter in the feedback path. If a low output impedance is desired, a unity gain buffer such as the LM110 can be tied to the output. An analog meter can be driven directly by placing it in series with R5 to ground. A series RC network across the meter to provide damping will improve response at very low frequencies.

Pulse Width Detector

By driving the logic terminal of the LM122 simultaneous to the trigger input, a simple, accurate pulse width detector can be made *(Figure 12)*.

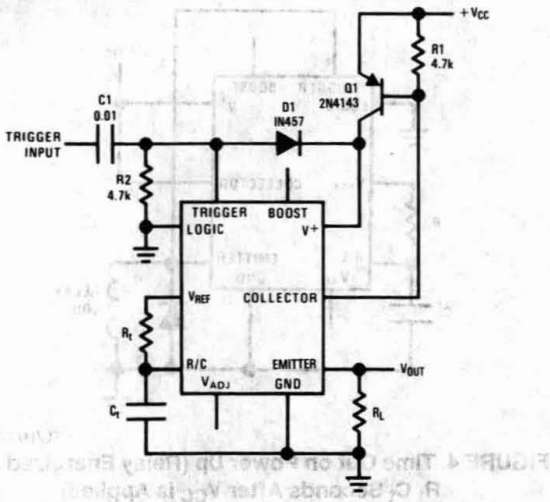

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FIGURE 10. Zero Power Dissipation Between Timing Intervals

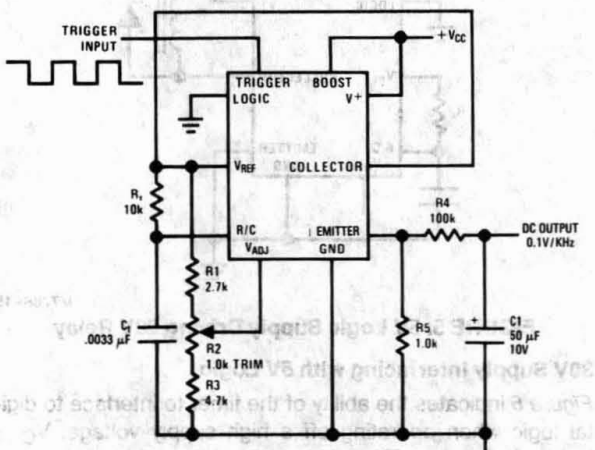

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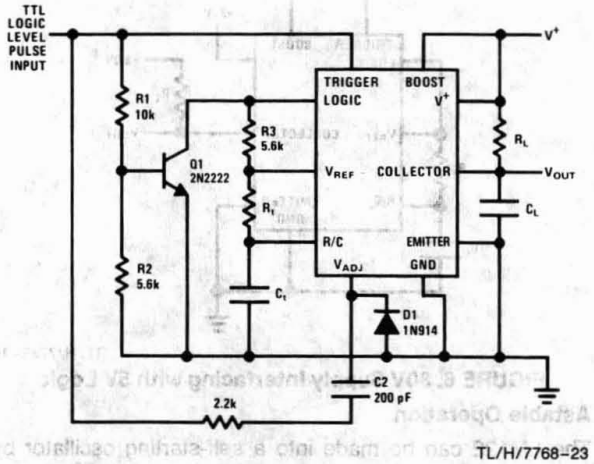
FIGURE 11. Frequency to Voltage Converter. (Tachometer) Output Independent of Supply Voltage.



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*V_{OUT} = 0 for W R_1 C_1

Pulse Out = W − R_1 C_1 for W R_1 C_1

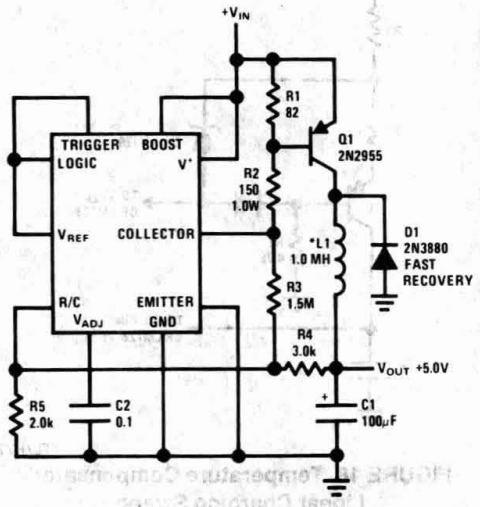
FIGURE 12. Pulse Width Detector

Typical Applications (Continued)

In this application the logic terminal is normally held high by R3. When a trigger pulse is received, Q1 is turned on, driving the logic terminal to ground. The result of triggering the timer and reversing the logic at the same time is that the output does not change from its initial low condition. The only time the output will change states is when the trigger input stays high longer than one time period set by R_t and C_t. The output pulse width is equal to the input trigger width minus $R_t \bullet C_t$. C2 insures no output pulse for short (<RC) trigger pulses by prematurely resetting the timing capacitor when the trigger pulse drops. C_L filters the narrow spikes which would occur at the output due to propagation delays during switching.

5V Switching Regulator

Figure 13 is an application where the LM122 does not use its timing function. A switching regulator is made using the internal reference and comparator to drive a PNP transistor switch. Features of this circuit include a 5.5V minimum input voltage at 1A output current, low part count, and good efficiency (> 75%) for input voltages to 10V. Line and load regulation are less than 0.5% and output ripple at the switching frequency is only 30 mV. Q1 is an inexpensive plastic device which does not need a heatsink for ambient temperature up to 50°C. D1 should be a fast switching diode. Output voltage can be adjusted between 1V and 30V by choosing proper values for R2, R3, R4, and R5. For outputs less than 2V, a divider with 250Ω Thevinin resistance must be connected between V_{REF} and ground with its tap point tied to V_{ADJ}.



*No. 22 Wire Wound on Molybdenum Permalloy Core TL/H/7768–24

FIGURE 13. 5V Switching Regulator with 1 Amp Output and 5.5V Minimum Input

Application Hints

Aborting a Timing Cycle

The LM122 does not have an input specifically allocated to a stop-timing function. If such a function is desired, it may be accomplished several ways:

- Ground V_{ADJ}
- Raise R/C more positive than V_{ADJ}
- Wire "OR" the output

Grounding V_{ADJ} will end the timing cycle just as if the timing capacitor had reached its normal discharge point. A new timing cycle can be started by the trigger terminal as soon as the ground is released. A switching transistor is best for driving V_{ADJ} to as near ground as possible. Worst case sink current is about 300 μA.

A timing cycle may also be ended by a positive pulse to a resistor ($R \leq R_t/100$) in series with the timing capacitor. The pulse amplitude must be at least equal to V_{ADJ} (2.0V), but should not exceed 5.0V. When the timing capacitor discharges, a negative spike of up to 2.0V will occur across the resistor, so some caution must be used if the drive pulse is used for other circuitry.

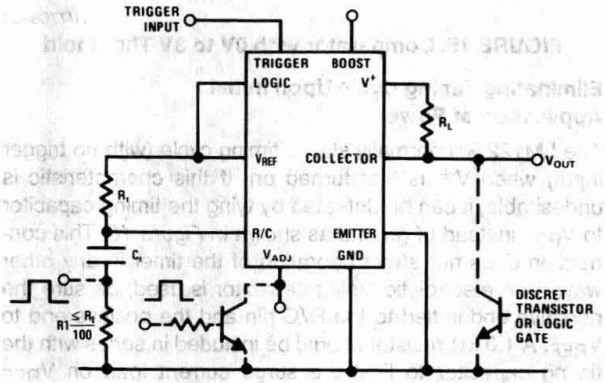


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FIGURE 14. Cycle Interrupt

The output of the timer can be wire ORed with a discrete transistor or an open collector logic gate output. This allows overriding of the timer output, but does not cause the timer to be reset until its normal cycle time has elapsed.

Using the LM122 as a Comparator

A built-in reference and zero volt common mode limit make the LM122 very useful as a comparator. Threshold may be adjusted from zero to three volts by driving the V_{ADJ} terminal with a divider tied to V_{REF}. Stability of the reference voltage is typically ±1% over a temperature range of −55°C to +125°C. Offset voltage drift in the comparator is typically 25 μV/°C in the boosted mode and 50 μV/°C unboosted. A resistor can be inserted in series with the input to allow overdrives up to ±50V as shown in *Figure 15*. There is actually no limit on input voltage as long as current is limited to ±1 mA. The resistor shown contributes a worst case of 5 mV to initial offset. In the unboosted mode, the error drops to 0.25 mV maximum. The capability of operating off a single 5V supply with internal reference should make this comparator very useful.

Application Hints (Continued)

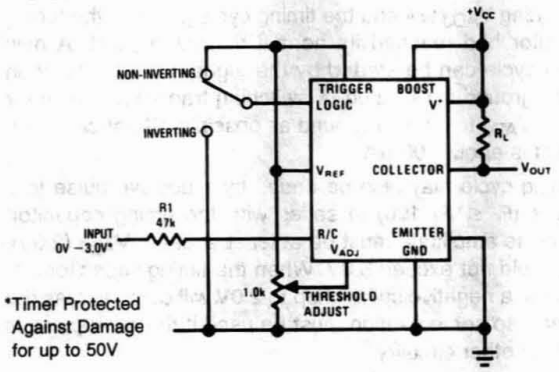

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FIGURE 15. Comparator with 0V to 3V Threshold

Eliminating Timing Cycle Upon Initial Application of Power

The LM122 will normally start a timing cycle (with no trigger input) when V^+ is first turned on. If this characteristic is undesirable, it can be defeated by tying the timing capacitor to V_{REF} instead of ground as shown in *Figure 16*. This connection does not affect operation of the timer in any other way. If an electrolytic timing capacitor is used, be sure the negative end is tied to the R/C pin and the positive end to V_{REF}. A 1.0 kΩ resistor should be included in series with the timing capacitor to limit the surge current load on V_{REF} when the capacitor is discharged.

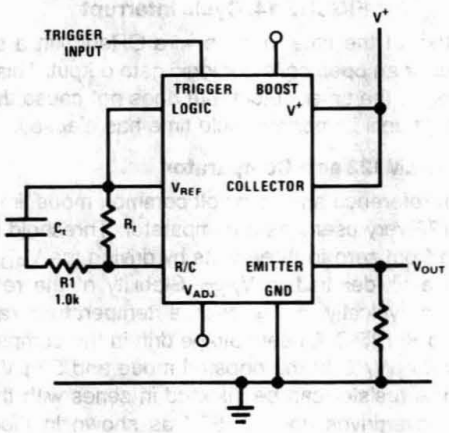

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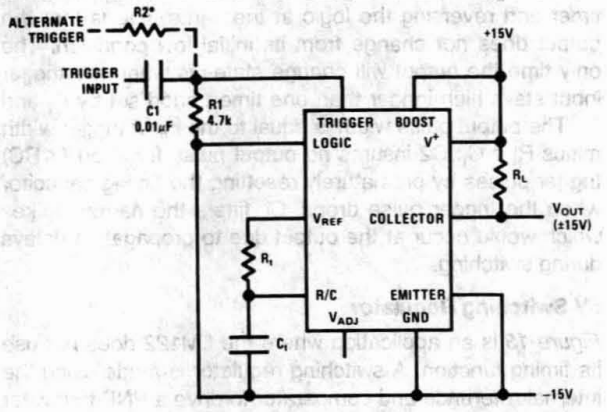
FIGURE 16. Eliminating Initial Timing Cycle

Using Dual Supplies

The LM122 can be operated off dual supplies as shown in *Figure 17*. The only limitation is that the emitter terminal cannot be tied to ground, it must either drive a load referred to V^- or be actually tied to V^- as shown. Although capacitive coupling is shown for the trigger input (to allow 5V triggering), a resistor can be substituted for C1. R2 must be chosen to give proper level shifting between the trigger signal and the trigger pin of the timer. Worst case "lo" on the trigger pin (with respect to V^-) is 0.8V, and worst case "high" is 2.5V. R2 may be calculated from the divider equation with R1 to give these levels.



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*Select for Proper Level Shift
Emitter Terminal or Emitter Load must be Tied to GND Pin of Timer

FIGURE 17. Operating Off Dual Supplies

Linearizing the Charging Sweep

In some applications (such as a linear pulse width modulator) it may be desirable to have the timing capacitor charge from a constant current source. A simple way to accomplish this is shown in *Figure 18*.

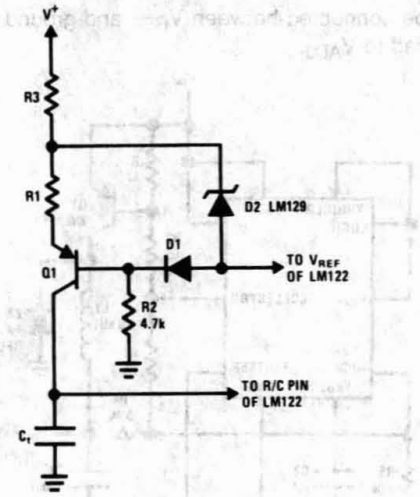

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FIGURE 18. Temperature Compensated Linear Charging Sweep

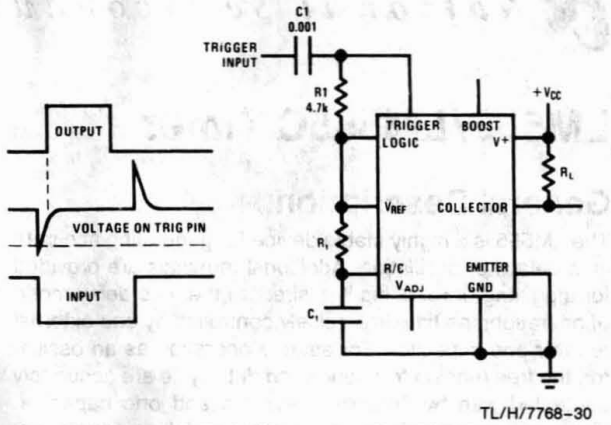
Q1 converts the current through R1 to a current source independent of the voltage across C_t. R2, R3, D1, and D2 are added to make the current through R1 independent of supply variations and temperature changes. (D2 is a low TC type) D2 and R3 can be omitted if the V^+ supply is stable and D1 and R2 can be omitted also if temperature stability is not critical. With D1, D2, R2 and R3 omitted, the current through R1 will change about 0.015%/°C with a 15V supply and 0.1%/°C with a 5.0V supply.

Application Hints (Continued)

Triggering with Negative Edge

Although the LM122 is triggered by a positive going trigger signal, a differentiator tied to a normally "high" trigger will result in negative edge triggering. In *Figure 19*, R1 serves the dual purpose of holding the trigger pin normally high and differentiating the input trigger pulse coupled through C1. The timing diagram included with *Figure 21* shows that triggering actually occurs a short time after the negative going trigger, while positive going triggers have no effect. The delay time between a negative trigger signal and actual starts of timing is approximately (0.5 to 1.5) (R1 • C1) depending on the trigger amplitude, or about 2.5 to 7.5 μs with the values shown. This time will have to be increased for C_t larger than 0.01 μF because C_t is charged to V_{REF} whenever the trigger pin is kept high and must reset itself during the short time that the trigger pin voltage is low. A conservative value for C1 is:

$$C1 \geq \frac{C_t}{10}$$

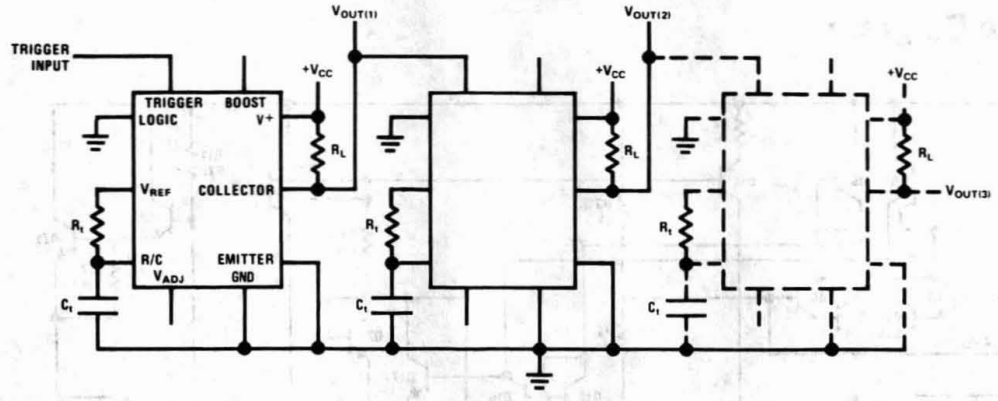


TL/H/7768–30

FIGURE 19. Timer Triggered by Negative Edge of Input Pulse

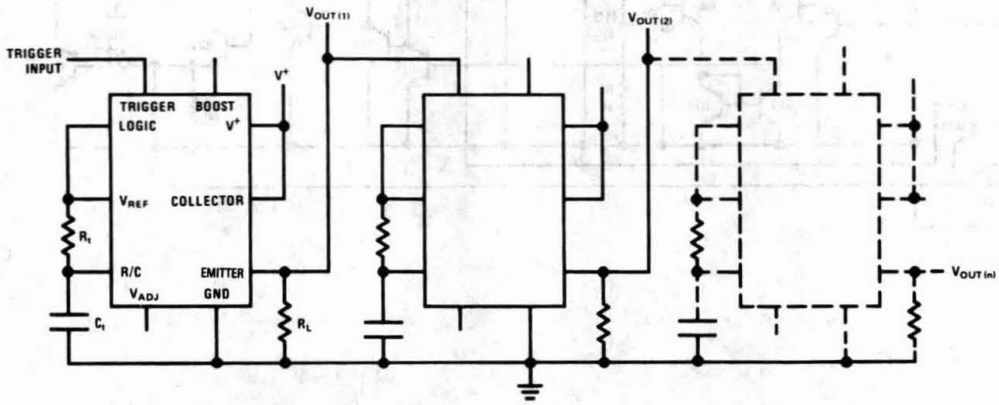
Chain of Timers

The LM122 can be connected as a chain of timers quite easily with no interface required. In *Figure 20A* and *20B*, two possible connections are shown. In both cases, the output of the timer is low during the timing period so that the positive going signal at the end of the timing period can trigger the next timer. There is no limitation on the timing period of one timer with respect to any other timer before or after it, because the trigger input to any timer can be high or low when that timer ends its timing period.



TL/H/7768–31

(a)



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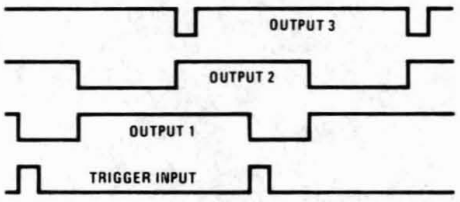

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(b)

FIGURE 20. Chain of Timers

National Semiconductor

LM555/LM555C Timer

General Description

The LM555 is a highly stable device for generating accurate time delays or oscillation. Additional terminals are provided for triggering or resetting if desired. In the time delay mode of operation, the time is precisely controlled by one external resistor and capacitor. For astable operation as an oscillator, the free running frequency and duty cycle are accurately controlled with two external resistors and one capacitor. The circuit may be triggered and reset on falling waveforms, and the output circuit can source or sink up to 200 mA or drive TTL circuits.

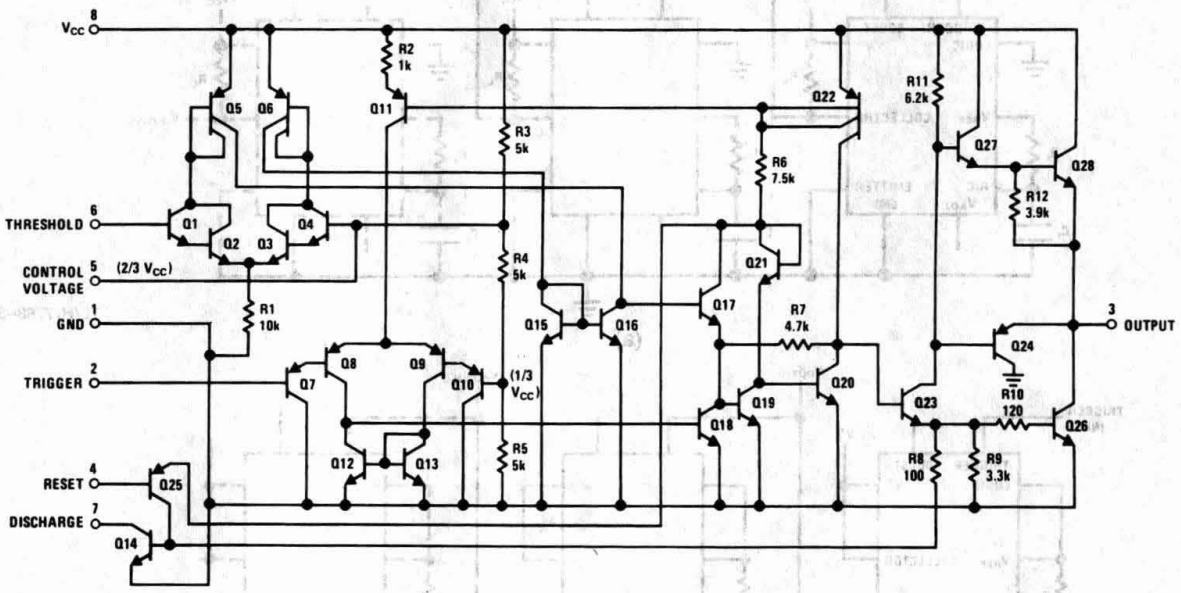
Features

- Direct replacement for SE555/NE555
- Timing from microseconds through hours
- Operates in both astable and monostable modes
- Adjustable duty cycle
- Output can source or sink 200 mA
- Output and supply TTL compatible
- Temperature stability better than 0.005% per °C
- Normally on and normally off output

Applications

- Precision timing
- Pulse generation
- Sequential timing
- Time delay generation
- Pulse width modulation
- Pulse position modulation
- Linear ramp generator

Schematic Diagram



TL/H/7851–1

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage +18V

Power Dissipation (Note 1)
- LM555H, LM555CH 760 mW
- LM555, LM555CN 1180 mW

Operating Temperature Ranges
- LM555C 0°C to +70°C
- LM555 −55°C to + 125°C

Storage Temperature Range −65°C to +150°C

Soldering Information
- Dual-In-Line Package
  - Soldering (10 Seconds) 260°C
- Small Outline Package
  - Vapor Phase (60 Seconds) 215°C
  - Infrared (15 Seconds) 220°C

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.

Electrical Characteristics (T_A = 25°C, V_{CC} = +5V to +15V, unless othewise specified)

Parameter	Conditions	Limits						Units
		LM555			LM555C			
		Min	Typ	Max	Min	Typ	Max	
Supply Voltage		4.5		18	4.5		16	V
Supply Current	V_{CC} = 5V, R_L = ∞		3	5		3	6	mA
	V_{CC} = 15V, R_L = ∞ (Low State) (Note 2)		10	12		10	15	mA
Timing Error, Monostable								
Initial Accuracy			0.5			1		%
Drift with Temperature	R_A = 1k to 100 kΩ, C = 0.1 μF, (Note 3)		30			50		ppm/°C
Accuracy over Temperature			1.5			1.5		%
Drift with Supply			0.05			0.1		%/V
Timing Error, Astable								
Initial Accuracy			1.5			2.25		%
Drift with Temperature	R_A, R_B = 1k to 100 kΩ, C = 0.1 μF, (Note 3)		90			150		ppm/°C
Accuracy over Temperature			2.5			3.0		%
Drift with Supply			0.15			0.30		%/V
Threshold Voltage			0.667			0.667		x V_{CC}
Trigger Voltage	V_{CC} = 15V	4.8	5	5.2		5		V
	V_{CC} = 5V	1.45	1.67	1.9		1.67		V
Trigger Current			0.01	0.5		0.5	0.9	μA
Reset Voltage		0.4	0.5	1	0.4	0.5	1	V
Reset Current			0.1	0.4		0.1	0.4	mA
Threshold Current	(Note 4)		0.1	0.25		0.1	0.25	μA
Control Voltage Level	V_{CC} = 15V	9.6	10	10.4	9	10	11	V
	V_{CC} = 5V	2.9	3.33	3.8	2.6	3.33	4	V
Pin 7 Leakage Output High			1	100		1	100	nA
Pin 7 Sat (Note 5)								
Output Low	V_{CC} = 15V, I_7 = 15 mA		150			180		mV
Output Low	V_{CC} = 4.5V, I_7 = 4.5 mA		70	100		80	200	mV

Electrical Characteristics $T_A = 25°C$, $V_{CC} = +5V$ to $+15V$, (unless othewise specified) (Continued)

Parameter	Conditions	Limits						Units
		LM555			LM555C			
		Min	Typ	Max	Min	Typ	Max	
Output Voltage Drop (Low)	$V_{CC} = 15V$							
	$I_{SINK} = 10$ mA		0.1	0.15		0.1	0.25	V
	$I_{SINK} = 50$ mA		0.4	0.5		0.4	0.75	V
	$I_{SINK} = 100$ mA		2	2.2		2	2.5	V
	$I_{SINK} = 200$ mA		2.5			2.5		V
	$V_{CC} = 5V$							
	$I_{SINK} = 8$ mA		0.1	0.25				V
	$I_{SINK} = 5$ mA					0.25	0.35	V
Output Voltage Drop (High)	$I_{SOURCE} = 200$ mA, $V_{CC} = 15V$		12.5			12.5		V
	$I_{SOURCE} = 100$ mA, $V_{CC} = 15V$	13	13.3		12.75	13.3		V
	$V_{CC} = 5V$	3	3.3		2.75	3.3		V
Rise Time of Output			100			100		ns
Fall Time of Output			100			100		ns

Note 1: For operating at elevated temperatures the device must be derated above 25°C based on a +150°C maximum junction temperature and a thermal resistance of 164°c/w (T0-5), 106°c/w (DIP) and 170°c/w (S0-8) junction to ambient.

Note 2: Supply current when output high typically 1 mA less at $V_{CC} = 5V$.

Note 3: Tested at $V_{CC} = 5V$ and $V_{CC} = 15V$.

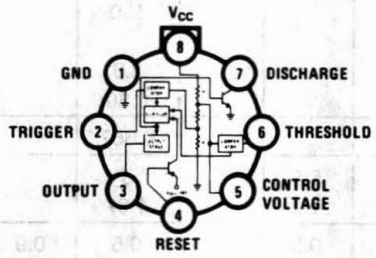
Note 4: This will determine the maximum value of $R_A + R_B$ for 15V operation. The maximum total ($R_A + R_B$) is 20 MΩ.

Note 5: No protection against excessive pin 7 current is necessary providing the package dissipation rating will not be exceeded.

Note 6: Refer to RETS555X drawing of military LM555H and LM555J versions for specifications.

Connection Diagrams

Metal Can Package

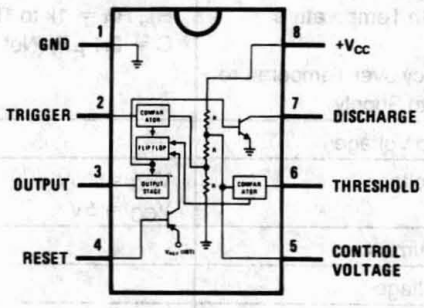


TL/H/7851–2

Top View

Order Number LM555H or LM555CH
See NS Package Number H08C

Dual-In-Line and Small Outline Packages



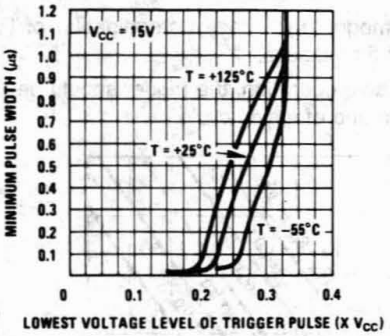
TL/H/7851–3

Top View

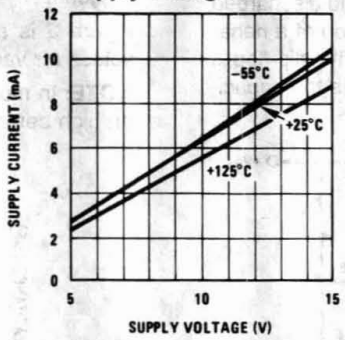
Order Number LM555J, LM555CJ, LM555CM or LM555CN
See NS Package Number J08A, M08A or N08E

Typical Performance Characteristics

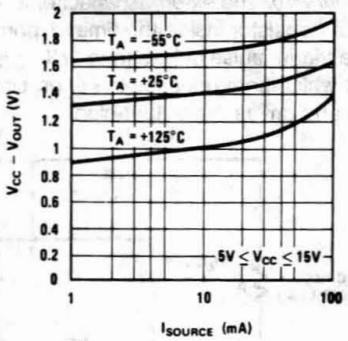
Minimuim Pulse Width Required for Triggering



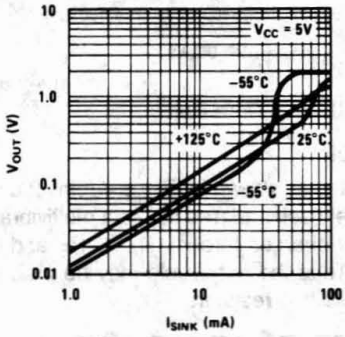
Supply Current vs Supply Voltage



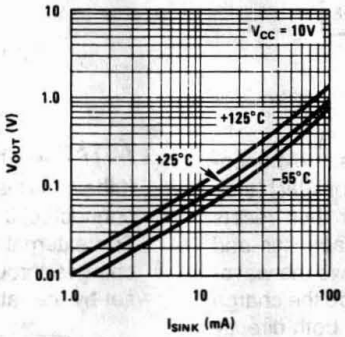
High Output Voltage vs Output Source Current



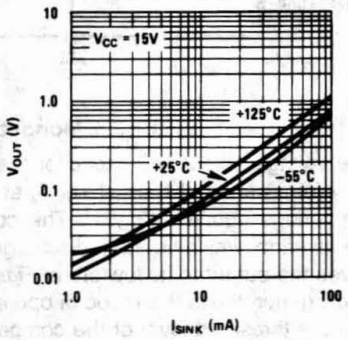
Low Output Voltage vs Output Sink Current



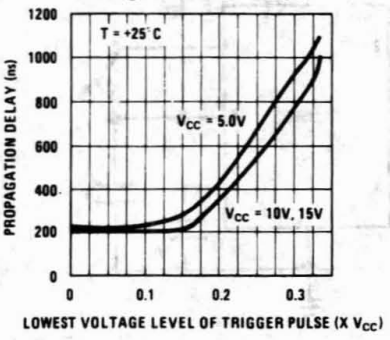
Low Output Voltage vs Output Sink Current



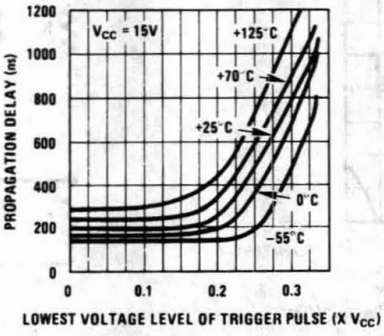
Low Output Voltage vs Output Sink Current



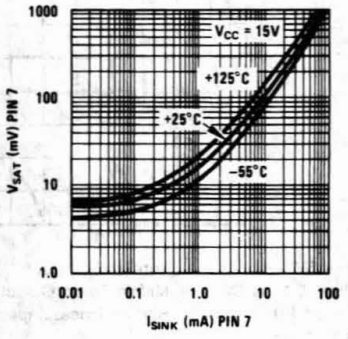
Output Propagation Delay vs Voltage Level of Trigger Pulse



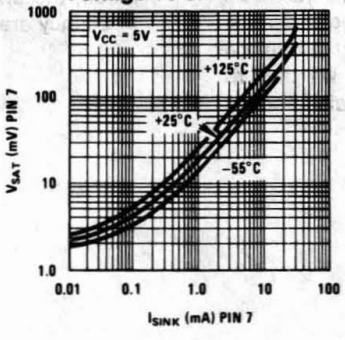
Output Propagation Delay vs Voltage Level of Trigger Pulse



Discharge Transistor (Pin 7) Voltage vs Sink Current



Discharge Transistor (Pin 7) Voltage vs Sink Current

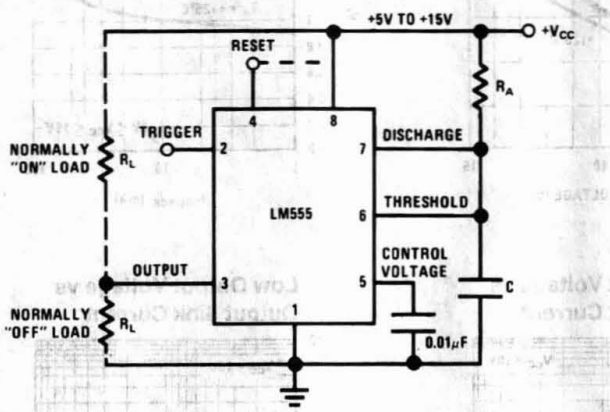


TL/H/7851–4

Applications Information

MONOSTABLE OPERATION

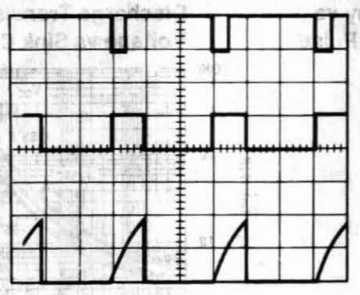
In this mode of operation, the timer functions as a one-shot *(Figure 1)*. The external capacitor is initially held discharged by a transistor inside the timer. Upon application of a negative trigger pulse of less than 1/3 V_{CC} to pin 2, the flip-flop is set which both releases the short circuit across the capacitor and drives the output high.



TL/H/7851–5

FIGURE 1. Monostable

The voltage across the capacitor then increases exponentially for a period of t = 1.1 R_A C, at the end of which time the voltage equals 2/3 V_{CC}. The comparator then resets the flip-flop which in turn discharges the capacitor and drives the output to its low state. *Figure 2* shows the waveforms generated in this mode of operation. Since the charge and the threshold level of the comparator are both directly proportional to supply voltage, the timing internal is independent of supply.



TL/H/7851–6

V_{CC} = 5V
TIME = 0.1 ms/DIV.
R_A = 9.1 kΩ
C = 0.01 μF

Top Trace: Input 5V/Div.
Middle Trace: Output 5V/Div.
Bottom Trace: Capacitor Voltage 2V/Div.

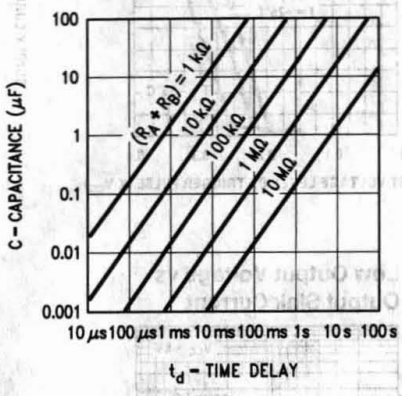
FIGURE 2. Monostable Waveforms

During the timing cycle when the output is high, the further application of a trigger pulse will not effect the circuit so long as the trigger input is returned high at least 10 μs before the end of the timing interval. However the circuit can be reset during this time by the application of a negative pulse to the reset terminal (pin 4). The output will then remain in the low state until a trigger pulse is again applied.

When the reset function is not in use, it is recommended that it be connected to V_{CC} to avoid any possibility of false triggering.

Figure 3 is a nomograph for easy determination of R, C values for various time delays.

NOTE: In monostable operation, the trigger should be driven high before the end of timing cycle.

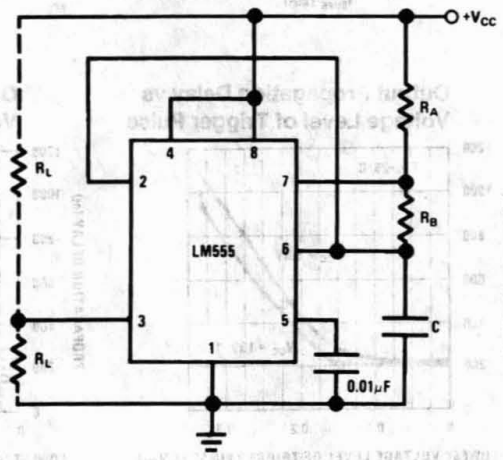


TL/H/7851–7

FIGURE 3. Time Delay

ASTABLE OPERATION

If the circuit is connected as shown in *Figure 4* (pins 2 and 6 connected) it will trigger itself and free run as a multivibrator. The external capacitor charges through R_A + R_B and discharges through R_B. Thus the duty cycle may be precisely set by the ratio of these two resistors.



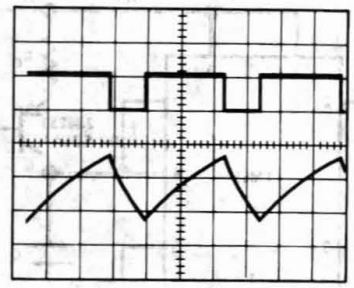
TL/H/7851–8

FIGURE 4. Astable

In this mode of operation, the capacitor charges and discharges between 1/3 V_{CC} and 2/3 V_{CC}. As in the triggered mode, the charge and discharge times, and therefore the frequency are independent of the supply voltage.

Applications Information (Continued)

Figure 5 shows the waveforms generated in this mode of operation.



TL/H/7851–9

V_{CC} = 5V
TIME = 20 μs/DIV.
R_A = 3.9 kΩ
R_B = 3 kΩ
C = 0.01 μF

Top Trace: Output 5V/Div.
Bottom Trace: Capacitor Voltage 1V/Div.

FIGURE 5. Astable Waveforms

The charge time (output high) is given by:

$$t_1 = 0.693\,(R_A + R_B)\,C$$

And the discharge time (output low) by:

$$t_2 = 0.693\,(R_B)\,C$$

Thus the total period is:

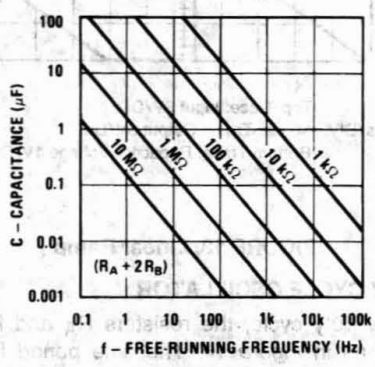
$$T = t_1 + t_2 = 0.693\,(R_A + 2R_B)\,C$$

The frequency of oscillation is:

$$f = \frac{1}{T} = \frac{1.44}{(R_A + 2R_B)\,C}$$

Figure 6 may be used for quick determination of these RC values.

The duty cycle is: $D = \dfrac{R_B}{R_A + 2R_B}$

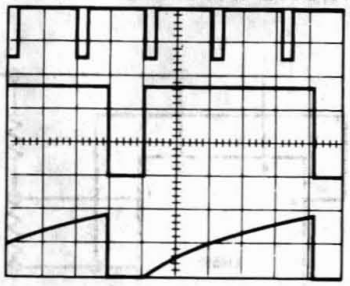


TL/H/7851–10

FIGURE 6. Free Running Frequency

FREQUENCY DIVIDER

The monostable circuit of *Figure 1* can be used as a frequency divider by adjusting the length of the timing cycle. *Figure 7* shows the waveforms generated in a divide by three circuit.



TL/H/7851–11

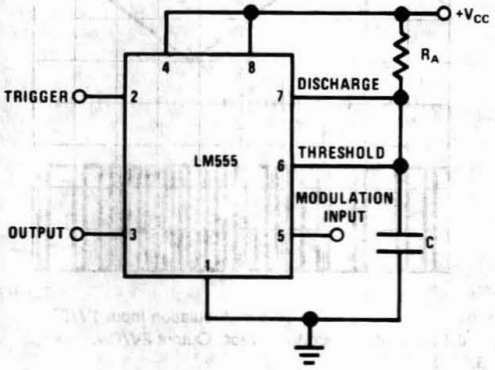
V_{CC} = 5V
TIME = 20 μs/DIV.
R_A = 9.1 kΩ
C = 0.01 μF

Top Trace: Input 4V/Div.
Middle Trace: Output 2V/Div.
Bottom Trace: Capacitor 2V/Div.

FIGURE 7. Frequency Divider

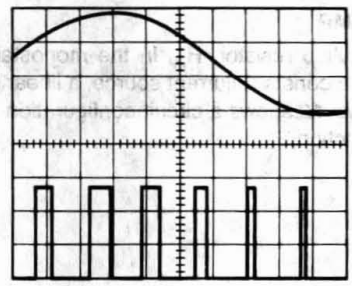
PULSE WIDTH MODULATOR

When the timer is connected in the monostable mode and triggered with a continuous pulse train, the output pulse width can be modulated by a signal applied to pin 5. *Figure 8* shows the circuit, and in *Figure 9* are some waveform examples.



TL/H/7851–12

FIGURE 8. Pulse Width Modulator



TL/H/7851–13

V_{CC} = 5V
TIME = 0.2 ms/DIV.
R_A = 9.1 kΩ
C = 0.01 μF

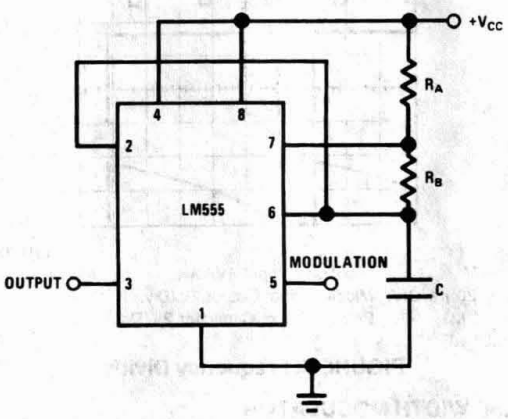
Top Trace: Modulation 1V/Div.
Bottom Trace: Output Voltage 2V/Div.

FIGURE 9. Pulse Width Modulator

PULSE POSITION MODULATOR

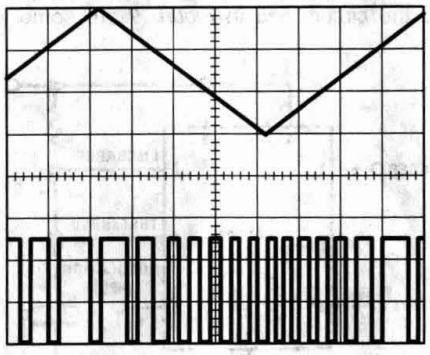
This application uses the timer connected for astable operation, as in *Figure 10,* with a modulating signal again applied to the control voltage terminal. The pulse position varies with the modulating signal, since the threshold voltage and hence the time delay is varied. *Figure 11* shows the waveforms generated for a triangle wave modulation signal.

Applications Information (Continued)



TL/H/7851–14

FIGURE 10. Pulse Position Modulator



TL/H/7851–15

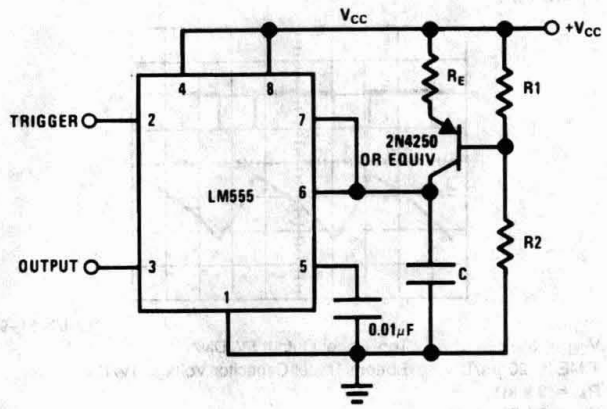
V_{CC} = 5V
TIME = 0.1 ms/DIV.
R_A = 3.9 kΩ
R_B = 3 kΩ
C = 0.01 μF

Top Trace: Modulation Input 1V/Div.
Bottom Trace: Output 2V/Div.

FIGURE 11. Pulse Position Modulator

LINEAR RAMP

When the pullup resistor, R_A, in the monostable circuit is replaced by a constant current source, a linear ramp is generated. *Figure 12* shows a circuit configuration that will perform this function.



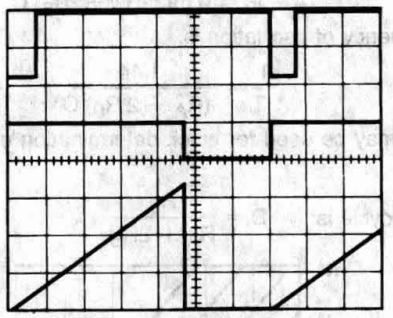
TL/H/7851–16

FIGURE 12

Figure 13 shows waveforms generated by the linear ramp. The time interval is given by:

$$T = \frac{2/3\, V_{CC}\, R_E\, (R_1 + R_2)\, C}{R_1\, V_{CC} - V_{BE}\, (R_1 + R_2)}$$

$$V_{BE} \cong 0.6V$$



TL/H/7851–17

V_{CC} = 5V
TIME = 20 μs/DIV.
R_1 = 47 kΩ
R_2 = 100 kΩ
R_E = 2.7 kΩ
C = 0.01 μF

Top Trace: Input 3V/Div.
Middle Trace: Output 5V/Div.
Bottom Trace: Capacitor Voltage 1V/Div.

FIGURE 13. Linear Ramp

50% DUTY CYCLE OSCILLATOR

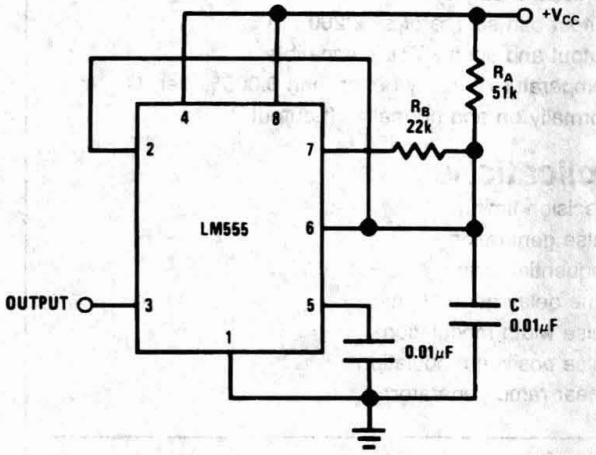
For a 50% duty cycle, the resistors R_A and R_B may be connected as in *Figure 14*. The time period for the out-

Applications Information (Continued)

put high is the same as previous, $t_1 = 0.693\ R_A\ C$. For the output low it is $t_2 =$

$$\left[(R_A\ R_B)/(R_A + R_B)\right] C\ \ell n \left[\frac{R_B - 2R_A}{2R_B - R_A}\right]$$

Thus the frequency of oscillation is $f = \frac{1}{t_1 + t_2}$



TL/H/7851–18

FIGURE 14. 50% Duty Cycle Oscillator

Note that this circuit will not oscillate if R_B is greater than 1/2 R_A because the junction of R_A and R_B cannot bring pin 2 down to 1/3 V_{CC} and trigger the lower comparator.

ADDITIONAL INFORMATION

Adequate power supply bypassing is necessary to protect associated circuitry. Minimum recommended is 0.1 μF in parallel with 1 μF electrolytic.

Lower comparator storage time can be as long as 10 μs when pin 2 is driven fully to ground for triggering. This limits the monostable pulse width to 10 μs minimum.

Delay time reset to output is 0.47 μs typical. Minimum reset pulse width must be 0.3 μs, typical.

Pin 7 current switches within 30 ns of the output (pin 3) voltage.

National Semiconductor

LM556/LM556C Dual Timer

General Description

The LM556 Dual timing circuit is a highly stable controller capable of producing accurate time delays or oscillation. The 556 is a dual 555. Timing is provided by an external resistor and capacitor for each timing function. The two timers operate independently of each other sharing only V_{CC} and ground. The circuits may be triggered and reset on falling waveforms. The output structures may sink or source 200 mA.

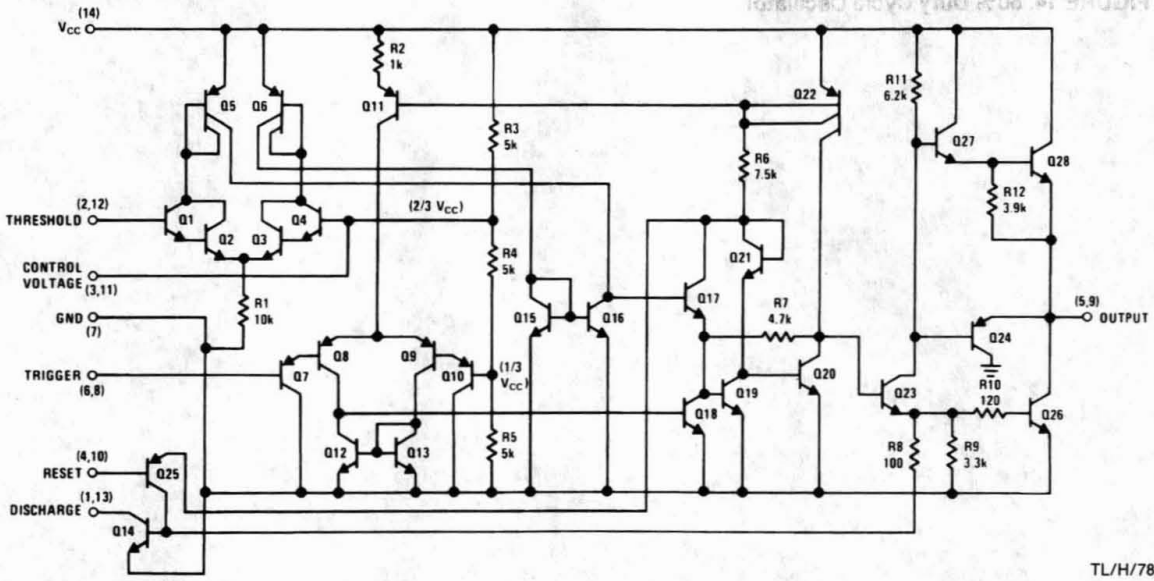
Features

- Direct replacement for SE556/NE556
- Timing from microseconds through hours
- Operates in both astable and monostable modes
- Replaces two 555 timers
- Adjustable duty cycle
- Output can source or sink 200 mA
- Output and supply TTL compatible
- Temperature stability better than 0.005% per °C
- Normally on and normally off output

Applications

- Precision timing
- Pulse generation
- Sequential timing
- Time delay generation
- Pulse width modulation
- Pulse position modulation
- Linear ramp generator

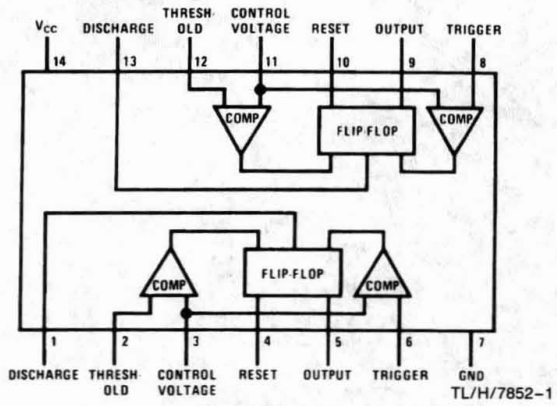
Schematic Diagram



TL/H/7852–2

Connection Diagram

Dual-In-Line and Small Outline Packages



TL/H/7852–1

Top View

Order Number LM556J or LM556CJ
See NS Package Number J14A

Order Number LM556CM
See NS Package Number M14A

Order Number LM556CN
See NS Package Number N14A

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage +18V

Power Dissipation (Note 1)
- LM556J, LM556CJ 1785 mW
- LM556CN 1620 mW

Operating Temperature Ranges
- LM556C 0°C to +70°C
- LM556 −55°C to +125°C

Storage Temperature Range −65°C to +150°C

Soldering Information
- Dual-In-Line Package
  - Soldering (10 seconds) 260°C
- Small Outline Package
  - Vapor phase (60 seconds) 215°C
  - Infrared (15 seconds) 220°C

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.

Electrical Characteristics (T_A = 25°C, V_{CC} = +5V to +15V, unless otherwise specified)

Parameter	Conditions	LM556			LM556C			Units
		Min	Typ	Max	Min	Typ	Max	
Supply Voltage		4.5		18	4.5		16	V
Supply Current	V_{CC} = 5V, R_L = ∞		3	5		3	6	mA
(Each Timer Section)	V_{CC} = 15V, R_L = ∞ (Low State) (Note 2)		10	11		10	14	mA
Timing Error, Monostable								
Initial Accuracy			0.5			0.75		%
Drift with Temperature	R_A = 1k to 100 kΩ, C = 0.1 μF, (Note 3)		30			50		ppm/°C
Accuracy over Temperature			1.5			1.5		%
Drift with Supply			0.05			0.1		%/V
Timing Error, Astable								
Initial Accuracy			1.5			2.25		%
Drift with Temperature	R_A, R_B = 1k to 100 kΩ,		90			150		ppm/°C
Accuracy over Temperature	C = 0.1 μF, (Note 3)		2.5			3.0		%
Drift with Supply			0.15			0.30		%/V
Trigger Voltage	V_{CC} = 15V	4.8	5	5.2	4.5	5	5.5	V
	V_{CC} = 5V	1.45	1.67	1.9	1.25	1.67	2.0	V
Trigger Current			0.1	0.5		0.2	1.0	μA
Reset Voltage	(Note 4)	0.4	0.5	1	0.4	0.5	1	V
Reset Current			0.1	0.4		0.1	0.6	mA
Threshold Current	V_{TH} = V-Control (Note 5)		0.03	0.1		0.03	0.1	μA
	V_{TH} = 11.2V			250			250	nA
Control Voltage Level and	V_{CC} = 15V	9.6	10	10.4	9	10	11	V
Threshold Voltage	V_{CC} = 5V	2.9	3.33	3.8	2.6	3.33	4	V
Pin 1, 13 Leakage Output High			1	100		1	100	nA
Pin 1, 13 Sat	(Note 6)							
Output Low	V_{CC} = 15V, I = 15 mA		150	240		180	300	mV
Output Low	V_{CC} = 4.5V, I = 4.5 mA		70	100		80	200	mV

Electrical Characteristics (T_A = 25°C, V_{CC} = +5V to +15V, unless otherwise specified) (Continued)

Parameter	Conditions	LM556			LM556C			Units
		Min	Typ	Max	Min	Typ	Max	
Output Voltage Drop (Low)	V_{CC} = 15V							
	I_{SINK} = 10 mA		0.1	0.15		0.1	0.25	V
	I_{SINK} = 50 mA		0.4	0.5		0.4	0.75	V
	I_{SINK} = 100 mA		2	2.25		2	2.75	V
	I_{SINK} = 200 mA		2.5			2.5		V
	V_{CC} = 5V							
	I_{SINK} = 8 mA		0.1	0.25				V
	I_{SINK} = 5 mA					0.25	0.35	V
Output Voltage Drop (High)	I_{SOURCE} = 200 mA, V_{CC} = 15V		12.5			12.5		V
	I_{SOURCE} = 100 mA, V_{CC} = 15V	13	13.3		12.75	13.3		V
	V_{CC} = 5V	3	3.3		2.75	3.3		V
Rise Time of Output			100			100		ns
Fall Time of Output			100			100		ns
Matching Characteristics	(Note 7)							
Initial Timing Accuracy			0.05	0.2		0.1	2.0	%
Timing Drift with Temperature			±10			±10		ppm/°C
Drift with Supply Voltage			0.1	0.2		0.2	0.5	%/V

Note 1: For operating at elevated temperatures the device must be derated based on a +150°C maximum junction temperature and a thermal resistance of 70°C/W (Ceramic), 77°C/W (Plastic DIP) and 110°C/W (SO-14 Narrow).

Note 2: Supply current when output high typically 1 mA less at V_{CC} = 5V.

Note 3: Tested at V_{CC} = 5V and V_{CC} = 15V.

Note 4: As reset voltage lowers, timing is inhibited and then the output goes low.

Note 5: This will determine the maximum value of $R_A + R_B$ for 15V operation. The maximum total ($R_A + R_B$) is 20 MΩ.

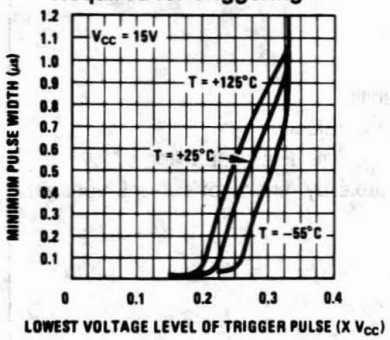
Note 6: No protection against excessive pin 1, 13 current is necessary providing the package dissipation rating will not be exceeded.

Note 7: Matching characteristics refer to the difference between performance characteristics of each timer section.

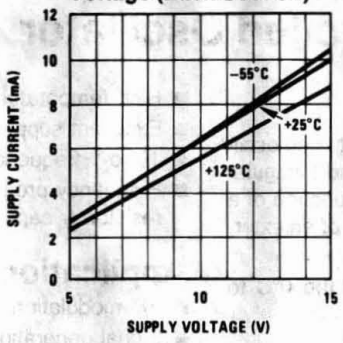
Note 8: Refer to RETS556X drawing for specifications of military LM556J version.

Typical Performance Characteristics

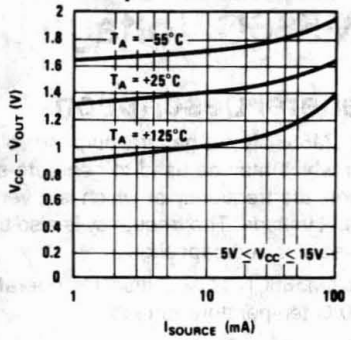
Minimum Pulse Width Required for Triggering



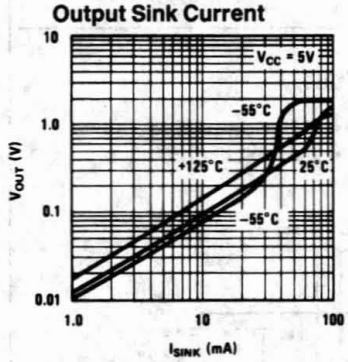
Supply Current vs Supply Voltage (Each Section)



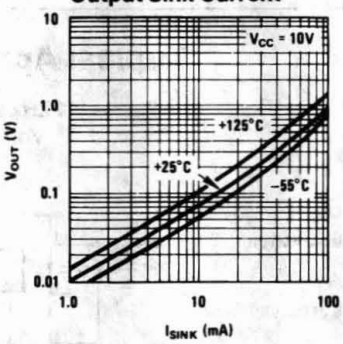
High Output Voltage vs Output Source Current



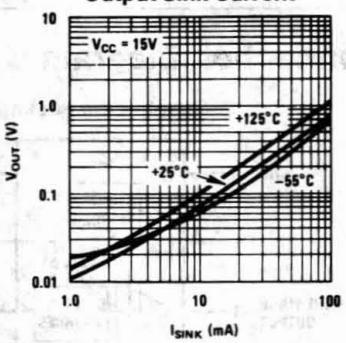
Low Output Voltage vs Output Sink Current



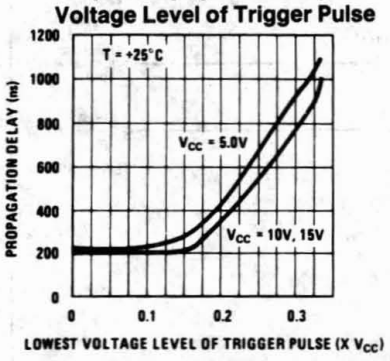
Low Output Voltage vs Output Sink Current



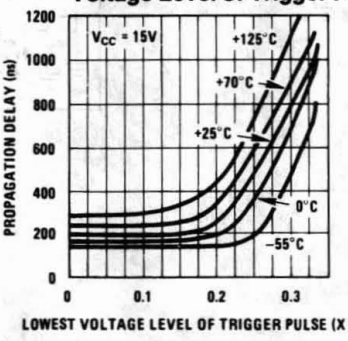
Low Output Voltage vs Output Sink Current



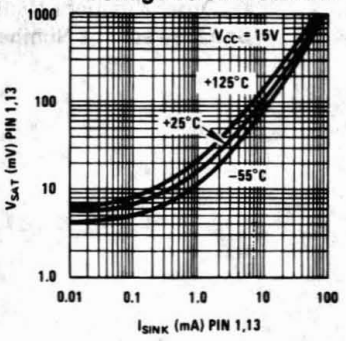
Output Propagation Delay vs Voltage Level of Trigger Pulse



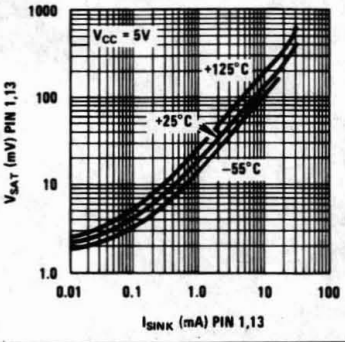
Output Propagation Delay vs Voltage Level of Trigger Pulse



Discharge Transistor (Pin 1, 13) Voltage vs Sink Current



Discharge Transistor (Pin 1, 13) Voltage vs Sink Current



TL/H/7852–3

4

National Semiconductor

LM566C Voltage Controlled Oscillator

General Description

The LM566CN is a general purpose voltage controlled oscillator which may be used to generate square and triangular waves, the frequency of which is a very linear function of a control voltage. The frequency is also a function of an external resistor and capacitor.

The LM566CN is specified for operation over the 0°C to +70°C temperature range.

Features

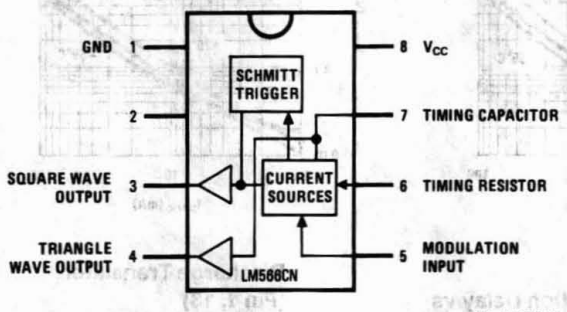
- Wide supply voltage range: 10V to 24V
- Very linear modulation characteristics
- High temperature stability
- Excellent supply voltage rejection
- 10 to 1 frequency range with fixed capacitor
- Frequency programmable by means of current, voltage, resistor or capacitor

Applications

- FM modulation
- Signal generation
- Function generation
- Frequency shift keying
- Tone generation

Connection Diagram

Dual-In-Line Package

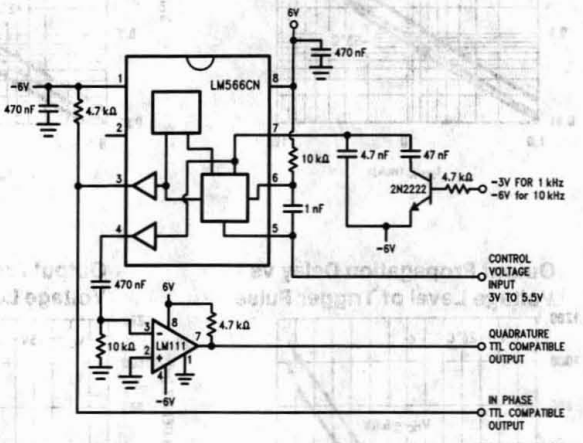


TL/H/7854–2

Order Number LM566CN
See NS Package Number N08E

Typical Application

1 kHz and 10 kHz TTL Compatible Voltage Controlled Oscillator



TL/H/7854–3

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Power Supply Voltage	26V
Power Dissipation (Note 1)	1000 mW
Operating Temperature Range, LM566CN	0°C to +70°C
Lead Temperature (Soldering, 10 sec.)	+260°C

Electrical Characteristics V_{CC} = 12V, T_A = 25°C, AC Test Circuit

Parameter	Conditions	LM566C			Units
		Min	Typ	Max	
Maximum Operating Frequency	R0 = 2k C0 = 2.7 pF	0.5	1		MHz
VCO Free-Running Frequency	C_O = 1.5 nF R_O = 20k f_O = 10 kHz	−30	0	+30	%
Input Voltage Range Pin 5		¾ V_{CC}		V_{CC}	
Average Temperature Coefficient of Operating Frequency			200		ppm/°C
Supply Voltage Rejection	10–20V		0.1	2	%/V
Input Impedance Pin 5		0.5	1		MΩ
VCO Sensitivity	For Pin 5, From 8–10V, f_O = 10 kHz	6.0	6.6	7.2	kHz/V
FM Distortion	±10% Deviation		0.2	1.5	%
Maximum Sweep Rate			1		MHz
Sweep Range			10:1		
Output Impedance Pin 3			50		Ω
Pin 4			50		Ω
Square Wave Output Level	R_{L1} = 10k	5.0	5.4		Vp-p
Triangle Wave Output Level	R_{L2} = 10k	2.0	2.4		Vp-p
Square Wave Duty Cycle		40	50	60	%
Square Wave Rise Time			20		ns
Square Wave Fall Time			50		ns
Triangle Wave Linearity	+1V Segment at ½ V_{CC}		0.5		%

Note 1: The maximum junction temperature of the LM566CN is 150°C. For operation at elevated junction temperatures, maximum power dissipation must be derated based on a thermal resistance of 115°C/W, junction to ambient.

Applications Information

The LM566CN may be operated from either a single supply as shown in this test circuit, or from a split (±) power supply. When operating from a split supply, the square wave output (pin 3) is TTL compatible (2 mA current sink) with the addition of a 4.7 kΩ resistor from pin 3 to ground.

A 0.001 μF capacitor is connected between pins 5 and 6 to prevent parasitic oscillations that may occur during VCO switching.

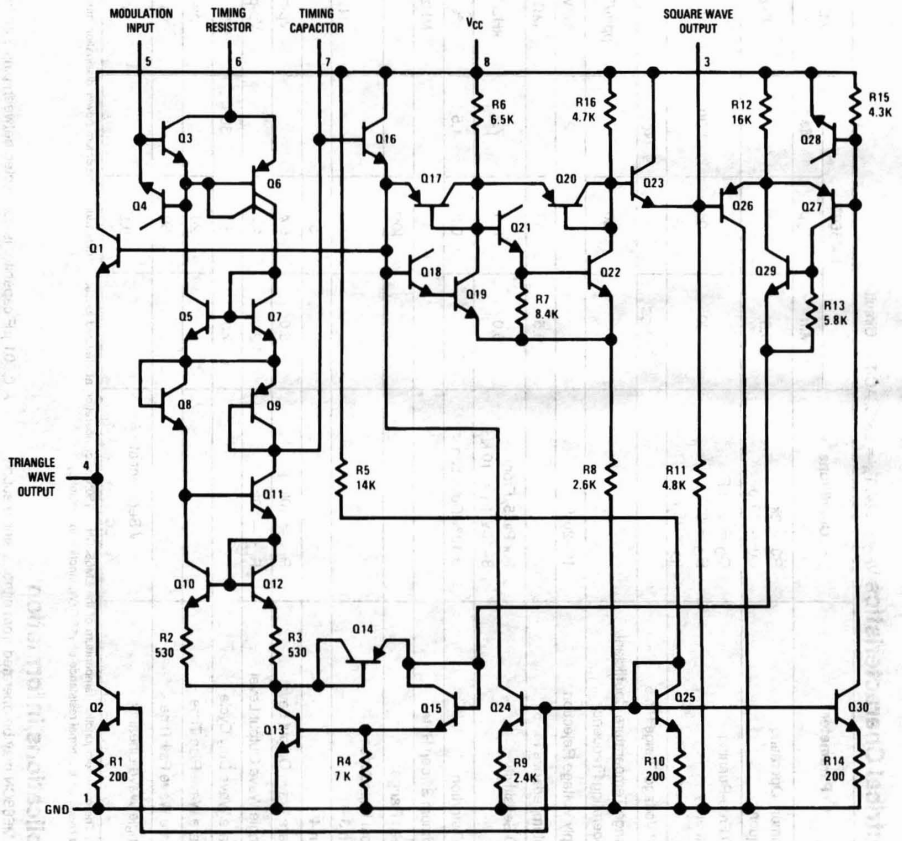
$$f_O = \frac{2.4(V^+ - V_5)}{R_O C_O V^+}$$

where

$2K < R_O < 20K$

and V_5 is voltage between pin 5 and pin 1.

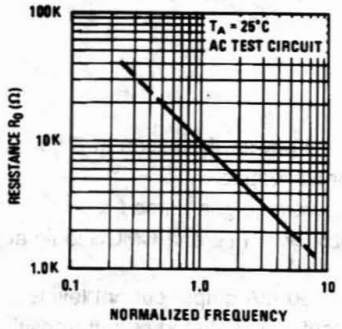
Schematic Diagram



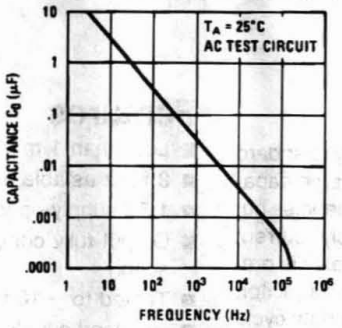
TL/H/7854–1

Typical Performance Characteristics

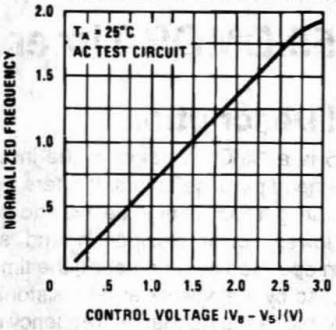
Operating Frequency as a Function of Timing Resistor



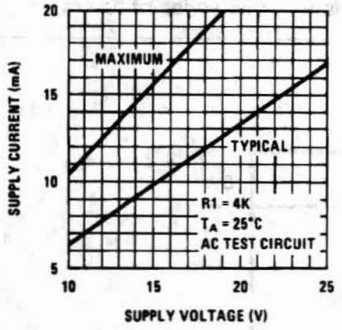
Operating Frequency as a Function of Timing Capacitor



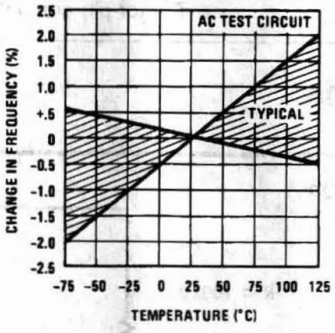
Normalized Frequency as a Function of Control Voltage



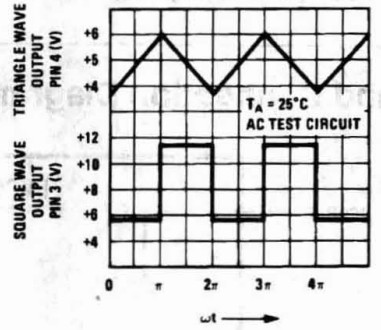
Power Supply Current



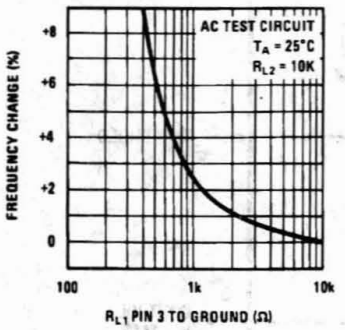
Temperature Stability



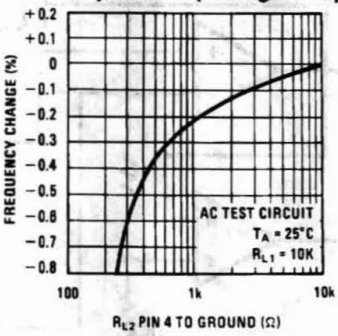
VCO Waveforms



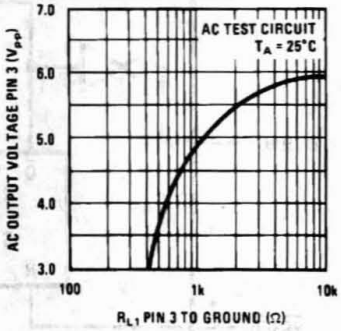
Frequency Stability vs Load Resistance (Square Wave Output)



Frequency Stability vs Load Impedance (Triangle Output)

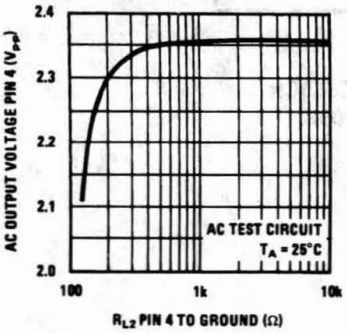


Square Wave Output Characteristics



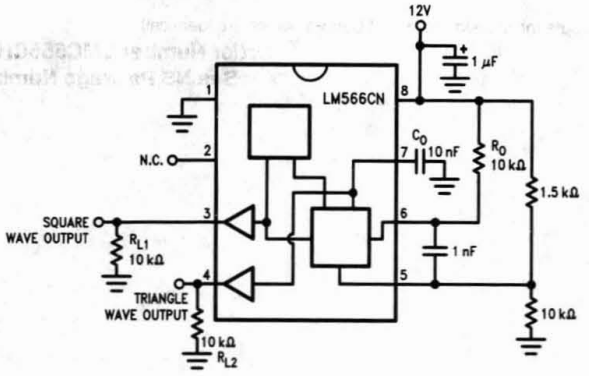
TL/H/7854–4

Triangle Wave Output Characteristics



TL/H/7854–5

AC Test Circuit



TL/H/7854–6

National Semiconductor

PRELIMINARY

LMC555 CMOS Timer

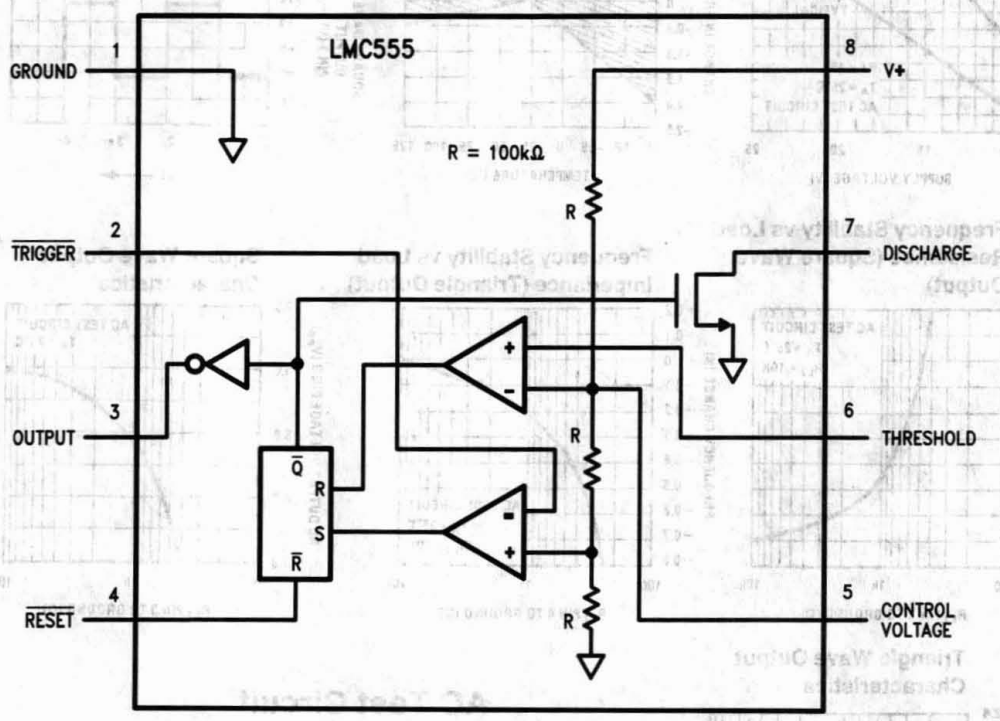
General Description

The LMC555 is a CMOS version of the industry standard 555 series general purpose timers. It offers the same capability of generating accurate time delays and frequencies but with much lower power dissipation and supply current spikes. When operated as a one-shot, the time delay is precisely controlled by a single external resistor and capacitor. In the astable mode the oscillation frequency and duty cycle are accurately set by two external resistors and one capacitor. The use of National Semiconductor's LMCMOS™ process extends both the frequency range and low supply capability.

Features

- Less than 1 mW typical power dissipation at 5V supply
- 3 MHz astable frequency capability
- 1.5V supply operating voltage guaranteed
- Output fully compatible with TTL and CMOS logic at 5V supply
- Tested to −10 mA, +50 mA output current levels
- Reduced supply current spikes during output transitions
- Extremely low reset, trigger, and threshold currents
- Excellent temperature stability
- Pin-for-pin compatible with 555 series of timers

Block and Connection Diagrams



TL/H/8669–1

(Pinouts for Molded and Metal Can Packages are identical)

Order Number LMC555CH, LMC555CM or LMC555CN
See NS Package Number H08C, M08A or N08E

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage, V8	15V
Input Voltages, V2, V4, V5, V6	−0.3V to V_S + 0.3V
Output Voltages, V3, V7	15V
Output Current I3, I7	100 mA
Operating Temperature Range (Note 1)	−40°C to +85°C*
Storage Temperature Range	−65°C to +150°C

Soldering Information

Dual-In-Line Package	
Soldering (10 seconds)	260°C
Small Outline Package	
Vapor Phase (60 seconds)	215°C
Infrared (15 seconds)	220°C

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.

Electrical Characteristics Test Circuit, T = 25°C, all switches open, $\overline{\text{RESET}}$ to V_S unless otherwise noted

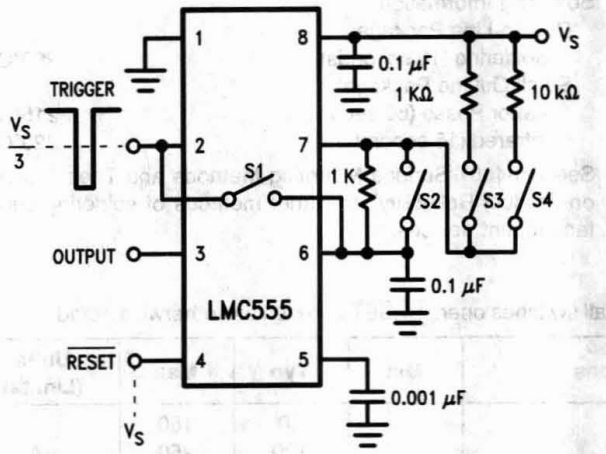
Symbol	Parameter	Conditions	Min	Typ	Max	Units (Limits)
I8	Supply Current	V_S = 1.5V V_S = 5V V_S = 12V		50 100 150	150 250 400	μA
V5	Control Voltage	V_S = 1.5V V_S = 5V V_S = 12V	0.8 2.9 7.4	1.0 3.3 8.0	1.2 3.8 8.6	V
V7	Discharge Saturation Voltage	V_S = 1.5V, I_7 = 1 mA V_S = 5V, I_7 = 10 mA		75 150	150 300	mV
$V3_L$	Output Voltage (Low)	V_S = 1.5V, I_3 = 1 mA V_S = 5V, I_3 = 8 mA V_S = 12V, I_3 = 50 mA		0.2 0.3 1.0	0.4 0.6 2.0	V
$V3_H$	Output Voltage (High)	V_S = 1.5V, I_3 = −0.25 mA V_S = 5V, I_3 = −2 mA V_S = 12V, I_3 = −10 mA	1.0 4.4 10.5	1.25 4.7 11.3		V
V2	Trigger Voltage	V_S = 1.5V V_S = 12V	0.4 3.7	0.5 4.0	0.6 4.3	V
I2	Trigger Current	V_S = 5V		10		pA
V4	Reset Voltage	V_S = 1.5V (Note 2) V_S = 12V	0.4 0.4	0.7 0.75	1.0 1.1	V
I4	Reset Current	V_S = 5V		10		pA
I6	Threshold Current	V_S = 5V		10		pA
I7	Discharge Leakage	V_S = 12V		1.0	100	nA
t	Timing Accuracy	SW 2, 4 Closed V_S = 1.5V V_S = 5V V_S = 12V	 0.9 1.0 1.0	 1.1 1.1 1.1	 1.25 1.20 1.25	ms
Δt/ΔVs	Timing Shift with Supply	V_S = 5V ±1V		0.3		%/V
Δt/ΔT	Timing Shift with Temperature	V_S = 5V −40°C ≤ T ≤ +85°C		75		ppm/°C
f_A	Astable Frequency	SW 1, 3 Closed V_S = 12V	4.0	4.8	5.6	kHz
f_{MAX}	Maximum Frequency	Max. Freq. Test Circuit, V_S = 5V		3.0		MHz
t_R, t_F	Output Rise and Fall Times	Max. Freq. Test Circuit V_S = 5V, C_L = 10 pF		15		ns
t_{PD}	Trigger Propagation Delay	V_S = 5V, Measure Delay from Trigger to Output		100		ns

* Refer to RETSC555X drawing for specifications of military LMC555H version.

Note 1: For operation at elevated temperatures, the device must be derated based on a 150°C maximum junction temperature and a thermal resistance of 111°C/W for the LMC555CN, 167°C/W for the LMC555CH, and 169°C/W for the LMC555CM. Maximum allowable dissipation at 25°C is 1126 mW for the LMC555CN, 755 mW for the LMC555CH, and 740 mW for the LMC555CM.

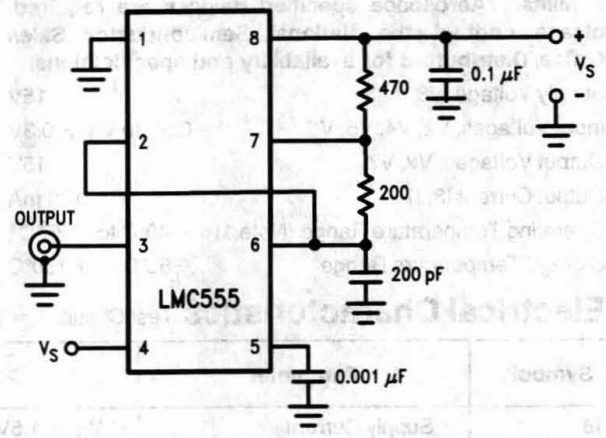
Note 2: If the $\overline{\text{RESET}}$ pin is to be used at temperatures of −20°C and below V_S is required to be 2.0V or greater.

Test Circuit



TL/H/8669–2

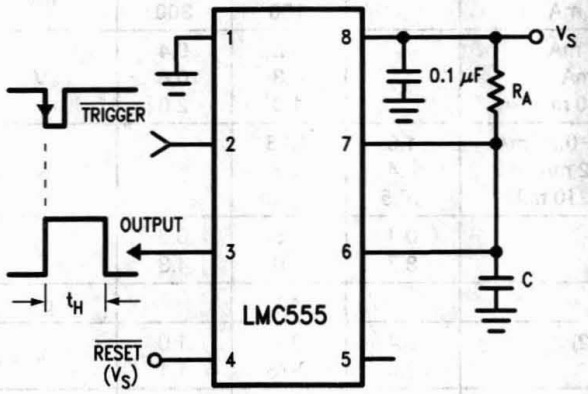
Maximum Frequency Test Circuit



TL/H/8669–3

Typical Applications

Monostable (One-Shot)



TL/H/8669–4

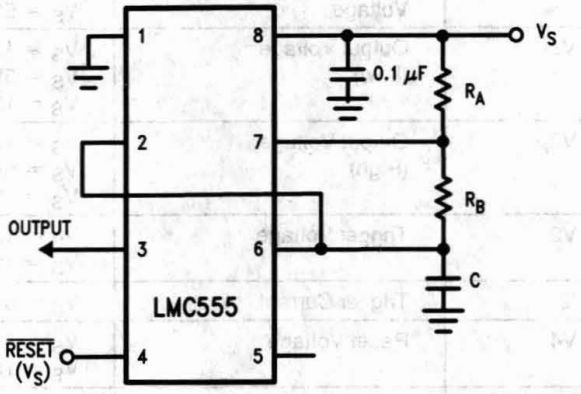
$t_H = 1.1\ R_AC$ (Gives time that output is high following trigger)

$\overline{\text{RESET}}$ overrides $\overline{\text{TRIGGER}}$, which can override THRESHOLD. Therefore, the trigger pulse must be shorter than the desired t_H.

The minimum trigger pulse width is 20 ns.

The minimum reset pulse width is 400 ns.

Variable Duty Cycle Oscillator

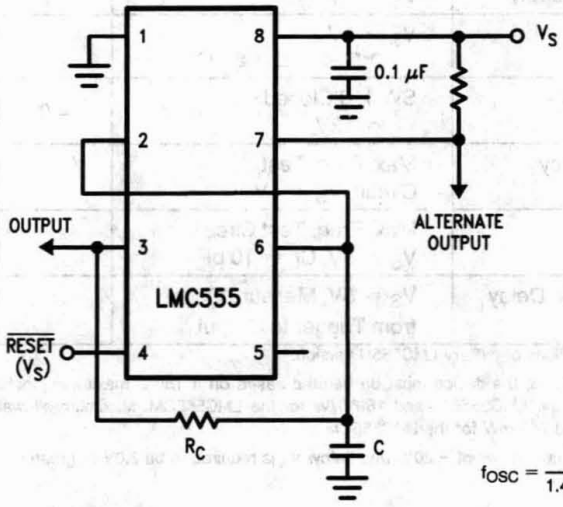


TL/H/8669–5

$$f_{OSC.} = \frac{1.44}{(R_A + 2R_B)C}$$

$$\text{Duty Cycle} = \frac{R_B}{R_A + 2R_B}$$ (Gives fraction of total period that output is low)

50% Duty Cycle Oscillator



$$f_{OSC} = \frac{1}{1.4R_CC}$$

TL/H/8669–6

National Semiconductor

MM5368 CMOS Oscillator Divider Circuit

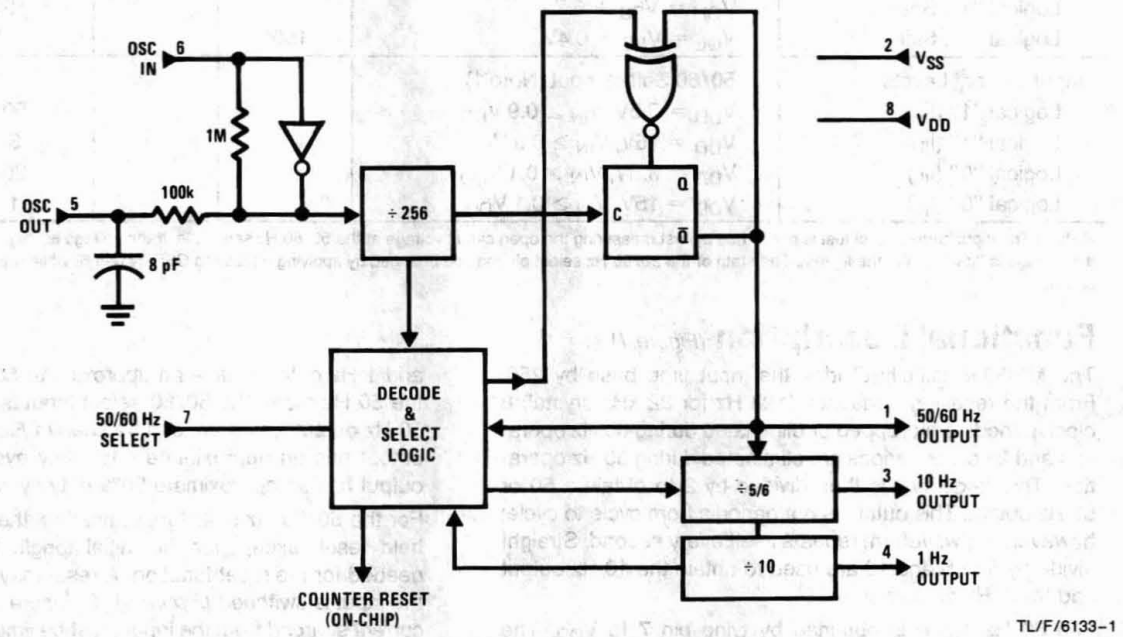
General Description

The MM5368 is a CMOS integrated circuit generating 50 or 60 Hz, 10 Hz, and 1 Hz outputs from a 32 kHz crystal (32,768 Hz). For the 60 Hz selected output the input time base is divided by 546.133, for the 50 Hz mode it is divided by 655.36. The 50/60 Hz output is then divided by 5 or 6 to obtain a 10 Hz output which is further divided to obtain a 1 Hz output. The 50/60 Hz select input can be floated for a counter reset.

Features

- 50/60 Hz output
- 1 Hz output
- 10 Hz output
- Low power dissipation
- Fully static operation
- Counter reset
- 3.5V–15V supply range
- On-chip oscillator—tuning and load capacitors are the only required external components besides the crystal. (For operation below 5V it may be necessary to use an ~ 1 MΩ pullup on the oscillator output to insure start-up.)

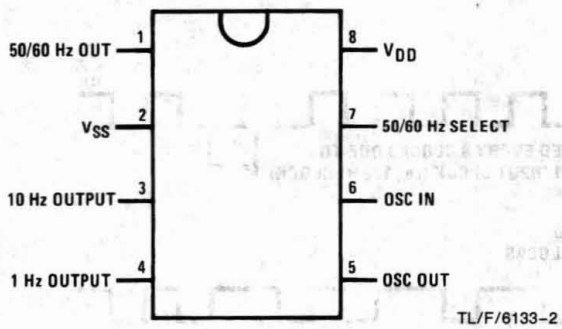
Block and Connection Diagrams



TL/F/6133–1

FIGURE 1

Dual-In-Line Package



TL/F/6133–2

Top View

FIGURE 2

Order Number MM5368N
See NS Package Number N08E

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Voltage at Any Pin	$-0.3V$ to $V_{DD} + 0.3V$
Operating Temperature	0°C to +70°C
Storage Temperature	−65°C to +150°C
Maximum V_{DD} Voltage	16V
Operating V_{DD} Range	$3.5V \le V_{DD} \le 15V$
Lead Temperature (Soldering, 10 sec.)	300°C

Electrical Characteristics T_A within operating range, $V_{SS} = 0V$

Parameter	Conditions	Min	Typ	Max	Units
Quiescent Current Drain	$V_{DD} = 15V$; 50/60 Select Floating			10	μA
Operating Current Drain	$f_{IN} = 32$ kHz, $V_{DD} = 3.5V$			60	μA
	$f_{IN} = 32$ kHz, $V_{DD} = 15V$			1500	μA
Maximum Input Frequency	$V_{DD} = 3.5V$			64	kHz
	$V_{DD} = 15V$			500	kHz
Output Current Levels	$V_{DD} = 5V$				
Logical "1", Source	$V_{OH} = V_{SS} + 2.7V$			−400	μA
Logical "0", Sink	$V_{OL} = V_{SS} + 0.4V$	400			μA
	$V_{DD} = 9V$				
Logical "1", Source	$V_{OH} = V_{SS} + 6.7V$			−1500	μA
Logical "0", Sink	$V_{OL} = V_{SS} + 0.4V$	1500			μA
Input Current Levels	50/60 Select Input (Note 1)				
Logical "1" (I_{IH})	$V_{DD} = 3.5V$, $V_{IN} \ge 0.9\ V_{DD}$			50	μA
Logical "1" (I_{IH})	$V_{DD} = 15V$, $V_{IN} \ge 0.9\ V_{DD}$			3	mA
Logical "0" (I_{IL})	$V_{DD} = 3.5V$, $V_{IN} \ge 0.1\ V_{DD}$			20	μA
Logical "0" (I_{IL})	$V_{DD} = 15V$, $V_{IN} \ge 0.1\ V_{DD}$			1	mA

Note 1: The input current level test is performed by first measuring the open circuit voltage at the 50/60 Hz select pin. If the voltage is "high", make the I_{IH} test. If the voltage is "low", make the I_{IL} test. The state of the 50/60 Hz select pin may be changed by applying a pulse to OSC IN (pin 6) while the 50/60 Hz pin is open circuit.

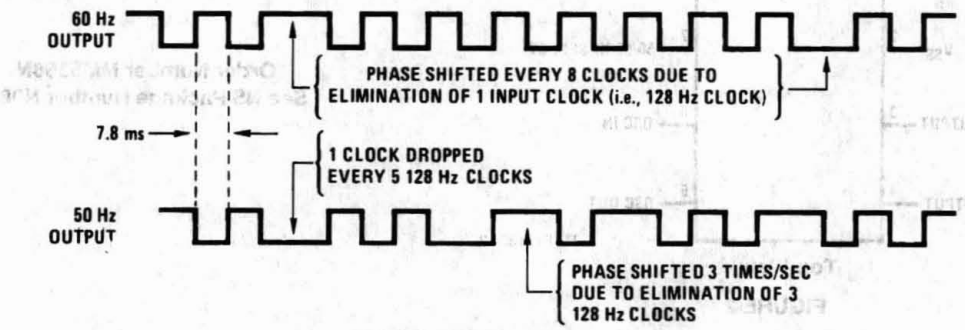
Functional Description *(Figure 1)*

The MM5368 initially divides the input time base by 256. From the resulting frequency (128 Hz for 32 kHz crystal) 8 clock periods are dropped or eliminated during 60 Hz operation and 28 clock periods are eliminated during 50 Hz operation. This frequency is then divided by 2 to obtain a 50 or 60 Hz output. This output is not periodic from cycle to cycle; however, the waveform repeats itself every second. Straight divide by 5 or 6 and 10 are used to obtain the 10 Hz output and the 1 Hz outputs.

The 60 Hz mode is obtained by tying pin 7 to V_{DD}. The 60 Hz output waveform can be seen in *Figure 3*. The 10 Hz and 1 Hz outputs have an approximate 50% duty cycle. In the 50 Hz mode the 50/60 select input is tied to V_{SS}. The 50 Hz output waveform can be seen in *Figure 3*. The 10 Hz output has an approximate 40% duty cycle and the 1 Hz output has an approximate 50% duty cycle.

For the 50/60 Hz select input floating, the counter chain is held reset, except for the initial toggle flip-flop which is needed for the reset function. A reset may also occur when the input is switched *(Figure 4)*. To insure the floating state, current sourced from the input must be limited to 1.0 μA and current sunk by the input must be limited to 1.0 μA for $V_{DD} = 3.5V$.

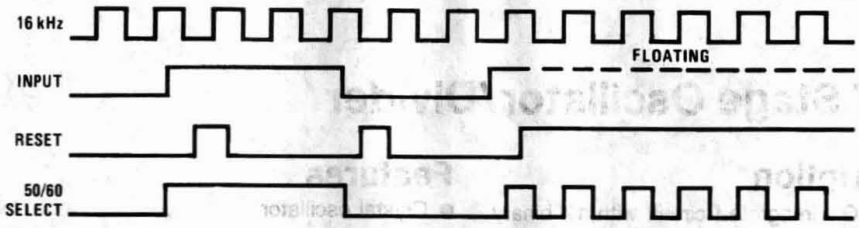
Timing Diagrams


60 Hz OUTPUT
PHASE SHIFTED EVERY 8 CLOCKS DUE TO ELIMINATION OF 1 INPUT CLOCK (i.e., 128 Hz CLOCK)
7.8 ms
1 CLOCK DROPPED EVERY 5 128 Hz CLOCKS
50 Hz OUTPUT
PHASE SHIFTED 3 TIMES/SEC DUE TO ELIMINATION OF 3 128 Hz CLOCKS

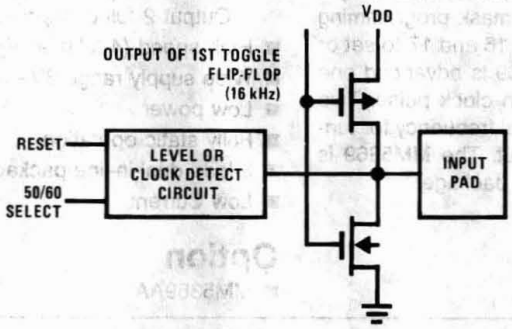
TL/F/6133–3

FIGURE 3. 50/60 Hz Output

Timing Diagrams (Continued)



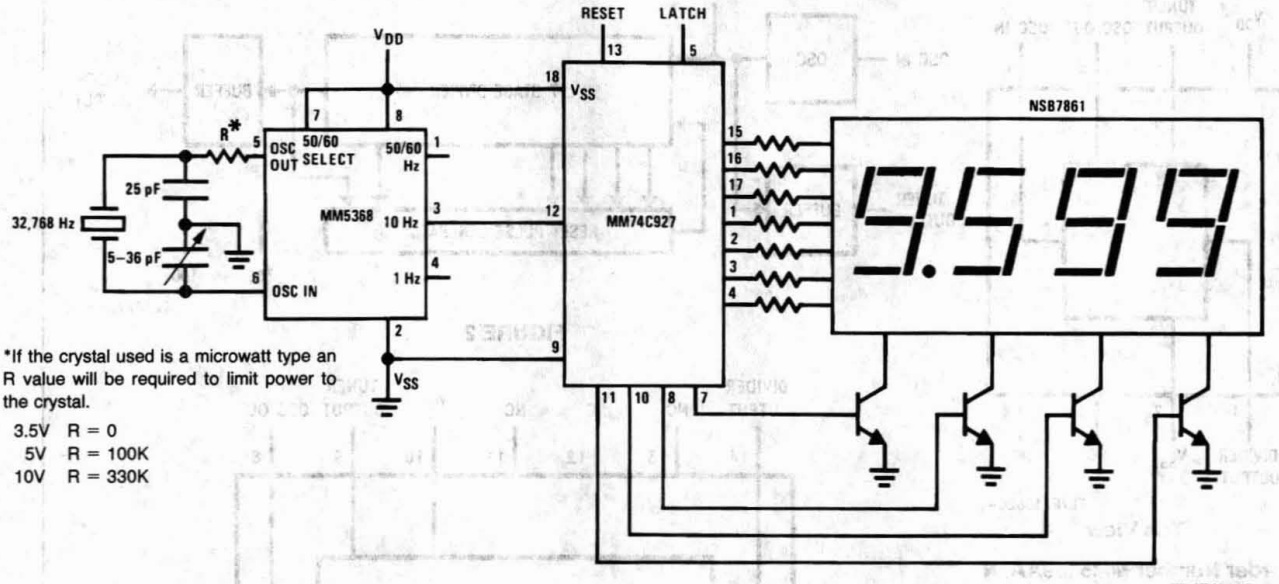
TL/F/6133–4



TL/F/6133–5

FIGURE 4. 50/60 Select and Reset

Typical Applications



*If the crystal used is a microwatt type an R value will be required to limit power to the crystal.

3.5V R = 0
5V R = 100K
10V R = 330K

TL/F/6133–6

FIGURE 5. 10 Minute (9:59.9) Timer

National Semiconductor

MM5369 17 Stage Oscillator/Divider

General Description

The MM5369 is a CMOS integrated circuit with 17 binary divider stages that can be used to generate a precise reference from commonly available high frequency quartz crystals. An internal pulse is generated by mask programming the combinations of stages 1 through 4, 16 and 17 to set or reset the individual stages. The MM5369 is advanced one count on the positive transition of each clock pulse. Two buffered outputs are available: the cyrstal frequency for tuning purposes and the 17th stage output. The MM5369 is available in an 8-lead dual-in-line epoxy package.

Features

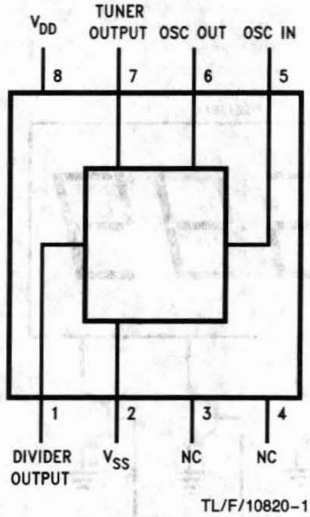
- Crystal oscillator
- Two buffered outputs
  - Output 1 crystal frequency
  - Output 2 full division
- High speed (4 MHz at V_{DD} = 10V)
- Wide supply range 3V–15V
- Low power
- Fully static operation
- 8-lead dual-in-line package
- Low Current

Option

- MM5369AA — 3.58 MHz to 60 Hz

Connection and Block Diagrams

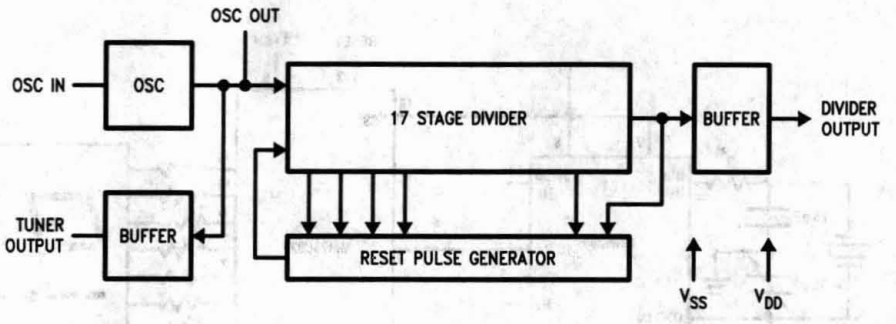
Dual-In-Line Package



TL/F/10820–1

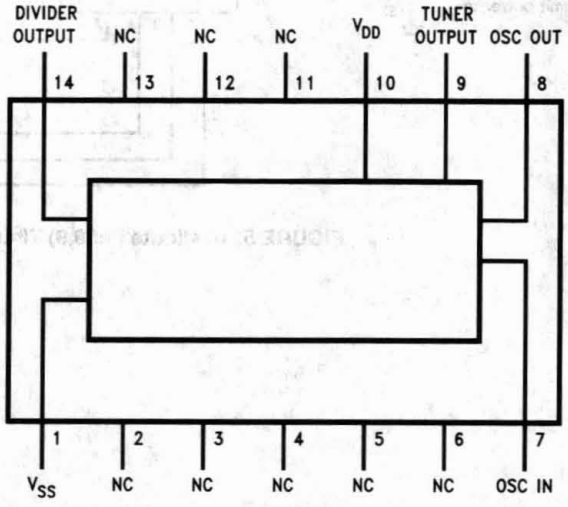
Top View

Order Number MM5369AA/N
See NS Package Number N08E



TL/F/10820–2

FIGURE 2



TL/F/10820–8

Order Number MM5369AA/M
See NS Package Number M14A

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Voltage at Any Pin	$-0.3V$ to $V_{DD} + 0.3V$
Operating Temperature	0°C to +70°C
Storage Temperature	−65°C to +150°C
Package Dissipation	500 mW
Maximum V_{CC} Voltage	16V
Operating V_{CC} Range	3V to 15V
Lead Temperature (Soldering, 10 seconds)	300°C

Electrical Characteristics

T_A within operating temperature range, V_{SS} = GND, $3V \le V_{DD} \le 15V$ unless otherwise specified.

Parameter	Conditions	Min	Typ	Max	Units
Quiescent Current Drain	V_{DD} = 15V			10	μA
Operating Current Drain	V_{DD} = 10V, f_{IN} = 4.19 MHz		1.2	2.5	mA
Frequency of Oscillation	V_{DD} = 10V V_{DD} = 6V	DC DC		4.5 2	MHz MHz
Output Current Levels	V_{DD} = 10V V_O = 5V				
Logical "1" Source		500			μA
Logical "0" Sink		500			μA
Output Voltage Levels	V_{DD} = 10V I_O = 10 μA				
Logical "1"		9.0			V
Logical "0"				1.0	V

Note: For 3.58 MHz operation, V_{DD} must be ≥ 10V.

Functional Description

A connection diagram for the MM5369 is shown in *Figure 1* and a block diagram is shown in *Figure 2.*

TIME BASE

A precision time base is provided by the interconnection of a 3,579,545 Hz quartz crystal and the RC network shown in *Figure 3* together with the CMOS inverter/amplifier provided between the OSC IN and the OSC OUT terminals. Resistor R1 is necessary to bias the inverter for class A amplifier operation. Capacitors C1 and C2 in series provide the parallel load capacitance required for precise tuning of the quartz crystal.

The network shown provides > 100 ppm tuning range when used with standard crystals trimmed for C_L = 12 pF. Tuning to better than ±2 ppm is easily obtainable.

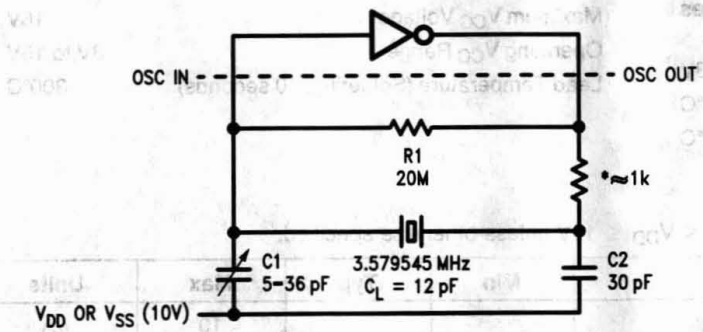
DIVIDER

A pulse is genertaed when divider stages 1 through 4, 16 and 17 are in the correct state. By mask options, this pulse is used to set or reset individual stages of the counter. *Figure 4* shows the relationship between the duty cycle and the programmed modulus.

OUTPUTS

The Tuner Output is a buffered output at the crystal oscillator frequency. This output is provided so that the crystal frequency can be obtained without disturbing the crystal oscillator. The Divide Output is the input frequency divided by the mask programmed number. Both outputs are push-pull outputs.

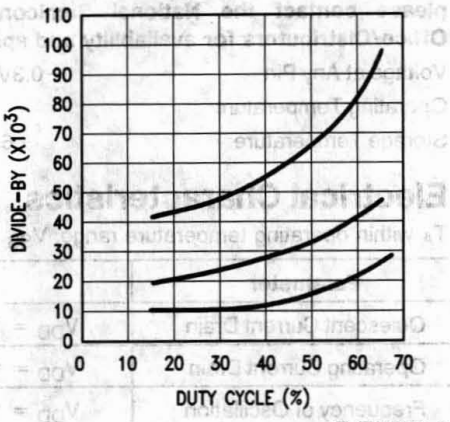
Functional Description (Continued)



TL/F/10820–3

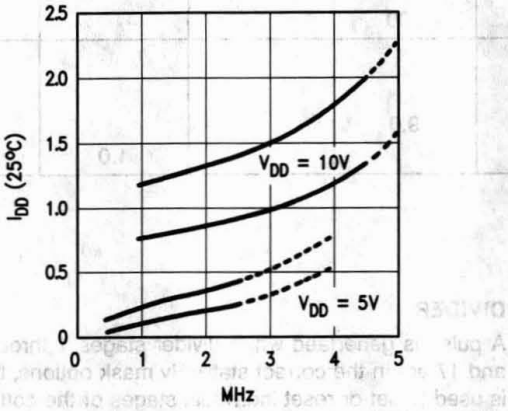
*To be selected based on xtal used

FIGURE 3. Crystal Oscillator Network



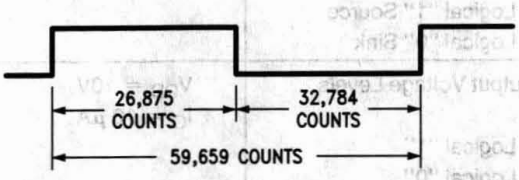
TL/F/10820–4

FIGURE 4. Plot of Divide-By vs Duty Cycle



TL/F/10820–5

FIGURE 5. Typical Current Drain vs Oscillator Frequency



TL/F/10820–6

FIGURE 6. Output Waveform for the MM5369AA

National Semiconductor

LM1851 Ground Fault Interrupter

General Description

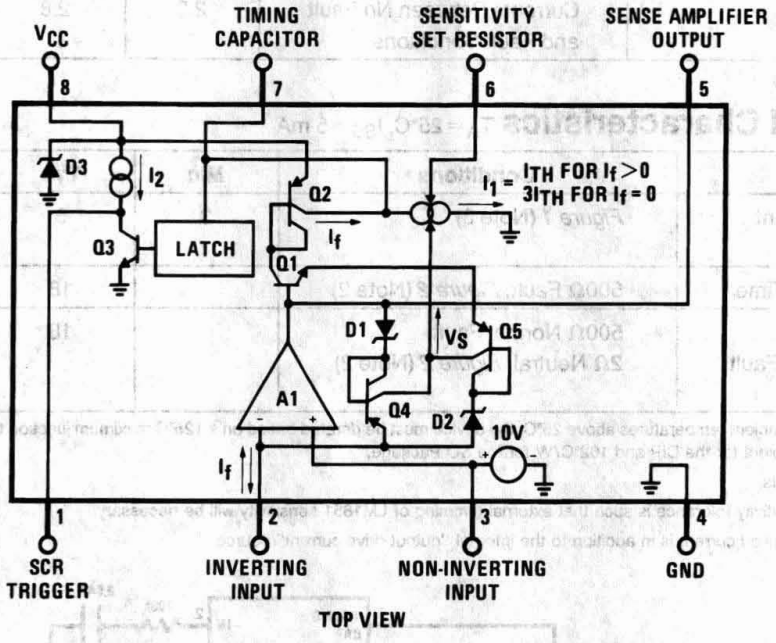
The LM1851 is designed to provide ground fault protection for AC power outlets in consumer and industrial environments. Ground fault currents greater than a presettable threshold value will trigger an external SCR-driven circuit breaker to interrupt the AC line and remove the fault condition. In addition to detection of conventional hot wire to ground faults, the neutral fault condition is also detected.

Full advantage of the U.S. UL943 timing specification is taken to insure maximum immunity to false triggering due to line noise. Special features include circuitry that rapidly resets the timing capacitor in the event that noise pulses introduce unwanted charging currents and a memory circuit that allows firing of even a sluggish breaker on either half-cycle of the line voltage when external full-wave rectification is used.

Features

- Internal power supply shunt regulator
- Externally programmable fault current threshold
- Externally programmable fault current integration time
- Direct interface to SCR
- Operates under line reversal; both load vs line and hot vs neutral
- Detects neutral line faults

Block and Connection Diagram



TOP VIEW

TL/H/5177–1

Order Number LM1851M or LM1851N
See NS Package Number M08A or N08E

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Current	19 mA
Power Dissipation (Note 1)	1250 mW
Operating Temperature Range	−40°C to +70°C
Storage Temperature Range	−55°C to +150°C

Soldering Information

Dual-In-Line Package (10 sec.)	260°C
Small Outline Package	
Vapor Phase (60 sec.)	215°C
Infrared (15 sec.)	220°C

See AN-450 "Surface Mounting and Their Effects on Product Reliability" for other methods of soldering surface mount devices.

DC Electrical Characteristics $T_A = 25°C$, $I_{SS} = 5$ mA

Parameter	Conditions	Min	Typ	Max	Units
Power Supply Shunt Regulator Voltage	Pin 8, Average Value	22	26	30	V
Latch Trigger Voltage	Pin 7	15	17.5	20	V
Sensitivity Set Voltage	Pin 8 to Pin 6	6	7	8.2	V
Output Drive Current	Pin 1, With Fault	0.5	1	2.4	mA
Output Saturation Voltage	Pin 1, Without Fault		100	240	mV
Output Saturation Resistance	Pin 1, Without Fault		100		Ω
Output External Current Sinking Capability	Pin 1, Without Fault, $V_{pin\ 1}$ Held to 0.3V (Note 4)	2.0	5		mA
Noise Integration Sink Current Ratio	Pin 7, Ratio of Discharge Currents Between No Fault and Fault Conditions	2.0	2.8	3.6	μA/μA

AC Electrical Characteristics $T_A = 25°C$, $I_{SS} = 5$ mA

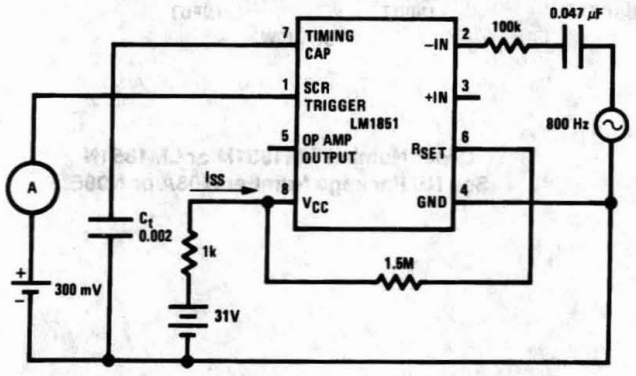
Parameter	Conditions	Min	Typ	Max	Units
Normal Fault Current Sensitivity	*Figure 1* (Note 3)	3	5	7	mA
Normal Fault Trip Time	500Ω Fault, *Figure 2* (Note 2)		18		ms
Normal Fault with Grounded Neutral Fault Trip Time	500Ω Normal Fault, 2Ω Neutral, *Figure 2* (Note 2)		18		ms

Note 1: For operation in ambient temperatures above 25°C, the device must be derated based on a 125°C maximum junction temperature and a thermal resistance of 80°C/W junction to ambient for the DIP and 162°C/W for the SO Package.

Note 2: Average of 10 trials.

Note 3: Required UL sensitivity tolerance is such that external trimming of LM1851 sensitivity will be necessary.

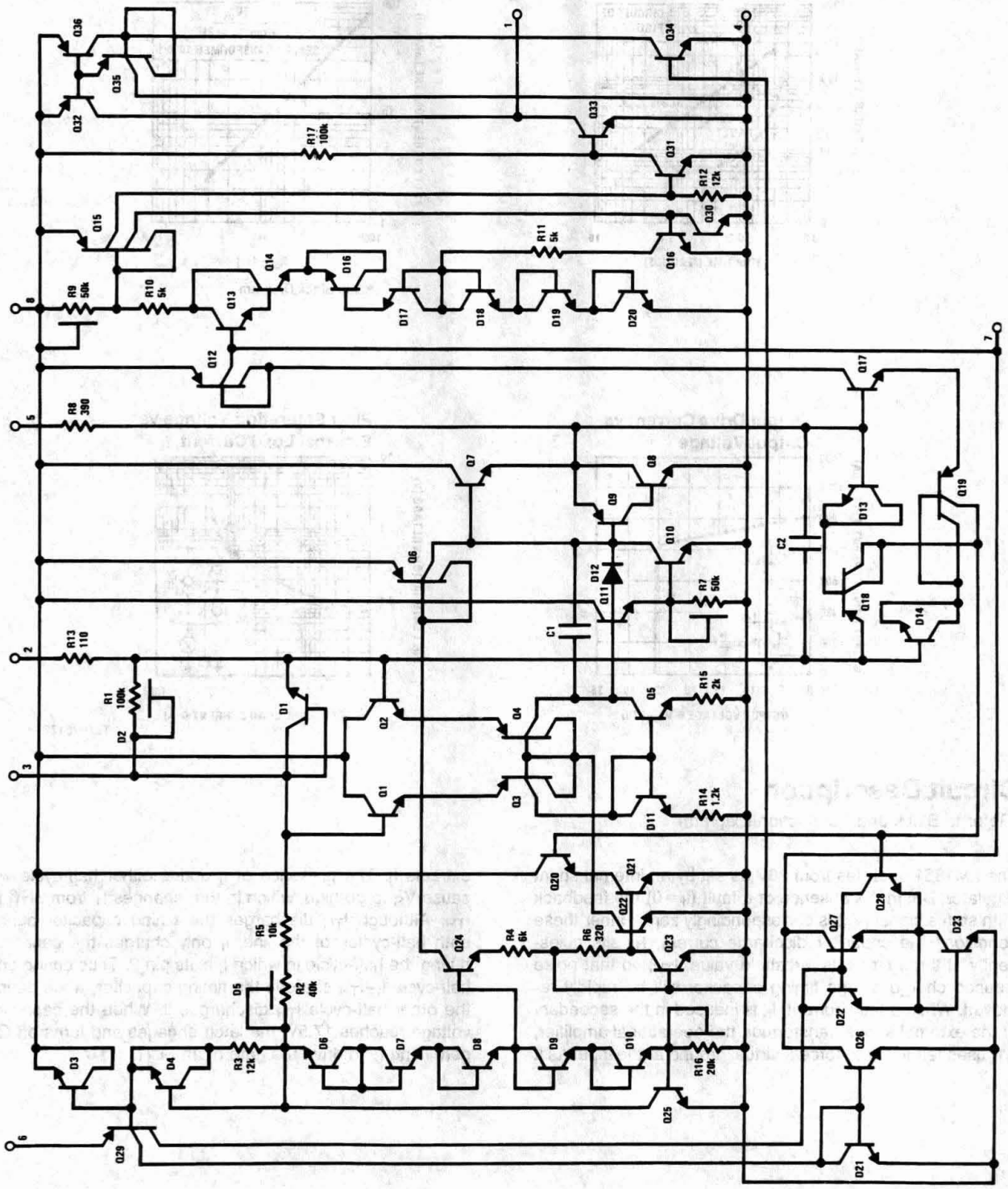
Note 4: This externally applied current is in addition to the internal "output drive current" source.



TL/H/5177–2

FIGURE 1. Normal Fault Sensitivity Test Circuit

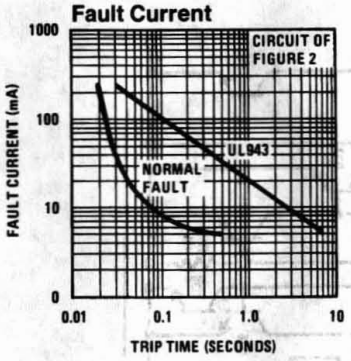
Internal Schematic Diagram



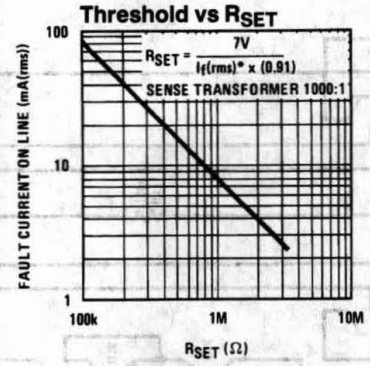
TL/H/5177–3

Typical Performance Characteristics

Average Trip Time vs Fault Current

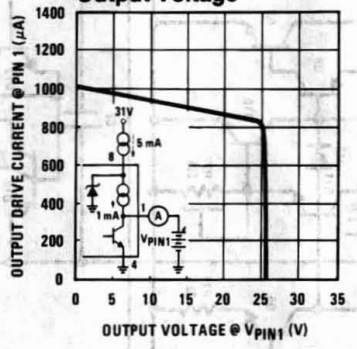


Normal Fault Current Threshold vs R_{SET}

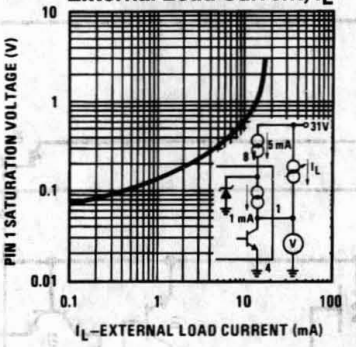


* See Block Diagram

Output Drive Current vs Output Voltage



Pin 1 Saturation Voltage vs External Load Current, I_L



TL/H/5177–4

Circuit Description

(Refer to Block and Connection Diagram)

The LM1851 operates from 26V as set by an internal shunt regulator, D3. In the absence of a fault ($I_f = 0$) the feedback path status signal (V_S) is correspondingly zero. Under these conditions the capacitor discharge current, I_1, sits quiescently at three times its threshold value, I_{TH}, so that noise induced charge on the timing capacitor will be rapidly removed. When a fault current, I_f, is induced in the secondary of the external sense transformer, the operational amplifier, A1, uses feedback to force a virtual ground at the input as it extracts I_f. The presence of I_f during either half-cycle will cause V_S to go high, which in turn changes I_1 from $3I_{TH}$ to I_{TH}. Although I_{TH} discharges the timing capacitor during both half-cycles of the line, I_f only charges the capacitor during the half-cycle in which I_f exits pin 2. Thus during one half-cycle $I_f - I_{TH}$ charges the timing capacitor, while during the other half-cycle I_{TH} discharges it. When the capacitor voltage reaches 17.5V, the latch engages and turns off Q3 permitting I_2 to drive the gate of an SCR.

Application Circuits

A typical ground fault interrupter circuit is shown in *Figure 2*. It is designed to operate on 120 V_{AC} line voltage with 5 mA normal fault sensitivity.

A full-wave rectifier bridge and a 15k/2W resistor are used to supply the DC power required by the IC. A 1 μF capacitor at pin 8 used to filter the ripple of the supply voltage and is also connected across the SCR to allow firing of the SCR on either half-cycle. When a fault causes the SCR to trigger, the circuit breaker is energized and line voltage is removed from the load. At this time no fault current flows and the IC discharge current increases from I_{TH} to $3I_{TH}$ (see Circuit Description and Block Diagram). This quickly resets both the timing capacitor and the output latch. At this time the circuit breaker can be reset and the line voltage again supplied to the load, assuming the fault has been removed. A 1000:1 sense transformer is used to detect the normal fault. The fault current, which is basically the difference current between the hot and neutral lines, is stepped down by 1000 and fed into the input pins of the operational amplifier through a 10 μF capacitor. The 0.0033 μF capacitor between pin 2 and pin 3 and the 200 pF between pins 3 and 4 are added to obtain better noise immunity. The normal fault sensitivity is determined by the timing capacitor discharging current, I_{TH}. I_{TH} can be calculated by:

$$I_{TH}=\frac{7V}{R_{SET}}\div 2 \qquad (1)$$

At the decision point, the average fault current just equals the threshold current, I_{TH}.

$$I_{TH}=\frac{I_{f(rms)}}{2}\times 0.91 \qquad (2)$$

where $I_{f(rms)}$ is the rms input fault current to the operational amp and the factor of 2 is due to the fact that I_f charges the timing capacitor only during one half-cycle, while I_{TH} discharges the capacitor continuously. The factor 0.91 converts the rms value to an average value. Combining equations (1) and (2) we have

$$R_{SET}=\frac{7V}{I_{f(rms)}\times 0.91} \qquad (3)$$

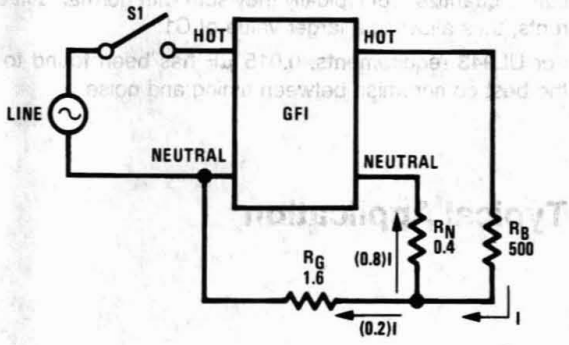
For example, to obtain 5 mA(rms) sensitivity for the circuit in *Figure 2* we have:

$$R_{SET}=\frac{7V}{\frac{5\text{ mA}\times 0.91}{1000}}=1.5\text{M }\Omega \qquad (4)$$

The correct value for R_{SET} can also be determined from the characteristic curve that plots equation (3). Note that this is an approximate calculation; the exact value of R_{SET} depends on the specific sense transformer used and LM1851 tolerances. Inasmuch as UL943 specifies a sensitivity "window" of 4 mA–6 mA, provision should be made to adjust R_{SET} on a per-product basis.

Independent of setting sensitivity, the desired integration time can be obtained through proper selection of the timing capacitor, C_t. Due to the large number of variables involved, proper selection of C_t is best done empirically. The following design example, then should only be used as a guideline.

Assume the goal is to meet UL943 timing requirements. Also assume that worst case timing occurs during GF1 start-up (S1 closure) with both a heavy normal fault and a 2Ω grounded neutral fault present. This situation is shown diagramatically below.



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UL943 specifies ≤25 ms average trip time under these conditions. Calculation of C_t based upon charging currents due to normal fault only is as follows:

≤25 ms Specification

−3 ms GFI turn-on time (15k and 1 μF)

−8 ms Potential loss of one half-cycle due to fault current sense of half-cycles only

−4 ms Time required to open a sluggish circuit breaker

≤10 ms Maximum integration time that could be allowed

8 ms Value of integration time that accommodates component tolerances and other variables

$$C_t=\frac{I\times T}{V} \qquad (5)$$

where T = integration time

V = threshold voltage

I = average fault current into C_t

$$I=\underbrace{\left(\frac{120\ V_{AC(rms)}}{R_B}\right)}_{\substack{\text{heavy fault}\\ \text{current generated}\\ \text{(swamps } I_{TH})}}\times\underbrace{\left(\frac{R_N}{R_G+R_N}\right)}_{\substack{\text{portion of}\\ \text{fault current}\\ \text{shunted}\\ \text{around GFI}}}$$

$$\times\underbrace{\left(\frac{1\text{ turn}}{1000\text{ turns}}\right)}_{\substack{\text{current}\\ \text{division of}\\ \text{input sense}\\ \text{transformer}}}\times\underbrace{\left(\frac{1}{2}\right)}_{\substack{C_t\text{ charging}\\ \text{on half-}\\ \text{cycles only}}}\times\underbrace{(0.91)}_{\substack{\text{rms to}\\ \text{average}\\ \text{conversion}}} \qquad (6)$$

therefore:

$$C_t=\frac{\left[\left(\frac{120}{500}\right)\times\left(\frac{0.4}{1.6+0.4}\right)\times\left(\frac{1}{1000}\right)\times\left(\frac{1}{2}\right)\times(0.91)\right]\times 0.0008}{17.5} \qquad (7)$$

$C_t=$ 0.01 μF

Application Circuits (Continued)

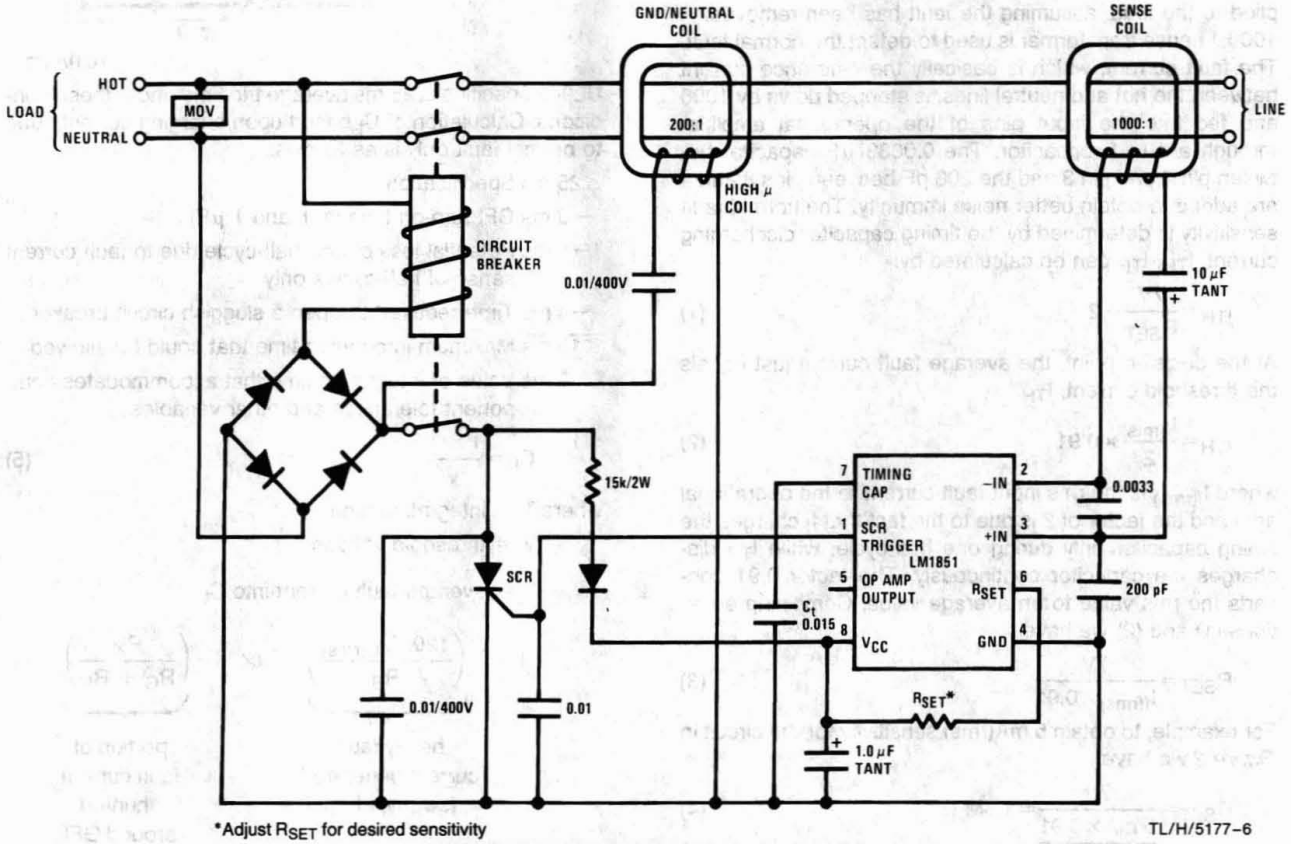
in practice, the actual value of C1 will have to be modified to include the effects of the neutral loop upon the net charging current. The effect of neutral loop induced currents is difficult to quantize, but typically they sum with normal fault currents, thus allowing a larger value of C1.

For UL943 requirements, 0.015 μF has been found to be the best compromise between timing and noise.

For those GFI standards not requiring grounded neutral detection, a still larger value capacitor can be used and better noise immunity obtained. The larger capacitor can be accommodated because R_N and R_G are not present, allowing the full fault current, I, to enter the GFI.

In *Figure 2*, grounded neutral detection is accomplished by feeding the neutral coil with 120 Hz energy continuously and allowing some of the energy to couple into the sense transformer during conditions of neutral fault.

Typical Application



*Adjust R_{SET} for desired sensitivity

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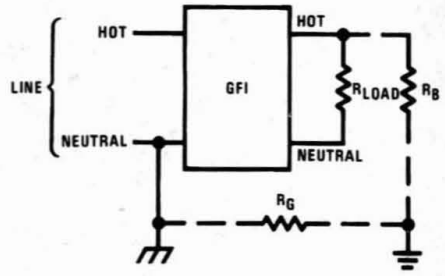
FIGURE 2. 120 Hz Neutral Transformer Approach

Definition of Terms

Normal Fault: An unintentional electrical path, R_B, between the load terminal of the hot line and the ground, as shown by the dashed lines.



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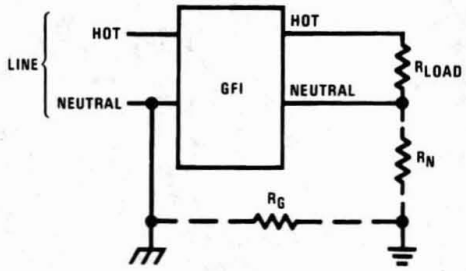
Grounded Neutral Fault: An unintentional electrical path between the load terminal of the neutral line and the ground, as shown by the dashed lines.



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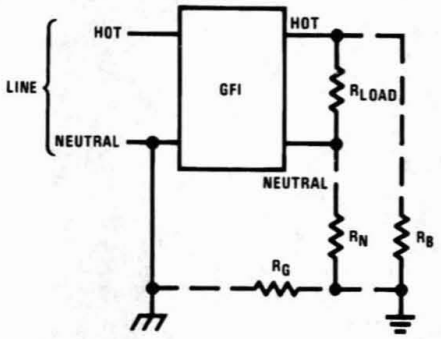
Normal Fault plus Grounded Neutral Fault: The combination of the normal fault and the grounded neutral fault, as shown by the dashed lines.



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Section 5
Surface Mount

Section 5 Contents

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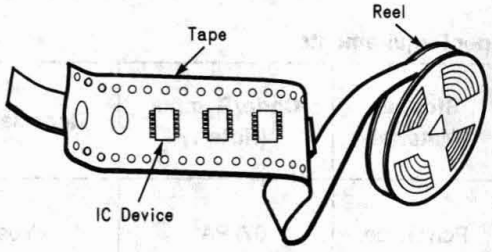
Packing Considerations (Methods, Materials and Recycling)

Transport Media

All NSC devices are prepared, inspected and packed to insure proper physical support and to protect during transport and shipment. All assembled devices are packed in one or more of the following container forms—immediate containers, intermediate containers and outer/shipping containers. An example of each container form is illustrated below.

IMMEDIATE CONTAINER



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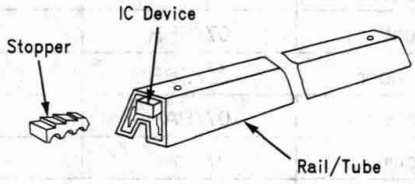

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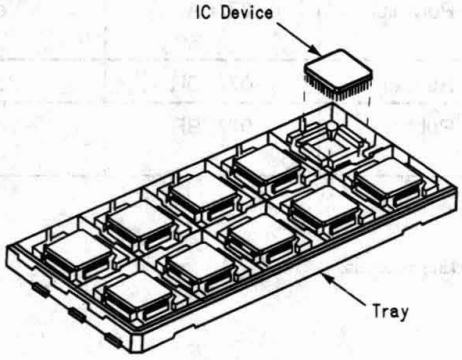

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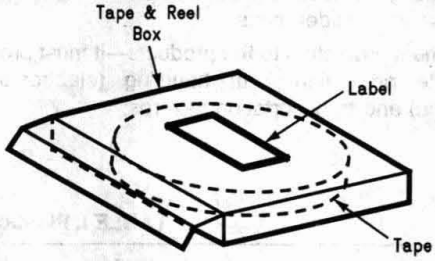
INTERMEDIATE CONTAINER



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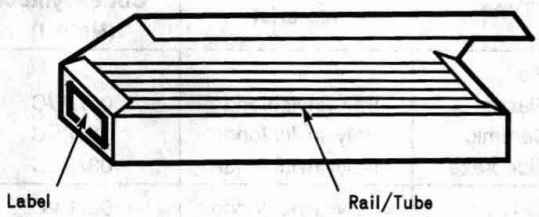

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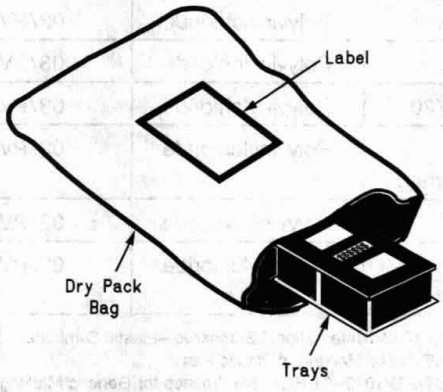

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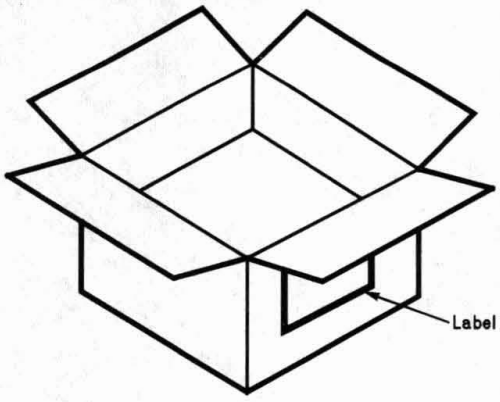
OUTER/SHIPPING CONTAINER



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Methods of immediate carrier packing include insertion of components into molded trays and rails/tubes, mounting of components onto tape and reel or placement in corrugated cartons. The immediate containers are then packed into intermediate containers (bags or boxes) which specify quantities of trays, rails/tubes or tape and reels. Outer/shipping containers are then filled or partially filled with intermediate containers to meet order quantity requirements and to further insure protection from transportation hazards. Additional dunnage filler material is required to fill voids within the intermediate and outer/shipping containers.

General Packing Requirements

NSC packing methods and materials are designed based on the following considerations:

— Optimum protection to the products—it must provide adequate protection from handling (electrostatic discharge) and transportation hazards;

— Ease of handling—it should be easy to assemble, load and unload products in and from it; and

— Impacts to the environment—it shall be reusable and recyclable.

Levels of Product Packing

IMMEDIATE CONTAINER

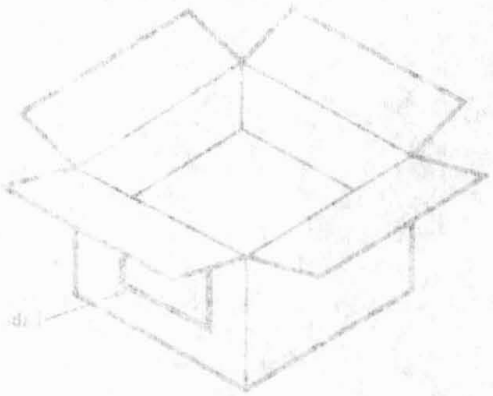
The first level of product packing is the immediate container. The immediate container type varies with the product or package being packed. In addition, the materials used in the immediate container depend on the fragility, size and profile of the product. The four types of immediate containers used by NSC are rails/tubes, trays, tape and reel, and corrugated and chipboard containers.

Rails/tubes are generally made of acrylic or polyvinyl chloride (PVC) plastics. The electrical characteristics of the material are altered by either intrinsically adding carbon fillers, and/or topically coating it with antistatic solution. Refer to Table I for rail/tube material and recyclabillty information.

TABLE I. Plastic Rail/Tube and Stopper Requirements

Package Type	Rail		Type	Stopper Material	Code/Symbol (Note 1)	Recyclability
	Material	Code/Symbol (Note 1)				
DIP's						
Plastic	Polyvinylchloride	03/PVC	Pin	Polyamide	07/PA	Yes
Ceramic	Polyvinylchloride	03/PVC	Pin	Polyamide	07/PA	Yes
Sidebraze	Polyvinylchloride	03/PVC	Pin	Polyamide	07/PA	Yes
PLCC	Polyvinylchloride	03/PVC	Plug	Rubber	07/SBR	Yes
TapePak	Polyvinylchloride	03/PVC	Plug	Rubber	07/SBR	Yes
Flatpack	Polyvinylchloride	03/PVC	Pin	Polymide	07/PA	Yes
Cerpack	Polyvinylchloride	03/PVC	Pin	Polymide	07/PA	Yes
TO-220/202	Polyvinylchloride	03/PVC	Pin	Polymide	07/PA	Yes
TO-5/8 (in Carrier)	Polyvinylchloride	03/PVC	Pin	Polymide	07/PA	Yes
SOP	Polyvinylchloride	03/PVC	Plug	Rubber	07/SBR	Yes
LCC 18L–44L	Polyvinylchloride	03/PVC	Plug	Rubber	07/SBR	Yes

Note 1: ISO 1043-1 International Standards—Plastic Symbols.
SAE J1344 Marking of Plastic Parts.
ASTM D 1972–91 Standard Practice for Generic Marking of Plastic Products.
DIN 6120, German Recycling Systems, RESY for paperbased and VGK for plastic packing materials.



Molded injection and vacuum formed trays can be either conductive or static dissipative. Molded injection trays are classified as either low-temperature or high-temperature depending on the material type. Vacuum formed trays are only used in ambient room temperature conditions. Refer to Table II for tray material and recyclability information.

TABLE II. Tray Requirements

Package Type	Class	Material	Tray		Binding Type
			Recyclability (Note 1)	Code/Symbol (Note 1)	
PQFP (All)	High Temperature	Polyethersulfone	Yes	07/PES	Wire Tie or Nylon Strap
	Low Temperature	Acrylonitrilebutadiene Styrene	Yes	07/ABS	Wire Tie or Nylon Strap
PGA, LDCC CERQUADs and LCC (48 leads–125 leads)	Low Temperature Only	ABS/PVC	Yes	07/ABS-PVC	Wire Tie
PPGA	Low Temperature Only	Polyarylsulfone	Yes	07/PAS	Wire Tie

Tape and reel is a multi-part immediate container system. The reel is made of either polystyrene (PS) material coated with antistatic solution or chipboard. The embossed or cavity tape is made of either PVC or PS material. The cover tape is made of polyester (PET) and polyethylene (PE) materials. Refer to Table III for tape and reel material and recyclability Information.

TABLE III. Tape and Reel Requirements

Package Type	Reel		Cover Type		Carrier Tape		Recyclability (Note 1)
	Material	Code/ Symbol (Note 1)	Material	Code/ Symbol (Note 1)	Material	Code/ Symbol (Note 1)	
TO-92	Chipboard	Resy	N/A		Paper Tape		Yes
SOP-23	Polystyrene Chipboard	06/PS Resy	Polystyrene	06/PS	PVC	03/PVC	Yes
SOP, SSOP and PLCC	Polystyrene Polyethylene	06/PS	Polyester	07/PET-PE	PVC	03/PVC	Yes

Note 1: 150 1043-1 International Standards—Plastic Symbols.
SAE J1344 Marking of Plastic Parts.
ASTM D 1972–91 Standard Practice for Generic Marking of Plastic Products.
DIN 6120, German Recycling Systems, RESY for paperbased and VGK for plastic packing materials.

Corrugated containers are generally constructed with fibreboard facings and a fluted corrugated medium in between the facings. Chipboard containers are comprised of just one fibreboard facing. Facings and corrugated medium are kraft (brown) fibreboard, and generally single wall construction. Refer to Table IV for material and recyclability information.

TABLE IV. Fibreboard Container Requirements

Package Type	Pack Method		Container Type		Recyclability
	Material	Code/ Symbol (Note 1)	Immediate (IMM) Intermediate (INT) Outer or Shipping (SHP)		
TO-92/18, TO-46/5, TO-39, 220, TO-202/126, TO-237	Corrugated (E070 BOX)	Resy	IMM		Yes
All Products	Corrguated	Resy	INT and SHIP		Yes
All Products	3-Ply Paper (Padpak)	Resy	Dunnage		Yes
All Products PLCC	Plastic Bubble Sheet	04/PE	Dunnage		Yes

Note 1: ISO 1043-1 International Standards—Plastic Symbols.
SAE J1344 Marking of Plastic Parts.
ASTM D1972–91 Standard Practice for Generic Marking of Plastic Products.
DIN 6120, German Recycling Systems, RESY for paperbased and VGK for plastic packing materials.

INTERMEDIATE CONTAINERS

The second level of product packing is the intermediate container. Three types on intermediate containers are used by NSC. They are plastic bags, moisture barrier bags and corrugated cartons/boxes.

Two types of plastic bags are used and usage of each type depends on the product or package being packed. Conductive bags are made of polyvinylchloride plastic material. The electrical characteristics of the bag are altered by adding carbon fillers which make the bag black (opaque) in color. Conductive bags are used on products or packages that are packed in static dissipative (SD) rails/tubes. Static shielding bags are made of two layers of SD polyethylene sheets with a metallized film separating the sheets. Refer to Table V for material and recyclability information.

Moisture barrier bags are used on rail/tube, tape and reel, and tray packs for moisture sensitive products. NSC uses National Metallizing's Stratoguard™ 4.6.

TABLE V. Conductive and Static Shielding Bag Requirements

Package Type	Container Type	Material Type	Mat'l and Symbol (Note 1)	Mat'l Recyclability
All Prod. in Rails	Conductive Bag	Polyethlene	04/PE	Yes
TO-92/81, TO-46/5, TO-39/220, TO-202/126, TO-3/237	Static Shielding Bag	Polyethlene Alum. Laminant	N/A	No

TABLE VI. Drypack Bag Requirements

Package Type	Container Type	Material Type	Mat'l and Symbol (Note 1)	Mat'l Recyclability
TapePak PLCC (52-84L) PQFP	Drypack Bag	Stratoguard™ 4.6	N/A	No

Note 1: ISO 1043-1 International Standards—Plastic Symbols.
SAE J1344 Marking of Plastic Parts.
ASTM D1972–91 Standard Practice for Generic Marking of Plastic Products.
DIN 6120, German Recycling Systems, RESY for paperbased and VGK for plastic packing materials

Corrugated cartons/boxes are generally constructed with fibreboard facings and a fluted corrugated medium in between the facings. Facings and corrugated medium are kraft (brown) fibreboards, and are generally of single wall construction. Carton style varies with the product that it will contain. For example, packing of a rail/tube will require the use of a carton with a roll end from lock (REFL) design. Other products generally use the regular slotted container (RSC) box. Refer to Table IV for material and recyclability information.

OUTER/SHIPPING CONTAINERS

The third level of product packing is the outer/shipping container. The outer/shipping containers use by NSC are similar to the corrugated containers used for immediate and intermediate packaging, but are heavier in facing thickness. The style generally used is the regular slotted container (RSC) box and can be single, double or triple wall, depending on the total weight of products being transported or shipped. Refer to Table IV for material and recyclability information.

OTHER PACKING MATERIALS

Additional dunnage and void filler materials are required to fill voids within the intermediate and outer/shipping containers. Two types of dunnage/flller material are Padpack and bubble pack. Padpak is a machine processed, 3-ply kraft paper sheet dunnage system. Refer to Table IV for material and recyclability information.

Bubble pack is made of polyethylene plastic sheets with air pockets trapped in between the plastic layers and can be either static dissipative or conductive. Refer to Table IV for material and recyclability information.

Immediate Container Pack Methods

The following table identifies the primary immediate container pack method for all hermetic and plastic packages offered by National Semiconductor. A secondary immediate container pack method is identified where applicable.

Immediate Packing Method for Ceramic Packages

Package Type (Code)	Package Marketing Drawing	Primary Immediate Container		Secondary Immediate Container	
		Method	Quantity	Method	Quantity
Ceramic Sidebrazed Dual-In-Line Package (SB)	D08C	Rail/Tube	35		
	D14D	Rail/Tube	25		
	D16C	Rail/Tube	20		
	D18A	Rail/Tube	20		
	D20A	Rail/Tube	18		
	D20B	Rail/Tube	18		
	D24C	Rail/Tube	15		
	D24H	Rail/Tube	15		
	D24K	Rail/Tube	15		
	D28D	Rail/Tube	13		
	D28G	Rail/Tube	13		
	D28H	Rail/Tube	13		
	D40C	Rail/Tube	9		
	D40J	Rail/Tube	9		
	D48A	Rail/Tube	7		
	D52A	Rail/Tube	7		
Ceramic Leadless Chip Carrier (LCC)	E20A	Rail/Tube	50		
	EA20B	Rail/Tube	50		
	E24B	Tray	25		
	E28A	Tray	28		
	EA028C	Tray	100		
	E32A	Rail/Tube	35		
	E32B	Rail/Tube	35		
	E32C	Rail/Tube	35		
	E40A	Rail/Tube	35		
	E44A	Rail/Tube	25		
	E48A	Tray	25		
	E68B	Tray	48		
	E68C	Tray	48		
	E84A	Tray	42		
	E84B	Tray	42		

Immediate Packing Method for Ceramic Packages (Continued)

Package Type (Code)	Package Marketing Drawing	Primary Immediate Container		Secondary Immediate Container	
		Method	Quantity	Method	Quantity
Ceramic Quad J-Bend (CQJB)	EL28A	Tray	96		
	EL44A	Tray	80		
	EL44B	Tray	80		
	EL44C	Tray	80		
	EL52A	Tray	50		
	EL68A	Tray	44		
	EL68B	Tray	44		
	EL68C	Tray	44		
	EL84A	Tray	42		
Ceramic Quad Flatpack (CQFP)	EL28B	Rail	15		
	EL64A	Box	36		
	EL100A	Tray	12		
	EL116A	Tray	12		
	EL132B	Tray	20		
	EL132C	Tray	20		
	EL132D	Tray	20		
	EL164A	Tray	12		
	EL172B	Tray	12		
	EL172C	Tray	12		
Ceramic Flatpack	F10B	Carrier/Rail	19	Carrier/Box	200
	F14C	Carrier/Rail	19	Carrier/Box	200
	F16B	Carrier/Rail	19	Carrier/Box	200

Immediate Packing Method for Ceramic Packages (Continued)

Package Type (Code)	Package Marketing Drawing	Primary Immediate Container		Secondary Immediate Container	
		Method	Quantity	Method	Quantity
Ceramic Dual-In-Line Package (Cerdip)	J08A	Rail/Tube	40		
	J14A	Rail/Tube	25		
	J16A	Rail/Tube	25		
	J18A	Rail/Tube	20		
	J20A	Rail/Tube	20		
	J22A	Rail/Tube	17		
	J24A	Rail/Tube	15		
	J24AQ	Rail/Tube	15		
	J24B-Q	Rail/Tube	15		
	J24CQ	Rail/Tube	15		
	J24E	Rail/Tube	16		
	J24F	Rail/Tube	15		
	J28A	Rail/Tube	12		
	J28AQ	Rail/Tube	12		
	J28B	Rail/Tube	12		
	J28BQ	Rail/Tube	12		
	J28CQ	Rail/Tube	13		
	J32B	Rail/Tube	11		
	J32AQ	Rail/Tube	11		
	J40A	Rail/Tube	9		
	J40AQ	Rail/Tube	9		
	J40BQ	Rail/Tube	9		
Ceramic Small Outline Package, Wide	MC16A	Rail/Tube	45		
	MC20A	Rail/Tube	36		
	MC20B	Rail/Tube	36		
	MC24A	Rail/Tube	30		
	MC28A	Rail/Tube	26		
	MC28B	Rail/Tube	26		

Immediate Packing Method for Ceramic Packages (Continued)

Package Type (Code)	Package Marketing Drawing	Primary Immediate Container		Secondary Immediate Container	
		Method	Quantity	Method	Quantity
Ceramic Pin Grid Array (CPGA)	U44A	Tray	80		
	U68B	Tray	42		
	U68C	Tray	42		
	U68D	Tray	42		
	U68E	Tray	42		
	U75A	Tray	35		
	U84A	Tray	42		
	U84B	Tray	42		
	U84C	Tray	42		
	U99A	Tray	25		
	U100A	Tray	30		
	U109A	Tray	25		
	U120A	Tray	30		
	U120C	Tray	30		
	U124A	Tray	30		
	U132A	Tray	30		
	U132B	Tray	30		
	U144A	Tray	20		
	U156A	Tray	20		
	U156B	Tray	20		
	U169A	Tray	20		
	U173A	Tray	20		
	U175A	Tray	20		
	U180A	Tray	20		
	U223A	Tray	20		
	U224A	Tray	20		
	U257A	Tray	12		
	U259A	Tray	12		
	U299A	Tray	12		
	U301A	Tray	12		
	U303A	Tray	12		
	U323A	Tray	12		

Immediate Packing Method for Ceramic Packages (Continued)

Package Type (Code)	Package Marketing Drawing	Primary Immediate Container		Secondary Immediate Container	
		Method	Quantity	Method	Quantity
Cerpack	W10A	Carrier/Rail	19	Carrier/Box	200
	W14B	Carrier/Rail	19	Carrier/Box	200
	W14C	Carrier/Rail	19	Carrier/Box	200
	W16A	Carrier/Rail	19	Carrier/Box	200
	W20A	Carrier/Rail	19	Carrier/Box	200
	W24C	Carrier/Rail	15	Carrier/Box	80
	W28A	Carrier/Rail	15	Carrier/Box	80
	WA28D	Carrier/Rail	15	Carrier/Box	80
Cerquad	W24B	Rail/Tube	15		
	W56B	Tray	20		
	W64A	Tray	20		
	W68A	Tray	12		
	W84A	Tray	12		
Cerquad, EIAJ	WA80A	Tray	84		
	WA80AQ	Tray	84		
	W120A	Tray	12		
	W144A	Tray	12		
	W144B	Tray	12		
	W160A	Tray	12		
	W208A	Tray	12		

Immediate Packing Method for Metal Cans

Package Type (Code)	Package Marketing Drawing	Primary Immediate Container		Secondary Immediate Container	
		Method	Quantity	Method	Quantity
TO-5	H06C	Tray	100	Carrier/Rail	18
	H08A	Tray	100	Carrier/Rail	18
	H08C	Tray	100	Carrier/Rail	18
	H10C	Tray	100	Cerrier/Rail	18
TO-18	H03C	Box	1800	Tray	100
TO-39	H03A	Tray	100	Carrier/Rail	18
	H03B	Tray	100	Carrier/Rail	18
	HA04E	Tray	100	Carrier/Rail	18
TO-46	H02A	Box	1800	Tray	100
	H03H	Box	1800	Tray	100
	H04A	Box	1800	Tray	100
	H04D	Box	1800	Tray	100
TO-52	H03J	Box	1800	Tray	100
TO-72	H04C	Box	1800	Tray	100

Immediate Packing Method for Plastic Packages

Package Type (Code)	Package Marketing Drawing	Primary Immediate Container		Secondary Immediate Container	
		Method	Quantity	Method	Quantity
Small Outline Transistor (SOT-23)	M03A	Tape and Reel	3000/ 10000	Bulk/Bag	500
	M03B	Tape and Reel	3000/ 10000	Bulk/Bag	500
Small Outline Package, JEDEC (SOP)	M08A	Rail/Tube	95	Tape and Reel	2500
	M14A	Rail/Tube	55	Tape and Reel	2500
	M14B	Rail/Tube	50	Tape and Reel	1000
	M16A	Rail/Tube	48	Tape and Reel	2500
	M16B	Rail/Tube	45	Tape and Reel	1000
	M20B	Rail/Tube	36	Tape and Reel	1000
	M24B	Rail/Tube	30	Tape and Reel	1000
	M28B	Rail/Tube	26	Tape and Reel	1000
Small Outline Package, EIAJ (SOP)	M14D	Rail/Tube	47	Tape and Reel	1000
	M16D	Rail/Tube	47	Tape and Reel	1000
	M20D	Rail/Tube	37	Tape and Reel	1000
Shrink Small Outline Package, JEDEC (SSOP)	MQA20	Rail/Tube	54	Tape and Reel	2500
	MQA24	Rail/Tube	54	Tape and Reel	2500
	MS48A	Rail/Tube	29	Tape and Reel	1000
	MS56A	Rail/Tube	25	Tape and Reel	1000
Shrink Small Outline Package, EIAJ (SSOP)	MSA20	Rail/Tube	65	Tape and Reel	1000
	MSA24	Rail/Tube	58	Tape and Reel	1000
	MS40A	Rail/Tube	34	Tape and Reel	1000
Very Small Outline Package (VSOP)	M40A	Rail/Tube	34	Tape and Reel	1000
Thin Small Outline Package, EIAJ (TSOP)	MBH32A	Tray	156		
Thin Shrink Small Outline Package, EIAJ (TSSOP)	MTA20	Tape and Reel	2500		

Immediate Packing Method for Plastic Packages (Continued)

Package Type (Code)	Package Marketing Drawing	Primary Immediate Container		Secondary Immediate Container	
		Method	Quantity	Method	Quantity
Molded Dual-In-Line Package (MDIP)	N08E	Rail/Tube	40		
	N14A	Rail/Tube	25		
	N16A	Rail/Tube	20		
	N16E	Rail/Tube	25		
	N16G	Rail/Tube	20		
	N18A	Rail/Tube	20		
	N20A	Rail/Tube	18		
	N22A	Rail/Tube	15		
	N22B	Rail/Tube	15		
	N24A	Rail/Tube	15		
	N24C	Rail/Tube	15		
	N24D	Rail/Tube	15		
	N24E	Rail/Tube	15		
	N28B	Rail/Tube	13		
	N40A	Rail/Tube	9		
	N48A	Rail/Tube	7		
TO-202	P03A	Rail/Tube	45	Box	300
	P03B	Rail/Tube	45	Box	300
	P03C	Rail/Tube	45	Box	300
	P03D	Rail/Tube	45	Box	300
	P03E	Rail/Tube	45	Box	300
	P03F	Rail/Tube	45	Box	300
	P03G	Rail/Tube	45	Box	300
	P03H	Rail/Tube	45	Box	300
	P03J	Rail/Tube	45	Box	300
	P04A	Rail/Tube	45	Box	300
	P11A	Rail/Tube	15		
TO-237	R03A	Box	1500	Tape and Reel	2000
	R03B	Box	1500	Tape and Reel	2000
	R03C	Box	1500	Tape and Reel	2000
	R03D	Box	1500	Tape and Reel	2000
TO-226	RC03A	Box	1500	Tape and Reel	2000
	RC03B	Box	1500	Tape and Reel	2000
	RC03C	Box	1500	Tape and Reel	2000
	RC03D	Box	1500	Tape and Reel	2000

Immediate Packing Method for Plastic Packages (Continued)

Package Type (Code)	Package Marketing Drawing	Primary Immediate Container		Secondary Immediate Container	
		Method	Quantity	Method	Quantity
TO-220	TA02A	Rail/Tube	45	Box	300
	T02D	Rail/Tube	45	Box	300
	TA03A	Rail/Tube	45	Box	300
	TA03B	Rail/Tube	45	Box	300
	TA03D	Rail/Tube	45	Box	300
	T03A	Rail/Tube	45	Box	300
	T03B	Rail/Tube	45	Box	300
	T03D	Rail/Tube	45	Box	300
	T03F	Rail/Tube	45	Box	300
	T05A	Rail/Tube	45	Box	300
	T05B	Rail/Tube	45	Box	300
	T05C	Rail/Tube	45	Box	300
	T05D	Rail/Tube	45	Box	300
	T05E	Rail/Tube	45	Box	300
	T05F	Rail/Tube	45	Box	300
	TA05A	Rail/Tube	45	Box	300
	TA05B	Rail/Tube	45	Box	300
	TA11A	Rail/Tube	20	Box	300
	TA11B	Rail/Tube	20	Box	300
	TA11C	Rail/Tube	20	Box	300
	TA11D	Rail/Tube	20	Box	300
	TA11E	Rail/Tube	20	Box	300
	TA12A	Rail/Tube	20	Box	300
	TA15A	Rail/Tube	20	Box	300
	TA23A	Rail/Tube	15	Box	300
TapePak®	TP40A	Coinstack Tube	100	Flat Rail	25
Plastic Pin Grid Array (PPGA)	UP124A	Tray	30		
	UP159A	Tray	20		
	UP175A	Tray	20		
Plastic Leaded Chip Carrier (PLCC)	V20A	Rail/Tube	40	Tape and Reel	1000
	V28A	Rail/Tube	35	Tape and Reel	750
	V32A	Rail/Tube	30		
	V44A	Rail/Tube	25	Tape and Reel	500
	V52A	Rail/Tube	22	Tape and Reel	500
	V68A	Rail/Tube	18	Tape and Reel	250
	V84A	Rail/Tube	15	Tape and Reel	250

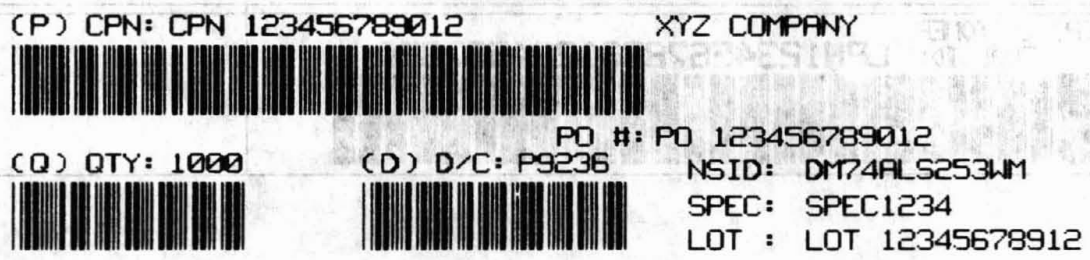
Immediate Packing Method for Plastic Packages (Continued)

Package Type (Code)	Package Marketing Drawing	Primary Immediate Container		Secondary Immediate Container	
		Method	Quantity	Method	Quantity
Plastic Quad Flatpack (PQFP)	VEF44A	Tray	96		
	VBG48A	Tray	60		
	VHG80A	Tray	60		
	VJE80A	Tray	84		
	VCC80A	Tray	50/66		
	VCE100A	Tray	84		
	VLJ100A	Tray	50		
	VJG100A	Tray	60		
	VNG144A	Tray	60		
	VUL160A	Tray	24		
	VQL160A	Tray	24		
	VUW208A	Tray	24		
	VF132A	Tray	36		
	VF196A	Tray	21		
TO-92	Z03A	Box	1800	Tape and Reel	2000
	Z03B	Box	1800	Tape and Reel	2000
	Z03C	Box	1800	Tape and Reel	2000
	Z03D	Box	1800	Tape and Reel	2000
	Z03E	Box	1800	Tape and Reel	2000
	Z03G	Box	1800	Tape and Reel	2000
	Z03H	Box	1800	Tape and Reel	2000
	Z03J	Box	1800	Tape and Reel	2000

Labeling

National Semiconductor offers 3 standard bar code labels; reel and intermediate container labels for Tape and Reel; intermediate container label other than for Tape and Reel; and outer/shipping container labels. The tape and reel, and intermediate container labels are National's own format while the outer/shipping container label is based on the EIA-556-A label standard.

NSC Standard Tape and Reel Label



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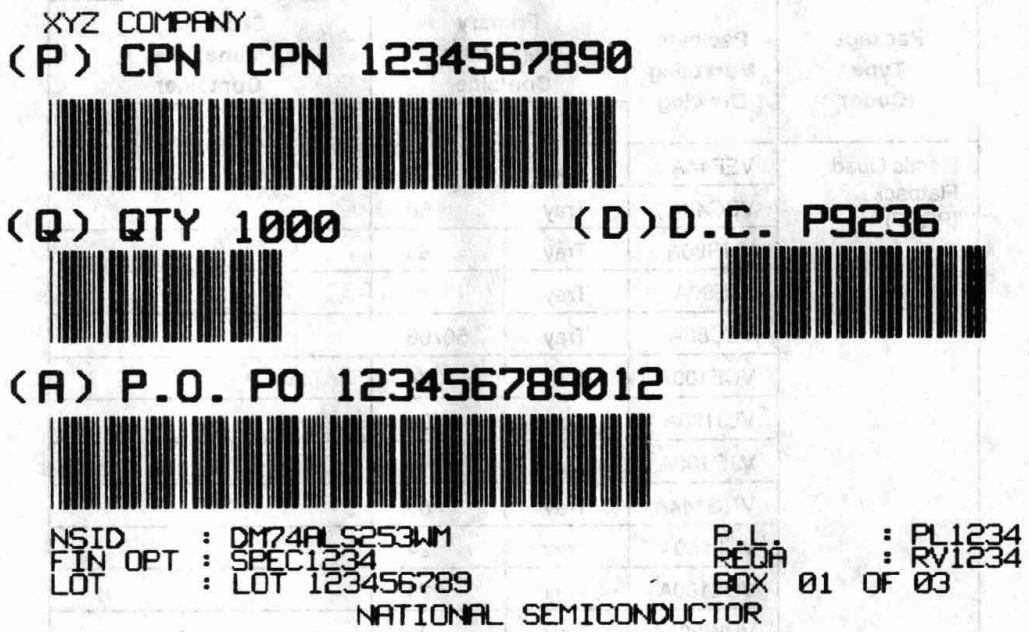
This label is placed on the reel (immediate container) as well as on the intermediate box.

NSC Standard Intermediate Container Label



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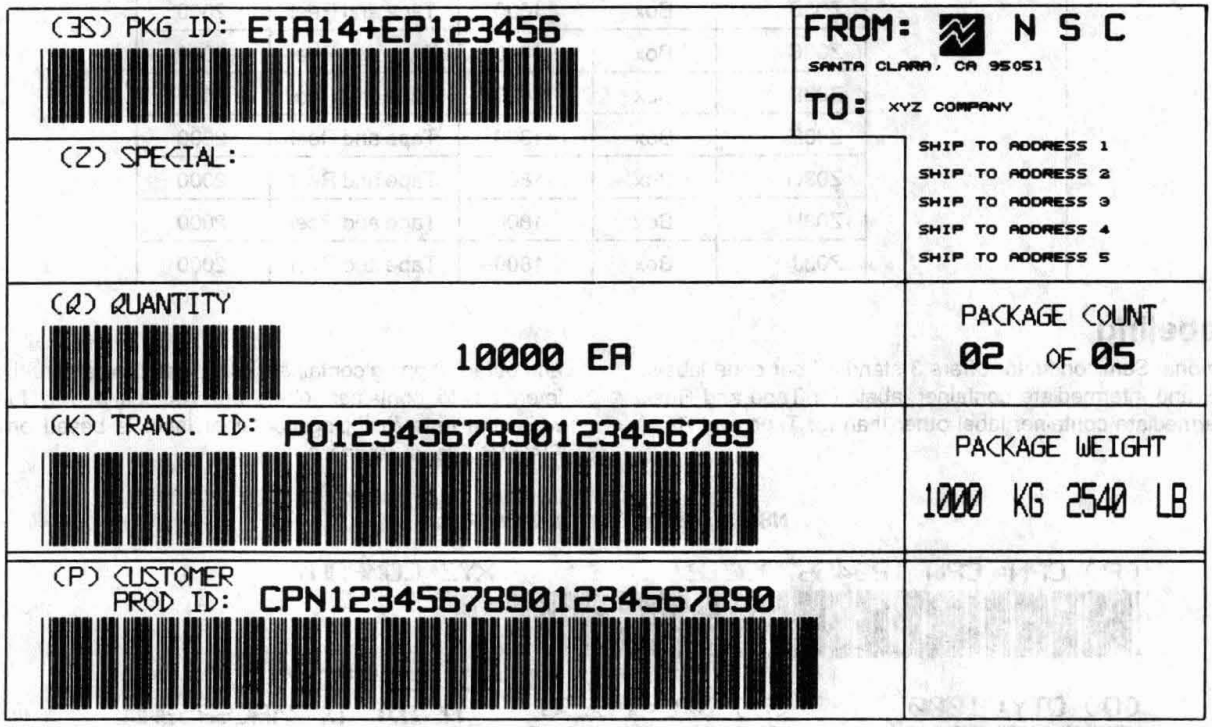
NSC Standard Outer/Shipping Container Label



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National Semiconductor

Board Mount of Surface Mount Components

Abstract

In facing the challenges of "Surface Mount Technology", many manufacturers of printed circuit boards have taken steps to convert some portions of their boards to this process. However, as the availability of all products as surface mount components is still limited, many have had to mix lead-inserted components with surface mount devices (SMD's). Furthermore, to take advantage of using both sides of the board, some surface mounted components are adhered to the bottom side of the board while the top side is reserved for the conventional lead-insert packages and fine pitch surface mount packages.

There are three surface mount processes in hi-volume use today:

1. **WAVE SOLDER;** the surface mounted components are adhered to the bottom side of the board while the top side is reserved for the lead-inserted packages. The surface mount components are subjected to severe thermal stress when they are immersed into the molten solder.
2. **INFRA-RED** mass reflow; the surface mount components are placed on the solder paste which has been applied to the board, the solder joints are formed when the board is passed thru the reflow media. The surface mount devices are subjected to a controlled thermal environment.
3. **VAPOR PHASE** mass reflow; the surface mount components are placed on the solder paste which has been applied to the board, tbe solder joints are formed when the board is passed thru the reflow media. The surface mount devices are subjected to a controlled thermal environment, more severe than Infra-red but much less than wavesolder.

A discussion of the effect of these processes on the reliability of plastic semiconductor packages follows.

Role of Wave Soldering in Application of SMDs

The generally acceptable methods of soldering SMDs are vapor phase reflow soldering and IR reflow soldering, both requiring application of solder paste on PW boards prior to placement of the components. However, sentiment still exists for retaining the use of the old wave soldering machine. The reasons being:

Most PC Board Assembly houses already possess wave soldering equipment. Switching to another technology such as vapor phase soldering requires substantial investment in equipment and people.

Due to the limited number of devices that are surface mount components, it is necessary to mix both lead inserted components and surface mount components on the same board.

Some components such as relays and switches are made of materials which would not be able to survive the temperature exposure in a vapor phase or IR furnace.

PW Board Assembly Procedures

There are two considerations in which through-hole ICs may be combined with surface mount components on the PW Board:

a) Whether to mount ICs on one or both sides of the board.

b) The sequence of soldering using Vapor Phase, IR or Wave Soldering singly or a combination of two or more methods.

The various processes that may be employed are:

A) WAVE SOLDER BEFORE VAPOR/IR REFLOW SOLDER

1. Components on the same side of PW Board. Lead insert standard DIPS onto PW Board Wave solder (conventional). Wash and lead trim. Dispense solder paste on SEM pads. Pick and place SMDs onto PW Board. Bake Vapor phase/IR reflow. Clean.
2. Components on opposite side of PW Board. Lead insert standard DIPs onto PW Board Wave Solder (conventional). Clean and lead trim. Invert PW Board. Dispense drop of adhesive on SMD sites (optional for smaller components). Pick and place SMDs onto board. Bake/Cure. Invert board to rest on raised fixture. Vapor/IR reflow soldering. Clean.

B) VAPOR/IR REFLOW SOLDER THEN WAVE SOLDER

1. Components on the same side of PW Board. Solder paste screened on SMD side of Printed Wire Board. Pick and place SMDs. Bake Vapor/IR reflow. Lead insert on same side as SMD's. Wave solder. Clean and trim underside of PCB.

C) VAPOR/IR REFLOW ONLY

1. Components on the same side of PW Board Trim and form standard DIPs in "gull wing" configuration. Solder paste screened on PW Board. Pick and place SMDs and DIPs. Bake Vapor/IR reflow. Clean.
2. Components on opposite sides of PW Board. Solder paste screened on SMD-side of Printed Wire Board. Adhesive dispensed at central location of each component. Pick and place SMDs. Bake. Solder paste screened on all pads on DIP-side or alternatively apply solder rings (performs) on leads. Lead insert DIPs. Vapor/IR reflow. Clean and lead trim.

PW Board Assembly Procedures

(Continued)

D) WAVE SOLDERING ONLY

1. Components on opposite sides of PW board. Adhesive dispense on SMD side of PW Board. Pick and place SMDs. Cure adhesive. Lead insert top side with DIPs. Wave solder with SMDs down and into solder bath. Clean and lead trim.

All of the above assembly procedures can be divided into three categories for IC. Reliability considerations:

1) Components are subjected to both a vapor phase/IR heat cycle then followed by a wave-solder heat cycle or vice versa.
2) Components are subjected to only a vapor phase/IR heat cycle.
3) Components are subjected to wave-soldering only and SMDs are subjected to heat by immersion into a solder pot.

Of these three categories, the last is the most severe regarding heat treatment to a semiconductor device. However, note that semiconductor molded packages generally possess a coating of solder on their leads as a final finish for solderability and protection of base leadframe material. Most semiconductor manufacturers solder-plate the component leads, while others perform hot solder dip. In the latter case the packages may be subjected to total immersion into a hot solder bath under controlled conditions (manual operation) or be partially immersed while in a "pallet" where automatic wave or DIP soldering processes are used. It is, therefore, possible to subject SMDs to solder heat under certain conditions and not cause catastrophic failures.

Thermal Characteristics of Molded Integrated Circuits

Since Plastic DIPs and SMDs are encapsulated with a thermoset epoxy, the thermal characteristics of the material generally correspond to a TMA (Thermo-Mechanical Analysis) graph. The critical parameters are (a) its Linear thermal expansion characteristics and (b) its glass transition temperature after the epoxy has been fully cured. A typical TMA graph is illustrated in *Figure 1.* Note that the epoxy changes to a higher thermal expansion once it is subjected to temperatures exceeding its glass transition temperature. Metals (as used on leadframes, for example) do not have this characteristic and generally will have a consistent Linear thermal expansion over the same temperature range.

In any good reliable plastic package, the choice of leadframe material should be such to match its thermal expansion properties to that of the encapsulating epoxy. In the event that there is a mismatch between the two, stresses can build up at the interface of the epoxy and metal. There now exists a tendency for the epoxy to separate from the metal leadframe in a manner similar to that observed on bimetallic thermal range.

In most cases when the packages are kept at temperatures below their glass transition, there is a small possibility of separation at the epoxy-metal interface. However, If the package is subjected to temperature above its glass-transition temperature, the epoxy will expand much faster than the metal and the probability of separation is greatly increased.

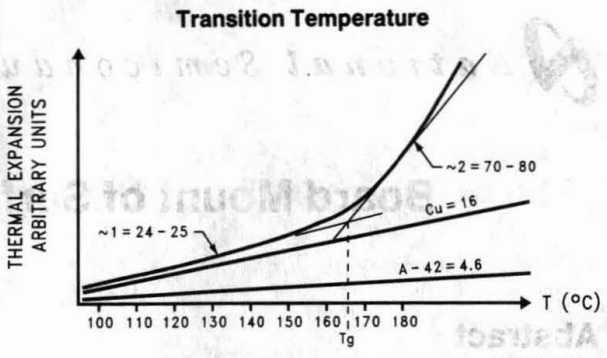

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FIGURE 1. Thermal Expansion and Glass

Conventional Wave Soldering

Most wave soldering operations occur at temperatures between 240°C–260°C. Conventional epoxies for encapsulation have glass-transition temperatures between 140°C–170°C. An I.C. directly exposed to these temperatures risks its long term functionality due to epoxy/metal separation.

Fortunately, there are factors that can reduce that element of risk:

1. The PW board has a certain amount of heat-sink effort and tends to shield the components from the temperature of the solder (if they were placed on the top side of the board). In actual measurements, DIPs achieve a temperature between 120°C–150°C in a 5-second pass over the solder. This accounts for the fact that DIPs mounted in the conventional manner are reliable.
2) In conventional soldering, only the tip of each lead in DIP would experience the solder temperature because the epoxy and die are standing above the PW board and out of the solder bath.

Effect on Package Performance by Epoxy-Metal Separation

In wave soldering, it is necessary to use fluxes to assist the solderability of the components and PW boards. Some facilities may even process the boards and components through some form of acid cleaning prior to the soldering temperature. If separation occurs, the flux residues and acid residues (which may be present owing to inadequate cleaning) will be forced into the package mainly by capillary action as the residues move away from the solder heat source. Once the package is cooled, these contaminants are now trapped within the package and are available to diffuse with moisture from the epoxy over time. It should be noted that electrical tests performed immediately after soldering generally will give no indication of this potential problem. In any case, the end result will be corrosion of the chip metalization over time and premature failure of the device in the field.

Vapor Phase/IR Reflow Soldering

In both vapor phase and IR reflow soldering, the risk of separation between epoxy/metal can also be high. Maximum operating temperatures are 219°C (vapor phase) or 240°C (IR) and duration may also be longer (30 sec–60 sec). On the same theoretical basis, there should also be separation. However, in both these methods, solder paste is applied to the pads of the boards; no fluxes are used. Also, the devices are not immersed into the hot solder. This reduces the possibility of solder forcing itself into the epoxy-leadframe interface. Furthermore, in the vapor phase system, the soldering environment is "oxygen-free" and considered "contaminant free". Being so, it could be visualized that as far as reliability with respect to corrosion, both of these methods are advantageous over wave soldering.

Bias Moisture Test

A bias moisture test was designed to determine the effect on package performance. In this test, the packages are pressured in a steam chamber to accelerate penetration of moisture into the package. An electrical bias is applied on the device. Should there be any contaminants trapped within the package, the moisture will quickly form an electrolyte and cause the electrodes (which are the lead fingers), the gold wire and the aluminum bond-pads of the silicon device to corrode. The aluminum bond-pads, being the weakest link of the system, will generally be the first to fail.

This proprietary accelerated bias/moisture pressure-test is significant in relation to the life test condition at 85°C and 85% relative humidity. One cycle of approximately 100 hours has been shown to be equivalent to 2,000 hours in the 85/85 condition. Should the packages start to fail within the first cycle in the test, it is anticipated that the boards with these components in the harsh operating environment (85°C/85% RH) will experience corrosion and eventual electrical failures within its first 2,000 hours of operation.

Whether this is significant to a circuit board manufacturer will obviously be dependent on the products being manufactured and the workmanship or reliability standards. Generally in systems with a long warranty and containing many components, it is advisable both on a reputation and cost basis to have the most reliable parts available.

Test Results

The comparison of vapor phase and wave-soldering upon the reliability of molded Small-Outline packages was performed using the bias moisture test (see Table IV). It is clearly seen that vapor phase reflow soldering gave more consistent results. Wave soldering results were based on manual operation giving variations in soldering parameters such as temperature and duration.

TABLE IV. Vapor Phase vs. Wave Solder

1. Vapor phase (60 sec. exposure @ 217°C)
   = 9 failures/1723 samples
   = 0.5% (average over 32 sample lots)
2. Wave solder (2 sec total immersion @ 260°C)
   = 16 failures/1201 samples
   = 1.3% (average over 27 sample lots)

Package: SO-14 lead
Test: Bias moisture test 85% R.H.
85°C for 2,000 hours
Device: LM324M

In Table V we examine the tolerance of the Small-Outlined (SOIC) package to varying immersion time in a hot solder pot. SO-14 lead molded packages were subjected to the bias moisture test after being treated to the various soldering conditions and repeated four (4) times. End point was an electrical test after an equivalent of 4,000 hours 85/85 test. Results were compared for packages by themselves against packages which were surface-mounted onto a FR-4 printed wire board.

TABLE V. Summary of Wave Solder Results

	Unmounted	Mounted
Control/Vapor Phase 15 sec @ 215°C	0/114	0/84
Solder Dip 4 Sec @ 260°C	2/144 (1.4%)	0/85
Solder Dip 4 Sec @ 260°C	—	0/83
Solder Dip 6 Sec @ 260°C	13/248 (5.2%)	1/76 (1.3%)
Solder Dip 10 Sec @ 260°C	14/127 (11.0%)	3/79 (3.8%)
Package: SO-14 lead Device: LM324M		

Since the package is of very small mass and experiences a rather sharp thermal shock followed by stresses created by the mismatch in expansion, the results show the packages being susceptible to failures after being immersed in excess of 6 seconds in a solder pot. In the second case where the packages were mounted, the effect of severe temperature excursion was reduced. In any case, because of the repeated treatment, the package had failures when subjected in excess of 6 seconds immersion in hot solder. The safety margin is therefore recommended as maximum 4 seconds immersion. If packages were immersed longer than 4 seconds, there is a probable chance of finding some long term reliability failures even though the immediate electrical test data could be acceptable.

Finally, Table VI examines the bias moisture test performed on surface mount (SOIC) components manufactured by various semiconductor houses. End point was an electrical test after an equivalent of 6,000 hours in an 85/85 test. Failures were analyzed and corrosion was checked for in each case to detect flaws in package integrity.

TABLE VI. U.S. Manufacturing Integrated Circuits Reliability in Various Solder Environments (# Failure/Total Environment)

Package SO-8	Vapor Phase 30 sec	Wave Solder 2 sec	Wave Solder 4 sec	Wave Solder 6 sec	Wave Solder 10 sec
Manuf A	8/30*	1/30*	0/30	12/30*	16/30*
Manuf B	2/30*	8/30*	2/30*	22/30*	20/30*
Manuf C	0/30	0/29	0/29	0/30	0/30
Manuf D	1/30*	12/30*	14/30*	2/30*	
Manuf E	1/30**	0/30	0/30	0/30	
Manuf F	0/30	0/30	0/30	0/30	
NSC	0/30	0/30	0/30	0/30	

*Corrosion failures

**No Visual Defects-Non-corrosion failues

Test Accelerated Bias Moisture Test: 85% R.H./85°C. 6,000 equivalent hours

Summary

Based on the results presented, it is noted that surface-mounted components are as reliable as standard molded DIP packages. Whereas DIPs were never processed by being totally immersed in hot solder wave during printed circuit board soldering, surface mounted components such as SOICs (Small Outline) are expected to survive a total immersion in the hot solder in order to capitalize on maximum population on boards. Being constructed from a thermoset plastic of relatively low T_g compared to the soldering temperature, the ability of the package to survive is dependent on the time of immersion and also the cleanliness of material. The results indicate that one should limit the immersion time of the package in the solder wave to a maximum of 4 seconds in order to truly duplicate the reliability of a DIP. As the package size is reduced, as in a SO-8 lead, the requirement becomes even more critical. This is shown by the various manufacturers' performance. Results indicate there is room for improvement since not all survived the hot solder immersion without compromise to lower reliability.

National Semiconductor

Recommended Soldering Profiles—Surface Mount

		Wave Solder	IR Profile	Vapor Phase
Ramp Up °C/sec	Maximum	6°C/sec	4°C/sec	24°C/sec
	Recommended	**4°C/sec***	**2°C/sec***	**2°C/sec**
	Minimum	**	**	**
ΔT	Maximum	135°C	N/A	N/A
	Recommended	**120°C**	**N/A**	**N/A**
	Minimum	110°C	N/A	N/A
Dwell Time ≥ 183°C	Maximum	N/A	85 seconds	85 seconds
	Recommended	**N/A**	**75 seconds***	**75 seconds***
	Minimum	N/A	30 seconds**	**
Solder Temperature	Maximum	260°C	240°C***	219°C
	Recommended	**240°C**	**215°C***	**215°C***
	Minimum	**	**	**
Dwell Time @ Max.	Maximum	4 seconds	10 seconds	75
	Recommended	**3 seconds**	**5 seconds**	**70 seconds**
	Minimum	**	1 second	**
Ramp Down °C/sec	Maximum	No Information	4°C/sec	4°C/sec
	Recommended	**4°C/sec**	**2°C/sec**	**2°C/sec**
	Minimum	No Information	**	**

Note: Temperature in degrees celcius. N/A = Not Applicable.

ΔT = The temperature differential between the final preheat stage and the soldering stage. Temperature measured at the component lead area.

*Will vary depending on board density, geometry, and package type.

**Will vary depending on package types, and board density.

***For plastic packages; ceramic packages maximum may be 250°C.

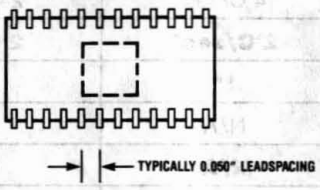
Small Outline (SO) Package Surface Mounting Methods-Parameters and Their Effect on Product Reliability

National Semiconductor
Application Note 450
Josip Huljev
W. K. Boey

The SO (small outline) package has been developed to meet customer demand for ever-increasing miniaturization and component density.

COMPONENT SIZE COMPARISON

S.O. Package



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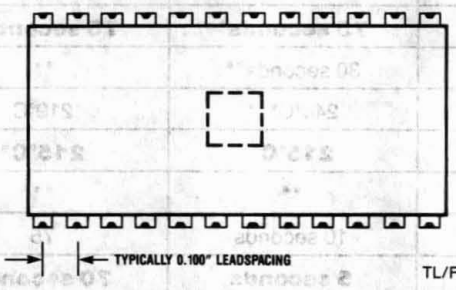
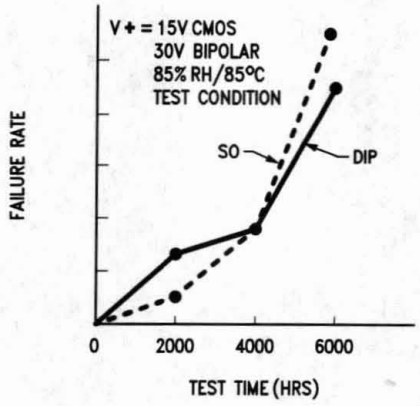
Standard DIP Package



TL/F/8766–2

Because of its small size, reliability of the product assembled in SO packages needs to be carefully evaluated.

SO packages at National were internally qualified for production under the condition that they be of comparable reliability performance to a standard dual in line package under all accelerated environmental tests. *Figure A* is a summary of accelarated bias moisture test performance on 30V bipolar and 15V CMOS product assembled in SO and DIP (control) packages.



TL/F/8766–3

FIGURE A

In order to achieve reliability performance comparable to DIPs—SO packages are designed and built with materials and processes that effectively compensate for their small size.

All SO packages tested on 85%RA, 85°C were assembled on PC conversion boards using vapor-phase reflow soldering. With this approach we are able to measure the effect of surface mounting methods on reliability of the process. As illustrated in *Figure A* no significant difference was detected between the long term reliability performance of surface mounted S.O. packages and the DIP control product for up to 6000 hours of accelerated 85%/85°C testing.

SURFACE-MOUNT PROCESS FLOW

The standard process flowcharts for basic surface-mount operation and mixed-lead insertion/surface-mount operations, are illustrated on the following pages.

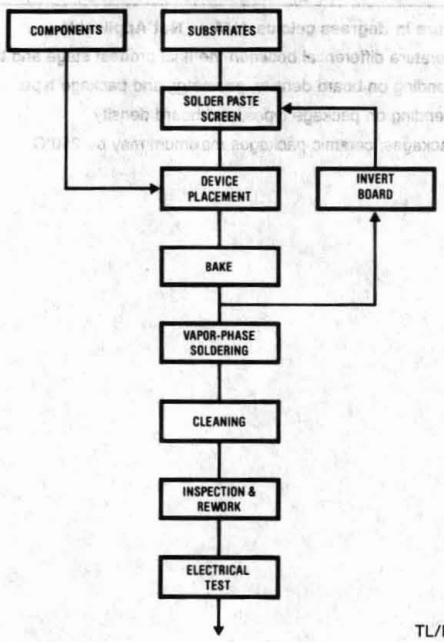
Usual variations encountered by users of SO packages are:

- Single-sided boards, surface-mounted components only.
- Single-sided boards, mixed-lead inserted and surface-mounted components.
- Double-sided boards, surface-mounted components only.
- Double-sided boards, mixed-lead inserted and surface-mounted components.

In consideration of these variations, it became necessary for users to utilize techniques involving wave soldering and adhesive applications, along with the commonly-used vapor-phase solder reflow soldering technique.

PRODUCTION FLOW

Basic Surface-Mount Production Flow



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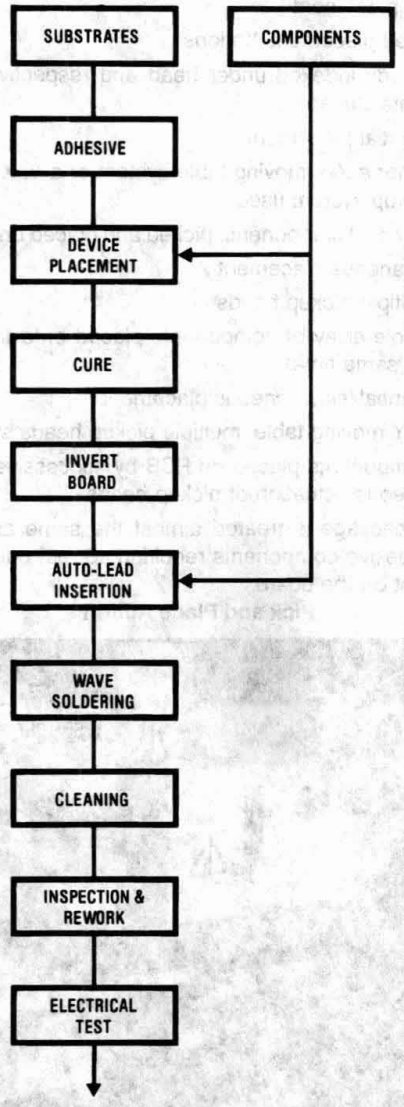
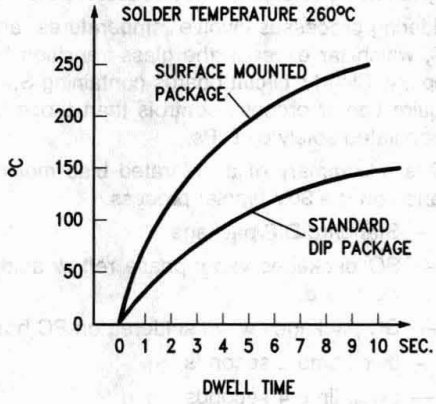
Mixed Surface-Mount and Axial-Leaded Insertion Components Production Flow



TL/F/8766–5

Thermal stress of the packages during surface-mounting processing is more severe than during standard DIP PC board mounting processes. *Figure B* illustrates package temperature versus wave soldering dwell time for surface mounted packages (components are immersed into the molten solder) and the standard DIP wave soldering process. (Only leads of the package are immersed into the molten solder).

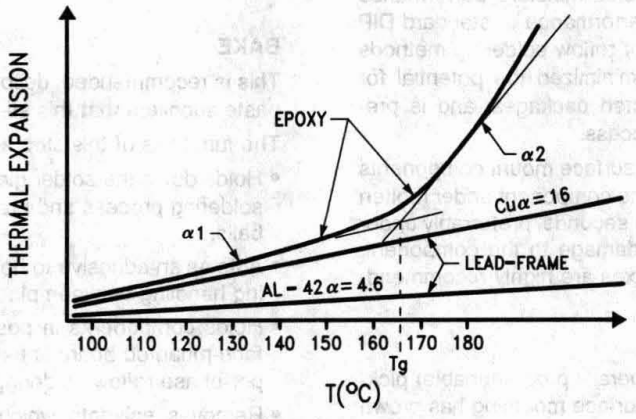


TL/F/8766–6

FIGURE B

For an ideal package, the thermal expansion rate of the encapsulant should match that of the leadframe material in order for the package to maintain mechanical integrity during the soldering process. Unfortunately, a perfect matchup of thermal expansion rates with most presently used packaging materials is scarce. The problem lies primarily with the epoxy compound.

Normally, thermal expansion rates for epoxy encapsulant and metal lead frame materials are linear and remain fairly close at temperatures approaching 160°C, *Figure C.* At lower temperatures the difference in expansion rate of the two materials is not great enough to cause interface separation. However, when the package reaches the glass-transition temperature (T_g) of epoxy (typically 160–165°C), the thermal expansion rate of the encapsulant increases sharply, and the material undergoes a transition into a plastic state. The epoxy begins to expand at a rate three times or more greater than the metal leadframe, causing a separation at the interface.



TL/F/8766–26

FIGURE C

When this happens during a conventional wave soldering process using flux and acid cleaners, process residues and even solder can enter the cavity created by the separation and become entrapped when the material cools. These contaminants can eventually diffuse into the interior of the package, especially in the presence of moisture. The result is die contamination, excessive leakage, and even catastrophic failure. Unfortunately, electrical tests performed immediately following soldering may not detect potential flaws.

Most soldering processes involve temperatures ranging up to 260°C, which far exceeds the glass-transition temperature of epoxy. Clearly, circuit boards containing SMD packages require tighter process controls than those used for boards populated solely by DIPs.

Figure D is a summary of accelerated bias moisture test performance on the 30V bipolar process.

Group 1 — Standard DIP package

Group 2 — SO packages vapor-phase reflow soldered on PC boards

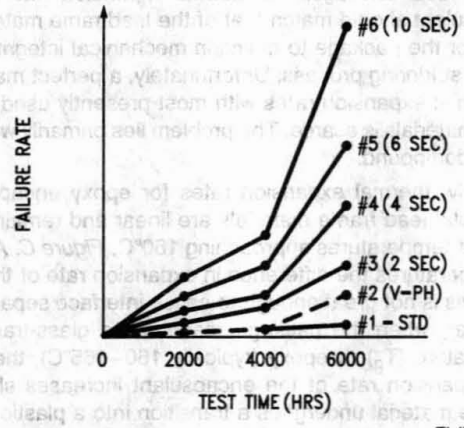
Group 3–6 SO packages wave soldered on PC boards

Group 3 — dwell time 2 seconds

4 — dwell time 4 seconds

5 — dwell time 6 seconds

6 — dwell time 10 seconds



TL/F/8766–7

FIGURE D

It is clear based on the data presented that SO packages soldered onto PC boards with the vapor phase reflow process have the best long term bias moisture performance and this is comparable to the performance of standard DIP packages. The key advantage of reflow soldering methods is the clean environment that minimized the potential for contamination of surface mounted packages, and is preferred for the surface-mount process.

When wave soldering is used to surface mount components on the board, the dwell time of the component under molten solder should be no more than 4 seconds, preferrably under 2 seconds in order to prevent damage to the component. Non-Halide, or (organic acid) fluxes are highly recommended.

PICK AND PLACE

The choice of automatic (all generally programmable) pick-and-place machines to handle surface mounting has grown considerably, and their selection is based on individual needs and degree of sophistication.

The basic component-placement systems available are classified as:

(a) In-line placement

— Fixed placement stations

— Boards indexed under head and respective components placed

(b) Sequential placement

— Either a X-Y moving table system or a θ, X-Y moving pickup system used

—Individual components picked and placed onto boards

(c) Simultaneous placement

— Multiple pickup heads

— Whole array of components placed onto the PCB at the same time

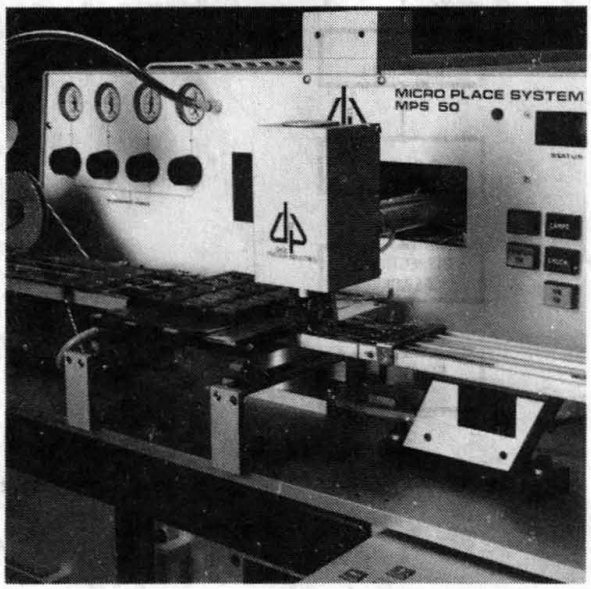
(d) Sequential/simultaneous placement

— X–Y moving table, multiple pickup heads system

— Components placed on PCB by successive or simultaneous actuation of pickup heads

The SO package is treated almost the same as surface-mount, passive components requiring correct orientation in placement on the board.

Pick and Place Action



TL/F/8766–8

BAKE

This is recommended, despite claims made by some solder paste suppliers that this step be omitted.

The functions of this step are:

- Holds down the solder globules during subsequent reflow soldering process and prevents expulsion of small solder balls.
- Acts as an adhesive to hold the components in place during handling between placement to reflow soldering.
- Holds components in position when a double-sided surface-mounted board is held upside down going into a vapor-phase reflow soldering operation.
- Removes solvents which might otherwise contaminate other equipment.
- Initiates activator cleaning of surfaces to be soldered.
- Prevents moisture absorption.

The process is moreover very simple. The usual schedule is about 20 minutes in a 65°C–95°C (dependent on solvent system of solder paste) oven with adequate venting. Longer bake time is not recommended due to the following reasons:

- The flux will degrade and affect the characteristics of the paste.
- Solder globules will begin to oxidize and cause solderability problems.
- The paste will creep and after reflow, may leave behind residues between traces which are difficult to remove and vulnerable to electro-migration problems.

REFLOW SOLDERING

There are various methods for reflowing the solder paste, namely:

- Hot air reflow
- Infrared heating (furnaces)
- Convectional oven heating
- Vapor-phase reflow soldering
- Laser soldering

For SO applications, hot air reflow/infrared furnace may be used for low-volume production or prototype work, but vapor-phase soldering reflow is more efficient for consistency and speed. Oven heating is not recommended because of "hot spots" in the oven and uneven melting may result. Laser soldering is more for specialized applications and requires a great amount of investment.

HOT GAS REFLOW/INFRARED HEATING

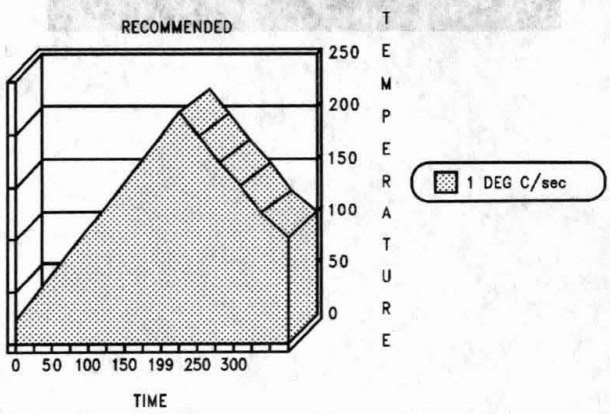
A hand-held or table-mount air blower (with appropriate orifice mask) can be used.

The boards are preheated to about 100°C and then subjected to an air jet at about 260°C. This is a slow process and results may be inconsistent due to various heat-sink properties of passive components.

INFRARED REFLOW SOLDERING

Use of an infrared furnace is currently the most popular method to automate mass reflow, the heating is promoted by use of IR lamps or panels. Early objections to this method were that certain materials may heat up at different rates under IR radiation and could result in damage to those components (usually sockets and connectors). This has been minimized by using far-infrared (non-focused) systems and convected air.

Infrared Profile



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VAPOR-PHASE REFLOW SOLDERING

Currently the most popular and consistent method, vapor-phase soldering utilizes a fluoroinert fluid with excellent heat-transfer properties to heat up components until the solder paste reflows. The maximum temperature is limited by the vapor temperature of the fluid.

The commonly used fluids (supplied by 3M Corp) are:

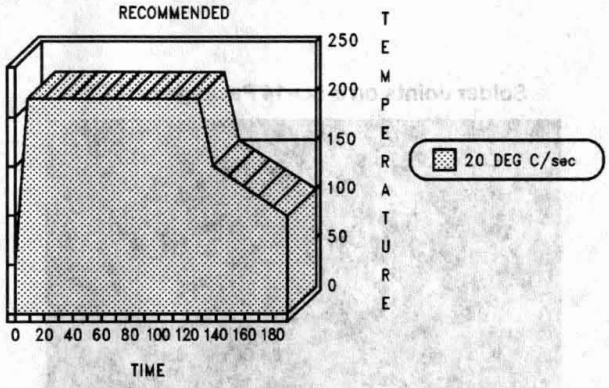
- FC-70, 215°C vapor (most applications) or FX-38
- FC-71, 253°C vapor (low-lead or tin-plate)

HTC, Concord, CA, manufactures equipment that utilizes this technique, with two options:

- Batch systems, where boards are lowered in a basket and subjected to the vapor from a tank of boiling fluid.
- In-line conveyorized systems, where boards are placed onto a continuous belt which transports them into a concealed tank where they are subjected to an environment of hot vapor.

Dwell time in the vapor is generally on the order of 15–30 seconds (depending on the mass of the boards and the loading density of boards on the belt).

Vapor-Phase Profile



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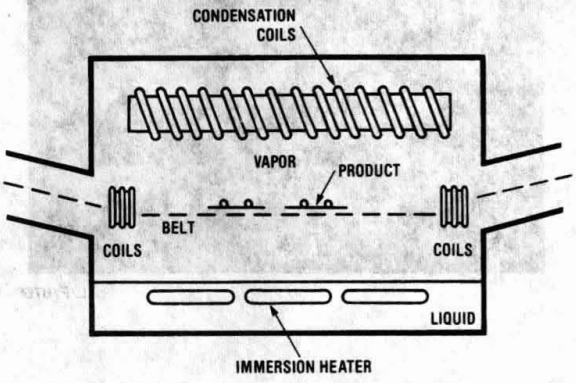
In-Line Conveyorized Vapor-Phase Soldering



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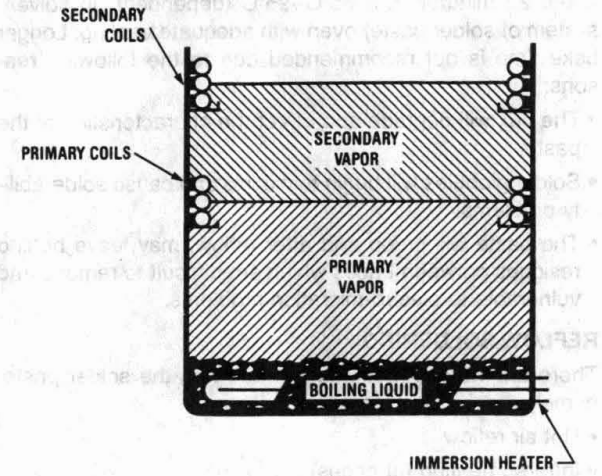
The question of thermal shock is asked frequently because of the relatively sharp increase in component temperature from room temperature to 215°C. SO packages mounted on representative boards have been tested and have shown little effect on the integrity of the packages. Various packages, such as cerdips, metal cans and TO-5 cans with glass seals, have also been tested.

Vapor-Phase Furnace

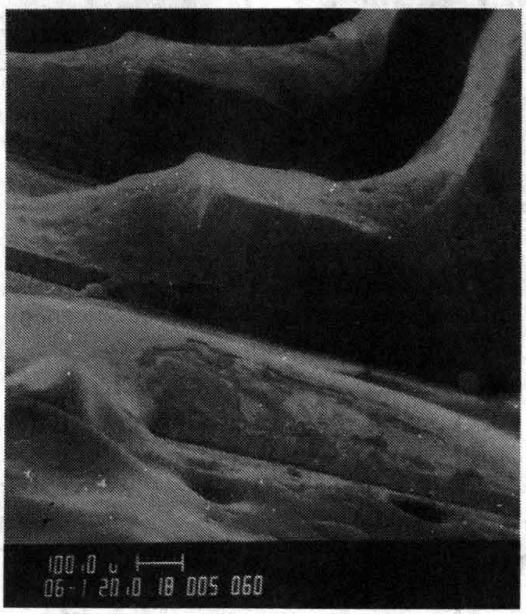
TL/F/8766–10

Batch-Fed Production Vapor-Phase Soldering Unit



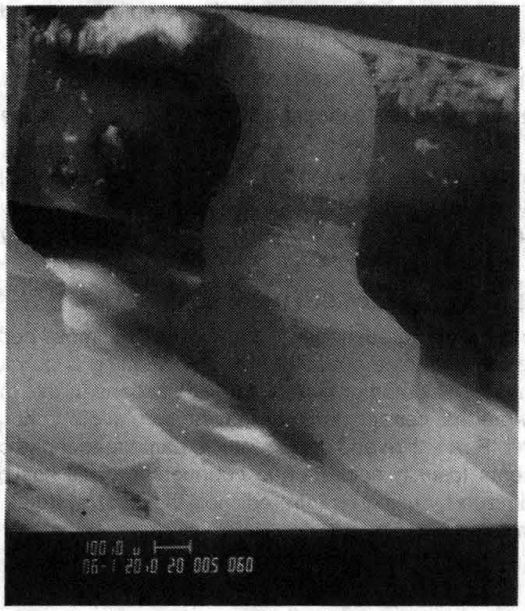
TL/F/8766–11

Solder Joints on a SO-14 Package on PCB



TL/F/8766–12

Solder Joints on a SO-14 Package on PCB



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PRINTED CIRCUIT BOARD

The SO package is molded out of clean, thermoset plastic compound and has no particular compatibility problems with most printed circuit board substrates.

The package can be reliably mounted onto substrates such as:

- G10 or FR4 glass/resin
- FR5 glass/resin systems for high-temperature applications
- Polymide boards, also high-temperature applications
- Ceramic substrates

General requirements for printed circuit boards are:

- Mounting pads should be solder-plated whenever applicable.
- Solder masks are commonly used to prevent solder bridging of fine lines during soldering.

  The mask also protects circuits from processing chemical contamination and corrosion.

  If coated over pre-tinned traces, residues may accumulate at the mask/trace interface during subsequent reflow, leading to possible reliability failures.

  Recommended application of solder resist on bare, clean traces prior to coating exposed areas with solder.

  General requirements for solder mask:

  — Good pattern resolution.

  — Complete coverage of circuit lines and resistance to flaking during soldering.

  — Adhesion should be excellent on substrate material to keep off moisture and chemicals.

  — Compatible with soldering and cleaning requirements.

SOLDER PASTE SCREEN PRINTING

With the initial choice of printed circuit lithographic design and substrate material, the first step in surface mounting is the application of solder paste.

The typical lithographic "footprints" for SO packages are illustrated below. Note that the 0.050″ lead center-center spacing is not easily managed by commercially-available air pressure, hand-held dispensers.

Using a stainless-steel, wire-mesh screen stencilled with an emulsion image of the substrate pads is by far the most common and well-tried method. The paste is forced through the screen by a V-shaped plastic squeegee in a sweeping manner onto the board placed beneath the screen.

The setup for SO packages has no special requirement from that required by other surface-mounted, passive components. Recommended working specifications are:

- Use stainless-steel, wire-mesh screens, #80 or #120, wire diameter 2.6 mils. Rule of thumb: mesh opening should be approximately 2.5–5 times larger than the average particle size of paste material.
- Use squeegee of Durometer 70.
- Experimentation with squeegee travel speed is recommended, if available on machine used.
- Use solder paste of mesh 200–325.
- Emulsion thickness of 0.005″ usually used to achieve a solder paste thickness (wet) of about 0.008″ typical.
- Mesh pattern should be 90 degrees, square grid.
- Snap-off height of screen should not exceed ⅛″, to avoid damage to screens and minimize distortion.

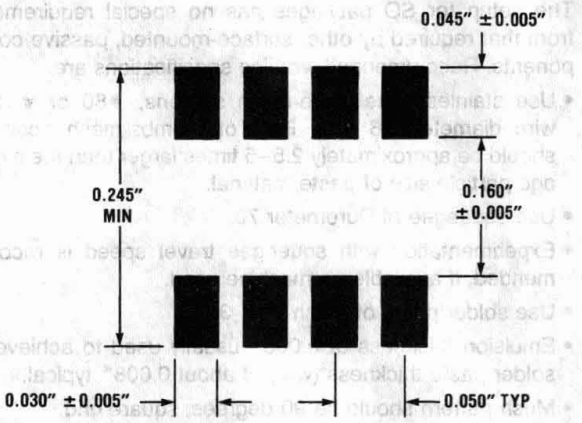
SOLDER PASTE

Selection of solder paste tends to be confusing, due to numerous formulations available from various manufacturers. In general, the following guidelines are sufficient to qualify a particular paste for production:

- Particle sizes (see following photographs). Mesh 325 (approximately 45 microns) should be used for general purposes, while larger (solder globules) particles are preferred for leadless components (LCC). The larger particles can easily be used for SO packages.
- Uniform particle distribution. Solder globules should be spherical in shape with uniform diameters and minimum amount of elongation (visual under 100/200 × magnification). Uneven distribution causes uneven melting and subsequent expulsion of smaller solder balls away from their proper sites.
- Composition, generally 60/40 or 63/37 Sn/Pb. Use 62/36 Sn/Pb with 2% Ag in the presence of Au on the soldering area. This formulation reduces problems of metal leaching from soldering pads.
- RMA flux system usually used.
- Use paste with aproximately 88–90% solids.

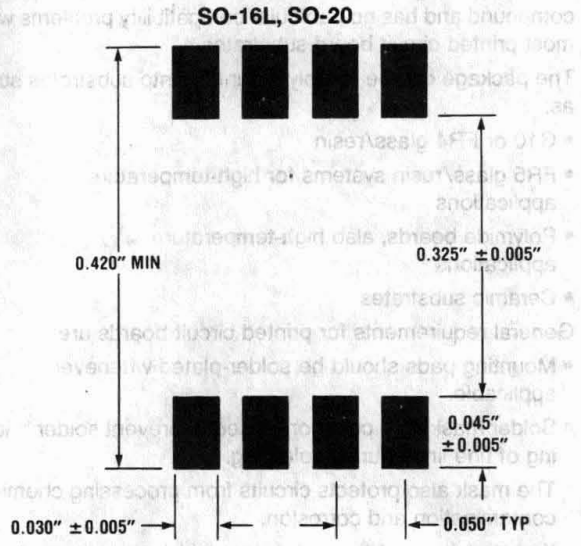
RECOMMENDED SOLDER PADS FOR SO PACKAGES

SO-8, SO-14, SO-16



TL/F/8766–14

SO-16L, SO-20



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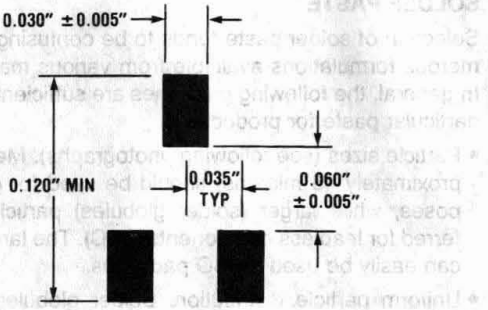
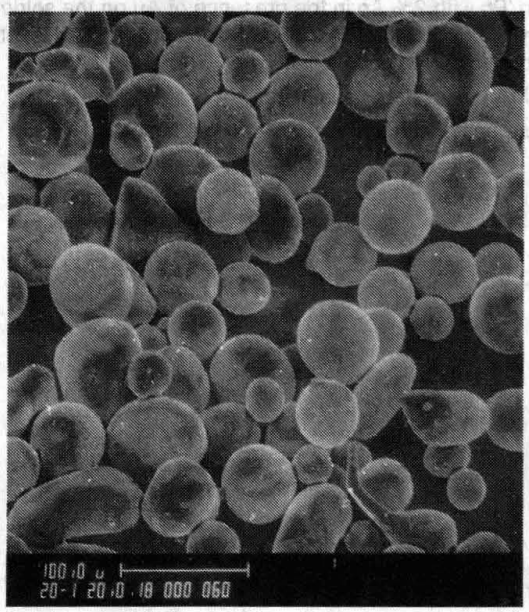
SOT-23



TL/F/8766–16

Comparison of Particle Size/Shape of Various Solder Pastes

200 × Alpha (62/36/2)



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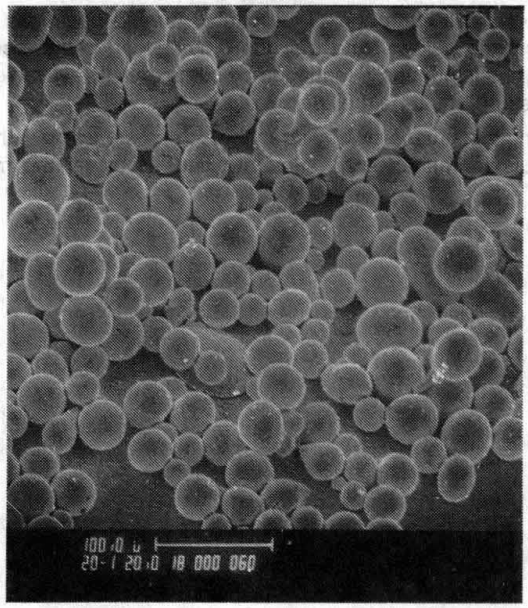
200 × Kester (63/37)



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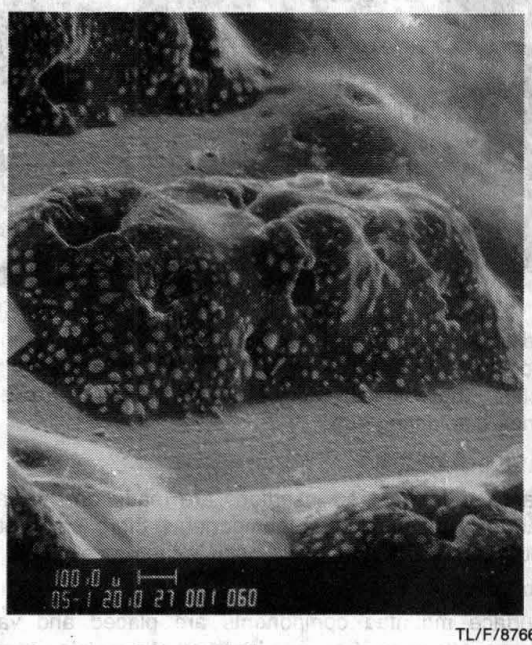
Comparison of Particle Size/Shape of Various Solder Pastes (Continued)

Solder Paste Screen on Pads



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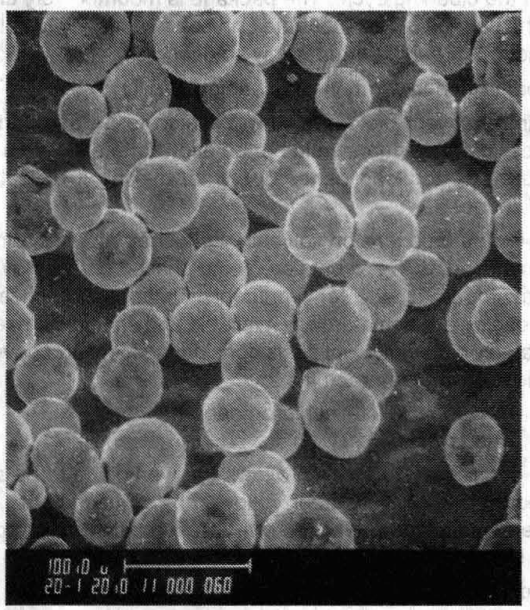
200 × Fry Metal (63/37)



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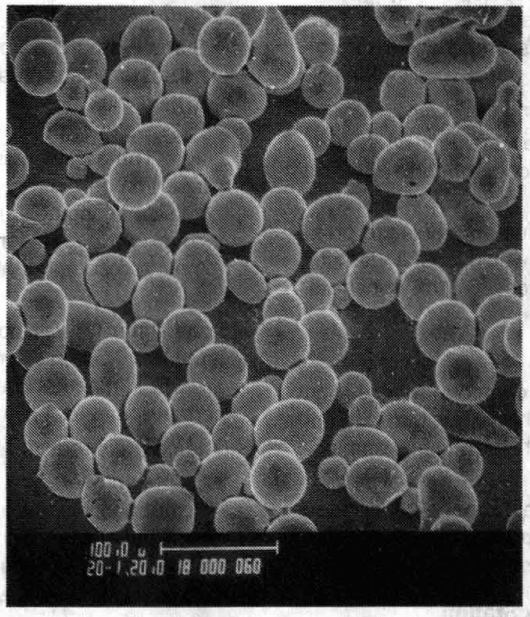
200 ESL (63/37)



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CLEANING

The most critical process in surface mounting SO packages is in the cleaning cycle. The package is mounted very close to the surface of the substrate and has a tendency to collect residue left behind after reflow soldering.

Important considerations in cleaning are:

- Time between soldering and cleaning to be as short as possible. Residue should not be allowed to solidify on the substrate for long periods of time, making it difficult to dislodge.
- A low surface tension solvent (high penetration) should be employed. CFC solvents are being phased out as they are hazardous to the environment. Other approaches to cleaning are commercially available and should be investigated on an individual basis considering local and government environmental rules.

  Prelete or 1,1,1-Trichloroethane
  Kester 5120/5121
- A defluxer system which allows the workpiece to be subjected to a solvent vapor, followed by a rinse in pure solvent and a high-pressure spray lance are the basic requirments for low-volume production.
- For volume production, a conveyorized, multiple hot solvent spray/jet system is recommended.
- Rosin, being a natural occurring material, is not readily soluble in solvents, and has long been a stumbling block to the cleaning process. In recent developments, synthetic flux (SA flux), which is readily soluble in Freon TMS solvent, has been developed. This should be explored where permissible.

The dangers of an inadequate cleaning cycle are:

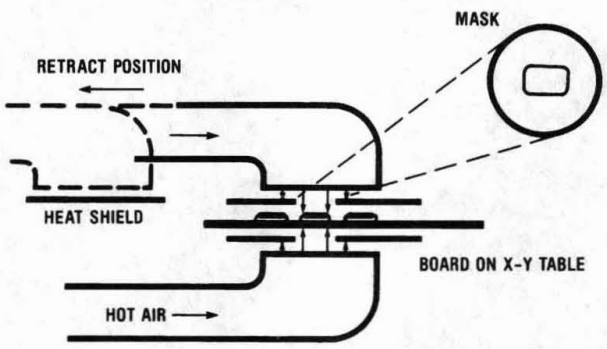
- Ion contamination, where ionic residue left on boards would cause corrosion to metallic components, affecting the performance of the board.
- Electro-migration, where ionic residue and moisture present on electrically-biased boards would cause dentritic growth between close spacing traces on the substrate, resulting in failures (shorts).

REWORK

Should there be a need to replace a component or re-align a previously disturbed component, a hot air system with appropriate orifice masking to protect surrounding components may be used.

When rework is necessary in the field, specially-designed tweezers that thermally heat the component may be used to remove it from its site. The replacement can be fluxed at the lead tips or, if necessary, solder paste can be dispensed onto the pads using a varimeter. After being placed into position, the solder is reflowed by a hot-air jet or even a standard soldering iron.

Hot-Air Solder Rework Station



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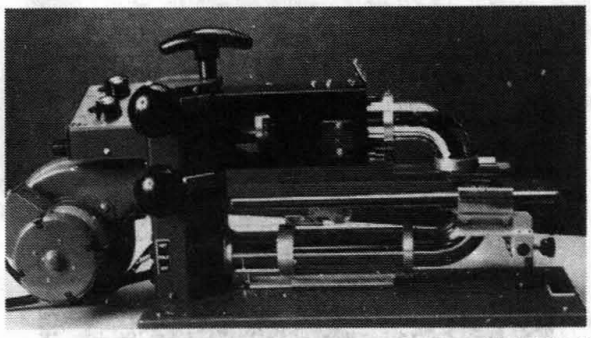
Hot-Air Rework Machine



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WAVE SOLDERING

In a case where lead insertions are made on the same board as surface-mounted components, there is a need to include a wave-soldering operation in the process flow.

Two options are used:

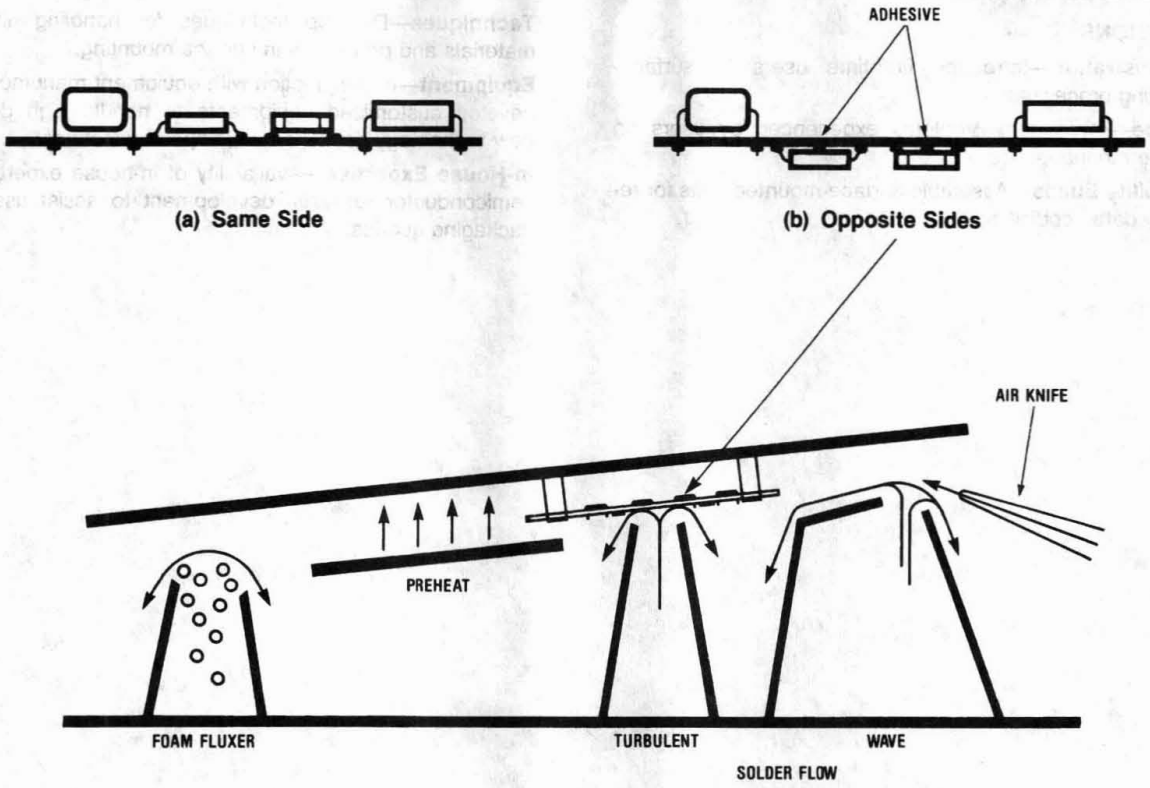
- Surface mounted components are placed and vapor phase reflowed before auto-insertion of remaining components. The board is carried over a standard wave-solder system and the underside of the board (only lead-inserted leads) soldered.
- Surface-mounted components are placed in position, but no solder paste is used. Instead, a drop of adhesive about 5 mils maximum in height with diameter not exceeding 25% width of the package is used to hold down the package. The adhesive is cured and then proceeded to auto-insertion on the reverse side of the board (surface-mounted side facing down). The assembly is then passed over a "dual wave" soldering system. Note that the surface-mounted components are immersed into the molten solder.

Lead trimming will pose a problem after soldering in the latter case, unless the leads of the insertion components are pre-trimmed or the board specially designed to localize certain areas for easy access to the trim blade.

The controls required for wave soldering are:

- Solder temperature to be 240–260°C. The dwell time of components under molten solder to be short (preferably kept under 2 seconds), to prevent damage to most components and semiconductor devices.
- RMA (Rosin Mildly Activated) flux or more aggressive OA (Organic Acid) flux are applied by either dipping or foam fluxing on boards prior to preheat and soldering. Cleaning procedures are also more difficult (aqueous, when OA flux is used), as the entire board has been treated by flux (unlike solder paste, which is more or less localized). Non-halide OA fluxes are highly recommended.
- Preheating of boards is essential to reduce thermal shock on components. Board should reach a temperature of about 100°C just before entering the solder wave.
- Due to the closer lead spacings (0.050″ vs 0.100″ for dual-in-line packages), bridging of traces by solder could occur. The reduced clearance between packages also causes "shadowing" of some areas, resulting in poor solder coverage. This is minimized by dual-wave solder systems.

Mixed Surface Mount and Lead Insertion



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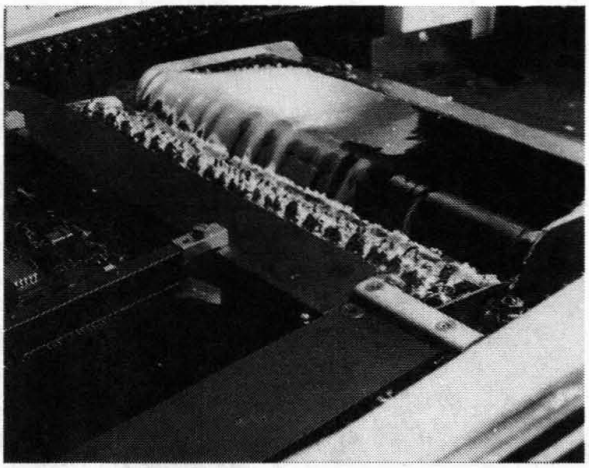
A typical dual-wave system is illustrated below, showing the various stages employed. The first wave typically is in turbulence and given a transverse motion (across the motion of the board). This covers areas where "shadowing" occurs. A second wave (usually a broad wave) then proceeds to perform the standard soldering. The departing edge from the solder is such to reduce "icicles," and is still further reduced by an air knife placed close to the final soldering step. This air knife will blow off excess solder (still in the fluid stage) which would otherwise cause shorts (bridging) and solder bumps.

AQUEOUS CLEANING

- For volume production, a conveyorized system is often used with a heated recirculating spray wash (water temperature 130°C), a final spray rinse (water temperature 45–55°C), and a hot (120°C) air/air-knife drying section.
- For low-volume production, the above cleaning can be done manually, using several water rinses/tanks. Fast-drying solvents, like alcohols that are miscible with water, are sometimes used to help the drying process.
- Neutralizing agents which will react with the corrosive materials in the flux and produce material readily soluble in water may be used; the choice depends on the type of flux used.
- Final rinse water should be free from chemicals which are introduced to maintain the biological purity of the water. These materials, mostly chlorides, are detrimental to the assemblies cleaned because they introduce a fresh amount of ionizable material.

Dual Wave



TL/F/8766–25

CONFORMAL COATING

Conformal coating is recommended for high-reliability PCBs to provide insulation resistance, as well as protection against contamination and degradation by moisture.

Requirements:

- Complete coating over components and solder joints.
- Thixotropic material which will not flow under the packages or fill voids, otherwise will introduce stress on solder joints on expansion.
- Compatibility and possess excellent adhesion with PCB material/components.
- Silicones are recommended where permissible in application.

SMD Lab Support

FUNCTIONS

Demonstration—Introduce first-time users to surface-mounting processes.

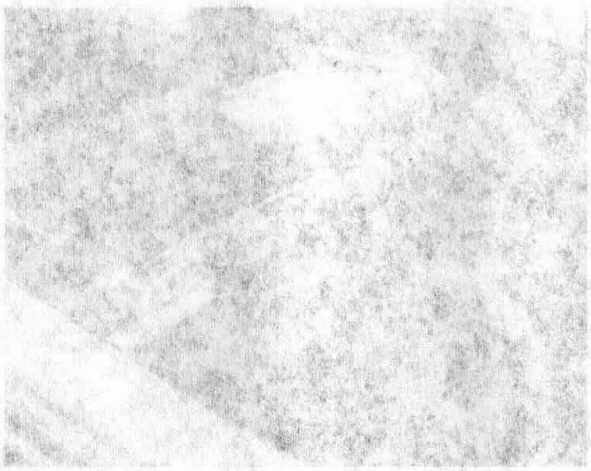
Service—Investigate problems experienced by users on surface mounting.

Reliability Builds—Assemble surface-mounted units for reliability data acquisition.

Techniques—Develop techniques for handling different materials and processes in surface mounting.

Equipment—In conjunction with equipment manufacturers, develop customized equipments to handle high density, new technology packages developed by National.

In-House Expertise—Availability of in-house expertise on semiconductor research/development to assist users on packaging queries.



National Semiconductor

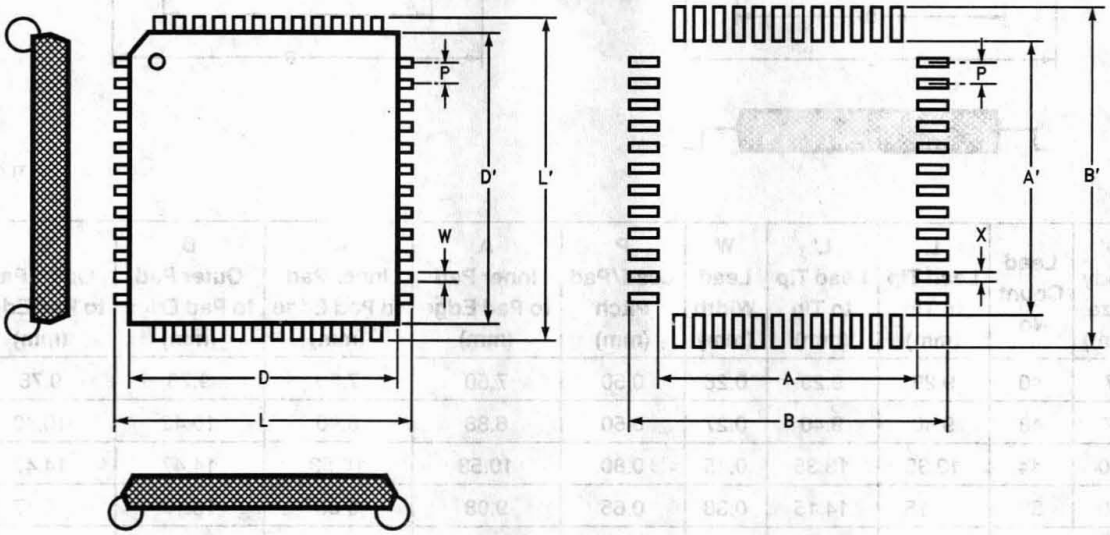
Land Pattern Recommendations

The following land pattern recommendations are provided as guidelines for board layout and assembly purposes.

These recommendations cover the following National Semiconductor packages: PLCC, PQFP, SOP, SSOP and TSOP.

For SOT-23 (5-Lead) and TO-263 (3- or 5-Lead) packages, refer to land patterns shown in the Physical Dimensions for MA05A and TS3B or TS5B packages, respectively.

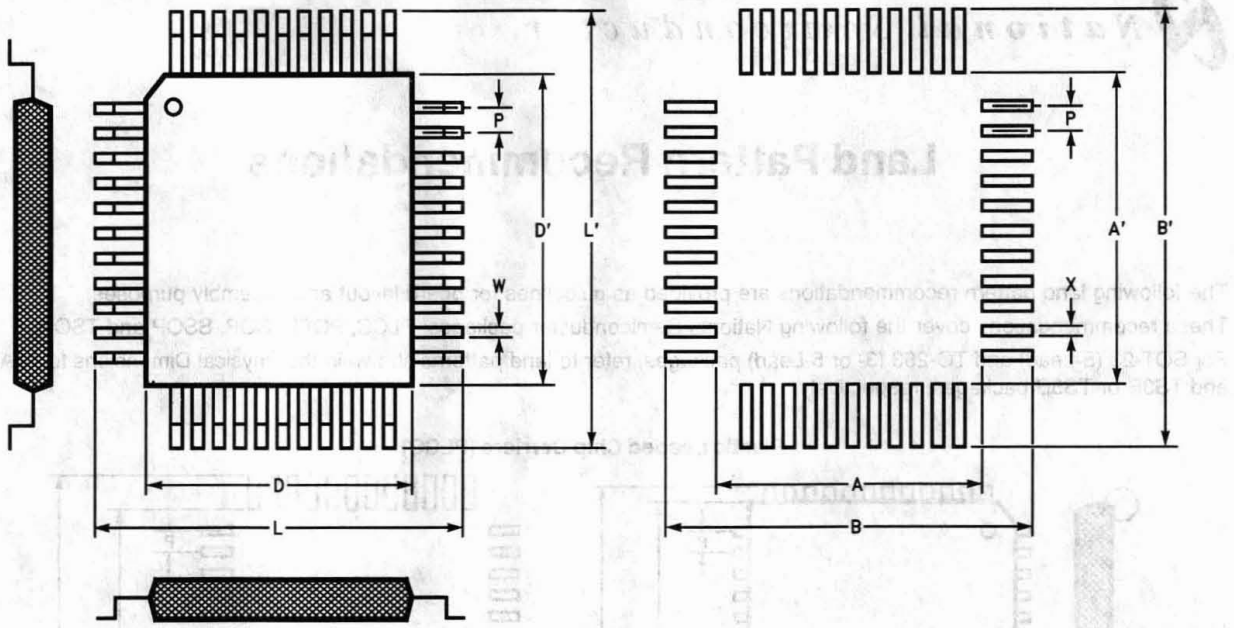
Plastic Leaded Chip Carriers (PLCC)



TL/P/11811–1

D Body Size (mm)	D' Body Size (mm)	Lead Count No.	L Lead Tip to Tip (mm)	L' Lead Tip to Tip (mm)	W Lead Width (mm)	P Lead/Pad Pitch (mm)	A Inner Pad to Pad Edge (mm)	A' Inner Pad to Pad Edge (mm)	B Outer Pad to Pad Edge (mm)	B' Outer Pad to Pad Edge (mm)	X Land Width (mm)
8.89	8.89	20	10.03	10.03	0.53	1.27	6.73	6.73	10.80	10.80	0.63
11.43	11.43	28	12.57	12.57	0.53	1.27	9.27	9.27	13.34	13.34	0.63
11.43	14.05	32	12.57	15.11	0.53	1.27	9.27	12.00	13.34	16.00	0.63
16.51	16.51	44	17.65	17.65	0.53	1.27	14.35	14.35	18.42	18.42	0.63
19.05	19.05	52	20.19	20.19	0.53	1.27	16.89	16.89	20.96	20.96	0.63
24.13	24.13	68	25.27	25.27	0.53	1.27	21.97	21.97	26.04	26.04	0.63
29.21	29.21	84	30.35	30.35	0.53	1.27	27.05	27.05	31.12	31.12	0.63

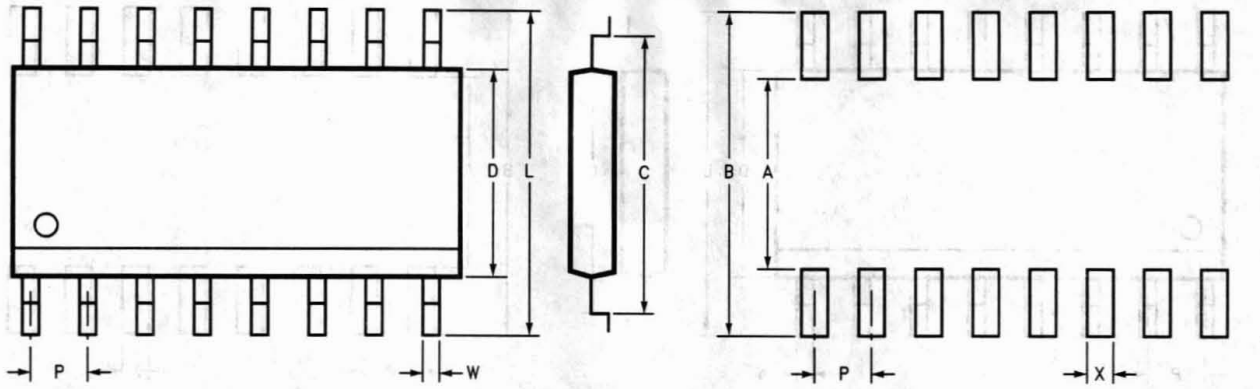
Plastic Quad Flat Packages (PQFP)



TL/P/11811–2

D Body Size (mm)	D' Body Size (mm)	Lead Count No.	L Lead Tip to Tip (mm)	L' Lead Tip to Tip (mm)	W Lead Width (mm)	P Lead/Pad Pitch (mm)	A Inner Pad to Pad Edge (mm)	A' Inner Pad to Pad Edge (mm)	B Outer Pad to Pad Edge (mm)	B' Outer Pad to Pad Edge (mm)	X Land Width (mm)
7	7	40	9.29	9.29	0.26	0.50	7.50	7.50	9.78	9.78	0.30
7	7	48	9.40	9.40	0.27	0.50	6.88	6.90	10.42	10.40	0.32
10	10	44	13.35	13.35	0.45	0.80	10.53	10.53	14.47	14.47	0.55
10	10	52	14.15	14.15	0.38	0.65	9.08	9.08	15.17	15.17	0.43
12	12	64	14.00	14.00	0.38	0.65	11.48	11.48	15.02	15.02	0.43
14	14	80	18.15	18.15	0.38	0.65	13.08	13.08	19.17	19.17	0.43
14	20	80	17.80	23.80	0.35	0.80	13.50	19.50	18.50	24.50	0.40
14	14	100	17.45	17.45	0.30	0.50	13.08	13.08	18.47	18.47	0.35
14	20	100	17.80	23.80	0.30	0.65	13.50	19.50	18.50	24.50	0.35
20	20	100	24.30	18.30	0.40	0.65	21.28	15.28	25.32	19.32	0.45
24	24	132	24.21	24.21	0.30	0.64	21.67	21.67	25.23	25.23	0.40
28	28	120	32.15	32.15	0.45	0.80	27.88	27.88	33.17	33.17	0.55
28	28	128	31.45	31.45	0.45	0.80	28.03	28.03	32.47	32.47	0.55
28	28	144	32.15	32.15	0.38	0.65	28.03	28.03	33.17	33.17	0.43
28	28	160	32.40	32.40	0.38	0.65	29.48	29.48	33.42	33.42	0.43
28	28	208	30.60	30.60	0.30	0.50	28.08	28.08	31.62	31.62	0.35

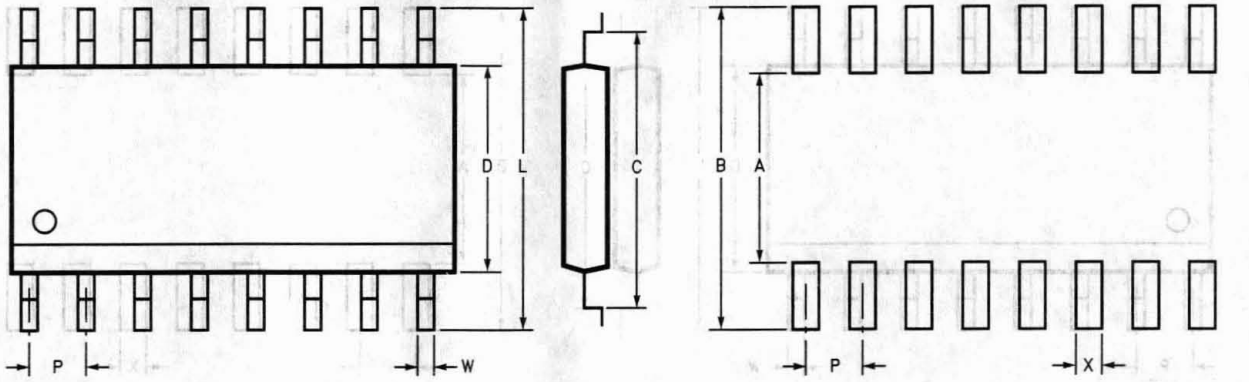
JEDEC Small Outline and Shrink Small Outline Packages (SOP and SSOP)



TL/P/11811–3

D Body Size (in)	Lead Count No.	C Shoulder to Shoulder (in)	L Lead Tip to Tip (in)	W Lead Width (in)	P Lead/Pad Pitch (in)	A Inner Pad to Pad Edge (in)	B Outer Pad to Pad Edge (in)	X Pad Width (in)
SOP								
0.150	8	0.144	0.244	0.020	0.050	0.094	0.294	0.028
0.150	14	0.144	0.244	0.020	0.050	0.094	0.294	0.028
0.150	16	0.144	0.244	0.020	0.050	0.094	0.294	0.028
0.300	14	0.3300	0.4100	0.0190	0.0500	0.2800	0.4600	0.0270
0.300	16	0.3300	0.4100	0.0190	0.0500	0.2800	0.4600	0.0270
0.300	20	0.3300	0.4100	0.0190	0.0500	0.2800	0.4600	0.0270
0.300	24	0.3300	0.4100	0.0190	0.0500	0.2800	0.4600	0.0270
0.300	28	0.3300	0.4100	0.0190	0.0500	0.2800	0.4600	0.0270
SSOP								
0.150	20	0.185	0.241	0.010	0.025	0.145	0.281	0.014
0.150	24	0.185	0.241	0.010	0.025	0.145	0.281	0.014
0.300	48	0.340	0.420	0.012	0.025	0.300	0.460	0.016
0.300	56	0.340	0.420	0.012	0.025	0.300	0.460	0.016

EIAJ Small Outline, Shrink Small Outline, and Thin Small Outline Packages (SOP, SSOP and TSOP)



TL/P/11811–4

D Body Size (mm)	Lead Count No.	C Shoulder to Shoulder (mm)	L Lead Tip to Tip (mm)	W Lead Width (mm)	P Lead/Pad Pitch (mm)	A Inner Pad to Pad Edge (mm)	B Outer Pad to Pad Edge (mm)	X Pad Width (mm)
SOP TYPE II								
5.300	14	6.280	8.000	0.400	1.270	5.010	9.270	0.600
5.300	16	6.280	8.000	0.400	1.270	5.010	9.270	0.600
5.300	20	6.280	8.000	0.400	1.270	5.010	9.270	0.600
SSOP TYPE II								
5.300	20	6.600	8.100	0.400	0.650	5.584	9.116	0.451
5.300	24	6.600	8.100	0.400	0.650	5.584	9.116	0.451
SSOP TYPE III								
7.500	40	8.900	10.500	0.350	0.650	7.884	11.516	0.452
TSOP TYPE I								
18.500	32	19.000	20.200	0.250	0.500	17.984	21.216	0.301

Section 6

Appendices/ Physical Dimensions

Section 6 Contents

Appendix A General Product Marking and Code Explanation 6-3
Appendix B Device/Application Literature Cross-Reference 6-4
Appendix C Summary of Commercial Reliability Programs 6-10
Appendix D Military Aerospace Programs from National Semiconductor 6-11
Appendix E Understanding Integrated Circuit Package Power Capabilities 6-21
Appendix F How to Get the Right Information from a Datasheet 6-26
Physical Dimensions 6-30
Bookshelf
Distributors

National Semiconductor

Appendix A
General Product Marking & Code Explanation

LF 356 N /A+

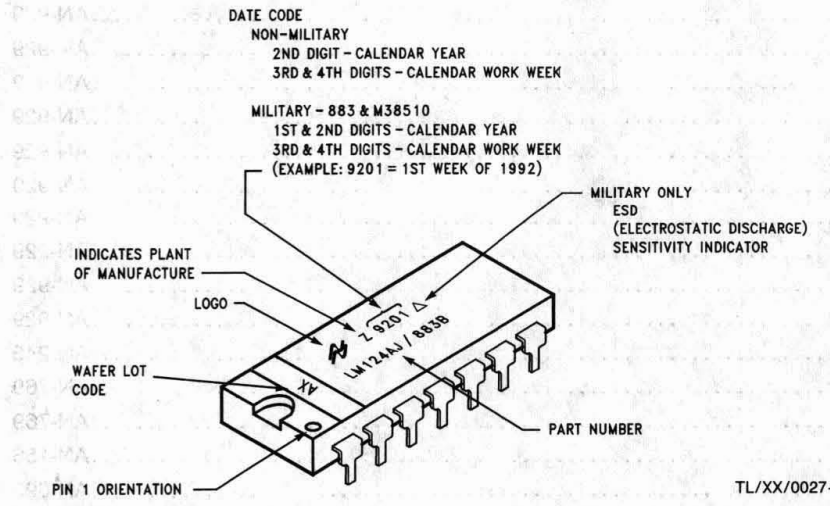
- /A+ — Reliability Program (Optional) (Refer to Appendix C)
- N — Package Type (See Right)
- 356 — Device Number (Generic Type) and Suffix Letter (Optional)
  - A or B: Improved Electrical Specification
  - C, I, E or M: Temperature Range
- LF — Device Family (See Below)

Device Family

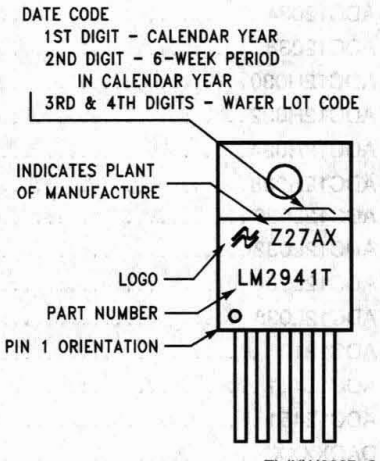
ADC	Data Conversion
AF	Active Filter
AH	Analog Switch (Hybrid)
DAC	Data Conversion
DM	Digital (Monolithic)
HS	Hybrid
LF	Linear (BI-FET™)
LH	Linear (Hybrid)
LM	Linear (Monolithic)
LMC	Linear CMOS
LMD	Linear DMOS
LP	Linear (Low Power)
LPC	Linear CMOS (Low Power)
MF	Linear (Monolithic Filter)
LMF	Linear Monolithic Filter

Package Type

D	Glass/Metal DIP
E	Ceramic Leadless Chip Carrier (LCC)
F	Glass/Metal Flat Pak (¼" x ¼")
G	12 Lead TO-8 Metal Can (M/C)
H	Multi-Lead Metal Can (M/C)
H-05	4 Lead M/C (TO-5) } Shipped with
H-46	4 Lead M/C (TO-46) } Thermal Shield
J	Lo-Temp Ceramic DIP
J-8	8 Lead Ceramic DIP ("MiniDIP")
J-14	14 Lead Ceramic DIP (-14 used only when product is also available in -8 pkg).
K	TO-3 M/C in Steel, except LM309K which is shipped in Aluminum
KC	TO-3 M/C (Aluminum)
K Steel	TO-3 M/C (Steel)
M	Small Outline Package
M3	3-Lead Small Outline Package
M5	5-Lead Small Outline Package
N	Molded DIP (EPOXY B)
N-01	Molded DIP (Epoxy B) with Staggered Leads
N-8	8 Lead Molded DIP (Epoxy B) ("Mini-DIP")
N-14	14 Lead Molded DIP (Epoxy B) (-14 used only when product is also available in -8 pkg).
P	3 Lead TO-202 Power Pkg
Q	Cerdip with UV Window
S	3,5,11, & 15 Lead TO-263 Surf. Mt. Power Pkg
T	3,5,11,15 & 23 Lead TO-220 PWR Pkg (Epoxy B)
V	Multi-lead Plastic Chip Carrier (PCC)
W	Lo-Temp Ceramic Flat Pak
WM	Wide Body Small Outline Package



TL/XX/0027-2



TL/XX/0027-3

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National Semiconductor

Appendix B
Device/Application Literature Cross-Reference

Device Number	Application Literature
ADCXXXX	AN-156
ADC80	AN-360
ADC0801	AN-233, AN-271, AN-274, AN-280, AN-281, AN-294, LB-53
ADC0802	AN-233, AN-274, AN-280, AN-281, LB-53
ADC0803	AN-233, AN-274, AN-280, AN-281, LB-53
ADC08031	AN-460
ADC0804	AN-233, AN-274, AN-276, AN-280, AN-281, AN-301, AN-460, LB-53
ADC0805	AN-233, AN-274, AN-280, AN-281, LB-53
ADC0808	AN-247, AN-280, AN-281
ADC0809	AN-247, AN-280
ADC0816	AN-193, AN-247, AN-258, AN-280
ADC0817	AN-247, AN-258, AN-280
ADC0820	AN-237
ADC0831	AN-280, AN-281
ADC0832	AN-280, AN-281
ADC0833	AN-280, AN-281
ADC0834	AN-280, AN-281
ADC0838	AN-280, AN-281
ADC1001	AN-276, AN-280, AN-281
ADC1005	AN-280
ADC10461	AN-769
ADC10462	AN-769
ADC10464	AN-769
ADC10662	AN-769
ADC10664	AN-769
ADC12030	AN-929
ADC12032	AN-929
ADC12034	AN-929
ADC12038	AN-929
ADC12H030	AN-929
ADC12H032	AN-929
ADC12H034	AN-929
ADC12H038	AN-929
ADC12L030	AN-929
ADC12L032	AN-929
ADC12L034	AN-929
ADC12L038	AN-929
ADC1210	AN-245
ADC12441	AN-769
ADC12451	AN-769
DACXXXX	AN-156
DAC0800	AN-693
DAC0830	AN-284

Device/Application Literature Cross-Reference (Continued)

Device Number	Application Literature
DAC0831	AN-271, AN-284
DAC0832	AN-271, AN-284
DAC1006	AN-271, AN-275, AN-277, AN-284
DAC1007	AN-271, AN-275, AN-277, AN-284
DAC1008	AN-271, AN-275, AN-277, AN-284
DAC1020	AN-263, AN-269, AN-2293, AN-294, AN-299
DAC1021	AN-269
DAC1022	AN-269
DAC1208	AN-271, AN-284
DAC1209	AN-271, AN-284
DAC1210	AN-271, AN-284
DAC1218	AN-293
DAC1219	AN-693
DAC1220	AN-253, AN-269
DAC1221	AN-269
DAC1222	AN-269
DAC1230	AN-284
DAC1231	AN-271, AN-284
DAC1232	AN-271, AN-284
DAC1280	AN-261, AN-263
DH0034	AN-253
DH0035	AN-49
INS8070	AN-260
LF111	LB-39
LF155	AN-263, AN-447
LF198	AN-245, AN-294
LF311	AN-301
LF347	AN-256, AN-262, AN-263, AN-265, AN-266, AN-301, AN-344, AN-447, LB-44
LF351	AN-242, AN-263, AN-266, AN-271, AN-275, AN-293, AN-447, Appendix C
LF351A	AN-240
LF351B	Appendix D
LF353	AN-256, AN-258, AN-262, AN-263, AN-266, AN-271, AN-285, AN-293, AN-447, LB-44, Appendix D
LF356	AN-253, AN-258, AN-260, AN-263, AN-266, AN-271, AN-272, AN-275, AN-293, AN-294, AN-295, AN-301, AN-447, AN-693
LF357	AN-263, AN-447, LB-42
LF398	AN-247, AN-258, AN-266, AN-294, AN-298, LB-45
LF411	AN-294, AN-301, AN-344, AN-447
LF412	AN-272, AN-299, AN-301, AN-344, AN-447
LF441	AN-301, AN-447
LF13006	AN-344
LF13007	AN-344
LF13331	AN-294, AN-447
LH0002	AN-13, AN-227, AN-263, AN-272, AN-301
LH0024	AN-253
LH0032	AN-242, AN-253
LH0033	AN-48, AN-227, AN-253
LH0063	AN-227
LH0070	AN-301
LH0071	AN-245
LH0094	AN-301
LH0101	AN-261

Device/Application Literature Cross-Reference (Continued)

Device Number	Application Literature
LH1605	AN-343
LH2424	AN-867
LM10	AN-211, AN-247, AN-258, AN-271, AN-288, AN-299, AN-300, AN-460, AN-693
LM11	AN-241, AN-242, AN-260, AN-266, AN-271
LM12	AN-446, AN-693, AN-706
LM101	AN-4, AN-13, AN-20, AN-24, LB-42, Appendix A
LM101A	AN-29, AN-30, AN-31, AN-79, AN-241 AN-711, LB-1, LB-2, LB-4, LB-8, LB-14, LB-16, LB-19, LB-28
LM102	AN-4, AN-13, AN-30, LB-1, LB-5, LB-6, LB-11
LM103	AN-110, LB-41
LM105	AN-23, AN-110, LB-3
LM106	AN-41, LB-6, LB-12
LM107	AN-20, AN-31, LB-1, LB-12, LB-19, Appendix A
LM108	AN-29, AN-30, AN-31, AN-79, AN-211, AN-241, LB-14, LB-15, LB-21
LM108A	AN-260, LB-15, LB-19
LM109	AN-42, LB-15
LM109A	LB-15
LM110	LB-11, LB-42
LM111	AN-41, AN-103, LB-12, LB-16, LB-32, LB-39
LM112	LB-19
LM113	AN-56, AN-110, LB-21, LB-24, LB-28, LB-37
LM117	AN-178, AN-181, AN-182, LB-46, LB-47
LM117HV	LB-46, LB-47
LM118	LB-17, LB-19, LB-21, LB-23, Appendix A
LM119	LB-23
LM120	AN-182
LM121	AN-79, AN-104, AN-184, AN-260, LB-22
LM121A	LB-32
LM122	AN-97, LB-38
LM125	AN-82
LM126	AN-82
LM129	AN-173, AN-178, AN-262, AN-266
LM131	AN-210, AN-460, Appendix D
LM131A	AN-210
LM134	LB-41, AN-460
LM135	AN-225, AN-262, AN-292, AN-298, AN-460
LM137	LB-46
LM137HV	LB-46
LM138	LB-46
LM139	AN-74
LM143	AN-127, AN-271
LM148	AN-260
LM150	LB-46
LM158	AN-116
LM160	AN-87
LM161	AN-87, AN-266
LM163	AN-295
LM194	AN-222, LB-21
LM195	AN-110
LM199	AN-161, AN-260
LM199A	AN-161
LM211	LB-39

Device/Application Literature Cross-Reference (Continued)

Device Number	Application Literature
LM231	AN-210
LM231A	AN-210
LM235	AN-225
LM239	AN-74
LM258	AN-116
LM260	AN-87
LM261	AN-87
LM34	AN-460
LM35	AN-460
LM301A	AN-178, AN-181, AN-222
LM308	AN-88, AN-184, AN-272, LB-22, LB-28, Appendix D
LM308A	AN-225, LB-24
LM309	AN-178, AN-182
LM311	AN-41, AN-103, AN-260, AN-263, AN-288, AN-294, AN-295, AN-307, LB-12, LB-16, LB-18, LB-39
LM313	AN-263
LM316	AN-258
LM317	AN-178, LB-35, LB-46
LM317H	LB-47
LM318	AN-299, LB-21
LM319	AN-828, AN-271, AN-293
LM320	AN-288
LM321	LB-24
LM324	AN-88, AN-258, AN-274, AN-284, AN-301, LB-44, AB-25, Appendix C
LM329	AN-256, AN-263, AN-284, AN-295, AN-301
LM329B	AN-225
LM330	AN-301
LM331	AN-210, AN-240, AN-265, AN-278, AN-285, AN-311, LB-45, Appendix C, Appendix D
LM331A	AN-210, Appendix C
LM334	AN-242, AN-256, AN-284
LM335	AN-225, AN-263, AN-295
LM336	AN-202, AN-247, AN-258
LM337	LB-46
LM338	LB-49, LB-51
LM339	AN-74, AN-245, AN-274
LM340	AN-103, AN-182
LM340L	AN-256
LM342	AN-288
LM346	AN-202, LB-54
LM348	AN-202, LB-42
LM349	LB-42
LM358	AN-116, AN-247, AN-271, AN-274, AN-284, AN-298, Appendix C
LM358A	Appendix D
LM359	AN-278, AB-24
LM360	AN-87
LM361	AN-87, AN-294
LM363	AN-271
LM380	AN-69, AN-146
LM385	AN-242, AN-256, AN-301, AN-344, AN-460, AN-693, AN-777
LM386	LB-54
LM391	AN-272
LM392	AN-274, AN-286

Device/Application Literature Cross-Reference (Continued)

Device Number	Application Literature
LM393	AN-271, AN-274, AN-293, AN-694
LM394	AN-262, AN-263, AN-271, AN-293, AN-299, AN-311, LB-52
LM395	AN-178, AN-181, AN-262, AN-263, AN-266, AN-301, AN-460, LB-28
LM399	AN-184
LM555	AN-694, AB-7
LM556	AB-7
LM565	AN-46, AN-146
LM566	AN-146
LM604	AN-460
LM628	AN-693, AN-706
LM629	AN-693, AN-694, AN-706
LM709	AN-24, AN-30
LM710	AN-41, LB-12
LM725	LB-22
LM741	AN-79, LB-19, LB-22
LM833	AN-346
LM1036	AN-390
LM1202	AN-867
LM1203	AN-861
LM1204	AN-934
LM1458	AN-116
LM1524	AN-272, AN-288, AN-292, AN-293
LM1558	AN-116
LM1578A	AB-30
LM1823	AN-391
LM1830	AB-10
LM1865	AN-390
LM1886	AN-402
LM1889	AN-402
LM1894	AN-384, AN-386, AN-390
LM2419	AN-861
LM2577	AN-776, AN-777
LM2876	AN-898
LM2889	AN-391, AN-402
LM2907	AN-162
LM2917	AN-162
LM2931	AB-12
LM2931CT	AB-11
LM3045	AN-286
LM3046	AN-146, AN-299
LM3089	AN-147
LM3524	AN-272, AN-288, AN-292, AN-293
LM3525A	AN-694
LM3578A	AB-30
LM3875	AN-898
LM3876	AN-898
LM3886	AN-898
LM3900	AN-72, AN-263, AN-274, AN-278, LB-20, AB-24
LM3909	AN-154
LM3914	AN-460, LB-48, AB-25
LM3915	AN-386
LM3999	AN-161

Device/Application Literature Cross-Reference (Continued)

Device Number	Application Literature
LM4250	AN-88, LB-34
LM6181	AN-813, AN-840
LM7800	AN-178
LM12454	AN-906, AN-947, AN-949
LM12458	AN-906, AN-947, AN-949
LM12H454	AN-906, AN-947, AN-949
LM12H458	AN-906, AN-947, AN-949
LM12L458	AN-906, AN-947, AN-949
LM18293	AN-706
LM78L12	AN-146
LM78S40	AN-711
LMC555	AN-460, AN-828
LMC660	AN-856
LMC835	AN-435
LMC6044	AN-856
LMC6062	AN-856
LMC6082	AN-856
LMC6484	AN-856
LMD18200	AN-694, AN-828
LMF40	AN-779
LMF60	AN-779
LMF90	AN-779
LMF100	AN-779
LMF380	AN-779
LMF390	AN-779
LP324	AN-284
LP395	AN-460
LPC660	AN-856
MF4	AN-779
MF5	AN-779
MF6	AN-779
MF8	AN-779
MF10	AN-307, AN-779
MM2716	LB-54
MM54104	AN-252, AN-287, LB-54
MM57110	AN-382
MM74C00	AN-88
MM74C02	AN-88
MM74C04	AN-88
MM74C948	AN-193
MM74HC86	AN-861, AN-867
MM74LS138	LB-54
MM53200	AN-290
2N4339	AN-32

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Appendix C
Summary of Commercial Reliability Programs

P+ Product Enhancement

The P+ product enhancement program involves dynamic tests that screen out assembly related and silicon defects that can lead to infant mortality and/or reduce the survivability of the device under high stress conditions. This program includes but is not limited to the following power devices:

Device	Package Types					
	TO-3 K STEEL	TO-39 (H)	TO-220 (T)	DIP (N)	SO (M)	TO-263 (S)
LM12	X					
LM109/309	X	X				
LM117/317	X	X	X			X
LM117HV/317HV	X	X				
LM120/320	X	X	X			
LM123/323	X					
LM133/333	X		X			
LM137/337	X	X	X			
LM137HV/337HV	X	X				
LM138/338	X		X			
LM140/340	X		X			
LM145/345	X					
LM150/350	X		X			
LM195/395	X	X	X			
LM2930/2935/2984			X			X
LM2937			X			X
LM2940/2941			X			X
LM2990/2991			X			X
LM2575/2575HV			X	X	X	X
LM2576			X			X
LM2577			X	X	X	X
LMD18200/18201			X			

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Appendix D
Military Aerospace Programs from National Semiconductor

This appendix is intended to provide a brief overview of military products available from National Semiconductor. The process flows and catagories shown below are for general reference only. For further information and availability, please contact the Customer Response Center at 1-800-272-9959, Military/Aerospace Marketing group or your local sales office.

National Semiconductor's Military/Aerospace Program is founded on dedication to excellence. National offers complete support across the broadest range of products with the widest selection of qualification levels and screening flows. These flows include:

Process Flows (Integrated Circuits)	Description
JAN S	QML products processed to MIL-I-38535 Level S or V for Space level applications.
JAN B	QML products processed to MIL-I-38535 Level B or Q for Military applications.
SMD	QML products processed to a Standard Microcircuit Drawing with Table I Electricals controlled by DESC.
883	QML products processed to MIL-STD-883 Level B for Military applications.
MLP	Products processed on the Monitored Line (Program) developed by the Air Force for Space level applications.
-MIL	Similar to MIL-STD-883 with exceptions noted on the Certificate of Conformance.
MSP	Military Screening Products for initial release of advanced products.
MCP	Commercial products processed in a military assembly. Electrical testing performed at 25°C, plus minimum and maximum operating temperature to commercial limits.
MCR	Commercial products processed in a military assembly. Electrical testing performed at 25°C to commercial limits
MRP	Military Ruggedized Plastic products processed to avionics requirements.
MRR	Commercial Ruggedized plastic product processed in a commercial assembly with electrical testing at 25°C.
MPC	Commercial plastic products processed in a commercial assembly with electrical testing at 25°C.

- **QML:** The purpose of the QML program, which is administered by the Defense Electronics Supply Center (DESC), is to provide the military community with standardized products that have been manufactured and screened to the highest quality and reliability standards in facilities that have been certified by the government. To achieve QML status, manufacturers must submit their facilities, quality procedures and design philosophies to a thorough audit aimed at confirming their ability to produce product to the highest design and quality standards. They must be listed on DESC's Qualified Manufacturer List (QML) before devices can be marked and shipped as QML product.

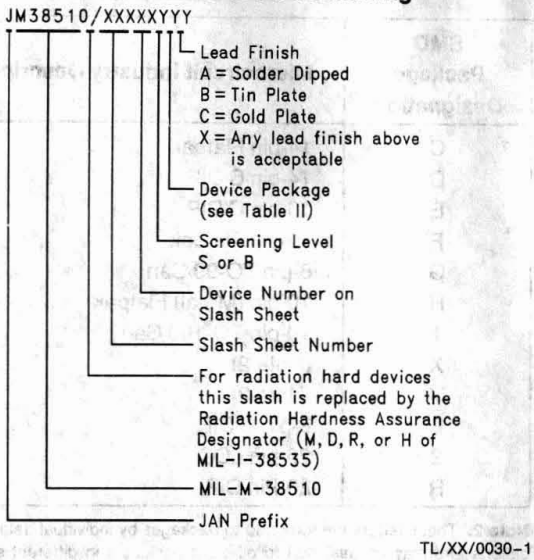
  Two processing levels are specified within MIL-I-38535, the QML standard: Class S (typically specified for space and strategic applications) and Class B (used for tactical missile, airborne, naval and ground systems). The requirements for both classes are defined within MIL-STD-883. National is one of the industry's leading suppliers of both classes.
- **Standard Microcircuit Drawings (SMD).** SMDs are issued to provide standardized versions of devices offered under QML. MIL-STD-883 screening is coupled with tightly controlled electrical test specifications that allow a manufacturer to use his standard electrical tests. Table I explains the marking of JAN devices, and Table II outlines current marking requirements for QML/SMD devices. Copies of MIL-I-38535 and the QML can be obtained from the Naval Publications and Forms Center (5801 Tabor Avenue, Philadelphia, PA 19120, 212/697-2179. A current listing of National's SMD offerings can be obtained from our authorized distributors, our sales offices, our Customer Response Center (Arlington, Texas, 817/468-6300), or from DESC.
- **MIL-STD-883.** Originally intended to establish uniform test methods and procedures, MIL-STD-883 has also become the general specification for non-SMD military product. MIL-STD-883 defines the minimum requirements for a device to be marked and advertised as 883-compliant. Design and construction criteria, documentation controls, electrical and mechanical screening requirements, and quality control procedures are outlined in paragraph 1.1.2 of MIL-STD-883.

  National offers both 883 Class B and 883 Class S product. The screening requirements for both classes of product are outlined in Table III.

  As with SMDs a manufacturer is allowed to use his standard electrical tests provided that all critical parameters are tested. Also, the electrical test parameters, test conditions, test limits and test temperatures must be clearly documented. At National Semiconductor, this information is available via our Table I (formerly RETS, Reliability Electrical Test Specification Program). The Table I document is a complete description of the electrical tests performed and is controlled by our QA department. Individual copies are available upon request.

  Some of National's products are produced on a flow similar to MIL-STD-883. These devices are screened to the same stringent requirements as 883 product, but are marked as **-MIL**; specific reasons for prevention of compliancy are clearly defined in the Certificate of Conformance (C of C) shipped with the product.
- **Monitored Line Program (MLP):** is a non JAN Level S program developed by the Air Force. Monitored Line product usually provides the shortest cycle time, and is acceptable for application in several space level programs. Lockheed Missiles and Space Company in Sunnyvale, California, under an Air Force contract, provides "on-site" monitoring of product processing, and as appropriate, program management. Monitored Line orders generally do not allow "customizing", and most flows do not include quality conformance inspection. Drawing control is maintained by the Lockheed Company.
- **Military Screening Program (MSP):** National's Military Screening Program was developed to make screened versions of advanced products such as gate arrays and microprocessors available more quickly. Through this program, screened product is made available for prototypes and breadboards prior to or during the QML activities. MSP products receive the 100% screening of Table III, but are not subjected to Group C and D quality conformance testing. Other criteria such as electrical testing and temperature range will vary depending upon individual device status and capability.

TABLE I. JAN S or B Part Marking


JM38510/XXXXXYYY
Lead Finish
A = Solder Dipped
B = Tin Plate
C = Gold Plate
X = Any lead finish above is acceptable
Device Package (see Table II)
Screening Level S or B
Device Number on Slash Sheet
Slash Sheet Number
For radiation hard devices this slash is replaced by the Radiation Hardness Assurance Designator (M, D, R, or H of MIL-I-38535)
MIL-M-38510
JAN Prefix

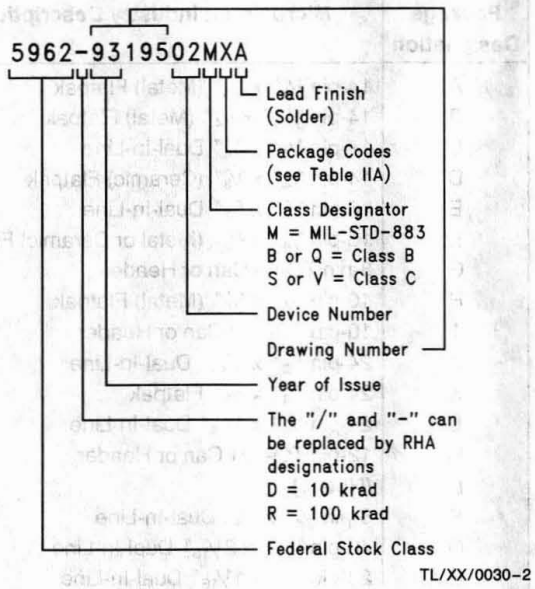
TL/XX/0030–1

TABLE I-A. JAN Package Codes

JAN Package Designation	Microcircuit Industry Description
A	14-pin 1/4" x 1/4" (Metal) Flatpak
B	14-pin 3/16" x 1/4" (Metal) Flatpak
C	14-pin 1/4" x 3/4" Dual-In-Line
D	14-pin 1/4" x 3/8" (Ceramic) Flatpak
E	16-pin 1/4" x 7/8" Dual-In-Line
F	16-pin 1/4" x 3/8" (Metal or Ceramic) Flatpak
G	8-pin TO-99 Can or Header
H	10-pin 1/4" x 1/4" (Metal) Flatpak
I	10-pin TO-100 Can or Header
J	24-pin 1/2" x 1 1/4" Dual-In-Line
K	24-pin 3/8" x 5/8" Flatpak
L	24-pin 1/4" x 1 1/4" Dual-In-Line
M	12-pin TO-101 Can or Header
N	(Note 1)
P	8-pin 1/4" x 3/8" Dual-In-Line
Q	40-pin 3/16" x 2 1/16" Dual-In-Line
R	20-pin 1/4" x 1 1/16" Dual-In-Line
S	20-pin 1/4" x 1/2" Flatpak
T	(Note 1)
U	(Note 1)
V	18-pin 3/8" x 15/16" Dual-In-Line
W	22-pin 3/8" x 1 1/8" Dual-In-Line
X	(Note 1)
Y	(Note 1)
Z	(Note 1)
2	20-terminal 0.350" x 0.350" Chip Carrier
3	28-terminal 0.450" x 0.450" Chip Carrier

Note 1: These letters are assigned to packages by individual detail specifications and may be assigned to different packages in different specifications.

TABLE II. Standard Military Drawing (SMD) Marking



TL/XX/0030–2

TABLE II-A. SMD Package Codes

SMD Package Designation	Microcircuit Industry Description
C	14-pin Flatpak
D	14-pin C DIP
E	16-pin C DIP
F	16-pin Flatpak
G	8-pin TO-99 Can
H	10-pin (Metal) Flatpak
I	10-pin TO-100 Can
X	(Note 2)
Y	(Note 2)
P	8-pin C DIP
2	20-pin LCC
R	20-Pin DIP

Note 2: These letters are assigned to packages by individual detail specifications and may be assigned to different packages in different specifications.

TABLE III. 100% Screening Requirements

	Screen	Class S		Class B	
		Method	Reqmt	Method	Reqmt
1.	Wafer Lot Acceptance	5007	All Lots		
2.	Nondestructive Bond Pull (Note 14)	2023	100%		
3.	Internal Visual (Note 1)	2020, Condition A	100%	2010, Condition B	100%
4.	Stabilization Bake (Note 16)	1008, Condition C, Min 24 Hrs. Min	100%	1008, Condition C, Min 24 Hrs. Min	100%
5.	Temperature Cycling (Note 2)	1010, Condition C	100%	1010, Condition C	100%
6.	Constant Acceleration	2001, Condition E Min Y_1 Orientation Only	100%	2001, Condition E Min Y_1 Orientation Only	100%
7.	Visual Inspection (Note 3)		100%		100%
8.	Particle Impact Noise Detection (PIND)	2010, Condition A (Note 4)	100%		
9.	Serialization	(Note 5)	100%		
10.	Interim (Pre-Burn-In) Electrical Parameters	Per Applicable Device Specification (Note 13)	100%	Per Applicable Device Specification (Note 6)	
11.	Burn-In Test	1015 240 Hrs. @ 125°C Min (Cond. F Not Allowed)	100%	1015 160 Hrs. @ 125°C Min	100%
12.	Interim (Post Burn-In) Electrical Parameters	Per Applicable Device Specification (Note 3)	100%		

TABLE III. 100% Screening Requirements (Continued)

	Screen	Class S		Class B	
		Method	Reqmt	Method	Reqmt
13.	Reverse Bias Burn-In (Note 7)	1015; Test Condition A, C, 72 Hrs. @ 150°C Min (Cond. F Not Allowed)	100%		
14.	Interim (Post-Burn-In) Electrical Parameters	Per Applicable Device Specification (Note 13)	100%	Per Applicable Device Specification	100%
15.	PDA Calculation	5% Parametric (Note 14), 3% Functional	All Lots	5% Parametric (Note 14)	All Lots
16.	Final Electrical Test (Note 15) a) Static Tests	Per Applicable Device Specification		Per Applicable Device Specification	
	1) 25°C (Subgroup 1, Table I, 5005)		100%		100%
	2) Max & Min Rated Operating Temp. (Subgroups 2, 3, Table I, 5005)		100%		100%
	b) Dynamic Tests or Functional Tests				
	1) 25°C (Subgroup 4 or 7)		100%		100%
	2) Max and Min Rated Operating Temp. (Subgroups 5 and 6 or 8, Table I, 5005)		100%		100%
	c) Switching Tests 25°C (Subgroup 9, Table I, 5005)		100%		100%
17.	Seal Fine, Gross	1014	100% (Note 8)	1014	100% (Note 9)
18.	Radiographic (Note 10)	2012 Two Views	100%		
19.	Qualification or Quality Conformance Inspection Test Sample Selection	(Note 11)	Samp.	(Note 11)	Samp.
20.	External Visual (Note 12)	2009	100%		100%

Note 1: Unless otherwise specified, at the manufacturer's option, test samples for Group B, bond strength (Method 5005) may be randomly selected prior to or following internal visual (Method 5004), prior to sealing provided all other specification requirements are satisfied (e.g., bond strength requirements shall apply to each inspection lot, bond failures shall be counted even if the bond would have failed internal visual).

Note 2: For Class B devices, this test may be replaced with thermal shock Method 1011, Test Condition A, minimum.

Note 3: At the manufacturer's option, visual inspection for catastrophic failures may be conducted after each of the thermal/mechanical screens, after the sequence or after seal test. Catastrophic failures are defined as missing leads, broken packages, or lids off.

Note 4: The PIND test may be performed in any sequence after step 6 and prior to step 16. See MIL-I-38585 paragraph 40.6.3.

Note 5: Class S devices shall be serialized prior to interim electrical parameter measurements.

Note 6: When specified, all devices shall be tested for those parameters requiring delta calculations.

Note 7: Reverse bias burn-in is a requirement only when specified in the applicable device specification. The order of performing burn-in and reverse bias burn-in may be inverted.

Note 8: For Class S devices, the seal test may be performed in any sequence between step 16 and step 19, but it shall be performed after all shearing and forming operations on the terminals.

Note 9: For Class B devices, the fine and gross seal tests shall be performed separately or together in any sequence and order between step 6 and step 20 except that they shall be performed after all shearing and forming operations on the terminals. When 100% seal screen cannot be performed after shearing and forming (e.g., flatpaks and chip carriers) the seal screen shall be done 100% prior to these operations and a sample test (LTPD = 5) shall be performed on each inspection lot following these operations. If the sample fails, 100% rescreening shall be required.

Note 10: The radiographic screen may be performed in any sequence after step 9.

Note 11: Samples shall be selected for testing in accordance with the specific device class and lot requirements of Method 5005.

Note 12: External Visual shall be performed on the lot any time after step 19 and prior to shipment.

Note 13: Read and record is required at steps 10 and 12 only for those parameters for which post-burn-in delta measurements are specified. All parameters shall be read and recorded at step 14.

Note 14: The PDA shall apply to all subgroup 1 parameters at 25°C and all delta parameters.

Note 15: Only one view is required for flat packages and leadless chip carriers with leads on all four sides.

Note 16: May be performed at any time prior to step 10.

Military Analog Products Available from National Semiconductor

Device	Package Styles (Note 1)	Description	Process Flows (Note 2)	SMD/JAN (Note 3)
HIGH PERFORMANCE AMPLIFIERS AND BUFFERS				
LF147	D, J	Wide BW Quad JFET Op Amp	SMD/JAN	/11906
LF155A	H	JFET Input Op Amp	883	—
LF156	H	JFET Input Op Amp	883	—
LF156A	H	JFET Input Op Amp	883	—
LF157	H	JFET Input Op Amp	883	—
LF157A	H	JFET Input Op Amp	883	—
LF411M	H	Low Offset, Low Drift JFET Input	883/JAN	/11904
LF412M	H, J	Low Offset, Low Drift JFET Input-Dual	883/JAN	/11905
LF441M	H	Low Power JFET Input	883	—
LF442M	H	Low Power JFET Input-Dual	883	—
LF444M	D	Low Power JFET Input-Quad	883	—
LH0002	H	Buffer Amp	"-MIL"	—
LH0021	K	1.0 Amp Power Op Amp	"-MIL"	—
LH0024	H	High Slew Rate Op Amp	"-MIL"	—
LH0032	G	Ultra Fast FET-Input Op Amp	"-MIL"	—
LH0041	G	0.2 Amp Power Op Amp	"-MIL"	—
LH0101	K	Power Op Amp	"-MIL"	—
LM10	H	Super-Block™ Micropower Op Amp/Ref	883/SMD	5962-87604
LM101A	J, H, W	General Purpose Op Amp	883/JAN	/10103
LM108A	J, H, W	Precision Op Amp	883/JAN	/10104
LM118	J, H	Fast Op Amp	883/JAN	/10107
LM124	J, E, W	Low Power Quad Op Amp	883/JAN	/11005
LM124A	J, E, W	Low Power Quad	883/JAN	/11006
LM146	J	Quad Programmable Op Amp	883	—
LM148	J, E	Quad 741 Op amp	883/JAN	/11001
LM158A	J, H	Low Power Dual Op Amp	883/SMD	5962-8771002
LM158	J, H	Low Power Dual Op Amp	883/SMD	5962-8771001
LM611AM	J	Super-Block Op Amp/Reference	883/SMD	—
LM613AM	J, E	Super-Block Dual Op Amp/Dual Comp/Ref	883/SMD	—
LM614AM	J	Super-Block Quad Op Amp/Ref	883/SMD	—
LM709A	H, J, W	General Purpose Op Amp	883/SMD	7800701
LM741	J, H, W	General Purpose Op Amp	883/JAN	/10101
LM747	J, H	General Purpose Dual Op Amp	883/JAN	/10102
LM6118	J, E	VIP Dual Op Amp	883/SMD	5962-91565
LM6121	H, J	VIP Buffer	883/SMD	5962-90812
LM6125	H	VIP Buffer with Error Flag	883/SMD	5962-90815
LM6161	J, E, W	VIP Op Amp (Unity Gain)	883/SMD	5962-89621
LM6162	J, E, W	VIP Op Amp ($A_V > 2, -1$)	883/SMD	5962-92165
LM6164	J, E, W	VIP Op Amp ($A_V > 5$)	883/SMD	5962-89624
LM6165	J, E, W	VIP Op Amp ($A_V > 25$)	883/SMD	5962-89625
LM6181AM	J	VIP Current Feedback Op Amp	883/SMD	5962-9081802
LM6182AM	J	VIP Current Feedback Dual Op Amp	883/SMD	5962-9460301
LMC660AM	J	Low Power CMOS Quad Op Amp	883/SMD	5962-9209301
LMC662AM	J	Low Power CMOS Dual Op Amp	883/SMD	5962-9209401
LPC660AM	J	Micropower CMOS Quad Op Amp	883/SMD	5962-9209302
LPC662AM	J	Micropower CMOS Dual Op Amp	883/SMD	5962-9209402
LMC6482AM	J	Rail to Rail CMOS Dual Op Amp	883/SMD	5962-9453401
LMC6484AM	J	Rail to Rail CMOS Quad Op Amp	883/SMD	5962-9453402
OP07	H	Precision Op Amp	883	—

Military Analog Products Available from National Semiconductor (Continued)

Device	Package Styles (Note 1)	Description	Process Flows (Note 2)	SMD/JAN (Note 3)
COMPARATORS				
LF111	H	Voltage Comparator	"-MIL"	—
LH2111	J, W	Dual Voltage Comparator	883/JAN	/10305
LM106	H, W	Voltage Comparator	883/SMD	8003701
LM111	J, H, E, W	Voltage Comparator	883/JAN	/10304
LM119	J, H, E, W	High Speed Dual Comparator	883/JAN	/10306
LM139	J, E, W	Quad Comparator	883/JAN	/11201
LM139A	J, E, W	Precision Quad Comparator	883/SMD	5962-87739
LM160	J, H	High Speed Differential Comparator	883/SMD	8767401
LM161	J, H, W	High Speed Differential Comparator	883/SMD	5962-87572
LM193	J, H	Dual Comparator	883	—
LM193A	J, H	Dual Comparator	883/JAN	/11202
LM612AM	J	Dual-Channel Comparator/Reference	883/SMD	5962-93002
LM613AM	J, E	Super-Block Dual Comparator/ Dual Op Amp/Adj Reference	883/SMD	5962-93003
LM615AM	J	Quad Comparator/Adjustable Reference	883	—
LM710A*	J, H, W	Voltage Comparator	883/JAN	/10301
LM711A*	J, H, W	Dual LM710	883/JAN	/10302
LM760	J, H	High Speed Differential Comparator	883/SMD	5962-87545

*Formerly manufactured by Fairchild Semiconductor as part numbers μA710 and μA711.

LINEAR REGULATORS				
Positive Voltage Regulators				
LM105	H	Adjustable Voltage Regulator	883/SMD	5962-89588
LM109	H	5V Regulator, I_O = 20 mA	883/JAN	/10701BXA
LM109	K	5V Regulator, I_O = 1A	883/JAN	/10701BYA
LM117	H, E, K	Adjustable Regulator	883/JAN	/11703, /11704
LM117HV	H	Adjustable Regulator, I_O = 0.5A	883/SMD	7703402XA
LM117HV	K	Adjustable Regulator, I_O = 1.5A	883/SMD	7703402YA
LM123	K	3A Voltage Regulator	883	—
LM138	K	5A Adjustable Regulator	"-MIL"	—
LM140-5.0	H	0.5A Fixed 5V Regulator	883/JAN	/10702
LM140-6.0	H	0.5A Fixed 6V Regulator	883	—
LM140-8.0	H	0.5A Fixed 8V Regulator	883	—
LM140-12	H	0.5A Fixed 12V Regulator	883/JAN	/10703
LM140-15	H	0.5A Fixed 15V Regulator	883/JAN	/10704
LM140-24	H	0.5A Fixed 24V Regulator	883	—
LM140A-5.0	K	1.0A Fixed 5V Regulator	883	—
LM140A-12	K	1.0A Fixed 12V Regulator	883	—
LM140A-15	K	1.0A Fixed 15V Regulator	883	—
LM140K-5.0	K	1.0A Fixed 5V Regulator	883/JAN	/10706
LM140K-12	K	1.0A Fixed 12V Regulator	883/JAN	/10707
LM140K-15	K	1.0A Fixed 15V Regulator	883/JAN	/10708
LM140LAH-5.0	H	100 mA Fixed 5V Regulator	883	—
LM140LAH-12	H	100 mA Fixed 12V Regulator	883	—
LM140LAH-15	H	100 mA Fixed 15V Regulator	883	—
LM150	K	3A Adjustable Power Regulator	883	—
LM2940-5.0	K	5V Low Dropout Regulator	883/SMD	5962-89587
LM2940-8.0	K	8V Low Dropout Regulator	883/SMD	5962-90883
LM2940-12	K	12V Low Dropout Regulator	883/SMD	5962-90884
LM2940-15	K	15V Low Dropout Regulator	883/SMD	5962-90885
LM2941	K	Adjustable Low Dropout Regulator	883/SMD	TBD
LM431	H, K	Adjustable Shunt Regulator	883	—
LM723	H, J, E	Precision Adjustable Regulator	883/JAN	/10201
LP2951	H, E, J	Adjustable Micropower LDO	883/SMD	5962-38705
LP2953AM	J	250 mA Adj. Micropower LDO	883/SMD	5962-9233601

Military Analog Products Available from National Semiconductor (Continued)

Device	Package Styles (Note 1)	Description	Process Flows (Note 2)	SMD/JAN (Note 3)
LINEAR REGULATORS (Continued)				
Negative Voltage Regulators				
LM120-5.0	H	Fixed 0.5A Regulator, $V_{OUT} = -5V$	883/JAN	/11501
LM120-8.0	H	Fixed 0.5A Regulator, $V_{OUT} = -8V$	883	—
LM120-12	H	Fixed 0.5A Regulator, $V_{OUT} = -12V$	883/JAN	/11502
LM120-15	H	Fixed 0.5A Regulator, $V_{OUT} = -15V$	883/JAN	/11503
LM120-5.0	K	Fixed 1.0A Regulator, $V_{OUT} = -5V$	883/JAN	/11505
LM120-12	K	Fixed 1.0A Regulator, $V_{OUT} = -12V$	883/JAN	/11506
LM120-15	K	Fixed 1.0A Regulator, $V_{OUT} = -15V$	883/JAN	/11507
LM137A	H	Precision Adjustable Regulator	883/SMD	7703406XA
LM137A	K	Precision Adjustable Regulator	883/SMD	7703406YA
LM137	H, K	Adjustable Regulator	883/JAN	/11803, /11804
LM137HV	H	Adjustable (High Voltage) Regulator	883/SMD	7703404XA
LM137HV	K	Adjustable (High Voltage) Regulator	883/SMD	7703404YA
LM145-5.0	K	Negative 3 Amp Regulator	883/SMD	5962-90645
LM145-5.2	K	Negative 3 Amp Regulator	883	—
SWITCHING REGULATORS				
LM1575-5	J, K	Simple Switcher™ Step-Down, $V_{OUT} = 5V$	883/SMD	5962-9167201
LM1575-12	J, K	Simple Switcher Step-Down, $V_{OUT} = 12V$	883/SMD	5962-9167301
LM1575-15	J, K	Simple Switcher Step-Down, $V_{OUT} = 15V$	883/SMD	5962-9167401
LM1575-ADJ	J, K	Simple Switcher Step-Down, Adj V_{OUT}	883/SMD	5962-9167101
LM1575HV-5	K	Simple Switcher Step-Down, $V_{OUT} = 5V$	883	—
LM1575HV-12	K	Simple Switcher Step-Down, $V_{OUT} = 12V$	883	—
LM1575HV-15	K	Simple Switcher Step-Down, $V_{OUT} = 15V$	883	—
LM1575HV-ADJ	K	Simple Switcher Step-Down, Adj V_{OUT}	883	—
LM1577-12	K	Simple Switcher Step-Up, $V_{OUT} = 12V$	883/SMD	5962-9216701
LM1577-15	K	Simple Switcher Step-Up, $V_{OUT} = 15V$	883/SMD	5962-9216801
LM1577-ADJ	K	Simple Switcher Step-Up, Adj V_{OUT}	883/SMD	5962-9216601
LM1578	H	750 mA Switching Regulator	883/SMD	5962-89586
LM78S40*	J	Universal Switching Regulator Subsystem	883/SMD	5962-88761
VOLTAGE REFERENCES				
LM103-3.0	H	Reference Diode, BV = 3.0V	883/SMD	7702806
LM103-3.3	H	Reference Diode, BV = 3.3V	883/SMD	7702807
LM103-3.6	H	Reference Diode, BV = 3.6V	883/SMD	7702808
LM103-3.9	H	Reference Diode, BV = 3.9V	883/SMD	7702809
LM113	H	Reference Diode with 5% Tolerance	883/SMD	5962-8671101
LM113-1	H	Reference Diode with 1% Tolerance	883/SMD	5962-8671102
LM113-2	H	Reference Diode with 2% Tolerance	883/SMD	5962-8671103
LM129A	H	Precision Reference, 10 ppm/°C Drift	883/SMD	5962-8992101XA
LM129B	H	Precision Reference, 20 ppm/°C Drift	883/SMD	5962-8992102XA
LM136A-2.5	H	2.5V Reference Diode, 1% V_{OUT} Tolerance	883	—
LM136A-5.0	H	5V Reference Diode, 1% V_{OUT} Tolerance	883/SMD	8418001
LM136-2.5	H	2.5V Reference Diode, 2% V_{OUT} Tolerance	883	—
LM136-5.0	H	5V Reference Diode, 2% V_{OUT} Tolerance	883	—

*Formerly manufactured by Fairchild Semiconductor as the μA78S40DMQB.

Military Analog Products Available from National Semiconductor (Continued)

Device	Package Styles (Note 1)	Description	Process Flows (Note 2)	SMD/JAN (Note 3)
VOLTAGE REFERENCES (Continued)				
LM169	H	10V Precision Reference, Low Tempco 0.05% Tolerance	883	—
LM185B	H, E	Adjustable Micropower Voltage Reference	883/SMD	5962-9041401
LM185BX2.5	H	2.5V Micropower Reference Diode, Ultralow Drift	883/SMD	5962-8759404
LM185BY	H	Adjustable Micropower Voltage Reference	883	—
LM185BY1.2	H	1.2V Micropower Reference Diode, Low Drift	883/SMD	5962-8759405
LM185BY2.5	H	2.5V Micropower Reference Diode, Low Drift	883/SMD	5962-8759406
LM185-1.2	H, E	1.2V Micropower Reference Diode, Low Drift	883/SMD	5962-8759401
LM185-2.5	H, E	2.5V Micropower Reference Diode, Low Drift	883/SMD	5962-8759402
LM199	H	Precision Reference, Low Tempco	883/SMD	5962-8856102
LM199A	H	Precision Reference, Ultralow Tempco	883/SMD	5962-8856101
LM199A-20	H	Precision Reference, Ultralow Tempco	883	—
LM611AM	J	Super-Block Op Amp/Reference	883	—
LM612AM	J	Super-Block Dual-Channel Comparator/Reference	883/SMD	5962-9300201
LM613AM	J, E	Super-Block Dual Op Amp/DualComp/Dual Ref	883/SMD	5962-9300301
LM614AM	J	Super-Block Quad Op Amp/Reference	883/SMD	5962-9300401
LM615AM	J	Super-Block Quad Comparator/Reference	883/SMD	TBD
LH0070-0	H	Precision BCD Buffered Reference	"-MIL"	—
LH0070-1	H	Precision BCD Buffered Reference	"-MIL"	—
LH0070-2	H	Precision BCD Buffered Reference	"-MIL"	—
DATA ACQUISITION				
ADC08020L	J	8-Bit μP-Compatible	883/SMD	5962-90966
ADC0851	J	8-Bit Analog Data Acquisition & Monitoring System	883/SMD	TBD
ADC0858	J	8-Bit Analog Data Acquisition & Monitoring System	883/SMD	TBD
ADC08061CM	J	8-Bit Multistep ADC	883/SMD	TBD
ADC10061CM	J	10-Bit Multistep ADC	883/SMD	TBD
ADC10062CM	J	10-Bit Multistep ADC w/Dual Input Mutiplexer	883/SMD	TBD
ADC10064CM	J	10-Bit Multistep ADC w/Quad Input Multiplexer	883/SMD	TBD
ADC1241CM	J	12-Bit Plus Sign Self-Calibrating with Sample/Hold Function	883/SMD	5962-9157801
ADC12441CM	J	Dynamically-Tested ADC1241	883/SMD	5962-9157802
ADC1251CM	J	12-Bit Plus Sign Self-Calibrating with Sample/Hold Function	883/SMD	5962-9157801
ADC12451CM	J	Dynamically-Tested ADC1251	883/SMD	TBD
DAC0854CM	J	Quad 8-Bit D/A Converter with Read Back	883/SMD	TBD
DAC1054CM	J	Quad 10-Bit D/A Converter with Read Back	883/SMD	TBD
LM12458M	EL, W	12-Bit Data Acquisition System	883/SMD	5962-9319501
LM12H458M	EL, W	12-Bit Data Acquisition System	883/SMD	5962-9319502

Military Analog Products Available from National Semiconductor (Continued)

Device	Package Styles (Note 1)	Description	Process Flows (Note 2)	SMD/JAN (Note 3)
DATA ACQUISITION SUPPORT				
Switched Capacitor Filters				
LMF60CMJ50	J	6th Order Butterworth Lowpass	883/SMD	5962-90967
LMF60CMJ100	J	6th Order Butterworth Lowpass	883/SMD	5962-90967
LMF90CM	J	4th Order Elliptic Notch	883/SMD	5962-90968
LMF100A	J, E	Dual 2nd Order General Purpose	883/SMD	5962-9153301
Sample and Hold				
LF198	H	Monolithic Sample and Hold	SMD/JA	5962-87608 /12501
Motion Control				
LMD18200-2	D	Dual 3A, 55V H-Bridge	883/JAN	5962-9232501

Note 1: D: Side-Brazed DIP
E: Leadless Ceramic Chip Carrier
G: Metal Can (TO-8)
H: Metal Can (TO-39, TO-5, TO-99, TO-100)
J: Ceramic DIP
K: Metal Can (TO-3)
W: Flatpak

Note 2: Process Flows
JAN = JM38510, Level B
SMD = Standard Military Drawing
883 = MIL-STD-883 Rev C
-MIL = Exceptions to 883C noted on Certificate of Conformance

Note 3: Please call your local sales office to determine price and availability of space-level products. All "LM" prefix products in this guide are availble with space-level processing.

National Semiconductor

Appendix E
Understanding Integrated Circuit Package Power Capabilities

INTRODUCTION

The short and long term reliability of National Semiconductor's interface circuits, like any integrated circuit, is very dependent on its environmental condition. Beyond the mechanical/environmental factors, nothing has a greater influence on this reliability than the electrical and thermal stress seen by the integrated circuit. Both of these stress issues are specifically addressed on every interface circuit data sheet, under the headings of Absolute Maximum Ratings and Recommended Operating Conditions.

However, through application calls, it has become clear that electrical stress conditions are generally more understood than the thermal stress conditions. Understanding the importance of electrical stress should never be reduced, but clearly, a higher focus and understanding must be placed on thermal stress. Thermal stress and its application to interface circuits from National Semiconductor is the subject of this application note.

FACTORS AFFECTING DEVICE RELIABILITY

Figure 1 shows the well known "bathtub" curve plotting failure rate versus time. Similar to all system hardware (mechanical or electrical) the reliability of interface integrated circuits conform to this curve. The key issues associated with this curve are infant mortality, failure rate, and useful life.

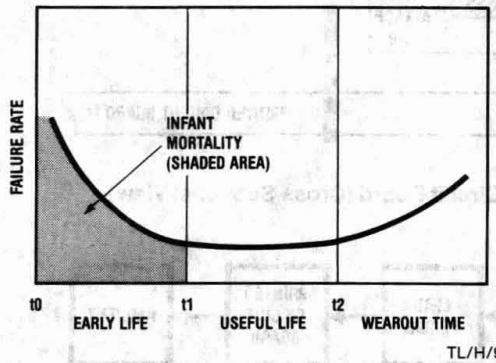


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FIGURE 1. Failure Rate vs Time

Infant mortality, the high failure rate from time t0 to t1 (early life), is greatly influenced by system stress conditions other than temperature, and can vary widely from one application to another. The main stress factors that contribute to infant mortality are electrical transients and noise, mechanical maltreatment and excessive temperatures. Most of these failures are discovered in device test, burn-in, card assembly and handling, and initial system test and operation. Although important, much literature is available on the subject of infant mortality in integrated circuits and is beyond the scope of this application note.

Failure rate is the number of devices that will be expected to fail in a given period of time (such as, per million hours). The mean time between failure (MTBF) is the average time (in hours) that will be expected to elapse after a unit has failed before the next unit failure will occur. These two primary "units of measure" for device reliability are inversely related:

$$\text{MTBF} = \frac{1}{\text{Failure Rate}}$$

Although the "bathtub" curve plots the overall failure rate versus time, the useful failure rate can be defined as the percentage of devices that fail per-unit-time during the flat portion of the curve. This area, called the useful life, extends between t1 and t2 or from the end of infant mortality to the onset of wearout. The useful life may be as short as several years but usually extends for decades if adequate design margins are used in the development of a system.

Many factors influence useful life including: pressure, mechanical stress, thermal cycling, and electrical stress. However, die temperature during the device's useful life plays an equally important role in triggering the onset of wearout.

FAILURE RATES vs TIME AND TEMPERATURE

The relationship between integrated circuit failure rates and time and temperature is a well established fact. The occurrence of these failures is a function which can be represented by the Arrhenius Model. Well validated and predominantly used for accelerated life testing of integrated circuits, the Arrhenius Model assumes the degradation of a performance parameter is linear with time and that MTBF is a function of temperature stress. The temperature dependence is an exponential function that defines the probability of occurrence. This results in a formula for expressing the lifetime or MTBF at a given temperature stress in relation to another MTBF at a different temperature. The ratio of these two MTBFs is called the acceleration factor F and is defined by the following equation:

$$F = \frac{X1}{X2} = \exp\left[\frac{E}{K}\left(\frac{1}{T2} - \frac{1}{T1}\right)\right]$$

Where: X1 = Failure rate at junction temperature T1
X2 = Failure rate at junction temperature T2
T = Junction temperature in degrees Kelvin
E = Thermal activation energy in electron volts (ev)
K = Boltzman's constant

However, the dramatic acceleration effect of junction temperature (chip temperature) on failure rate is illustrated in a plot of the above equation for three different activation energies in *Figure 2*. This graph clearly demonstrates the importance of the relationship of junction temperature to device failure rate. For example, using the 0.99 ev line, a 30° rise in junction temperature, say from 130°C to 160°C, results in a 10 to 1 increase in failure rate.

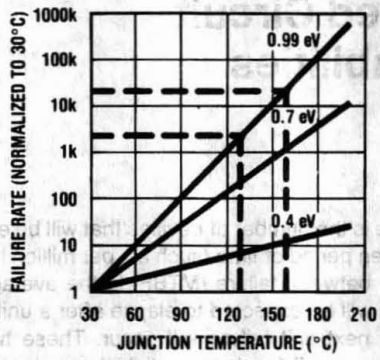

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FIGURE 2. Failure Rate as a Function of Junction Temperature

DEVICE THERMAL CAPABILITIES

There are many factors which affect the thermal capability of an integrated circuit. To understand these we need to understand the predominant paths for heat to transfer out of the integrated circuit package. This is illustrated by *Figures 3* and *4*.

Figure 3 shows a cross-sectional view of an assembled integrated circuit mounted into a printed circuit board.

Figure 4 is a flow chart showing how the heat generated at the power source, the junctions of the integrated circuit flows from the chip to the ultimate heat sink, the ambient environment. There are two predominant paths. The first is from the die to the die attach pad to the surrounding package material to the package lead frame to the printed circuit board and then to the ambient. The second path is from the package directly to the ambient air.

Improving the thermal characteristics of any stage in the flow chart of *Figure 4* will result in an improvement in device thermal characteristics. However, grouping all these characteristics into one equation determining the overall thermal capability of an integrated circuit/package/environmental condition is possible. The equation that expresses this relationship is:

$$T_J = T_A + P_D (\theta_{JA})$$

Where: T_J = Die junction temperature

T_A = Ambient temperature in the vicinity device

P_D = Total power dissipation (in watts)

θ_{JA} = Thermal resistance junction-to-ambient

θ_{JA}, the thermal resistance from device junction-to-ambient temperature, is measured and specified by the manufacturers of integrated circuits. National Semiconductor utilizes special vehicles and methods to measure and monitor this parameter. All circuit data sheets specify the thermal characteristics and capabilities of the packages available for a given device under specific conditions—these package power ratings directly relate to thermal resistance junction-to-ambient or θ_{JA}.

Although National provides these thermal ratings, it is critical that the end user understand how to use these numbers to improve thermal characteristics in the development of his system using IC components.

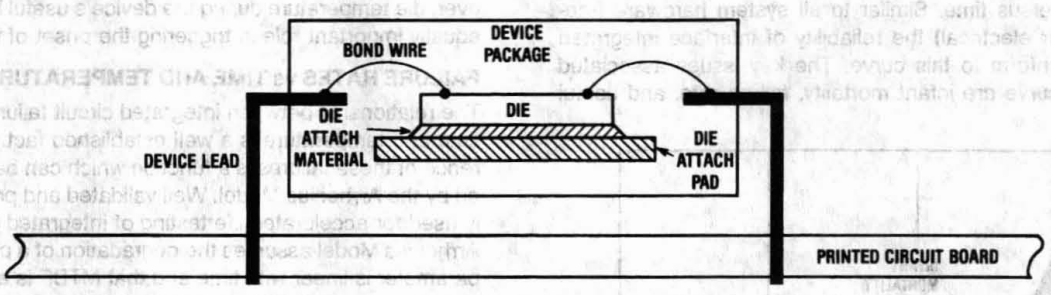

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FIGURE 3. Integrated Circuit Soldered into a Printed Circuit Board (Cross-Sectional View)

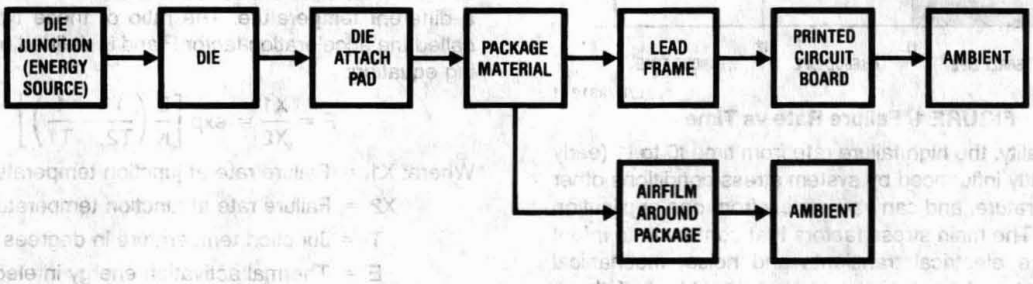

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FIGURE 4. Thermal Flow (Predominant Paths)

DETERMINING DEVICE OPERATING JUNCTION TEMPERATURE

From the above equation the method of determining actual worst-case device operating junction temperature becomes straightforward. Given a package thermal characteristic, θ_{JA}, worst-case ambient operating temperature, T_A(max), the only unknown parameter is device power dissipation, P_D. In calculating this parameter, the dissipation of the integrated circuit due to its own supply has to be considered, the dissipation within the package due to the external load must also be added. The power associated with the load in a dynamic (switching) situation must also be considered. For example, the power associated with an inductor or a capacitor in a static versus dynamic (say, 1 MHz) condition is significantly different.

The junction temperature of a device with a total package power of 600 mW at 70°C in a package with a thermal resistance of 63°C/W is 108°C.

$$T_J = 70°C + (63°C/W) \times (0.6W) = 108°C$$

The next obvious question is, "how safe is 108°C?"

MAXIMUM ALLOWABLE JUNCTION TEMPERATURES

What is an acceptable maximum operating junction temperature is in itself somewhat of a difficult question to answer. Many companies have established their own standards based on corporate policy. However, the semiconductor industry has developed some defacto standards based on the device package type. These have been well accepted as numbers that relate to reasonable (acceptable) device lifetimes, thus failure rates.

National Semiconductor has adopted these industry-wide standards. For devices fabricated in a molded package, the maximum allowable junction temperature is 150°C. For these devices assembled in ceramic or cavity DIP packages, the maximum allowable junction temperature is 175°C. The numbers are different because of the differences in package types. The thermal strain associated with the die package interface in a cavity package is much less than that exhibited in a molded package where the integrated circuit chip is in direct contact with the package material.

Let us use this new information and our thermal equation to construct a graph which displays the safe thermal (power) operating area for a given package type. *Figure 5* is an example of such a graph. The end points of this graph are easily determined. For a 16-pin molded package, the maximum allowable temperature is 150°C; at this point no power dissipation is allowable. The power capability at 25°C is 1.98W as given by the following calculation:

$$P_D @ 25°C = \frac{T_J(max) - T_A}{\theta_{JA}} = \frac{150°C - 25°C}{63°C/W} = 1.98W$$

The slope of the straight line between these two points is minus the inversion of the thermal resistance. This is referred to as the derating factor.

$$\text{Derating Factor} = -\frac{1}{\theta_{JA}}$$

As mentioned, *Figure 5* is a plot of the safe thermal operating area for a device in a 16-pin molded DIP. As long as the intersection of a vertical line defining the maximum ambient temperature (70°C in our previous example) and maximum device package power (600 mW) remains below the maximum package thermal capability line the junction temperature will remain below 150°C—the limit for a molded package. If the intersection of ambient temperature and package power fails on this line, the maximum junction temperature will be 150°C. Any intersection that occurs above this line will result in a junction temperature in excess of 150°C and is not an appropriate operating condition.

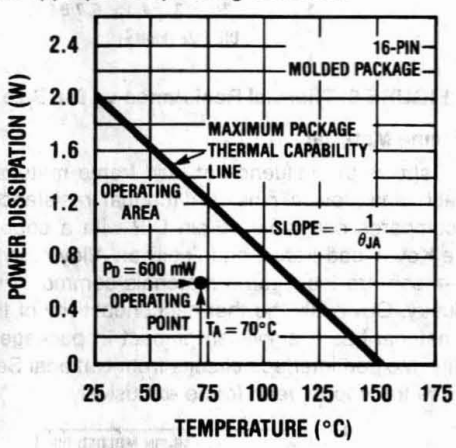

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FIGURE 5. Package Power Capability vs Temperature

The thermal capabilities of all integrated circuits are expressed as a power capability at 25°C still air environment with a given derating factor. This simply states, for every degree of ambient temperature rise above 25°C, reduce the package power capability stated by the derating factor which is expressed in mW/°C. For our example—a θ_{JA} of 63°C/W relates to a derating factor of 15.9 mW/°C.

FACTORS INFLUENCING PACKAGE THERMAL RESISTANCE

As discussed earlier, improving any portion of the two primary thermal flow paths will result in an improvement in overall thermal resistance junction-to-ambient. This section discusses those components of thermal resistance that can be influenced by the manufacturer of the integrated circuit. It also discusses those factors in the overall thermal resistance that can be impacted by the end user of the integrated circuit. Understanding these issues will go a long way in understanding chip power capabilities and what can be done to insure the best possible operating conditions and, thus, best overall reliability.

Die Size

Figure 6 shows a graph of our 16-pin DIP thermal resistance as a function of integrated circuit die size. Clearly, as the chip size increases the thermal resistance decreases—this relates directly to having a larger area with which to dissipate a given power.

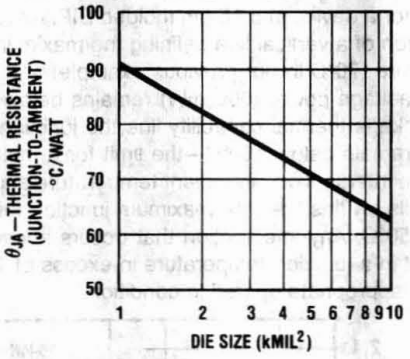

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FIGURE 6. Thermal Resistance vs Die Size

Lead Frame Material

Figure 7 shows the influence of lead frame material (both die attach and device pins) on thermal resistance. This graph compares our same 16-pin DIP with a copper lead frame, a Kovar lead frame, and finally an Alloy 42 type lead frame—these are lead frame materials commonly used in the industry. Obviously the thermal conductivity of the lead frame material has a significant impact in package power capability. Molded interface circuits from National Semiconductor use the copper lead frame exclusively.

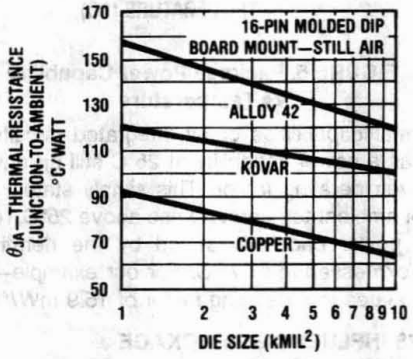

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FIGURE 7. Thermal Resistance vs Lead Frame Material

Board vs Socket Mount

One of the major paths of dissipating energy generated by the integrated circuit is through the device leads. As a result of this, the graph of *Figure 8* comes as no surprise. This compares the thermal resistance of our 16-pin package soldered into a printed circuit board (board mount) compared to the same package placed in a socket (socket mount). Adding a socket in the path between the PC board and the device adds another stage in the thermal flow path, thus increasing the overall thermal resistance. The thermal capabilities of National Semiconductor's interface circuits are specified assuming board mount conditions. If the devices are placed in a socket the thermal capabilities should be reduced by approximately 5% to 10%.

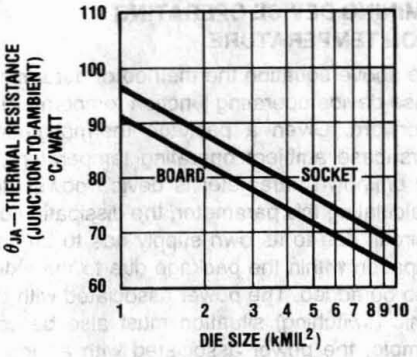

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FIGURE 8. Thermal Resistance vs Board or Socket Mount

Air Flow

When a high power situation exists and the ambient temperature cannot be reduced, the next best thing is to provide air flow in the vicinity of the package. The graph of *Figure 9* illustrates the impact this has on thermal resistance. This graph plots the relative reduction in thermal resistance normalized to the still air condition for our 16-pin molded DIP. The thermal ratings on National Semiconductor's interface circuits data sheets relate to the still air environment.

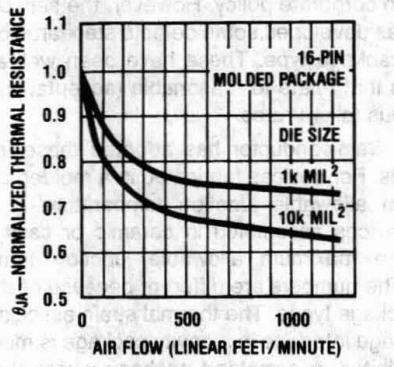

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FIGURE 9. Thermal Resistance vs Air Flow

Other Factors

A number of other factors influence thermal resistance. The most important of these is using thermal epoxy in mounting ICs to the PC board and heat sinks. Generally these techniques are required only in the very highest of power applications.

Some confusion exists between the difference in thermal resistance junction-to-ambient (θ_{JA}) and thermal resistance junction-to-case (θ_{JC}). The best measure of actual junction temperature is the junction-to-ambient number since nearly all systems operate in an open air environment. The only situation where thermal resistance junction-to-case is important is when the entire system is immersed in a thermal bath and the environmental temperature is indeed the case temperature. This is only used in extreme cases and is the exception to the rule and, for this reason, is not addressed in this application note.

NATIONAL SEMICONDUCTOR PACKAGE CAPABILITIES

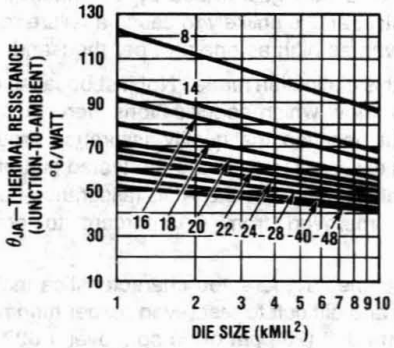
Figures 10 and *11* show composite plots of the thermal characteristics of the most common package types in the National Semiconductor Linear Circuits product family. *Figure 10* is a composite of the copper lead frame molded

package. *Figure 11* is a composite of the ceramic (cavity) DIP using poly die attach. These graphs represent board mount still air thermal capabilities. Another, and final, thermal resistance trend will be noticed in these graphs. As the number of device pins increase in a DIP the thermal resistance decreases. Referring back to the thermal flow chart, this trend should, by now, be obvious.

RATINGS ON INTEGRATED CIRCUITS DATA SHEETS

In conclusion, all National Semiconductor Linear Products define power dissipation (thermal) capability. This information can be found in the Absolute Maximum Ratings section of the data sheet. The thermal information shown in this application note represents average data for characterization of the indicated package. Actual thermal resistance can vary from ±10% to ±15% due to fluctuations in assembly quality, die shape, die thickness, distribution of heat sources on the die, etc. The numbers quoted in the linear data sheets reflect a 15% safety margin from the average numbers found in this application note. Insuring that total package power remains under a specified level will guarantee that the maximum junction temperature will not exceed the package maximum.

Molded (N Package) DIP*
Copper Leadframe—HTP
Die Attach Board Mount—
Still Air



*Packages from 8- to 20-pin 0.3 mil width
22-pin 0.4 mil width
24- to 40-pin 0.6 mil width

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FIGURE 10. Thermal Resistance vs Die Size vs Package Type (Molded Package)

Surface Mount (M, MW Packages),
Board Mount, Still Air

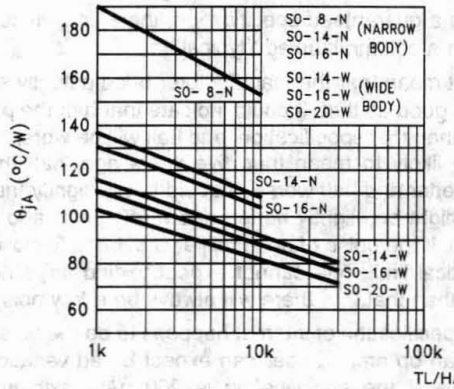

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FIGURE 12. Thermal Resistance for "SO" Packages (Board Mount)

The package power ratings are specified as a maximum power at 25°C ambient with an associated derating factor for ambient temperatures above 25°C. It is easy to determine the power capability at an elevated temperature. The power specified at 25°C should be reduced by the derating factor for every degree of ambient temperature above 25°C. For example, in a given product data sheet the following will be found:

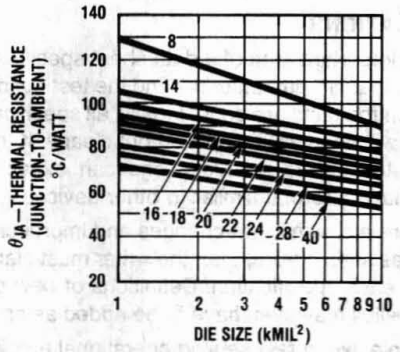
Maximum Power Dissipation* at 25°C
Cavity Package 1509 mW
Molded Package 1476 mW

* Derate cavity package at 10 mW/°C above 25°C; derate molded package at 11.8 mW/°C above 25°C.

If the molded package is used at a maximum ambient temperature of 70°C, the package power capability is 945 mW.

$$P_D \text{ @ } 70°C = 1476 \text{ mW} - (11.8 \text{ mW/°C}) \times (70°C - 25°C)$$
$$= 945 \text{ mW}$$

Cavity (J Package) DIP*
Poly Die Attach Board
Mount—Still Air



*Packages from 8- to 20-pin 0.3 mil width
22-pin 0.4 mil width
24- to 48-pin 0.6 mil width

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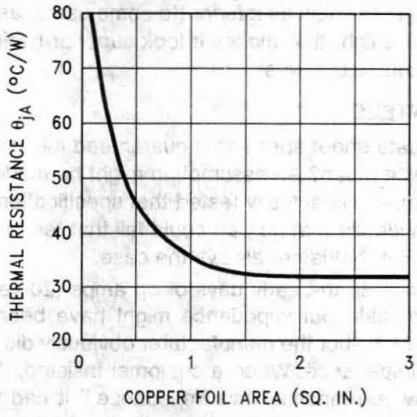
FIGURE 11. Thermal Resistance vs Die Size vs Package Type (Cavity Package)

TO-263 (S Package)
Board Mount, Still Air



TL/H/9312-13

*For products with high current ratings (>3A), thermal resistance may be lower. Consult product datasheet for more information.

FIGURE 13. Thermal Resistance (typ.*) for 3-, 5-, and 7-L TO-263 packages mounted on 1 oz. (0.036mm) PC board foil

6

National Semiconductor

APPENDIX F
How to Get the Right Information From a Data Sheet

Not All Data Sheets Are Created Alike, and False Assumptions Could Cost an Engineer Time and Money

By Robert A. Pease

When a new product arrives in the marketplace, it hopefully will have a good, clear data sheet with it.

The data sheet can show the prospective user how to apply the device, what performance specifications are guaranteed and various typical applications and characteristics. If the data-sheet writer has done a good job, the user can decide if the product will be valuable to him, exactly how well it will be of use to him and what precautions to take to avoid problems.

SPECIFICATIONS

The most important area of a data sheet specifies the characteristics that are guaranteed—and the test conditions that apply when the tests are done. Ideally, all specifications that the users will need will be spelled out clearly. If the product is similar to existing products, one can expect the data sheet to have a format similar to other devices.

But, if there are significant changes and improvements that nobody has seen before, then the writer must clarify what is meant by each specification. Definitions of new phrases or characteristics may even have to be added as an appendix.

For example, when fast-settling operational amplifiers were first introduced, some manufacturers defined settling time as the time after slewing before the output finally enters and stays within the error-band; but other manufacturers included the slewing time in their definition. Because both groups made their definitions clear, the user was unlikely to be confused or misled.

However, the reader ought to be on the alert. In a few cases, the data-sheet writer is playing a specsmanship game, and is trying to show an inferior (to some users) aspect of a product in a light that makes it look superior (which it may be, to a couple of users).

GUARANTEES

When a data sheet specifies a guaranteed minimum value, what does it mean? An assumption might be made that the manufacturer has actually tested that specification and has great confidence that no part could fail that test and still be shipped. Yet that is not always the case.

For instance, in the early days of op amps (20 years ago), the differential-input impedance might have been guaranteed at 1 MΩ—but the manufacturer obviously did not measure the impedance. When a customer insisted, "I have to know how you measure this impedance," it had to be explained that the impedance was not measured, but that the base current was. The correlation between I_b and Z_{in} permitted the substitution of this simple dc test for a rather messy, noisy, hard-to-interpret test.

Every year, for the last 20 years, manufacturers have been trying to explain, with varying success, why they do not measure the Z_{in} *per se,* even though they do guarantee it.

In other cases, the manufacturer may specify a test that can be made only on the die as it is probed on the wafer, but cannot be tested after the die is packaged because that signal is not accessible any longer. To avoid frustrating and confusing the customer, some manufacturers are establishing two classes of guaranteed specifications:

- The tested limit represents a test that cannot be doubted, one that is actually performed directly on 100 percent of the devices, 100 percent of the time.
- The design limit covers other tests that may be indirect, implicit or simply guaranteed by the inherent design of the device, and is unlikely to cause a failure rate (on that test), even as high as one part per thousand.

Why was this distinction made? Not just because customers wanted to know which specifications were guaranteed by testing, but because the quality-assurance group insisted that it was essential to separate the tested guarantees from the design limits so that the AQL (assurance-quality level) could be improved from 0.1 percent to down below 100 ppm.

Some data sheets guarantee characteristics that are quite expensive and difficult to test (even harder than noise) such as long-term drift (20 ppm or 50 ppm over 1,000 hours).

The data sheet may not tell the reader if it is measured, tested or estimated. One manufacturer may perform a 100-percent test, while another states, "Guaranteed by sample testing." This is not a very comforting assurance that a part is good, especially in a critical case where only a long-term test can prove if the device did meet the manufacturer's specification. If in doubt, question the manufacturer.

TYPICALS

Next to a guaranteed specification, there is likely to be another in a column labeled "typical".

It might mean that the manufacturer once actually saw one part as good as that. It could indicate that half the parts are better than that specification, and half will be worse. But it is equally likely to mean that, five years ago, half the parts were better and half worse. It could easily signify that a few parts might be slightly better, and a few parts a lot worse; after all, if the noise of an amplifier is extremely close to the theoretical limit, one cannot expect to find anything much better than that, but there will always be a few noisy ones.

If the specification of interest happens to be the bias current (I_b) of an op amp, a user can expect broad variations. For example, if the specification is 200 nA maximum, there might be many parts where I_b is 40 nA on one batch (where the beta is high), and a month later, many parts where the I_b is 140 nA when the beta is low.

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Absolute Maximum Ratings (Note 11)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	+35V to −0.2V
Output Voltage	+6V to −1.0V
Output Current	10 mA
Storage Temperature,	
TO-46 Package	−76°F to +356°F
TO-92 Package	−76°F to +300°F
Lead Temp. (Soldering, 4 seconds) *	
TO-46 Package	+300°C
TO-92 Package	+260°C

Specified Operating Temp. Range (Note 2)

	T_{MIN} to T_{MAX}
LM34, LM34A	−50°F to +300°F
LM34C, LM34CA	−40°F to +230°F
LM34D	+32°F to +212°F

DC Electrical Characteristics (Note 1, Note 6)

Parameter	Conditions	LM34A			LM34CA			Units (Max)
		Typical	Tested Limit (Note 4)	Design Limit (Note 5)	Typical	Tested Limit (Note 4)	Design Limit (Note 5)	
Accuracy (Note 7)	T_A = +77°F	±0.4	±1.0		±0.4	±1.0		°F
	T_A = 0°F	±0.6			±0.6		±2.0	°F
	T_A = T_{MAX}	±0.8	±2.0		±0.8	±2.0		°F
	T_A = T_{MIN}	±0.8	±2.0		±0.8		±3.0	°F
Nonlinearity (Note 8)	$T_{MIN} \le T_A \le T_{MAX}$	**±0.35**		**±0.7**	**±0.30**		**±0.6**	°F
Sensor Gain (Average Slope)	$T_{MIN} \le T_A \le T_{MAX}$	**+10.0**	**+9.9, +10.1**		**+10.0**		**+9.9, +10.1**	mV/°F, min mV/°F, max
Load Regulation (Note 3)	T_A = +77°F	±0.4	±1.0		±0.4	±1.0		mV/mA
	$T_{MIN} \le T_A \le T_{MAX}$	**±0.5**		**±3.0**	**±0.5**		**±3.0**	mV/mA
	$0 \le I_L \le 1$ mA							
Line Regulation (Note 3)	T_A = +77°F	±0.01	±0.05		±0.01	±0.05		mV/V
	$5V \le V_S \le 30V$	**±0.02**		**±0.1**	**±0.02**		**±0.1**	mV/V
Quiescent Current (Note 9)	V_S = +5V, +77°F	75	90		75	90		µA
	V_S = +5V	**131**		**160**	**116**		**139**	µA
	V_S = +30V, +77°F	76	92		76	92		µA
	V_S = +30V	**132**		**163**	**117**		**142**	µA
Change of Quiescent Current (Note 3)	$4V \le V_S \le 30V$, +77°F	+0.5	2.0		0.5	2.0		µA
	$5V \le V_S \le 30V$	**+1.0**		**3.0**	**1.0**		**3.0**	µA
Temperature Coefficient of Quiescent Current		**+0.30**		**+0.5**	**+0.30**		**+0.5**	µA/°F
Minimum Temperature for Rated Accuracy	In circuit of *Figure 1*, I_L = 0	+3.0		+5.0	+3.0		+5.0	°F
Long-Term Stability	T_j = T_{MAX} for 1000 hours	±0.16			±0.16			°F

Note 1: Unless otherwise noted, these specifications apply: $-50°F \le T_j \le +300°F$ for the LM34 and LM34A; $-40°F \le T_j \le +230°F$ for the LM34C and LM34CA; and $+32°F \le T_j \le +212°F$ for the LM34D. V_S = +5 Vdc and I_{LOAD} = 50 µA in the circuit of *Figure 2*; +6 Vdc for LM34 and LM34A for $230°F \le T_j \le 300°F$. These specifications also apply from +5°F to T_{MAX} in the circuit of *Figure 1*.

Note 2: Thermal resistance of the TO-46 package is 292°F/W junction to ambient and 43°F/W junction to case. Thermal resistance of the TO-92 package is 324°F/W junction to ambient.

Note 3: Regulation is measured at constant junction temperature using pulse testing with a low duty cycle. Changes in output due to heating effects can be computed by multiplying the internal dissipation by the thermal resistance.

Note 4: Tested limits are guaranteed and 100% tested in production.

Note 5: Design limits are guaranteed (but not 100% production tested) over the indicated temperature and supply voltage ranges. These limits are not used to calculate outgoing quality levels.

Note 6: Specification in **BOLDFACE TYPE** apply over the full rated temperature range.

Note 7: Accuracy is defined as the error between the output voltage and 10 mV/°F times the device's case temperature at specified conditions of voltage, current, and temperature (expressed in °F).

Note 8: Nonlinearity is defined as the deviation of the output-voltage-versus-temperature curve from the best-fit straight line over the device's rated temperature range.

Note 9: Quiescent current is defined in the circuit of *Figure 1*.

Note 10: Contact factory for availability of LM34CAZ.

** **Note 11:** Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications do not apply when operating the device beyond its rated operating conditions (see Note 1).

A Point-By-Point Look

Let's look a little more closely at the data sheet of the National Semiconductor LM34, which happens to be a temperature sensor.

Note 1 lists the nominal test conditions and test circuits in which all the characteristics are defined. Some additional test conditions are listed in the column "Conditions", but Note 1 helps minimize the clutter.

Note 2 gives the thermal impedance, (which may also be shown in a chart or table).

Note 3 warns that an output impedance test, if done with a long pulse, could cause significant self-heating and thus, error.

Note 6 is intended to show which specs apply at all rated temperatures.

Note 7 is the definition of the "Accuracy" spec, and Note 8 the definition for non-linearity. Note 9 states in what test circuit the quiescent current is defined. Note 10 indicates that one model of the family may not be available at the time of printing (but happens to be available now), and Note 11 is the definition of Absolute Max Ratings.

* Note—the "4 seconds" soldering time is a new standard for plastic packages.

** Note—the wording of Note 11 has been revised—this is the best wording we can devise, and we will use it on all future datasheets.

APPLICATIONS

Another important part of the data sheet is the applications section. It indicates the novel and conventional ways to use a device. Sometimes these applications are just little ideas to tweak a reader's mind. After looking at a couple of applications, one can invent other ideas that are useful. Some applications may be of no real interest or use.

In other cases, an application circuit may be the complete definition of the system's performance; it can be the test circuit in which the specification limits are defined, tested and guaranteed. But, in all other instances, the performance of a typical application circuit is not guaranteed, it is only typical. In many circumstances, the performance may depend on external components and their precision and matching. Some manufacturers have added a phrase to their data sheets:

"Applications for any circuits contained in this document are for illustration purposes only and the manufacturer makes no representation or warranty that such applications will be suitable for the use indicated without further testing or modification."

In the future, manufacturers may find it necessary to add disclaimers of this kind to avoid disappointing users with circuits that work well, much of the time, but cannot be easily guaranteed.

The applications section is also a good place to look for advice on quirks—potential drawbacks or little details that may not be so little when a user wants to know if a device will actually deliver the expected performance.

For example, if a buffer can drive heavy loads and can handle fast signals cleanly (at no load), the maker isn't doing anybody any favors if there is no mention that the distortion goes sky-high if the rated load is applied.

Another example is the application hint for the LF156 family:

"Exceeding the negative common-mode limit on either input will cause a reversal of the phase to output and force the amplifier output to the corresponding high or low state. Exceeding the negative common-mode limit on both inputs will force the amplifier output to a high state. In neither case does a latch occur, since raising the input back within the common-mode range again puts the input stage and, thus the amplifier, in a normal operating mode."

That's the kind of information a manufacturer should really give to a data-sheet reader because no one could ever guess it.

Sometimes, a writer slips a quirk into a characteristic curve, but it's wiser to draw attention to it with a line of text. This is because it's better to make the user sad before one gets started, rather than when one goes into production. Conversely, if a user is going to spend more than 10 minutes using a new product, one ought to spend a full five minutes reading the entire data sheet.

FINE PRINT

What other fine print can be found on a data sheet? Sometimes the front page may be marked "advance" or "preliminary." Then on the back page, the fine print may say something such as:

"This data sheet contains preliminary limits and design specifications. Supplemental information will be published at a later date. The manufacturer reserves the right to make changes in the products contained in this document in order to improve design or performance and to supply the best possible products. We also assume no responsibility for the use of any circuits described herein, convey no license under any patent or other right and make no representation that the circuits are free from patent infringement."

In fact, after a device is released to the marketplace in a preliminary status, the engineers love to make small improvements and upgrades in specifications and characteristics, and hate to degrade a specification from its first published value—but occasionally that is necessary.

Another item in the fine print is the manufacturer's telephone number. Usually it is best to refer questions to the local sales representative or field-applications engineer, because they may know the answer or they may be best able to put a questioner in touch with the right person at the factory.

Occasionally, the factory's applications engineers have all the information. Other times, they have to bring in product engineers, test engineers or marketing people. And sometimes the answer can't be generated quickly—data have to be gathered, opinions solidified or policies formulated before the manufacturer can answer the question. Still, the telephone number is the key to getting the factory to help.

ORIGINS OF DATA SHEETS

Of course, historically, most data sheets for a class of products have been closely modeled on the data sheet of the forerunner of that class. The first data sheet was copied to make new versions.

That's the way it happened with the UA709 (the first monolithic op amp) and all its copies, as well as many other similar families of circuits.

Even today, an attempt is made to build on the good things learned from the past and add a few improvements when necessary. But, it's important to have real improvements, not just change for the sake of change.

So, while it's not easy to get the format and everything in it exactly right to please everybody, new data sheets are continually surfacing with new features, applications ideas, specifications and aids for the user. And, if the users complain loudly enough about misleading or inadequate data sheets, they can help lead the way to change data sheets. That's how many of today's improvements came about—through customer demand.

Who writes data sheets? In some cases, a marketing person does the actual writing and engineers do the checking. In other companies, the engineer writes, while marketing people and other engineers check. Sometimes, a committee seems to be doing the writing. None of these ways is necessarily wrong.

For example, one approach might be: The original designer of the product writes the data sheet (inside his head) at the same time the product is designed. The concept here is, if one can't find the proper ingredients for a data sheet—good applications, convenient features for the user and nicely tested specifications as the part is being designed—then maybe it's not a very good product until all those ingredients are completed. Thus, the collection of raw materials for a good data sheet is an integral part of the design of a product. The actual assembly of these materials is an art which can take place later.

WHEN TO WRITE DATA SHEETS

A new product becomes available. The applications engineers start evaluating their application circuits and the test engineers examine their production test equipment.

But how can the users evaluate the new device? They have to have a data sheet—which is still in the process of being written. Every week, as the data sheet writer tries to polish and refine the incipient data sheet, other engineers are reporting, "These spec limits and conditions have to be revised," and, "Those application circuits don't work like we thought they would; we'll have one running in a couple of days." The marketing people insist that the data sheet must be finalized and frozen right away so that they can start printing copies to go out with evaluation samples.

These trying conditions may explain why data sheets always seem to have been thrown together under panic conditions and why they have so many rough spots. Users should be aware of the conflicting requirements: Getting a data sheet "as completely as possible" and "as accurately as possible" is compromised if one wants to get the data sheet "as quickly as possible."

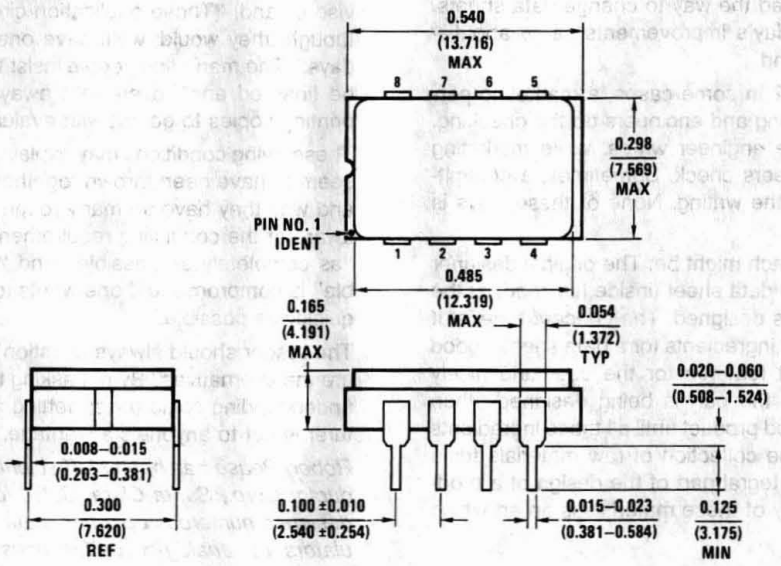
The reader should always question the manufacturer. What are the alternatives? By not asking the right question, a misunderstanding could arise; getting angry with the manufacturer is not to anyone's advantage.

Robert Pease has been staff scientist at National Semiconductor Corp., Santa Clara, Calif., for eleven years. He has designed numerous op amps, data converters, voltage regulators and analog-circuit functions.

National Semiconductor

8 Lead Ceramic Sidebrazed Dual-in-Line Package
NS Package Number D08C

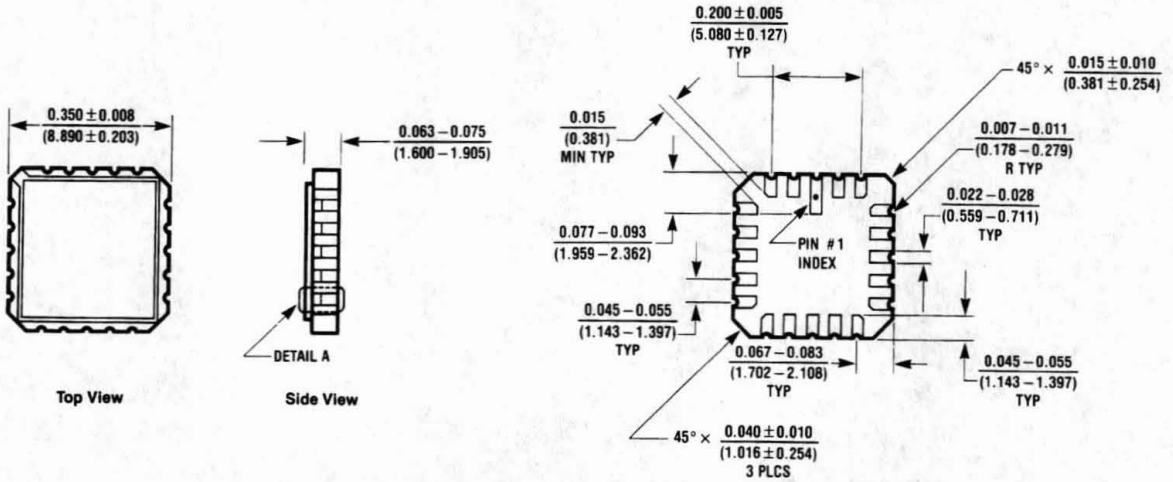
All dimensions are in inches (millimeters)

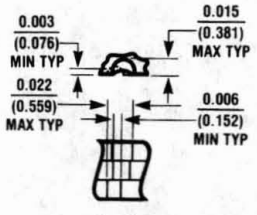


D08C (REV C)

20 Lead Ceramic Leadless Chip Carrier, Type C
NS Package Number E20A

All dimensions are in inches (millimeters)

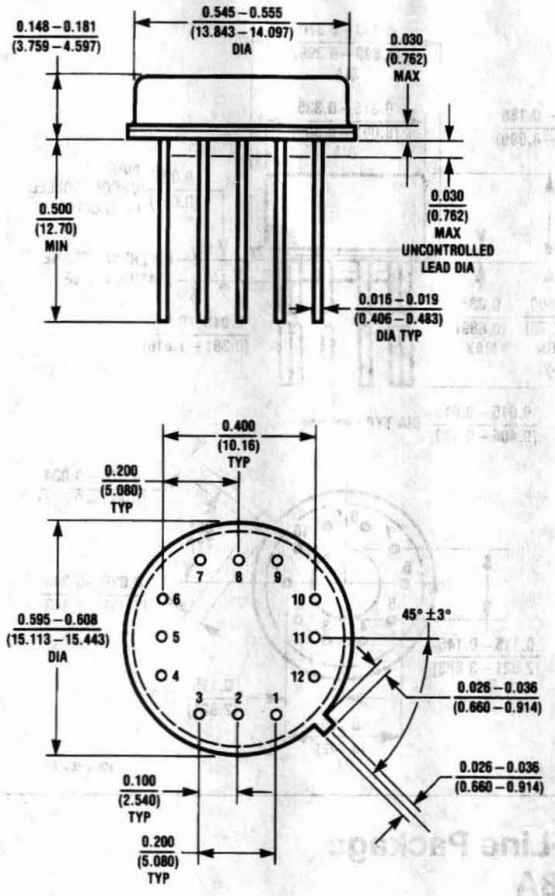




E20A (REV D)

12 Lead (0.400" Square Pattern) TO-8 Metal Can Package
NS Package Number G12B

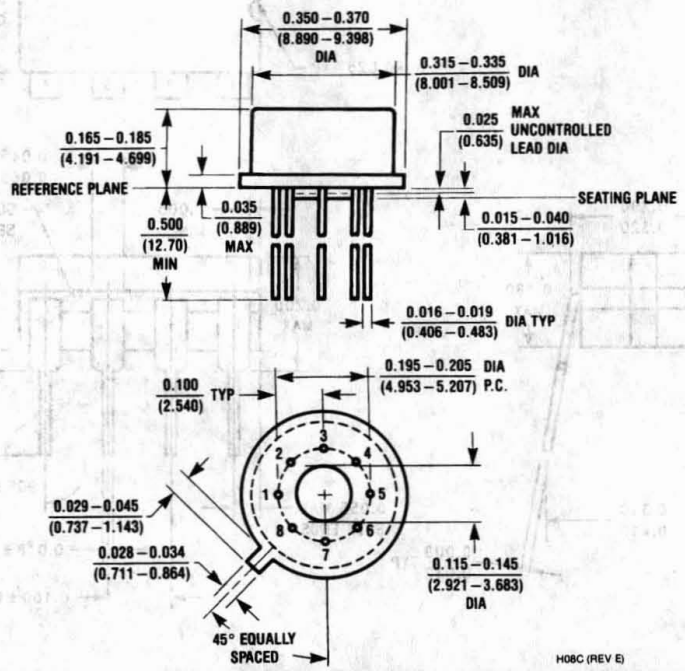
All dimensions are in inches (millimeters)



G12B (REV C)

8 Lead (0.200" Diameter P.C.) TO-5 Metal Can Package
NS Package Number H08C

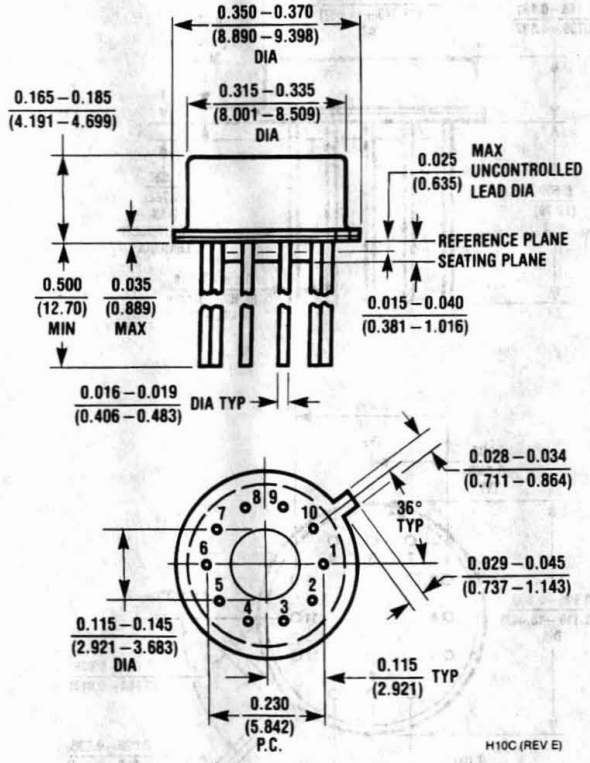
All dimensions are in inches (millimeters)



H08C (REV E)

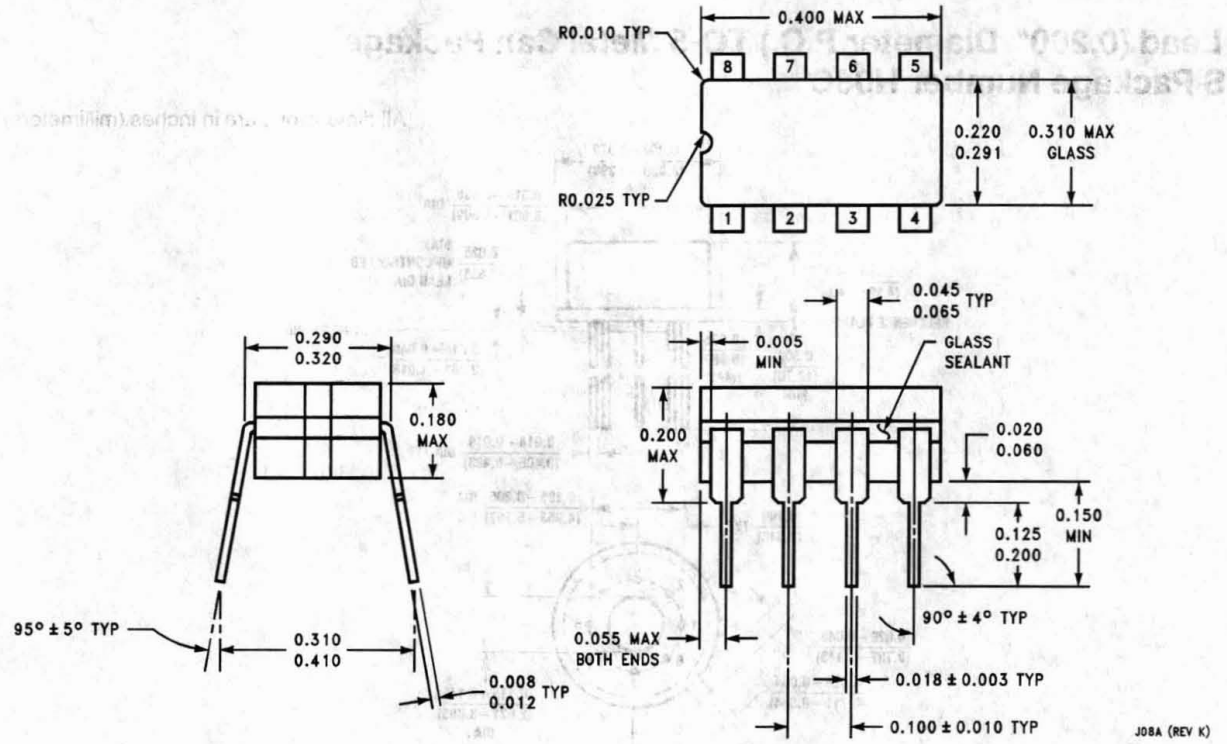
10 Lead (0.230" Diameter P.C.) TO-5 Metal Can Package
NS Package Number H10C

All dimensions are in inches (millimeters)



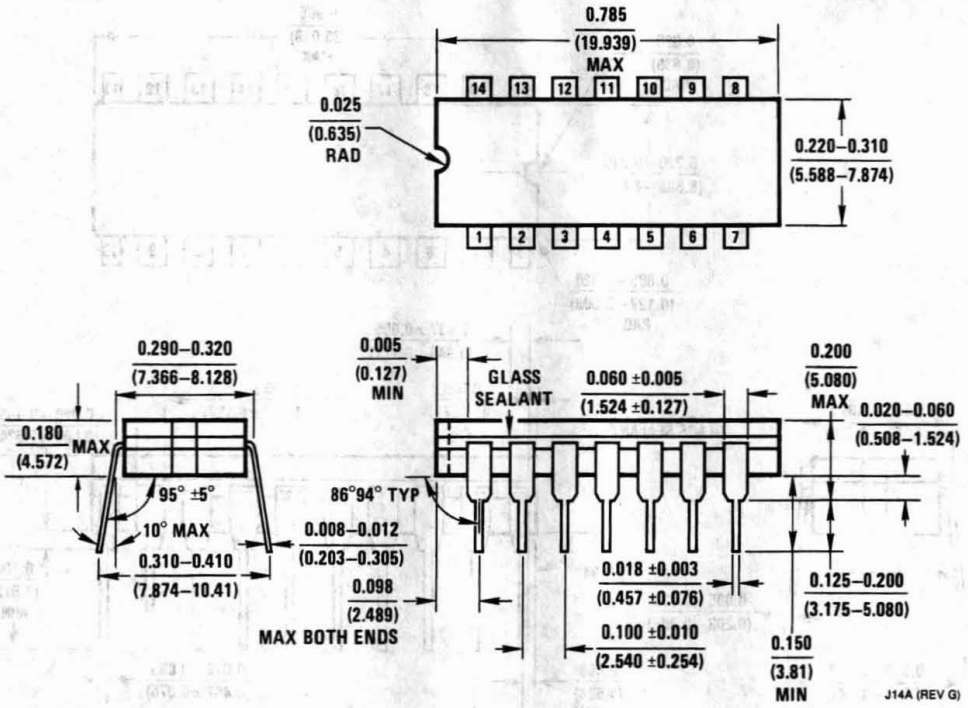
8 Lead Ceramic Dual-in-Line Package
NS Package Number J08A

All dimensions are in inches



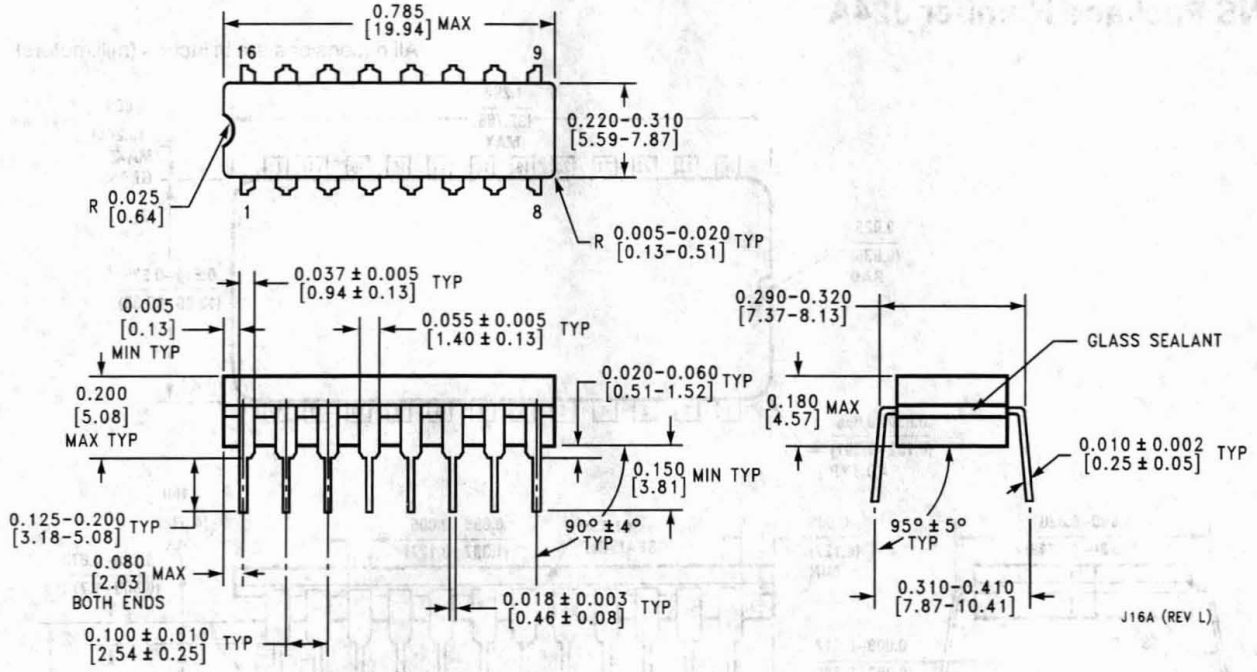
14 Lead Ceramic Dual-in-Line Package
NS Package Number J14A

All dimensions are in inches (millimeters)



16 Lead Ceramic Dual-in-Line Package
NS Package Number J16A

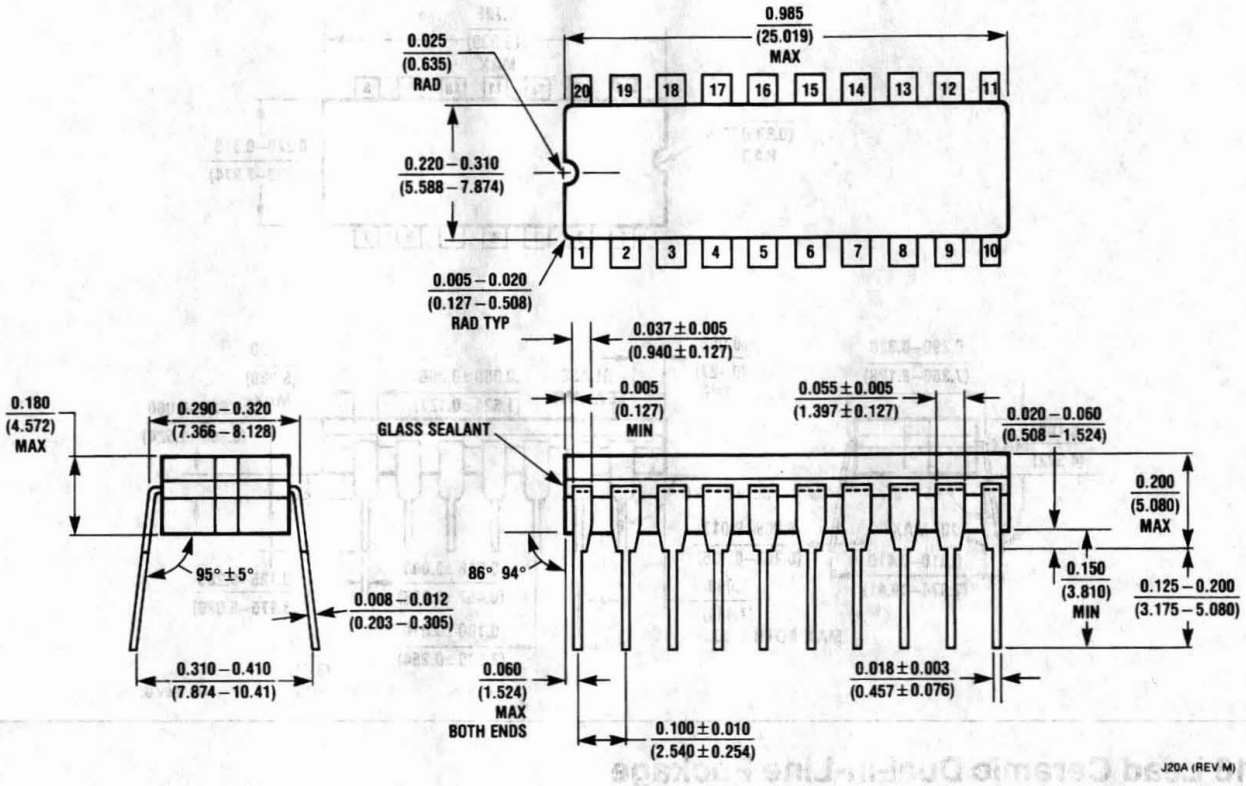
All dimensions are in inches [millimeters]



6

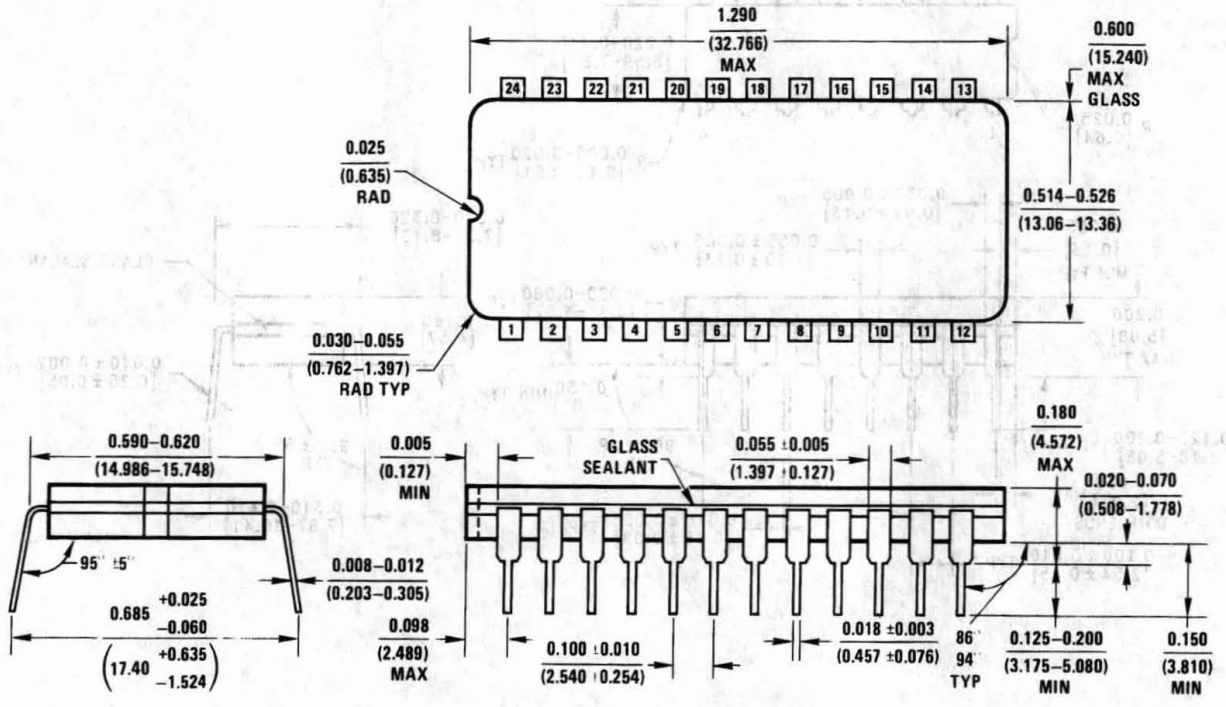
20 Lead Ceramic Dual-in-Line Package
NS Package Number J20A

All dimensions are in inches (millimeters)



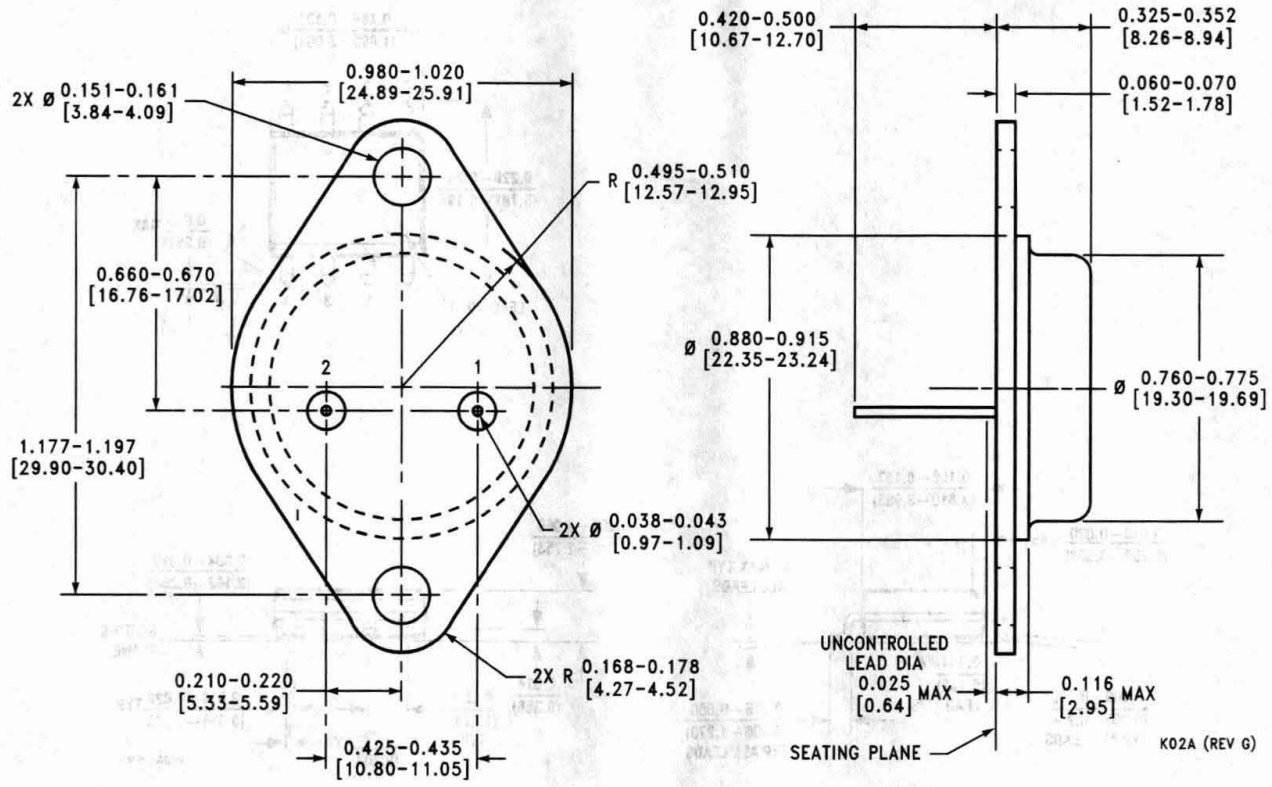
24 Lead Ceramic Dual-in-Line Package
NS Package Number J24A

All dimensions are in inches (millimeters)



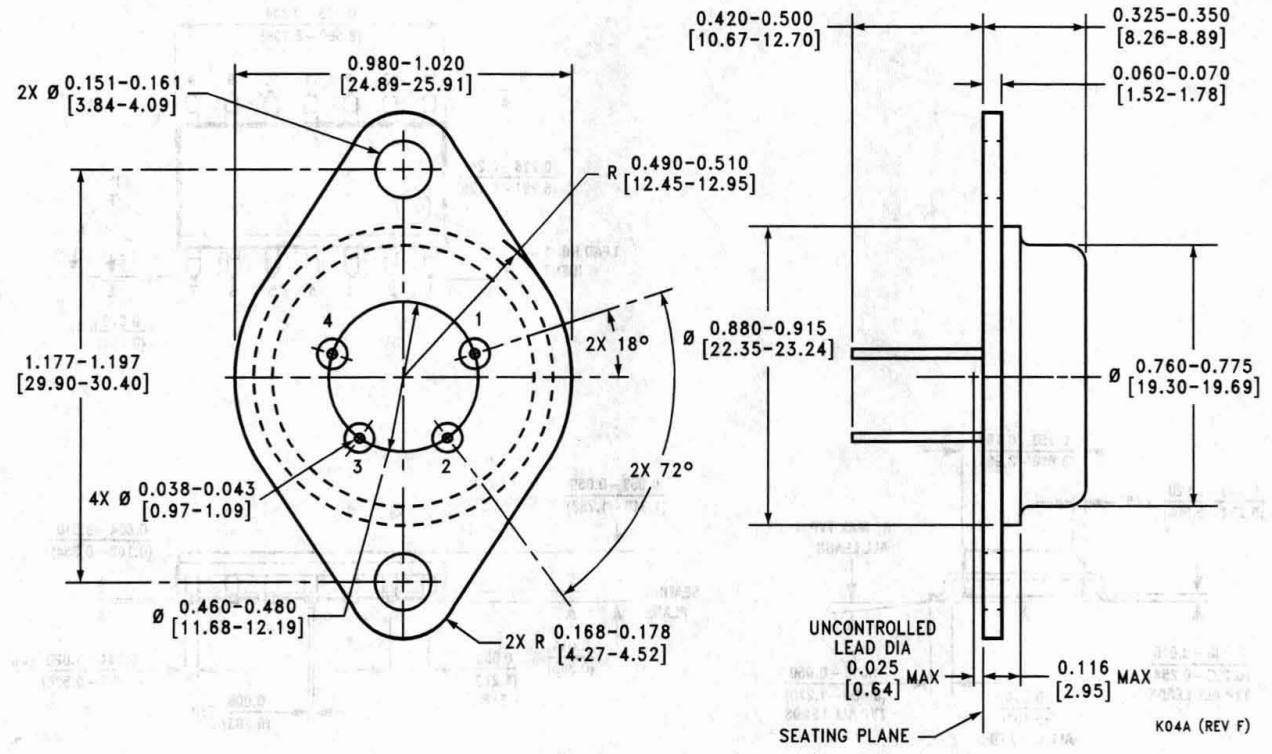
2 Lead TO-3 Metal Can Package
NS Package Number K02A

All dimensions are in inches [millimeters]



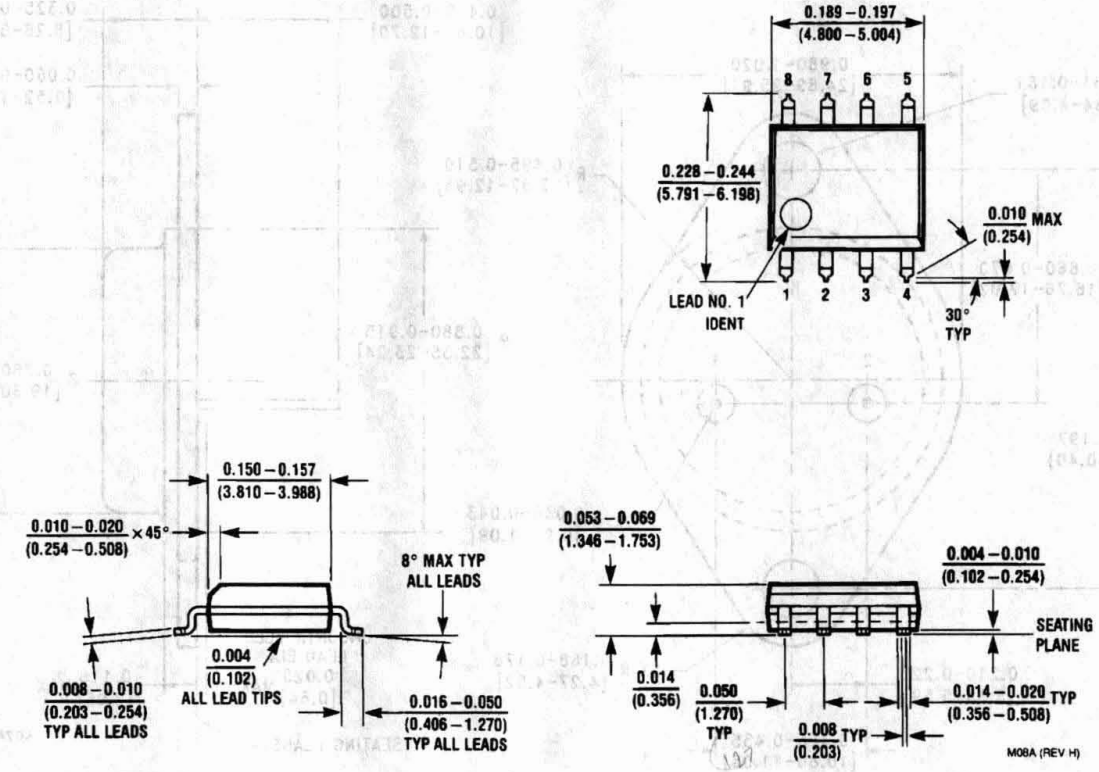
4 Lead TO-3 Metal Can Package
NS Package Number K04A

All dimensions are in inches [millimeters]



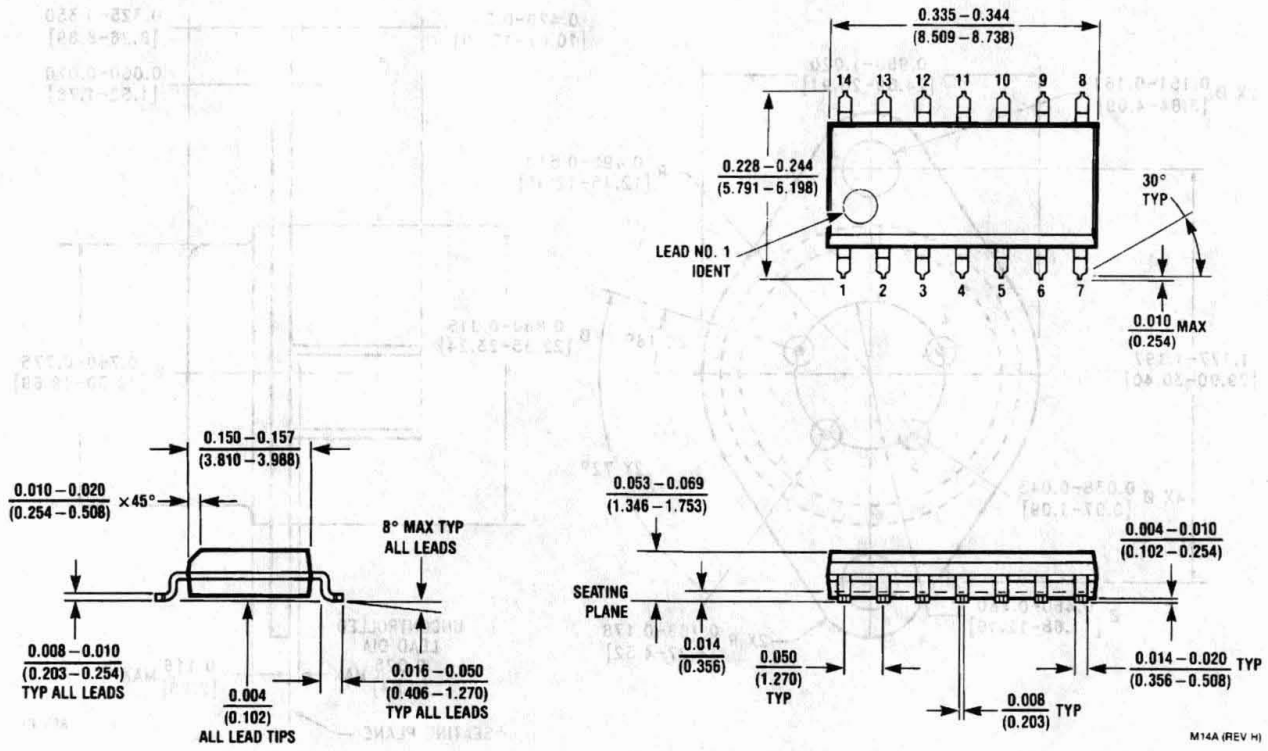
8 Lead (0.150″ Wide) Molded Small Outline Package, JEDEC
NS Package Number M08A

All dimensions are in inches (millimeters)



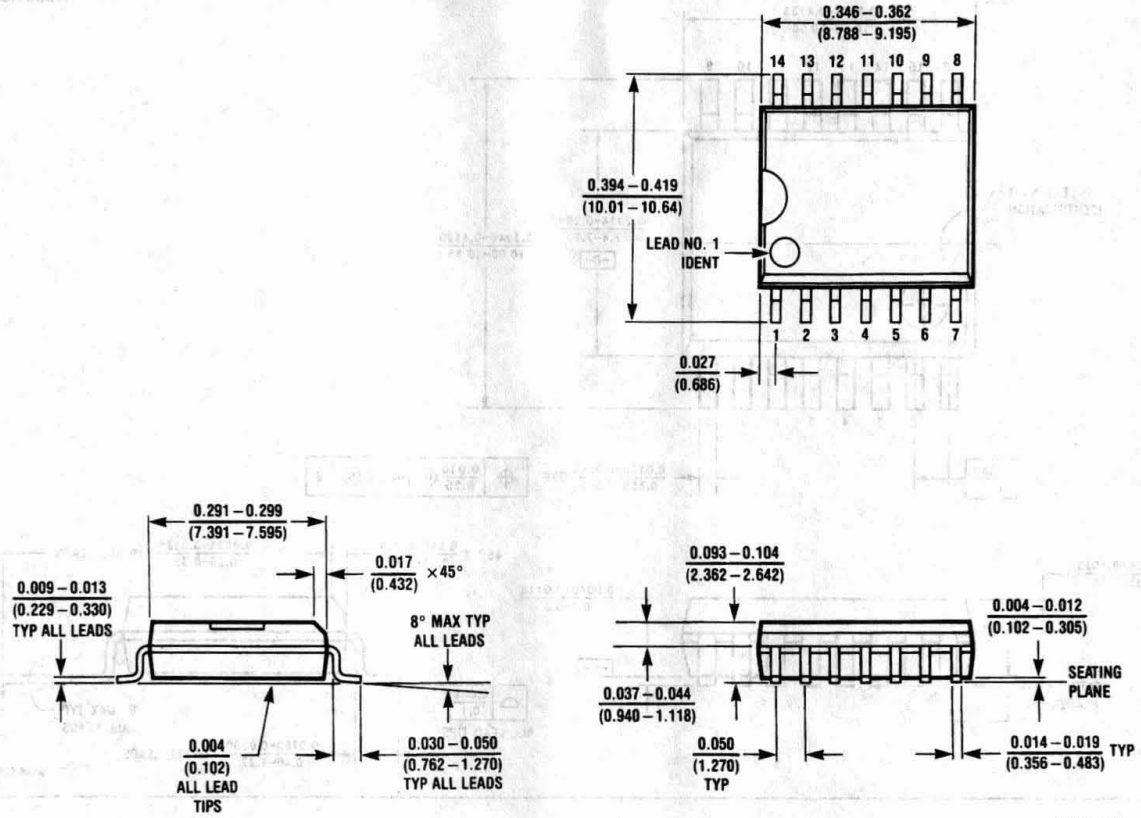
14 Lead (0.150″ Wide) Molded Small Outline Package, JEDEC
NS Package Number M14A

All dimensions are in inches (millimeters)



14 Lead (0.300" Wide) Molded Small Outline Package, JEDEC
NS Package Number M14B

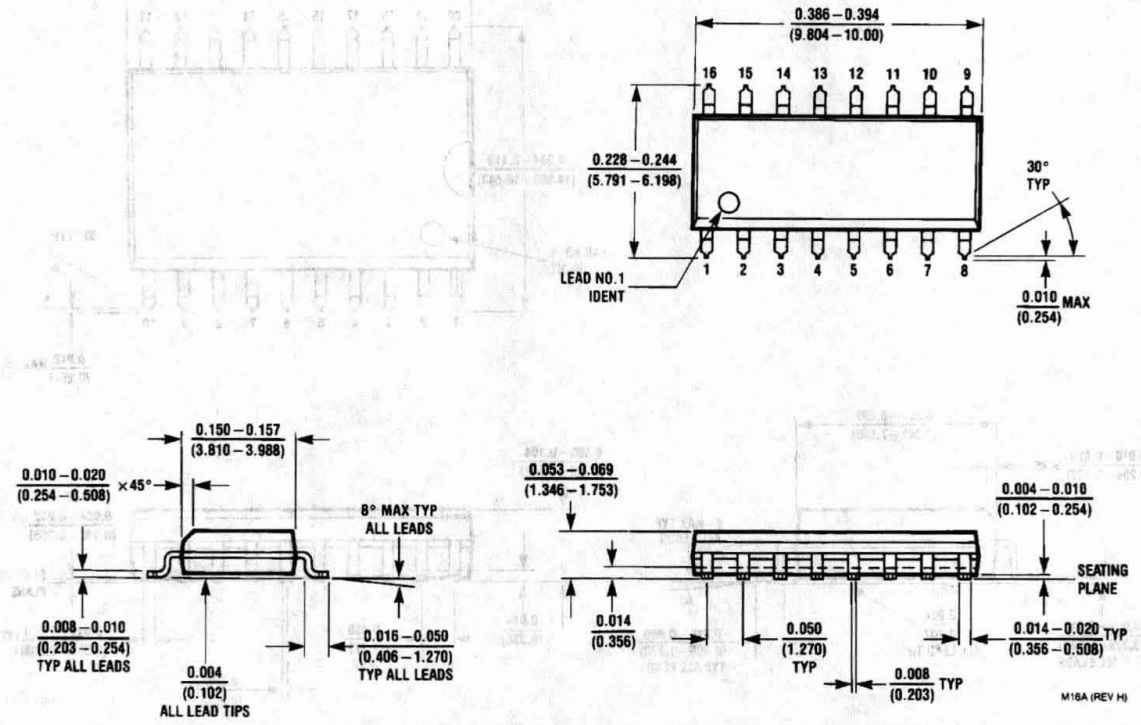
All dimensions are in inches (millimeters)



M14B (REV D)

16 Lead (0.150" Wide) Molded Small Outline Package, JEDEC
NS Package Number M16A

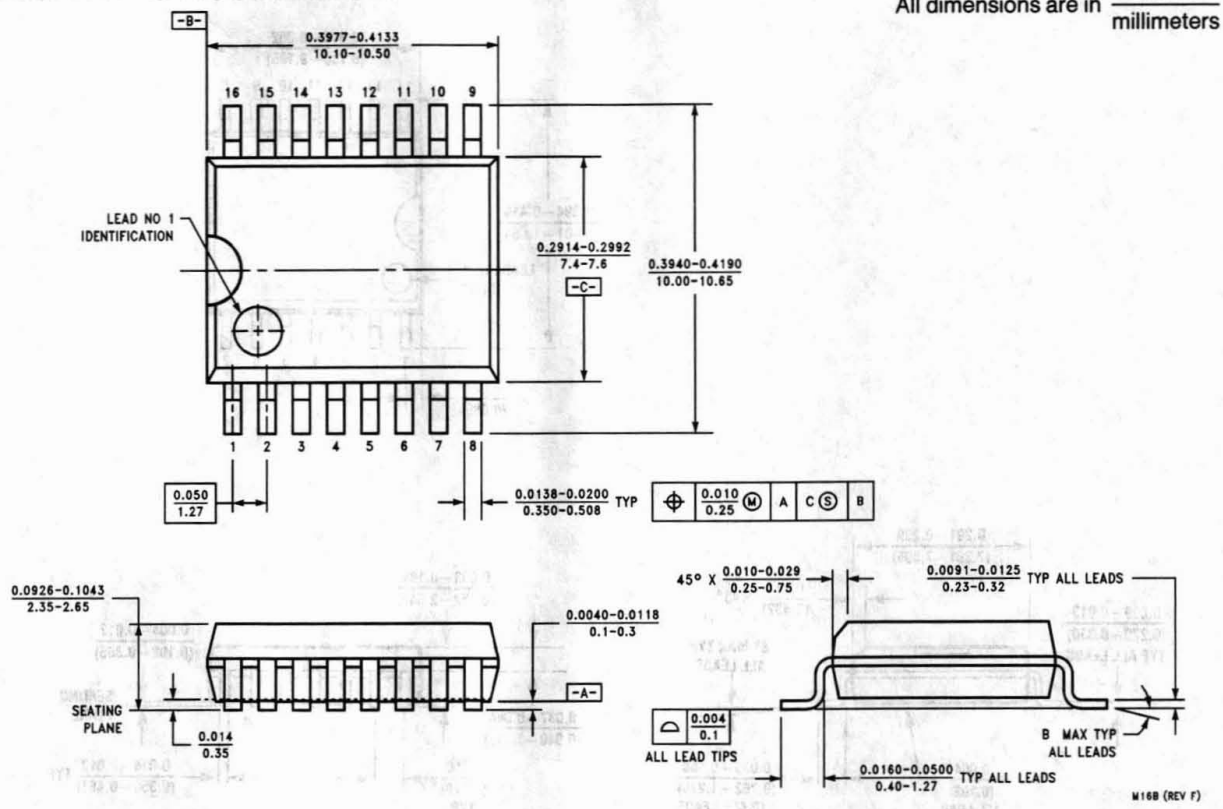
All dimensions are in inches (millimeters)



M16A (REV H)

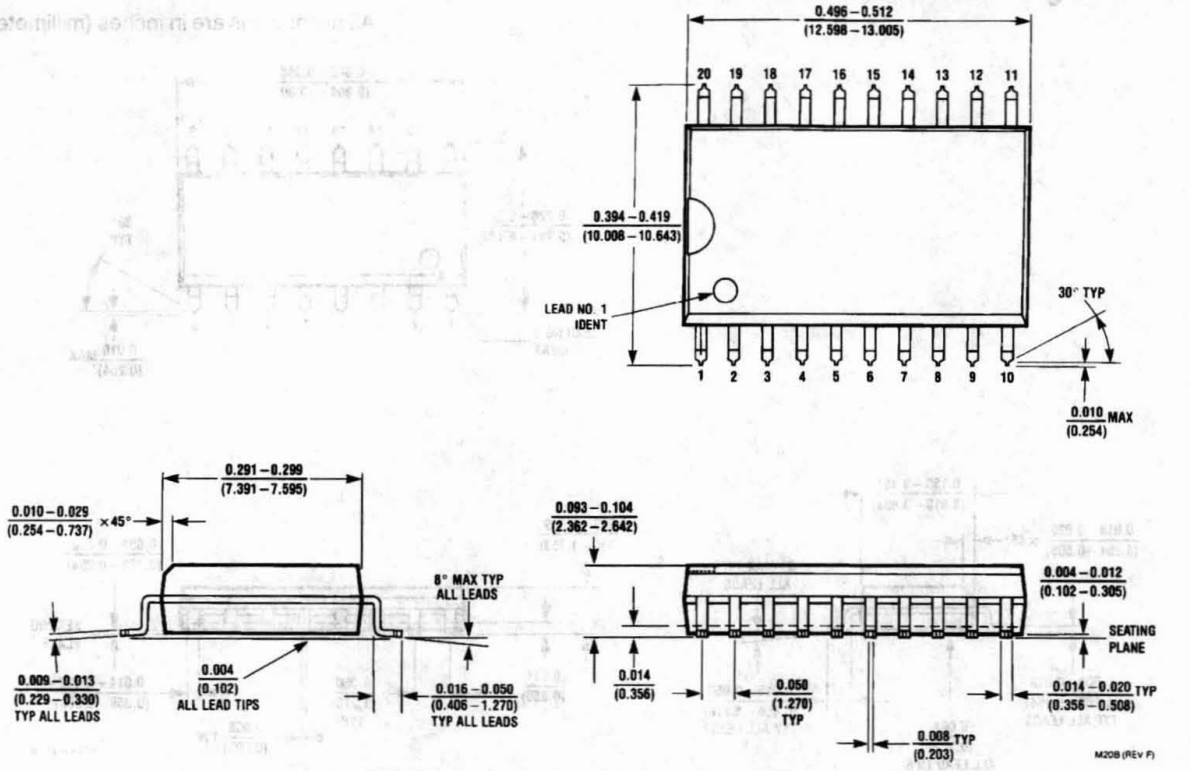
16 Lead (0.300" Wide) Molded Small Outline Package, JEDEC
NS Package Number M16B

All dimensions are in $\frac{\text{inches}}{\text{millimeters}}$



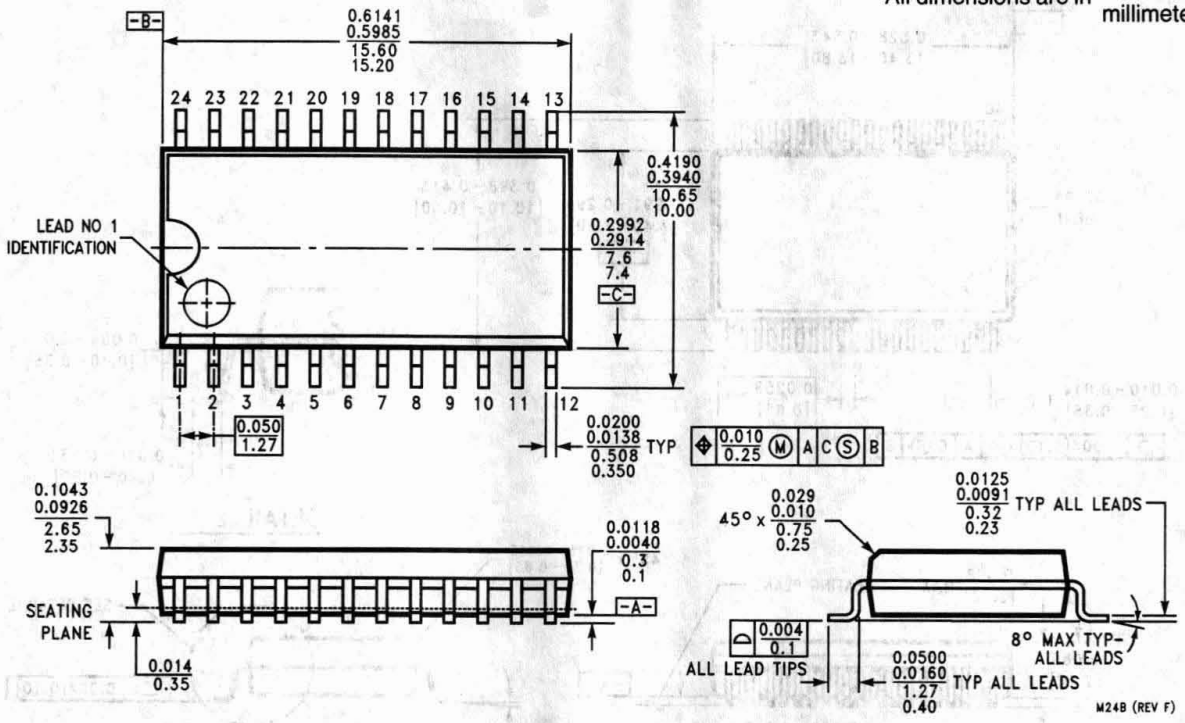
20 Lead (0.300" Wide) Molded Small Outline Package, JEDEC
NS Package Number M20B

All dimensions are in inches (millimeters)



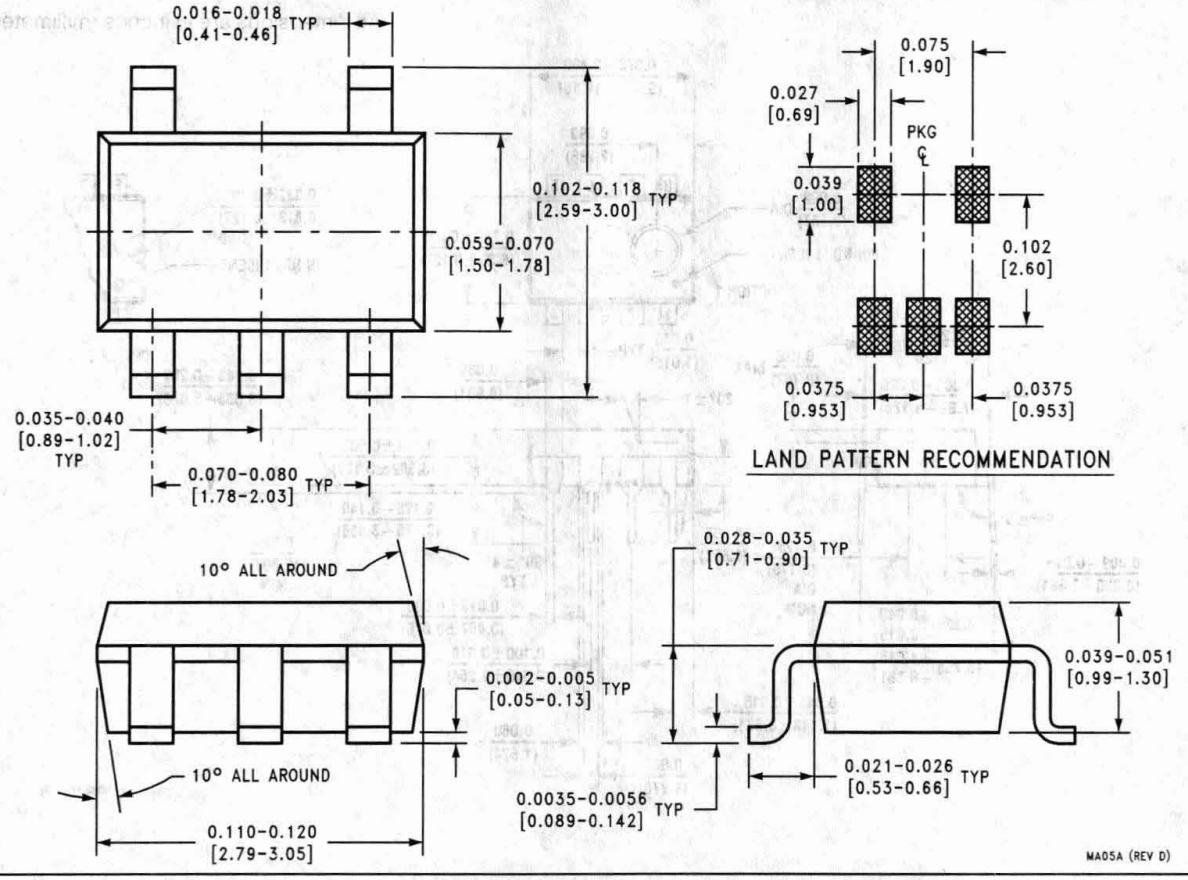
24 Lead (0.300" Wide) Molded Small Outline Package, JEDEC
NS Package Number M24B

All dimensions are in inches / millimeters



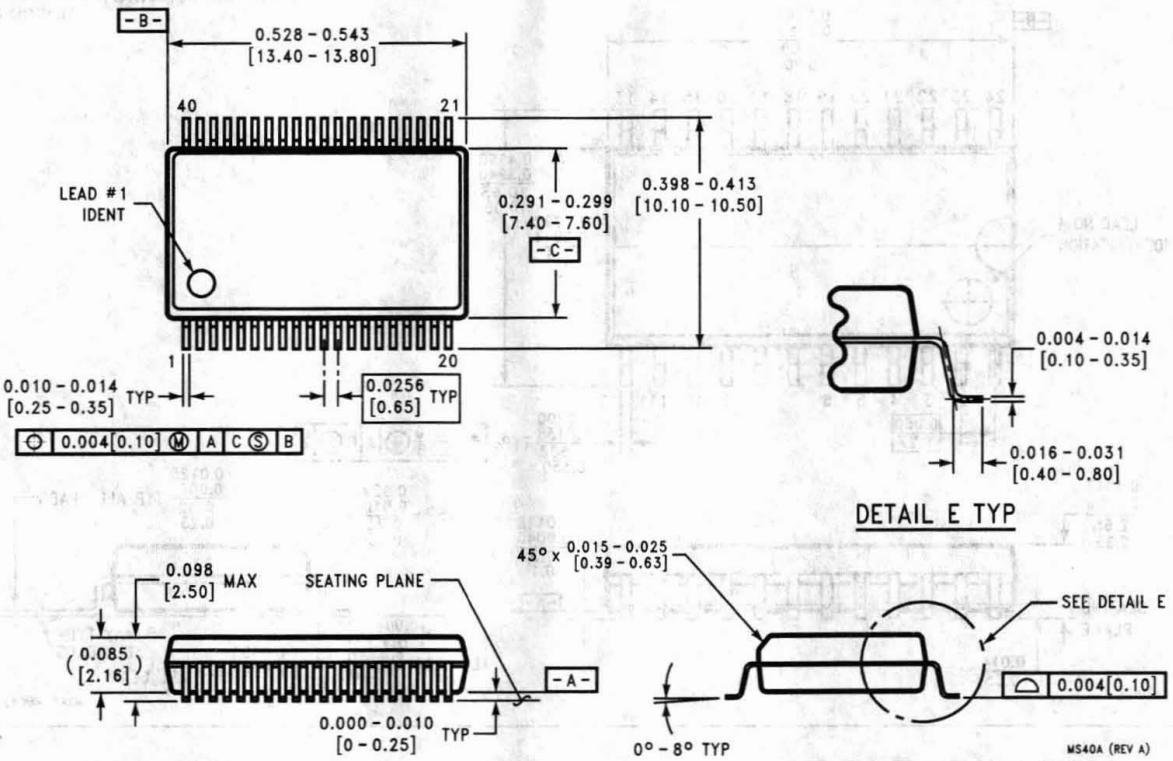
5 Lead Molded SOT-23-5
NS Package Number MA05A

All dimensions are in inches [millimeters]



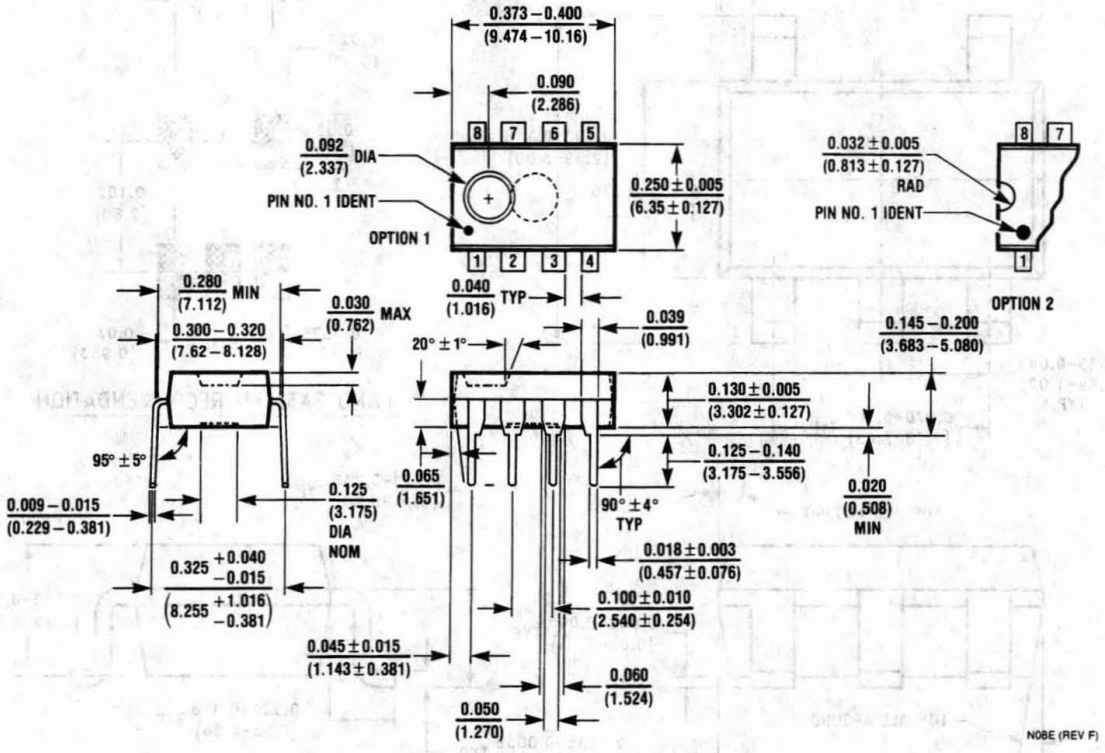
40 Lead Molded Shrink Small Outline Package, EIAJ, Type III
NS Package Number MS40A

All dimensions are in inches [millimeters]



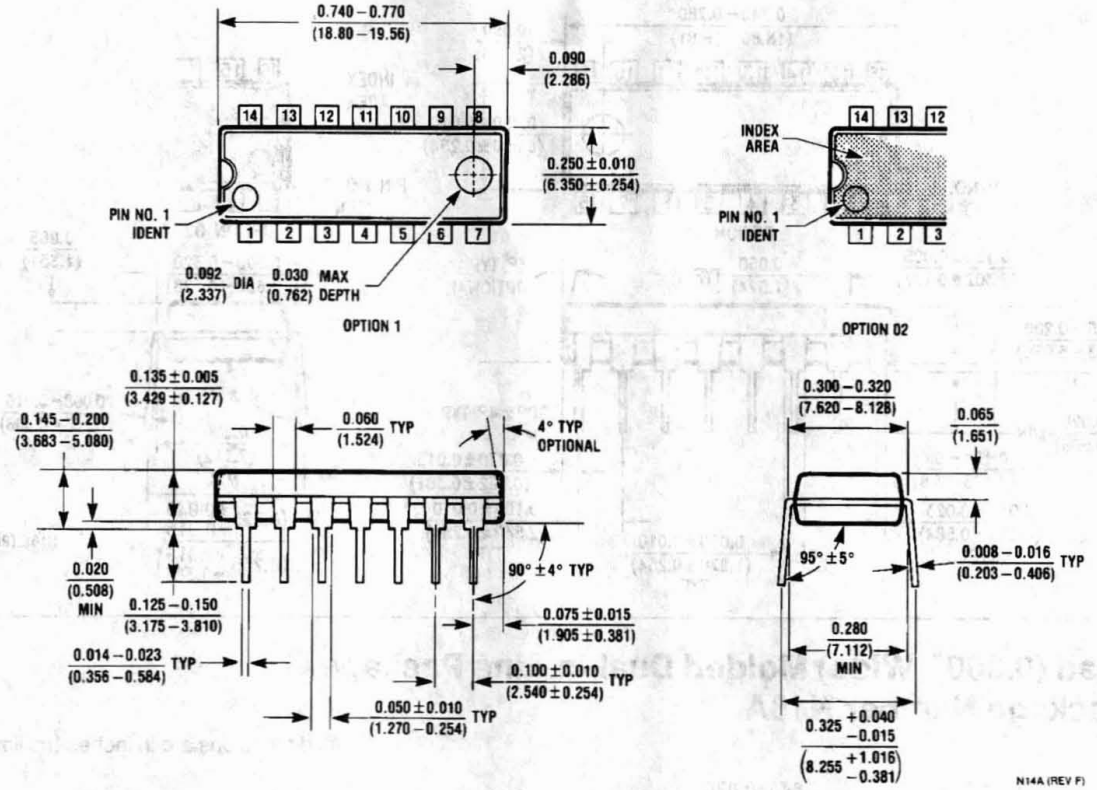
8 Lead (0.300" Wide) Molded Dual-in-Line Package
NS Package Number N08E

All dimensions are in inches (millimeters)



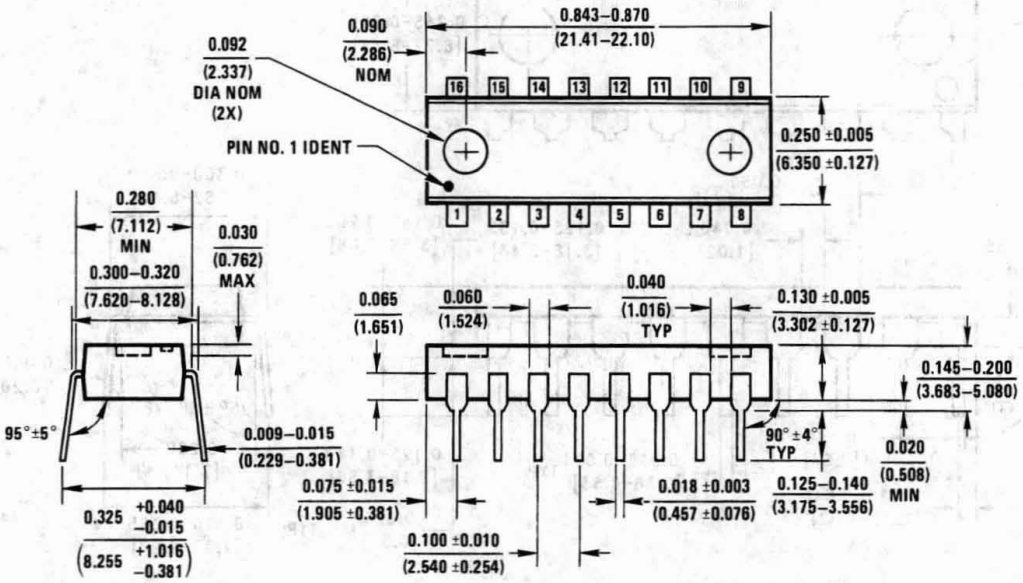
14 Lead (0.300″ Wide) Molded Dual-in-Line Package
NS Package Number N14A

All dimensions are in inches (millimeters)



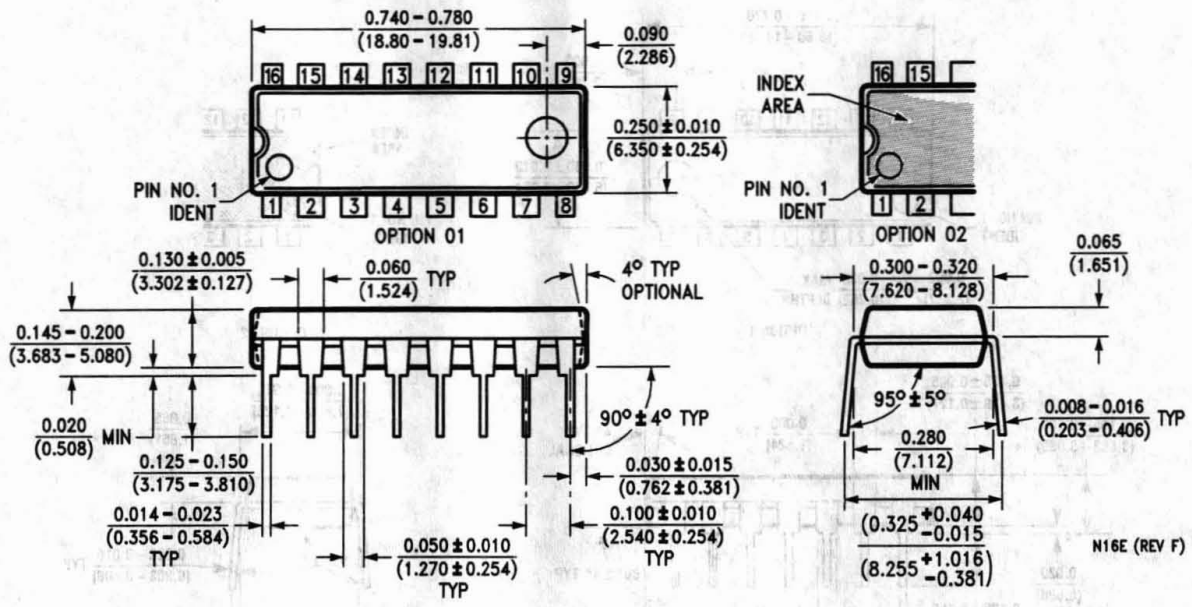
16 Lead (0.300″ Wide) Molded Dual-in-Line Package
NS Package Number N16A

All dimensions are in inches (millimeters)



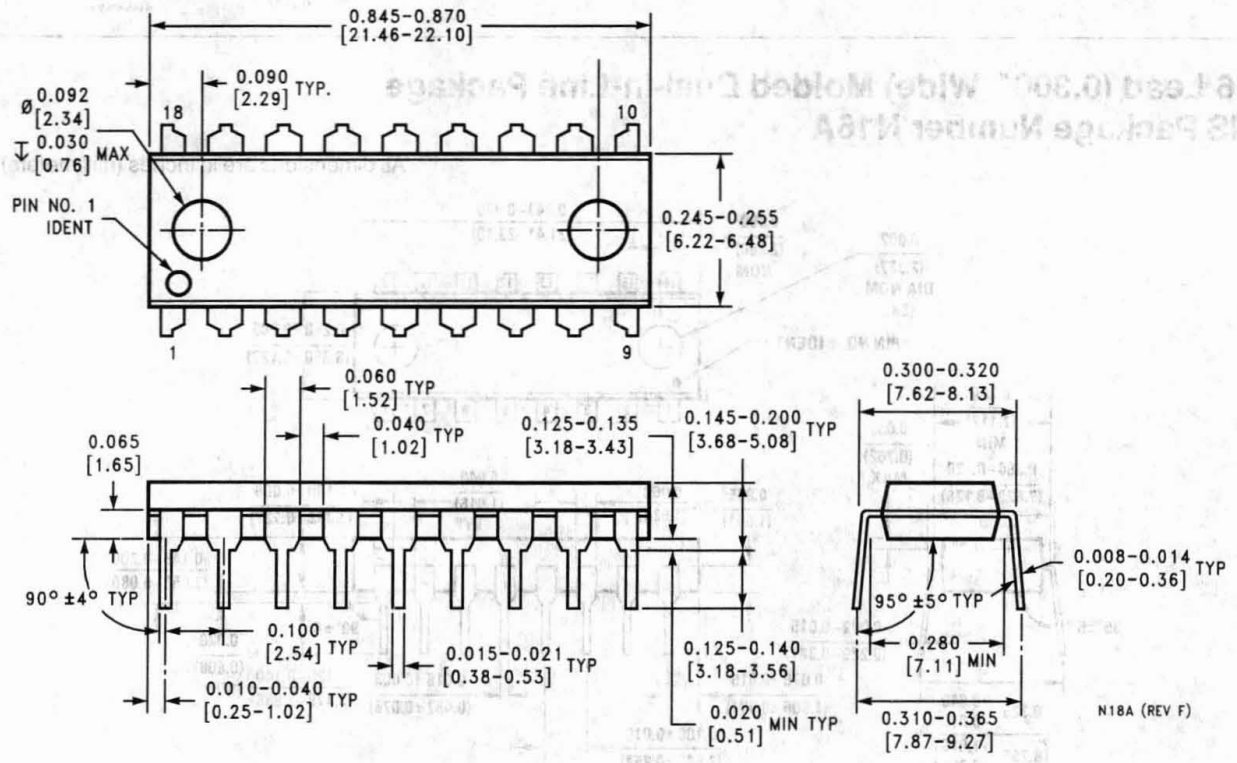
16 Lead (0.300" Wide) Molded Dual-in-Line Package
NS Package Number N16E

All dimensions are in inches (millimeters)



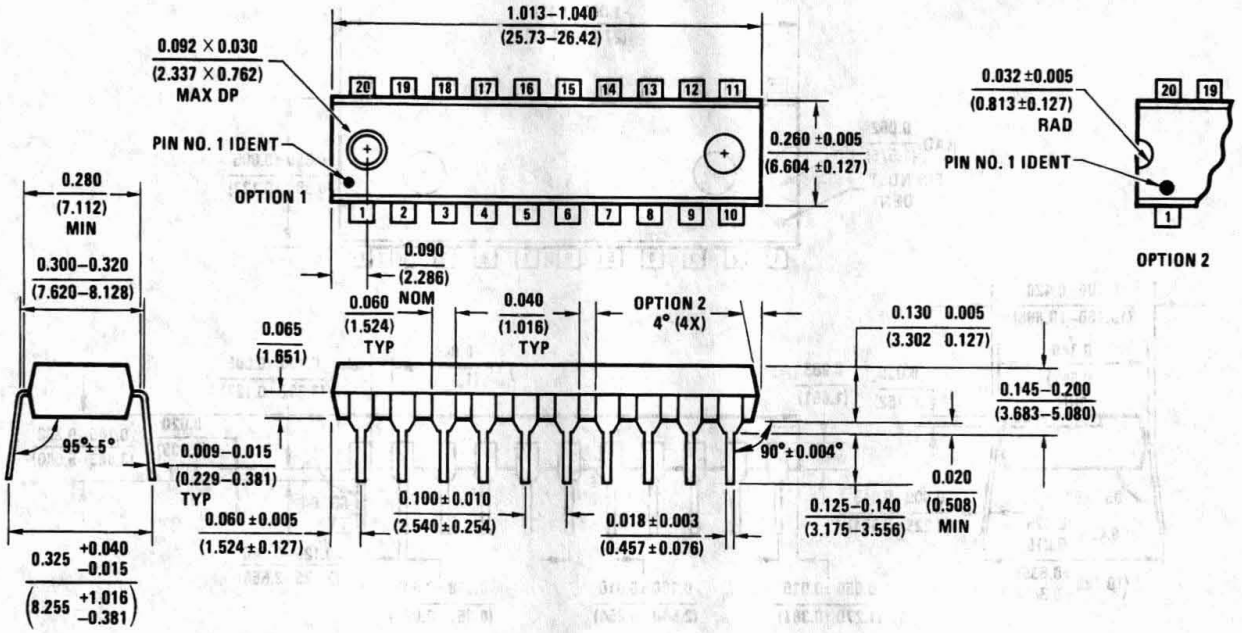
18 Lead (0.300" Wide) Molded Dual-in-Line Package
NS Package Number N18A

All dimensions are in inches [millimeters]



20 Lead (0.300" Wide) Molded Dual-in-Line Package
NS Package Number N20A

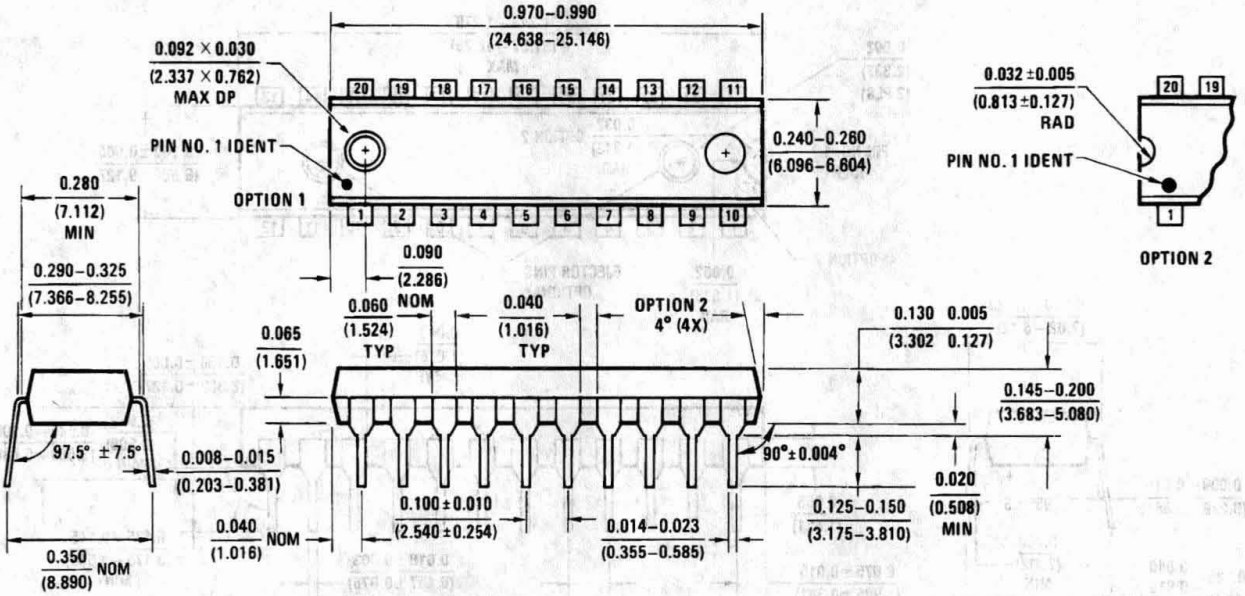
All dimensions are in inches (millimeters)



N20A (REV G)

20 Lead (0.300" Wide) Molded Dual-in-Line Package
NS Package Number N20B

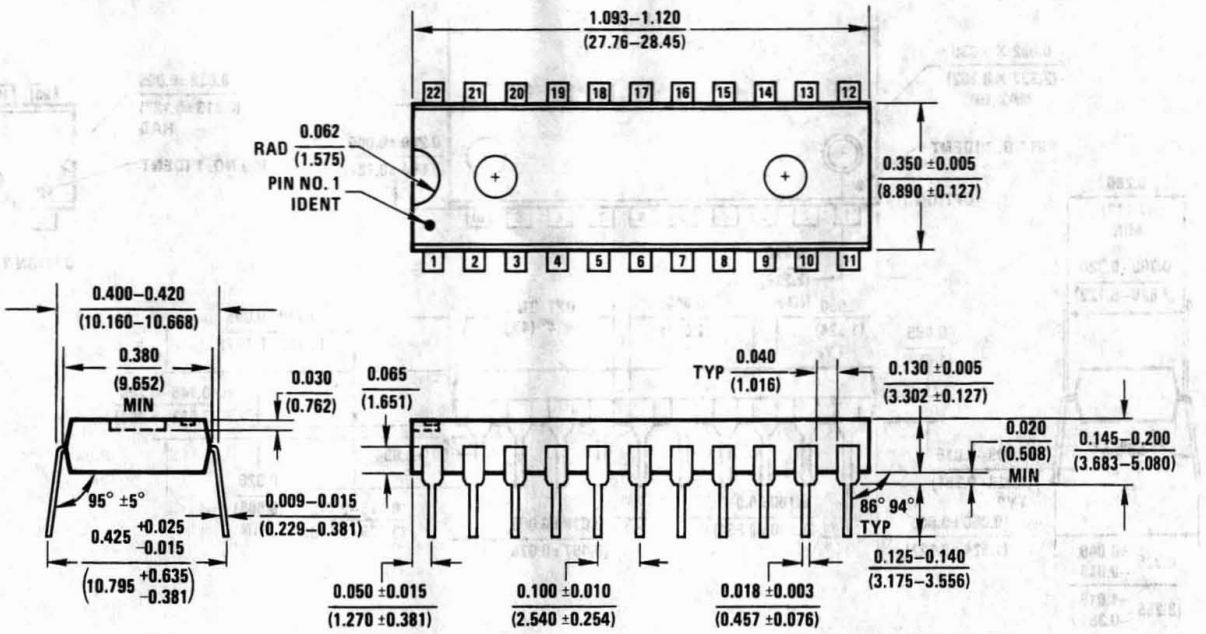
All dimensions are in inches (millimeters)



N20B (REV A)

22 Lead (0.300″ Wide) Molded Dual-in-Line Package
NS Package Number N22A

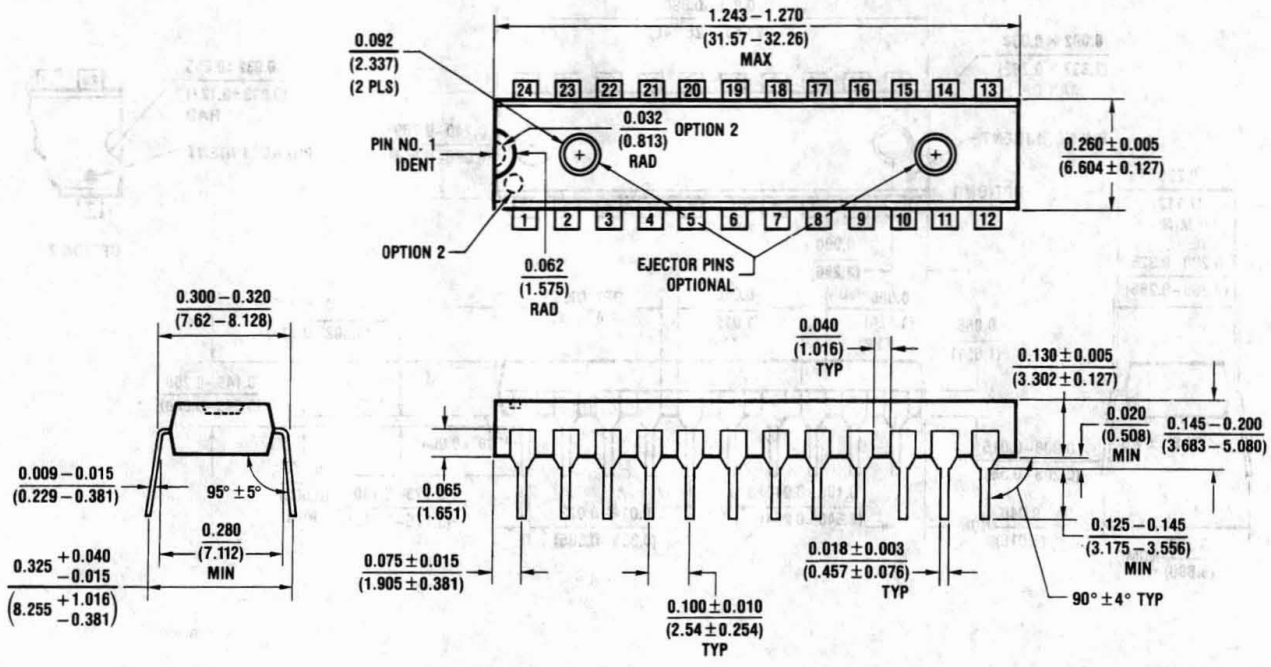
All dimensions are in inches (millimeters)



N22A (REV D)

24 Lead (0.300″ Wide) Molded Dual-in-Line Package
NS Package Number N24C

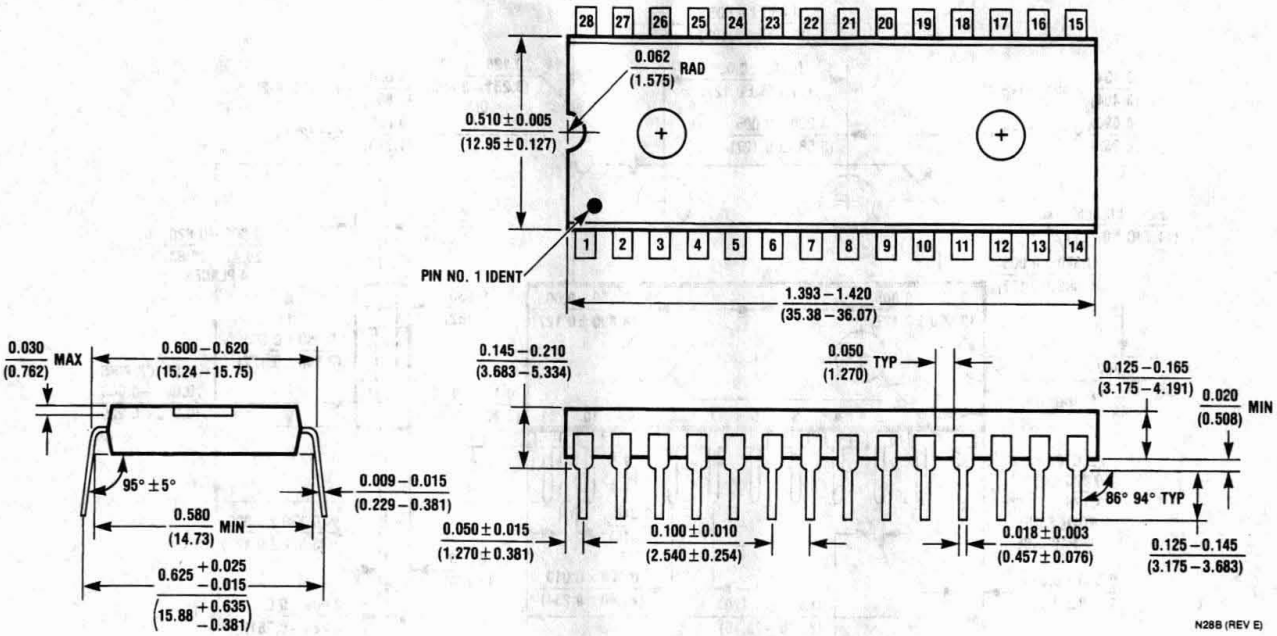
All dimensions are in inches (millimeters)



N24C (REV F)

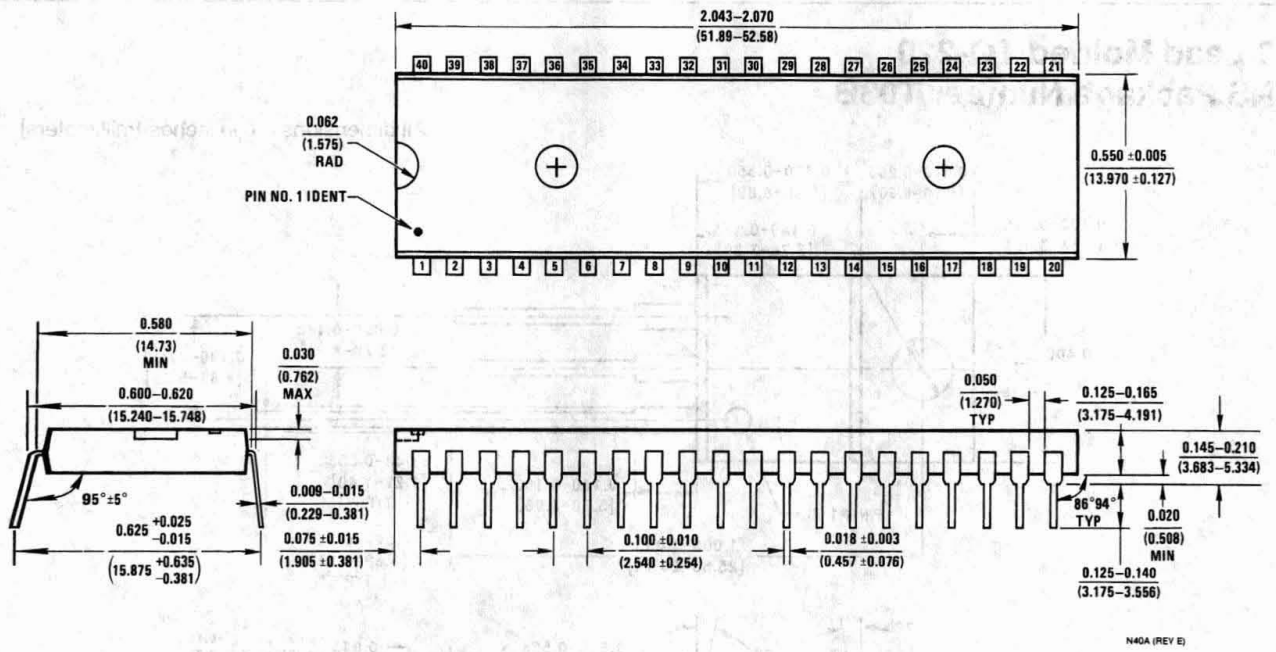
28 Lead (0.600" Wide) Molded Dual-in-Line Package
NS Package Number N28B

All dimensions are in inches (millimeters)



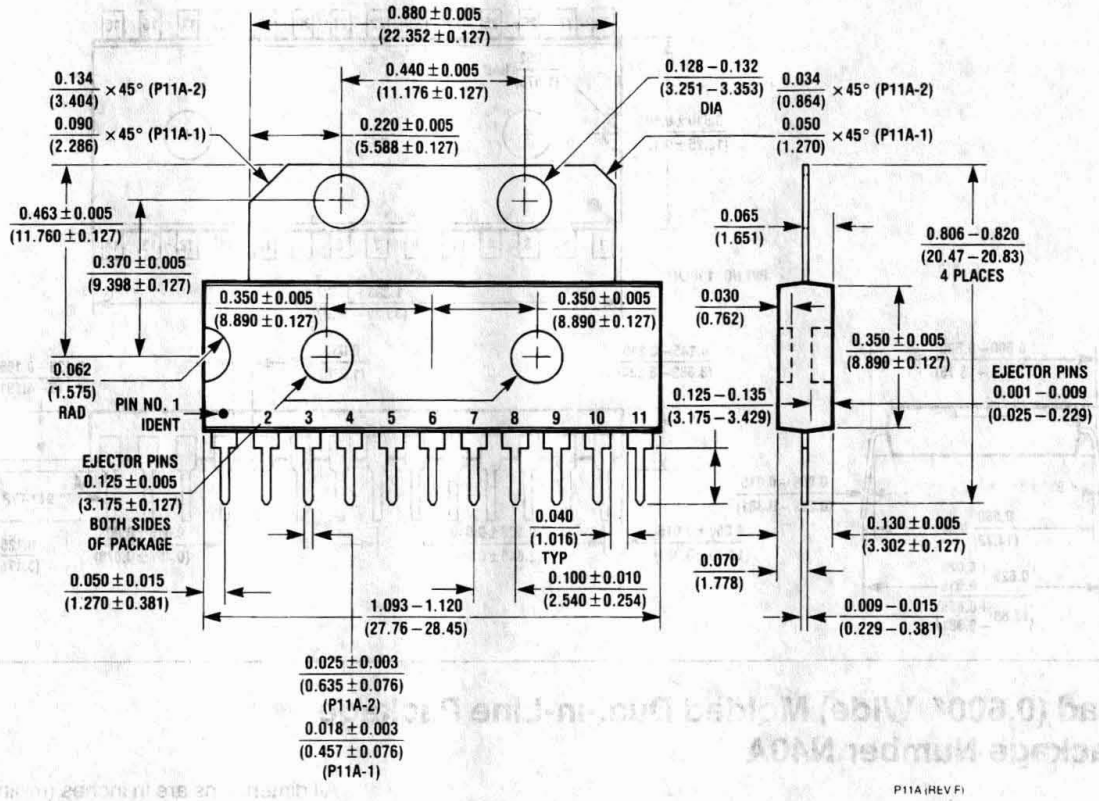
40 Lead (0.600" Wide) Molded Dual-in-Line Package
NS Package Number N40A

All dimensions are in inches (millimeters)



11 Lead Molded TO-202
NS Package Number P11A

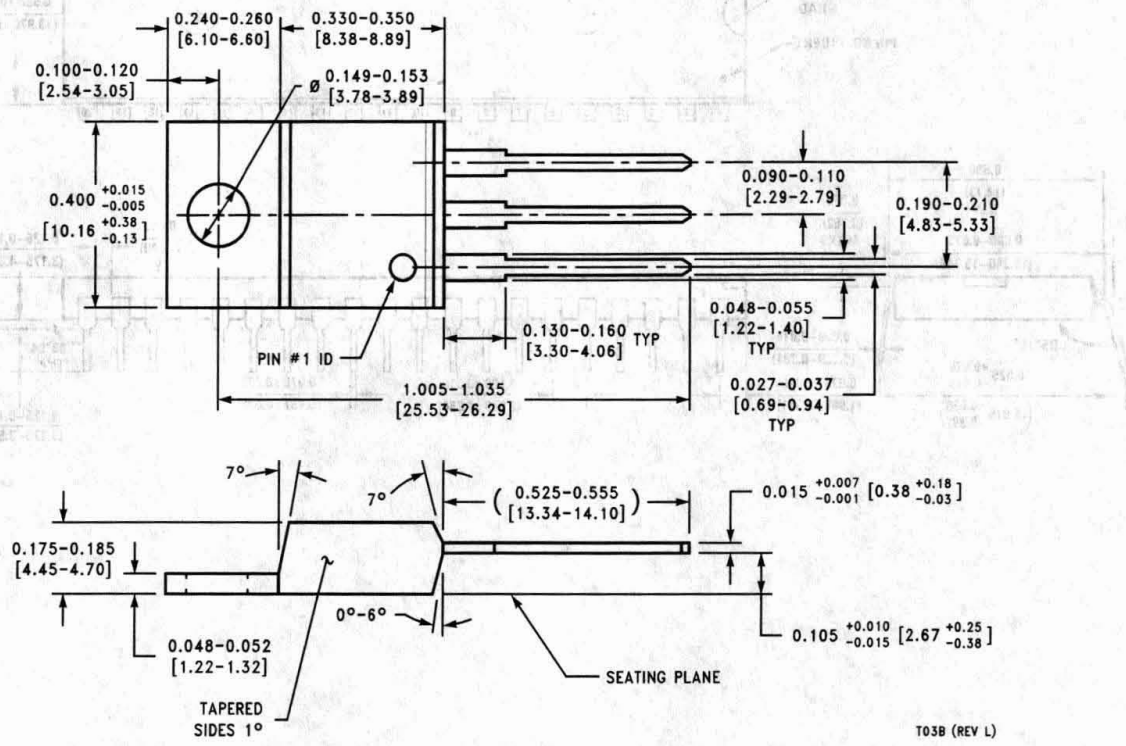
All dimensions are in inches (millimeters)



P11A (REV F)

3 Lead Molded TO-220
NS Package Number T03B

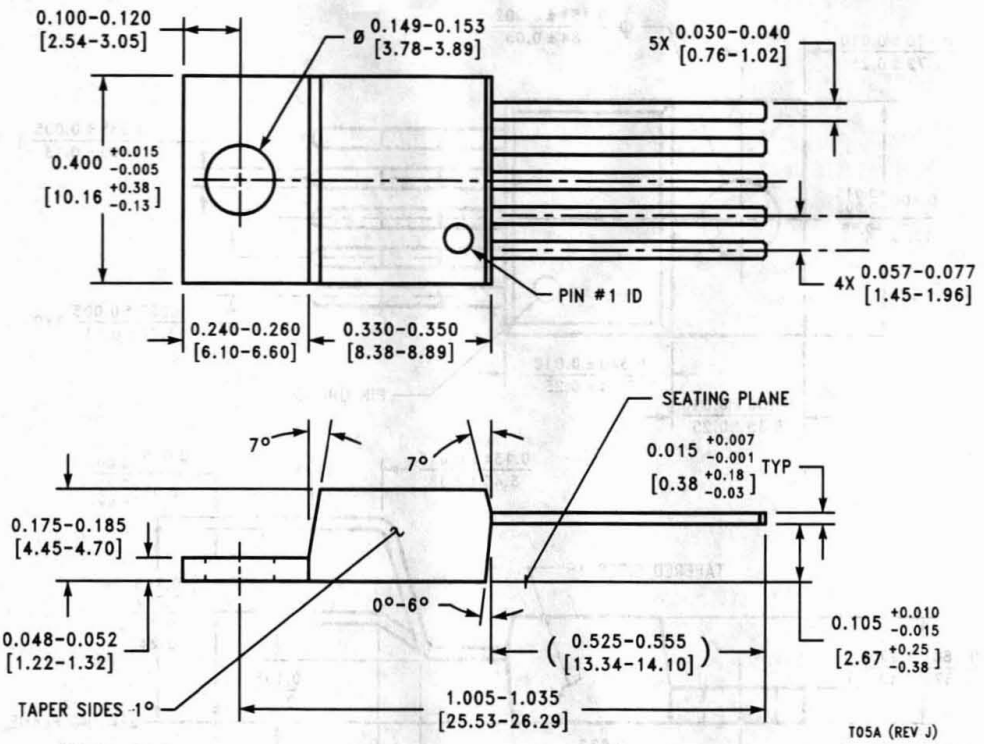
All dimensions are in inches [millimeters]



T03B (REV L)

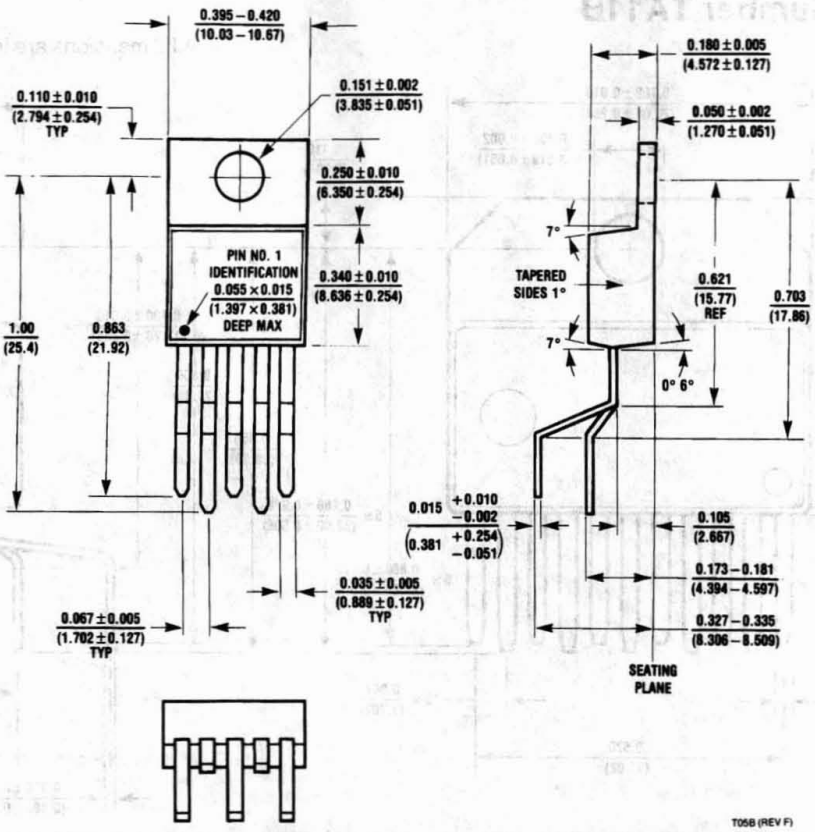
5 Lead Molded TO-220
NS Package Number T05A

All dimensions are in inches [millimeters]



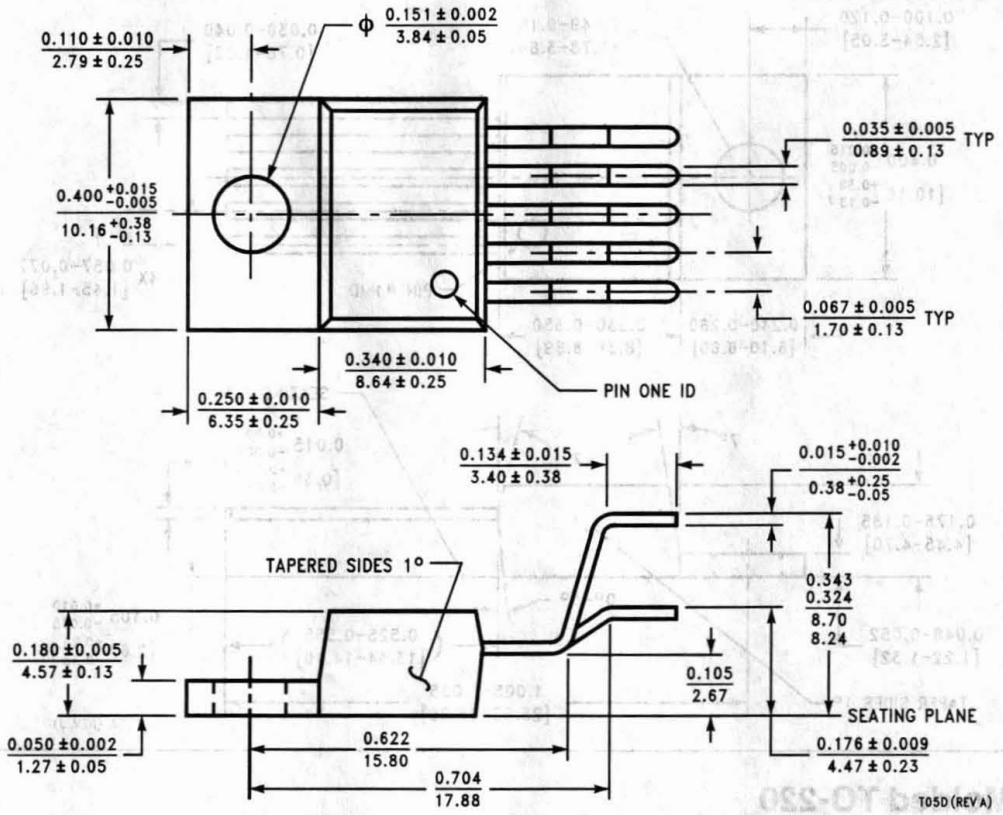
5 Lead Molded TO-220
NS Package Number T05B

All dimensions are in inches (millimeters)



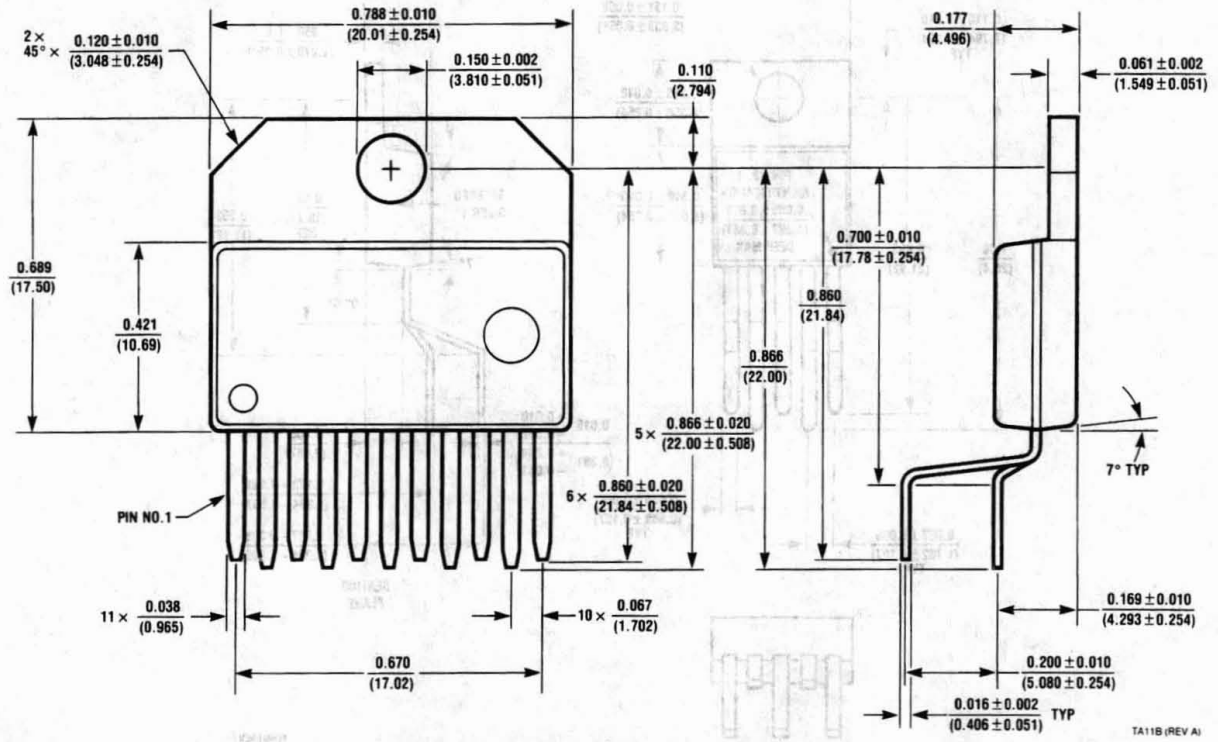
5 Lead Molded TO-220
NS Package Number T05D

All dimensions are in inches / millimeters



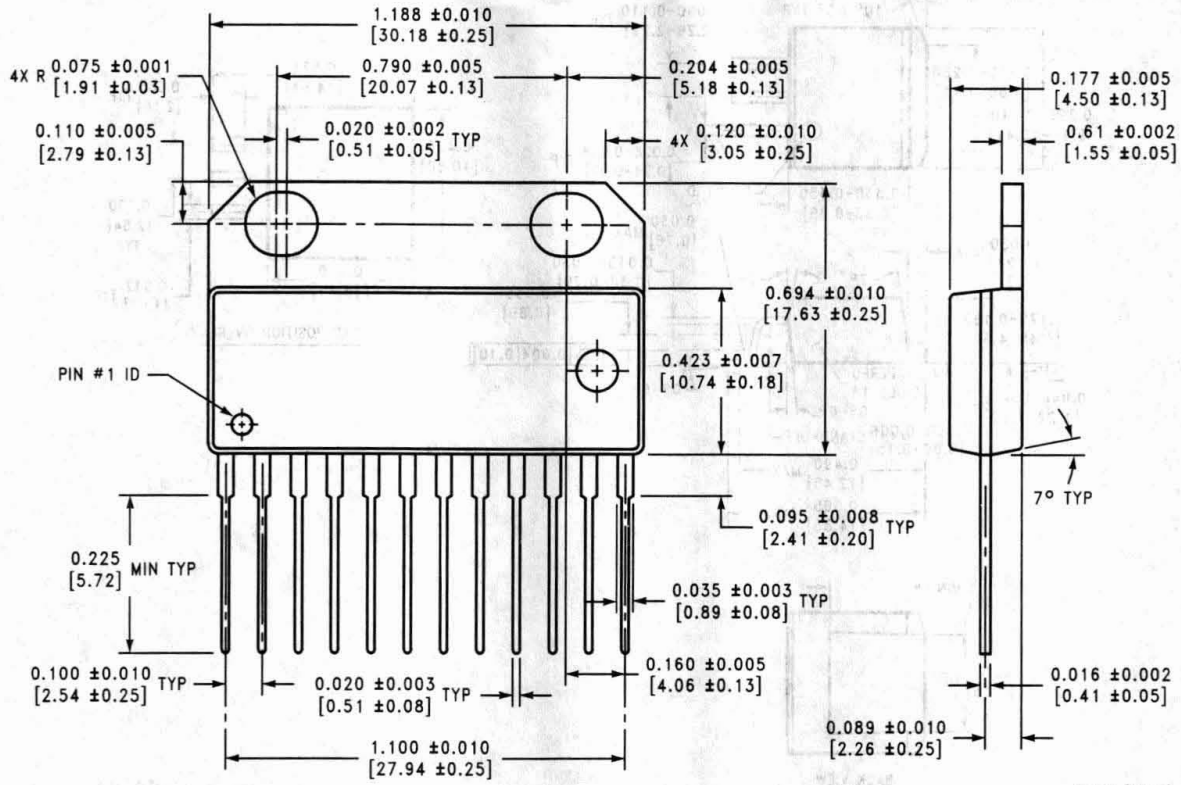
11 Lead Molded TO-220
NS Package Number TA11B

All dimensions are in inches (millimeters)



12 Lead Molded TO-220
NS Package Number TA12A

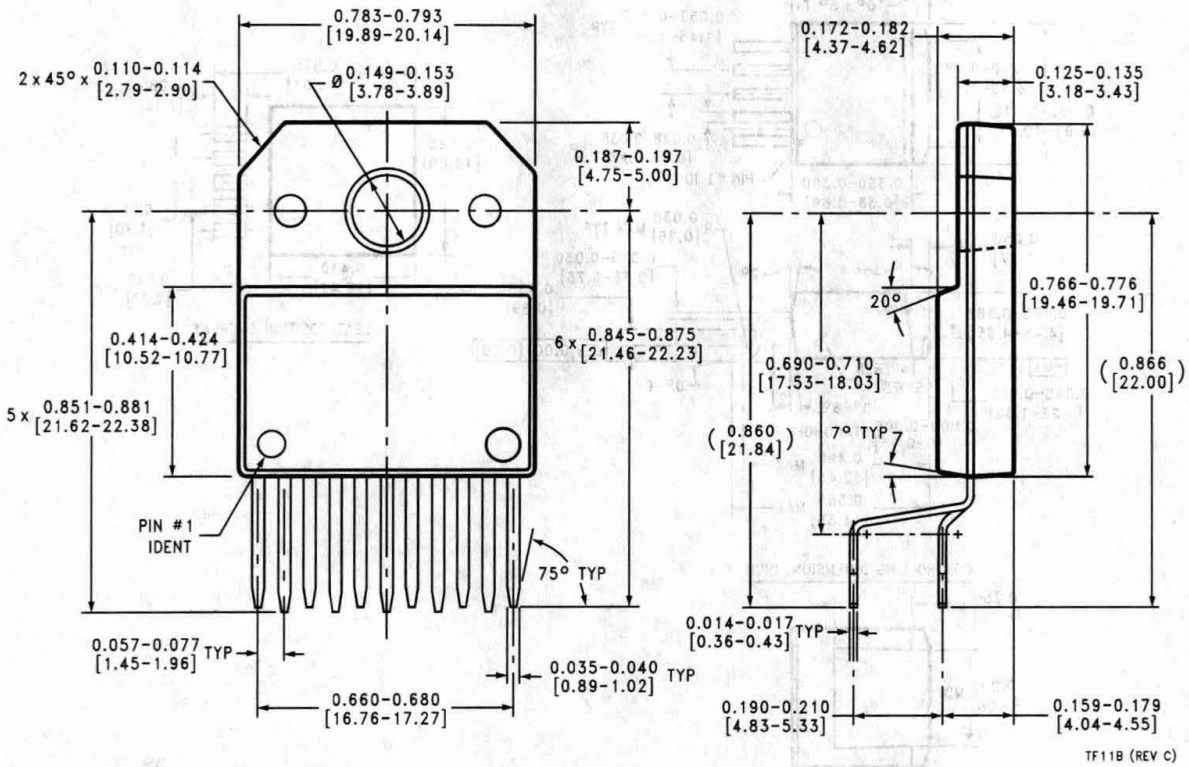
All dimensions are in inches [millimeters]



TA12A (REV B)

11 Lead Molded TO-220
NS Package Number TF11B

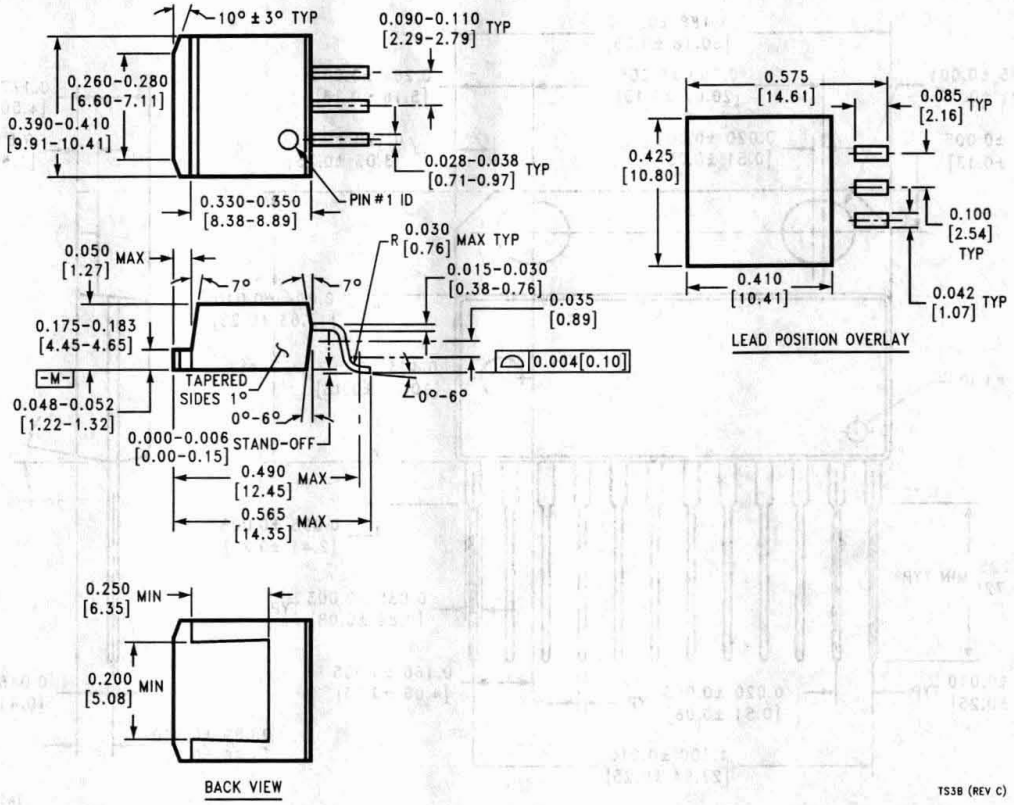
All dimensions are in inches [millimeters]



TF11B (REV C)

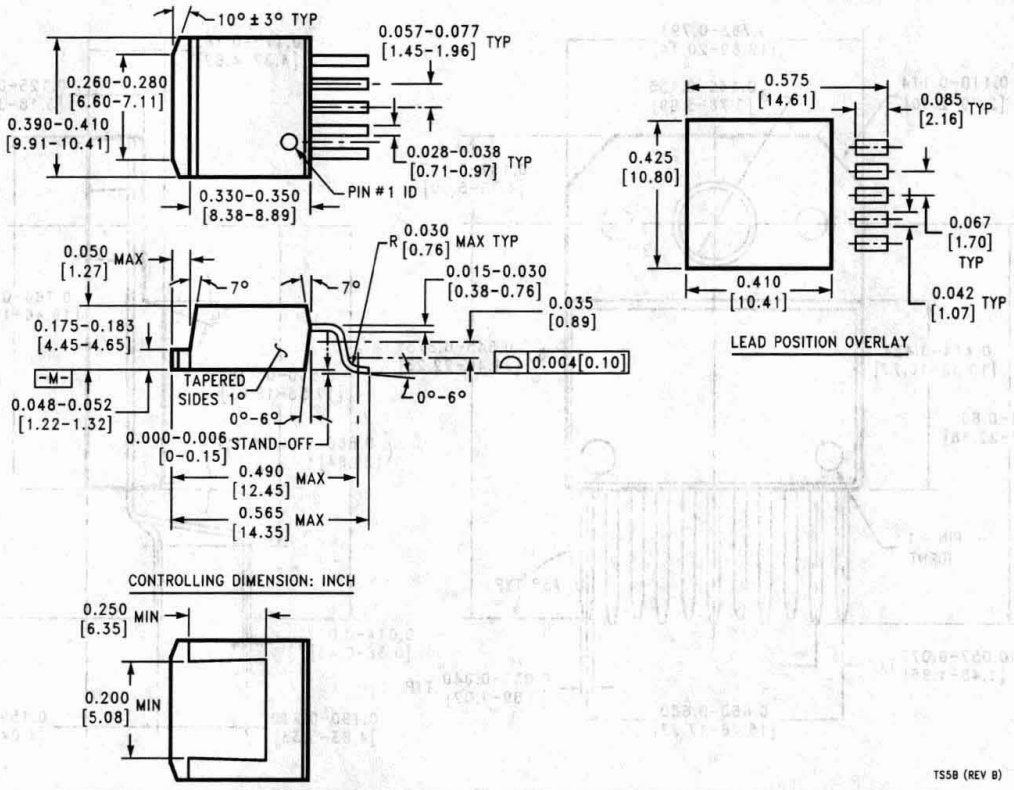
3 Lead Molded TO-263
NS Package Number TS3B

All dimensions are in inches [millimeters]



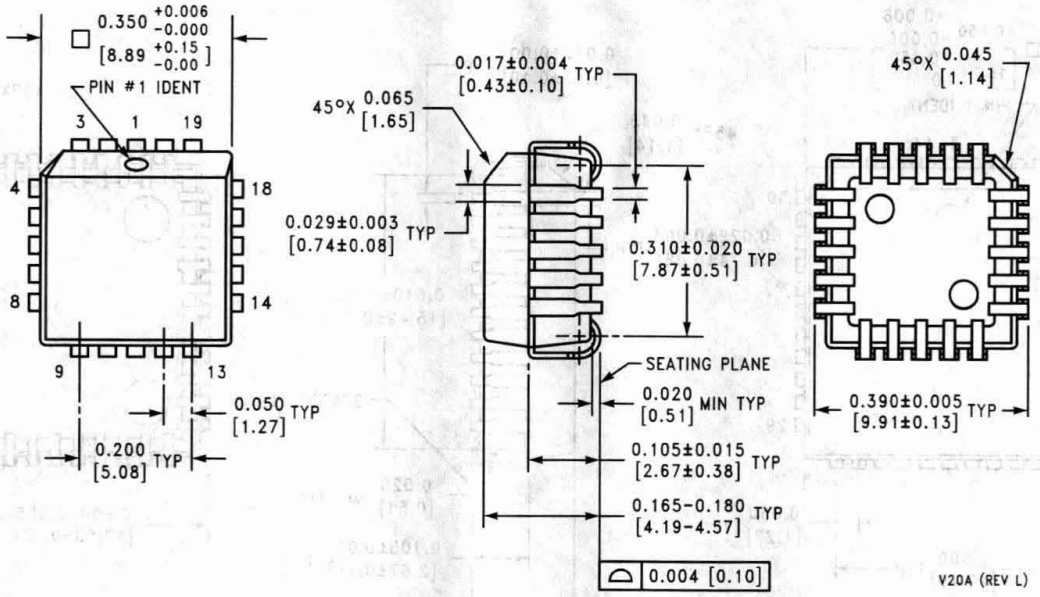
5 Lead Molded TO-263
NS Package Number TS5B

All dimensions are in inches [millimeters]



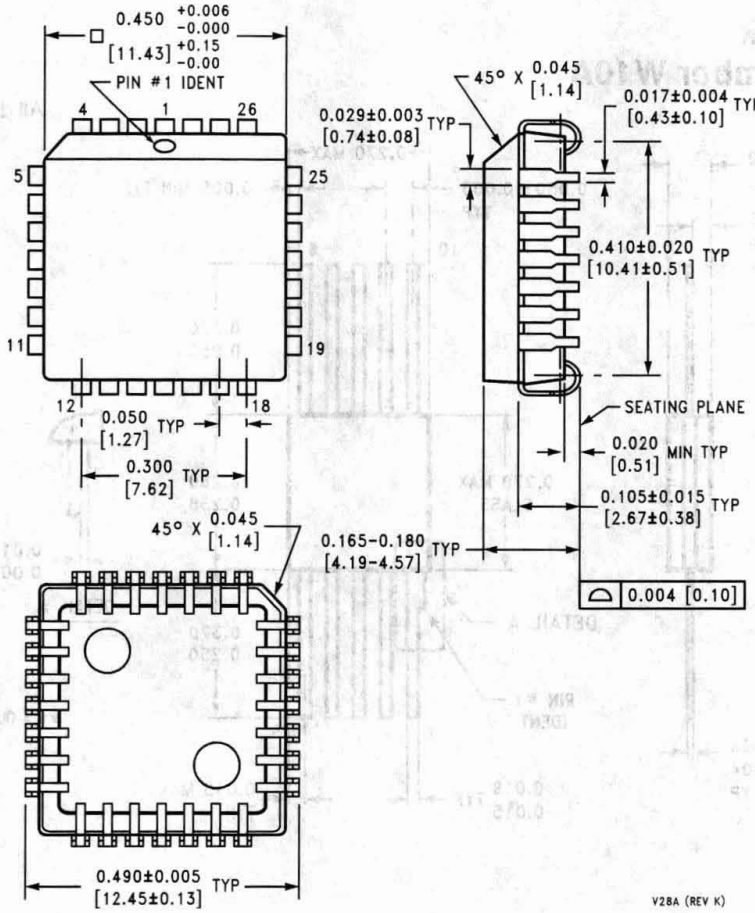
20 Lead Molded Plastic Leaded Chip Carrier
NS Package Number V20A

All dimensions are in inches [millimeters]



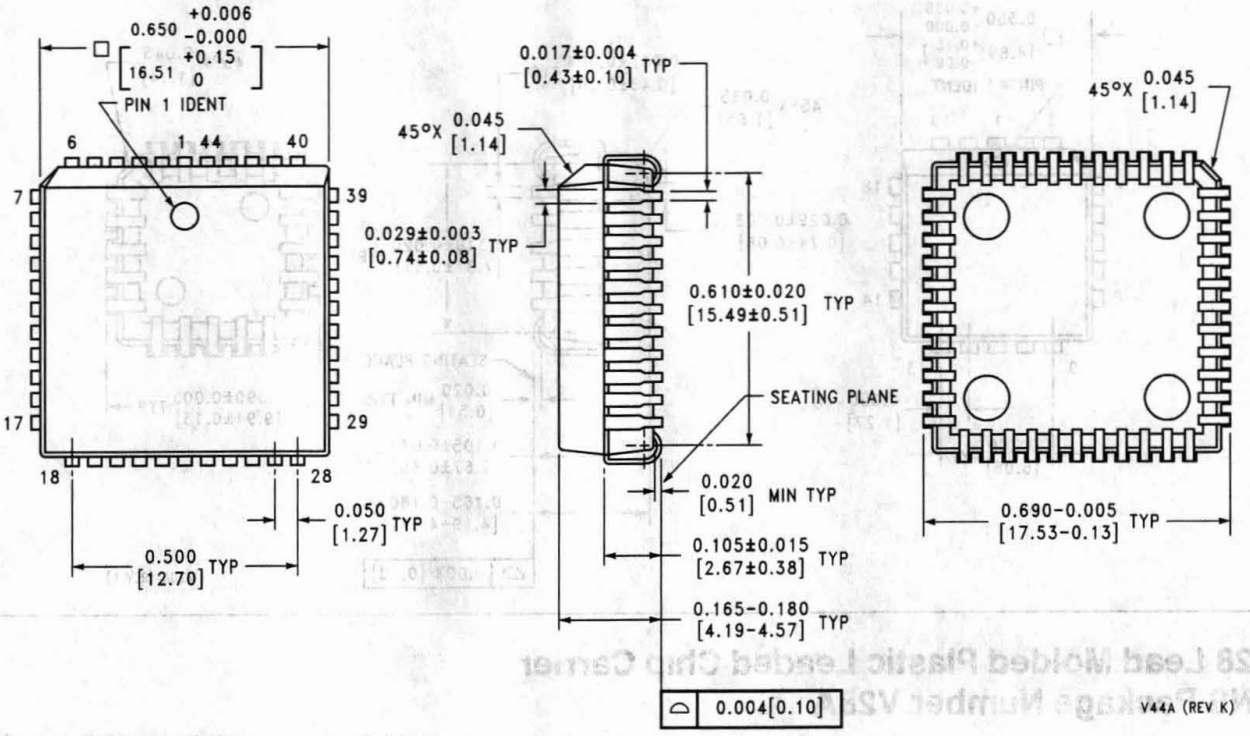
28 Lead Molded Plastic Leaded Chip Carrier
NS Package Number V28A

All dimensions are in inches [millimeters]



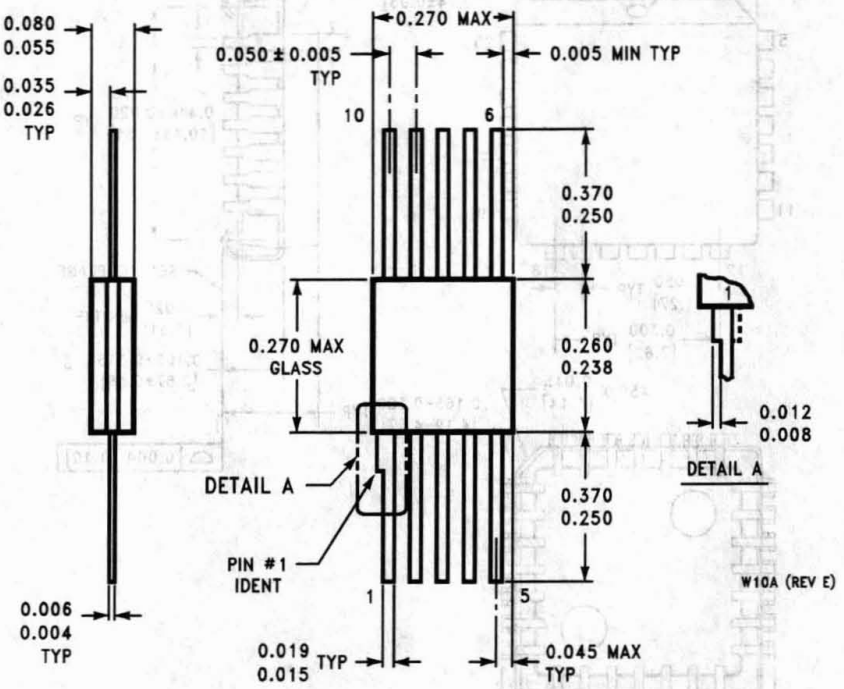
44 Lead Molded Plastic Leaded Chip Carrier
NS Package Number V44A

All dimensions are in inches [millimeters]



10 Lead Cerpack
NS Package Number W10A

All dimensions are in inches



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Temperature Sensors • Active Filters • Analog Switches/Multiplexers • Surface Mount

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Bipolar PNP Transistors • JFET Transistors • Surface Mount Products • Pro-Electron Series
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Microprocessor Applications

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MICROWIRE and MICROWIRE/PLUS Peripherals • Microcontroller Development Tools

FDDI DATABOOK—1994

Datasheets • Application Notes

F100K ECL LOGIC DATABOOK & DESIGN GUIDE—1992

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Power Distribution and Thermal Considerations • Testing Techniques • 300 Series Package Qualification
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Design Considerations • 54AC/74ACXXX • 54ACT/74ACTXXX • Quiet Series: 54ACQ/74ACQXXX
Quiet Series: 54ACTQ/74ACTQXXX • 54FCT/74FCTXXX • FCTA: 54FCTXXXA/74FCTXXXA/B

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LINEAR APPLICATIONS HANDBOOK—1994

The purpose of this handbook is to provide a fully indexed and cross-referenced collection of linear integrated circuit applications using both monolithic and hybrid circuits from National Semiconductor.

Individual application notes are normally written to explain the operation and use of one particular device or to detail various methods of accomplishing a given function. The organization of this handbook takes advantage of this innate coherence by keeping each application note intact, arranging them in numerical order, and providing a detailed Subject Index.

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LOW VOLTAGE DATABOOK—1992

This databook contains information on National's expanding portfolio of low and extended voltage products. Product datasheets included for: Low Voltage Logic (LVQ), Linear, EPROM, EEPROM, SRAM, Interface, ASIC, Embedded Controllers, Real Time Clocks, and Clock Generation and Support (CGS).

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Radiation Environment • Electrostatic Discharge • Discrete Device • Standardization
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Other IEEE 1149.1 Devices

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VHC/VHCT ADVANCED CMOS LOGIC DATABOOK—1993

This databook introduces National's Very High Speed CMOS (VHC) and Very High Speed TTL Compatible CMOS (VHCT) designs. The databook includes Description and Family Characteristics • Ratings, Specifications and Waveforms Design Considerations and Product Datasheets. The topics discussed are the advantages of VHC/VHCT AC Performance, Low Noise Characteristics and Improved Interface Capabilities.

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